TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73S8009R

Demo Board User Manual

May 7, 2010
Rev. 1.2
UM_8009R_065

Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

Table of Contents

Figures

Tables

1 Introduction

The Teridian Semiconductor Corporation 73S8009R Demo Board is a platform for evaluating the Teridian 73S8009R Smart Card Interface IC. It incorporates the 73S8009R integrated circuit and it is designed to operate either as a standalone platform (to be used in conjunction with an external microcontroller) or as a daughter card to be used in conjunction with the 73S12xxF evaluation platform.

1.1 Package Contents

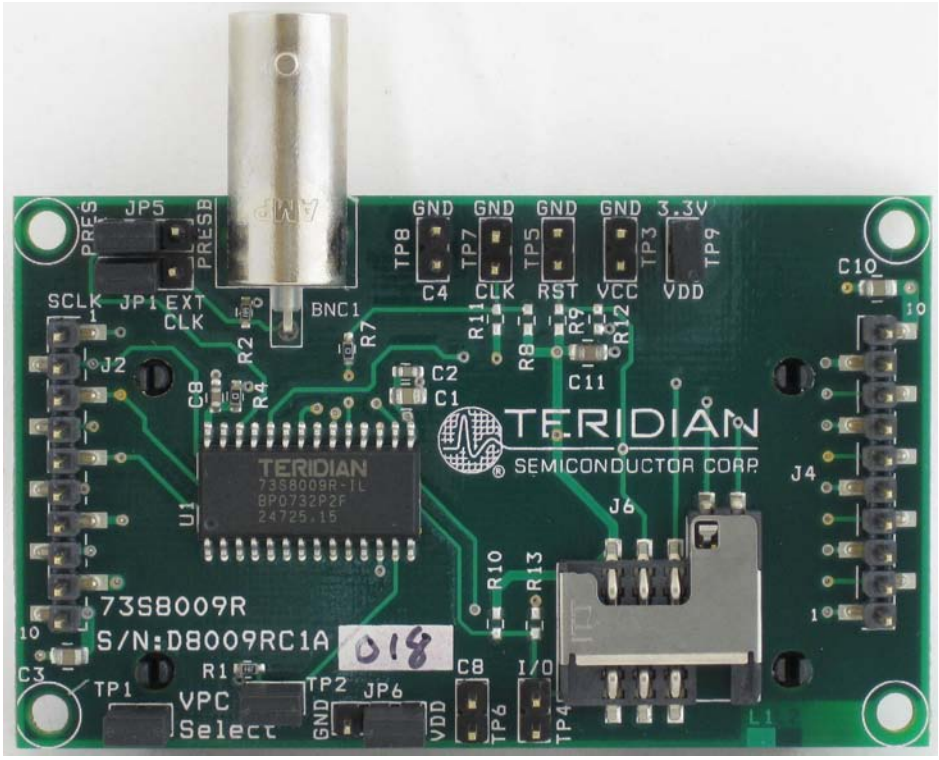

Figure 1: 73S8009R Demo Board

The 73S8009R Demo Board Kit includes:

- A 73S8009R Demo Board (Rev. 1)
- The following documents:
  - *73S8009R Data Sheet*
  - *73S8009R Demo Board User Manual* (this document)

1.2 Safety and ESD Notes

Connecting live voltages to the 73S8009R Demo Board system will result in potentially hazardous voltages on the boards.

Extreme caution should be taken when handling the 73S8009R Demo Board after connection to live voltages!

The 73S8009R Demo Board is ESD sensitive! ESD precautions should be taken when handling this board!

1.3 Recommended Operating Conditions and Absolute Maximum Ratings

Table 1: Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 3.6 VDC
Supply Voltage V_{PC}	4.75 to 5.5 VDC (ISO-7816 and EMV applications) 4.85 V to 5.5 VDC (NDS applications)
Ambient Operating Temperature	-40 °C to +85 °C
Input Voltage for Digital Inputs	0 V to V_{DD} + 0.3 V

Table 2: Absolute Maximum Ratings

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 4.0 VDC
Supply Voltage V_{PC}	-0.5 to 6.5 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD}+0.5) VDC
Storage Temperature	-60 to 150 °C
Pin Voltage (except card interface)	-0.3 to (V_{DD}+0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC}+0.5) VDC
Pin Current	± 100 mA
ESD Tolerance – Card interface pins	± 6 kV
ESD Tolerance – Other pins	± 2 kV

Operation outside these rating limits may cause permanent damage to the device.

ESD testing on Card pins is HBM condition, 3 pulses, each polarity referenced to ground.

2 Connections

This section describes the 73S8009R Demo Board external connectors. All the digital signals and power supply connections are made through 10-pin header connectors labeled J2 and J4 in Figure 2.

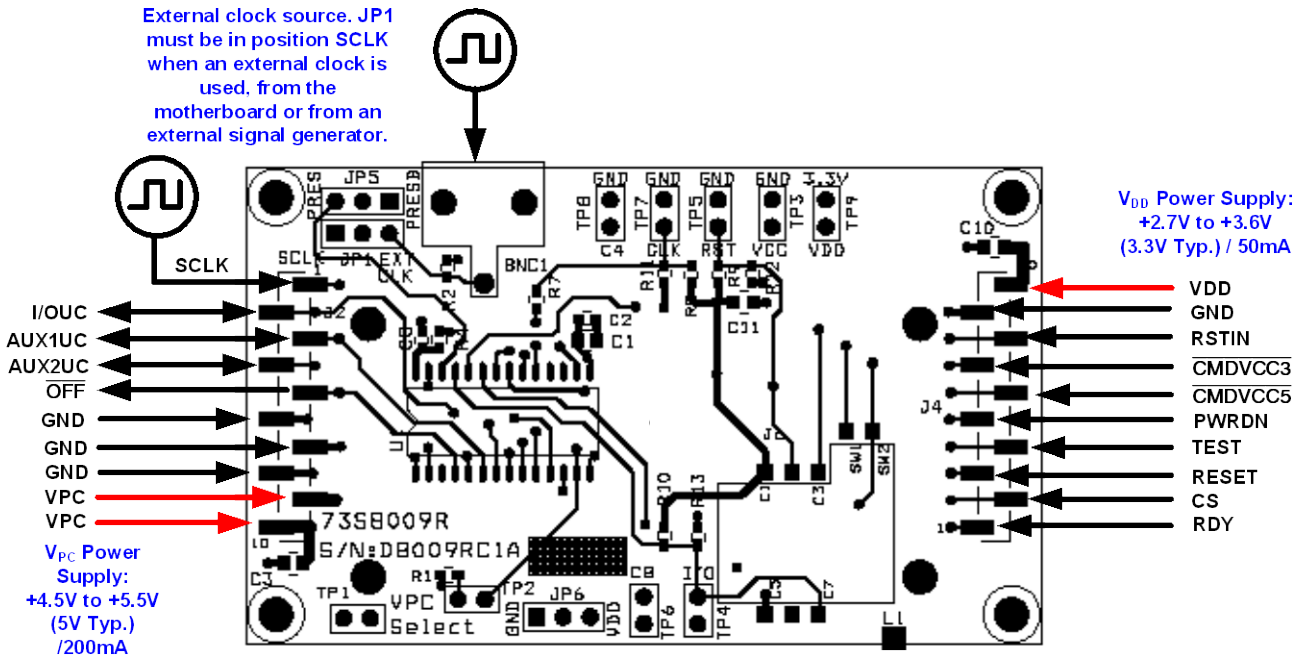

Figure 2: 73S8009R Demo Board External Connectors

Table 3 describes the pins for the J4 connector.

Table 3: J4 Pin Descriptions

Pin	Pin Name	Function
1	RDY	Indicates when smart card power supply is stable and ready.
2	CS	Chip Select – active high.
3	RESET	
4	TEST	
5	PWRDN	
6	$\overline{\text{CMDVCC5}}$	Controls the turn-on, output voltage value, and turn-off of V_{CC}.
7	$\overline{\text{CMDVCC3}}$	
8	RSTIN	Controls the card reset signal.
9	GND	Ground.
10	VDD	System interface supply voltage and supply voltage for companion controller circuitry.

Table 4 describes the J2 connector pins.

Table 4: J2 Pin Descriptions

Pin	Pin Name	Function
1	SCLK	Clock source input.
2	I/OUC	System controller data I/O to/from the card.
3	AUX1UC	System controller auxiliary data C4 to/from the card.
4	AUX2UC	System controller auxiliary data C8 to/from the card.
5	$\overline{OFF}$	Interrupt signal to the processor. Indicator of card presence and any card fault conditions.
6	GND	Ground.
7	GND	Ground.
8	GND	Ground.
9	VPC IN	Must be between 2.7 V and 6.5 V.
10	VPC IN	Must be between 2.7 V and 6.5 V.

Connections should be made in this order:

- Power Supplies: Apply 3.3 V to pin 10 of J4 or 5 V to pins 9 and 10 of J2 depending on the setting of JP2.
- Press the ON/OFF button.
- Control signals to the device can be connected through J2 and J4. See Figure 2 and Figure 4.
- Apply the clock signal.

3 Jumpers, Switches and Test Points

The items marked in Figure 3 are described in Table 5.

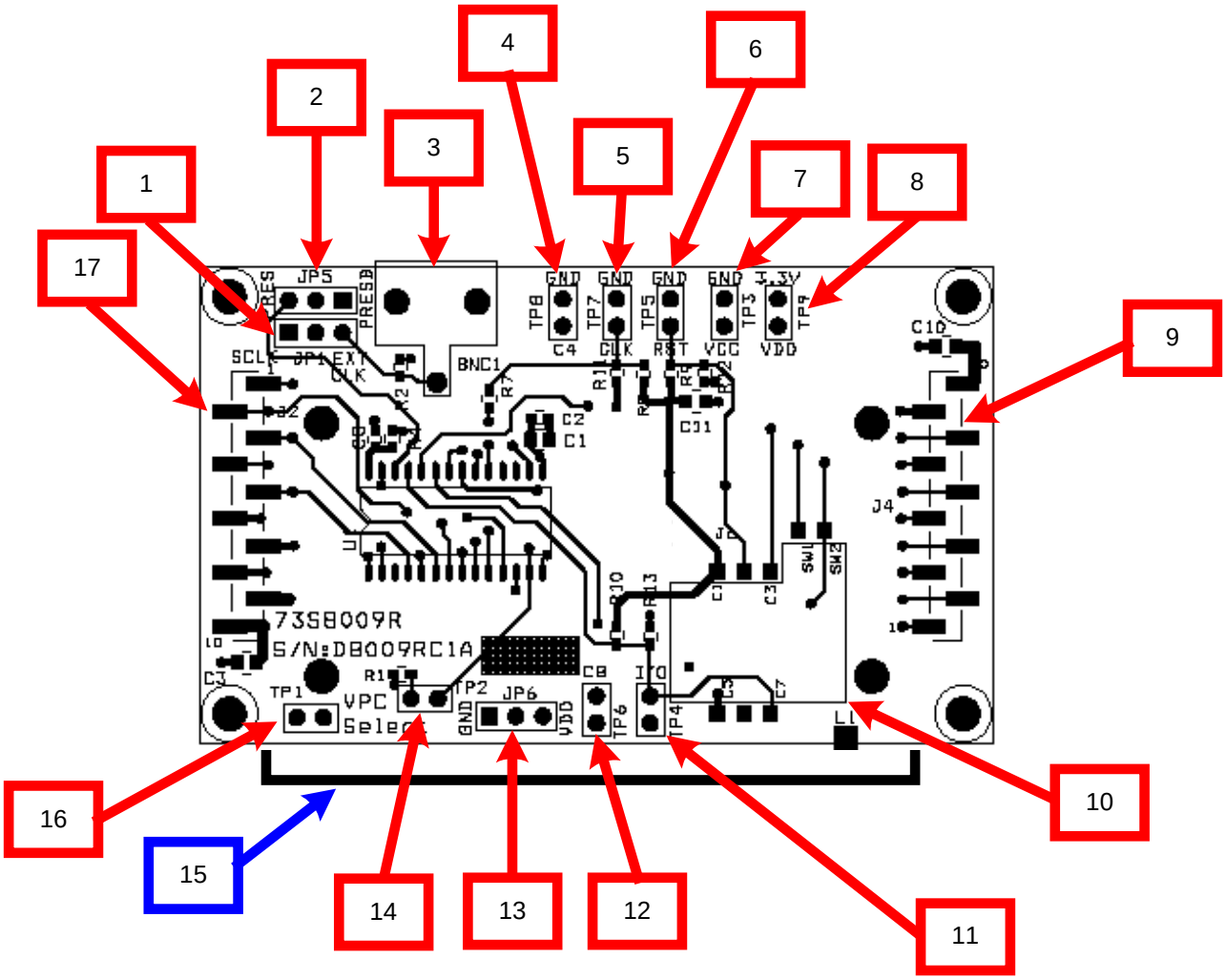

Figure 3: 73S8009R Demo Board Description

Table 5: 73S8009R Demo Board Description

Item # (Figure 3)	Schematic & PCB Reference	Name	Use
1	JP1	Clock selection.	Jumper to select between a clock from 12xx device or external clock as the frequency reference to the device.
2 13	JP5 JP6	Card Polarity detect select	The setting of these two jumpers depends on the type of smart card connector used (whether switch is nominally open or closed), and which of the card presence switch input of the 73S8009R is used. In this demo board, the switch is nominally open. The jumpers can be set in one of two ways: 1. Default setting: Use of PRES: JP5 must be set to PRES, and JP6 set to VDD. 2. Alternative use: Use of $\overline{\text{PRES}}$: JP5 must be set to PREB, and JP6 set to GND.
3	BNC1	EXTCLK	BNC input for external clock when JP1 is in the EXTCLK selection (jumper JP1 between terminal 2 and 3).
4 5 6 7 11 12	TP7 TP8 TP5 TP3 TP4 TP6	Test Points: CLK C4 RST VCC I/O C8	Two-pin test points for each respective smart card signal. The pin label name is the respective signal (i.e. VCC, CLK) and the other pin is GND.
8	TP9	VDD Select	Two-pin header. Shorting bar jumper must be in place for normal operation. The shorting jumper can be replaced with an ammeter to measure the VDD current to the IC. VDD must be at set with a 3.3V supply.
9	J4	Board 3.3V supply and digital control signals	Connector that gathers the 3.3V supply of the board, the 73S8009R host control signal pins RDY, CS, RESET, TEST, PWRDN, $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$, and RSTIN.
10	J6	Smart Card Connector	SIM/SAM smart card format connector Note that J6 is wired in parallel to the smart card connector J5 (underneath the PCB). No SIM/SAM should be inserted when using the credit-card size connector J5.
14	TP2	PWRDN Pull-Down Selection	Two-pin header. When shorted with a jumper, the device is in power down mode.
15	J5	Smart Card Connector	Smart card connector. When inserting a card (credit card size format), contacts must face up.
16	TP1	VPC select	Two-pin header. Shorting bar jumper must be in place for normal operation. The shorting jumper can be replaced with an ammeter to measure the VPC current to the IC. VPC must be at set with a 5V supply.
17	J2	Board 5V supply and host digital interface	Connector that gathers the 5V supply of the board, the 73S8009R interface IOU, external clock (SCLK) and interrupt ($\overline{\text{OFF}}$) pins.

4 Design Considerations

4.1 General Layout Rules

Follow these layout rules:

- Route I/O and auxiliary signals away from card interface signals.
- Keep CLK trace as short as possible and with minimal bends in the trace. If possible, keep routing of the CLK trace to one layer (avoid vias to other layers). Keep CLK trace away from other traces especially RST, I/O and VCC. Filtering of the CLK trace is allowed for noise purposes. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. Also, the zero Ω series resistor (R7) can be replaced with a small resistor for additional filtering (no more than 100 Ω).
- Keep VCC trace as short as possible. Make trace a minimum of 0.5 mm thick. Also, keep VCC away from other traces especially RST and CLK.
- Keep RST trace away from VCC and CLK traces. Up to 30 pF to ground is allowed for filtering.
- Keep 0.1 μF close to VDD pin of the device and directly take other end to ground.
- Keep 0.1 μF and 10 μF close to VPC pin of the device and directly take other end to ground.
- Keep 3.3 μF (1.0 μF for NDS) close to VCC pin of the smart card connector and directly take other end to ground.

4.2 Optimization for Compliance with EMV

Default configuration of the Demo Board contains a 27 pF capacitor (C12) from the CLK pin of the smart connector to ground and a 27 pF capacitor (C13) from the RST pin of the smart connector to ground. These capacitors serve as filters for CLK and RST signals in the case of long traces or test equipment perturbations. The capacitor on CLK reduces ringing on the trace, reduces coupling to other traces and slows down the edge of the CLK signal. The capacitor on RST helps the perturbation specification in a noisy environment. The filter capacitors can be useful in the EMV test environment and have no effect on NDS testing

C12 and C13 are represented on both schematic and BOM. These capacitors are optional filter capacitors on the smart card lines CLK and RST, respectively for each card interface. These capacitors may be adjusted (value, not to exceed 30 pF) or removed to optimize performance in each specific application (PCB, card clock frequency, compliance with applicable standards etc).

The default VCC capacitor of 3.3 μF is required to meet the dynamic VCC (smart card supply) transient current requirement in EMV2000 version 4.0.

5 73S8009R Demo Board Schematics, PCB Layouts and Bill of Materials

5.1 Schematics

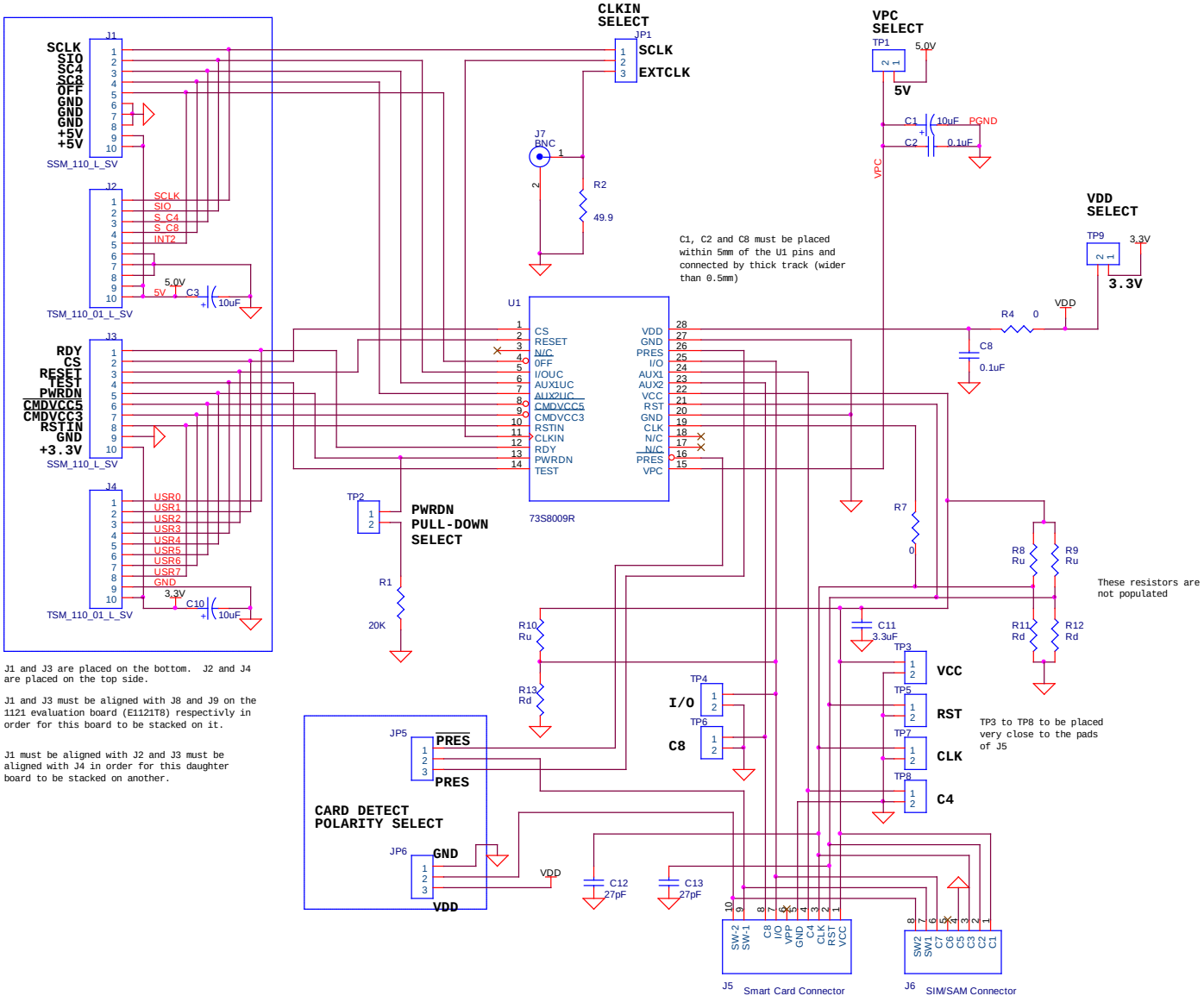

Figure 4: 73S8009R Electrical Schematic

5.2 73S8009R PCB Layouts

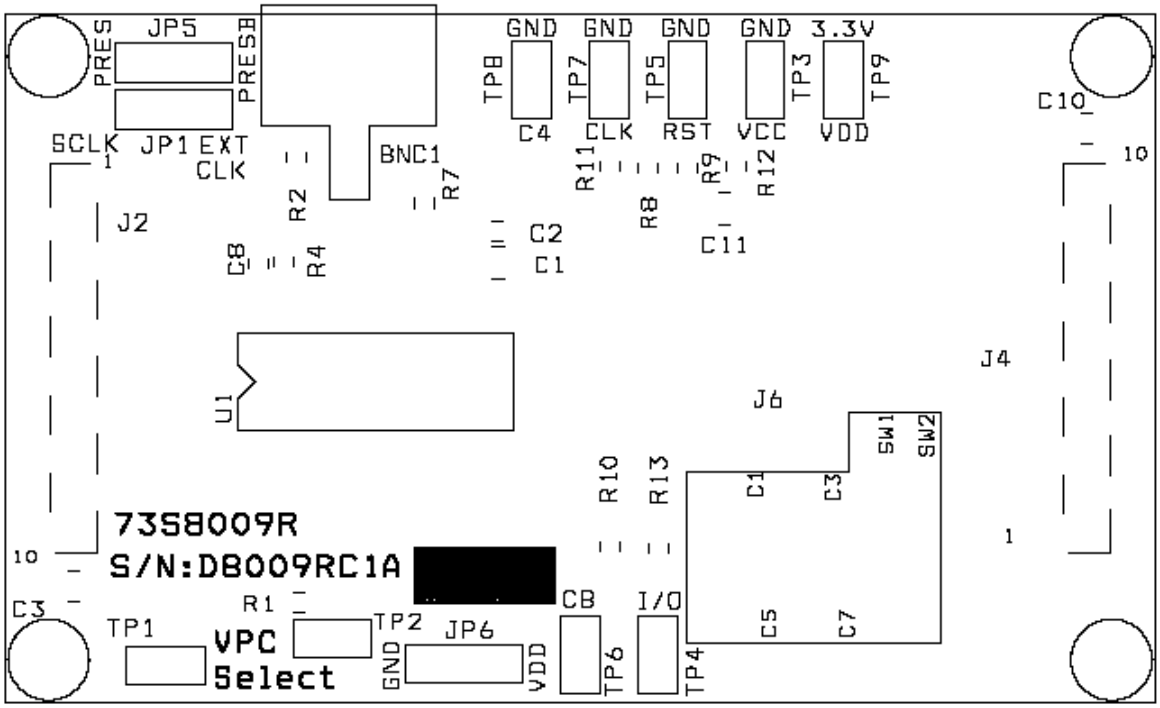

Figure 5: 73S8009R Demo Board: Top View

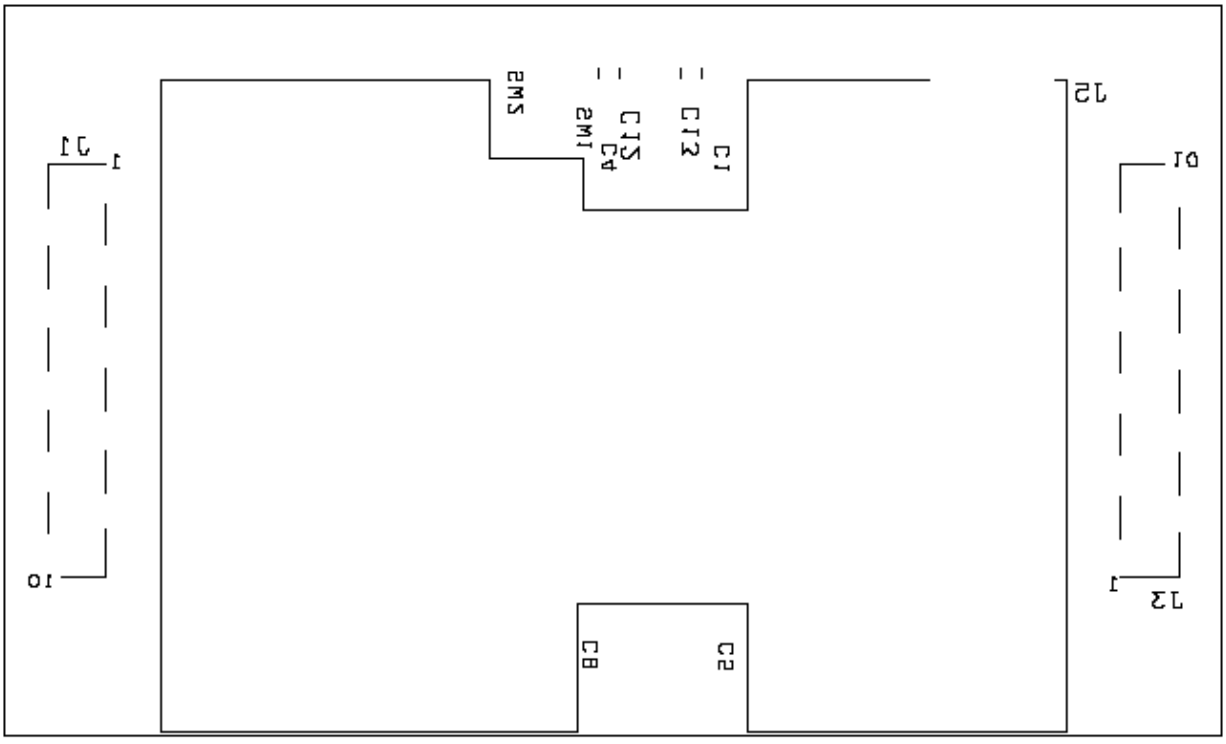

Figure 6: 73S8009R Demo Board: Bottom View

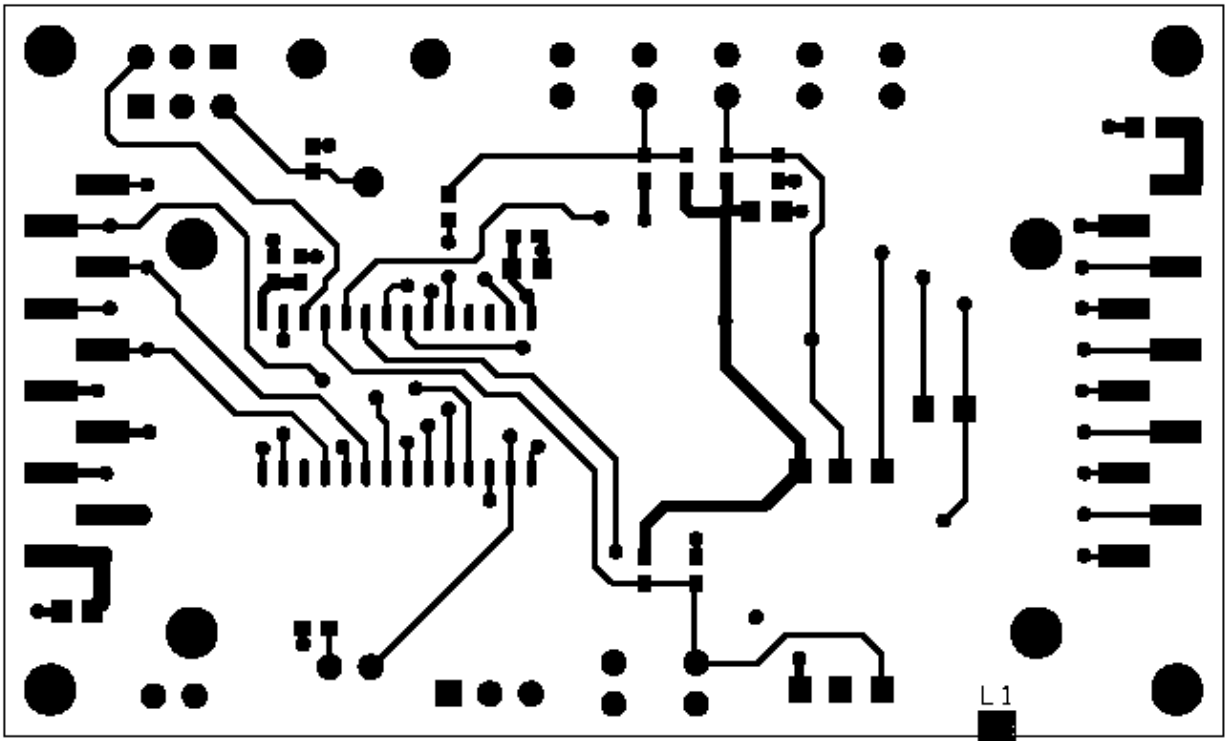

Figure 7: 73S8009R Demo Board: Top Signal Layer

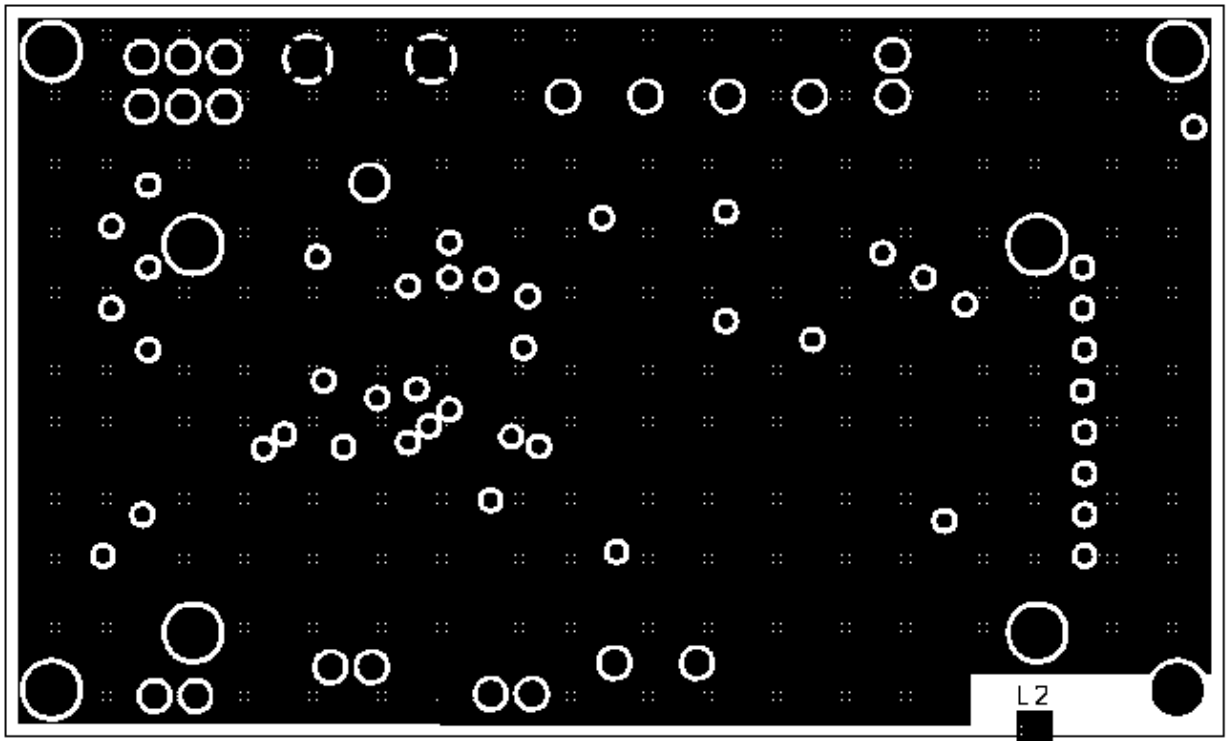

Figure 8: 73S8009R Demo Board: Middle Layer 1, Ground Plane

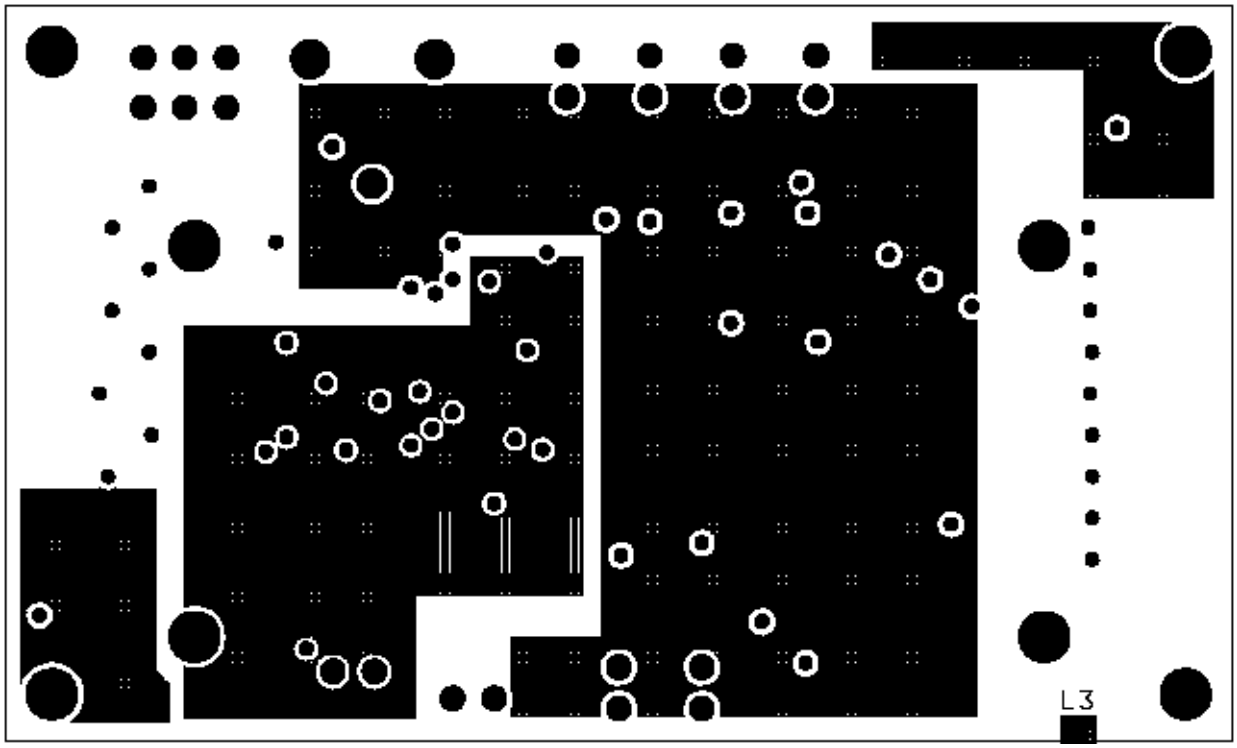

Figure 9: 73S8009R Demo Board: Middle Layer 2, Supply Plane

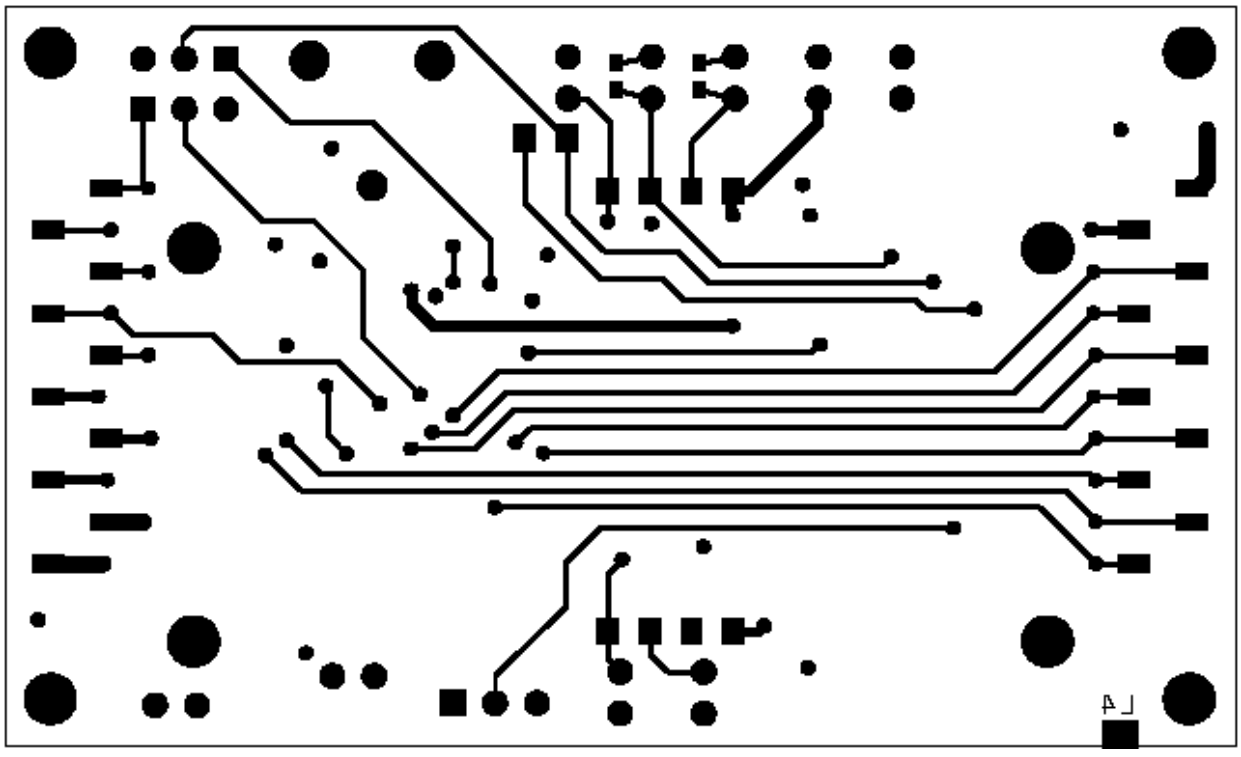

Figure 10: 73S8009R Demo Board: Bottom Signal Layer

5.3 73S8009R Demo Board Bill of Materials

Table 6: 73S8009R Demo Board Bill of Materials

Qty	Reference	Part	PCB Footprint	Digikey Part Number	Part Number	Manufacturer
3	C1,C3,C10	10 μF	805	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
2	C2, C8	0.1 μF	603	PCC1762CT-ND	ECJ-1VB1C104K	Panasonic
1	C11	3.3 μF	805	PCC1925CT-ND	ECJ-2YB0J335K	Panasonic
2	C12, C13	27 pF	603	PCC270ACVCT-ND	ECJ-1VC1H270J	Panasonic
3	JP1, JP5, JP6	Header 3	3pins, 2.54mm pitch	S1011E-36-ND	PBC36SAAN	Sullins
2	J1, J3	SSM_110_L_SV	SSM_110_L_SV	X	SSM_110_L_SV	Samtec
2	J2, J4	TSM_110_01_L_SV	TSM_110_01_L_SV	X	TSM_110_01_L_SV	Samtec
1	J5	Smart Card Connector	ITT_CCM02-2504	CCM02-2504-ND	CCM02-2504	ITTCannon
1	J6	SIM/SAM Connector	ITT_CCM03-3754	CCM03-3754CT-ND	CCM03-3754	ITTCannon
1	BNC1	BNC Connector	BNC	A24539-ND	414373-1	AMP
2	R4,R7	0	603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
1	R1	20 K	603	P20KGCT-ND	ERJ-3GEYJ203V	Panasonic
1	R2	49.9	603	P49.9HCT	ERJ-3EKF49R0V	Panasonic
3	R8,R9,R10	Ru	603	X	X	
3	R11,R12, R13	Rd	603	X	X	
9	TP1,TP2, TP3,TP4, TP5,TP6, TP7,TP8, TP9	TP2	2X1_Header	S1011-36-ND	PZC36SAAN	Sullins
1	U1	73S8009R	28SOP	X	73S8009R	Teridian

Note: The resistors noted Ru and Rd in the schematic are not populated on the board. They can be implemented to adjust the features of the smart card reader.

6 Ordering Information

Table 7 lists the order number used to identify the 73S8009R Demo Board.

Table 7: 73S8009R Demo Board Order Number

Part Description	Order Number
73S8009R 28-Pin SO Demo Board	73S8009R-DB

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8009R, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	5/22/2007	First publication.
1.1	8/9/2007	Corrected schematic error.
1.2	5/7/2010	Formatted in the new Teridian style. Added Section 1.1, Package Contents. Added Section 1.2, Safety and ESD Notes. Added Table 3: J4 Pin Descriptions. Added Table 4: J2 Pin Descriptions. Added Section 7, Ordering Information. Added Section 9, Contact Information. Miscellaneous editorial corrections.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

73S8009R-DB