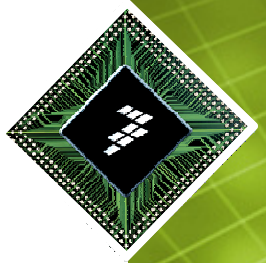
KL25 Analog-to-Digital Converter

16-bit SAR



Agenda

1. ADC Features overview
2. External signal connections
3. Configuration registers
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ADC Features overview

- ✓ Linear successive approximation algorithm with up to 16-bit resolution
- ✓ Up to four pairs of differential and 24 single-ended external analog inputs
- ✓ Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two's complement 16-bit sign-extended format
  - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- ✓ Single or continuous conversion
- ✓ Configurable sample time and conversion speed/power
- ✓ Conversion complete and hardware average complete flag and interrupt
- ✓ Input clock selectable from up to four sources

ADC Features overview (cont.)

- ✓ Operation in low power modes for lower noise operation
- ✓ Asynchronous clock source for lower noise operation with option to output the clock
- ✓ Selectable asynchronous hardware conversion trigger with hardware channel select
- ✓ Automatic compare with interrupt for various programmable values
- ✓ Temperature sensor
- ✓ Hardware average function
- ✓ Selectable voltage reference
- ✓ Self-calibration mode

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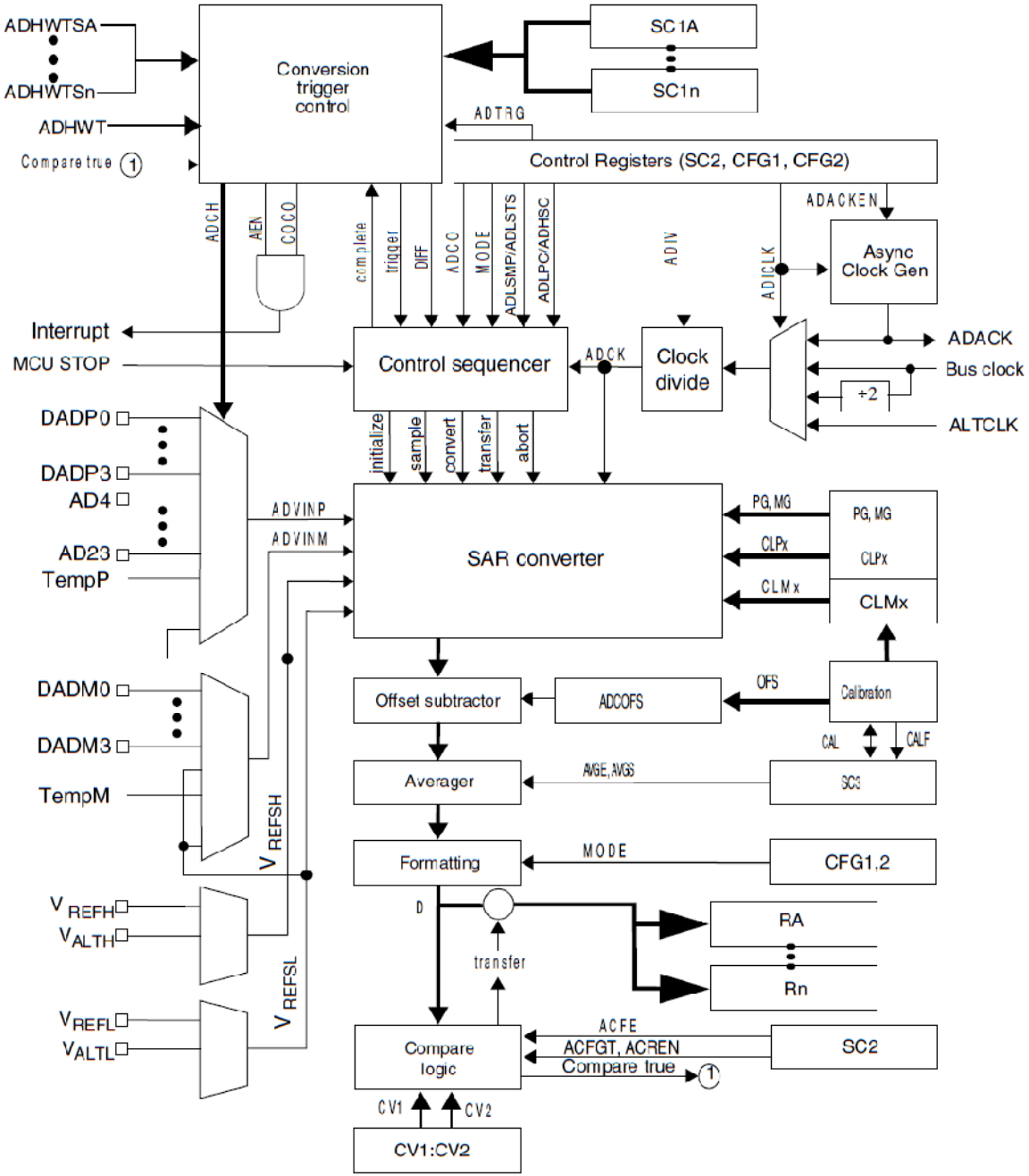
ADC Block Diagram

Signal	Description
DADP3–DADP0	Differential Analog Channel Inputs (+)
DADM3–DADM0	Differential Analog Channel Inputs (-)
ADn	Single-Ended Analog Channel Inputs
VREFSH	Voltage Reference Select High
VREFSL	Voltage Reference Select Low
VDDA	Analog Power Supply
VSSA	Analog Ground



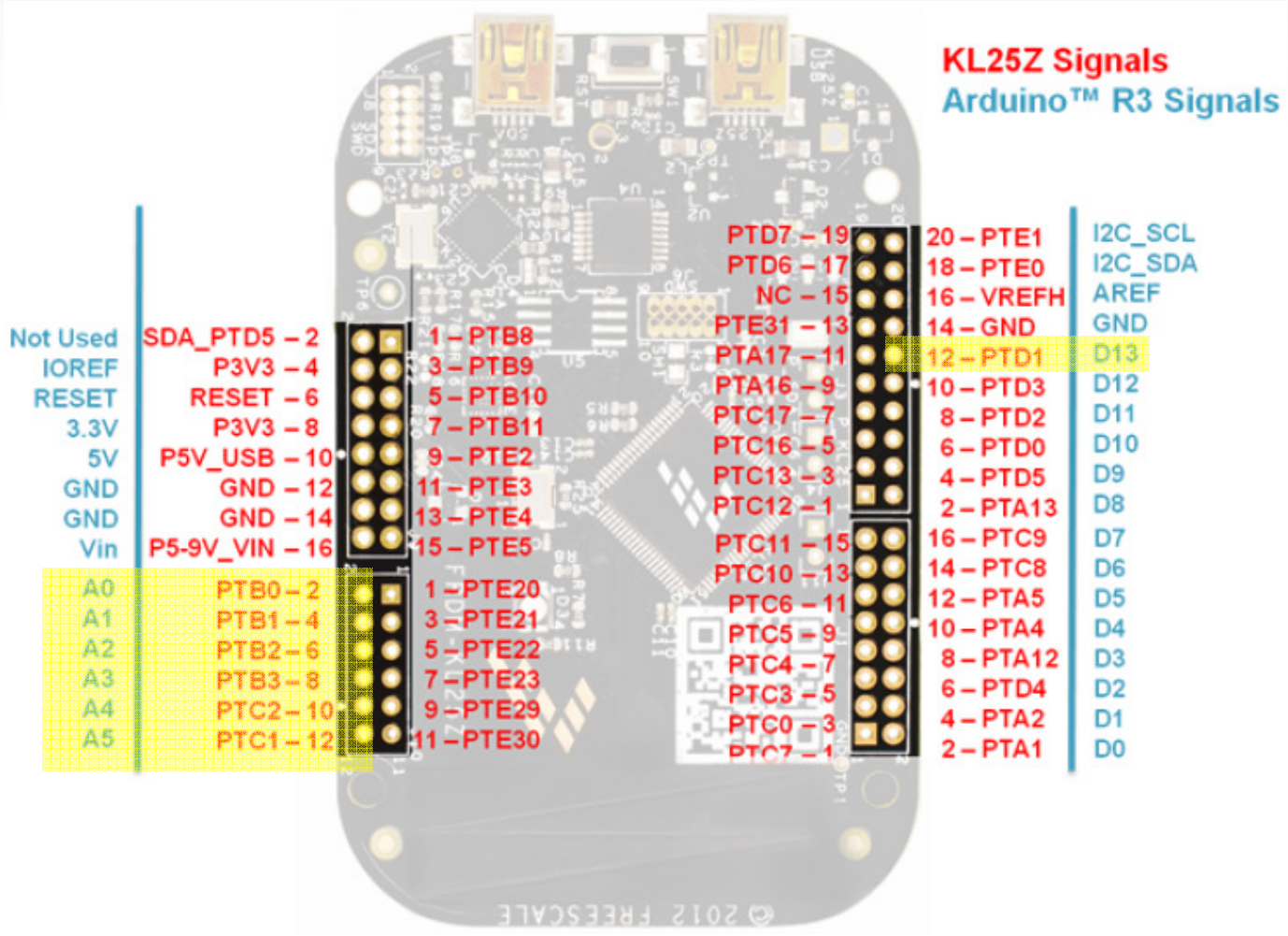
ADC Channel Assignment

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC0_DP0 and ADC0_DM0	ADC0_DP0/ADC0_SE0
00001	DAD1	ADC0_DP1 and ADC0_DM1	ADC0_DP1/ADC0_SE1
00010	DAD2	ADC0_DP2 and ADC0_DM2	ADC0_DP2/ADC0_SE2
00011	DAD3	ADC0_DP3 and ADC0_DM3	ADC0_DP3/ADC0_SE3
00100[1]	AD4a	Reserved	ADC0_DM0/ADC0_SE4a
00101[1]	AD5a	Reserved	ADC0_DM1/ADC0_SE5a
00110[1]	AD6a	Reserved	ADC0_DM2/ADC0_SE6a
00111[1]	AD7a	Reserved	ADC0_DM3/ADC0_SE7a
00100[1]	AD4b	Reserved	ADC0_SE4b
00101[1]	AD5b	Reserved	ADC0_SE5b
00110[1]	AD6b	Reserved	ADC0_SE6b
00111[1]	AD7b	Reserved	ADC0_SE7b
01000	AD8	Reserved	ADC0_SE8
01001	AD9	Reserved	ADC0_SE9
01010	AD10	Reserved	Reserved
01011	AD11	Reserved	ADC0_SE11
01100	AD12	Reserved	ADC0_SE12
01101	AD13	Reserved	ADC0_SE13
01110	AD14	Reserved	ADC0_SE14
01111	AD15	Reserved	ADC0_SE15

ADC Channel Assignment (cont.)

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
10000	AD16	Reserved	Reserved
10001	AD17	Reserved	Reserved
10010	AD18	Reserved	Reserved
10011	AD19	Reserved	Reserved
10100	AD20	Reserved	Reserved
10101	AD21	Reserved	Reserved
10110	AD22	Reserved	Reserved
10111	AD23	Reserved	12-bit DAC0 Output/ ADC0_SE23
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[2]	Bandgap (S.E)[2]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

ADC Channels on FRDM-KL25Z board



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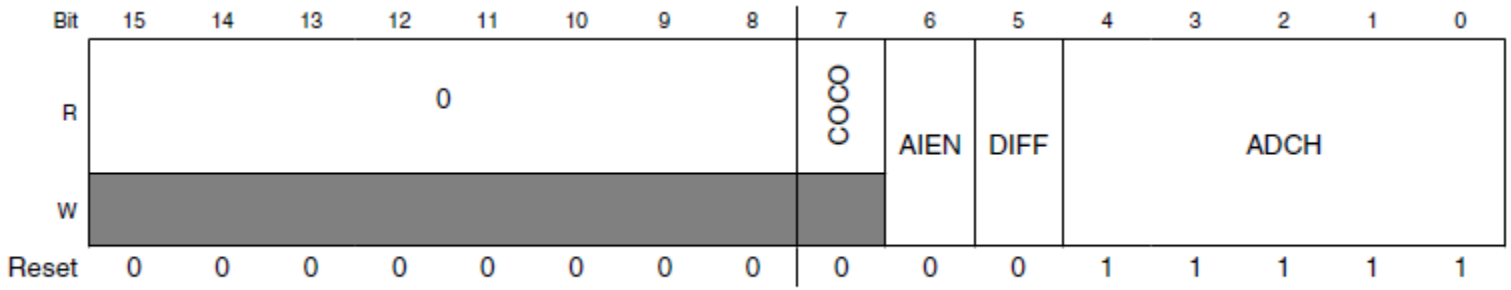
Status and Control Registers 1

- **ADC0_SC1A, ADC0_SC1B**



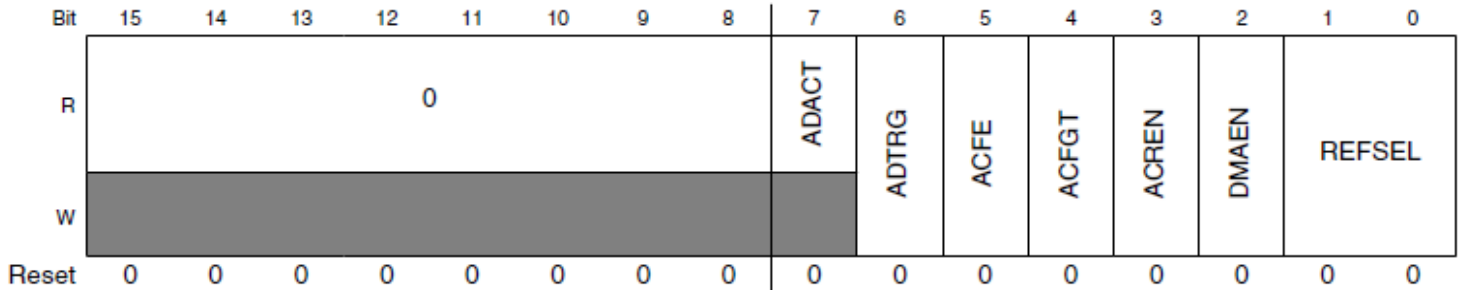
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								COCO	AIEN	DIFF	ADCH				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

ADCx_SC1*n* field descriptions

- **COCO**: Conversion Complete flag, a 1 indicates when the ADC conversion has finished.
- **AIEN**: Enables the Conversion Complete interrupt when its value is 1; otherwise, interrupts will not be asserted.
- **DIFF**: If it is 0, single-ended mode is enabled. If it is 1, differential mode is enabled.
- **ADCH**: Indicates the channel that will be converted. When all bits are 1, the ADC module will be disabled.

Status and Control Register 2

- **ADC0_SC2**



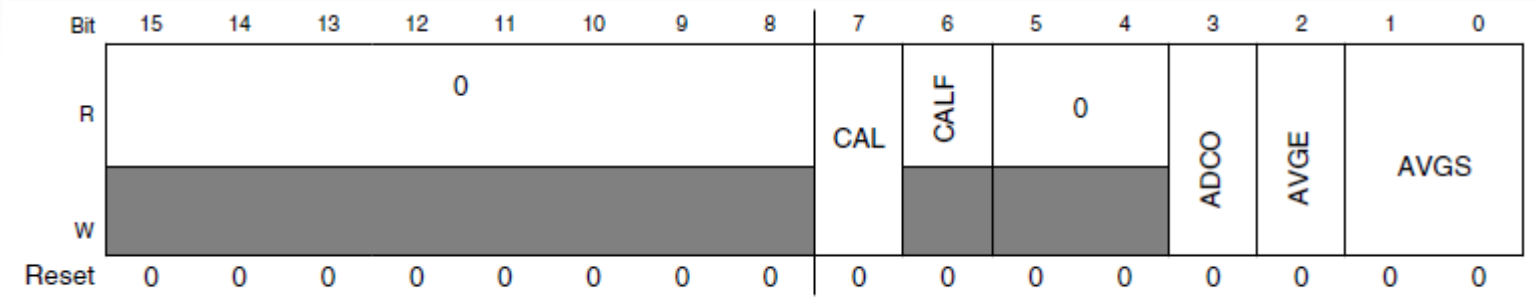
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								ADACT	ADTRG	ACFE	ACFGT	ACREN	DMAEN	REFSEL	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_SC2 field descriptions

- **ADACT**: This flag indicates that a conversion or hardware averaging is in progress.
- **ADTRG**: Selects the type of trigger used for initiating a conversion: 0 for software, 1 for hardware.
- **ACFE**: If it is 1, the compare function is enabled.
- **ACFGT**: Only has effect if the ACFE bit is 1. With a value of 0, configures the Less Than threshold. With a value of 1, configures the Greater Than threshold.
- **ACREN**: Enables the Range Comparison. If it is 0, just CV1 is compared. If it is 1, both CV1 and CV2 are compared.
- **DMAEN**: If it is 1, DMA-based conversion will be enabled.
- **REFSEL**: Selects the High and Low references: 0b00 for default reference pins (VREFH and VREFL). 0b01 for alternate pins (VALTH and VALTL). 0b10 and 0b11 are reserved.

Status and Control Register 3

- **ADC0_SC3**



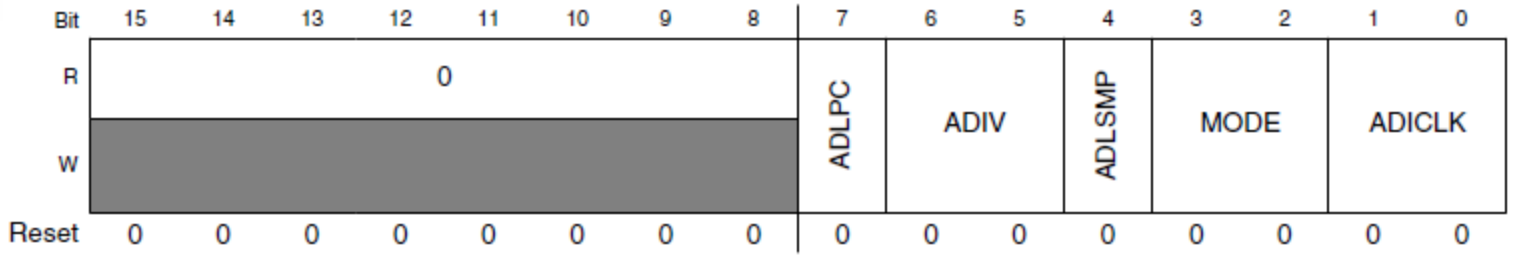
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CAL	CALF	0		ADCO	AVGE	AVGS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_SC3 field descriptions

- **CAL**: Begins the calibration sequence when set.
- **CALF**: If it is 0, calibration completed normally. If it is 1, calibration failed. It will fail if any ADC register is modified during calibration process.
- **ADCO**: If it is 0, single conversion is configured. If it is 1, continuous conversions are configured.
- **AVGE**: If it is 1, hardware average function is enabled; otherwise, average is disabled.
- **AVGS**: If AVGE bit is set, these bits select how many samples will be averaged: 0b00 for 4 samples. 0b01 for 8 samples. 0b10 for 16 samples. 0b11 for 32 samples.

Configuration Register 1

- **ADC0_CFG1**



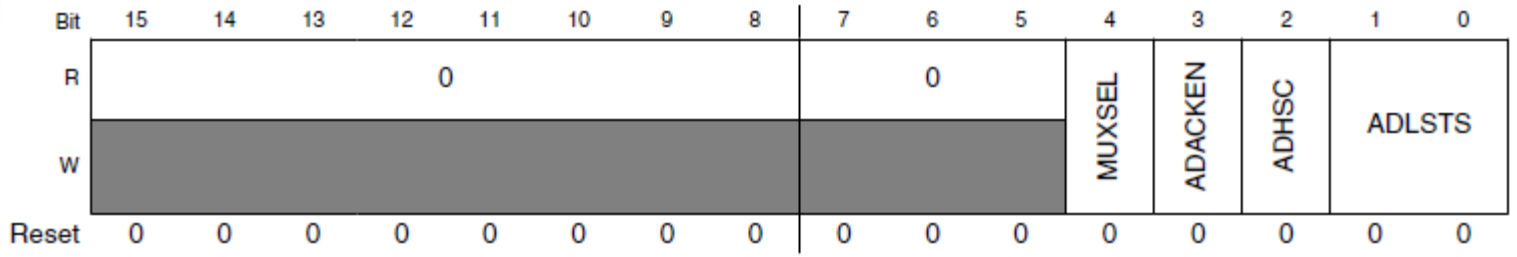
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								ADLPC	ADIV		ADLSMP	MODE		ADICLK	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_CFG1 field descriptions

- **ADLPC** : If it is 1, ADC low-power configuration is enabled.
- **ADIV**: Selects the divide ratio used by the ADC to generate the internal clock ADCK: 0b00 for divide by 1. 0b01 for divide by 2. 0b10 for divide by 4. 0b11 for divide by 8.
- **ADLSMP**: If it is 0, short sample time is configured. If it is 1, long sample time is configured.
- **MODE**: Selects the ADC resolution mode: 0b00 for 8-bit single-ended or 9-bit differential. 0b01 for for 12-bit single-ended or 13-bit differential. 0b10 for for 10-bit single-ended or 11-bit differential. 0b11 for for 16-bit single-ended or differential.
- **ADICLK**: Selects the input clock source to generate the ADC clock: 0b00 for Bus clock. 0b01 for Bus clock divided by 2. 0b10 for Alternate clock (ALTCLK). 0b11 for Asynchronous clock (ADACK).

Configuration Register 2

- **ADC0_CFG2**



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0			MUXSEL	ADACKEN	ADHSC	ADLSTS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_CFG2 field descriptions

- **MUXSEL**: Changes the ADC mux setting to select between alternate sets of ADC channels. If it is 0, ADxxa channels are selected. If it is 1, ADxxb channels are selected.
- **ADACKEN**: If it is 1, enables the asynchronous clock source and the clock source output regardless of the conversion and status of CFG1[ADICLK].
- **ADHSC**: If it is 1, High-Speed conversion sequence is selected. Otherwise, Normal conversion sequence is selected.
- **ADLSTS**: Selects between the extended sample times when long sample time is selected (CFG1[ADLSMP]=1). 0b00 for 20 extra cycles. 0b01 for 12 extra cycles. 0b10 for 6 extra cycles. 0b11 for 2 extra cycles.

Data Result Registers

- **ADC0_RA, ADC0_RB:**
- Contain the result of an ADC conversion of the channel selected by the corresponding status and channel control register (SC1A:SC1n). For every status and channel control register, there is a corresponding data result register.

Conversion mode	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Format
16-bit differential	S	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Signed 2's complement
16-bit single-ended	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Unsigned right justified
13-bit differential	S	S	S	S	D	D	D	D	D	D	D	D	D	D	D	D	Sign-extended 2's complement
12-bit single-ended	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	Unsigned right-justified
11-bit differential	S	S	S	S	S	S	D	D	D	D	D	D	D	D	D	D	Sign-extended 2's complement
10-bit single-ended	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	Unsigned right-justified
9-bit differential	S	S	S	S	S	S	S	S	D	D	D	D	D	D	D	D	Sign-extended 2's complement
8-bit single-ended	0	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	Unsigned right-justified

Compare Value Registers

- **ADC0_CV1**, **ADC0_CV2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																CV															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCx_CV*n* field descriptions

- **CV**: Contain a compare value used to compare the conversion result when the compare function is enabled (SC2[ACFE]=1).
- The compare value 2 register (CV2) is used only when the compare range function is enabled (SC2[ACREN]=1).

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ADC Hands-On

- On this example, the ADC will be initialized to 16-bit single-ended mode for reading the 1.0V Bandgap reference voltage (channel AD27).

11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[2]	Bandgap (S.E)[2]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
2. This is the PMC bandgap 1V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

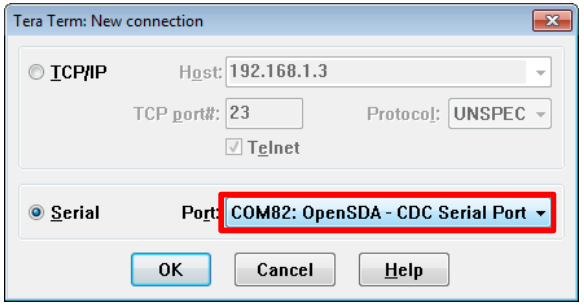
- It is required to turn on the Bandgap buffer by setting the bit BGBE of PMC_REGSC register; otherwise, conversions will return random values.

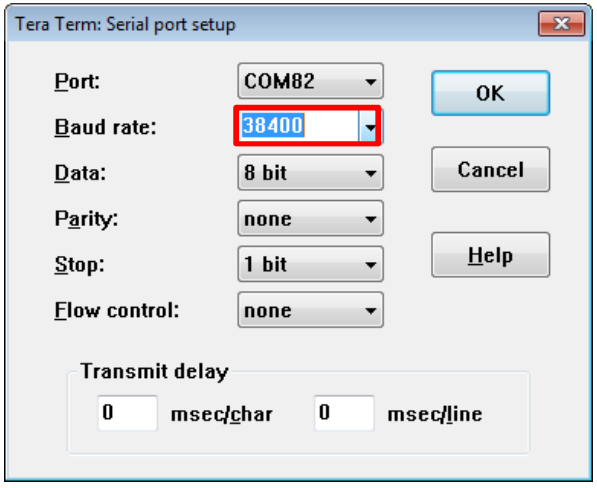
Bit	7	6	5	4	3	2	1	0
Read	0		Reserved	BGEN	ACKISO	REGONS	Reserved	BGBE
Write					w1c			
Reset	0	0	0	0	0	1	0	0

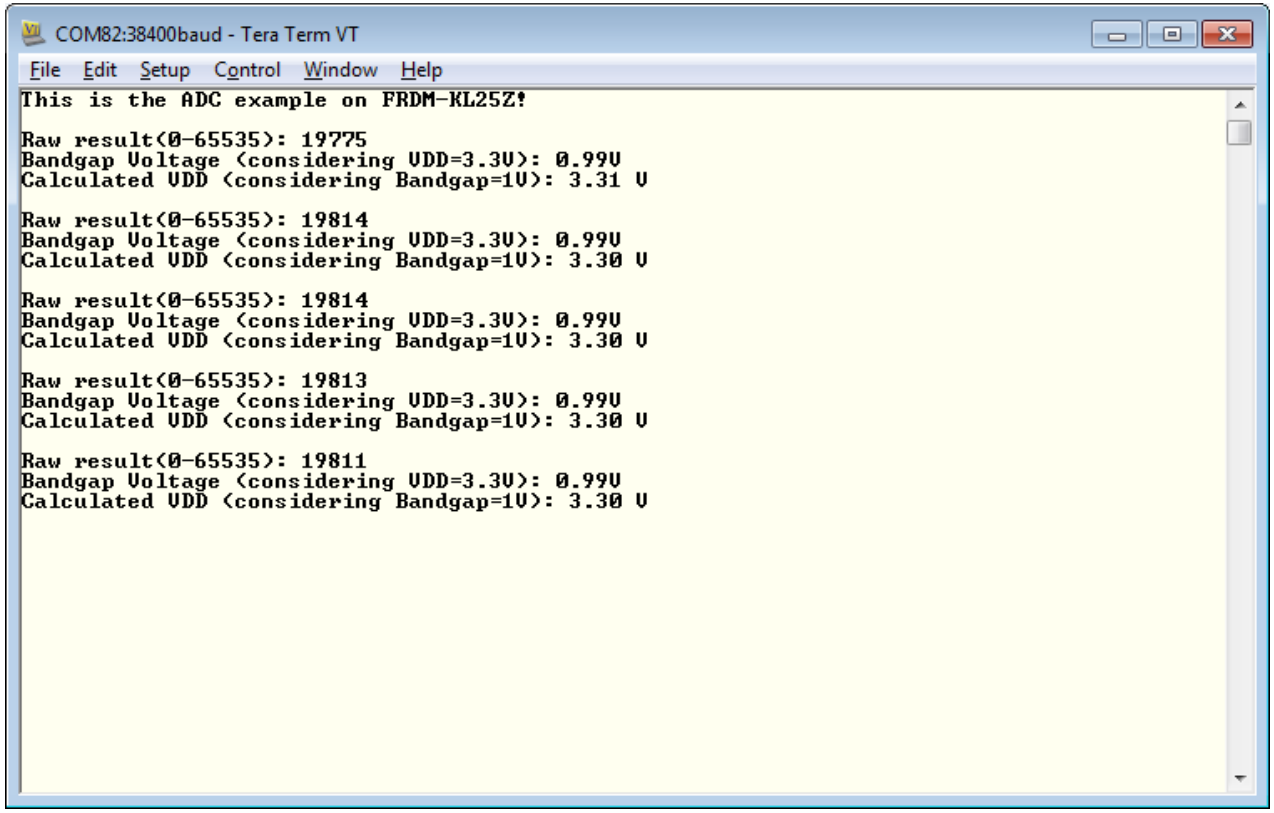
PMC_REGSC field descriptions

ADC Hands-On (cont.)

- Open Tera Term and ensure that the Serial Port is the “Open SDA – CDC Serial Port”, with a baud rate of 38400 bps.
- The raw data, the calculated Bandgap voltage (considering VDD = 3.3V), and the calculated VDD voltage (considering Bandgap = 1V) will be printed.







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Reference Material

More information about using the temperature sensor available on AN3031 "*Temperature Sensor for the HCS08 Microcontroller Family*":
http://www.freescale.com/files/microcontrollers/doc/app_note/AN3031.pdf

Complete pin out description on FRDM-KL25Z User's Manual :
http://www.freescale.com/files/32bit/doc/user_guide/FRDMKL25ZUM.zip

Kinetis L Peripheral Module Quick Reference:
http://www.freescale.com/files/32bit/doc/quick_ref_guide/KLQRUG.pdf


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