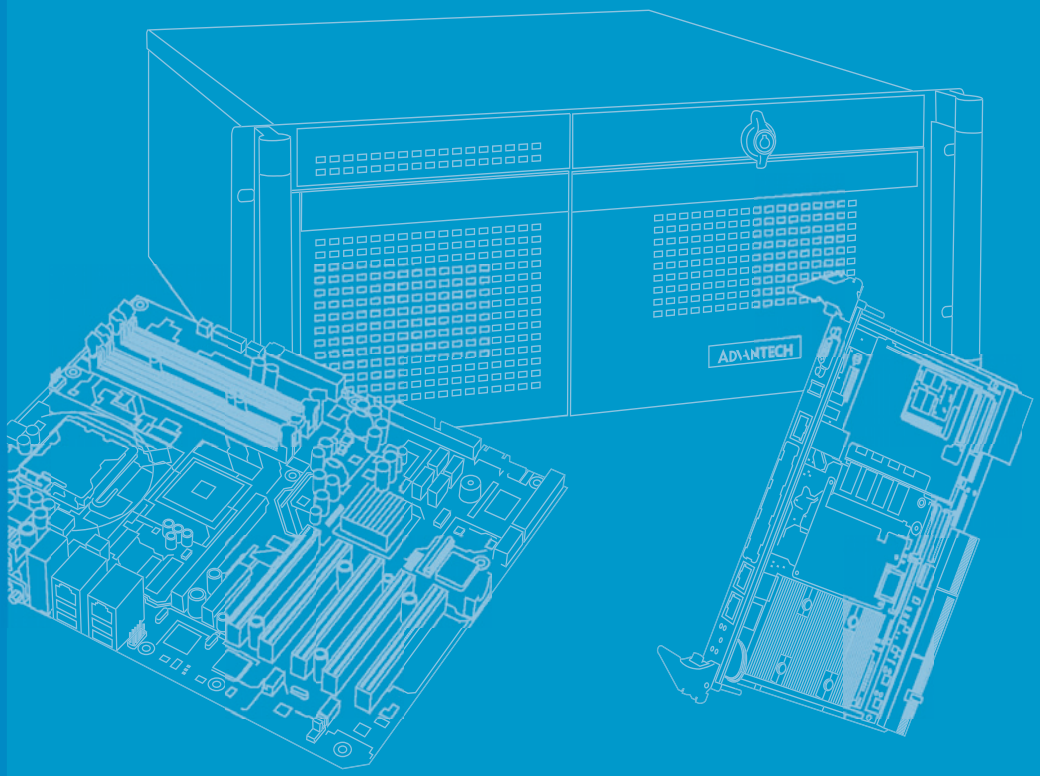

User Manual

MIC-6311

OpenVPX CPU Blade with Intel® 4th Core™ Processor

ADVANTECH

Enabling an Intelligent Planet

Copyright

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Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

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1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Part No. 2002631101 Edition 2

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In such a case, users are required to correct the interference at their own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com to obtain the latest information about this product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support should you require additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - Comprehensive description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

New batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we welcome your comments and constructive criticism. Please send all feedback in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the list, please contact your dealer immediately.

- MIC-6311 all-in-one single board computer (CPU heatsink and PCH heatsink included) x 1
- Daughter board for SATA HDD x 1 (assembled)
- HDD tray and screws x 1
- Solder-side cover x 1 (assembled)
- RJ45 to DB9 cable x 1
- Warranty certificate document x 1
- Safety Warnings: CE, FCC Class A

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use only a damp cloth for cleaning. Do not apply liquid or spray detergents.
4. For plug-in equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect this equipment from humidity.
6. Place this equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect this equipment from overheating. DO NOT COVER THE OPENINGS.
8. Ensure the power supply voltage is correct before connecting the equipment to the power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped or damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WITH A STORAGE TEMPERATURE THAT FLUCTUATES BELOW -20°C (-4°F) OR ABOVE 60°C (140°F). THIS MAY DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE STORED IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before handling the equipment. Do not touch components on the CPU card or other cards while the PC is on.
- Disconnect the power supply before making any configuration changes. A sudden rush of power after a jumper is connected or a card installed may damage sensitive electronic components.

We Appreciate Your Input

Please let us know whether any aspect of this product, including the manual, can benefit from improvements or corrections. We appreciate your valuable input in helping improve our products.

Contents

Chapter 1

Hardware Configuration

This chapter describes how to configure the MIC-6311 hardware.

1.1 Introduction

Advantech's MIC-6311 is a single processor VPX blade based on an Intel 4th generation Core i3/i5/i7 platform. The MIC-6311 enables the highest possible performance in the 6U VPX form factor with two SRIOx4 ports on the VPX data plane and two PCI Express x8 2nd generation lanes in the VPX expansion plane for workstation and computation-intensive applications. Two Serial RapidIO ports enable the MIC-6311 to be interfaced with digital front ends, such as DSP and FPGA cards, via a high-speed, low latency deterministic interconnect. In addition, PCI Express ports with up to 5GB/s throughput rates offer a high-performance interface to mainstream peripherals and I/O cards. With a SO-DIMM socket and additional soldered, onboard DRAM with ECC in a dual-channel design running at 1600MT/s, the MIC-6311 is suitable for harsh environments, maintains maximum memory throughput, and supports memory expansion using the latest SO DIMM technology. Moreover, the 4th generation Core processors provide an increased cache size and efficiency, as well as instruction set improvements, which make the MIC-6311 a high-performance computing engine with an outstanding floating point and vector processing performance.

Targeted to harsh environments, the MIC-6311 is designed to support conduction-cooling heat sinks. Additionally, it features an onboard soldered, industrial SSD for maximum reliability. Using Intel's latest PCH (Lynx Point) and advanced SATA controller, the MIC-6311 supports enhanced storage options, such as a 2.5" SATA III HDD/SSD socket with high storage capacity and up to 6 Gbps transfer speed. The CFast socket offers an ideal alternative for implementing a cost-efficient, pluggable SSD, and the onboard XMC/PMC site with PCIe x8 2nd generation connectivity is capable of hosting high-speed offload or I/O mezzanines. Two USB 3.0 ports located on the front panel can be connected to external USB devices, offering data transfer rates of up to 5Gbps. Network and remote connectivity is achievable via a RS232 console (RJ45) and two GbE RJ45 ports, and powered using Intel's latest Gigabit Ethernet controller - the I350.

The processor's integrated enhanced graphics engine Iris offers up to 2x the graphic performance than that of previous generation solutions. Triple independent display support can be implemented by using the MIC-6311's VGA front panel port and two DisplayPort / HDMI interfaces on the rear transition modules. Additionally, audio port support via the backplane interface provides enhanced media capabilities, and three SATA ports (SATAIII) and four USB ports (4x USB 2.0, 2x USB 3.0) are connected to the backplane to satisfy demands for additional I/O ports or storage. Two GbE/SERDES ports support system-level IP connectivity, and two UART interfaces can be leveraged to interface with legacy devices and consoles.

1.1.1 MIC-6311 SKU Introduction

Table 1.1: Processor Type

MIC-6311 Model Number	CPU	Core #	Cooling	Onboard DIMM Capacity
MIC-6311-A1I8E	I7-4700EQ	4	Air cooling	8 GB

1.2 Specifications

1.2.1 OpenVPX Interface

The MIC-6311 complies with the OpenVPX MOD6-PAY-4F1Q2U2T-12.2.1-2 profile. Two lanes of SRIO Gen2 x4, which offer 5G baud rates, are provided in the P1 data plane. The MIC-6311 uses two lanes of PCIe Gen2 x8 in the P2 expansion plane. Two lanes of 1GBase-T or SERDES (on request) are used for the P4 control plane.

1.2.2 CPU

The MIC-6311 supports the Intel 4th generation Core i3/i5/i7 Haswell processor family, with clock frequencies of up to 3.4 GHz. Intel 4th generation Core i3/i5/i7 processors are integrated with the embedded graphic controller Iris. By incorporating Iris, the MIC-6311 can support OpenGL 4.0, DirectX 11 and OpenCL 1.2, enabling enhanced 3D graphics processing. The Haswell CPU also offers superior performance when Intel Turbo Boost Technology 2.0 is required. Turbo Boost is automatically activated when the OS requests the highest processor performance state.

The Haswell CPU exhibits a superior performance 2x that provided by previous generations. Using Intel HT Technology, the MIC-6311 is capable of running demanding applications simultaneously, while maintaining system responsiveness.

1.2.3 Processor

The I7-4700EQ is the default CPU for the MIC-6311 air-cooled SKU (MIC-6311-A1I8E), and I5-4402E is the default CPU for the MIC-6311 conduction-cooled SKU (available on request). Please contact your distributor or local Advantech branch for information regarding the availability of I5-4400E/4402E SKUs.

Table 1.2: Processor Type

Intel CPU Model Number	CPU architecture	Core #	Freq.	Cache	DMI	CPU TDP	Package	Required Airflow
I7-4700EQ	Haswell (22nm)	4	2.4 GHz	6 MB	5 GT/s	47 W	FCBGA	35 CFM
I5-4400E	Haswell (22nm)	2	2.7 GHz	3 MB	5 GT/s	37 W	FCBGA	30 CFM
I5-4402E	Haswell (22nm)	2	1.6 GHz	3 MB	5 GT/s	25 W	FCBGA	30 CFM

Note! *Because the power consumption and thermal restrictions differ for various VPX systems, please double check these items before installing a higher-speed CPU not specified in the table above.*

1.2.4 BIOS

An 8 Mbyte SPI flash featuring a board-specific BIOS (from AMI) was designed to satisfy industrial and embedded system requirements.

1.2.5 Chipset

The Intel Mobile QM87 (Lynx Point) chipset integrates several capabilities to provide flexibility when connecting I/O devices. The Intel QM87 chipset offers fast access to peripheral devices and delivers outstanding system performance through high-bandwidth interfaces such as PCI Express, Serial ATA solid-state drives (SSDs) and traditional hard disk drives (HDDs), and integrated USB 3.0. The chipset also drives lower power through enhanced link power management of the Advanced Host Controller

Interface (AHCI), enables easier expandability with support for native hot plug, and enhances boot and multitasking performance with Native Command Queuing (NCQ).

1.2.6 Memory

The MIC-6311 features 8 GB of onboard DDR3L memory with ECC support, and one 204-pin SO-DIMM socket that can accommodate an additional 8GB of 1.35V memory.

1.2.7 Ethernet

The MIC-6311 uses an Intel I350AM4 LAN controller to offer two 10/100/1000Base-T Ethernet connectivity (on LAN1 & LAN2) and provides two 10/100/1000Base-T Ethernet connectivity to P4. Optional settings for the source of each Gigabit Ethernet port can be found in the BIOS menu.

- Front I/O (RJ-45)
- Backplane (GbE) (SERDES on request)

1.2.8 Storage Interface

The MIC-6311 supports SATA III and three SATA II interfaces. The SATA III inter-face is routed to the 2.5" SATA hard disk drive connector on the MIC-6311. Three SATAIII are routed to P5; however, users must add a re-driver to their Rear-IO to ensure that these drivers can perform at SATAIII speed. Another SATA interface is connected to an onboard soldered, industrial SSD for maximum reliability. Currently, an 8G SATAI driver is provided with the MIC-6311 as the standard storage capacity. Please contact your local Advantech branch or distributor to request the customized option.

1.2.9 Serial ports

One RJ-45 COM1 port (RS-232 interface) is provided on the front panel. Two COM ports are routed to the backplane via a P5 connector, and can be configured to RS232 / RS485 / RS422 modes using the onboard switch.

1.2.10 USB Ports

Two USB 3.0-compliant ports with fuse protection are provided. Both ports are routed to the front panel connectors on the MIC-6311 and to the rear I/O module via a P5 connector.

1.2.11 LEDs

Four LEDs are provided on the front panel as follows:

- One bi-color LED (blue/yellow) indicates hot swap and HDD activity. Blue indicates that the board can be safely removed from the system, whereas yellow indicates HDD activity.
- One LED is used to indicate the power status. The emission of green light indicates that power is provided to the board.

1.2.12 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control.

The programmable time interval is 1 to 255 seconds.

1.2.13 Optional Rear I/O Modules

Please contact your local Advantech branch or distributor for all inquires regarding customized RIO options.

1.2.14 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 55°C (32 ~ 131°F) for industrial-temperature SKUs; -40 ~ 70°C(-40 ~140°F) for wide-temperature SKUs. Please contact your Advantech representative regarding the availability of wide-temperature SKUs.

Note! *The operating temperature range of the MIC-6311 depends on the processor installed and the airflow through the chassis.*

- **Storage Temperature:** -40 ~ 85°C (-40 ~ 185°F)
- **Humidity:** 95% @ 40°C (non-condensing)
- **Humidity (non-operating):** 95% @ 60°C (non-condensing)
- **Vibration:** 5~100Hz, 1.06Grms (without on-board 2.5” SATA HDD)
- **Vibration (non-operating):** 5~100 Hz, 2 Grms
- **Shock:** 20 G (without on-board 2.5” SATA HDD)
- **Shock (non-operating):** 50 G
- **Altitude:** 4,000 m above sea level
- **Board size:** 233.35 x 160 mm (6U size), 1-slot (4 TE) wide
- **Weight:** 0.8 kg (1.76 lb)

1.2.15 Compact Mechanical Design

The MIC-6311 has a specially designed CPU heatsink to enable fanless operation. Please contact your distributor or local Advantech branch regarding the feasibility of a customized conduction-cooling heatsink design.

1.2.16 PCIE Bridge

The MIC-6311 uses a PLX PEX8733 component and 32-lane, 18-port, PCIe Gen3 switch device as the gateway to an intelligent subsystem. When configured as a system controller, the bridge acts as a standard transparent PCI Express to PCI/PCI-X Bridge. The MIC-6311 receives power from the backplane and supports a rear I/O. The PLX PEX 8733 offers the following features:

- PCI Interface
  - Full compliance with the PCI Local Bus Specification, Revision 3.0
  - PCI Power Management Spec, r1.2
- Supports transparent and non-transparent mode of operations.
- Supports forward and reverse bridging
- 64-bit, 66MHz asynchronous operation
- Integrated DMA engine, four DMA Channels
- End-to-end CRC (ECRC) protection
- Failover support, can be configured for 1+1 redundancy or N+1 redundancy

Please consult the PLX PEX 8733 data book for details.

1.2.17 I/O Connectivity

For MIC-6311, front panel I/O is provided through two RJ-45 Gigabit Ethernet ports, one RJ-45 COM port, two USB 3.0 ports, one USB 2.0, one VGA connector, and one XMC/PMC knockout.

The onboard I/O consists of one SATA channel, which can be connected to a daughter board for 2.5" SATA HDD and a CFast slot. Rear I/O connectivity is available via the following VPX connectors:

- P1: two lanes of SRIO Gen2 x4.
- P2: two PCIe Gen2 x8
- P3: PMC IO
- P4: XMC IO, KB/mouse, and two lanes of GbE or SERDES
- P5: two COM ports, two DisplayPorts, two USB 2.0 ports, two USB 3.0 ports, and audio outputs

Please refer to the appendix for the details of the pin definitions.

1.2.18 PMC (PCI Mezzanine Card) IEEE1386.1 Compliant

Additional I/O or co-processing functionality is supported by add-on PMC modules. The MIC-6311 supports one PMC site that is fully compliant with the VITA 46.9 PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard specification. The PMC supports a 133 MHz PCI-X bus interface and both 3.3 V and 5 V VIO depending on usage.

The two-layer front panel design complies with IEEE 1101.10. Connectors are screwed to the front panel, and a shielding gasket is attached to the panel edge, reducing emissions and increasing protection from external interference.

1.2.19 Hardware Monitor

One hardware monitor (NCT6776D) is provided for monitoring critical hardware parameters. This monitor is attached to the BMC to facilitate monitoring of the CPU temperature and core voltage.

1.2.20 Super I/O

The MIC-6311 Super I/O device supports the following legacy PC devices:

- Serial ports COM1 and COM2 are connected to the rear I/O module or front panel via a multiplexer in the FPGA.
- The PS2 (KB/mouse) is routed to the rear I/O module.

1.2.21 RTC and Battery

The RTC module maintains the date and time. The RTC circuitry on MIC-6311 is connected to a battery (CR2032M1S8-LF, 3V, 210 mAH).

1.2.22 IPMI

The MIC-6311 features the Intelligent Platform Management Interface (IPMI) for monitoring the health of the entire system. A NXP LPC1768 microcontroller provides BMC functionality to interface between the system management software and platform hardware. Full IPMI details are covered in Chapter 3.

1.2.23 BMC

The MIC-6311 management firmware is implemented on a 32-bit ARM Cortex-M3 core. An external SPI EEPROM is used for storing FRU inventory data and non-volatile configurations.

1.2.23.1 Key Features

- Advantech Integrity Sensor
- Based on an Advantech IPMI Core, and designed for xTCA, CPCI and VPX
- Compliant with IPMI 1.5 and IPMI 2.0 specifications
- IPMI-over-LAN
- Serial-over-LAN

- KCS interface enables direct IPMI communication between the OS and BMC
- BIOS failover, including a BIOS watchdog
- Full BMC watchdog support, as defined in the IPMI specification
- Full BMC firmware redundancy
  - Manual rollback
  - Automatic rollback in the event of update failure
- HPM.1 for in field updates, supporting:
  - BMC firmware
  - FPGA
  - BIOS
- UART muxing between all serial interfaces for easy console access
- Additional sensors for hardware monitoring

1.3 Functional Block Diagram

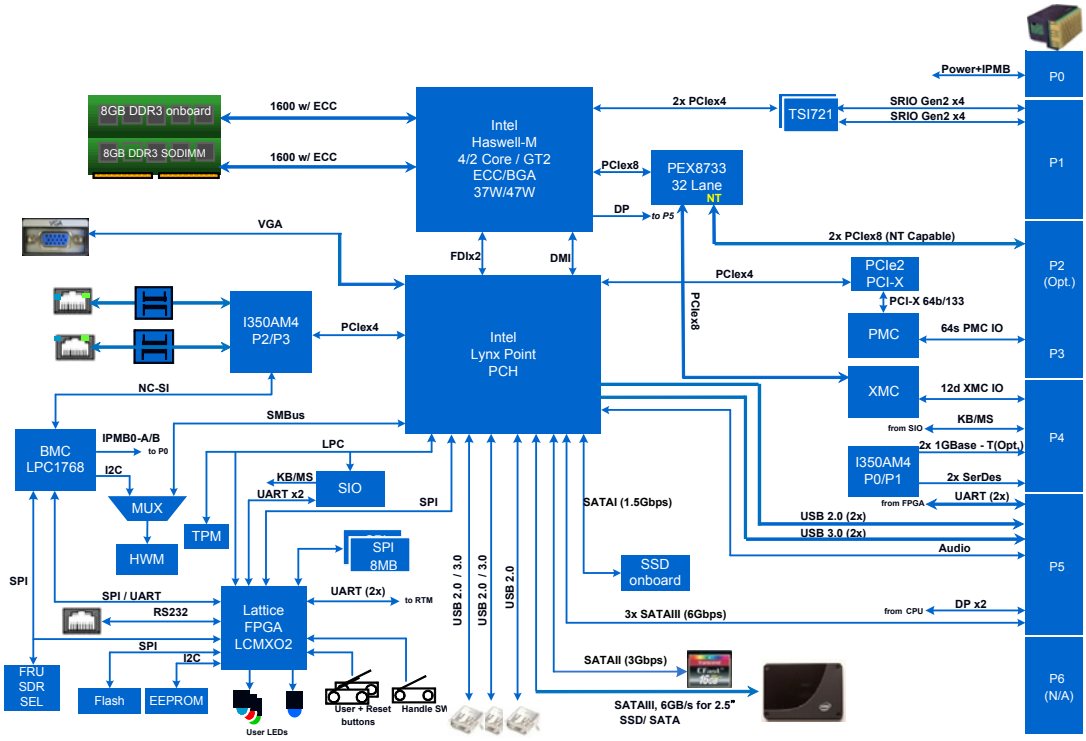


Figure 1.1 MIC-6311 functional block diagram

1.4 Board Map

The figure below shows the location of the main components, jumpers, switches and thermal sensors.

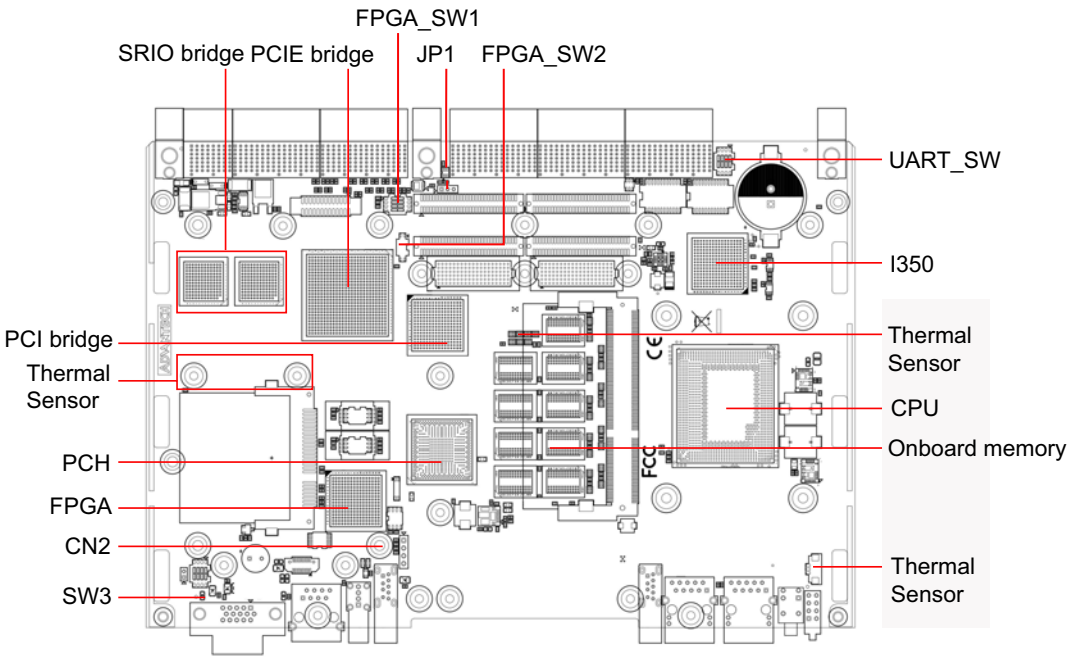


Figure 1.2 Board map

1.5 Jumpers and Switches

Table 1.4 and Table 1.5 list the jumper and switch functions. Read this section carefully before changing the jumper and switch settings on your MIC-6311 board.

Table 1.3: MIC-6311 Jumper Descriptions

Number	Function
CN2	Clear CMOS
JP1	PMC VIO

Table 1.4: MIC-6311 Switch Descriptions

Number	Function
FPGA_SW1	These two switches are for PCIE NT setting LAN configuration
FPGA_SW2	
UART_SW	RIO COM RS232/RS485/ RS422 mode selection
SW3	Front COM & RTM COM1/COM2 ports selection for SIO UART

1.5.1 Clear CMOS (CN2)

This jumper is used to erase CMOS data. Follow the procedures below to clear the CMOS.

1. Turn off the system.
2. Close jumper CN2 for approximately 3 seconds.
3. Set jumper CN2 as **Normal**.
4. Turn on the system. The BIOS is reset to the default setting.

Table 1.5: CN2 Clear RTC	
	Closed
Clear RTC	Default
Open	Normal

1.5.2 PMC VIO Setting (JP1)

This jumper is used to set the PMC IO voltage.

1. JP11 (1-2) for +3.3 V
2. JP11 (2-3) for +5 V

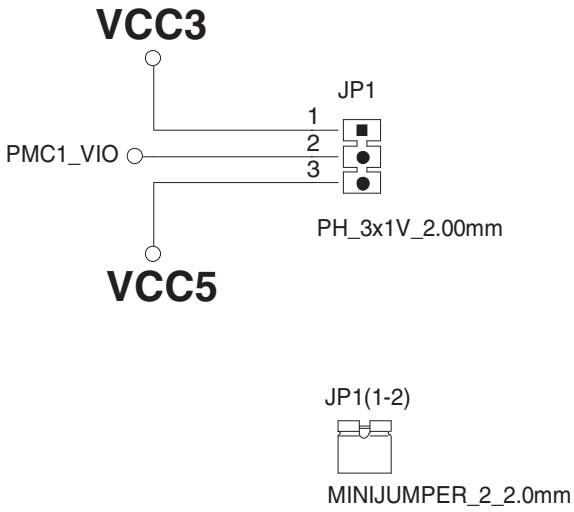
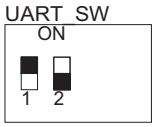
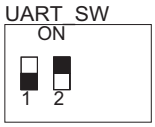
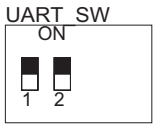
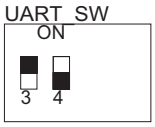
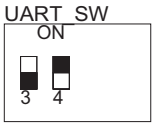
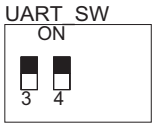


Figure 1.3 JP11 for PMC VIO (+3.3 V or +5 V)

1.5.3 Switch Settings

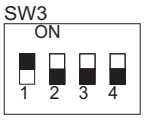
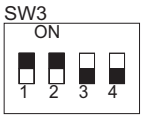
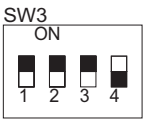
Note! ■ *represents the key.*

Table 1.6: FPGA_SW1 & FPGA_SW2 PCIE NT Setting		
NT is disabled (default)	NT is port 1	NT is port 9
FPGA_SW1 ON 1 2 3 FPGA_SW2 ON 1 2	FPGA_SW1 ON 1 2 3 FPGA_SW2 ON 1 2	FPGA_SW1 ON 1 2 3 FPGA_SW2 ON 1 2

RIO COM RS232/RS485/ RS422 mode selection		
COM1 to backplane is set to RS232	COM1 to backplane is set to RS485	COM1 to backplane is set to RS422
		
COM2 to backplane is set to RS232	COM2 to backplane is set to RS485	COM2 to backplane is set to RS422
		

The COM1 and COM2 that are routed to the backplane can be configured as three different console modes.

Table 1.7: SW3 Front COM and RTM COM1/COM2 Port Selection for BMC/SIO UART

Default	Front COM for BMC RTM COM1 for SIO COM1 RTM COM2 for SIO COM2	
	Front COM for SIO COM1 RTM COM1 for BMC RTM COM2 for SIO COM2	
	Front COM for SIO COM2 RTM COM1 for SIO COM1 RTM COM2 for BMC	

The keys must be oriented as **ON** either the front panel COM, RTM COM1 or RTM COM2 are connected to the BMC.

1.6 Connector Definitions

Table 1.14 lists the function of each connector, and Figures 1.3 and 1.4 illustrate the location of each connector.

Table 1.8: MIC-6311 connector descriptions

Number	Function
HDD	SATA HDD daughter board
XMCJ5/XMCJ6	XMC
DIMM1	SODIMM socket
PMCJ1/PMCJ2	PMC
CFast	CFast card slot

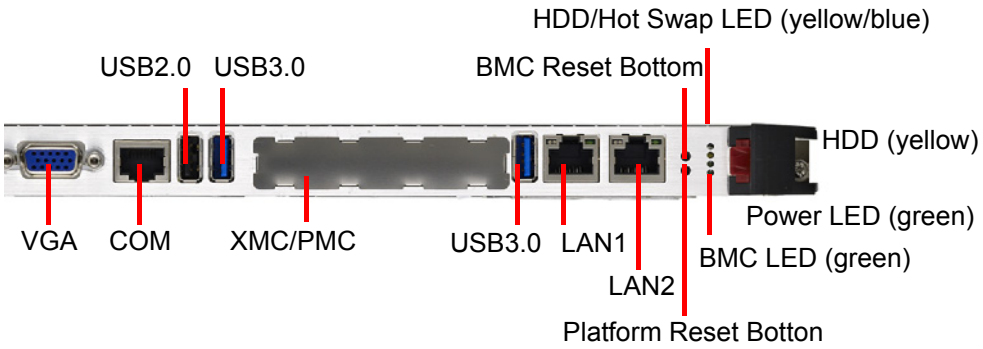


Figure 1.4 MIC-6311 front panel ports, indicators and buttons

MIC-6311 supports three BMC-controlled front panel LEDs.

Table 1.9: Front Panel LEDs

LED	Color	Description
1	Blue	Hot swap indicator
2	Green	BMC indicator
3	Green	Flashing = FW application active, payload (x86) in sleep Solid = FW application active, payload (x86) active

The LED illuminates as follows to indicate various states.

Item	Meaning	Color	Behavior
Power	Power on	Green	LED On
HDD	HDD active	Yellow	Blinking
Hot swap	Ready to perform hot swap	Blue	LED On
BMC act LED	BMC active	Green	LED On

1.6.1 USB Connectors

MIC-6311 features both Universal Serial Bus (USB) 3.0 and 2.0 channels. Two USB 3.0 ports, USB1 and USB2, and one 2.0 port are located on the front panel. Two USB 2.0 and USB3.0 channels are routed to the P5 connector. The USB interface provides complete plug-and-play functionality and hot attach/detach for up to 127 external devices. The MIC-6311 USB interface complies with USB specification R3.0 and is fuse protected (5 V @ 1.1 A). The USB interface can be disabled in the system BIOS setup. The USB controller default is set to **Enabled**.

1.6.2 Serial Ports

MIC-6311 has one serial port and two serial ports routed to P5. They function as RS-232 interfaces via RJ-45 connectors on the front panel. A RS-422/485 mode can be selected using the switch UART_SW. An RJ-45 to DB-9 adaptor cable is provided among the MIC-6311 accessories to facilitate connectivity to external consoles or modem devices. The BIOS Advanced Setup program covered in Chapter 2 provides a user interface with functions that include enabling or disabling ports and setting the port address. The RS-232 standard implementation method differs between serial devices. If you have problems with a serial device, check the connector pin assignments listed in Table 1.11. The IRQ and address range for these ports are fixed. However, should you wish to disable the port or change these parameters, you can access these options in the system BIOS setup.

1.6.3 Ethernet Configuration

MIC-6311 is equipped with a high-performance PCI Express-based network interface controller, the I350, which provides IEEE802.3-compliant 10/100/1000Base-TX Ethernet interfaces. Two GbE interfaces are connected to the front panel, and another two GbE interfaces are routed to the backplane. These two GbE interfaces can be configured to SERDES. Please contact your local Advantech distributor or branch for information regarding the availability of SERDES SKUs.

1.6.4 SATA Daughter Board Connector (CN7 and Extension Module)

MIC-6311 provides one SATA interface for a daughter card of a SATA HDD via the CN7 connector. The SATA HDD can also function as an optional onboard HDD. Two SATA interfaces are connected to the XTM for processing additional SATA HDD requests.

1.6.5 System Reset and BMC Reset Button

MIC-6311 features a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry, but does not reset the system management (IPMI) related circuitry. A separate BMC reset button is provided on the front panel for resetting the BMC and related hardware.

1.7 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your VPX chassis before direct handling. Do not touch any components on the CPU board or other boards while the VPX chassis is powered.
- Disconnect the power before implementing any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to eliminate any static charge before touching the CPU board. Be particularly careful not to touch the chip connectors.
- Contemporary integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Leave the board in its antistatic packaging when not installed in the chassis, and place it on a static dissipative mat when working with it. Wear a grounding wrist strap for continuous protection.

1.8 Installation

MIC-6311 contains electrostatically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch the components or connector pins. We recommend that you assemble the device on an anti-static workbench.

1.8.1 HDD Installation

MIC-6311 supports a 2.5” SATA hard disk drive. The SATA HDD daughter board is not assembled on the MIC-6311. The SATA HDD installation steps are illustrated in the following figures.

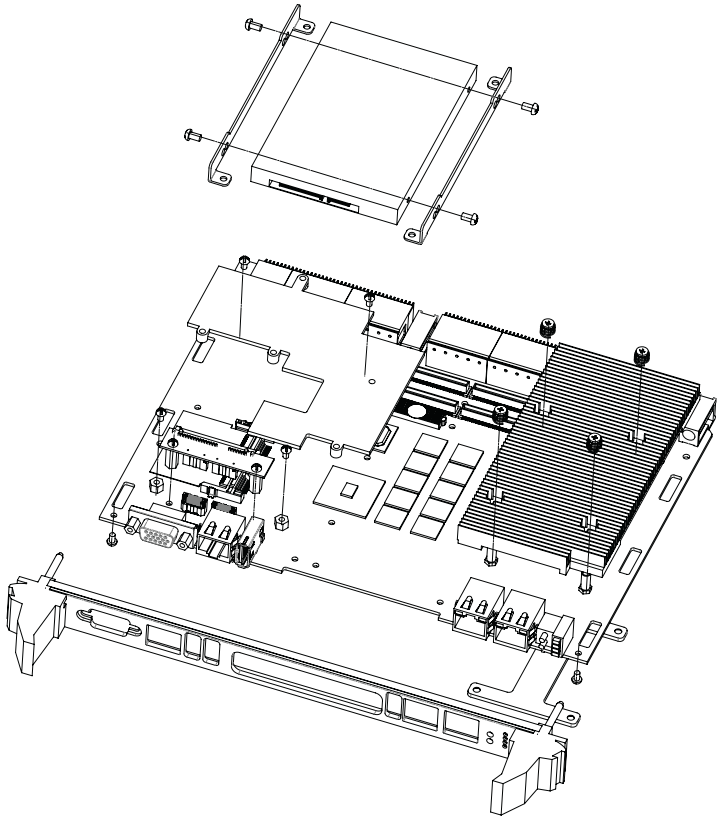


Figure 1.5 Complete assembly of MIC-6311 with SATA HDD

1. Align the HDD bracket to the side of the HDD, then use four M2.5 screws to fasten the bracket.

Figure 1.6 Fastening screws to the SATA HDD bracket

2. Place the SATA HDD with bracket on the post and insert the SATA HDD into the SATA connector.

Figure 1.7 Inserting the SATA HDD into the SATA connector

1.8.2 PMC/XMC Installation

MIC-6311 supports PMC/XMC cards compliant to standard PMC form factors. The following steps illustrate the installation of the PMC/XMC.

1.9 Battery Replacement

MIC-6311 uses a 3 V, 210 mAh battery (model number CR2032M1S8-LF). Replacement batteries can be purchased from Advantech. Before ordering a battery, please contact your local Advantech sales office to check availability.

1750129010 – BATTERY 3V/210 mAh with WIRE ASS'Y CR2032M1S8-LF

1.10 Software Support

Windows 7, Fedora 17 and Red Hat Enterprise Linux have been thoroughly tested on MIC-6311. Please contact your local sales representative for details or support regarding alternative operating systems.

Chapter 2

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

This section describes the BIOS, which was specifically adapted to MIC-6311. The AMI BIOS Setup program can be used to modify BIOS settings and control the special features of MIC-6311. The setup program comprises numerous menus with options for changing or turning the special features on or off. Basic navigation of the MIC-6311 setup screens is explained in this chapter.

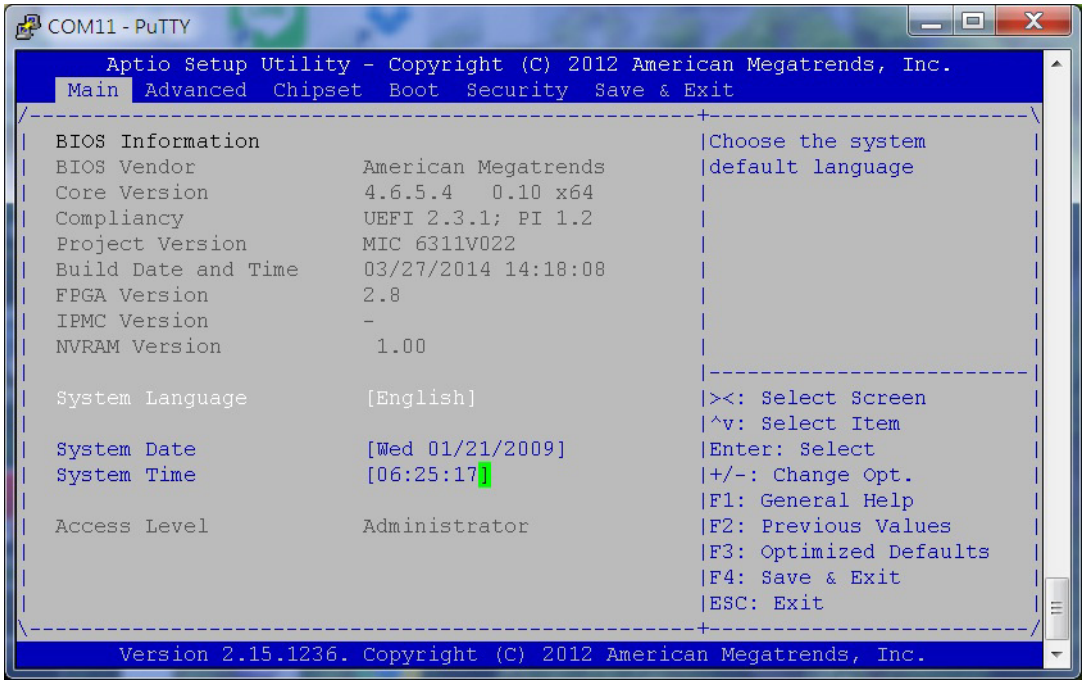


Figure 2.1 Setup program initial screen

2.2 BIOS Setup

The MIC-6311 board features an in-built AMI BIOS and a SETUP utility that allows users to configure the required settings or activate specific system features.

When the power is turned on, press the <Del> button during the BIOS POST (Power On Self-Test) to access the SETUP screen.

Control Keys	
< ↑ >< ↓ >< ← >< → >	Move to select an item
<Enter>	Select Item
<Esc>	Main Menu - Quit without saving changes Sub Menu - Exit current page and return to Main Menu
<Page Up/+>	Increase numeric value or make changes
<Page Down/->	Decrease numeric value or make changes
<F1>	General help, opens the Setup Sub Menu
<F2>	Previous values
<F3>	Optimized defaults
<F4>	Save and exit

2.3 Entering Setup

After turning on the computer, users should see a POST (Power On Self-Test) screen showing the BIOS supporting the CPU. If no number is assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file to ensure that the CPU system status is valid. After ensuring that a number is assigned to the patch code, press <F2> or <DEL> for immediate access to the Setup.

2.3.1 Main Setup

Upon initially entering the BIOS setup utility, users land on the main setup screen. Users can return to the main setup screen by selecting the **Main** tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

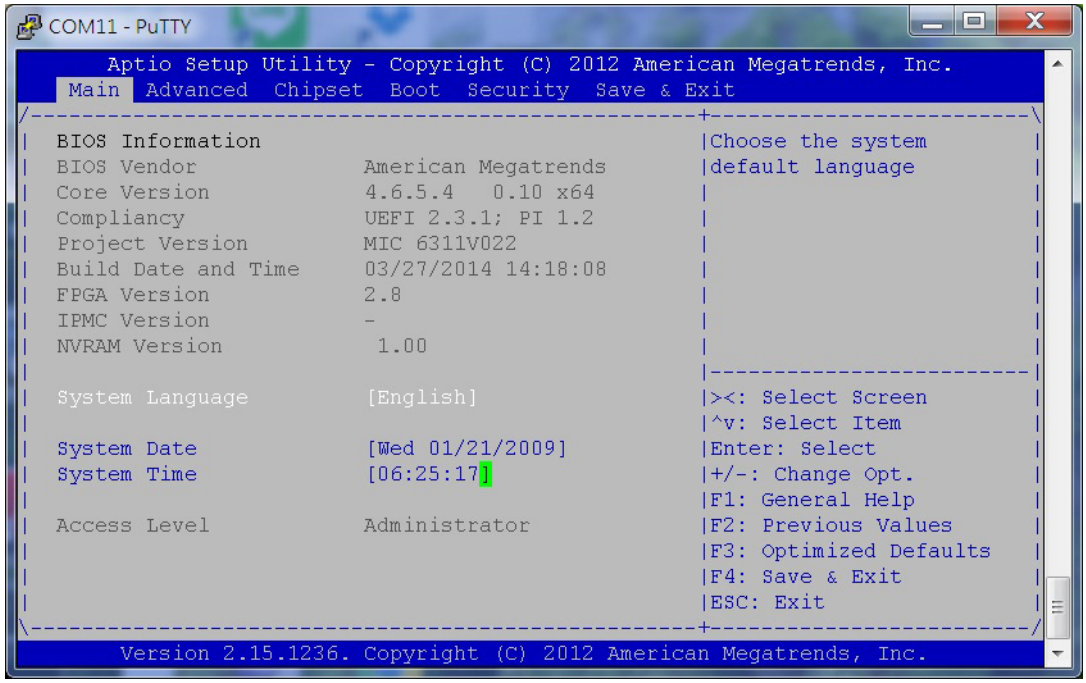


Figure 2.2 Main setup screen

The main BIOS setup menu screen comprises two primary frames. The left frame displays all options that can be configured. The “grayed-out” options cannot be configured, whereas the blue options can. The right frame displays the key legend. The area above the key legend is reserved for text messages. When an option is selected in the left frame, it appears highlighted in white and is often accompanied by a text notification.

- **System Time / System Date**

  Use this option to change the system time and date. Select “System Time” or “System Date” using the <Arrow> keys. Enter new values using the keyboard. Press the <Tab> or the <Arrow> keys to move between fields. The date must be input in MM/DD/YY format. The time is input in HH:MM:SS format.

2.3.2 Advanced BIOS Features Setup

Select the **Advanced** tab from the MIC-6311 setup screen to enter the Advanced BIOS Setup screen. Users can select any item, such as CPU Configuration, in the left frame of the screen to access the sub menu for that item. The details of each Advanced BIOS Setup option can be displayed by using the <Arrow> keys to highlight the desired item. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are also described in subsequent sections.

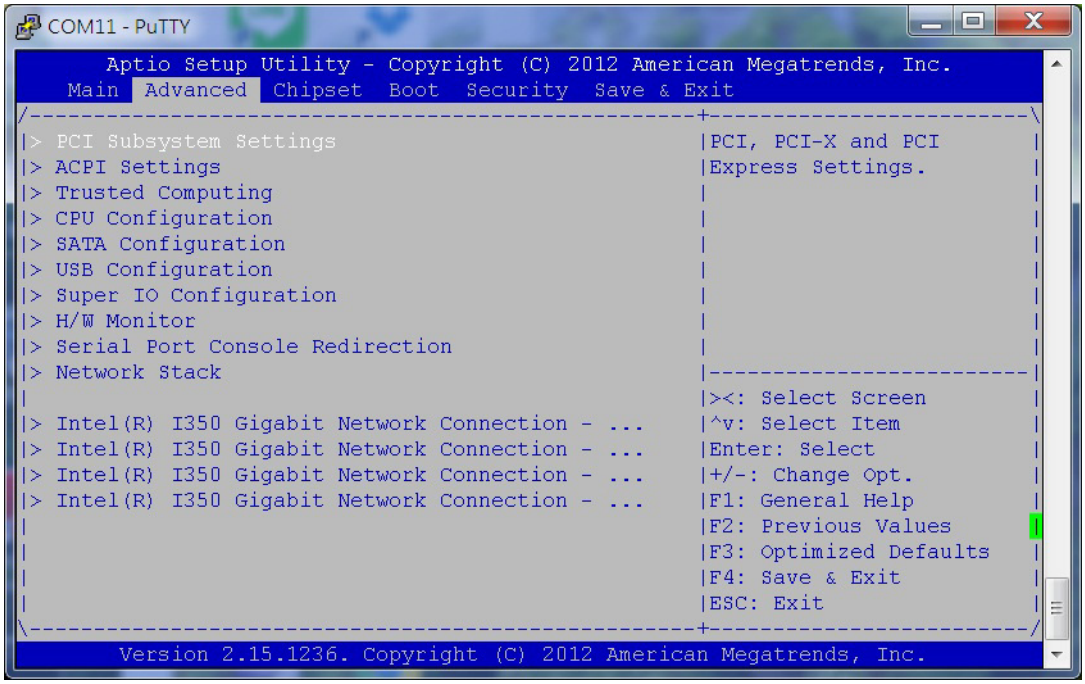


Figure 2.3 Advanced BIOS features setup screen

2.3.2.1 PCI Subsystem Setting

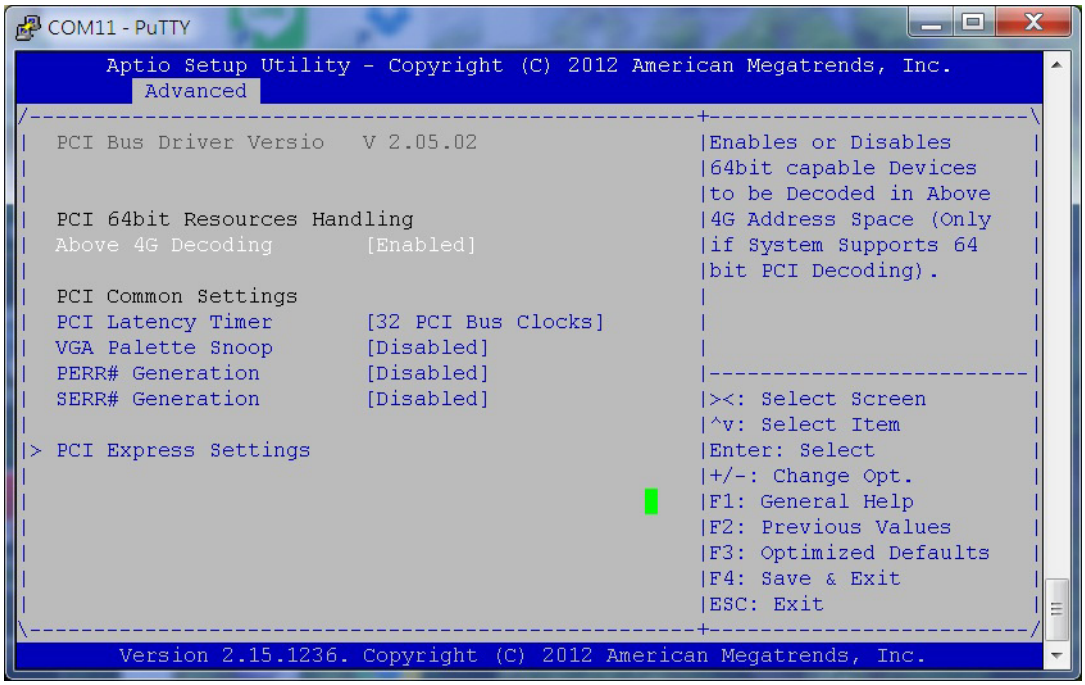


Figure 2.4 PCI settings

- **PCI Bus Driver Version**
- **Above 4G Decoding**

  This item allows users to enable/disable the memory usability for above 4G addresses in 64-bit devices. A 64-bit OS is required to support this function.
- **Common PCI Settings**
- **PCI Latency Timer**

  Sets the value to be programmed in the PCI Latency Timer register, affecting the amount of time a parallel PCI bus master can hold the bus and maximize throughput, which potentially delays other devices waiting for bus ownership. The latency timer does not apply to PCI Express devices.
- **VGA Palette Snoop**

  Enables or disables VGA Palette Snoop for add-on display cards. VGA Palette Snooping is always disabled for on-board Intel graphics.
- **PERR/SERR#**

  Enable or disable to suppress the PCI bridge system error capability.
- **PCI Express Device Settings**

  Allows users to set maximum payload/maximum read requests.

2.3.2.2 ACPI Setting

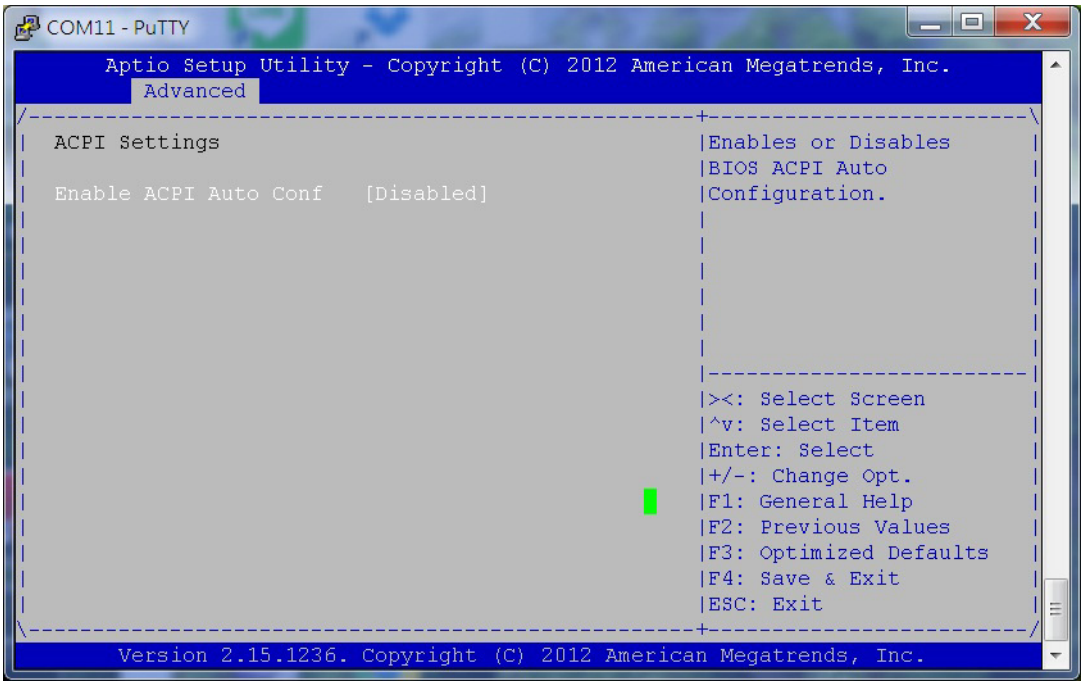


Figure 2.5 ACPI settings

- **Enable ACPI Auto Configuration**

  Enable or disable BIOS ACPI auto configuration. The following parameter is hidden when enabled.

2.3.2.3 CPU Configuration

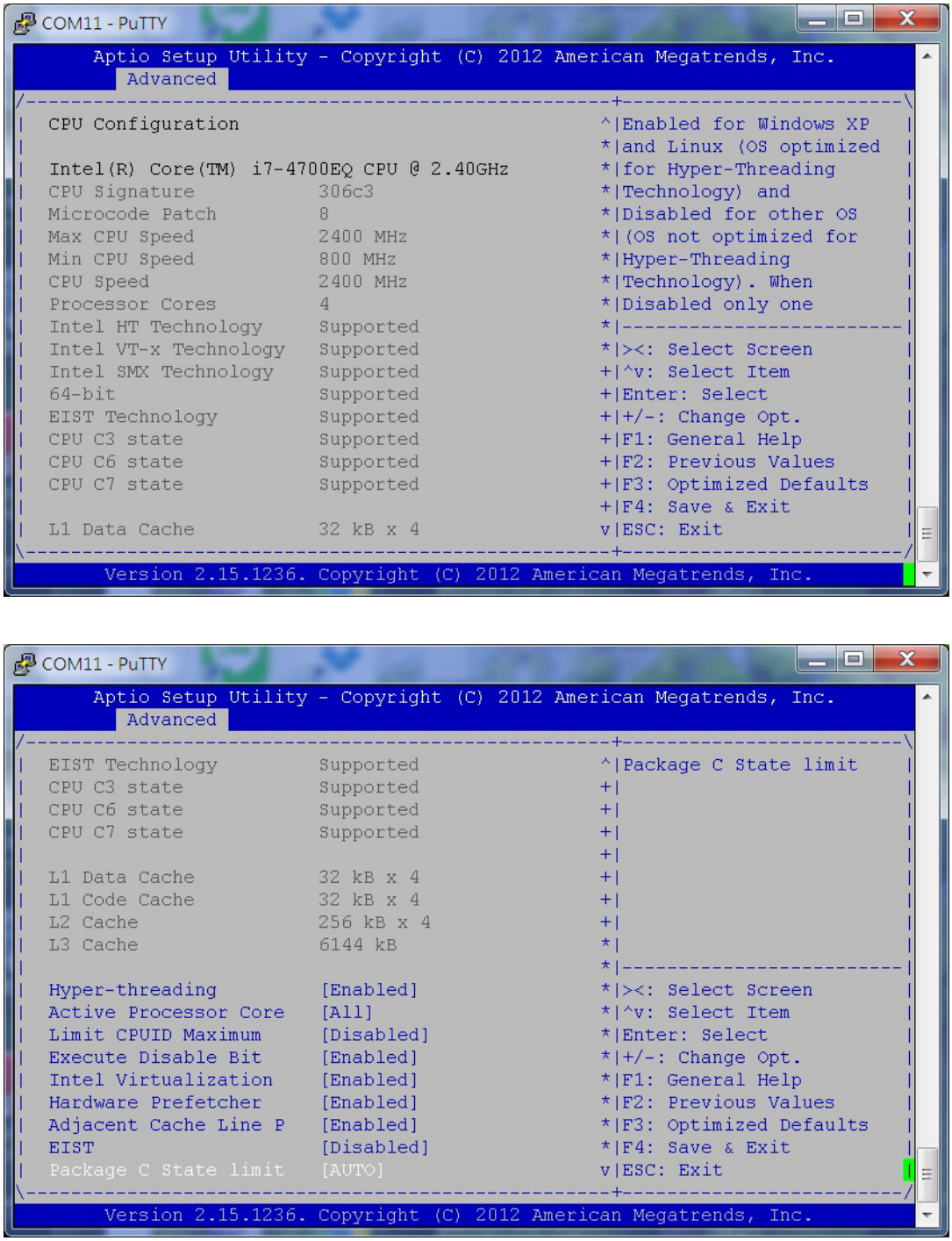


Figure 2.6 CPU configuration

- **Hyper-Threading**
  This item allows users to enable or disable Intel Hyper Threading technology.
- **Active Processor Core**
  This item allows users to choose the number of CPU cores to activate in each processor package.
- **Limit CPUID Maximum**
  This item allows users to limit the CPUID maximum value.

- **Execute Disable Bit**

  This item allows users to enable or disable No-Execute page-protection technology.

- **Intel Virtualization Technology**

  Intel Virtualization Technology (Intel VT) is a set of hardware enhancements for Intel server and client platforms that provide software-based virtualization solutions.

  Intel VT allows a platform to run multiple operating systems and applications on independent partitions, enabling one computer system to function as multiple virtual systems.

- **Hardware Prefetcher**

  The processor prefetches data and instructions that are likely to be required in the near future from the memory to the cache. This reduces the latency associated with memory reads.

- **Adjacent Cache Line Prefetcher**

  This item allows users to enable or disable the adjacent cache line prefetcher feature.

- **EIST**

  This option allows users to enable or disable CPU EIST (Enhanced Intel Speed-Step Technology)

- **Turbo Mode**

  Intel Turbo Boost is a technology implemented by Intel in certain versions of their Nehalem-, Sandy-Bridge-, Ivy-Bridge-, and Haswell-based CPUs. This technology allows the processor to operate above the base operating frequency by dynamically controlling the CPU's “clock rate,” and is activated when the OS requests the highest processor performance state. The processor performance states are defined in the Advanced Configuration and Power Interface (ACPI) specification, an open standard supported by all major OS. No additional software or drivers are required to support the technology. The design concept behind Turbo Boost is commonly referred to as “dynamic overclocking.”

- **Energy Performance**

- **CPU C states**

  This item allows users to turn off unused components to save power.

- **Enhanced C1 State**

  This item allows users to enable or disable the Enhanced C1 state (Enhanced Halt State) to reduce power consumption.

- **CPU C3 / C6 / C7Report**

  This item enables users to allow or disallow the CPU to enter C3 / C6 / C7 states.

- **Package C State limit**

  This item allows users to set the C states the CPU can enter.

- **Intel TXT(LT) Support**

  Intel Trusted Execution Technology (Intel TXT) verifies the authenticity of the platform and OS, ensuring that an authentic OS starts in a trusted environment and can, therefore, be considered a trusted OS. Intel TXT also provides a trusted OS with additional security capabilities not available to an unproven OS.

- **ACPI T State**

  T-states exist to prevent processors from burnout in the event of cooling fan failure. When a temperature sensor registers that the junction temperature is reaching a level that may damage the device or its contents, the HW power

manager assigns the processor to a T-state according to the temperature; the higher the temperature, the higher the T-state.

The standard processor running state is T0. When the processor enters a higher T-state, the manager clockgates the cores to slow execution and enable the processor to cool.

2.3.2.4 SATA Configuration

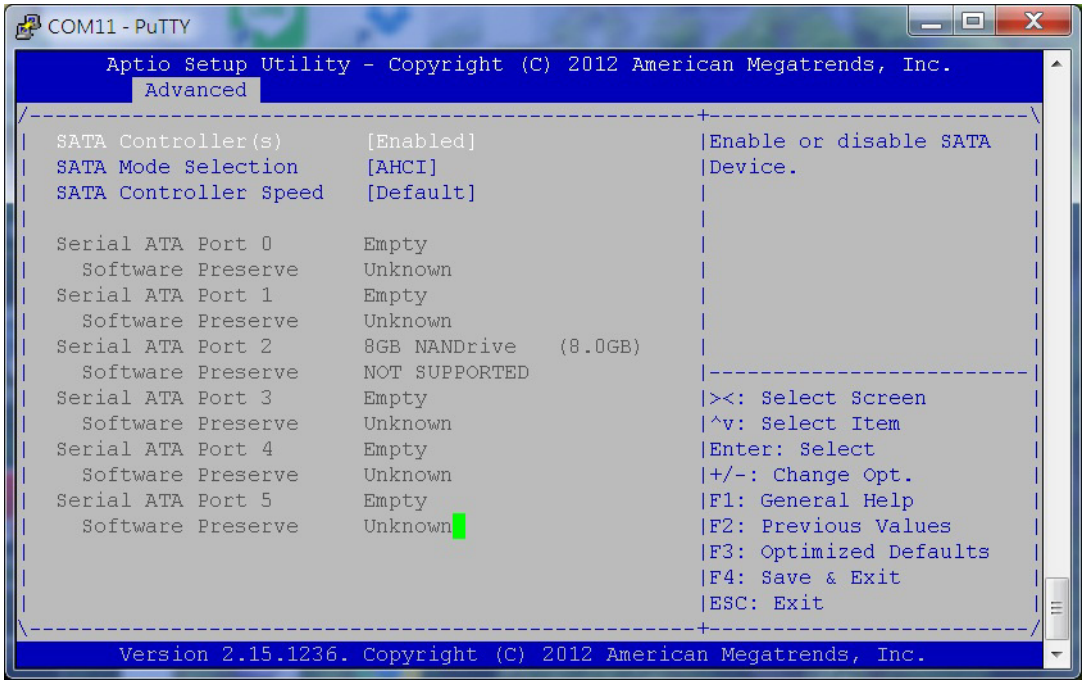


Figure 2.7 SATA configuration

- **SATA Controller**
  This item can only be accessed when the SATA mode is set as “IDE.”
- **[Disabled]**
  This items indicates that SATA function is disabled.
- **SATA mode selection**
  This item can be configured as IDE or AHCI mode.
- **SATA Controller Speed**
  This can be Gen1/Gen2/Gen3.
- **Disable**
  This items allows users to disable SATA function.
- **IDE mode**
  Set to “IDE” mode to use the serial ATA hard disk drives as parallel ATA physical storage devices.
- **ACHI mode**
  Set to “AHCI” mode to assign SATA hard disk drives to use the Advanced Host Controller Interface. In AHCI mode, the onboard storage driver enables advanced serial ATA features that increase storage performance for random workloads by internally optimizing the command order.

2.3.2.5 USB Configuration

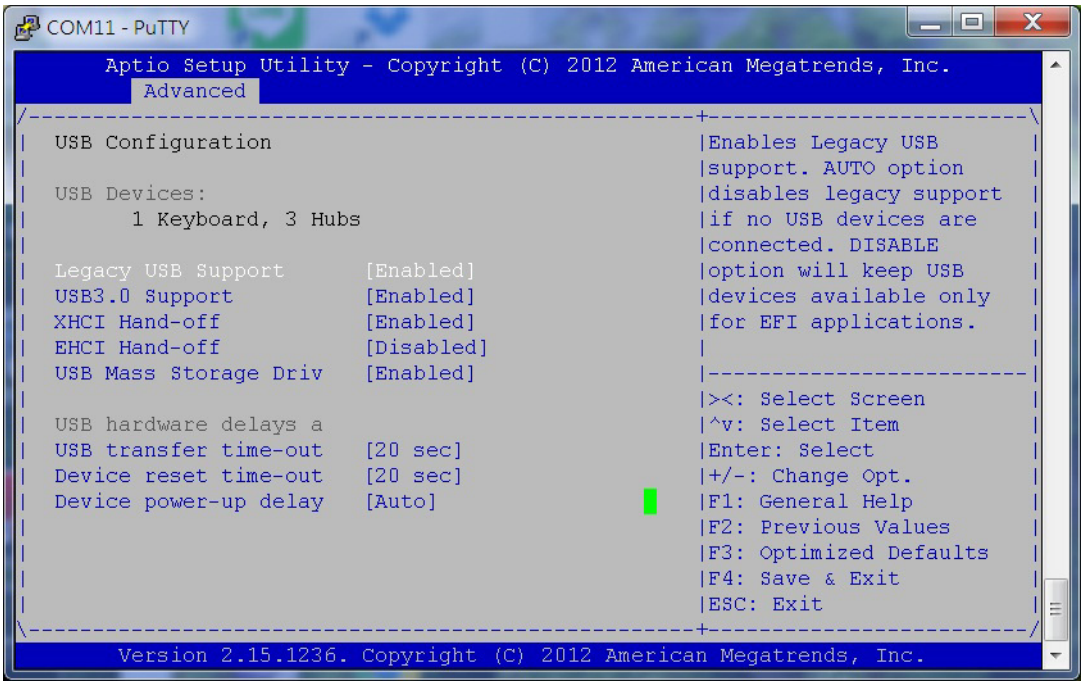


Figure 2.8 USB configuration

- **Legacy USB Support**
  Enables support for legacy USB. The auto option disables legacy support if no USB devices are connected.
- **USB3.0 Support**
  Enables support for USB 3.0.
- **XHCI /EHCI Hand-off**
  This item is a workaround for an OS without XHCI / EHCI hand-off support.
- **Mass Storage Devices**
  Shows details of USB mass storage devices.
  USB hardware delays and time-outs:
- **USB Transfer Time-outs**
  Sets the USB transfer time-out value for control, bulk, and interrupt transfers.
- **Device Reset Time-outs**
  Sets the time-out periods for USB device initialization and the Start Unit command to enable mass storage access operations.
- **Device Power-up Delay**
  Set the time allocated for devices to report themselves to the host controller through USB hubs. When set to Auto, root port devices are allocated 100 milliseconds, and devices connected to hubs are allocated the time specified in the hub descriptor. When this parameter is set to Manual, a delay of 1 to 40 seconds can be selected.
- **Device Power-up Delay in Seconds**
  The “device power-up delay in seconds” field must be enabled to set a delay of 1 to 5 seconds.

2.3.2.6 Super IO Configuration

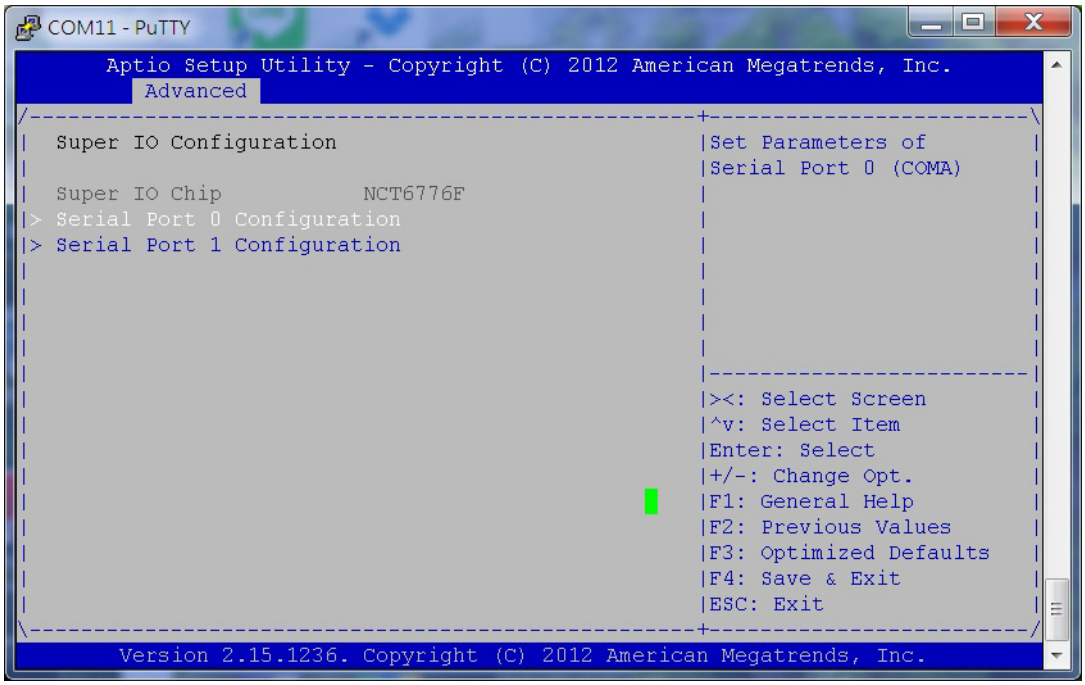
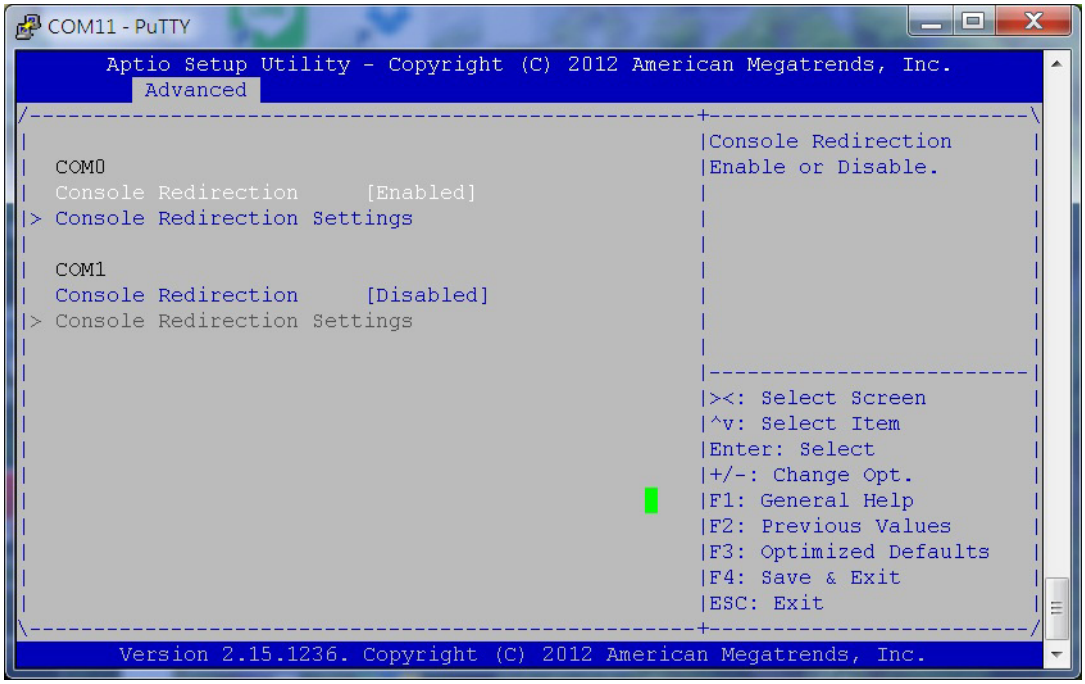


Figure 2.9 Super IO configuration

- **Serial Port Configuration**

  For serial port, IRQ and I/O mode resource configuration, users can select IRQ, IO and MODE.



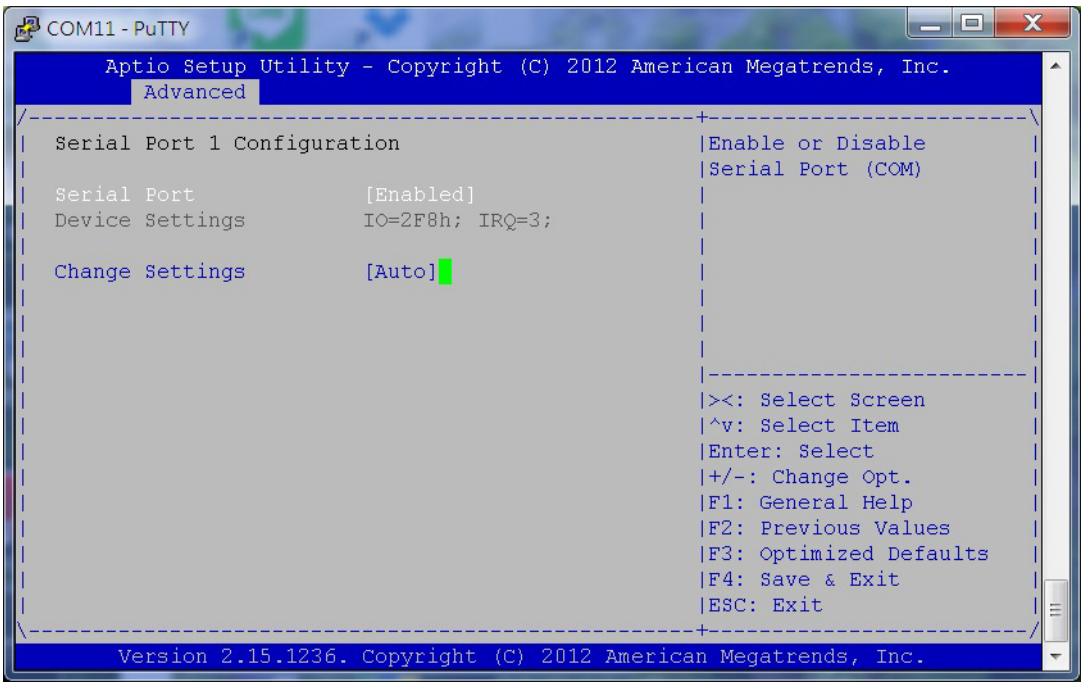
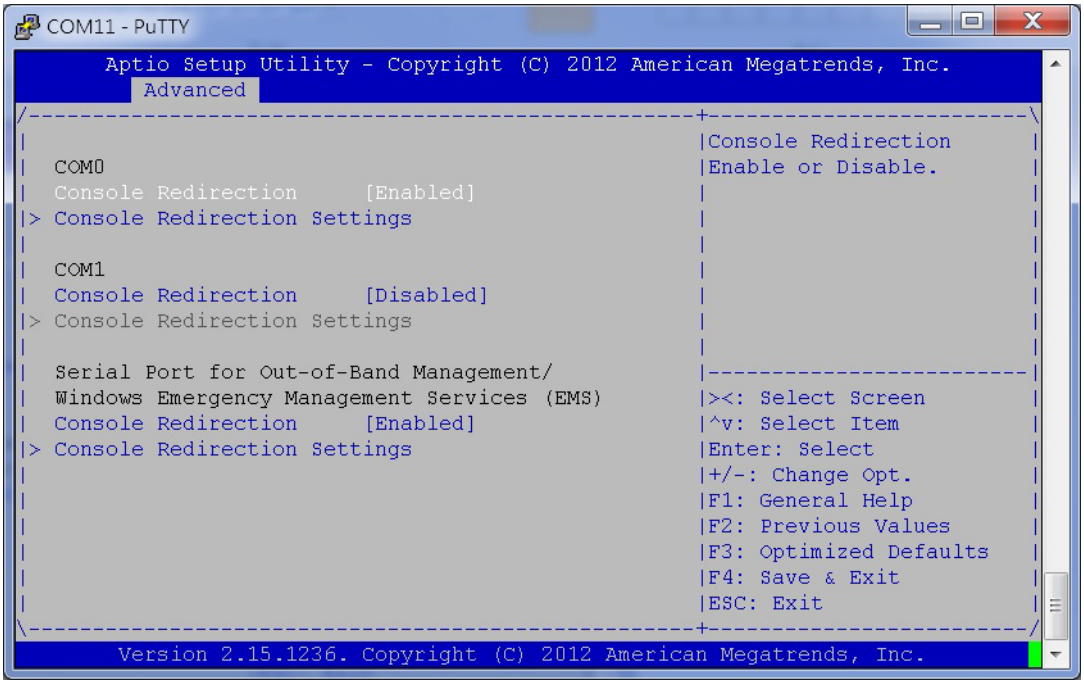


Figure 2.10 Serial port configuration

2.3.2.7 Serial Port Console Redirection Setting



- **Console Redirection**
  This item allows users to enable or disable console redirection or Microsoft Windows Emergency Management Services (EMS).

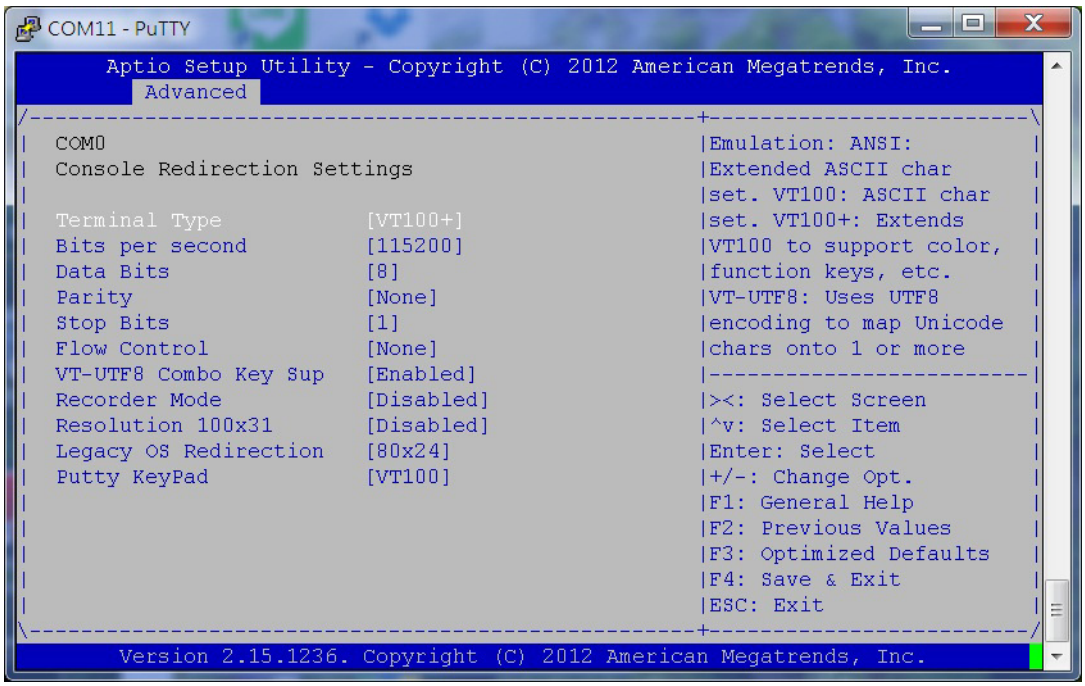


Figure 2.11 Console redirection settings

- **Terminal Type**

  VT-UTF8 is the optimal terminal type for out-of-band management, followed by VT100+ and then VT100.

2.3.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item, such as PCI Express Configuration, in the left frame of the screen to access the sub menu for that item. Users can view a Chipset Setup option by highlighting the item using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub menus are also described in subsequent sections.

2.3.3.1 PCH-IO Configuration

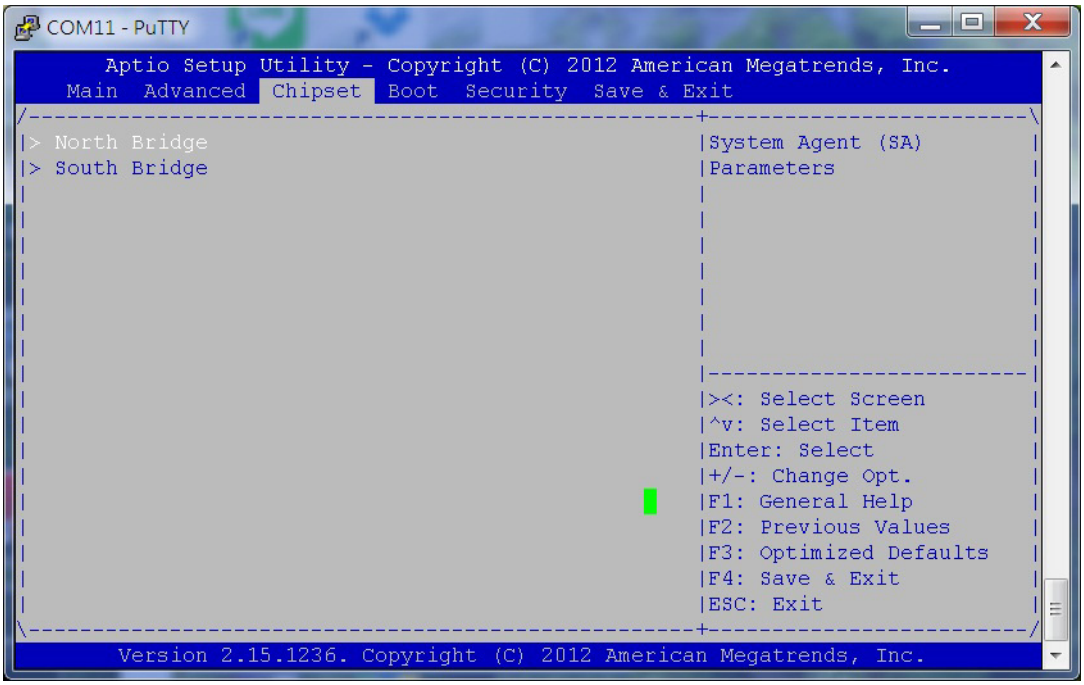


Figure 2.12 PCH-IO configuration

2.3.3.2 North Bridge Configuration

- **System Agent (SA) Configuration**

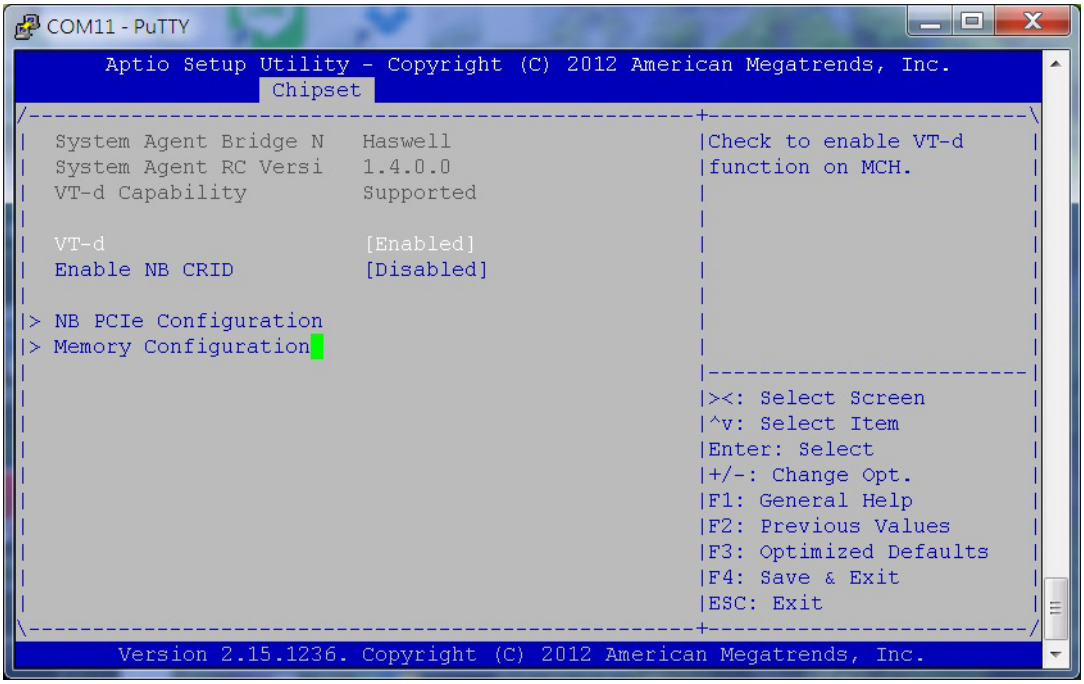


Figure 2.13 System Agent (SA) configuration

– **VT-d**
  This item allows users to enable or disable VT-d.
– **Enable NB CRID**
  Enable or disable NB CRID WorkAround.

NB PCIe Configuration

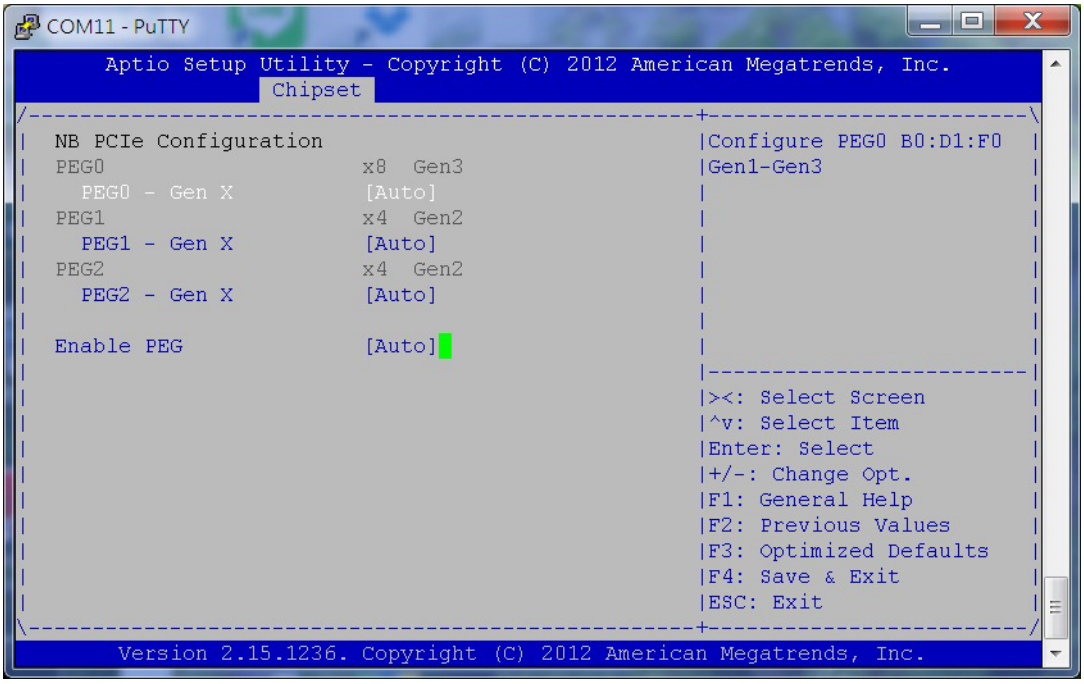


Figure 2.14 NB PCIe configuration

– **PEG0 – Gen x**
  Select PEG0 speed.
– **Always enabled PEG**
  This item allows users to always enable or disable PEG.

2.3.3.3 Memory Configuration

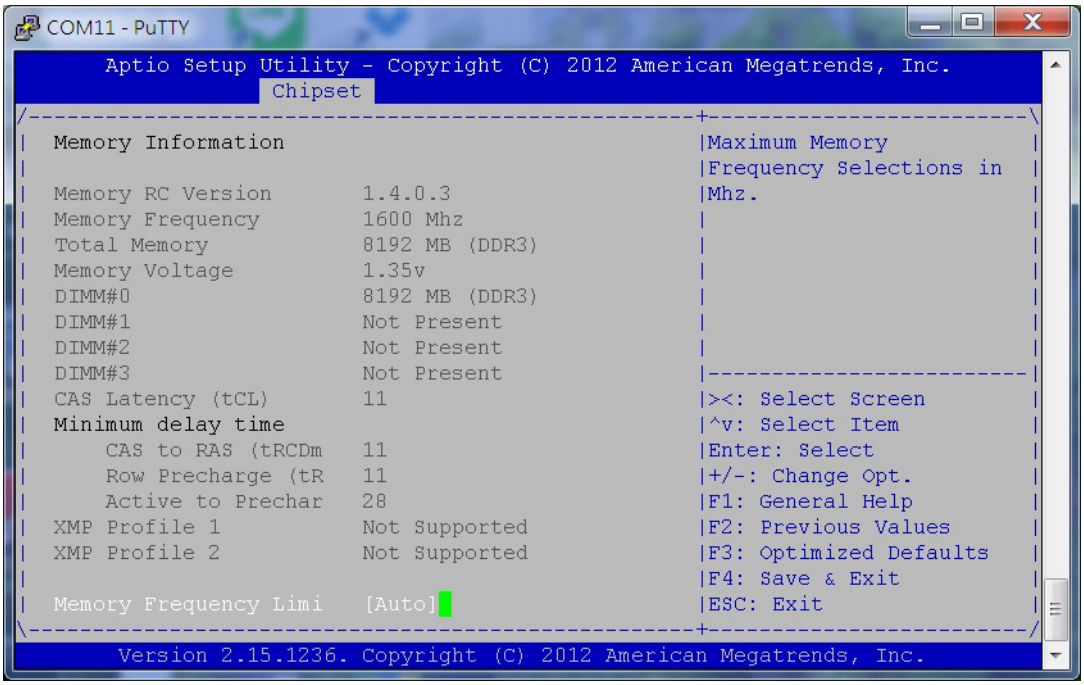


Figure 2.15 Memory configuration

- **DIMM Profile**
  This item allows users to select the DIMM timing profile used.
- **Channel A/B DIMM Control**
  This item allows users enable or disable DIMMs on Channels A or B.

2.3.4 Boot Settings

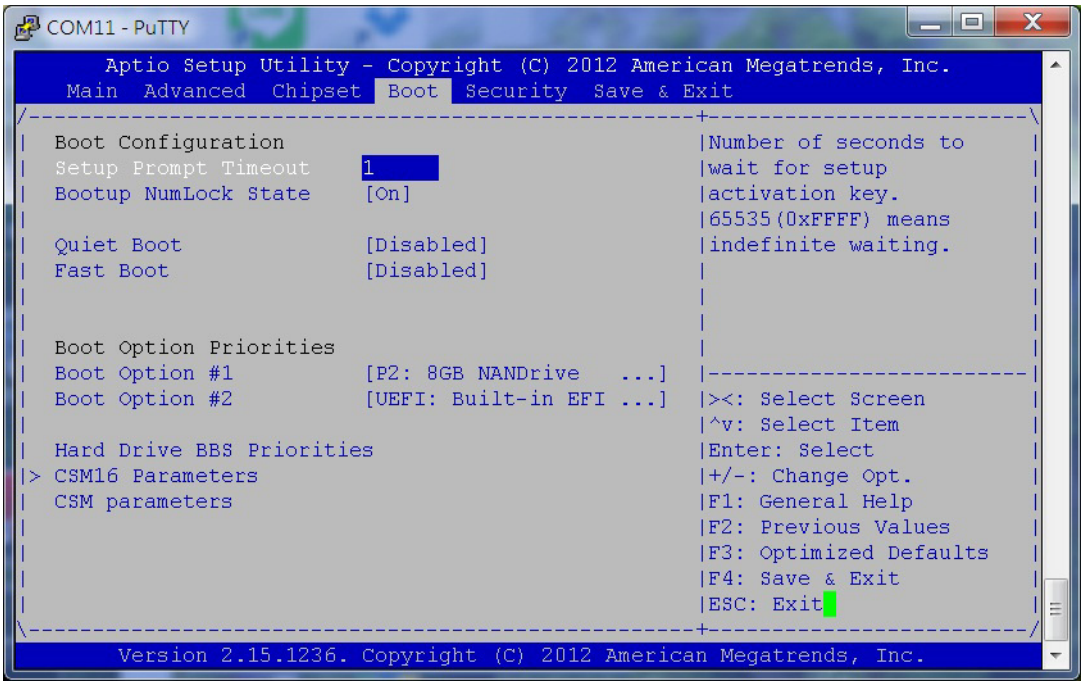


Figure 2.16 Boot settings

- **Setup Prompt Time-out**
  Number of seconds to wait for a setup activation key (65535 means indefinitely).
- **Bootup NumLock State**
  When “ON” the keyboard NumLock state will stay “ON” after booting. When “OFF” the keyboard NumLock state will stay “OFF” after booting.
- **Quiet Boot**
  If this option is set to Disabled, the BIOS displays normal POST messages. If enabled, an OEM logo is shown instead of POST messages.

- **Fast Boot**
  This item allows the BIOS to skip certain tests when booting. This reduces the time required to boot the system.
- **Boot Option Priority**
  Boot Option #1
  Boot Option #2
  Boot Option #3
  Boot Option #4
  Shows the boot device choices.
- **CSM16 Parameters**
- **Option ROM Message**
  Sets display mode for Option ROM.
- **INT 19 Trap Response**
  When set to Enable, this item allows users to use Option ROMs to trap Int 19.
- **CSM Parameters**
  This item allows users to configure the boot settings.
- **Launch CSM**
- **Boot option filter**
  This item controls the devices that the system boots to.
- **Launch PXE OpROM Policy**
  This item controls the execution of UEFI and Legacy PXE OpROM (Option-ROM).
- **Launch Storage OpROM**
  This item controls the execution of UEFI and Legacy Storage OpROM.
- **Launch Video OpROM Policy**
  This item controls the execution of UEFI and Legacy Video OpROM.
- **Other PCI device ROM**
  For non network, mass storage, or video PCI devices, this item defines which OpROM to launch.
- **GateA20 Active**
  UPON REQUEST: GA20 can be disabled using BIOS services.
  Always: do not allow disabled GA20.
- **Interrupt19 Capture**
  Enable or disable this item for ROM to trap into 19.
- **Hard Drive BBS Priorities**
  Select the main hard disk device type to function as a boot hard drive.

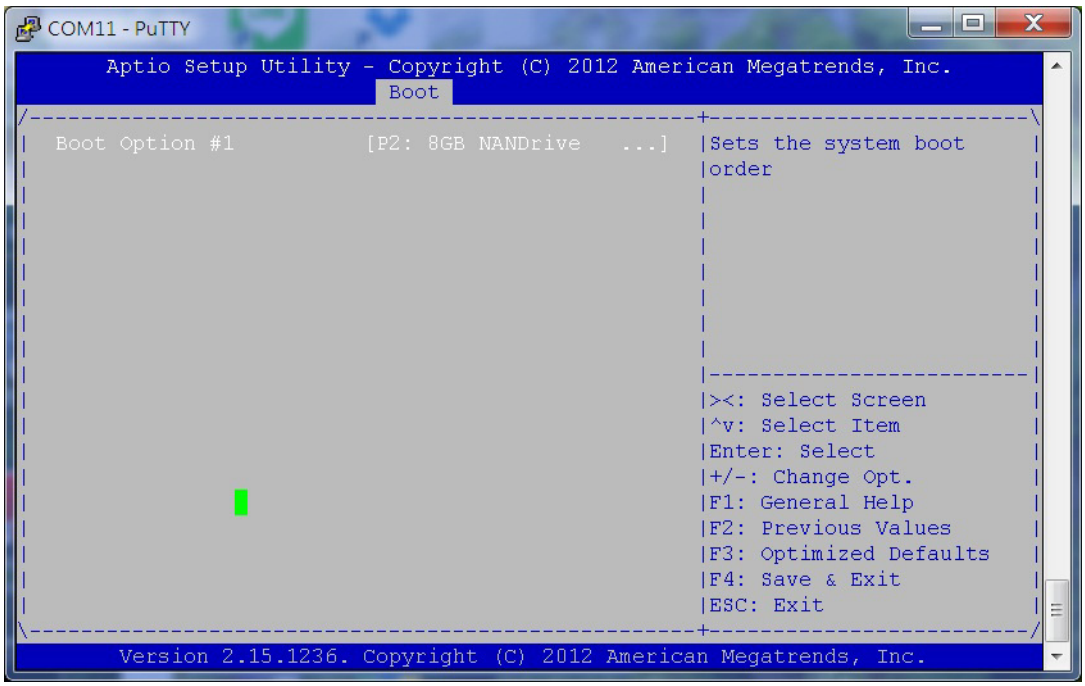


Figure 2.17 Choose boot option priority

2.3.5 Security Settings

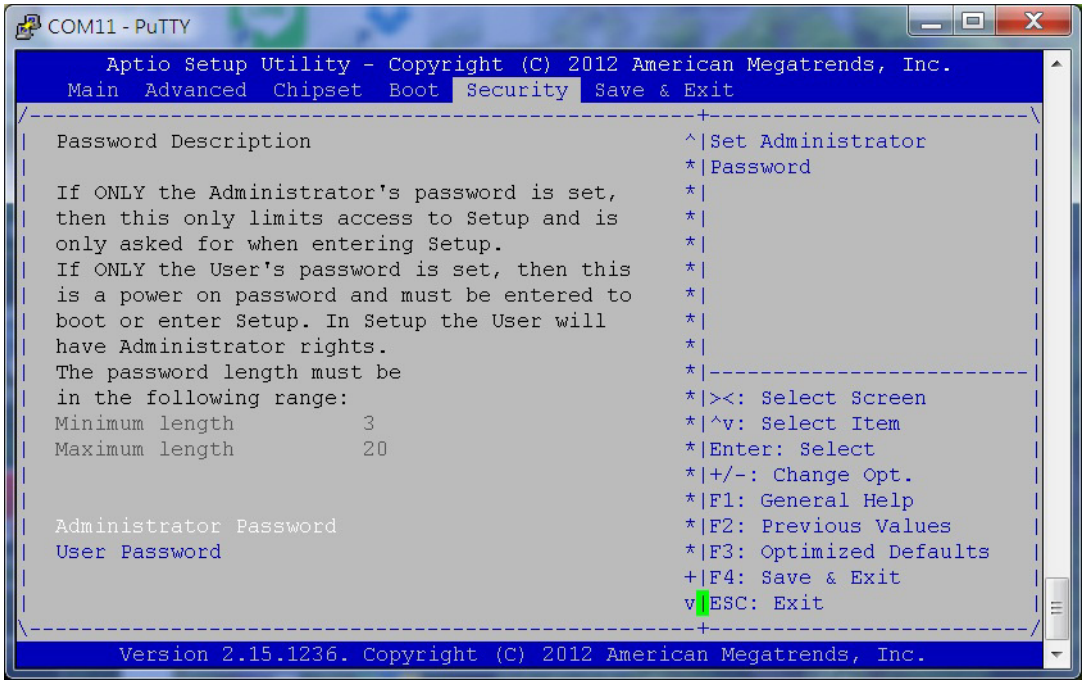


Figure 2.18 Security settings

- **Administrator Password**
  Select this option and press <ENTER> to access the sub menu, then input a password. Set the Administrator password.
- **User Password**
  Select this option and press <ENTER> to access the sub menu, then input a password. Set the User password.

2.3.6 Server Management

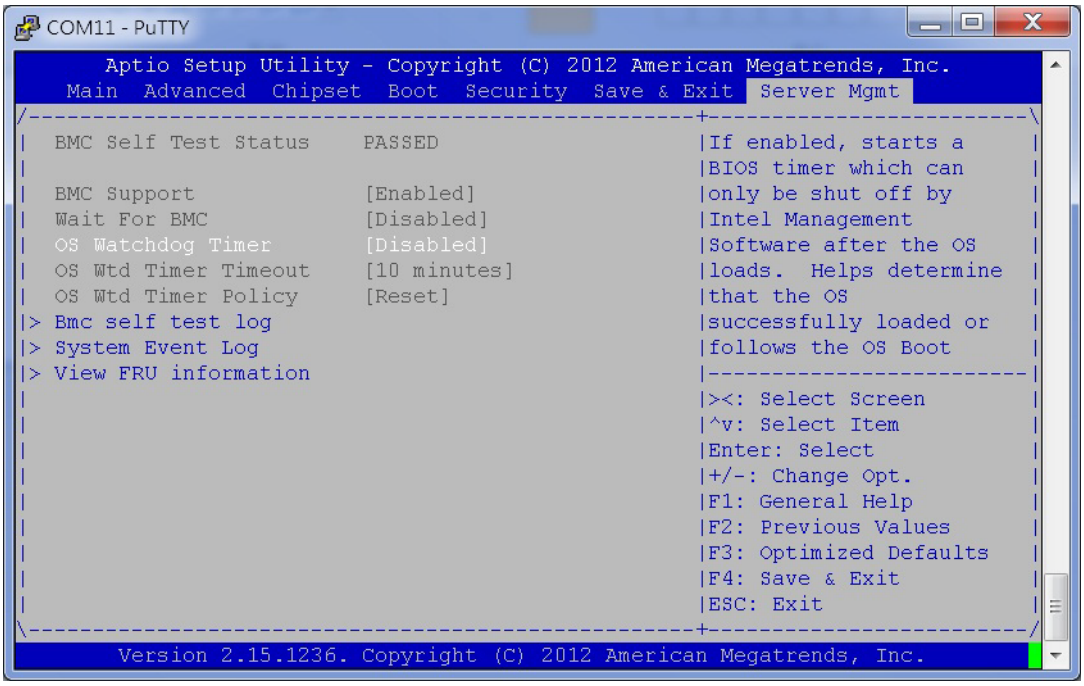


Figure 2.19 Server management

- **BMC Self Test Status**

  Use this information to resolve BMC self-test errors by referencing the error codes and following the suggested corrective actions.
- **BMC Support**
- **Wait for BMC**

  Allows users to set the number of seconds to wait for BMC. Use the <+> and <-> keys to adjust the value.
- **FRB-2 Timer**

  The FRB-2 timer is started during POST and used to recover the system if necessary.
- **FRB-2 Timer Time-out**

  Enter a value between 3 to 6 minutes to set the FRB timer expiration value.
- **FRB-2 Timer Policy**

  Allows users to configure the system response should the FRB-2 timer expire. Not available if the FRB-2 timer is disabled.
- **OS Watchdog Timer**

  If enabled, this item starts a BIOS timer that can only be deactivated using Intel Management Software after the OS loads. This indicates whether the OS has successfully loaded or follows the O/S Boot Watchdog Timer Policy.
- **OS Watchdog Timer Time-out**

  Allows users to configure the length of the O/S Boot Watchdog Timer. Not available if the O/S Boot Watchdog Timer is disabled.
- **OS Watchdog Timer Policy**

  Allows users to configure the system response should the OS Boot Watchdog Timer expire. Not available if the O/S Boot Watchdog Timer is disabled.

- **BMC Self-Test Log**
  Allows users to choose options for erasing the log and responses to a full log.
- **System Event Log**
- **SEL Components**
  This item allows users to enable or disable all system event log features during boot.
- **Erase SEL**
  Allows users to choose options for erasing the SEL.
- **When SEL is Full**
  Allows users to choose options for reactions to a full SEL.
- **Log EFI Status Codes**
  This item allows users to disable the logging of EFI status codes or log only error codes, only progress codes, or both.

2.3.7 Save and Exit Configuration

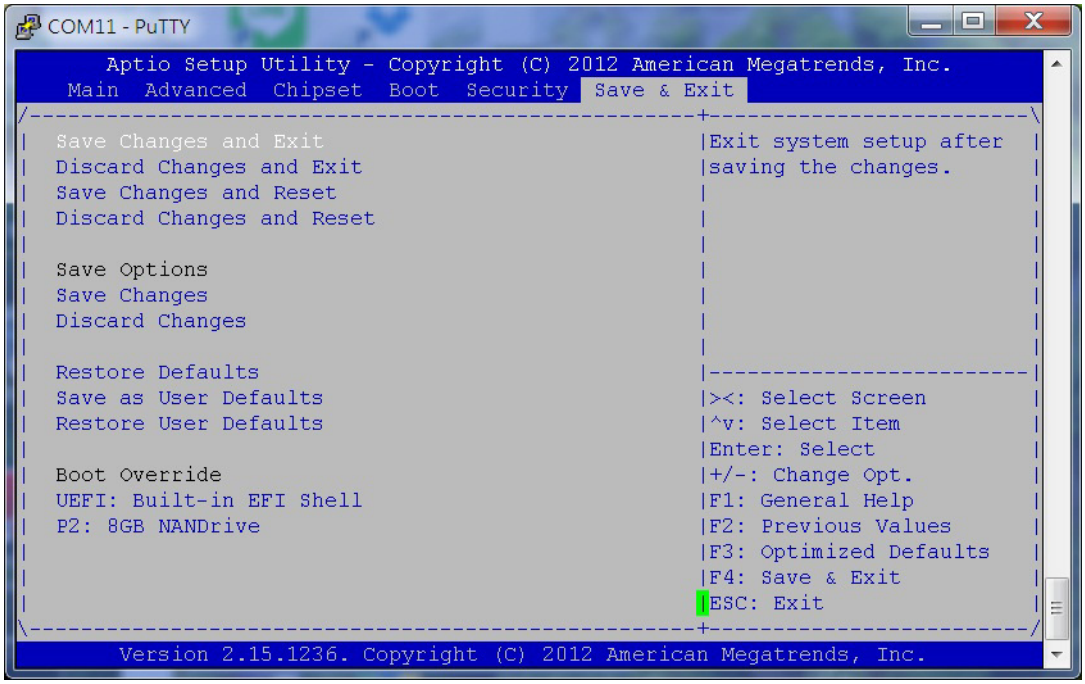


Figure 2.20 Save and exit configuration

- **Save Changes and Exit**
  Upon completing the system configuration, select this option to save changes, exit the BIOS setup menu and reboot the computer for all system configuration parameters to take effect.
  1. Select Exit and Save Changes in the Exit menu and press <Enter>. The following message should appear: “Save Configuration Changes and Exit Now [OK] [Cancel]”
  2. Select OK or Cancel.
- **Discard Changes and Exit**
  Select this option to quit setup without making permanent changes to the system configuration.
  1. Select Exit and Discard Changes in the Exit menu and press <Enter>. The following message should appear: “Discard Changes and Exit Setup Now [Ok] [Cancel]”

2. Select OK to discard changes and exit. To discard changes only, select Discard Changes in the Exit menu and press <Enter>.

- **Restore Defaults**

  The BIOS automatically changes all setup items to the optimal default settings when this option is selected. Defaults are designed for maximum system performance, but may not be ideal for all computer applications. Specifically, do not implement the default settings if the computer is experiencing system configuration problems. Instead, select Restore Defaults in the Exit menu and press <Enter>.

- **Save as User Default**

  Save all of the current settings as a user default.

- **Restore User Default**

  Restore all settings to user default values.

- **Boot Override**

  Show the boot device types on the system.

Chapter 3

BMC Firmware Operation

This chapter describes the BMC firmware features.

3.1 Module Management

The IPMI Baseboard Management Controller (BMC) located on the MIC-6311 is the essential part of the Board. It acts as standard IPMI management controller. Main tasks are module health (monitoring voltage and temperature sensors), payload state management, information data storage and provision of several IPMI communication interfaces.

3.2 IPMI Interfaces

The MIC-6311 provides three main IPMI messaging interfaces to connect to the modules BMC. These are the local IPMB bus (IPMB) for basic communication with other modules in the Chassis, the LAN side band interface (RMCP/RMCP+) and the onboard payload interface to x86 (KCS).

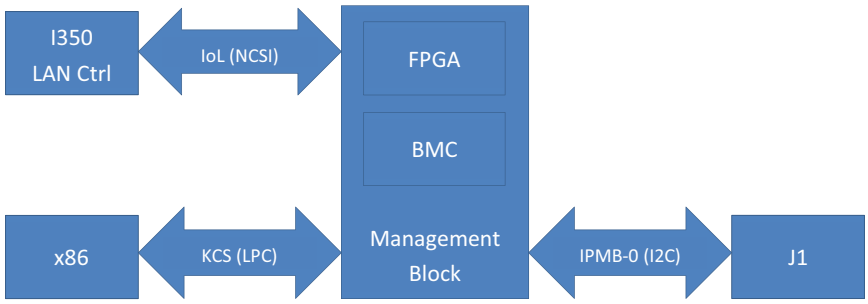


Figure 3.1 IPMI interfaces

3.2.1 IPMB

Basic IPMI connection of a BMC is the I2C based, serial IPMB interface routed to the backplane connector. Once plugged in a backplane and supplied with management power, the BMC discovers the slot connector Geographic Address (GA). The GA is used to assign a unique IPMB address according to the slot number. With this IPMB address, the BMC is able to communicate with other parts in the chassis.

The open source IPMI tool can be used to access the BMC via IPMB.

3.2.2 KCS

The Keyboard Controller Style (KCS) protocol is used as IPMI system interface connection to the x86 part on MIC-6311. It's based on the Low Pin Count (LPC) bus and used as the local BMC interface to BIOS and the Operating System (OS) on the Board. KCS is a fast IPMI interface compared to IPMB, but requires active payload.

IPMI driver support is needed to be able to use the IPMI tool from OS level via the KCS BMC interface (refer to chapter H - Driver and Tools-). With a working IPMI driver, the BMC can be easily accessed from OS via KCS. No interface parameters are needed at all, to use the local onboard IPMI connection:

```
ipmitool <Command>
```

3.2.3 LAN

The IPMI LAN Interface on MIC-6311 is accomplished by using a shared LAN Controller together with the x86 system. In addition to systems PCI-Express link, a LAN controller side-band interface (Network Controller Sideband Interface, short NC-SI) is connected to the BMC. This NC-SI channel is used by the BMC to receive and transmit IPMI management traffic from and to network with help of the LAN controller.

IPMI over LAN (IOL) uses the Remote Management Control Protocol (RMCP, specified in IPMI v1.5) in request-response manner for IPMI communication. IPMI v1.5 LAN messages are encapsulated in RMCP packets, while IPMI v2.0 specification added an enhanced protocol (RMCP+) for transferring IPMI messages and other types of payloads. RMCP+ uses RMCP overall packet format, but defines extensions, such as encryption and the ability to carry additional traffic types (e.g. serial data) in addition to IPMI messages (refer to 3.11).

Three of MIC-6311's Ethernet interfaces can be used for IPMI over LAN:

- Both backplane interfaces: Port 0 and 1
- The front panel LAN RJ-45 connectors

Note! *The LAN controller used for IPMI communication is connected to the payload power domain. Thus, the payload needs to be powered, to be able to use IPMI over LAN.*

Following IPMItool parameters are needed to connect to the BMC vial LAN:

```
ipmitool -I lan -H <IP-Address> -U <User> -P <Password>
<Command>
```

Command Line Syntax:

I lan	Specifies Ethernet interface
H <IP-Address>	IP address assigned to the BMC
U <User>	User account, default "administrator"
P <Password>	Password used with specified user account (default password for user "administrator" is "advantech")

3.3 Sensors

Monitoring board voltages and temperatures in one of the main tasks of the BMC populated on the MIC-6311. All important voltages and temperatures are connected to the BMC sensor part.

Moreover, the BMC Management Subsystem also registers below logical sensors:

- PICMG Hot Swap sensor
- BMC Watchdog sensor
- FW Progress sensor
- Version change sensor
- Advantech OEM Sensor: Integrity Sensor

3.3.1 Sensor List

All sensors available on the MIC-6311 Board are listed in the table below (inclusive FRU Device Locator record):

Table 3.1: Sensor List

No.	Sensor ID	Sensor Type (Event/Reading Type)	Description
0	MIC-6311		IPMI FRU Device Locator
1	HOTSWAP	Hot Swap (Discrete)	Module Hot Swap sensor
12	VCC-RTC-VOL	Voltage (Threshold)	RTC supply voltage
15	CPU-TMP	Temperature (Threshold)	CPU PECI temperature
17	INTEGRITY	OEM	Advantech Integrity sensor
18	BMC_WATCHDOG	Watchdog 2 (Discrete)	IPMI BMC Watchdog sensor
19	FW_PROGRESS	System Firmware Progress (Discrete)	IPMI FW Progress sensor
20	VERSION_CHANGE	Version Change (Discrete)	IPMI Version Change sensor

3.3.2 Threshold Based Sensors

According to the IPMI specification, sensor event thresholds are classified as Non-critical, Critical, or Non-recoverable. When different thresholds are reached, different actions may be executed by the carrier or shelf manager (e.g. fan speed adjustment for temperature sensor events).

The table below lists the six sensor thresholds specified for threshold based sensors in the following sub-chapters.

Table 3.2: Threshold Descriptions

Threshold	Description
UNR	Upper Non-recoverable
UC	Upper Critical
UNC	Upper Non-critical
LNC	Lower Non-critical
LC	Lower Critical
LNR	Lower Non-recoverable

3.3.2.1 Voltage Sensors

All listed voltages listed below are monitored by the BMC and readable via IPMI.

Table 3.3: Voltage Sensor List

Sensor Name	Nominal Value	LNR	LCR	LNC	UNC	UCR	UNR
MP-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
V12-VOL	12.0	9.90	10.2	10.8	13.2	13.8	14.1
V5_0-VOL	5.00	4.40	4.50	4.75	5.25	5.50	5.60
V0_75-VOL	0.75	0.60	0.675	0.71	0.79	0.825	0.90
V1_8-VOL	1.8	1.58	1.62	1.71	1.89	1.98	2.02
V1_5-VOL	1.5	1.26	1.35	1.425	1.575	1.65	1.74
V1_0-VOL	1.0	0.88	0.90	0.93	1.07	1.10	1.12
V0_85-VOL	0.85	0.71	0.765	0.80	0.90	0.935	0.99
V1_05-VOL	1.05	0.88	0.945	0.99	1.11	1.155	1.22
V3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
VCC-RTC-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70

3.3.2.2 Temperature Sensors

The MIC-6311 supports some [FW2] temperature sensors, either via board populated IC's (e.g. TMP75) or readings from CPU/Chipset interfaces (PECI/SMBus).

Table 3.4: Temperature Sensor List

Sensor Name	Value	LNR	LCR	LNC	UNC	UCR	UNR
CPU-TMP	40	-15	-10	-5	80	90	105

3.3.3 Discrete Sensors

3.3.3.1 BMC Device Locator

Each BMC provides a PICMG compliant FRU device locator for the subsystem. This record is used to hold location and type information of the BMC.

3.3.3.2 BMC Watchdog Sensor

The BMC Watchdog sensor is supported according to the Watchdog 2 sensor type listed in the IPMI specification.

3.3.3.3 FW Progress Sensor

The BMC SDR contains a FW Progress sensor in order to support logging of the OS boot process.The BMC supports adding and forwarding of SEL entries from the BIOS/OS system firmware progress events by sending 'Add sel entry' commands with the matching sensor type to the BMC through the KCS interface.

3.3.3.4 Version Change Sensor

A Version Change sensor is supported according to the IPMI specification.

3.3.4 Example Sensor Data

Below example shows a MIC-6311 sensor reading list printed with the open source IPMItool:

```
[root@localhost ~]# ipmitool sdr list
TBD
```

```
[root@localhost ~]# ipmitool sdr elist all
TBD
```

3.3.5 Integrity Sensor

3.3.5.1 Overview

The Advantech Integrity Sensor is an OEM sensor according to the SDR (Sensor Data Record) definitions in the IPMI specification. Its main purpose is to monitor internal firmware states and report events to the operator that would otherwise go unnoticed (hence “integrity sensor”).

Examples for those events are checksum errors, firmware update success/failure, firmware rollbacks.

3.3.5.2 Sensor Characteristics

The Integrity sensor does not support sensor reading, but generates event messages only. These events are stored in the local System Event Log (SEL) and sent to the default event receiver.

The event message contains three bytes of event data. The first byte defines how the event is supposed to be treated: the value of 0xA0 defines that event data 2 and 3 contain OEM data (please verify the IPMI specification for details on OEM sensors).

Event data 2 is used to identify which component the event relates to. This can either be a HPM.1 component, a logical component/feature on the board (for example FRU, RTC) or simply a board specific event.

Event data 3 [7..3] identifies the action or a subcomponent. For example: If the component in byte 2 was a HPM.1 component, it might report if this was an update, a rollback, or boot failure. If the component in byte 2 was “FRU”, it might indicate the subcomponent = area within the FRU that the event relates to.

Event data 3 [2..0] holds the result code. For the HPM.1 example above, it might report that an update or rollback either succeeded or failed. For the FRU example, it might indicate a checksum error.

3.3.5.3 Event Data Byte Definition

The following list provides the exact Integrity sensor event bytes definition.

Table 3.5: Integrity Sensor Event Definitions

Data Byte	[Bit]	Description	Value	Event Data
1	[7:0]	IPMI Header	0xA0	Event data 2 & event data 3 used as OEM data
2	[7:0]	Component	0x00 – 0x07	HPM.1 component (FW, FPGA, BIOS…) Logical component (FRU, RTC…) Board specific event

Table 3.5: Integrity Sensor Event Definitions				
3	[7:3]	Action / Subcomponent	b00000 b00001 b00010 b00011 b00100 b00101 b00110 b00111 b01000 b01001 b01010 b01011 b01100 b01101 b01110 b01111… …b11111	Update Recovery/Rollback Manual Rollback Automatic Rollback Activation Flash 0 Boot Flash 1 Boot Common Header Internal Area Chassis Info Area Board Info Area Product Info Area Multi Record Area Time synchronization Graceful Shutdown Not defined yet… Not defined yet
3	[2:0]	Result	b000 b001 b010 b011 b100 b101 b110 b111	Successful Failed Aborted Checksum Error Timeout Initiated Finished Unspecified Error

3.3.5.4 Event Data Translation

The structured definition allows simple translation of each Integrity Sensor event message. Below is an example Integrity Sensor SEL event (0x0A0100). The three event data bytes could be translated in following manner:

Data 1: 0x0A: Header
Data 2: 0x01: logical Component (BMC FW)
Data 3: 0x00: b 0 0 0 0 00 0 0
Update Successful

The example Integrity Sensor event reports a successful BMC Firmware update.

3.3.5.5 Event Data Table

All event data combinations supported by the BMC Integrity Sensor can be found in following list.

Table 3.6: Integrity Sensor's Event Data Table				
Component	**Action / Subcomponent**	**Result**	**Byte 1**	**Byte2**
BMC FW	Update	Successful	0x01	0x00
	Update	Timeout	0x01	0x04
	Update	Aborted	0x01	0x02
	Activation	Failed	0x01	0x21
	Manual Rollback	Initiated	0x01	0x15
	Automatic Rollback	Initiated	0x01	0x1D
	Rollback	Finished	0x01	0x0E
	Rollback	Failed	0x01	0x09

Table 3.6: Integrity Sensor's Event Data Table				
	Graceful Shutdown	Timeout	0x01	0x74
FPGA	Update	Successful	0x02	0x00
	Update	Timeout	0x02	0x04
	Update	Aborted	0x02	0x02
	Recovery	Finished	0x02	0x0E
BIOS	Update	Successful	0x03	0x00
	Update	Timeout	0x03	0x04
	Update	Aborted	0x03	0x02
	Flash 0 Boot	Failed	0x03	0x29
	Flash 1 Boot	Failed	0x03	0x31

3.3.5.6 Example Event Identification

The Integrity Sensor is listed as last MIC-6311 sensor (verify below IPMItool example).

```
[root@localhost ~]# ipmitool sdr elist
…
INTEGRITY         | 10h | ns  | 193.100 | Disabled
```

As mentioned before, the Integrity Sensor does not provide a sensor reading (disabled), but supports event generation at any time.

Occurred events are stored as records in the System Event Log and can be read out with following IPMItool command:

```
[root@localhost ~]# ipmitool sel elist
…
e | 04/23/2012 | 10:13:31 | OEM | OEM Specific | Asserted
…
```

Detailed information to single system events (event data bytes) in the SEL can be displayed with IPMItool "sel get <entry>".

```
[root@localhost ~]# ipmitool sel get 0x0e
SEL Record ID          : 000e
 Record Type           : 02
 Timestamp             : 04/23/2012 10:13:31
 Generator ID          : 0074
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 10
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data            : a00100
 Description           : OEM Specific
```

The "Event Data" field reflects the three needed bytes to identify the occurred Integrity Sensor event.

3.4 FRU Information

The BMC provides IPMI defined Field Replaceable Unit (FRU) information about the Board. The MIC-6311 FRU data include general board information's such as product name, HW version or serial number. A total of 2 kB non-volatile storage space is reserved for the FRU data. The boards IPMI FRU information can be made accessible via all BMC interfaces and the information can be retrieved at any time.

3.4.1 FRU Information Access Commands

The FRU device IPMI commands are supported by the BMC to read and write the boards FRU information. Correct and board specific FRU data is programmed to each single module in factory.

Caution! Please be very careful using the regular IPMI FRU write command (avoid if possible). Wrong FRU data content could destroy the payload functionality!

3.4.2 Example FRU Data

Below example shows a default MIC-6311 FRU data excerpt (Board and Product Info areas) using the Linux "IPMItool":

3.5 OEM Commands

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI defined OEM/Group Network Function (NetFn) Codes 2Eh, 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response. Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The MIC-6311 BMC supports following Advantech IPMI OEM commands:

Table 3.7: OEM Command Overview

Command	LUN	NetFn	CMD
Store Configuration Settings	00h	2Eh, 2Fh	40h
Read Configuration Settings	00h	2Eh, 2Fh	41h
Read Port 80 (BIOS POST Code)	00h	2Eh, 2Fh	80h
Clear NVRAM data	00h	2Eh, 2Fh	81h
Read MAC Address	00h	2Eh, 2Fh	E2h
Load Default Configuration	00h	2Eh, 2Fh	F2h

3.5.1 IPMItool Raw Command

To be able to use the Advantech OEM commands with the open source IPMItool, users have to employ the "raw" command of IPMItool. Please find below command structure details of the IPMItool raw command.

General raw request:

```
ipmitool raw <netfn> <cmd> [data]
```

Response, if raw <netfn> is 2Eh (OEM/Group):

```
<IANA Enterprise Number> [data]
```

3.5.2 Configuration Setting OEM Commands

The Read and Store Configuration OEM commands can be used to read and change several important board settings. The following sub-chapters describe the needed command details.

3.5.3 LAN Controller Interface Selection

The BMC firmware provides an OEM IPMI command to allow users to switch the BMC connected NC-SI interface between one front panel LAN IO RJ-45 connectors and the backplane connector Base interface (Ports 0 & 1). These commands can be used to read out the actual selected IPMI-over-LAN / Serial-over-LAN interface and to change the selection.

LAN controller interface selection settings:

00h: Front panel LAN IO

01h: backplane connector LAN BI (default)

Read LAN Interface selection:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x00
```

Response:

```
39 28 00 <setting>
```

Change LAN Interface selection:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x00 <setting>
```

Response:

```
39 28 00
```

3.5.4 LAN Controller Channel Selection And Priority

In addition to the selected LAN controller interface, users may need to configure each single LAN controller channel (port) as dedicated NC-SI interface to the BMC. Additional OEM commands for the configuration of the NC-SI LAN controller channel selection and priority are provided to allow a flexible configuration.

LAN channel selection priority setting list:

0 = The first channel that links up, gets the NC-SI connection to the BMC.

1 = Channel 1 is the preferred port if it is up, otherwise use channel 2 if it is up.

2 = Channel 2 is the preferred port if it is up, otherwise use channel 1 if it is up.

3 = Channel 1 is the only allowed port, always use it, never change to channel 2.

4 = Channel 2 is the only allowed port, always use it, never change to channel 1.

The NC-SI LAN controller channel setting will be stored permanently (non-volatile EEPROM). The default value is 0.

Read LAN channel selection priority:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x01
```

Response:

```
39 28 00 <setting>
```

Change LAN channel selection priority:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x01 <setting>
```

Response:

```
39 28 00
```

3.5.5 FPGA COM Port UART MUX

MIC-6311 implements several serial interfaces, which can be configured in multiple ways. This is done by implementing an UART MUX (refer to Chapter– UART and UART Multiplexer-). The BMC provides OEM commands to configure these UARTs via IPMI. Following COM1 / COM2 port settings are available:

Caution! (Caution: Verify note below about the UART dependency!):

COM interfaces:

Table 3.8: OEM Interfaces

Port	Interface
0x00	COM1
0x01	COM2

COM1 MUX:

Table 3.9: COM1 UART MUX Settings

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL)
0x02	Front panel Micro-USB (default)
0x03	AMC connector port 15

COM2 MUX:

Table 3.10: COM2 UART MUX Settings

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL) (default)
0x02	Front panel Micro-USB
0x03	AMC connector port 15

Note! *The COM1 UART is the main interface with higher priority!*

Read COM port UART MUX setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x08 <port>
```

Response:

```
39 28 00 <setting>
```

Change COM port UART MUX setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x08 <port> <setting>
```

Response:

```
39 28 00
```

3.5.6 Read Port 80 (BIOS POST Code) OEM Command

To be able to read out the actual BIOS boot state via IPMI, the BMC provides an Advantech OEM command to reflect the actual BIOS POST (Port 80) code.

```
ipmitool raw 0x2e 0x80 0x39 0x28 0x00
```

Response:

```
39 28 00 <POST Code>
```

3.5.7 Clear NVRAM Data OEM Command

The BMC implements an OEM command to be able to clear the BIOS settings in NVRAM from SW side without the need of extracting the board and performing any jumper plug and re-plug. This command can be used to load the default BIOS settings.

```
ipmitool raw 0x2e 0x81 0x39 0x28 0x00
```

Response

```
39 28 00
```

3.5.8 MAC Address Mirroring OEM Command

The LAN Controller MAC addresses will also be stored in the FRU EEPROM, making the MAC's available even if the payload is not powered. This helps to relate the MAC address and the physical/logical module location.

The MIC-6311 board is equipped with 5 MAC addresses in total.

Table 3.11: MAC Address Mapping Table

MAC Number	LAN Interface
0	AMC port 0 (BI 0) - 82580 MAC 0
1	AMC port 1 (BI 1) - 82580 MAC 1
2	FP LAN 1 (IO 0) - 82579 MAC 2

Table 3.11: MAC Address Mapping Table	
3	FP LAN 2 (IO 1) - 82580 MAC 3
4	BMC MAC

Read MAC Address OEM command:

```
ipmitool raw 0x2e 0xe2 0x39 0x28 0x00 <MAC Number>
```

Response:

```
39 28 00 <MAC-Address>
```

3.5.9 Load Default Configuration OEM Command

Several configurations settings are provided by the BMC. To reset all of them to their default values, a single OEM command is available to perform this with only one IPMI command.

```
ipmitool raw 0x2e 0xF2 0x39 0x28 0x00
```

Response:

```
39 28 00
```

3.6 UART and UART-Multiplexer

3.6.1 UART Block Diagram

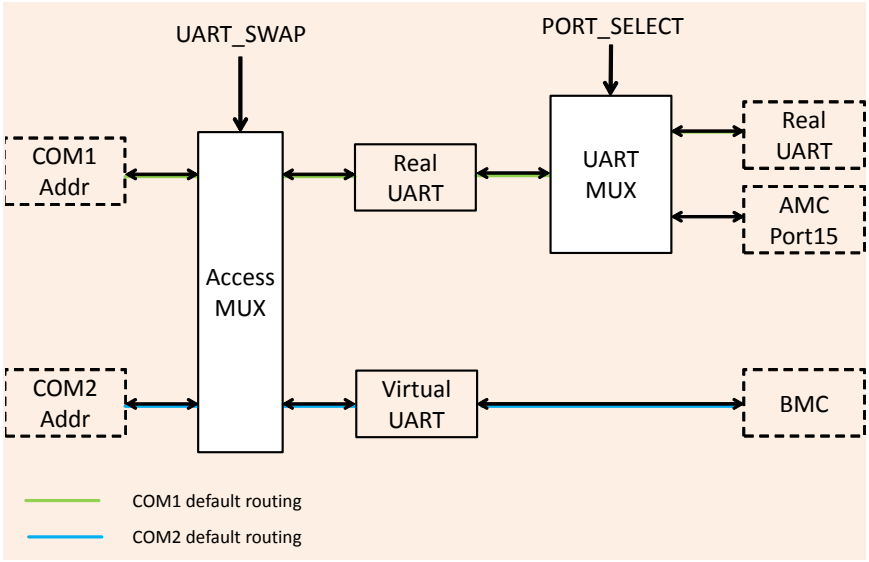


Figure 3.2 UART functional block overview

3.7 ACPI

3.7.1 ACPI Featured Graceful Shutdown

Note! *The payload OS used with MIC-6311 needs to support ACPI to benefit from the module's graceful shutdown feature!*

If there's an shutdown request (e.g. hot swap front panel handle "open" event or IPMI command), the BMC will initiate the OS shutdown with help from the ACPI Power Button signal routed to the x86 system. The ACPI daemon running on the payload OS starts to shutdown the system once it detects the ACPI event. When OS shutdown is finished, the payload will indicate the achieved sleep state to the BMC.

3.7.2 Graceful Shutdown Timeout

A Graceful Shutdown timeout is implemented for payload operating systems without ACPI support or in case the shutdown process is not finished (no active x86 sleep state).

If the BMC does not get the activated sleep state signal within the timeout value of 60 seconds, it will power off the payload anyway.

3.8 BIOS Failover/Redundancy

3.8.1 Overview

The MIC-6311 supports BIOS redundancy handled by the BMC. Two BIOS SPI flashes are populated on the board. This BIOS redundancy mechanism is responsible to manage the flash failover, in case the actual selected BIOS fail to boot.

For example this could happen if a BIOS update over HPM.1 was done and the new BIOS version does not boot, then the BMC will switch back to the previous used BIOS version.

3.8.2 BIOS Boot Watchdog

An IPMI compliant BMC Watchdog, implemented in the BMC, is used to monitor the BIOS boot progress. The BMC will initiate the BIOS SPI flash swap in case of a BMC Watchdog is triggered during BIOS execution (e.g. selected BIOS corrupt).

3.9 Supported Watchdogs

3.9.1 Firmware Watchdog

The FW Watchdog monitors the BMC functionality. If the BMC hangs and stops execution, the watchdog will not be restarted. The watchdog "bites" after a timeout and resets the BMC to recover the controller from current error state.

If the Watchdog is triggered, the IPMB is isolated from the controller. The Payload is not affected and the FRUs operational state stays untouched.

3.9.2 BMC Watchdog

The BMC Watchdog is full IPMI v2.0 Specification compliant. It supports the following IPMI commands:

- Reset Watchdog Timer (IPMI 2.0 Specification 27.5)
- Set Watchdog Timer (IPMI 2.0 Specification 27.6)
- Get Watchdog Timer (IPMI 2.0 Specification 27.7)

To ensure a high reliability of the MIC-6311 Payload, the BMC Watchdog is enabled by default for BIOS monitoring. The details are described in BIOS failover chapter.

3.10 Resets

Several different reset types are supported by the board. This chapter provides an overviewabout the naming used and the differences between the available resets.

3.10.1 Baseboard Management Controller Resets

The MIC-6311 BMC support two different resets types: cold and warm resets following the IPMI specification.

3.10.1.1 BMC Cold Reset

The cold BMC reset causes default setting of all internal and external data/states (e.g. message buffers, interrupt settings, sensor and event configurations, and FRU LED states) and power up defaults to be restored.

Following events lead to BMC cold resets:

- When the BMC is powered on, a cold BMC reset is performed.
- In case management power drops below some critical value, the BMC is cold reset. When the management power returns to its normal value, the BMC is brought out of reset.
- Another example for the cold reset scenario is if the internal watchdog timer of the BMC expires and resets the BMC.
- Users can force a BMC cold reset by pressing the front panel reset button for more than five seconds.
- Finally, a cold reset can also be executed by software with help of the standard IPMI “Cold Reset” command.

3.10.1.2 BMC Warm Reset

The warm BMC reset is similar to cold reset, but with additional preserved data/states (e.g. addresses, and enables). On a warm reset, which can be executed by a standard IPMI command, the BMC firmware recovers its state from local memory.

3.10.1.3 Payload Reset

In addition to the management controller reset types, the board also supports payload resets. The x86 system represents the payload of the MIC-6311 board.

3.10.1.4 Payload Cold Reset

A payload cold reset means hardware reset to the modules' payload, similar to a power on reset. The following events cause payload cold resets:

- Payload power activation after hot swap state change.
- The front panel reset button is pressed for a short period (less than five seconds).
- The PICMG "FRU Control (Cold Reset)" IPMI command is send to the BMC.
- The IPMI Chassis Power command is sent to the BMC
- IPMI BMC Watchdog events.
- Control-Alt-Delete", (on a connected keyboard).
- Standard operating system reset commands (e.g. Linux "reboot").

3.11 SOL Setup

Serial over LAN (SOL) is an extension to IPMI over LAN (IOL) and allows to transmit serial data via LAN. It's defined in the IPMI v2.0 specification and based on the RMCP+ protocol to encapsulate serial data in network packets and exchange them via LAN.

With the help of SOL, user can connect to a virtual serial console (e.g. payload x86 system) from remote. SOL can be used on MIC-6311 for serial-based OS and pre-OS communication over LAN (e.g. OS command-line interface and serial redirected BIOS menu).

3.11.1 Preconditions for SOL

3.11.1.1 Supported LAN Interfaces

All of MIC-6311's Ethernet interfaces can be used for Serial over LAN:

- Both backplane interfaces: Port 0 and 1
- The front panel LAN RJ-45 connectors

Note! *The LAN controller used for SOL is connected to the payload power domain. To be able to use Serial over LAN, the payload needs to be powered!*

3.11.1.2 LAN Controller and UART MUX Configuration

The LAN and UART configuration is flexible and allows different configurations. To avoid "wrong" setups, users should always verify the actual LAN and UART configuration settings before working with SOL:

1. Select the LAN interface to be used (front panel or backplane interface)
2. Make sure the LAN channel priority is appropriate
3. Select UART interface to be used (COM1 or COM2)

3.11.1.3 Default parameter

Following default parameters are good to know for the initial MIC-6311 LAN setup:

IP-Address: 192.168.1.1

LAN Channel Number: 5

Username: "administrator"

Password: "advantech"

3.11.2 LAN Configuration with IPMItool

The open source IPMItool utility is used in this chapter for the MIC-6311 SOL and LAN parameter configuration. Any other utility, based on standard IPMI commands, can be used as well.

To get an overview of all possible commands within an IPMItool command group, please use the single keywords (e.g. “lan”, “user” or “sol”) only.

3.11.2.1 LAN Commands

- lan print [channel number]

Get the LAN configuration parameters for a given channel.

```
[root@localhost ~]# ipmitool lan print
Set in Progress         : Set Complete
Auth Type Support       : NONE MD5 PASSWORD
Auth Type Enable        : Callback : NONE MD5 PASSWORD
                        : User     : NONE MD5 PASSWORD
                        : Operator : NONE MD5 PASSWORD
                        : Admin    : NONE MD5 PASSWORD
                        : OEM      :
IP Address Source       : Static Address
IP Address              : 192.168.1.1
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0b:ab:3e:45:87
Default Gateway IP      : 0.0.0.0
RMCP+ Cipher Suites     : 0,1,2,3,6,7,8,11,12
Cipher Suite Priv Max   : aaaaaaaaaXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
                        :     O=OEM
```

- lan set <channel> <command> [option]

This command can be used to change several BMC LAN parameters (e.g. IP address, netmask, gateway IP address). Below example demonstrates how to change the BMC IP address.

```
[root@localhost ~]# ipmitool lan set 5 ipaddr 172.21.35.104
Setting LAN IP Address to 172.21.35.104
```

3.11.2.2 User Commands

- user list

Get the list of all supported users.

```
[root@localhost ~]# ipmitool user list
ID  Name     Callin  Link Auth  IPMI Msg  ChannelPriv Limit
1            true    true       true       NO ACCESS
2   callback true    true       true       NO ACCESS
3   user     true    true       true       NO ACCESS
4   operator  true    true       true       NO ACCESS
```

- user set name <user id> [username]

This command can be used to change the user name.

```
[root@localhost ~]# ipmitool user set name 2 newuser
```

- user set password <user id> [password]

This command can be is used change the user password.

```
[root@localhost ~]# ipmitool user set password 2 newpass-
word
```

3.11.2.3 SOL session with IPMItool

Advantech recommends using IPMItool to successful open a SOL session with MIC-6311. The “lanplus” interface (RMCP+) of IPMItool must be used to be able to change SOL parameters and establish SOL sessions.

Following general IPMItool parameters are needed for RMCP+ and IPMItool “sol” commands:

```
ipmitool -I lanplus -H <IP-Address> -U <User> -P <Password>
sol <SOL-Command>
```

Command Line Syntax:

I lanplus	Specifies RMCP+ as desired protocol
H <IP-Address>	IP address assigned to the BMC
U <User>	User account, default “administrator”
P <Password>	Password used with specified user account (default password for user “administrator” is “advantech”)

3.11.2.4 SOL Parameter Commands

- sol info [channel number]

Read out the SOL configuration parameters for a given channel.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password>
sol info
Set in progress                 : set-complete
Enabled                         : false
Force Encryption                : true
Force Authentication            : true
Privilege Level                 : ADMINISTRATOR
Character Accumulate Level (ms) : 250
Character Send Threshold        : 32
Retry Count                     : 2
Retry Interval (ms)             : 1000
Volatile Bit Rate (kbps)        : 115.2
```

```
Non-Volatile Bit Rate (kbps)     : 115.2
Payload Channel                  : 7 (0x07)
Payload Port                     : 623
```

- sol set <parameter> <value> [channel]

This command allows modifying special SOL configuration parameters.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password>
sol set

SOL set parameters and values:

  set-in-progress             set-complete | set-in-prog
                              ress | commit-write
  enabled                     true | false
  force-encryption            true | false
  force-authentication        true | false
  privilege-level             user | operator | admin | oem
  character-accumulate-level  <in 5 ms increments>
  character-send-threshold    N
  retry-count                 N
  retry-interval              <in 10 ms increments>
  non-volatile-bit-rate       serial | 9.6 | 19.2 | 38.4 |
                              57.6 | 115.2
  volatile-bit-rate           serial | 9.6 | 19.2 | 38.4 |
                              57.6 | 115.2
```

3.11.2.5 SOL Session Activation

Finally, the IPMItool “sol activate” command need to be issued to establish the SOL session to MIC-6311 from remote.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password>
sol activate
[SOL Session operational.  Use ~? for help]
…
~. [terminated ipmitool]
```

To terminate an active IPMItool SOL session, please use the key sequence“~” + “.” (tilde and dot).

Chapter 4

HPM.1 Update

This chapter describes the update of following software / firmware components.

Sections include:

- BMC Firmware
- FPGA Configuration
- BIOS Image
- NVRAM Image (BIOS Settings)

4.1 HPM.1 Preconditions

4.1.1 IPMItool

Before upgrading, users need to prepare a HPM.1 capable update utility. Advantech recommends to use the open and verified "IPMItool" (>= version 1.8.10).

In general, any tool compliant to the PICMG HPM.1 R1.0 specification can be used.

4.1.2 Interfaces

HPM.1 provides a way to upgrade firmware via different interfaces.

The MIC-6311 supports following IPMI interfaces:

- KCS (local payload interface, active payload and OS support needed)
- IPMB (remote, bridged via Carrier-/Shelf Manager, independent of payload)
- LAN interface (remote, active payload required)

The upgrade procedures in the following chapters are described with the help of KCS, since this is the easiest method. Using LAN or IPMB is similar, only the IPMI-tool interface parameters, which need to be used, are different.

4.2 BMC Firmware Upgrade

4.2.1 Load New BMC Firmware Image

Type IPMItool HPM.1 upgrade command and select the new BMC firmware image.

```
[root@localhost ~]# ipmitool hpm upgrade mic6311_standard_hpm_fw_00_24.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/n y
OK

Performing upgrade stage:

--------------------------------------------------------------------------------
|ID | Name      |    Versions           |    Upload Progress  | Upload| Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time  | Size  |
|---|-----------|-------|-------|-------||----+----+----+----||-------|-------|
| 1 |6311 BMC   |  0.22 |  0.20 |  0.24 ||...................|| 02.16 | 39d60 |
--------------------------------------------------------------------------------

Firmware upgrade procedure successful
```

Firmware upgrade procedure successful

4.2.2 Activate BMC Firmware

Although the new BMC FW is successfully downloaded to the board (called "deferred" version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:

Waiting firmware activation...OK
```

The front panel FRU LED's 1 and 2 (green BMC and green payload LED) are flashing during the FW update activation! This procedure needs around 60 seconds to finalize the update.

4.3 FPGA Configuration Upgrade

4.3.1 Load New FPGA Image

Type IPMItool HPM.1 upgrade command and select the new FPGA image.

```
[root@localhost ~]# ipmitool hpm upgrade mic6311_standard_hpm_fpga_02_12.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/n y
OK

Performing upgrade stage:

--------------------------------------------------------------------------------
|ID | Name      |    Versions           |    Upload Progress  | Upload| Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time  | Size  |
|---|-----------|-------|-------|-------||----+----+----+----||-------|-------|
|*2 |6311 FPGAA |  2.10 |  2.08 |  2.12 ||.................|| 02.21 | 3bf70 |
--------------------------------------------------------------------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.3.2 Activate FPGA Configuration

Although the new FPGA configuration is successfully stored on the board ("deferred" version), it needs to be activated before it's loaded into the FPGA chip. Following two actions are needed to finish the upgrade.

4.3.2.1 HPM.1 Activate Command

Schedule the FPGA load with the HPM.1 "Activate" command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:
```

4.3.2.2 Payload Cold Reset

In order to activate the new FPGA image a payload cold reset is required.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways:

- If the user is working on the local OS (KCS), a linux "reboot","poweroff" or "halt".
- If the user accesses the BMC through the other interfaces (LAN/IPMB), a deactivation and activation cycle is needed, in order to update the FPGA.

The front panel FRU LED's 1 and 2 (green BMC and green payload LED) are flashing during the FW update activation! This procedure needs around 200 seconds to finalize the update.

4.4 BIOS Upgrade

4.4.1 Load New BIOS Image

Type IPMItool HPM.1 upgrade command and select the new BIOS image.

```
[root@localhost ~]# ipmitool hpm upgrade mic6311_standard_hpm_bios_00_10.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/n y
OK

Performing upgrade stage:

--------------------------------------------------------------------------------
|ID | Name       |    Versions           |    Upload Progress   | Upload| Image |
|   |            | Active| Backup| File  |0%       50%     100%| Time  | Size  |
|---|------------|-------|-------|-------||----+----+----+----||-------|-------|
|*3 |6311 BIOS   |  0.08 |  0.09 |  0.10 ||....................|| 25.21 | 7c000c|
--------------------------------------------------------------------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.4.2 Activate BIOS Image

Although the new BIOS image is successfully loaded ("deferred" version), it needs to be activated before users can boot the new BIOS. The following two actions are needed to finish the upgrade.

4.4.2.1 HPM.1 Activate Command

Schedule the BIOS load with the HPM.1 "Activate" command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:
```

4.4.2.2 Payload Cold Reset

A payload cold reset is required to activate the new BIOS image.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways:

- If the user is working on the local OS (KCS), a linux "reboot","poweroff" or "halt".
- If the user accesses the BMC through the other interfaces (LAN/IPMB), a deactivation and activation cycle is needed to load the new BIOS image.

4.5 Verify Successful Upgrades

```
To verify successful updates, the IPMItool hpm check command can be used.
[root@localhost ~]# ipmitool hpm check

PICMG HPM.1 Upgrade Agent 1.0.2:

-------Target Information-------
Device Id           : 0x21
Device Revision     : 0x81
Product Id          : 0x6311
Manufacturer Id     : 0x2839 (Unknown (0x2839))
```

```
---------------------------------
|ID | Name       |    Versions   |
|   |            | Active| Backup|
---------------------------------
| 0 |6311 BLL    |  0.22 | --.-- |
| 1 |6311 BMC    |  0.24 |  0.22 |
|*2 |6311 FPGAA  |  2.12 |  2.10 |
|*3 |6311 BIOSS  |  0.10 |  0.08 |
|*4 |6311 NVRAMM|  0.03 | --.-- |
---------------------------------
(*) Component requires Payload Cold Reset
```

After a successful upgrade, the new backup version should be the former active version (if "Backup" versions are supported). And the new "Active" version should be the version of the used upload file.

Appendix A

Pin Assignments

A.1 P0 Connector

Table A.1: P0 VPX I/O							
	G	**F**	**E**	**D**	**C**	**B**	**A**
1	+12 V	+12 V	+12 V	No Pad	+12 V	+12 V	+12 V
2	+12 V	+12 V	+12 V	No Pad	+12 V	+12 V	+12 V
3	+5 V	+5 V	+5 V	No Pad	+5 V	+5 V	+5 V
4	IPMB0-B_CLK	IPMB0-B_DAT	GND	-12V_AUX	GND	SYSRE-SET	NVMRO
5	GAP	GA4	GND	3.3V_AUX	GND	IPMB0-A_CLK	IPMB0-A_DAT
6	GA3	GA2	GND	NC	GND	GA1	GA0
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND

Note! *NC: No Connect*

#: Active Low

A.2 P1 Connector

Table A.2: P1 VPX I/O							
	G	**F**	**E**	**D**	**C**	**B**	**A**
1		GND	FP1_TX0-	FP1_TX0+	GND	FP1_RX0-	FP1_RX0+
2	GND	FP1_TX1-	FP1_TX1+	GND	FP1_RX1-	FP1_RX1+	GND
3		GND	FP1_TX2-	FP1_TX2+	GND	FP1_RX2-	FP1_RX2+
4	GND	FP1_TX3-	FP1_TX3+	GND	FP1_RX3-	FP1_RX3+	GND
5	SYS_CON#	GND	FP2_TX0-	FP2_TX0+	GND	FP2_RX0-	FP2_RX0+
6	GND	FP2_TX1-	FP2_TX1+	GND	FP2_RX1-	FP2_RX1+	GND
7		GND	FP2_TX2-	FP2_TX2+	GND	FP2_RX2-	FP2_RX2+
8	GND	FP2_TX3-	FP2_TX3+	GND	FP2_RX3-	FP2_RX3+	GND
9		GND			GND		
10	GND			GND			GND
11		GND			GND		
12	GND			GND			GND
13		GND			GND		
14	GND			GND			GND
15		GND			GND		
16	GND			GND			GND

Note! *NC: No Connect*

#: Active Low

A.3 P2 Connector

Table A.3: P2: I/O

Plug-in Module P2				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2				Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	X16 using[15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-T-	EP00-T+	GND	GND-J2	EP00-R-	EP00-R+
2				GND	EP01-T-	EP01-T+	GND-J2	GND	EP01-R-	EP01-R+	GND-J2	GND
3				UD	GND	GND-J2	EP02-T-	EP02-T+	GND	GND-J2	EP02-R-	EP02-R+
4				GND	EP03-T-	EP03-T+	GND-J2	GND	EP03-R-	EP03-R+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using [15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP011-T-	EP011-T+	GND-J2	GND	EP011-R-	EP011-R+	GND-J2	GND
13			x4 using [15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP013-T-	EP013-T+	GND-J2	GND	EP013-R-	EP013-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP015-T-	EP015-T+	GND-J2	GND	EP015-R-	EP015-R+	GND-J2	GND

PCIe port only supports an X4 link

Note! *NC: No Connect*

#: Active Low

A.4 P3 Connector

Table A.4: P3 VPX I/O Port								
Wafer offset	**Row G**	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**	
n+1		GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4	P64s
n+2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND	
n+3		GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12	
n+4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND	
n+5		GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20	
n+6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND	
n+7		GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28	
n+8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND	
n+9		GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36	
n+10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND	
n+11		GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44	
n+12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND	
n+13		GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52	
n+14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND	
n+15		GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60	
n+16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND	

Note! *NC: No Connect*

#: Active Low

A.5 P4 Connector

Table A.5: P4 CompactPCI I/O Port							
	G	**F**	**E**	**D**	**C**	**B**	**A**
1	RIO_SATA_LED	GND	Jn6-A5	Jn6-B5	GND	Jn6-D5	Jn6-E5
2	GND	Jn6-A7	Jn6-B7	GND	Jn6-D7	Jn6-E7	GND
3	RIO_PRESENT#	GND	Jn6-A9	Jn6-B9	GND	Jn6-D9	Jn6-E9
4	GND	Jn6-A15	Jn6-B15	GND	Jn6-D15	Jn6-E15	GND
5		GND	Jn6-A17	Jn6-B17	GND	Jn6-D17	Jn6-E17
6	GND	Jn6-A19	Jn6-B19	GND	Jn6-D19	Jn6-E19	GND
7		GND	USB-	USB+	GND	USB-	USB+
8	GND	KB_CLK	KB_DAT	GND	MSC_DATA	MSC_CLK	GND
9		GND			GND		
10	GND			GND			GND
11		GND	SERDES2_TX-	SERDES2_TX+	GND	SERDES2_RX-	SERDES2_RX+
12	GND	SERDES1_TX-	SERDES1_TX+	GND	SERDES1_RX-	SERDES1_RX+	GND
13		GND	GBE2_DB-	GBE2_DB+	GND	GBE2_DA-	GBE2_DA+
14	GND	GBE2_DD-	GBE2_DD+	GND	GBE2_DC-	GBE2_DC+	GND
15		GND	GBE1_DB-	GBE1_DB+	GND	GBE1_DA-	GBE1_DA+
16	GND	GBE1_DD-	GBE1_DD+	GND	GBE1_DC-	GBE1_DC+	GND

Note! *NC: No Connect*

#: Active Low

A.6 P5 Connector

Table A.6: J5 CompactPCI I/O Port

	G	F	E	D	C	B	A
1	DP2_HPD	GND	DP2_1-	DP2_1+	GND	DP2_0-	DP2_0+
2	GND	DP2_3-	DP2_3+	GND	DP2_2-	DP2_2+	GND
3	DP1_HPD	GND	DP1_1-	DP1_1+	GND	DP1_0-	DP1_0+
4	GND	DP1_3-	DP1_3+	GND	DP1_2-	DP1_2+	GND
5	HDA_RST#	GND	DP2_AUX-	DP2_AUX+	GND	DP1_AUX-	DP1_AUX+
6	GND	USB3_5_TX+	USB3_5_Tx-	GND	USB3_5_RX-	USB3_5_RX+	GND
7	HDA_SYNC	GND	USB3_6_TX-	USB3_6_TX+	GND	USB3_6_RX-	USB3_6_RX+
8	GND	SATA4_TX-	SATA4_Tx+	GND	SATA4_RX-	SATA4_RX+	GND
9	HDA_BCLK	GND	SATA5_Tx-	SATA5_Tx+	GND	SATA5_RX-	SATA5_RX+
10	GND	DPC_CTRL_DATA	DPC_CTRL_CLK	GND	DPB_CTRL_DATA	DPB_CTRL_CLK	GND
11	HDA_SDO	GND	SATA1_TX-	SATA1_TX+	GND	SATA1_RX-	SATA1_RX+
12	GND	USB4-	USB4+	GND	USB3-	USB3+	GND
13	HDA_SDI	GND	COM1_DCD	COM1_RI	GND	COM1_RX	COM1_TX
14	GND	COM1_RTS	COM1_CTS	GND	COM1_DTR#	COM1_DSR	GND
15	NC	GND	COM2_DCD	COM2_RI	GND	COM2_RX	COM2_TX
16	GND	COM2_RTS	COM2_CTS	GND	COM2_DTR#	COM2_DSR#	GND

Note! *NC: No Connect*

#: Active Low

A.7 Other Connectors

Table A.7: CNSATA1 Daughter Board Connector			
1	GND	2	GND
3	SATA0_TX+	4	SATA1_TX+
5	SATA0_TX-	6	SATA1_TX-
7	GND	8	GND
9	SATA0_RX+	10	SATA1_RX+
11	SATA0_RX-	12	SATA1_RX-
13	GND	14	GND
15	GND	16	GND
17	VCC5	18	VCC3
19	VCC5	20	VCC3

Table A.8: J15(P15) XMC1 Connector						
Pin	**A**	**B**	**C**	**D**	**E**	**F**
1	PETX_P0	PETX_N0	+3.3 V	PETX_P1	PETX_N1	VPWR(+5 V)
2	GND	GND	NC(JRST#)	GND	GND	PRST#
3	PETX_P2	PETX_N2	+3.3 V	PETX_P3	PETX_N3	VPWR(+5 V)
4	GND	GND	NC(JTCK)	GND	GND	NC(MRSTO#)
5	PETX_P4	PETX_N4	+3.3 V	PETX_P5	PETX_N5	VPWR(+5 V)
6	GND	GND	NC(JTMS)	GND	GND	+12 V
7	PETX_P6	PETX_N6	+3.3 V	PETX_P7	PETX_N7	VPWR(+5 V)
8	GND	GND	NC(JTDI)	GND	GND	-12 V
9	NC	NC	NC	NC	NC	VPWR(+5 V)
10	GND	GND	NC(JTDO)	GND	GND	GA0
11	PERX_P0	PERX_N0	NC(MBIST#)	PERX_P1	PERX_N1	VPWR(+5 V)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERX_P2	PERX_N2	NC(+3.3V_AUX)	PERX_P3	PERX_N3	VPWR(+5 V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PERX_P4	PERX_N4	NC	PERX_P5	PERX_N5	VPWR(+5 V)
16	GND	GND	NC(MVMRO)	GND	GND	TBD_SCLK
17	PERX_P6	PERX_N6	NC	PERX_P7	PERX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100Mhz	CLK_100Mhz#	FPGAIO2	NC(WAKE#)	NC(ROOT#)	NC

Table A.9: VCN1 VGA Connector			
1	RED	9	+5 V
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

Table A.10: CNCOM1 (RJ45) Connector			
1	DCD#	6	DSR#
2	SIN	7	RTS#
3	SOUT	8	CTS#
4	DTR#		
5	GND		

Table A.11: CN & CN5 USB Port 1 & Port 2			
1	+5 V (fused)	1	+5 V (fused)
2	USBD0-	2	USBD1-
3	USBD0+	3	USBD1+
4	GND	4	GND

Table A.12: BT1 CMOS Battery			
1	BAT_VCC	2	GND

Table A.13: RJ1 LAN1 Connector			
1	LAN_0+	5	LAN_2-
2	LAN_0-	6	LAN_1-
3	LAN_1+	7	LAN_3+
4	LAN_2+	8	LAN_3-

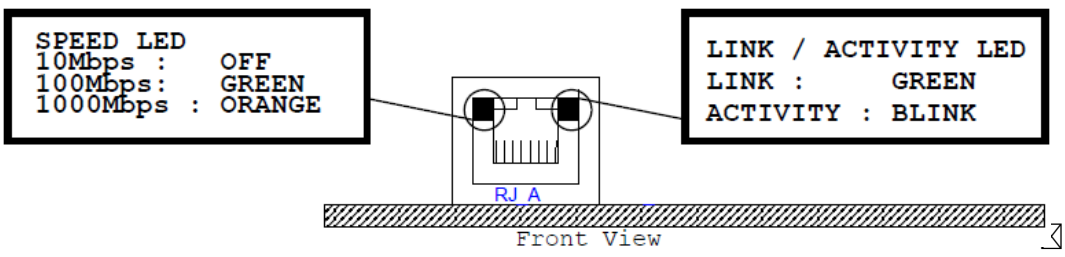
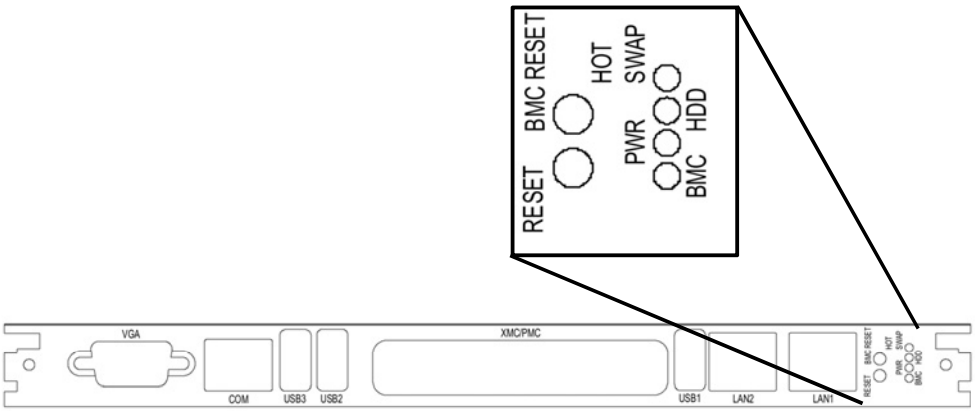


Figure A.1 RJ11 LAN indicator

A.7.1 M/D, PWR, BMC HB, and IDE/Hot-swap LEDs



Name	Description
PWR (Green)	Indicates power status
BMC (Yellow)	Indicates BMC status (heart beat indicates BMC is active)
HDD/Hot Swap (Yellow/Blue)	Yellow indicates IDE activity, blue indicates the board is ready to be hot swapped

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

B.1 Watchdog Timer Programming Procedure

To program the watchdog timer, you must execute a program that writes a value to the I/O port address 443/444 (hex) for Enable/Disable. This output value represents a time interval. The value range is 01 (hex) to FF (hex), and the related time interval is 1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
. .	
3F	63 sec

After data entry, the program must refresh the watchdog timer by rewriting the I/O port 443/443 (hex) while simultaneously setting the address. To disable the watchdog timer, use the program to read I/O port 444 (hex). The following is an example of how the watchdog timer can be programmed in BASIC:

```
10 REM Watchdog timer example program
20 OUT & H443, data REM Start and restart the watchdog
30 GOSUB 1000 REM Your application task #1,
40 OUT & H443, data REM Reset the timer
50 GOSUB 2000 REM Your application task #2,
60 OUT & H443, data REM Reset the timer
70 X=INP (& H444) REM, Disable the watchdog timer
80 END
1000 REM Subroutine #1, your application task
.
1070 RETURN
2000 REM Subroutine #2, your application task
.
2090 RETURN
```

Appendix C

FPGA

This appendix describes the FPGA configuration.

C.1 Features

- Hot swap: Hot insertion and removal control
- VPX backplane: VPX slot addressing
- LPC bus: Provides LPC bus access
- Watchdog
- Debug message: Boot time POST message

C.2 FPGA I/O Registers

Advantech's MIC-6311 FPGA communicates with the main I/O spaces. The LPC unit is used to interconnect the Intel ICH9R LPC signals. The Debug Port Unit is used to decode POST codes. The Hot-Swap Out-Of-Service LED Control Unit is used to control the blue LED during Hot-Insert and Hot-Remove operations. The Drone Mode Unit is used to disable the VPX. The other signals in the Miscellaneous Unit are for interfacing with corresponding I/O interface signals.

Table C.1: LPC I/O Address Register

LPC Address	I/O Type	Description
0x 80h	W	Port 80 display
0x 443h / 0x 444h	RW	Watchdog register
0x 445h	R	FPGA revision
0x 447h	R	Geographic Address (GA)

Appendix D

IO Controller List

D.1 IO Controller List

I/O Port	Controller
Display Port to back-plane	Intel Haswell
VGA	Intel Lynx Point
Onboard flash	Intel Lynx Point
SATA	Intel Lynx Point
SATA to backplane	Intel Lynx Point
CFast	Intel Lynx Point
USB 2.0/3.0 to front panel	Intel Lynx Point
USB 2.0/3.0 to back-plane	Intel Lynx Point
Audio to backplane	Intel Lynx Point
Front panel RJ45	Intel I350AM4
SERDES to backplane	Intel I350AM4
GBE to backplane	Intel I350AM4
UART to front panel	Lattice LCMXO2
UART to backplane	Lattice LCMXO2

Appendix E

Glossary

E.1 Glossary

ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
CF	CompactFlash
CPU	Central Processing Unit
CPCI	CompactPCI
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
FCBGA	Flip Chip BGA
FRU	Field Replaceable Unit
FPGA	Field Programmable Gate Arrays
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HPM	Hardware Platform Management
HW	Hardware
I/O	Input/Output
IC	Integrated Circuit
IOL	IPMI-Over-LAN
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
LED	Light-Emitting Diode
LPC	Low Pin Count
MAC	Medium Access Control
NCSI	Network Controller Sideband Interface
NVRAM	Non-Volatile Random-Access Memory
OS	Operating System
PCB	Printed Wiring Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical layer Interface
PCH	Platform Controller Hub
PICMG	PCI Industrial Computer Manufacturers Group
PXE	Pre-boot Execution Environment
RMCP	Remote Management Control Protocol
RIO	Rear Input/Output
RS-232	An Interface specified by Electronic Industries Alliance
RTC	Real Time Clock
RTM	Rear Transition Module
SFP	Small Form Factor Pluggable
SDR	Sensor Data Record
SerDes	Serializer/Deserializer
SOL	Serial-Over-LAN

SPI	Serial Peripheral Interface
SPD	Serial Presence Detect
SW	Software
ULV	Ultra Low Voltage
UART	Universal Asynchronous Receiver Transmitter
XTM	Extension Module

Appendix F

BIOS Checkpoint

F.1 Introduction

A status code is a data value used to indicate progress during the boot phase. A subset of these status codes, commonly known as checkpoints, indicate common phases of the BIOS boot process.

Checkpoints are typically output to I/O port 80h; however, the Aptio 4.x core can be configured to send status codes to various sources. The Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task that the system is currently executing. Checkpoints are extremely useful in enabling software developers or technicians to debug and resolve problems that occur during the pre-boot process.

To perform traditional BIOS functions, the Aptio 4.x core adheres to the firmware model specified in the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers to the following "boot phases", which may apply to various status code and checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization
- Driver Execution Environment (DXE) – main hardware initialization
- Boot Device Selection (BDS) – system setup, pre-OS user interface and bootable device selection (CD/DVD, HDD, USB, Network, Shell, etc)

F.2 Checkpoint Ranges / Descriptions

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

F.3 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard)
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core started
0x11	Pre-memory CPU initialization started
0x12	Pre-memory CPU initialization (CPU module-specific)
0x13	Pre-memory CPU initialization (CPU module-specific)
0x14	Pre-memory CPU initialization (CPU module-specific)
0x15	Pre-memory North Bridge initialization started
0x16	Pre-memory North Bridge initialization (North Bridge module-specific)
0x17	Pre-memory North Bridge initialization (North Bridge module-specific)
0x18	Pre-memory North Bridge initialization (North Bridge module-specific)
0x19	Pre-memory South Bridge initialization started
0x1A	Pre-memory South Bridge initialization (South Bridge module-specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module-specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module-specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory

0x2F	Memory initialization (other)
0x30	Reserved for ASL (see the ASL Status Codes section below)
0x31	Memory installed
0x32	CPU post-memory initialization started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-memory North Bridge initialization started
0x38	Post-memory North Bridge initialization (North Bridge module specific)
0x39	Post-memory North Bridge initialization (North Bridge module specific)
0x3A	Post-memory North Bridge initialization (North Bridge module specific)
0x3B	Post-memory South Bridge initialization started
0x3C	Post-memory South Bridge initialization (South Bridge module specific)
0x3D	Post-memory South Bridge initialization (South Bridge module specific)
0x3E	Post-memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post-memory initialization codes
0x4F	DXE IPL started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error
0x55	Memory not installed
0x56	Invalid CPU type or speed
0x57	CPU mismatch
0x58	CPU self-test failed or possible CPU cache error
0x59	CPU micro-code not found or micro-code update failed
0x5A	Internal CPU error
0x5B	Reset PPI unavailable
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume started (S3 resume PPI called by the DXE IPL)
0xE1	S3 Boot script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume failed
0xE9	S3 Resume PPI not found

0xEA	S3 Resume boot script error
0xEB	S3 OS wake error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (auto recovery)
0xF1	Recovery condition triggered by user (forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image found
0xF4	Recovery firmware image loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI unavailable
0xF9	Recovery capsule not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core started
0x61	
0x62	
0x63	
0x64	
0x65	CPU DXE initialization (CPU module-specific)
0x66	CPU DXE initialization (CPU module-specific)
0x67	CPU DXE initialization (CPU module-specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization started
0x6A	North Bridge DXE SMM initialization started
0x6B	North Bridge DXE initialization (North Bridge module-specific)
0x6C	North Bridge DXE initialization (North Bridge module-specific)
0x6D	North Bridge DXE initialization (North Bridge module-specific)
0x6E	North Bridge DXE initialization (North Bridge module-specific)
0x6F	North Bridge DXE initialization (North Bridge module-specific)
0x70	South Bridge DXE initialization started
0x71	South Bridge DXE SMM initialization started
0x72	South Bridge devices initializing
0x73	South Bridge DXE initialization (South Bridge module-specific)
0x74	South Bridge DXE initialization (South Bridge module-specific)
0x75	South Bridge DXE initialization (South Bridge module-specific)
0x76	South Bridge DXE initialization (South Bridge module-specific)
0x77	South Bridge DXE initialization (South Bridge module-specific)
0x78	ACPI module initialization

0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase started
0x91	Driver connecting started
0x92	PCI bus initialization started
0x93	PCI bus hot plug controller initializing
0x94	PCI bus enumeration
0x95	PCI bus request resources
0x96	PCI bus assign resources
0x97	Console output devices connecting
0x98	Console input devices connecting
0x99	Super I/O initialization
0x9A	USB initialization started
0x9B	USB reset
0x9C	USB detect
0x9D	USB enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization started
0xA1	IDE reset
0xA2	IDE detect
0xA3	IDE enable
0xA4	SCSI initialization started
0xA5	SCSI reset
0xA6	SCSI detect
0xA7	SCSI enable
0xA8	Setup verification password
0xA9	Start of setup
0xAA	Reserved for ASL (see the ASL Status Codes section below)
0xAB	Setup input wait
0xAC	Reserved for ASL (see the ASL Status Codes section below)
0xAD	Ready to boot event
0xAE	Legacy boot event
0xAF	Exit boot services event
0xB0	Runtime set virtual address MAP begin
0xB1	Runtime set virtual address MAP end
0xB2	Legacy option ROM initialization
0xB3	System reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes

DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some architectural protocols unavailable
0xD4	PCI resource allocation error. Out of resources
0xD5	No space for legacy option ROM
0xD6	No console output devices found
0xD7	No console input devices found
0xD8	Invalid password
0xD9	Error loading boot option (LoadImage returned error)
0xDA	Boot option failed (StartImage returned error)
0xDB	Flash update failed
0xDC	Reset protocol unavailable

ACPI/ASL Checkpoints

Status Code	Description
0x01	System entering S1 sleep state
0x02	System entering S2 sleep state
0x03	System entering S3 sleep state
0x04	System entering S4 sleep state
0x05	System entering S5 sleep state
0x10	System waking from the S1 sleep state
0x20	System waking from the S2 sleep state
0x30	System waking from the S3 sleep state
0x40	System waking from the S4 sleep state
0xAC	System transitioned into ACPI mode. Interrupt controller in PIC mode
0xAA	System transitioned into ACPI mode. Interrupt controller in APIC mode

OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post-memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Appendix G

IPMI/PICMG Command Subset Supported by BMC

G.1 Standard IPMI Commands (v2.0)

Table G.1: IPM Device “Global” Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get Device ID	20.1	App	01h	Mandatory	Yes
Cold Reset	20.2	App	02h	Optional	Yes
Warm Reset	20.3	App	03h	Optional	Yes
Get Self Test Results	20.4	App	04h	Mandatory	Yes
Manufacturing Test On	20.5	App	05h	Optional	No
Set ACPI Power State	20.6	App	06h	Optional	No
Get ACPI Power State	20.7	App	07h	Optional	No
Get Device GUID	20.8	App	08h	Optional	Yes
Broadcast ‘Get Device ID’	20.9	App	01h	Optional/Man-datory	Yes

Table G.2: BMC Watchdog Timer Commands					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Reset Watchdog Timer	27.5	App	22h	Mandatory	Yes
Set Watchdog Timer	27.6	App	24h	Mandatory	Yes
Get Watchdog Timer	27.7	App	25h	Mandatory	Yes

Table G.3: BMC Device and Messaging Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Set BMC Global Enables	22.1	App	2Eh	Mandatory	Yes
Get BMC Global Enables	22.2	App	2Fh	Mandatory	Yes
Clear Message Flags	22.3	App	30h	Mandatory	Yes
Get Message Flags	22.4	App	31h	Mandatory	Yes
Enable Message Channel Receive	22.5	App	32h	Optional	No
Get Message	22.6	App	33h	Mandatory	Yes
Send Message	22.7	App	34h	Mandatory	Yes
Read Event Message Buffer	22.8	App	35h	Optional	Yes
Get BT Interface Capabilities	22.10	App	36h	Mandatory	No
Get System GUID	22.14	App	37h	Optional	Yes
Get Channel Authentication Capabilities	22.13	App	38h	Optional	Yes
Get Session Challenge	22.15	App	39h	Optional	Yes
Activate Session	22.17	App	3Ah	Optional	Yes
Set Session Privilege Level	22.18	App	3Bh	Optional	Yes
Close Session	22.19	App	3Ch	Optional	Yes

Table G.3: BMC Device and Messaging Commands					
Get Session Info	22.20	App	3Dh	Optional	Yes
Get AuthCode	22.21	App	3Fh	Optional	No
Set Channel Access	22.22	App	40h	Optional	Yes
Get Channel Access	22.23	App	41h	Optional	Yes
Get Channel Info	22.24	App	42h	Optional	Yes
Set User Access	22.26	App	43h	Optional	Yes
Get User Access	22.27	App	44h	Optional	Yes
Set User Name	22.28	App	45h	Optional	Yes
Get User Name	22.29	App	46h	Optional	Yes
Set User Password	22.30	App	47h	Optional	Yes
Activate Payload	24.1	App	48h	-	Yes
Deactivate Payload	24.2	App	49h	-	Yes
Get Payload Activation Status	24.4	App	4Ah	-	No
Get Payload Instance Info	24.5	App	4Bh	-	No
Set User Payload Access	24.6	App	4Ch	-	Yes
Get User Payload Access	24.7	App	4Dh	-	Yes
Get Channel Payload Support	24.8	App	4Eh	-	No
Get Channel Payload Version	24.9	App	4Fh	-	No
Get Channel OEM Payload Info	24.10	App	50h	-	No
Master Write-Read	22.11	App	52h	Mandatory	Yes
Get Channel Cipher Suites	22.15	App	54h	-	Yes
Suspend/Resume Payload Encryption	24.3	App	55h	-	No
Set Channel Security Keys	22.25	App	56h	-	Yes
Get System Interface Capabilities	22.9	App	57h	-	No

Table G.4: Chassis Device Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get Chassis Capabilities	28.1	Chassis	00h	Mandatory	Yes
Get Chassis Status	28.2	Chassis	01h	Optional/Mandatory	No
Chassis Control	28.3	Chassis	02h	Optional/Mandatory	Yes
Chassis Reset	28.4	Chassis	03h	Optional	Yes
Chassis Identify	28.5	Chassis	04h	Optional	No
Set Front Panel Button Enables	28.6	Chassis	0Ah	-	No
Set Chassis Capabilities	28.7	Chassis	05h	Optional	No
Set Power Restore Policy	28.8	Chassis	06h	Optional	Yes
Set Power Cycle Interval	28.9	Chassis	0Bh	-	No
Get System Restart Cause	28.11	Chassis	07h	Optional	No

Table G.4: Chassis Device Commands					
Set System Boot Options	28.12	Chassis	08h	Optional	Yes
Get System Boot Options	28.13	Chassis	09h	Optional	Yes
Get POH Counter	28.14	Chassis	0Fh	Optional	No

Table G.5: Event Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Set Event Receiver	29.1	S/E	00h	Mandatory	Yes
Get Event Receiver	29.2	S/E	01h	Mandatory	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	02h	Mandatory	Yes

Table G.6: PEF and Alerting Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get PEF Capabilities	30.1	S/E	10h	Mandatory	No
Arm PEF Postpone Timer	30.2	S/E	11h	Mandatory	No
Set PEF Configuration Parameters	30.3	S/E	12h	Mandatory	No
Get PEF Configuration Parameters	30.4	S/E	13h	Mandatory	No
Set Last Processed Event ID	30.5	S/E	14h	Mandatory	No
Get Last Processed Event ID	30.6	S/E	15h	Mandatory	No
Alert Immediate	30.7	S/E	16h	Optional	No
PET Acknowledge	30.8	S/E	17h	Optional	No

Table G.7: Sensor Device Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get Device SDR Info	35.2	S/E	20h	Optional	Yes
Get Device SDR	35.3	S/E	21h	Optional	Yes
Reserve Device SDR Repos-itory	35.4	S/E	22h	Optional	Yes
Get Sensor Reading Factors	35.5	S/E	23h	Optional	No
Set Sensor Hysteresis	35.6	S/E	24h	Optional	No
Get Sensor Hysteresis	35.7	S/E	25h	Optional	No
Set Sensor Threshold	35.8	S/E	26h	Optional	Yes
Get Sensor Threshold	35.9	S/E	27h	Optional	Yes
Set Sensor Event Enable	35.10	S/E	28h	Optional	Yes
Get Sensor Event Enable	35.11	S/E	29h	Optional	Yes
Re-arm Sensor Events	35.12	S/E	2Ah	Optional	Yes
Get Sensor Event Status	35.13	S/E	2Bh	Optional	Yes
Get Sensor Reading	35.14	S/E	2Dh	Mandatory	Yes

Table G.7: Sensor Device Commands					
Set Sensor Type	35.15	S/E	2Eh	Optional	No
Get Sensor Type	35.16	S/E	2Fh	Optional	No

Table G.8: FRU Device Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get FRU Inventory Area Info	34.1	Storage	10h	Mandatory	Yes
Read FRU Data	34.2	Storage	11h	Mandatory	Yes
Write FRU Data	34.3	Storage	12h	Mandatory	Yes

Table G.9: SDR Device Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get SDR Repository Info	33.9	Storage	20h	Mandatory	Yes
Get SDR Repository Allocation Info	33.10	Storage	21h	Optional	No
Reserve SDR Repository	33.11	Storage	22h	Mandatory	Yes
Get SDR	33.12	Storage	23h	Mandatory	Yes
Add SDR	33.13	Storage	24h	Mandatory	No
Partial Add SDR	33.14	Storage	25h	Mandatory	No
Delete SDR	33.15	Storage	26h	Optional	No
Clear SDR Repository	33.16	Storage	27h	Mandatory	Yes
Get SDR Repository Time	33.17	Storage	28h	Optional/Mandatory	Yes
Set SDR Repository Time	33.18	Storage	29h	Optional/Mandatory	Yes
Enter SDR Repository Update Mode	33.19	Storage	2Ah	Optional	No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	Mandatory	No
Run Initialization Agent	33.21	Storage	2Ch	Optional	No

Table G.10: SEL Device Commands					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get SEL Info	31.2	Storage	40h	Mandatory	Yes
Get SEL Allocation Info	31.3	Storage	41h	Optional	No
Reserve SEL	31.4	Storage	42h	Optional	Yes
Get SEL Entry	31.5	Storage	43h	Mandatory	Yes
Add SEL Entry	31.6	Storage	44h	Mandatory	Yes
Partial Add SEL Entry	31.7	Storage	45h	Mandatory	No
Delete SEL Entry	31.8	Storage	46h	Optional	No
Clear SEL	31.9	Storage	47h	Mandatory	Yes

Table G.10: SEL Device Commands					
Get SEL Time	31.10	Storage	48h	Mandatory	Yes
Set SEL Time	31.11	Storage	49h	Mandatory	Yes
Get Auxiliary Log Status	31.12	Storage	5Ah	Optional	No
Set Auxiliary Log Status	31.13	Storage	5Bh	Optional	No

Table G.11: LAN Device Commands					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Set LAN Configuration Parameters	23.1	Transport	01h	Optional/Mandatory	Yes
Get LAN Configuration Parameters	23.2	Transport	02h	Optional/Mandatory	Yes
Suspend BMC ARPs	23.3	Transport	03h	Optional/Mandatory	No
Get IP/UDP/RMCP Statistics	23.4	Transport	04h	Optional	No

Table G.12: Serial/Modem Device Commands					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Set Serial/Modem Configuration	25.1	Transport	10h	Optional/Mandatory	No
Get Serial/Modem Configuration	25.2	Transport	11h	Optional/Mandatory	No
Set Serial/Modem Mux	25.3	Transport	12h	Optional	No
Get TAP Response Codes	25.4	Transport	13h	Optional	No
Set PPP UDP Proxy Transmit Data	25.5	Transport	14h	Optional	No
Get PPP UDP Proxy Transmit Data	25.6	Transport	15h	Optional	No
Send PPP UDP Proxy Packet	25.7	Transport	16h	Optional	No
Get PPP UDP Proxy Receive Data	25.8	Transport	17h	Optional	No
Serial/Modem Connection Active	25.9	Transport	18h	Optional/Mandatory	No
Callback	25.10	Transport	19h	Optional	No
Set User Callback Options	25.11	Transport	1Ah	Optional	No
Get User Callback Options	25.12	Transport	1Bh	Optional	No
SOL Activating	26.1	Transport	20h	-	Yes
Set SOL Configuration Parameters	26.2	Transport	21h	-	Yes
Get SOL Configuration Parameters	26.3	Transport	22h	-	Yes

Table G.13: Bridge Management Commands (ICMB)					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Bridge State	[ICMB]	Bridge	00h	Optional/Mandatory	No
Set Bridge State	[ICMB]	Bridge	01h	Optional/Mandatory	No
Get ICMB Address	[ICMB]	Bridge	02h	Optional/Mandatory	No
Set ICMB Address	[ICMB]	Bridge	03h	Optional/Mandatory	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	Optional/Mandatory	No
Get Bridge Statistics	[ICMB]	Bridge	05h	Optional/Mandatory	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	Optional/Mandatory	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	Optional/Mandatory	No
Get Bridge Proxy Address	[ICMB]	Bridge	09h	Optional/Mandatory	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	Optional/Mandatory	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	Optional/Mandatory	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	Optional/Mandatory	No

Table G.14: Discovery Commands (ICMB)					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Prepare For Discovery	[ICMB]	Bridge	10h	Optional/Mandatory	No
Get Addresses	[ICMB]	Bridge	11h	Optional/Mandatory	No
Set Discovered	[ICMB]	Bridge	12h	Optional/Mandatory	No
Get Chassis Device ID	[ICMB]	Bridge	13h	Optional/Mandatory	No
Set Chassis Device ID	[ICMB]	Bridge	14h	Optional/Mandatory	No

Table G.15: Bridging Commands (ICMB)					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Bridge Request	[ICMB]	Bridge	20h	Optional/Mandatory	No
Bridge Message	[ICMB]	Bridge	21h	Optional/Mandatory	No

Table G.16: Event Commands (ICMB)					
Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get Event Count	[ICMB]	Bridge	30h	Optional/Man-datory	No
Set Event Destination	[ICMB]	Bridge	31h	Optional/Man-datory	No
Set Event Reception State	[ICMB]	Bridge	32h	Optional/Man-datory	No
Send ICMB Event Message	[ICMB]	Bridge	33h	Optional/Man-datory	No
Get Event Destination	[ICMB]	Bridge	34h	Optional/Man-datory	No
Get Event Reception State	[ICMB]	Bridge	35h	Optional/Man-datory	No

Table G.17: OEM Commands for Bridge NetFn					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
OEM Commands	[ICMB]	Bridge	C0h-FEh	Optional/Man-datory	No

Table G.18: Other Bridge Commands					
Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Error Report	[ICMB]	Bridge	FFh	Optional/Man-datory	No

G.2 PICMG IPMI Commands

Table G.19: AdvancedTCA (PICMG 3.0 R3.0 AdvancedTCA Base Specification)

Command	PICMG 3.0 Table	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get PICMG Properties	3-11	PICMG	00h	-	Yes
Get Address Info	3-10	PICMG	01h	-	No
Get Shelf Address Info	3-16	PICMG	02h	-	No
Set Shelf Address Info	3-17	PICMG	03h	-	No
FRU Control	3-27	PICMG	04h	-	Yes
Get FRU LED Properties	3-29	PICMG	05h	-	Yes
Get LED Color Capabilities	3-30	PICMG	06h	-	Yes
Set FRU LED State	3-31	PICMG	07h	-	Yes
Get FRU LED State	3-32	PICMG	08h	-	Yes
Set IPMB State	3-70	PICMG	09h	-	No
Set FRU Activation Policy	3-20	PICMG	0Ah	-	No
Get FRU Activation Policy	3-21	PICMG	0Bh	-	No
Set FRU Activation	3-19	PICMG	0Ch	-	No
Get Device Locator Record ID	3-39	PICMG	0Dh	-	Yes
Set Port State	3-59	PICMG	0Eh	-	No
Get Port State	3-60	PICMG	0Fh	-	No
Compute Power Properties	3-82	PICMG	10h	-	No
Set Power Level	3-84	PICMG	11h	-	No
Get Power Level	3-83	PICMG	12h	-	No
Renegotiate Power	3-91	PICMG	13h	-	No
Get Fan Speed Properties	3-86	PICMG	14h	-	No
Set Fan Level	3-88	PICMG	15h	-	No
Get Fan Level	3-87	PICMG	16h	-	No
Bused Resource	3-62	PICMG	17h	-	No
Get IPMB Link Info	3-68	PICMG	18h	-	No
Get Shelf Manager IPMB Address	3-38	PICMG	1Bh	-	No
Set Fan Policy	3-89	PICMG	1Ch	-	No
Get Fan Policy	3-90	PICMG	1Dh	-	No
FRU Control Capabilities	3-26	PICMG	1Eh	-	Yes
FRU Inventory Device Lock Control	3-42	PICMG	1Fh	-	No
FRU Inventory Device Write	3-43	PICMG	20h	-	No
Get Shelf Manager IP-Addresses	3-36	PICMG	21h	-	No
Get Shelf Power Allocation	3-85	PICMG	22h	-	No
Get Telco Alarm Capability	3-93	PICMG	29h	-	No
Set Telco Alarm State	3-94	PICMG	2Ah	-	No
Get Telco Alarm State	3-95	PICMG	2Bh	-	No
Get Telco Alarm Location	3-96	PICMG	39h	-	No

Table G.19: AdvancedTCA (PICMG 3.0 R3.0 AdvancedTCA Base Specification)					
Set FRU Extracted	3-25	PICMG	3Ah	-	No

Table G.20: HPM.1 (R1.0)					
Command	**HPM.1 Table**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Get target upgrade capabilities	3-3	PICMG	2Eh	-	Yes
Get component properties	3-5	PICMG	2Fh	-	Yes
Abort Firmware Upgrade	3-15	PICMG	30h	-	Yes
Initiate upgrade action	3-8	PICMG	31h	-	Yes
Upload firmware block	3-9	PICMG	32h	-	Yes
Finish firmware upload	3-10	PICMG	33h	-	Yes
Get upgrade status	3-2	PICMG	34h	-	Yes
Activate firmware	3-11	PICMG	35h	-	Yes
Query Self-test Results	3-12	PICMG	36h	-	Yes
Query Rollback status	3-13	PICMG	37h	-	Yes
Initiate Manual Rollback	3-14	PICMG	38h	-	Yes

G.3 OEM/Group IPMI Commands

Table G.21: Advantech OEM Commands				
Command	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Store Configuration Settings	OEM/Group	40h	-	Yes
Read Configuration Settings	OEM/Group	41h	-	Yes
Read Port 80	OEM/Group	80h	-	Yes
Clear NVRAM Data	OEM/Group	81h	-	Yes
Read MAC Address	OEM/Group	E2h	-	Yes
Load Default Configuration	OEM/Group	F2h	-	Yes

Appendix H

Driver & Tools

H.1 OpenIPMI

The OpenIPMI project provides an IPMI Kernel driver which is available in most of the Linux distributions.

The Open IPMI Linux device driver is designed as a full-function IPMI device driver with the following features:

- Allows multiple users.
- Allows multiple interfaces.
- Allows both kernel and userland things to use the interface.
- Fully supports the watchdog timer.
- It works like IPMI drivers are supposed to. It tracks outgoing messages and matches up their responses automatically. It automatically fetches events, received messages, etc.
- It supports interrupts (I have tested them now).
- It has backwards-compatability modules for supporting the Radisys IPMI driver and the Intel IMB driver.
- It's modular. You don't have to have the standard userland interface. You don't have to have the watchdog. Etc.
- It supports generating an event on a panic.

Source: OpenIPMI Page (http://openipmi.sourceforge.net/)

More information regarding the IPMI driver can be found on the OpenIPMI Project page, http://openipmi.sourceforge.net/

The KCS register interfaces are at 0xCA2 /0xCA3 and used by the OpenIPMI driver as default.

H.2 IPMITool

The IPMITool provides an easy-to-use set of functions and commands, to access the BMC via the KCS interface within the Operating System of the MIC-6311 or via Ethernet through NC-SI from external. The IPMI Tool also supports bridged IPMI commands to access the BMC, if the carrier manager provides an IPMI-over-LAN interface. See Chapter xxx for a more detailed description of different access methods and IPMITool calls.

The IPMITool source code can be downloaded from the official project page:

http://ipmitool.sourceforge.net.

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