NEX-VME

VME Bus Adapter Users Manual

Including these Software Support packages:

VME

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1.0 OVERVIEW

1.1 General Information

The NEX-VME adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, a 92A96, or a 92C96 acquisition module to a VME backplane. In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

The included software will permit the acquisition of VME bus cycles, and will display the data in easy-to-read symbolic form rather than raw hexadecimal or binary data.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA600/700 apply to a TLA704, 711, 714, 715, 720 or 721 chassis with one or more 7*3/4 acquisition cards.

Appendix D is a silk-screen print of the NEX-VME Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the VME Bus specification and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with M.S. Windows.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

One 3½” diskette has been included with the NEX-VME Bus Adapter. It is used with the TLA600/700 series. Diskettes for the DAS9200 or TLA500 are available upon request. Please see Appendix E for contact information.

2.1 TLA600/700

The VME support software is loaded in the same method as other Winows programs. Place the NEX-VME Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose VME and click on **Okay**. Note that the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "VME Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-VME BUS ADAPTER

3.1 General Information

The number of signals defined by the VME specification exceeds the channel count of a single 92A96 acquisition card. Because of this, jumper blocks have been defined to permit the selective monitoring of specific signals. By placing a shorting jumper across the pair of pins next to the desired signal name, that signal can then be monitored during the acquisition. These jumper blocks are provided for the BR0-3~ and BGIN0-3~ signals. For information on physically modifying the NEX-VME adapter to monitor signals not provided with the standard implementation, refer to Appendix C.

4.0 CONNECTING to the NEX-VME ADAPTER

4.1 General

The NEX-VME adapter is designed to plug directly into a VME backplane slot. The board will fit in 'B', 'C', and 'D' size VME slots.

4.2 TLA600/700

When using NEX-VME support with a TLA600/700 containing a 7*3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the A96. Follow the silk-screened information on the board that shows the proper relationship between the signal and

reference inputs. When properly connected, the sides of the podlets that have writing on them should be visible.

Connect the four clock leads to their specified locations at J15 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA600/700 when used with the NEX-VME adapter.

4.3 92A96

When using a 92A96 or 92C96, connect the grouped pods to their appropriate locations by following the silk-screen information printed on the adapter board. The 92A/C96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. When properly connected, the colored sides of the podlets should be visible.

Connect the four clock leads (one per A96 cable) to their specified locations at J15 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-VME adapter.

Group Name	Signal Name	VME Pin #	TLA600/700 / 92A96 input	Group Name	Signal Name	VME Pin #	TLA600/700 / 92A96 input
Address (Hex)	A31	J2/B11	A3:7	Data (Hex)	D31	J2/B30	D3:7
	A30	J2/B10	A3:6		D30	J2/B29	D3:6
	A29	J2/B09	A3:5		D29	J2/B28	D3:5
	A28	J2/B08	A3:4		D28	J2/B27	D3:4
	A27	J2/B07	A3:3		D27	J2/B26	D3:3
	A26	J2/B06	A3:2		D26	J2/B25	D3:2
	A25	J2/B05	A3:1		D25	J2/B24	D3:1
	A24	J2/B04	A3:0		D24	J2/B23	D3:0
	A23	J1/C15	A2:7		D23	J2/B21	D2:7
	A22	J1/C16	A2:6		D22	J2/B20	D2:6
	A21	J1/C17	A2:5		D21	J2/B19	D2:5
	A20	J1/C18	A2:4		D20	J2/B18	D2:4
	A19	J1/C19	A2:3		D19	J2/B17	D2:3
	A18	J1/C20	A2:2		D18	J2/B16	D2:2
	A17	J1/C21	A2:1		D17	J2/B15	D2:1
	A16	J1/C22	A2:0		D16	J2/B14	D2:0
	A15	J1/C23	A1:7		D15	J1/C08	D1:7
	A14	J1/C24	A1:6		D14	J1/C07	D1:6
	A13	J1/C25	A1:5		D13	J1/C06	D1:5
	A12	J1/C26	A1:4		D12	J1/C05	D1:4
	A11	J1/C27	A1:3		D11	J1/C04	D1:3
	A10	J1/C28	A1:2		D10	J1/C03	D1:2
	A9	J1/C29	A1:1		D9	J1/C02	D1:1
	A8	J1/C30	A1:0		D8	J1/C01	D1:0
	A7	J1/A24	A0:7		D7	J1/A08	D0:7
	A6	J1/A25	A0:6		D6	J1/A07	D0:6
	A5	J1/A26	A0:5		D5	J1/A06	D0:5
	A4	J1/A27	A0:4		D4	J1/A05	D0:4
	A3	J1/A28	A0:3		D3	J1/A04	D0:3
	A2	J1/A29	A0:2		D2	J1/A03	D0:2
	A1	J1/A30	A0:1		D1	J1/A02	D0:1
	A0	ground	A0:0		D0	J1/A01	D0:0
Transfer (Sym)	DS1~	J1/A12	C2:3	Mode (Sym)	AM5	J1/C14	C0:5
	DS0~	J1/A13	C2:2		AM4	J1/A23	C0:4
	A1	J1/A30	C2:7		AM3	J1/B19	C0:3
	LWORD	J1/C13	C2:6		AM2	J1/B18	C0:2
Misc (Sym)	SYSCLK	J1/A10	C3:6		AM1	J1/B17	C0:1
	SRST~	J1/C12	C1:0		AM0	J1/B16	C0:0
	ACFAIL~	J1/B03	C3:5	Intrpts (Hex)	IACKIN~	J1/A21	C0:7
	SYSFAIL~	J1/C10	C3:4		IACK~	J1/A20	C0:6
	DTACK~	J1/A16	C2:0		IRQ7~	J1/B24	C1:7
	BERR~	J1/C11	C2:1		IRQ6~	J1/B25	C1:6
	AS~	J1/A18	C2:5		IRQ5~	J1/B26	C1:5
	WRITE~	J1/A14	C2:4		IRQ4~	J1/B27	C1:4
BusMstr (Hex)	BCLR~	J1/B02	C3:3		IRQ3~	J1/B28	C1:3
	BBSY~	J1/B01	C3:2		IRQ2~	J1/B29	C1:2
	BR#~	- - -	C3:1		IRQ1~	J1/B30	C1:1
	BG#IN~	- - -	C3:0	Clock:0	DTACK~	J1/A16	- - - - -
				Clock:1	BERR~	J1/C11	- - - - -
				Clock:2	SYSCLK	J1/A10	- - - - -
				Clock:3	AS~	J1/A14	- - - - -

Table 1- VME TLA600/700/92A96 Wiring

5.0 CLOCK SELECTION and VIEWING DATA

5.1 General Information

All VME data is acquired on either the falling edge of DTACK~ or the falling edge of BERR~.

5.2 Viewing State Data on the TLA600/700

After making an initial acquisition, the TLA600/700 will display the data in the Listing (State) format. Address and Data information is displayed in hexadecimal format; Transfer, Mode, and Misc data is displayed using symbols; Interrupts (Intrpts) and Bus Master (BusMstr) data groups default to Hexadecimal.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-VME, a symbol table (VME_Xfer, Table 2) has been provided to show the type of transfer that occurred on the VME bus. This symbol table quickly shows how wide the bus transfer was (1-byte, 2-bytes, etc.). A second symbol table (VME_Misc, Table 3) shows whether the bus transaction was a Read, Write, Bus Error, etc. A third symbol table (VME_Mode, Table 4) shows the type of operation (Supervisory, Privileged, etc.).

It is important to note that changing the group, channel, or wiring of the Transfer, Misc, or Mode groups can result in incorrect symbol information being displayed.

Pattern	TLA600/700 / 92A96 Symbol
0000	Quad_byte_0-3
0001	Double_byte_0-1
0010	Byte_1-2
0011	Double_byte_2-3
0100	Byte_0-2
0101	Single_even_byte0
0110	Illegal
0111	Single_even_byte2
1000	Byte_1-3
1001	Single_odd_byte1
1010	Illegal
1011	Single_odd_byte3
11xx	Address_only

Table 2- VME_Xfer Symbol Table

Signals, from left to right: DS1~, DS0~, A1, LWORD

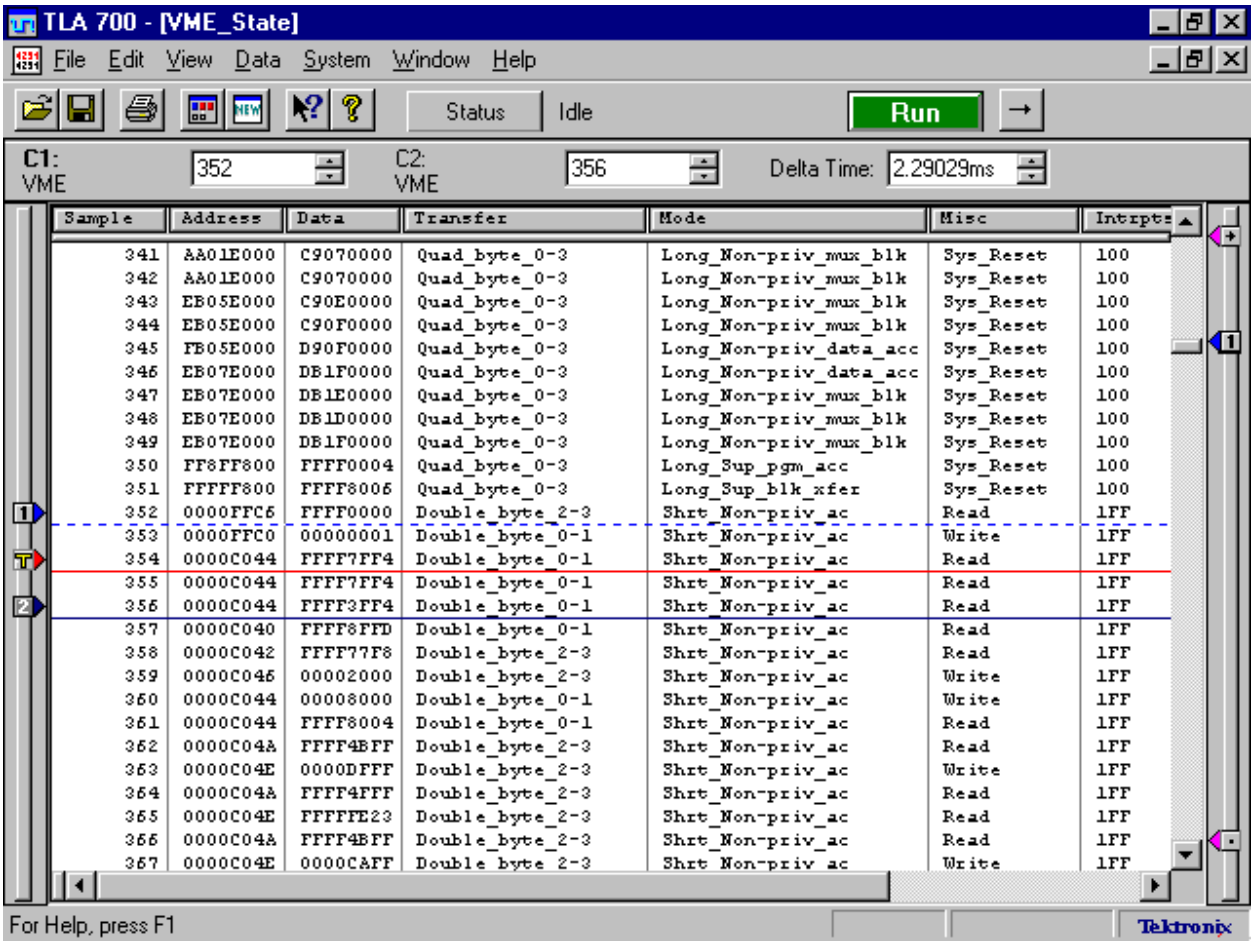


Figure 1- VME State Display on TLA600/700

Pattern	TLA600/700 / 92A96 Symbol
x0xxxxxx	Sys_Reset
xx0xxxxx	AC_Fail
xxx0xxxx	Sys_Fail
xxxxx0xx	Bus_Error
xxxxxxx0	Write
xxxxxxx1	Read

Table 3- VME_Misc Symbol Table

Signals, from left to right: SYSCLK, SRST~, ACFAIL~, SYSFAIL~, DTACK~, BERR~, AS~, WRITE~

Pattern	TLA600/700 / 92A96 Symbol	Meaning
111111	Std_Sup_blk_xfer	Standard Supervisory Block Transfer
111110	Std_Sup_pgm_acc	Standard Supervisory Program Access
111101	Std_Sup_data_acc	Standard Supervisory Data Access
111100	Std_Sup_mux_blk	Standard Supervisory Muxed Block Transfer
111011	Std_Non-priv_blk	Standard Non-Privileged Block Transfer
111010	Std_Non-priv_pgm	Standard Non-Privileged Program Access
111001	Std_Non-priv_dat	Standard Non-Privileged Data Access
111000	Std_Non-priv_mux_blk	Standard Non-Privileged Muxed Block Transfer
110xxx	Reserved	Reserved by VME Bus Specification
10111x	Reserved	Reserved by VME Bus Specification
101101	Shrt_Sup_access	Short Supervisory Access
101100	Reserved	Reserved by VME Bus Specification
10101x	Reserved	Reserved by VME Bus Specification
101001	Shrt_Non-priv_ac	Short Non-Privileged Access
101000	Reserved	Reserved by VME Bus Specification
100xxx	Reserved	Reserved by VME Bus Specification
01xxxx	User-defined	Available for User Definition
001111	Ext_Sup_blk_xfer	Extended Supervisory Block Transfer
001110	Ext_Sup_pgm_acc	Extended Supervisory Program Access
001101	Ext_Sup_data_acc	Extended Supervisory Data Access
001100	Ext_Sup_mux_blk	Extended Supervisory Muxed Block Transfer
001011	Ext_Non-priv_blk	Extended Non-Privileged Block Transfer
001010	Ext_Non-priv_pgm	Extended Non-Privileged Program Access
001001	Ext_Non-priv_data	Extended Non-Privileged Data Access
001000	Ext_Non-priv_mux_blk	Extended Non-Privileged Muxed Block Transfer
000111	Long_Sup_blk_xfer	Long Supervisory Block Transfer
000110	Long_Sup_pgm_acc	Long Supervisory Program Access
000101	Long_Sup_data_acc	Long Supervisory Data Access
000100	Long_Sup_mux_blk	Long Supervisory Muxed Block Transfer
000011	Long_Non-priv_blk_xfer	Long Non-Privileged Block Transfer
000010	Long_Non-priv_pgm_acc	Long Non-Privileged Program Access
000001	Long_Non-priv_data_acc	Long Non-Privileged Data Access
000000	Long_Non-priv_mux_blk	Long Non-Privileged Muxed Block Transfer

Table 4- VME_Mode Symbol Table

Signals, from left to right: AM5, AM4, AM3, AM2, AM1, AM0

5.3 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: VME and VME-MagniVu. The first (VME) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, VME-MagniVu, will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

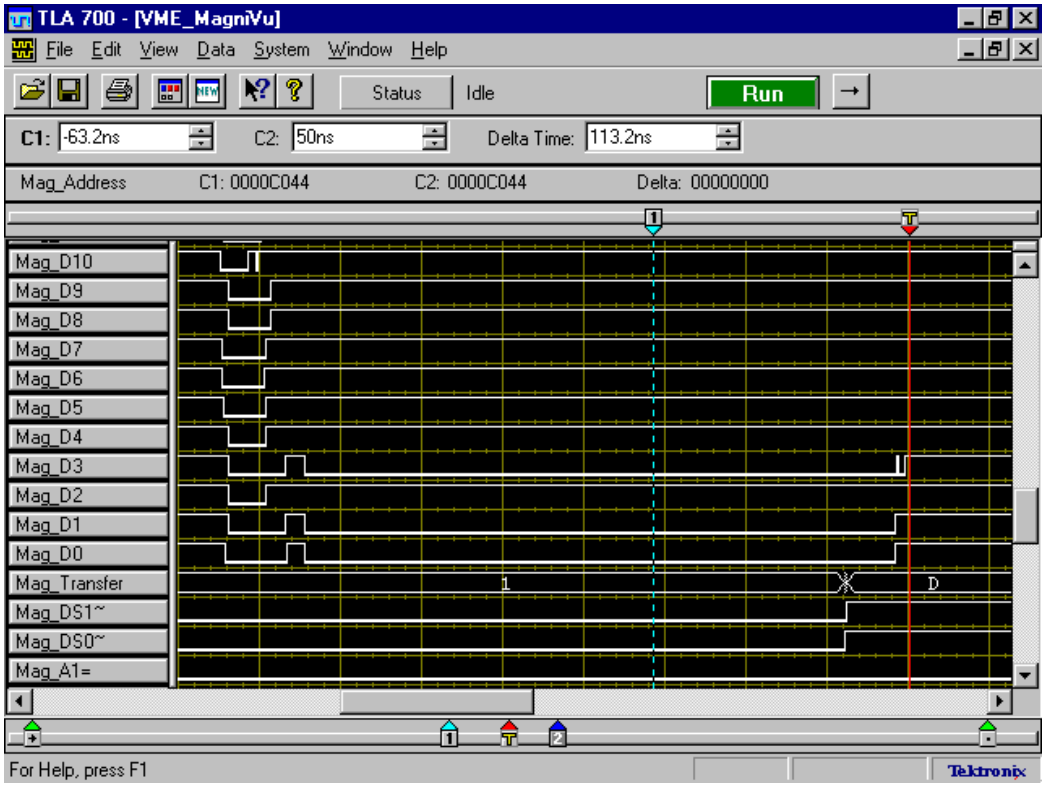


Figure 2- VME MagniVu Display on TLA600/700

5.4 Viewing State Data on the DAS9200/TLA500

After making an initial acquisition, the DAS9200 Logic Analyzer will display the data in the State format. Address and Data information is displayed in hexadecimal format; Transfer, Mode, and Misc data is displayed using symbols; Interrupts (Intrpts) and Bus Master (BusMstr) data groups default to Hexadecimal.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-VME, a symbol table (VME_Xfer, Table 2) has been provided to show the type of transfer that occurred on the VME bus. This symbol table quickly shows how wide the bus transfer was (1-byte, 2-bytes, etc.). A second symbol table (VME_Misc, Table 3) shows whether the bus transaction was a Read, Write, Bus Error, etc. A third symbol table (VME_Mode, Table 4) shows the type of operation (Supervisory, Privileged, etc.).

It is important to note that changing the group, channel, or wiring of the Transfer, Misc, or Mode groups can result in incorrect symbol information being displayed.

5.5 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire VME data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

APPENDIX A - Necessary Signals for Clocking

Because of the relative simplicity of the VME bus, only DTACK~ and BERR~ are needed to clock data from the backplane.

APPENDIX B - Considerations

B.1 VME Loading

It must be noted that the NEX-VME Bus Adapter violates the VME specification of 2½" maximum run length. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-SIA adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 or 92A96 acquisition cards is low enough so that VME signal degradation will not occur.

The NEX-VME Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity.

B.2 "Patch" Areas

If signal loading or reflection does become a concern, the capability exists to add series resistors to any VME signal. Patch areas have been provided next to each TLA600/700/A96 connector, consisting of two rows of plated through holes. These areas (outlined on the silk-screen and labeled as Nxx) are suitable for individual resistors or resistor networks. To add a series resistor, simply cut the trace of the desired signal on the component side of the board, and solder the resistor between the two feed-throughs.

B.3 Prototype Area

A 2-inch-by-2-inch grid of holes can be used as a prototype area. This area can be used to monitor VXI bus signals with other equipment, or to add connectors to monitor other user-defined signals. The power supply voltages from the backplane are also brought out to pads and labeled for easy access.

B.4 Pattern Generation

Because there is no buffer circuitry on the NEX-VME Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS9200. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without providing adequate cooling for their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which are passive and do not have such cooling requirements.

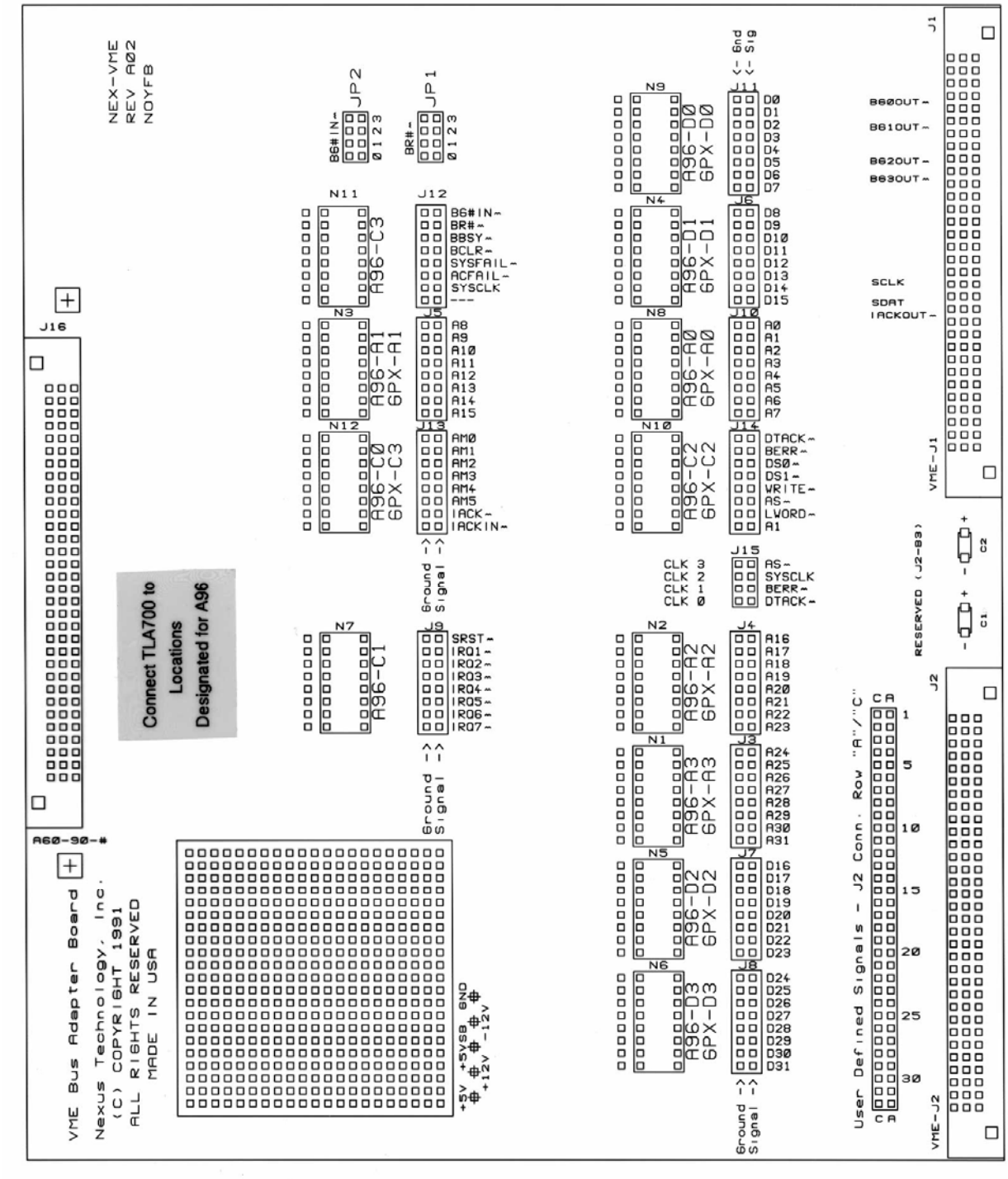
B.5 BGIN~ and BGOUT~ Signals

Unlike standard VME cards, the BGIN~ and BGOUT~ signals are not connected on the NEX-VME adapter. This requires the user to ensure that these signals are jumpered on the backplane for proper signal continuity. This concern can be avoided by installing the NEX-VME card in the last slot of the VME backplane.

APPENDIX C - VME Bus Pinout

J1/P1 Pin Assignments				J2/P2 Pin Assignments			
Pin #	**ROWa**	**ROWb**	**ROWc**	**Pin #**	**ROWa**	**ROWb**	**ROWc**
1	D0	BBSY~	D8	1	User Defined	+5V	User Defined
2	D1	BCLR~	D9	2	“	ground	“
3	D2	ACFAIL~	D10	3	“	RESERVD	“
4	D3	BG0IN~	D11	4	“	A24	“
5	D4	BG0OUT~	D12	5	“	A25	“
6	D5	BG1IN~	D13	6	“	A26	“
7	D6	BG1OUT~	D14	7	“	A27	“
8	D7	BG2IN~	D15	8	“	A28	“
9	ground	BG2OUT~	ground	9	“	A29	“
10	SYSCLK	BG3IN~	SYSFAIL~	10	“	A30	“
11	ground	BG3OUT~	BERR~	11	“	A31	“
12	DS1~	BR0~	SYSRST~	12	“	ground	“
13	DS0~	BR1~	LWORD~	13	“	+5V	“
14	WRITE~	BR2~	AM5	14	“	D16	“
15	ground	BR3~	A23	15	“	D17	“
16	DTACK~	AM0	A22	16	“	D18	“
17	ground	AM1	A21	17	“	D19	“
18	AS~	AM2	A20	18	“	D20	“
19	ground	AM3	A19	19	“	D21	“
20	IACK~	ground	A18	20	“	D22	“
21	IACKIN~	SERCLK1	A17	21	“	D23	“
22	IACKOUT~	SERDAT1~	A16	22	“	ground	“
23	AM4	ground	A15	23	“	D24	“
24	A7	IRQ7~	A14	24	“	D25	“
25	A6	IRQ6~	A13	25	“	D26	“
26	A5	IRQ5~	A12	26	“	D27	“
27	A4	IRQ4~	A11	27	“	D28	“
28	A3	IRQ3~	A10	28	“	D29	“
29	A2	IRQ2~	A9	29	“	D30	“
30	A1	IRQ1~	A8	30	“	D31	“
31	-12V	+5VSTDBY	+12V	31	“	ground	“
32	+5V	+5V	+5V	32	“	+5V	“

APPENDIX D - NEX-VME Silk Screen



APPENDIX E - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX F - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Logic Analyzer User's Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

IEEE Standard for a Versatile Backplane Bus: VMEbus
ANSI/IEEE Std 1014-1987