PowerDNA DIO-40x User Manual

24-channel Digital I/O layer
for the PowerDNA Cube

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Introduction

This document outlines the feature-set and use of the DIO-401, DIO-402, and DIO-404/5 digital input layers for the PowerDNA I/O Cube.

Organization of this manual

This PowerDNA DIO-401/2/5 User Manual is organized as follows:

Introduction
This chapter provides an overview of PowerDNA Digital Input Series board features, the various models available and what you need to get started.

The DIO-401/2/5 layer
This chapter provides an overview of the device architecture, connectivity, and logic of the DIO-401/2/5 series layer.

Programming using the UeiDaq Framework High-Level API
This chapter provides an overview of the how to create a session, configure the session for digital data acquisition/output, and format relevant output.

Programming using the Low-Level API
Low-level API commands for configuring and using the DIO-401/2/5 series layer.

Appendix A - Accessories
This appendix outlines accessories available for DIO-401/2/5 series layer.

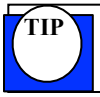
Appendix B - Layer Verification
This appendix outlines how to verify calibration for the DIO-401/2/5 series layer.

Glossary
This is an alphabetical listing of key terms you will encounter in working with the PowerDNA cube and test systems in general.

Index
This is an alphabetical listing of the topics covered in this manual.

Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:



Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

Note Notes alert you to important information.

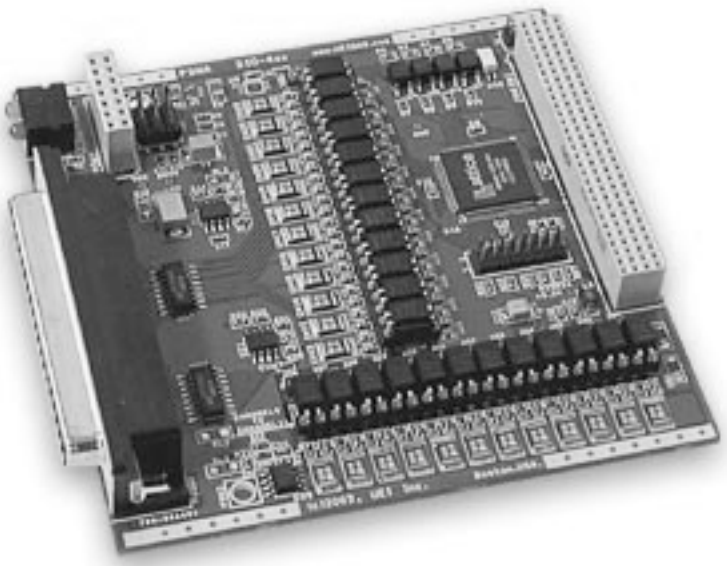
CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: "You can instruct users how to run setup using a command such as **setup.exe**."

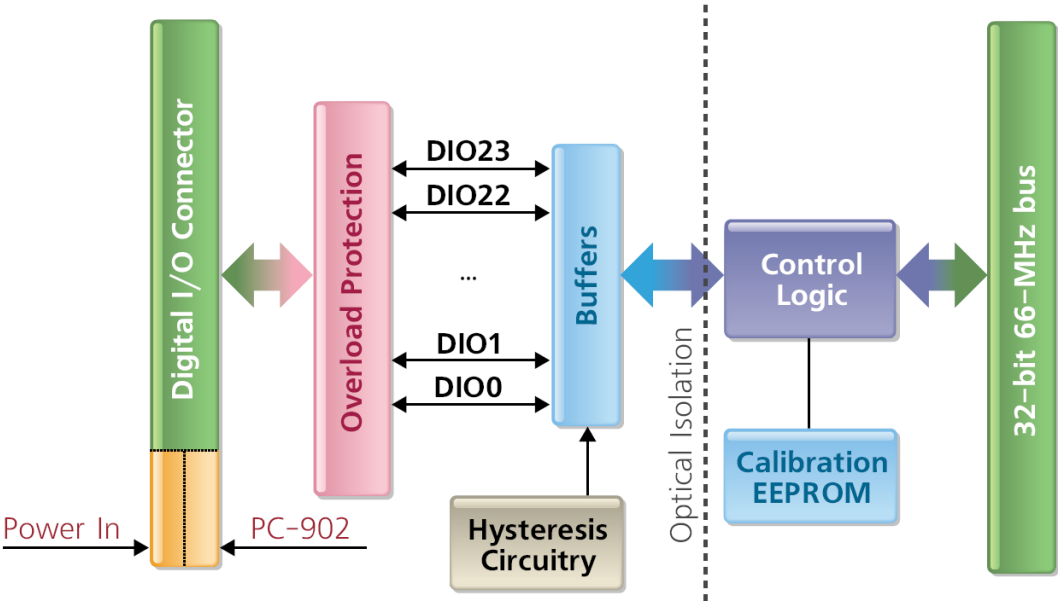
1 The DIO-40x Layer

The DIO-40x layers have the following functions:

- DIO-401/2/5 are digital I/O layers.
- DIO-401 has 24 digital inputs.
- DIO-402 has 24 digital outputs.
- DIO-405 has 12 digital inputs and 12 digital outputs.
- Lines handle levels to 24V on inputs and outputs
- Lines protected to 1000V peak-peak and 7-kV electrostatic
- Over and under-voltage protection to +/-36V
- Input rate is 2k samples/sec with hysteresis enabled
- Outputs provide drive capability of 80 mA/channel, resetable fuse protected to 100mA
- Inputs have 1024 point programmable low and high hysteresis settings
- Peak detection 1ms
- Triggering, edge detection, event time stamping is available on digital inputs at software level
- Power consumption: 2.5W at full load



1.1 Device architecture



The DIO-40x layers have similar architecture. The I/O part of the layer is isolated from the logic interface via optocouplers.

1.2 Layer connectors and wiring

DNA-DIO-401

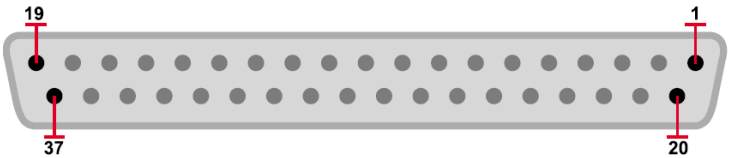
*VCC	37	19	VCC*
DGND	36	18	VCC*
DIN23	35	17	DGND
DIN21	34	16	DIN22
DIN20	33	15	DGND
DIN18	32	14	DIN19
DIN17	31	13	DGND
DIN15	30	12	DIN16
DIN14	29	11	DGND
DIN12	28	10	DIN13
DIN11	27	9	DGND
DIN9	26	8	DIN10
DIN8	25	7	DGND
DIN6	24	6	DIN7
DIN5	23	5	DGND
DIN3	22	4	DIN4
DIN2	21	3	DGND
DIN0	20	2	DIN1
		1	DGND

DNA-DIO-402

*VCC	37	19	VCC*
DGND	36	18	VCC*
DOUT23	35	17	DGND
DOUT21	34	16	DOUT22
DOUT20	33	15	DGND
DOUT18	32	14	DOUT19
DOUT17	31	13	DGND
DOUT15	30	12	DOUT16
DOUT14	29	11	DGND
DOUT12	28	10	DOUT13
DOUT11	27	9	DGND
DOUT9	26	8	DOUT10
DOUT8	25	7	DGND
DOUT6	24	6	DOUT7
DOUT5	23	5	DGND
DOUT3	22	4	DOUT4
DOUT2	21	3	DGND
DOUT0	20	2	DOUT1
		1	DGND

DNA-DIO-405[1]

*VCC	37	19	VCC*
DGND	36	18	VCC*
DOUT11	35	17	DGND
DOUT9	34	16	DOUT10
DOUT8	33	15	DGND
DOUT6	32	14	DOUT7
DOUT5	31	13	DGND
DOUT3	30	12	DOUT4
DOUT2	29	11	DGND
DOUT0	28	10	DOUT1
DIN11	27	9	DGND
DIN9	26	8	DIN10
DIN8	25	7	DGND
DIN6	24	6	DIN7
DIN5	23	5	DGND
DIN3	22	4	DIN4
DIN2	21	3	DGND
DIN0	20	2	DIN1
		1	DGND



[1]Please notice that DIO-405 outputs are numbered from *DOut0* through *DOut11*. All layers in the DIO-40x family have similar connector layout.

Note the **VCC*** pins. This layer must be supplied power in one of two forms:

- By use of the VCC pins on the DNA-STP-37 or STP-37D or DNA-DIO-O22 terminal panels: connect a 5-36V source to the VCC pins.
- By use of the PC-902 power conversion layers, which supply power internally and will not break any isolation.

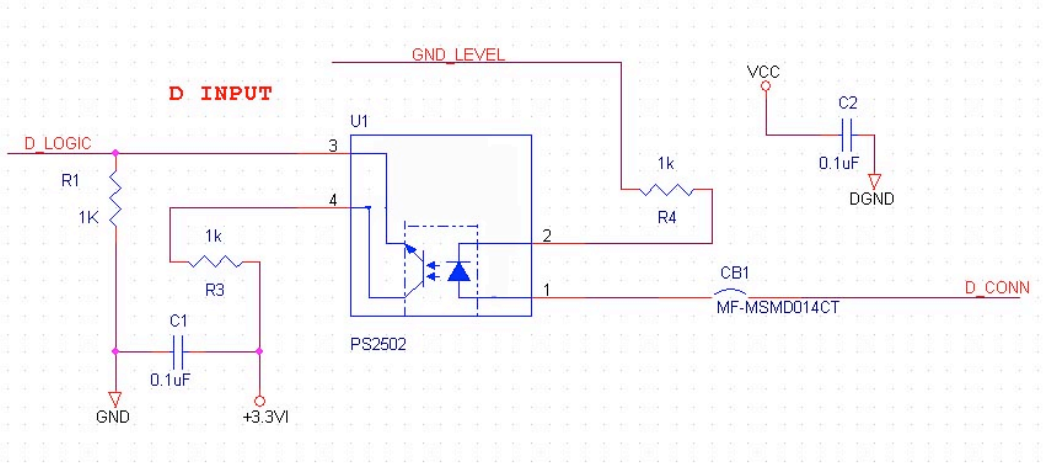
When power is provided to the layer, the RDY LED turns on. When no power is supplied, the RDY LED is off, and the DNA-DIO-40x layer will not operate.

1.3 Layer capabilities

Inputs and outputs of these layers are powered externally. The user has to supply from 5V to 24V external power to *VCC* line. Depending on power supply, the layer accepts the following levels:

VCC	Input "0"	Input "1"	Output "0"	Output "1"
5V	1.2V	3.0V	0.6V	4.5V
24V	5V	12V	2V	22V
36V	7V	12V	-	-

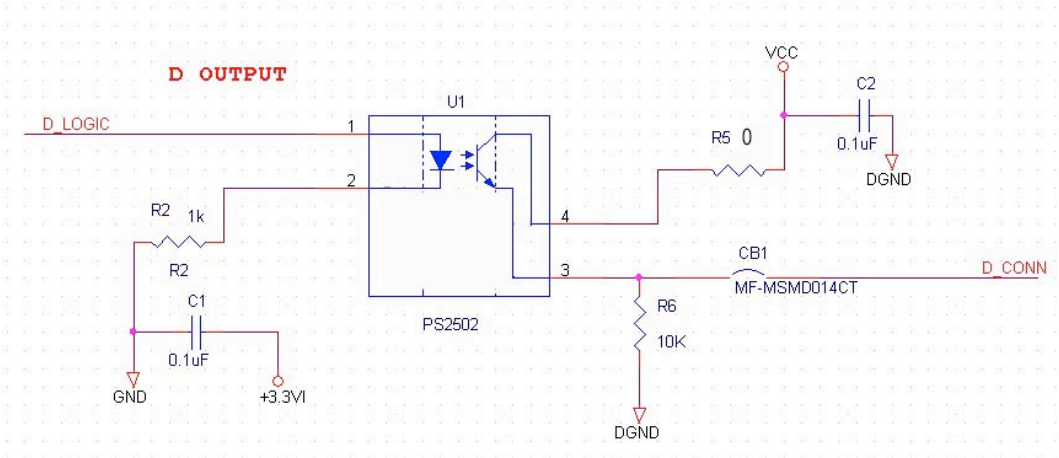
Every input circuitry is built as follows:



To switch input to a logical one, the user should provide current flowing through the LED in the optical isolator. The minimum current requirement is 2.4mA. The current is limited by resistor R4 and can be as high as 36mA at the maximum input voltage.

The user can put a current limiting resistor in series with input to limit both current flowing through the LED, and the power dissipation inside the PowerDNA cube. *VCC* is required to power ground level DACs to provide ground level reference. Inputs will not work properly without supplying *VCC* unless ground layer feature is disabled internally by shorting ground level to *DGND* by jumpers.

Every output circuitry is built as follows:



The maximum current thru the transistor should is limited to 100mA by the *CB1* fuse. User should supply *VCC* to collector of the transistor.

For testing, place a 1k to 10k resistor in-line between the Digital Output and ground. The voltage across the resistor is the output, plus loss.

2 Programming using the UeiDaq Framework

This section describes how to control the PowerDNA DIO-401/2/5 using the UeiDaq's framework API.
The UeiDaq framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.
The following section will focus on the C++ API but the concept stay the same no matter what programming language you use.
Please refer to the "UeiDaq Framework User Manual" to get more information on using other programming languages.

2.1 Creating a session

The Session object controls all operations on your PowerDNA device. Therefore, the first task is to create a session object:

```
CUeiSession session;
```

2.2 Configuring the resource string

The framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>

For PowerDNA the device class is **pdna**.
For example the following resource string selects digital input channels 0,1,2,3 on device 1 at IP address 192.168.100.2: "pdna://192.168.100.2/Dev1/Di0:3"

Note In the framework a digital channel correspond to a physical port on the device. You cannot configure a session to only access a subset of the lines within a digital port.

```
// Configure session to read from port 0 on device 1
di_session.CreateDIChannel("pdna://192.168.100.2/Dev1/Di0");
```

```
// Configure session to write to port 0 on device 1
do_session.CreateDOChannel("pdna://192.168.100.2/Dev1/Do0");
```

Note Sessions are unidirectional. If your device has both input and output ports or has bidirectional ports, you need to configure two sessions: one for input and one for output.

2.3 Configuring the timing

You can configure the DIO-401/2/5 to run in simple mode (point by point) or buffered mode (ACB mode).
In simple mode, the delay between samples is determined by software on the host computer.
In buffered mode the delay between samples is determined by the DIO-401/2/5 on-board clock.

The following sample shows how to configure the simple mode. Please refer to the "UeiDaq Framework User's Manual" to learn how to use the other timing modes.

```
di_session.ConfigureTimingForSimpleIO();
```

2.4 Configuring the hysteresis

The PowerDNA DIO-401/2/5 layers are equipped with a hysteresis circuitry whose low and high threshold levels can be programmed using custom properties.

- "lowhysteresis":A floating-point value representing the low hysteresis voltage as a percentage of the power supply voltage (Vcc).
- "highhysteresis": A floating-point value representing the high hysteresis voltage as a percentage of the power supply voltage (Vcc).

```
// Program low threshold to 10% and high threshold to 90%
double lowHyst = 0.1;
double highHyst = 0.9;
di_session.SetCustomProperty("lowhysteresis", sizeof(double),
&lowHyst);
di_session.SetCustomProperty("highhysteresis", sizeof(double),
&highHyst);
```

2.5 Reading and Writing data

Reading data from the DIO-401/2/5 is done using a reader object.
The following sample code shows how to create a scaled reader object and read samples.

```
// Create a reader and link it to the session's stream
CUeiDigitalReader reader(di_session.GetDataStream());

// read one scan, the buffer must be big enough to contain
// one value per channel
uInt16 data;
reader.ReadSingleScan(&data);
```

Writing data is done using a writer object. The following sample shows how to create a writer object and write data .

```
// Create a writer and link it to the session's stream
CUeiDigitalWriter writer(do_session.GetDataStream());

// write one scan, the buffer must contain
// one value per channel
uInt16 data = 0xFEFE;
writer.WriteSingleScan(&data);
```

2.6 Cleaning-up the session

The session object will clean itself up when it goes out of scope or when it is destroyed. However, you can manually clean up the session (to reuse the object with a different set of channels or parameters).

```
di_session.CleanUp();
```

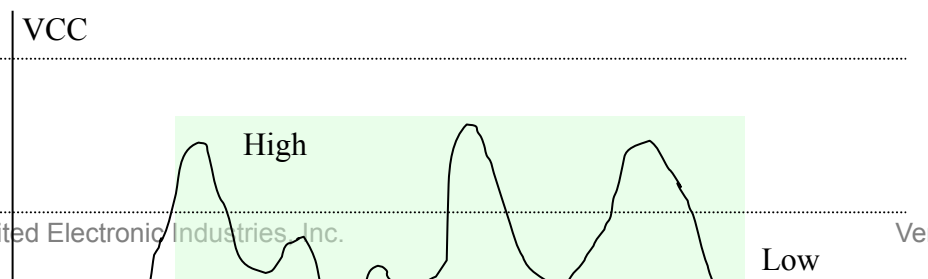
3 Programming using the Low-Level API

This section describes how to program the PowerDNA cube using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to directly access device registers.
We recommend that you use the UeiDaq framework (*see Section 2 above*) which is easier to use.
You should only need to use the low-level API if you are using an operating system other than Windows.

3.1 Programming hysteresis

The ground level of the inputs can be set from *DGND* level to *VCC* level in 1024 steps (increments). For the optical isolator to open input level, it should be above ground level to at least 2.4V to supply enough current for isolator LED.
When programmable hysteresis mode is disabled, input becomes "1" if input voltage is 2.4V above selected ground level (to provide enough current to the isolating LED.)
When programmable hysteresis mode is selected, the device logic constantly changes ground level between two programmed levels. This change of ground level occurs at 2kHz rate. Every time the logic changes ground level, it performs "read". Then the logic produces output based on two consecutive reads at low and high ground level. The following table summarizes the result.

Logic level\ Read result	Read at low	Read at High	Result
	0	0	0
	1	0	Keep previous value
	1	1	1



The following diagram shows the hysteresis feature. The input stays at “0” until it crosses both low and high ground levels. If the signal falls below high ground level but never crosses low ground level (for more than 1ms) it remains at “1”.

Hysteresis is a specific feature of DIO-40x layers. To access this feature you should enable it in the configuration word:

```
#define DQ_L401_HYSTEN      (1UL<<18)   // hysteresis programming is
enabled
```

By default, hysteresis levels are selected at 25% of VCC (low) and 75% of VCC (high). User can set hysteresis levels using layer-specific function

```
DqAdv40xSetHyst(int hd, int devn, uint16 level0,
                uint16 level1)
```

`level0` and `level1` are 10-bit relative values for low and high hysteresis levels.

3.2 Data representation

Layer \ Bits	31…24	23…12	11…0
DIO-401	reserved	DIn23…12	DIn11…0
DIO-402	reserved	DOut23…12	DOut11…0
DIO-405	reserved	N/A	DIn/Out11…0

Data representation is straightforward.
Please note that output lines on DIO-405 layer used to occupies bits 11…0. Thus, to set up all lines into one, you have to write 0x000fff to DIO-405. State of bits 31…12 don’t matter.

3.3 Configuration settings

Configuration setting are passed in `DqCmdSetCfg()` function.
Not all configuration bits apply to DIO-40x layers.

The following bits are used:

```
#define DQ_LN_MAPPED     (1L<<15)  // For WRRD (DMAP) devices (automatically
selected)
#define DQ_LN_ACTIVE     (1L<<1)   // "STS" LED status
#define DQ_LN_ENABLED    (1L<<0)   // enable operations
```

The AO-40x has a range of layer-specific settings as follows.

Upper part of the configuration word – DIO-40x specific:

```
#define DQ_L401_HYSTEN      (1UL<<18)   // hysteresis programming is
enabled
```

The following modes are reserved for future use:

```
#define DQ_L401_MODESCAN   (FIFO_MODESCAN)  // single scan update mod (no
buffer)
#define DQ_L401_MODEDGE    (1UL << 16)      // edge detect mode
#define DQ_L401_MODEFIFO   (FIFO_MODEFIFO)  // continuous acquisition with
FIFO
                                            // (simplified buffer)
#define DQ_L401_MODECONT   (FIFO_MODECONT)  // continuous acquisition
(buffered)
```

`DQ_LN_ACTIVE` is needed to switch on “STS” LED on CPU layer.
`DQ_LN_ENABLE` enables all operations with the layer

3.4 Channel list settings

Channel list is not required.

3.5 Layer-specific commands and parameters

There are two layer-specific functions defined:

- `DqAdv40xWrite()`
  This function writes 24-bit word to the DIO-40x layer using `DQCMD_WRCHNL`.
- `DqAdv40xRead()`
  This function reads input status using `DQCMD_RDCHNL`.
- `DqAdv40xSetHyst()`

This function sets hysteresis levels.

These functions can be called anytime in configuration and operation mode.

3.6 Using layer in ACB mode

DIO-40x layer currently do not support ACB mode.

3.7 Using layer in DMap mode

This example shows communication between two layers: a layer 0 DI-401, and a layer 1 DO-402.

For a DIO-405, `DEVNIN` and `DEVNOUT` would be the same, and we'd assign a value only to bits 0-11 of `ooffset`, and read bits 0-11 of `ioffset`.

```
#include "PDNA.h"
```

1. Start DQE engine

```
#ifndef _WIN32
    DqInitDAQLib();
#endif

    // Start engine
    DqStartDQEngine(1000*10, &pDqe, NULL);

    // open communication with IOM
    DqOpenIOM(IOM_IPADDR0, DQ_UDP_DAQ_PORT, TIMEOUT_DELAY,
&DQRdCfg);

    // Set hysteresis at this point
    DqAdv40xSetHyst(hd0, DEVNIN, 0x132, 0x2CA);

    // Receive IOM crucial identification data
    DqCmdEcho(hd0, DQRdCfg);

    for (i = 0; i < DQ_MAXDEVN; i++) {
        if (DQRdCfg->devmod[i]) {
            printf("Model: %x Option: %x\n", DQRdCfg->devmod[i],
DQRdCfg->option[i]);
        } else {
```

```
            break;
        }
    }
```

2. Create and initialize host and IOM sides

```
    DqDmapCreate(pDqe, hd0, &pBcb, UPDATE_PERIOD, &dmapin,
&dmapout);
```

3. Add channels into DMap

```
    DqDmapSetEntry(pBcb, DEVNIN, DQ_SS0IN, 0, DQ_ACB_DATA_RAW, 1,
&ioffset);
    DqDmapSetEntry(pBcb, DEVNOUT, DQ_SS0OUT, 0, DQ_ACB_DATA_RAW,
1, &ooffset));

    DqDmapInitOps(pBcb);
    DqeSetEvent(pBcb, DQ_eDataAvailable|DQ_ePacketLost|
DQ_eBufferError|DQ_ePacketOOB);
```

4. Start operation

```
    DqeEnable(TRUE, &pBcb, 1, FALSE);
```

5. Process data

```
    while (keep_looping) {

        DqeWaitForEvent(&pBcb, 1, FALSE, timeout, &eventsin);

        if (eventsin & DQ_eDataAvailable) {
            datarcv++;
            printf("\ndata %08x ", *(uint32*)ioffset);
            *(uint32*)ooffset = datarcv;
        }
    }
```

6. Stop operation

```
    DqeEnable(FALSE, &pBcb, 1, FALSE);
```

7. Clean up

```
    DqDmapDestroy(pBcb);
    DqStopDQEngine(pDqe);
    DqCloseIOM(hd0);
```

```
#ifndef _WIN32
    DqCleanUpDAQLib();
#endif
```

4 Appendix

Appendix A - Accessories

The following cables and STP boards are available for the DIO-401/2/5 layer.

DNA-PC-902
+24V power conversion layer; supplies +24V to external devices at up to 40W

DNA-CBL-37
3ft, 37-way flat ribbon cable; connects layers to terminal panel.

DNA-DIO-O22
Accessory panel for PowerDNA DIO layers

DNA-STP-37
37-way screw terminal panel

DNA-STP-37D
37-way direct-connect screw terminal panel

Appendix B - Layer verification

The DIO-40x layers do not require calibration.
Layer verification is performed using “simod 1” command. To access it, the user should attach serial interface to the PowerDNA cube and run serial terminal program on the host PC. For DIO-40x “simod 1” command allows to read and write port (“r” and “w” command) as well as select hysteresis DAC (“1” and “2”) and adjust it using “[,],{,}” keys.
“q” or Esc causes the routine to exit.
The verification is done by setting up hysteresis levels (default are 25% for low and 75% for high ground levels) and continuously reading inputs while changing voltage on inputs. The easiest way to verify output is to attach LEDs between

layer outputs and DGND in series with proper resistors. For example, you can use 2 to 4.7 KOhm resistors to limit current flowing thru LEDs.

5 Glossary

A

ACB	see Advanced Circular Buffer
A/D (see ADC)	Analog/digital, often used in connection with an A/D converter.
adapter	Alternate designation for a function card that plugs into a backplane, often a PC.
ADC (also see A/D)	Analog-to-Digital Converter. An integrated circuit that converts an analog voltage to a digital number.
ADC conversion	The process of converting an analog input to its digital equivalent.
ADC conversion Start	Signal used to start the process of converting an analog input to a digital value. The source of this signal can be an internal clock or an external asynchronous signal.
ADC Channel List Start	Signal used to start the acquisition of digitized values as defined in the Channel List. The triggering edge of this signal (falling edge) enables the ADC conversion Start signals.
Advanced Circular Buffer	A special user-defined buffer in host memory that stores frames of collected data. The PowerDNA driver allows the user application to fetch data from this buffer in several modes.
alias	A false lower-frequency component that appears in sampled data that has been acquired at an insufficiently high sampling rate.
analog trigger	A trigger that occurs when an analog signal reaches a user-selected level. Users can configure triggering

to occur at a specific level on either an increasing or a decreasing signal (positive or negative slope).

API — Application Programming Interface, a collection of high-level language function calls that provide access the functions in a driver or other utility.

asynchronous — (1) Hardware—A property of an event that occurs at an arbitrary time, without synchronization to a reference clock.

(2) Software—A property of a function that begins an operation and returns prior to the completion or termination of the operation.

B

background acquisition — Data is acquired by a DAQ system while another program or processing routine is running without apparent interruption.

base address — A memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.

bipolar — A signal range that includes both positive and negative values (for example, -5V to +5V, also represented as ±5V).

bit — One binary digit, either 0 or 1.

Block mode — A high-speed data transfer in which the address of the data is sent followed by a specified number of back-to-back data words.

Burst mode — A high-speed data transfer in which the address of the data is sent followed by back-to-back data words while a physical signal is asserted.

bus The group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the PCI bus and the PXI bus.

bus master A type of plug-in board or controller that can read and write to devices on the computer bus without the assistance of the host CPU.

byte Eight related bits of data, an 8-bit binary number. Also used to denote the amount of memory required to store one byte of data.

C

cache High-speed processor memory that buffers commonly used instructions or data to increase processing throughput.

calibration The setting or correcting of a measuring device or base level, usually by adjusting it to match or conform to a dependably known and unvarying measure.

channel list For AO Series boards, a set of entries, one for every channel that should be updated. When the simultaneous-update feature is enabled, all channels are usually updated upon a write to the first or last channel in the channel list.

Channel List FIFO The on-board memory that holds the Channel List.

CL clock The Channel List clock, also known as the Burst clock, tells the control logic how quickly to move to the next entry in the Channel List and set up the front-end operating parameters such as gain.

control register Register containing control bits that set up and configure various onboard subsystems.

CMRR Common-Mode Rejection Ratio, a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).

code generator A software program, controlled from an intuitive user interface, that creates syntactically correct high-level source code in languages such as C or Basic.

cold-junction compensation The means to compensate for the ambient temperature in a thermocouple measurement circuit.

common-mode range The input range over which a circuit can handle a common-mode signal.

common-mode signal The mathematical average voltage, relative to the computer's ground, of the signals going into a differential input.

component software An application that contains one or more component objects that can freely interact with other component software. Examples

include OLE-enabled applications such as Microsoft Visual Basic and OLE Controls.

conversion time The time, in an analog input or output system, from the moment a channel is interrogated (such as with a Read instruction) to the moment that accurate data is available.

counter/timer A circuit that counts external pulses or clock pulses (timing), such as the Intel 8254 device.

coupling	The manner in which a signal is connected from one location to another.
crosstalk	An unwanted signal on one channel due to an input on a different channel.
current drive capability	The amount of current a digital or analog output channel can source or sink while still operating within voltage range specifications.
current sinking	The ability of a DAQ card to dissipate power from an output signal, either analog or digital. Some sensors apply a voltage to a loop, and the DAQ card must be able to accept the resulting current flow.
current sourcing	The ability of a DAQ card to supply current for analog or digital output signals.
CV clock	The Conversion Clock, also known as the Pacer clock, it triggers individual acquisitions and thus tells the A/D how fast to digitize successive samples.

D

D/A	Digital-to-analog, digital/analog
DAC	Digital-to-Analog Converter, an integrated circuit that converts a digital value into a corresponding analog voltage or current.
DAC conversion Start	Signal used to start the process of converting a digital value to an analog output. The source of this signal can be either an internal synchronous clock or an external asynchronous signal.
DAQ	Data Acquisition:

	(1) Collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures, and moving them to a computer for processing; (2) Collecting and measuring the same kinds of electrical signals with A/D or DIO boards plugged into a PC, and possibly generating control signals with D/A or DIO boards in the same PC.
dB	Decibel, the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = $20\log_{10}(V1/V2)$ for signals in volts.
differential input	An analog-input configuration that measures the difference between signals on two terminals, both of which are isolated from computer ground.
DIO	Digital input/output.
DLL	Dynamic Link Library, a software module in Microsoft Windows containing executable code and data that can be called or used by Windows applications or other DLLs. Functions and data in a DLL are loaded and linked at run time when they are referenced by a Windows application or other DLLs.
DNL	Differential nonlinearity, a measure in LSBs of the worst-case deviation of code widths from their ideal value of 1 LSB.
DMA	Direct Memory Access, a method of transferring data to/from computer memory from/to a device or memory on the bus, taking place while the host processor does something else. DMA is the fastest method of transferring data to/from computer memory.

drivers	Software that controls a specific hardware device such as a DAQ board.
DSP	Digital signal processing.
dual-access memory	Memory that can be sequentially accessed by more than one controller or processor but not simultaneously. Also known as shared memory.
dual-port memory	Memory that can be simultaneously accessed by more than one controller or processor.
dynamic range	The ratio, normally expressed in dB, of the largest signal level in a circuit to the smallest signal level. In DAQ cards it typically refers to the range of signals a board can handle or the amount of noise it suppresses.

E

EEPROM	Electrically Erasable Programmable Read-Only Memory, a nonvolatile memory device you can repeatedly program for storage, erase and reprogram.
encoder	A device that converts linear or rotary displacement into digital or pulse signals. The most popular type of encoder is the optical encoder.
EPROM	Erasable Programmable Read-Only Memory: A nonvolatile memory device that can be erased (usually by ultraviolet light exposure) and reprogrammed.
ESSI	All DSP56300 devices contain two independent and identical Enhanced Synchronous Serial Interfaces, ESSI0 and ESSI1. Its maximum frequency is the

	speed of the DSP core divided by four, and thus on most PowerDAQ cards 16.5 MHz.
event	A signal or interrupt generated by a device to notify another device of an asynchronous event. The contents of events are device-dependent.
event-based mode	A board operating mode whereby it notifies the user application of certain predefined subsystem events using Win32 calls. It allows you to write asynchronous applications.
external trigger	A voltage pulse from an external source that triggers an event such as an A/D conversion.
F	
FIFO	First-In First-Out, usually used in reference to a memory buffer where the first data stored is the first sent out.
Firmware Simultaneous Update	A method for multichannel updates, when every channel holds its value when new data is written and all channels are updated at the same time when data is written to the specific channel/channels.
fixed point	A format for processing or storing numbers as digital integers. In fixed-point arithmetic all numbers are represented by integers, fractions (usually restricted between ±1.0) or a combination of both integers and fractions. Thus integer mathematics can be implemented on all general-purpose processors.

floating point Representing data as a combination of a mantissa and an exponent. The mantissa is usually described by a signed fractional value that has a magnitude >= 1.0 and restricted to< 2.0. The exponent, instead, is an integer and represents the number of places any binary number must be shifted, left or right, in order to yield the desired value.

frame A user-defined number of scans, and these datapoints reside in a predefined portion of a buffer in host-memory. This host-memory buffer is also known as the Advanced Circular Buffer (ACB).

function A set of software instructions executed by a single line of code that may have input and/or output parameters and returns a value when executed.

G

gain The factor by which a signal is amplified, sometimes expressed in dB.

gain accuracy A measure of the deviation of an amplifier's gain from the ideal gain.

GUI Graphical User Interface, an intuitive means of communicating information to and from a computer program by means of graphical screen displays. GUIs can resemble the front panels of instruments or other objects associated with a computer program.

H

handler A device driver installed as part of the computer's OS.

hardware The physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on.

Hardware Simultaneous Update On AO Series boards, a multichannel update mode whereby when you preprogram the AO logic to update all DACs upon a write to a certain DAC.

High Density Family (HDF) Applies to AO Series boards; models with 96 D/A outputs.

I

IMD Intermodulation Distortion, the ratio, in dB, of the total RMS signal level of harmonic sum and difference distortion products, to the overall RMS signal level. The test signal consists of two sinewaves added together.

INL Integral Nonlinearity, a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry.

input bias current The current that flows into the inputs of a circuit.

input impedance The measured resistance and impedance between the input terminals of a circuit.

input offset current The difference in the input bias currents of the two inputs of an instrumentation amplifier.

instrumentation amplifier A circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two inputs.

integral control — A control action that eliminates the offset inherent in proportional control.

integrating A/D — An A/D whose output code represents the average value of the input voltage over a given time interval.

interrupt — A computer signal indicating that the CPU should suspend its current task to service a designated activity.

I/O — Input/Output, the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data-acquisition and control interfaces.

IPC — Interprocess Communication, protocol by which processes can pass messages. Messages can be either blocks of data and information packets, or instructions and requests for process(es) to perform actions. A process can send messages to itself, other processes on the same machine, or processes located anywhere on the network.

isolation voltage — The voltage that an isolated circuit can normally withstand, usually specified from input to input and/ or from any input to the amplifier output, or to the computer bus.

K

k — kilo, the standard metric prefix for 1000 or 10^3, used with units of measure such as volts, Hertz, and meters.

L

linearity	The adherence of device response to the equation R = KS, where R = response, S = stimulus, and K is a constant.
LSB	Least-significant bit.

M

M	mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and Hertz; the prefix for 1,048,576, or 2^{20}, when used to quantify data or computer memory.
Mbytes/s	A unit for data transfer that means 1 million or 10^6 bytes/sec.
MMI	Man-machine interface, the means by which an operator interacts with an industrial automation system; often called a GUI.
multiplexer	A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.
multitasking	A property of an operating system in which several processes can run simultaneously.
mux	see multiplexer

N

noise	An undesirable electrical signal. Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters as well as internal sources such as semiconductors, resistors and capacitors.
O	
OLE	Object Linking and Embedding, a set of system services that provides a means for applications to interact and interoperate. Based on the underlying Component Object Model, OLE is object-enabling system software. Through OLE Automation, an application can dynamically identify and use the services of other applications. OLE also makes it possible to create compound documents consisting of multiple sources of information from different applications.
OLE controls	see ActiveX controls.
operating system	Base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices.
optical isolation	The technique of using an optoelectronic transmitter and receiver to transfer data without electrical continuity to eliminate high potential differences and transients.
OS	see operating system

output settling time	The amount of time required for the analog output voltage of an amplifier to reach its final value within specified limits.
output slew rate	The rate of change of an analog output voltage from one level to another.
overhead	The amount of computer processing resources, such as time or memory, required to accomplish a task.
P	
paging	A technique used for extending the address range of a device to point into a larger address space
PCI	Peripheral Component Interconnect, an expansion bus architecture originally developed by Intel to replace ISA and EISA. It offers a theoretical maximum transfer rate of 132M bytes/sec.
PDXI	PowerDAQ eXtensions for Instrumentation, UEI's implementation of the PXI bus standard.
PGA	see Programmable-gain amplifier
PID control	A 3-term control algorithm combining proportional, integral and derivative control actions.
pipeline	A high-performance processor structure in which the completion of an instruction is broken into its elements so that several elements can be processed simultaneously from different instructions.
PLC	Programmable logic controller, a special-purpose computer used in industrial monitoring and control applications. PLCs typically have proprietary programming and networking protocols and special-purpose digital and analog I/O ports.

Polled mode	DAQ card operating mode whereby the user application queries the board about the status of various subsystems as needed.
port	A communications connection on a computer or a remote controller.
postriggering	The technique used on a DAQ card to acquire a programmed number of samples after trigger conditions are met.
potentiometer	An electrical device whose resistance you can manually adjusted; known among engineers as a "pot."
pretriggering	The technique used on a DAQ card to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition.
programmable-gain amplifier	also see PGA, an amplifier where you can change the amount of gain applied to the inputs. Gain settings today are usually made with software instead of setting jumpers as was necessary with first-generation DAQ boards.
programmed I/O	The standard method a CPU uses to access an I/O device—each byte of data is read or written by the CPU.
propagation delay	The amount of time required for a signal to pass through a circuit.
proportional control	A control action whose output is proportional to the deviation of the controlled variable from a desired setpoint.

protocol The exact sequence of bits, characters and control codes used to transfer data between computers and peripherals through a communications channel.

pseudodifferential An analog-input configuration where all channels refer their inputs to a common ground—but this ground is not connected to the computer ground.

PXI PCI eXtensions for Instrumentation, a bus standard that combines the mechanical form factor of the CompactPCI specification and the electrical aspects of the PCI bus. It also adds integrated timing and triggering designed specifically for measurement and automation applications.

Q

quantization error The inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process.

R

real time A system in which the desired action takes place immediately when all input conditions are fulfilled; it never has to wait for other processes to complete before it can start. In DAQ terms, it generally refers to the processing of data as it is acquired instead of being accumulated and getting processed at a later time.

relative accuracy A measure in LSB of the accuracy of an A/D. It includes all nonlinearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.

resolution The smallest signal increment that a measurement system can detect. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has a resolution equal to 12 bits = one part in 4,096 = 0.0244% of full scale.

resource locking A technique whereby a device is signaled not to use one of its resources, often local memory, while that resource is being used by another device, generally the system bus.

ribbon cable A flat cable in which conductors are placed side by side.

RMS Root-mean square, computed by squaring the instantaneous voltage, integrating over the desired time and taking the square root.

RTD Resistance temperature detectors operate based on the principle that electrical resistance varies with temperature. They generally use pure metal elements, platinum being the most widely specified RTD element type although nickel, copper, and Balco (nickel-iron) alloys are also used. Platinum is popular due to its wide temperature range, accuracy, stability as well as the degree of standardization among manufacturers. RTDs are characterized by a linear positive change in resistance with respect to temperature. They exhibit the most linear signal over temperature of any electronic sensing device

RTSI Real Time Systems Integration bus, developed by National Instruments, this intercard bus allows you to transfer data and control signals without using the backplane bus.

S

sample	16-bit binary data that should be converted to the voltage
samples/sec	expresses the rate at which a DAQ board digitizes an analog signal.
scan	one run through the presently configured Channel List
SDK	Software developer's kit, a collection of drivers and utilities that allow engineers to write their own application programs.
SE	see single-ended.
self-calibrating	reference to a DAQ board that calibrates its own A/D and D/A circuits with a reference source, sometimes provided internally with a precision D/A converter.
sensor	A device that generates an electrical signal in response to a physical stimulus (such as heat, light, sound, pressure, motion or flow).
Sequential Update mode	Performs multi channel updates where every write to the analog-output channel immediately leads to a change in the output voltage.
S/H	Sample/Hold, a circuit that acquires and stores an analog voltage on a capacitor for a short period of time.
simultaneous sampling	the act of digitizing multiple channels simultaneously, with interchannel skew often being measured in psec.

Simultaneous update mode On AO Series boards, this mode (also referred to as Update All) all channels previously written to in the Write&Hold mode update their outputs at the same time.

single-ended a term used to describe an analog-input configuration where you measure each channel with respect to a common analog ground.

Single-Point Update mode In an AO Series board, performs an independent update of any available DACs.

Slow Bit a control bit in the analog-input configuration word that instructs the A/D to wait a short while before actually digitizing the input voltage; it gives the input amplifier time to settle, and is very useful when working with very high gains.

SNR also S/N ratio or Signal/Noise ratio, the ratio of the peak power level to the remaining noise power, expressed in dB.

software trigger A programmed event that triggers an event such as a data acquisition.

SPDT Single-pole double-throw, a switch in which one terminal can be connected to one of two other terminals.

SSH Simultaneous Sample/Hold, see simultaneous sampling

S/s, S/sec see samples/sec

strain gage A sensor that converts mechanical motion into an electronic signal. A change in capacitance, inductance or resistance is proportional to the strain experienced by the sensor, but resistance is the most

	widely used characteristic that varies in proportion to strain.
Standard Density Family (SDF)	Applies to AO Series boards; all models with from 8 to 32 D/A outputs.
subroutine	A set of software instructions executed by a single line of code that may have input and/or output parameters.
subsystem	On PowerDAQ cards, a group of circuits that perform either analog input, analog output, digital input, digital output or counter/timer functions.
successive-approximation A/D	An A/D that sequentially compares a series of binary-weighted values with an analog input to produce an output digital word in n steps, where n is the A/D's resolution in bits.
synchronous	A property of a function that begins an operation and returns only when the operation is complete.
system noise	A measure of the amount of noise seen by an analog circuit or an A/D when the analog inputs are grounded.
T	
TCP/IP	Transmission Control Protocol/Internet Protocol, the basic multi-layer communication protocol of the Internet but that is also used in a private network (either an intranet or an extranet). The higher layer, TCP, manages the assembling of a message or file into smaller packets that are transmitted and received by a TCP layer that reassembles the packets into the original message. IP handles the

	address portion of each packet so it gets to the right destination.
THD	Total harmonic distortion, the ratio of the total RMS signal due to harmonic distortion to the overall RMS signal, expressed in dB or percent.
THD+N	The percentage of Total Harmonic Distortion + Noise (THD+N) of a sine wave equals 100 times the ratio of the RMS voltage measured with the fundamental component of a sine wave removed by a notch filter, to the RMS voltage of the fundamental component.
thermistor	A temperature-sensing element that exhibits a large change in resistance proportional to a small change in temperature. Thermistors usually have negative temperature coefficients. They tend to be more accurate than thermocouples or RTDs, but they have a much more limited temperature range.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of temperature.
throughput rate	The flow of data, measured in bytes/sec, for a given continuous operation.
transducer	A device that converts energy from one form to another. Generally applied to devices that convert a physical phenomenon (such as pressure, temperature, humidity, or flow) to an electrical signal.
transfer rate	The rate, measured in bytes/sec, at which data is moved from a source to a destination after software

	initialization and setup operations; the maximum rate at which the hardware can operate.
Trigger	A signal, in either hardware or software, that initiates or halts a process. In DAQ boards, it generally refers to a signal that starts or stops an A/D, D/A or DIO operation.
U	
UCT	User counter/timer
unipolar	A signal range that is always positive (e.g. 0 to 10 V).
Update All	Applicable to AO Series boards; see Simultaneous Update mode
W	
Write&Hold mode	On AO Series boards, a mode whereby data is written to the output register but the output voltage remains unchanged and stays at the previous update value.
Z	
zero offset	The difference between true zero and an indication given by a measuring instrument.
zero-overhead looping	The ability of a high-performance processor to repeat instructions without requiring time to branch to the beginning of the instructions.
zero-wait-state memory	Memory fast enough that the processor does not have to wait during any reads and writes to the memory.

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