nuvoTon

User Manual

NUC740 Evaluation Board
User Manual

.

For additional information or questions, please contact:Nuvoton Electronics Corp.

1 Revision history

version	date	page	description
A	May 13, 2003	-	Initial Issued
A1	Sep 3,2008	-	Update
B	Apr 6,2009	-	Change part number to NUC740

2 General Description

The evaluation board is a test platform that is suitable for the sample of NUC740. The board include the powerful 16/32-bit ARM® based RISC micro-controller (NUC740), USB function, memory, PCMCIA function, power control system, LAN and WAN Ethernet port. This allows us to test and debug all NUC740CD function.

This document shows the system-based hardware design. We would describe the jumper function, selectable function and how to connect with the NUC740 in detail.

3 Features

- NUC740: 16/32-bit ARM7TDMI® RISC micro-controller
- Boot ROM and AP flash-- 2M*16 bits for expansion.
- SDRAM: One 512*4 banks*32 M bits SDRAM
- External I/O: PCMCIA application (Wireless LAN)
- General I/O: control signal, UART or 2nd USB, show status (LEDs)
- USB: USB function
- LAN and WAN 10/100M Ethernet interface
- Embedded ICE™ Interface
- Expansion Function: one port WAN and 4 ports LAN.

4 The Function Blocks

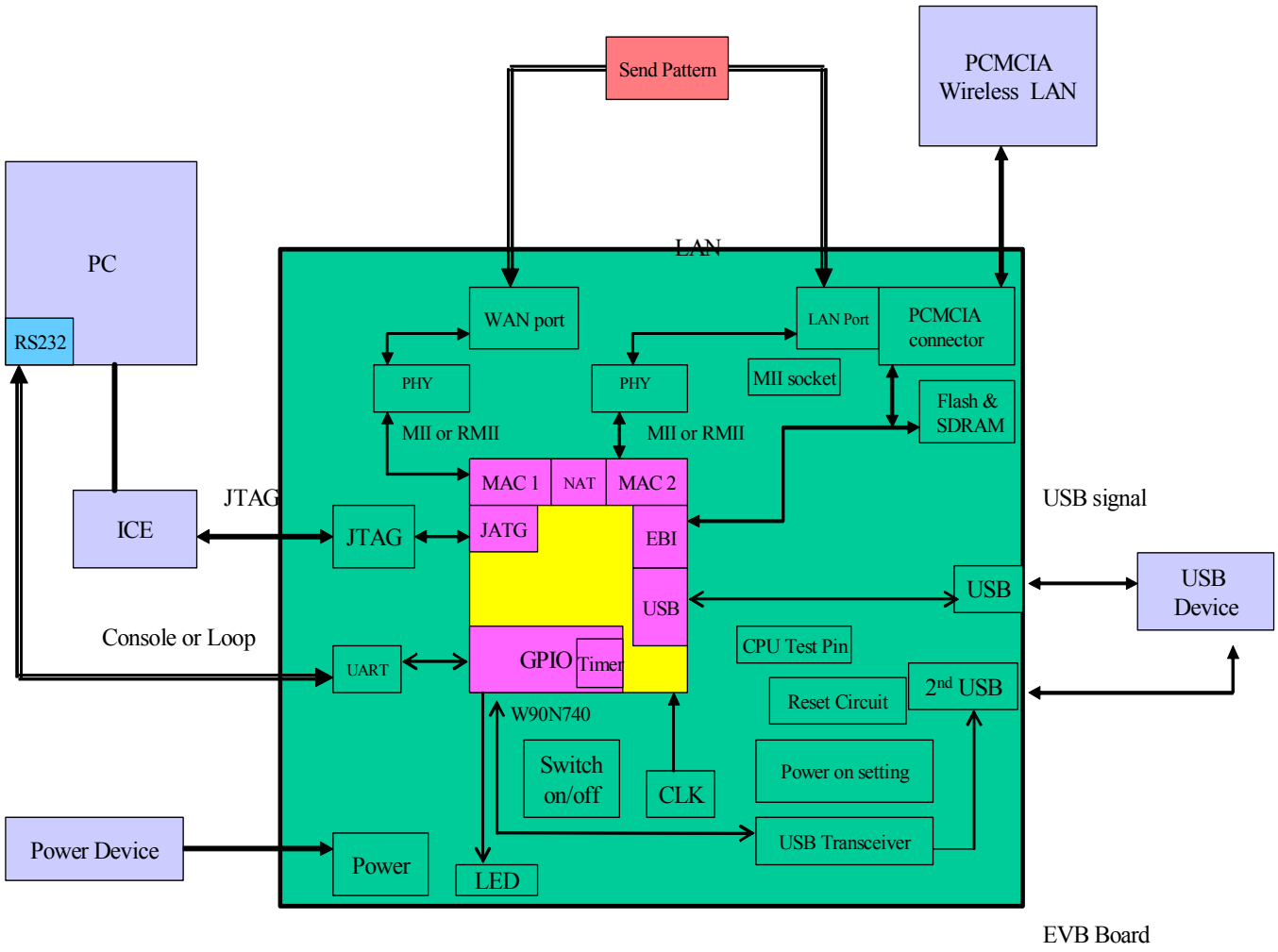


Fig 1 The Function Block of Evaluation Board

4.1 CPU: NUC740

NUC740 is our protagonist. That is for her what we do every thing. The NUC740 is using ARM7TDMI® core inside. It is a low power, general-purpose integrated circuits. The NUC740 offers an 8K-byte I-cache/SRAM, a 2K-byte D-cache/SRAM and two MACs of Ethernet controller that reduces total system cost. An NAT Accelerator is support to reduce the software loading for network address translation processing.

We support 15MHZ frequency for CPU. In the PCBA, that would have test point for every one pin. The

others that we do use power regulator support the power of the NUC740.

4.2 Flash and SDRAM

We put boot room, flash and SDRAM on the evaluation board. The boot room sizes are 1 piece 256K*8 bits, PLCC package. They are using the ROM bank. We would put the other flash for application program. The sizes could be 2M*16 or 1M*16 bytes or 0.5M*16 bytes, TSOP package, which used the external I/O bank. The SDRAM has one piece and sizes are 2M*32 bytes.

4.3 PCMCIA connector

We support one PCMCIA 16-bits PC Card socket. The main goal destination is which can connects with wireless LAN card. It is using the external memory interface of CPU. We would use bank two and high address, A23, to control I/O or attribute access.

4.4 PHY, WAN port and LAN port

This is main function that do broadband gateway. We choose one port PHY IC of DM9161 of the DAVICOM. It supports MII mode and RMII mode. We made connect WAN port and LAN port on board or it can connect with an external wire. The function block would show some connect status LED.

We have an extension function, one MII socket. That is for used the daughter board to extension 4 ports switch output.

4.5 JTAG.

We used it to connect to CPU with ICE. It's debug tool.

4.6 UART, 2nd USB and LED

Those functions are creating by the programmable I/O ports of CPU. The UART and 2nd USB are optional functions. We used switch to select it. The UART can do console connection or RS232 full function connector. The 2nd USB needs a transceiver or external USB transceiver connects to USB device.

The LED function is showing the power on or power off mode.

4.7 USB

We have one USB host controller. It is USB 1.1 compliant specification. On the evaluation board, that we would have one power-switch IC. This IC can output current typically limited to 0.85A below the 5A safety requirement.

4.8 Power on setting

After power on reset, there are four Power-On setting pins to configure NUC740 system configuration. We must set the next function:

- D15 pin： Internal System Clock Select
- D14 pin： Big / Little Endian Mode Select
- D [13:12] ： Boot ROM/FLASH Data Bus Width
- D [11:10] ： Test Chip Configuration
- D [9:8] ： Package Type Select

We would have eight groups jumper setting to do it. On section 5.1 have more improve description.

4.9 Reset schematic

We put one schematic on the board. It use reset IC schematic that make sure reset timer is fine. The other things that on board device-reset function would have two choices to do reset function. One is that device has reset schematic on itself side. The other one is which be control by the GPIO of the CPU.

We use a keypad for system reset. The push bottom must functional when system is shutdown.

4.10 Power

5V, 3.3V and 1.8V are we needed power. We used external DC 5V adapter supply the board power and used linear regulator change from 5V voltage to the 3.3V voltage and change from 3.3V voltage to 1.8V voltage. We put the 5 linear regulators support CPU power, VDD18, VDD33, USBVDD, DVDD18, AVDD18, that destination is measure the CPU current.

5 Circuit Block Description and Jumper Setting

The circuit block has 7 parts.

1. MCU
2. Power Block
3. Memory Block
4. PCMCIA Function Block
5. LAN Block
6. WAN Block
7. USB Function Block

The Circuit blocks are shown in FIGURE 2.

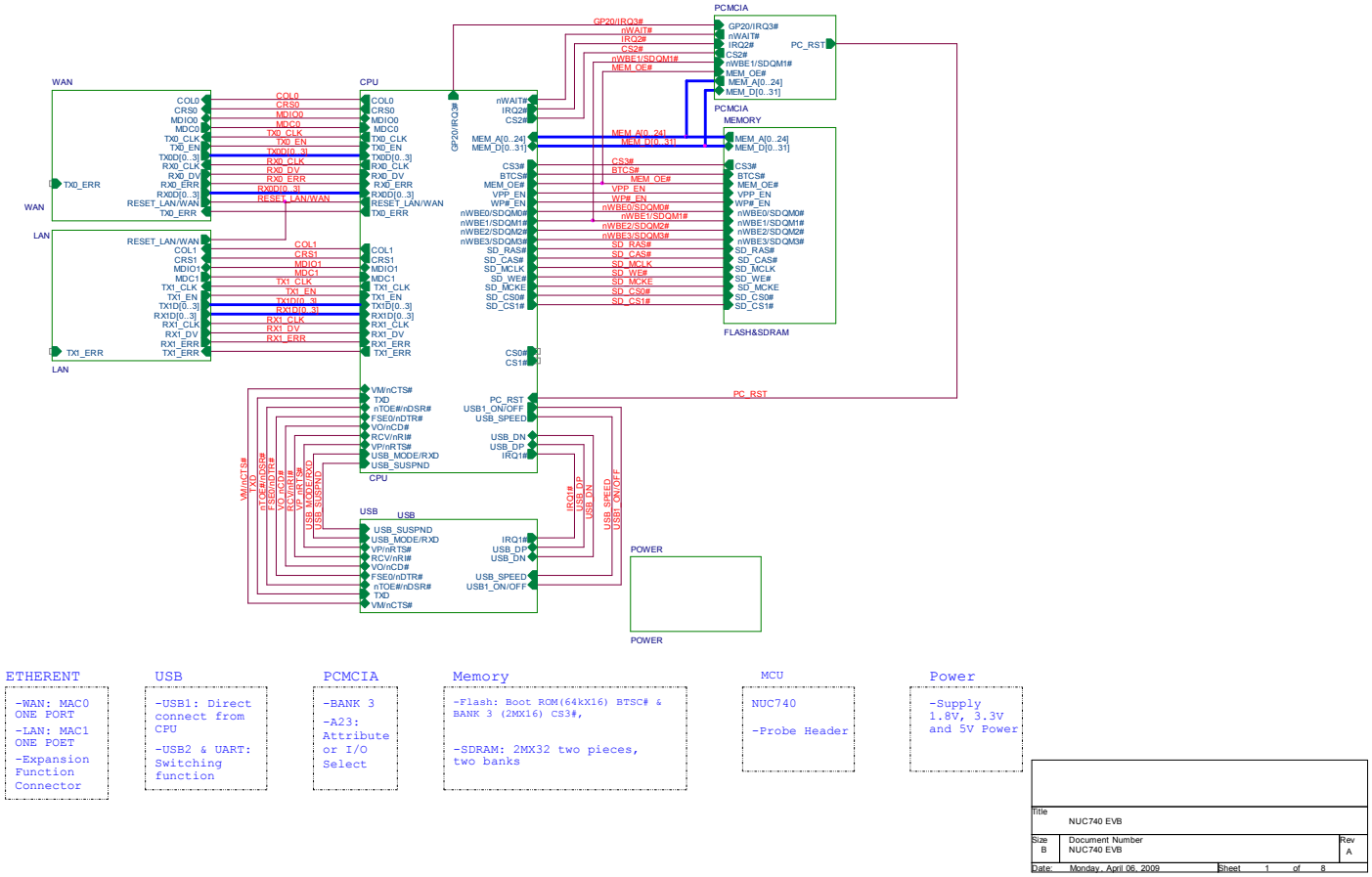


FIGURE 2: Circuit Function Block

5.1 MCU

The MCU Block consists of 8/16/32 bits RISC controller NUC740, clock generator, reset circuit, display LED, boot up setting and muti-ice connector.

- The 8/16/32 bits CPU NUC740 is our production. We have connector that is the same pin with NUC740 for easy debugging.
- The 15MHZ crystal is must mount on the board.

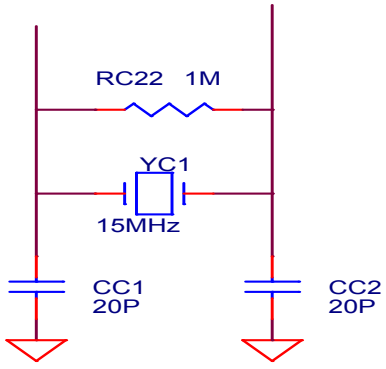


FIGURE.3: Clock Generator

- We used the MIC811 reset IC that make sure reset time more than 240ms. The function of the device is to assert a reset if either the power supply drops below a designated reset threshold level or MR# is forced low. This function take more ensure for system. The other thing is that have a buffer to make sure reset signal fan out is enough. We used a "and" gate to association reset signal come from JTAG and MIC811 (Reset IC).

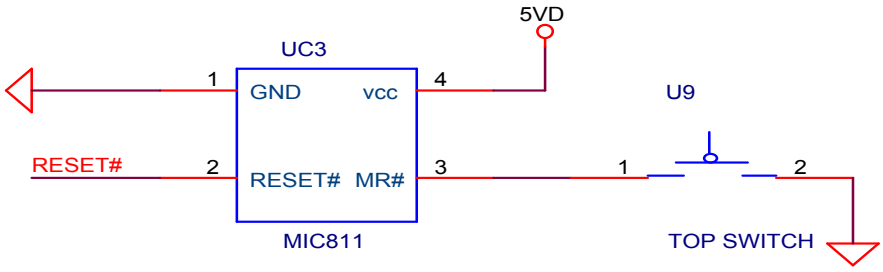


FIGURE 4: Reset schematic

- We have expansion function is show the status by 7 LEDs that control by GPIO of the NUC740CD. They are GPIO0, GPIO1, GPIO2, GPIO3, GPIO15 and GPIO16.

Function	EBI Test	GDMA Test	Cache On/Off	APB module	MAC & NAT	USB test
GPIO	GPIO 0	GPIO 1	GPIO 2	GPIO 3	GPIO 15	GPIO 16
Signal Name	LMD0	LMD1	LMD2	LMD3	E0	E1

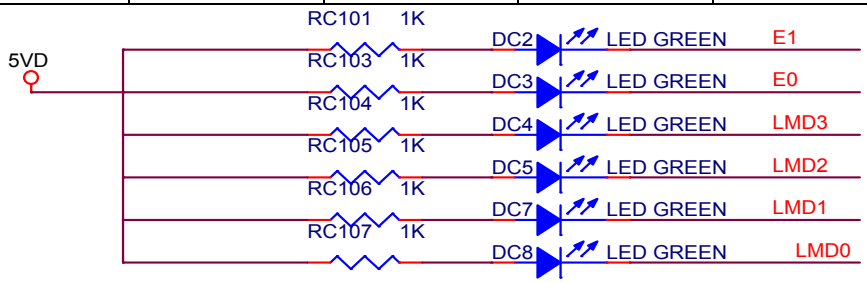
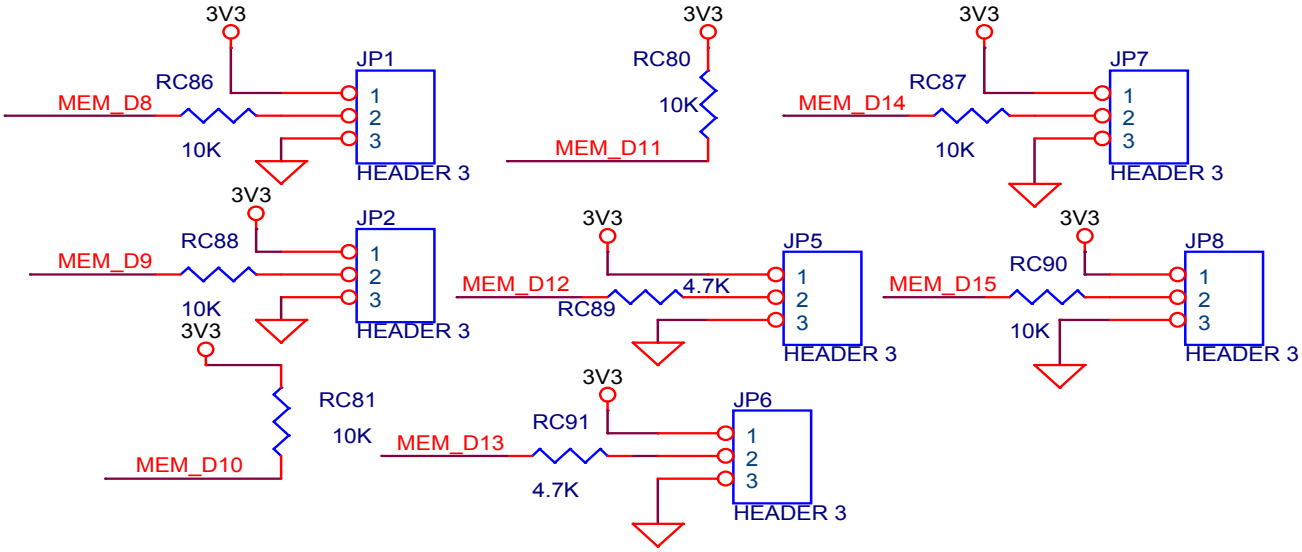


FIGURE 5: Status LED

- The power on setting that we follow next table.

Power-On Setting	Pin
Internal System Clock Select	D15 (JP8)
Little/Big Endian Mode Select	D14 (JP7)
Boot ROM/FLASH Data Bus Width	D [13:12] (JP6, JP5)
Test Chip ConFiguration	D [11:10] Fixed
Package Type Select	D [9:8] (JP2, JP1)

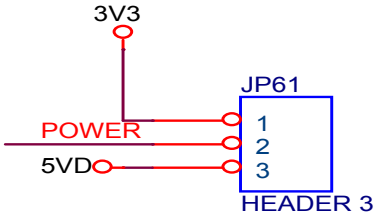



```
JP8: LO--external clock from EXTAL pin is served as internal system clock
JP8: HI-- PLL output clock is used as internal system clock
JP7: HI--the external memory format is Little Endian mode
JP7: LO--the external memory format is Big Endian mode
```

JP6	JP5	BUS WIDTH	JP2	JP1	PACKAGE
LO	LO	8 BITS	LO	LO	RESERVED
LO	HI	16 BITS	LO	HI	128 PINS
HI	LO	32 BITS	HI	LO	160 PINS
HI	HI	RESERVED	HI	HI	176 PINS

FIGURE 6: Power on setting

- JTAG interface: We put two kinds JTAG connector for ICE. In which one has 20 pins and the other has 14 pins. JP61 decide the JATG power is 3.3V or 5V.



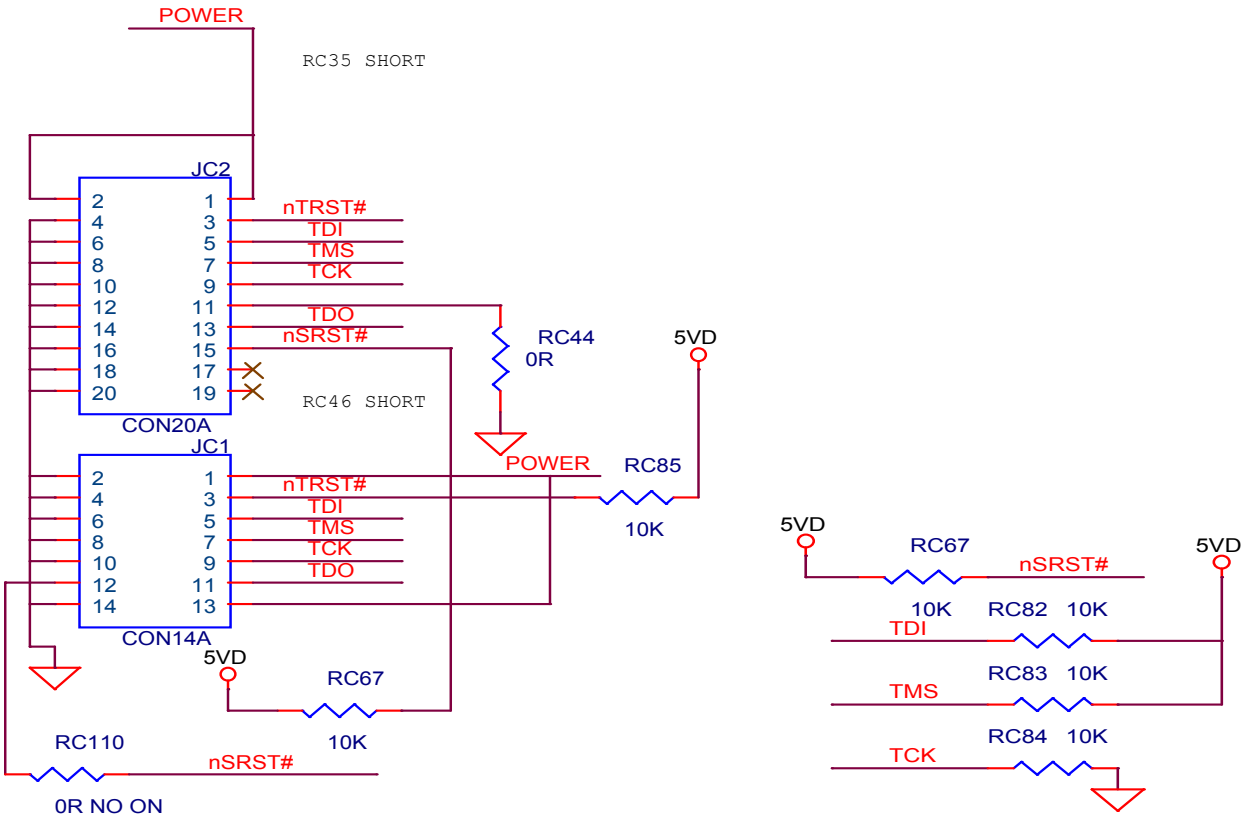


Figure 8: JTAG Connector

5.2 Power

We used 5V 3A adapter for the evaluation board. We planned use 2 pieces of 1A current regulator change voltage from 5V to 3.3V. One supports the peripheral power that are PHY and memory. The other one only support to NUC740. The CPU core power is come from 1.8V regulator. We used the inductor to separator the analog and digital power. We put the fuse on the voltage input side for measure the current of NUC740. We had put a switch on the power input line that can let the power shut down and did not DC 5V on the PCBA.

If LAN port needs supply four ports. The 2.5V power would come from the other 2.5V regulator. The Power flow chart was show in FIGURE 8.

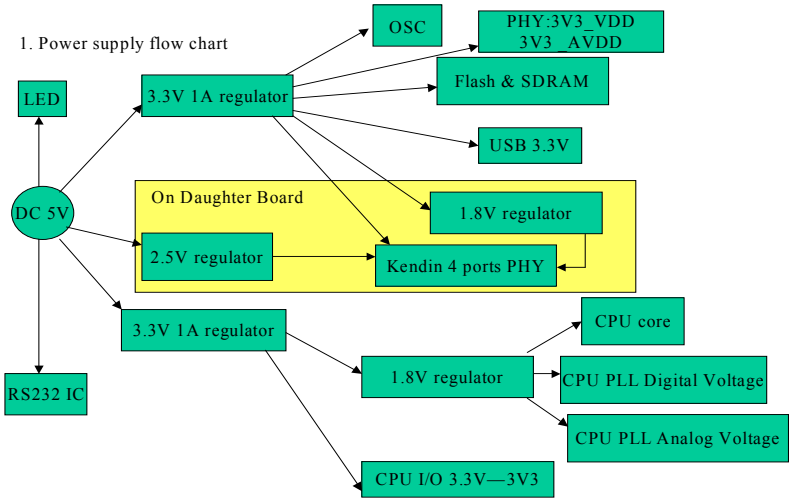
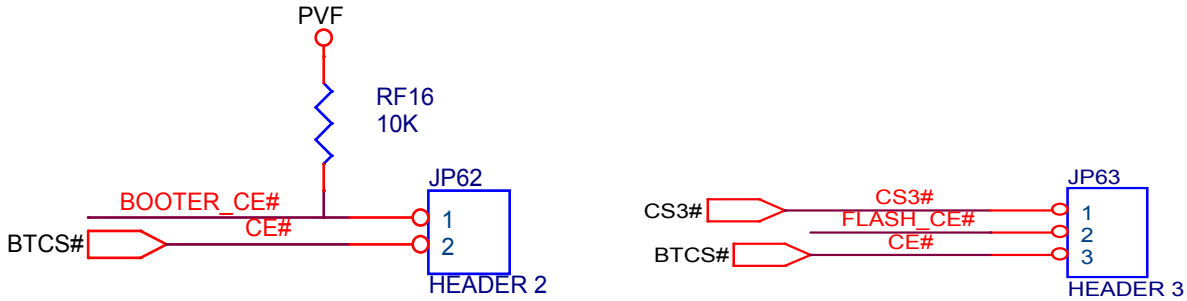


FIGURE.8: Power flow chart

5.3 Memory Block

The memory block includes three parts: 128k*8 boot ROM, 2M*16 bits for application program and 512*4*32 M bits SDRAM.

The UF1 is 128k*8 boot ROM. The JP62 must short pin1 and pin 2. The JP63 must short pin1 and pin2 for UF2 that saved the application program. When the user uses the UF2 flash memory connects to boot rom bank that JP62 must open and JP63 must short pin 2,3. When you do this change that you must take care the boot room type.



SDRAM size is 512*4 Banks*32 bits. We use the Nuvoton solution W986432DH. We connect with SDRAM follow rule of the FIGURE 8.

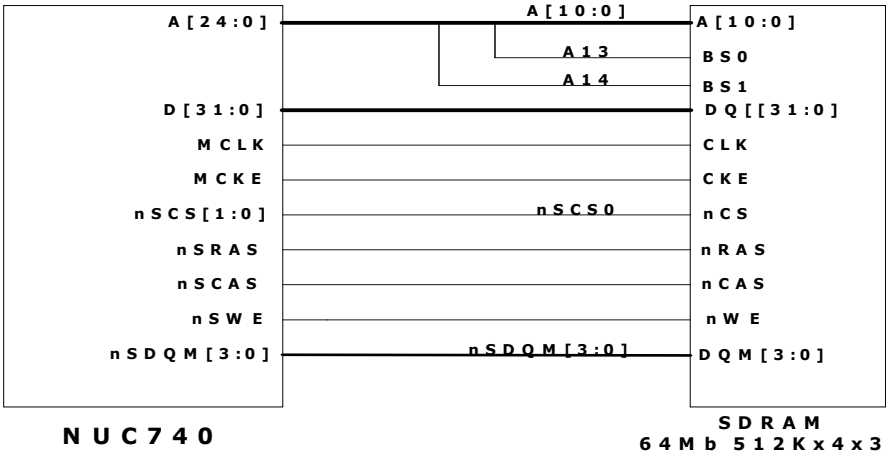


FIGURE 8: SDRAM Interface

5.4 PCMCIA Function Block

The PCMCIA function is using one bank of the external memory that is the bank 2. We select I/O and attribute memory Read/Write by address A23. When A23 is 'High' state that memory is access I/O memory. If A23 is 'Low' state that memory is access attribute memory. The PCMCIA function block is used the external bank 2. The CS2# signal must connect with PCMCIA connector. The REG signal control by GPIO20/IRQ3#. The PCMCIA power depends on LI1, LI2, LI3 and LI4. If thePCBA are mounted the LI1 and LI2. The power is 5V. Otherwise, the PCBA are mounted the LI3 and LI4 that the power is 3.3V.

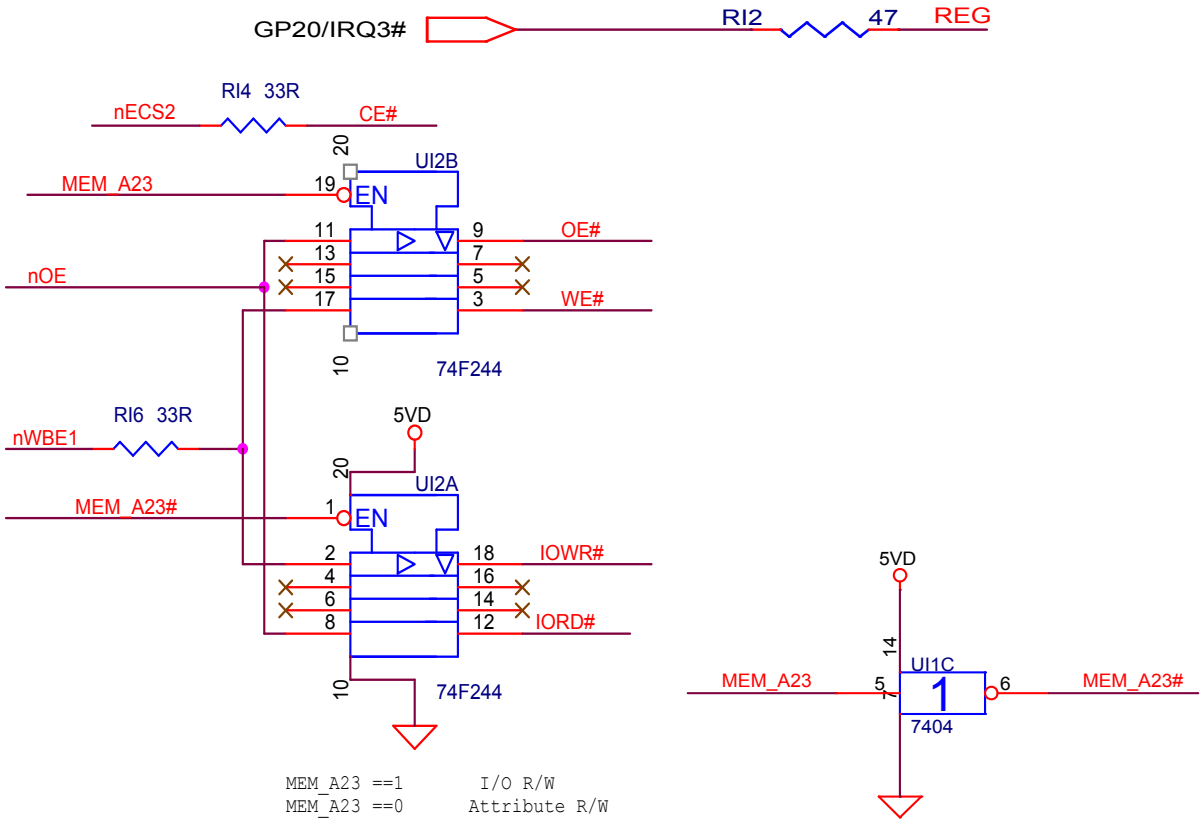


FIGURE 9: PCMCIA bank selector

The PCMCIA signals “VS1, VS2” can select “HI” or “LOW” by the JP64 and JP65

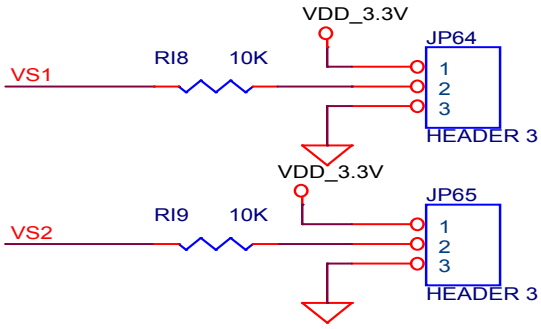


Figure 10 VS1 and VS2 jump selector

5.5 LAN & WAN Function Blocks

In LAN and WAN block that we used 10/100 physical layer IC DM9161 of the DAVICOM. It can support MII and RMII mode.

We let reset signal come from two schematic. One connects to reset system. The other is local RC reset schematic. Which one used depends by system design. They (JP16, JP36) show on the FIGURE 11.

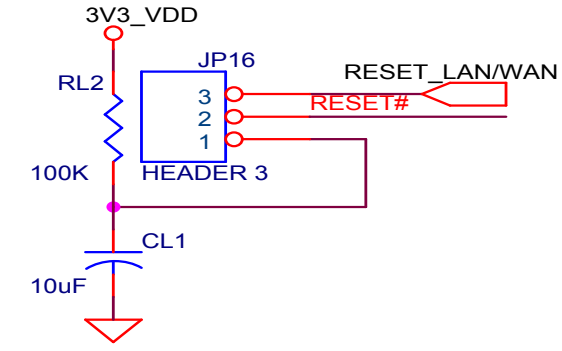


FIGURE 11: Reset Schematic

The LAN clock is come from two kind parts too. They are crystal and OSC. The FIGURE 12 is their schematic.

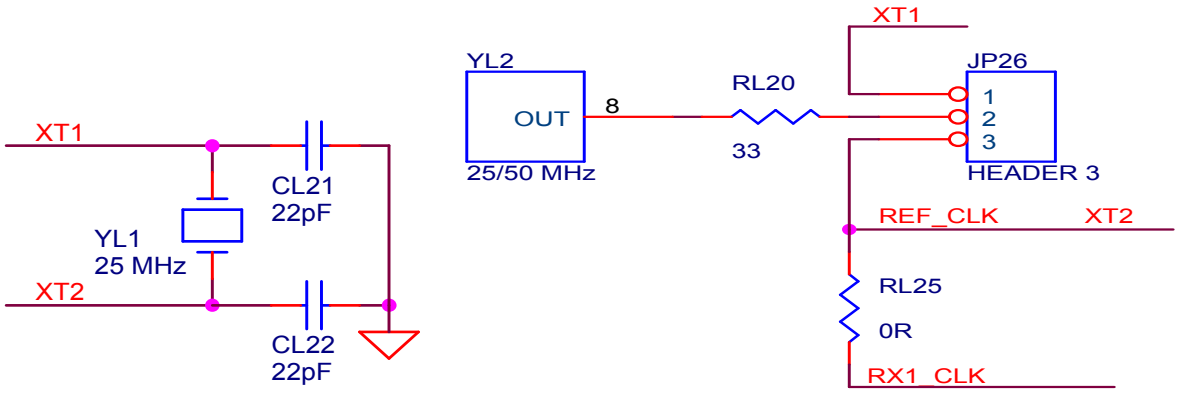


FIGURE 12: LAN Clock generator

In order to make sure that expand function work well. We control on/off MII signal with the switch—SW1, SW2, SW3 (LAN) and SW4, SW5, SW6 (WAN). We must turn off them, when we test Ethernet expansion function. That can make sure MII signals no influence with others. They show on FIGURE 13

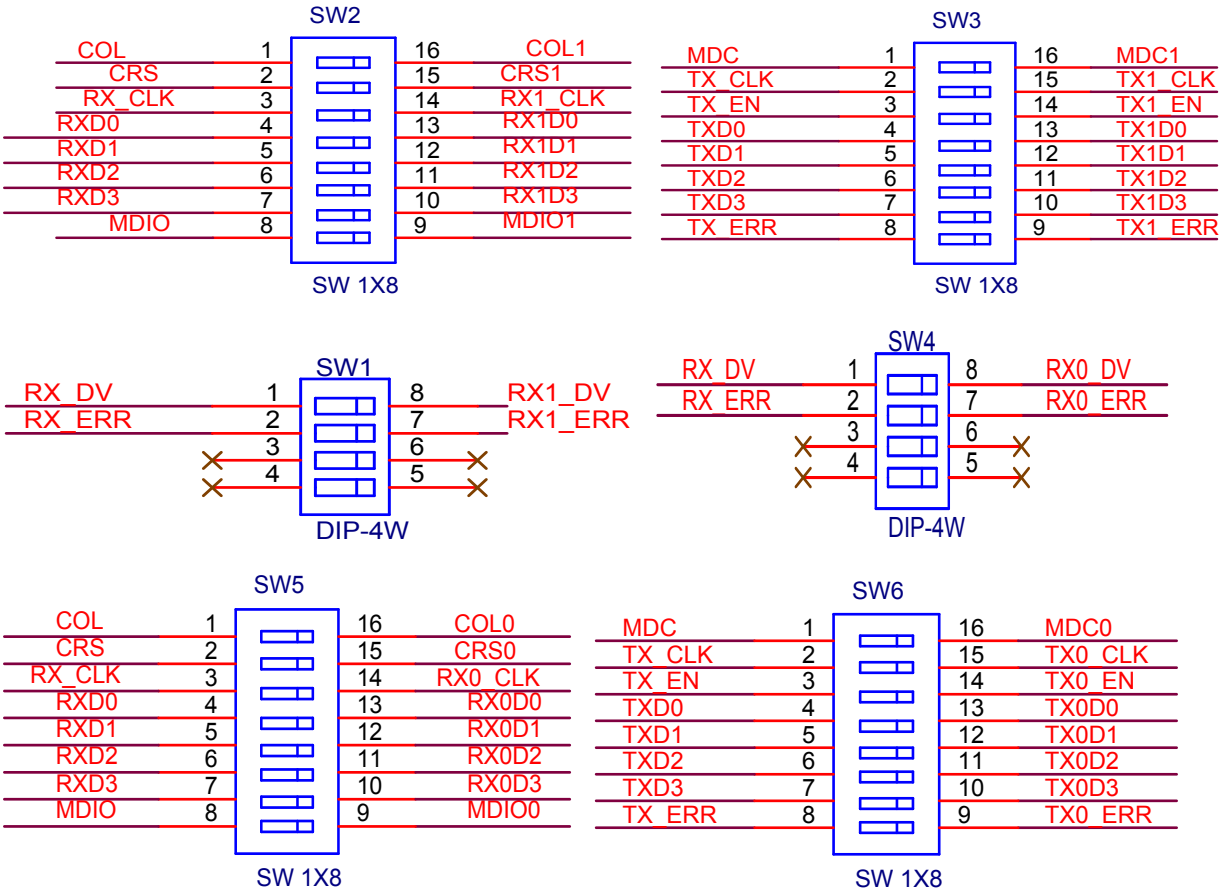


FIGURE 13: LAN and WAN MII Switch

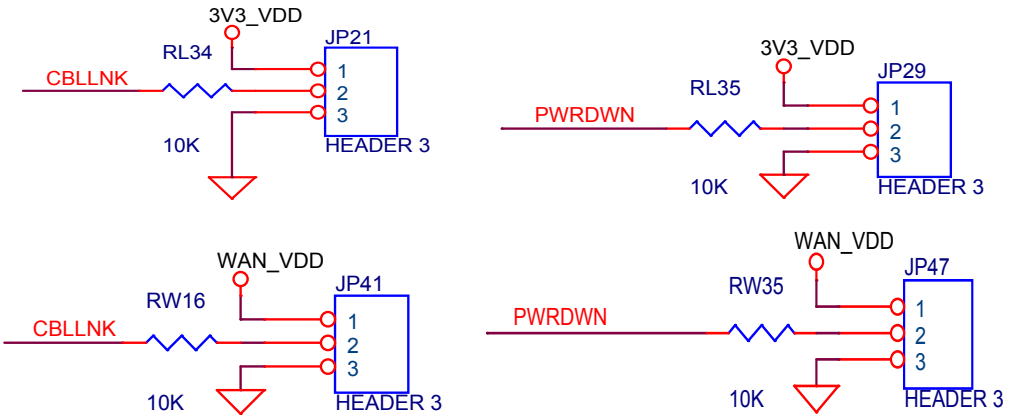
In LAN and WAN blocks that have some power on set functions must setting. They show on the next table and FIGURE 14.

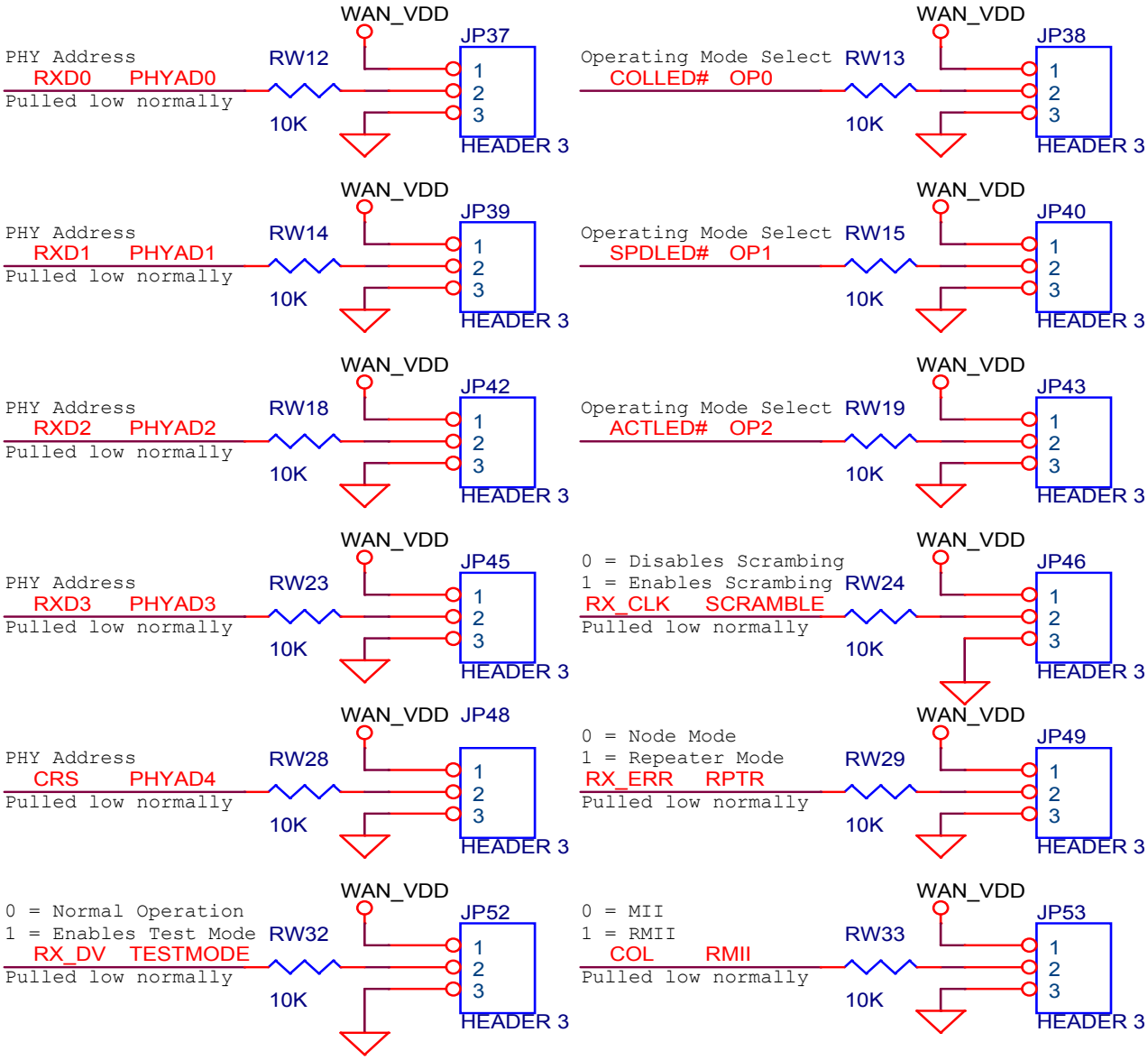
Setting	Hi	Lo	Note
Phy address bit 0	1	0	RX*D0[1]:
Phy address bit 1	1	0	RX*D1
Phy address bit 2	1	0	RX*D2
Phy address bit 3	1	0	RX*D3
Phy address bit 3	1	0	CRS*
Testmode	Normal Option	Test Mode	Rx*_DV
RMII	RMII	MII	COL*
RPTR	Repeater mode	Node mode(default)	RX*_ERR
Scramble	Enable	Disable	RX*_CLK
Cable/Link	Link	Without Link	CBLLNK
Power down mode	Power Down mode	Normal mode	PWRDWN

Note1: *:1 is LAN function block. *: 0 WAN Function Block

OP2	OP1	OP0	Function	Note
0	0	0	Dual speed 100/10 HDX	OP0: COLLED*#
0	0	1	Reserved	OP1: SPDLED*#
0	1	0	Reversved	OP2: ACTLED*#
0	1	1	Manual select 10TX HDX	
1	0	0	Manual select 10TX FDX	
1	0	1	Manual select 100TX HDX	
1	1	0	Manual select 100TX FDX	
1	1	1	Auto negotiation enable with all capabilities	

The LAN setting headers are JP17, JP18, JP19, JP20, JP22, JP23, JP27, JP28, JP30, JP31, JP32, JP33, JP21 and JP29. The WAN setting headers are JP37, JP38, JP39, JP40, JP42, JP43, JP45, JP46, JP48, JP49, JP52 JP53, JP41 and JP47.




WAN_VDD
JP37
PHY Address
RXD0 PHYAD0
Pulled low normally
RW12
10K
1
2
3
HEADER 3
WAN_VDD
JP38
Operating Mode Select
COLLED# OP0
RW13
10K
1
2
3
HEADER 3
WAN_VDD
JP39
PHY Address
RXD1 PHYAD1
Pulled low normally
RW14
10K
1
2
3
HEADER 3
WAN_VDD
JP40
Operating Mode Select
SPDLED# OP1
RW15
10K
1
2
3
HEADER 3
WAN_VDD
JP42
PHY Address
RXD2 PHYAD2
Pulled low normally
RW18
10K
1
2
3
HEADER 3
WAN_VDD
JP43
Operating Mode Select
ACTLED# OP2
RW19
10K
1
2
3
HEADER 3
WAN_VDD
JP45
PHY Address
RXD3 PHYAD3
Pulled low normally
RW23
10K
1
2
3
HEADER 3
WAN_VDD
JP46
0 = Disables Scrambling
1 = Enables Scrambling
RX_CLK SCRAMBLE
Pulled low normally
RW24
10K
1
2
3
HEADER 3
WAN_VDD
JP48
PHY Address
CRS PHYAD4
Pulled low normally
RW28
10K
1
2
3
HEADER 3
WAN_VDD
JP49
0 = Node Mode
1 = Repeater Mode
RX_ERR RPTR
Pulled low normally
RW29
10K
1
2
3
HEADER 3
WAN_VDD
JP52
0 = Normal Operation
1 = Enables Test Mode
RX_DV TESTMODE
Pulled low normally
RW32
10K
1
2
3
HEADER 3
WAN_VDD
JP53
0 = MII
1 = RMII
COL RMII
Pulled low normally
RW33
10K
1
2
3
HEADER 3

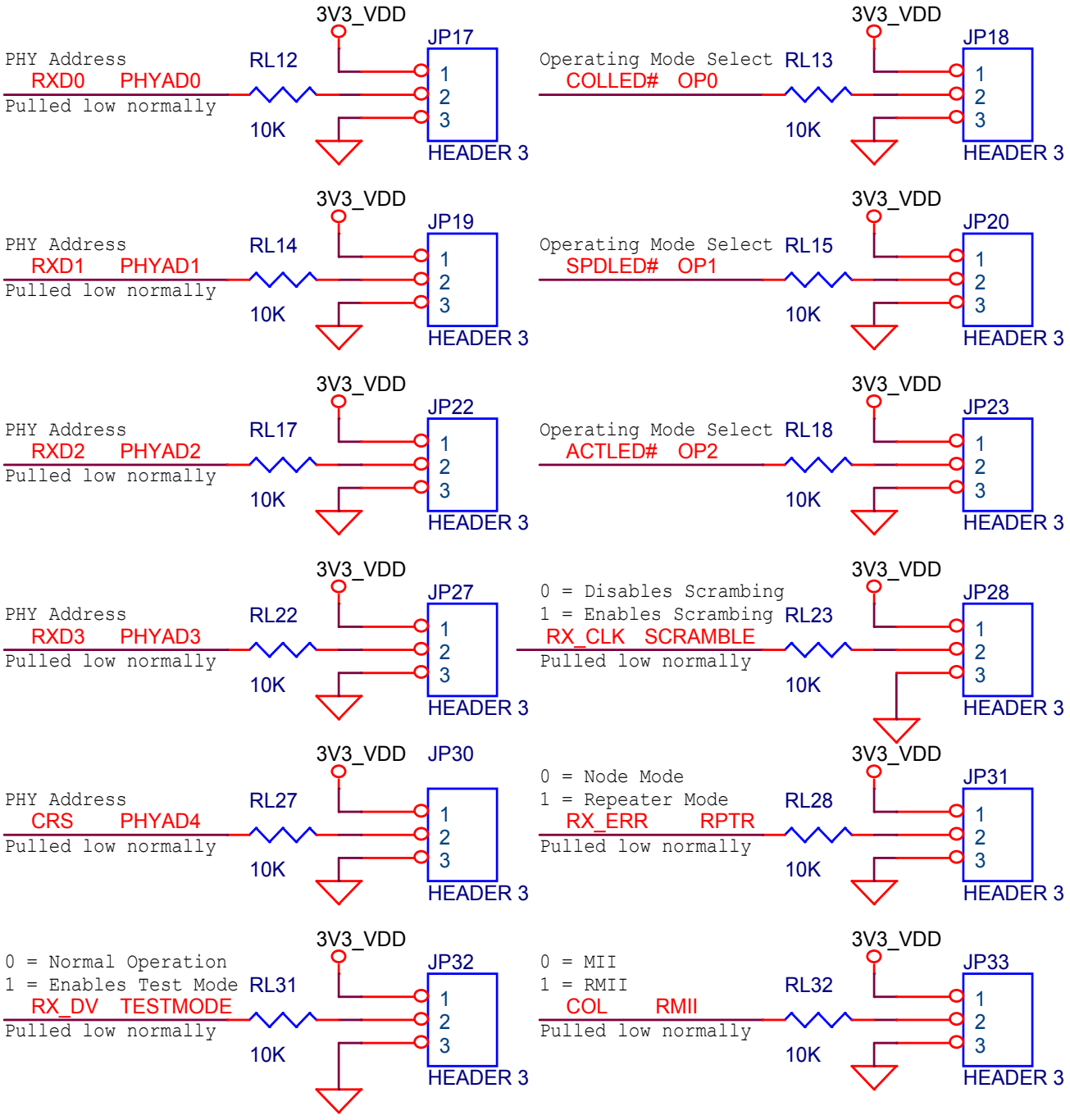


FIGURE 14: Ethernet Power on Setting

5.6 USB and UART Functions

USB is a main function and difference with other broadband router. We have an independent USB port that connect to NUC740 USB function and a second USB port that is connect to GPIO. However, the second USB function is optional with UART function.

Our USB is host controller that must supply the current to other device. Therefore, we have a power switch (UU8) to control the current. The 2nd USB is the same (UU6). In order to let 2nd USB and UART function cannot conflict that we used switch to separate the control signal. That is UU1 and UU5, FIGURE 15. UU1 is turn off the UART function. UU5 is turn off the 2nd USB function. You must turn off the switch 1 of the UU5 when use the console and UART function of the NUC740.

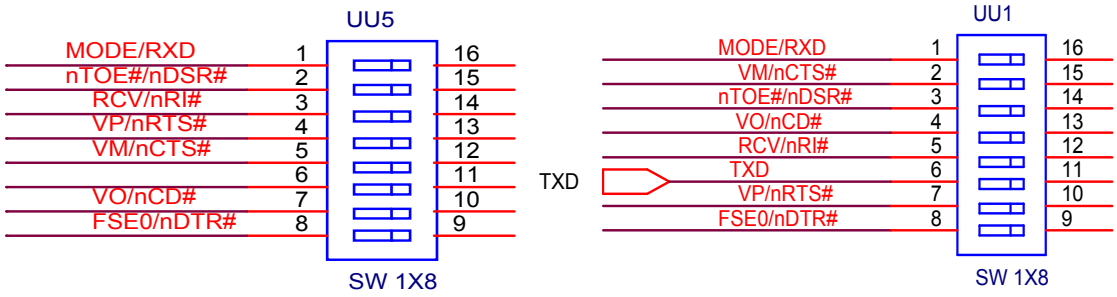


FIGURE 15: Switch devices for 2nd USB and UART

The 2nd USB must have a transceiver to improve the function. The control signal is next.

GPIO	USB	UART	Note
GP4	RCV	nRI	
GP5	VP	nRTS	
GP6	VM	nCTS	
GP7	VO	nCD	
GP8	FSE0	nTDR	
GP9	NTOE	nDSR	
GP10	*	TXD	
GP11	USB_Mode	RXD	
GP13	Suspend	*	

In order to control the USB power switch. That must select over current protect by GP18/NIRQ1 and control USB function on/off by GP12.

6 BOM

NUC740
EVB Broad of NUC740

Bill Of Materials April 11,2003 15:07:17 Page1

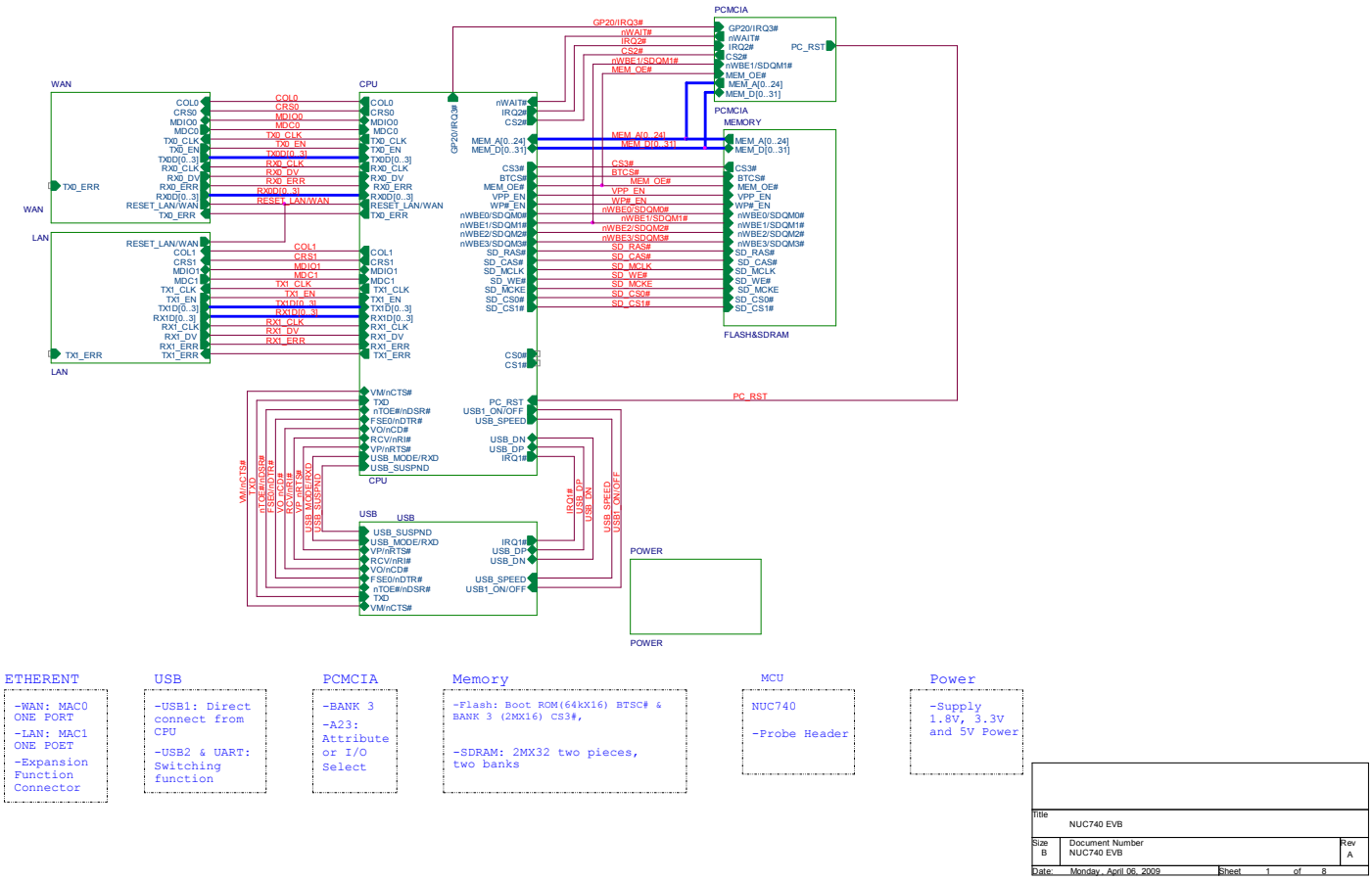
Item	Quantity	Reference	Part
1	2	CC1,CC2	20P
2	78	CP1,CI1,CF1,CD1,CW2,CL2, CF2,CD2,CW3,CL3,CI3,CD3, CC3,CW4,CP4,CL4,CD4,CC4, CW5,CL5,CF5,CD5,CC5,CU6, CP6,CF6,CD6,CC6,CF7,CD7, CC7,CW8,CP8,CL8,CD8,CC8, CW9,CL9,CD9,CC9,CW10, CL10,CD10,CC10,CU11,CD11, CC11,CD12,CC12,CW13,CL13, CC13,CP14,CC14,CD15,CC15, CD16,CW17,CP17,CL17,CD17, CW18,CP18,CL18,CD18,CW19, CL19,CD19,CP20,CD20,CD21, CD22,CP23,CD23,CP24,CD24, CD25,CD26	0.1uF
3	20	CI2,CI4,CP5,CP7,CF8,CF10, CP13,CD13,CD14,CP15,CC16, CC17,CC18,CP19,CC19,CC20, CP21,CC21,CD27,CD28	47U 16V
4	10	CC22,CW23,CL23,CC24,CC25, CC26,CC28,CC29,CC37,CC38	10P NO ON
5	1	CC23	10P
6	7	CU8,CU10,CF11,CW12,CL12, CW16,CL16	0.01UF
7	12	CW1,CL1,CU3,CU4,CU5,CU9, CW14,CL14,CW15,CL15,CP16, CP22	10UF 16V
8	4	CW6,CL6,CW7,CL7	0.1uF 2KV
9	4	CW21,CL21,CW22,CL22	22pF
10	2	CONU1,CONU2	USB CON
11	2	CP3,CP2	100UF 16V
12	3	CU1,CU7,CU12	33uF/16V
13	1	CU2	1UF 16V
14	3	DW1,DL1,DC1	RED
15	11	DC2,DW3,DL3,DC3,DC4,DC5, DC7,DC8,DC9,DC10,DC11	GREEN
16	1	DC6	3.0V ZENER
17	2	DL2,DW2	YELLOW
18	2	DL4,DW4	ORG
19	1	JC1	CON14A
20	1	JC2	CON20A

21	2	JC3,JC4 CON1	
22	2	JL1,JW1 CON26A	
23	2	JL2,JW2 RJ-45L	
24	42	JP1,JP2,JP5,JP6,JP7,JP8, HEADER 3 JP16,JP17,JP18,JP19,JP20, JP21,JP22,JP23,JP26,JP27, JP28,JP29,JP30,JP31,JP32, JP33,JP36,JP37,JP38,JP39, JP40,JP41,JP42,JP43,JP44, JP45,JP46,JP47,JP48,JP49, JP52,JP53,JP61,JP63,JP64, JP65	
25	2	JP14,JP12 HEADER 22X2	
26	1	JP13 HEADER 16X2	
27	1	JP15 HEADER 5X2	
28	5	JP24,JP50,JP51,JP55,JP62	HEADER 2
29	2	J4,J5 HEADER 30	
30	2	J7,J6 HEADER 30X2	
31	27	LP1,LF1,LD1,LC1,LW2,LP2, LL2,LF2,LC2,LL3,LI3,LF3, LW4,LP4,LL4,LI4,LC4,LW5, LP5,LL5,LC5,LW6,LP6,LC6, LC7,LC8,LC9	FB
32	2	LI1,LI2 NO USE	
33	4	LU1,LU2,LU3,LU4 FB1206	
34	18	PR1,PR2,PR3,PR4,PR5,PR6, PR7,PR8,PR9,PR10,PR11, PR12,PR13,PR14,PR15,PR16, PR17,PR18	33PR
35	2	QF1,QF2 BC558 NO ON	
36	1	QF3 BC548B	
37	3	RC1,RI4,RI6 33R	
38	62	RI2,RC2,RI3,RC3,RC4,RI5, RC5,RC6,RC7,RP8,RC8,RC9, RC10,RC11,RC12,RC13,RC14, RC15,RC16,RC17,RC18,RC19, RC23,RC24,RC25,RC26,RC27, RC28,RC29,RC30,RC33,RC34, RC36,RC37,RC40,RC41,RC42, RC43,RC45,RC47,RC48,RC49, RC52,RC53,RC54,RC55,RC58, RC59,RC60,RC61,RC62,RC63, RC64,RC65,RC66,RC69,RC70, RC71,RC72,RC73,RC78,RC79	47
39	16	RU3,RF8,RF10,RU12,RC20, RC21,RL25,RW26,RC31,RC32, RC38,RC39,RC44,RC50,RC51, RC68	0R
40	1	RC22 1M	
41	2	RC56,RC57 NO ON	
42	53	RU1,RI1,RU2,RP3,RI7,RI8, RI9,RI10,RI11,RW12,RL12,	10K

		RI12,RW13,RL13,RI13,RW14, RL14,RI14,RW15,RL15,RW16, RL17,RW18,RL18,RW19,RL22, RW23,RL23,RW24,RL27,RW28, RL28,RW29,RL31,RW32,RL32, RW33,RL33,RW34,RL34,RW35, RL35,RC67,RC80,RC81,RC82, RC83,RC84,RC85,RC86,RC87, RC88,RC90	
43	3	RW1,RL2,RC74	100K
44	4	RF15,RC75,RC89,RC91	4.7K
45	10	RU5,RP9,RF13,RC100,RC101, RC103,RC104,RC105,RC106, RC107	1K
46	1	RC102	10
47	5	RW36,RL36,RC108,RC109, RC110	0R NO ON
48	4	RF6,RF7,RF9,RF11	4.7K NO ON
49	2	RF12,RF14	47K
50	2	RL1,RW3	1.5K
51	8	RW2,RL3,RW4,RL4,RW5,RL5, RW10,RL10	50R 1%
52	8	RW6,RL6,RW7,RL7,RW8,RL8, RW9,RL9	75R 1%
53	2	RL11,RW11	6.8K
54	8	RL16,RW17,RL21,RW22,RL26, RW27,RL30,RW31	300R
55	2	RL20,RW21	33
56	2	RP6,RP1	2K
57	3	RP2,RP5,RP7	1.2K
58	1	RP4	560R
59	1	RP10	560
60	1	RU4	100
61	4	RU6,RU7,RU8,RU9	15K
62	2	RU10,RU11	27
63	1	SP1	POWER SW
64	2	SW1,SW4	DIP-4W
65	6	UU1,SW2,SW3,UU5,SW5,SW6	SW 1X8
66	1	UC1	NUC740
67	1	UC3	MIC811
68	1	UC4	7408
69	1	UC5	74HC04
70	1	UC6	TOP SWITCH
71	2	UD2,UD1	512X4X32 64M
72	1	UF1	W39L010
73	1	UF2	W28J160B/T 2MX16
74	2	UI1,UF4	7404
75	1	UI2	74F244
76	1	UI3	PCMCIA SOCKET
77	2	UL1,UW1	PE-68515L
78	2	UL2,UW2	DM9161
79	1	UP1	Power CON

80	2	UP2,UP4	MIC29152
81	1	UP3	MSOP-8 MIC3975
82	1	UU2	MAX241/SO
83	1	UU6	AP1212H
84	1	UU7	CONNECTOR DB9 Female
85	1	UU8	PDIUSBP11A
86	8	U1,U2,U4,U5,U6,U7,U8,U9	Nuvoton Logo
87	1	YC1	15MHz
88	2	YL1,YW1	25 MHz
89	2	YL2,YW2	25/50 MHz

7 Schematic



ETHERENT	USB	PCMCIA	Memory	MCU	Power
-WAN: MAC0 ONE PORT -LAN: MAC1 ONE POET -Expansion Function Connector	-USB1: Direct connect from CPU -USB2 & UART: Switching function	-BANK 3 -A23: Attribute or I/O Select	-Flash: Boot ROM(64kX16) BTSC# & BANK 3 (2MX16) CS3#, -SDRAM: 2MX32 two pieces, two banks	NUC740 -Probe Header	-Supply 1.8V, 3.3V and 5V Power

Title	NUC740 EVB		
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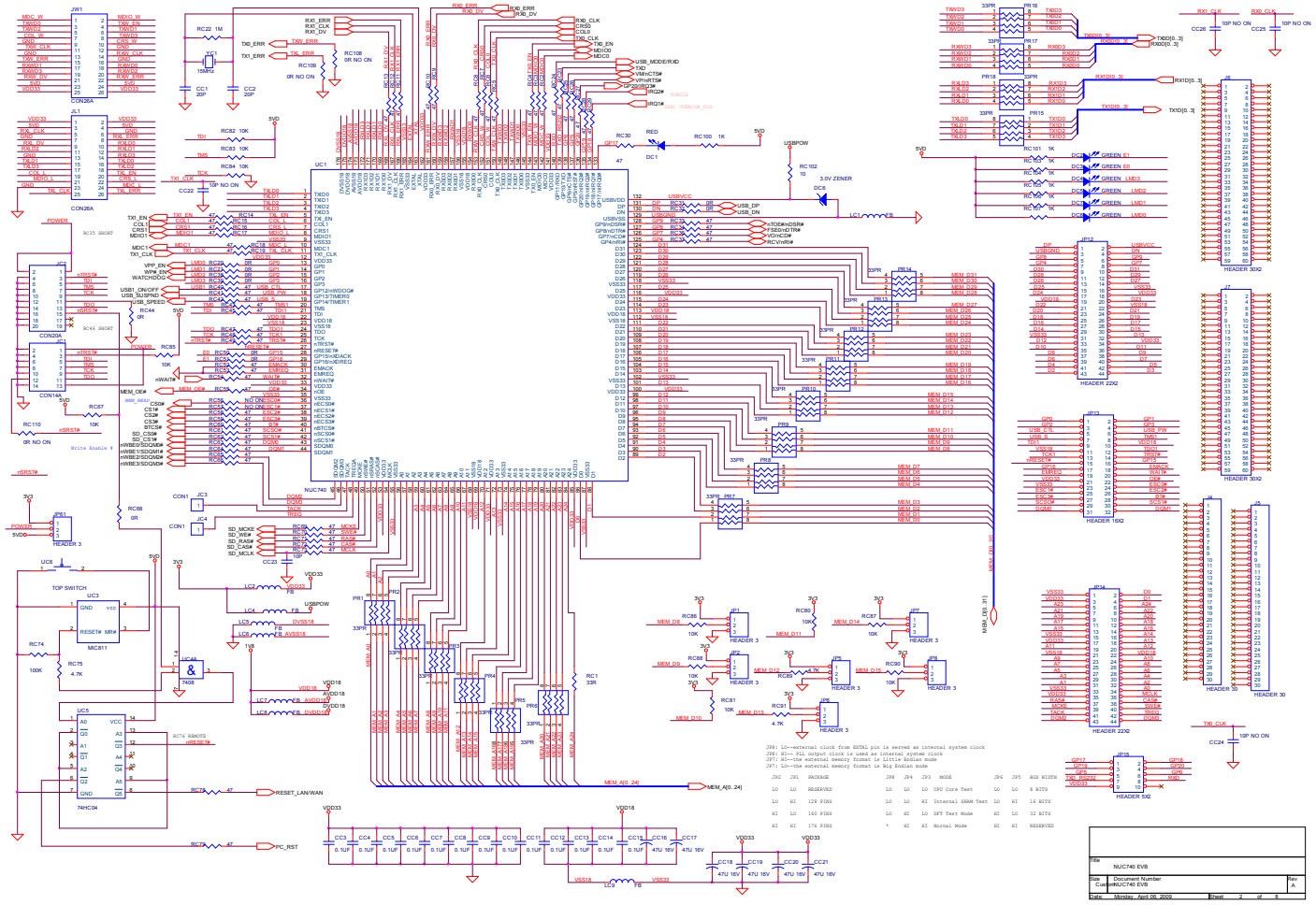

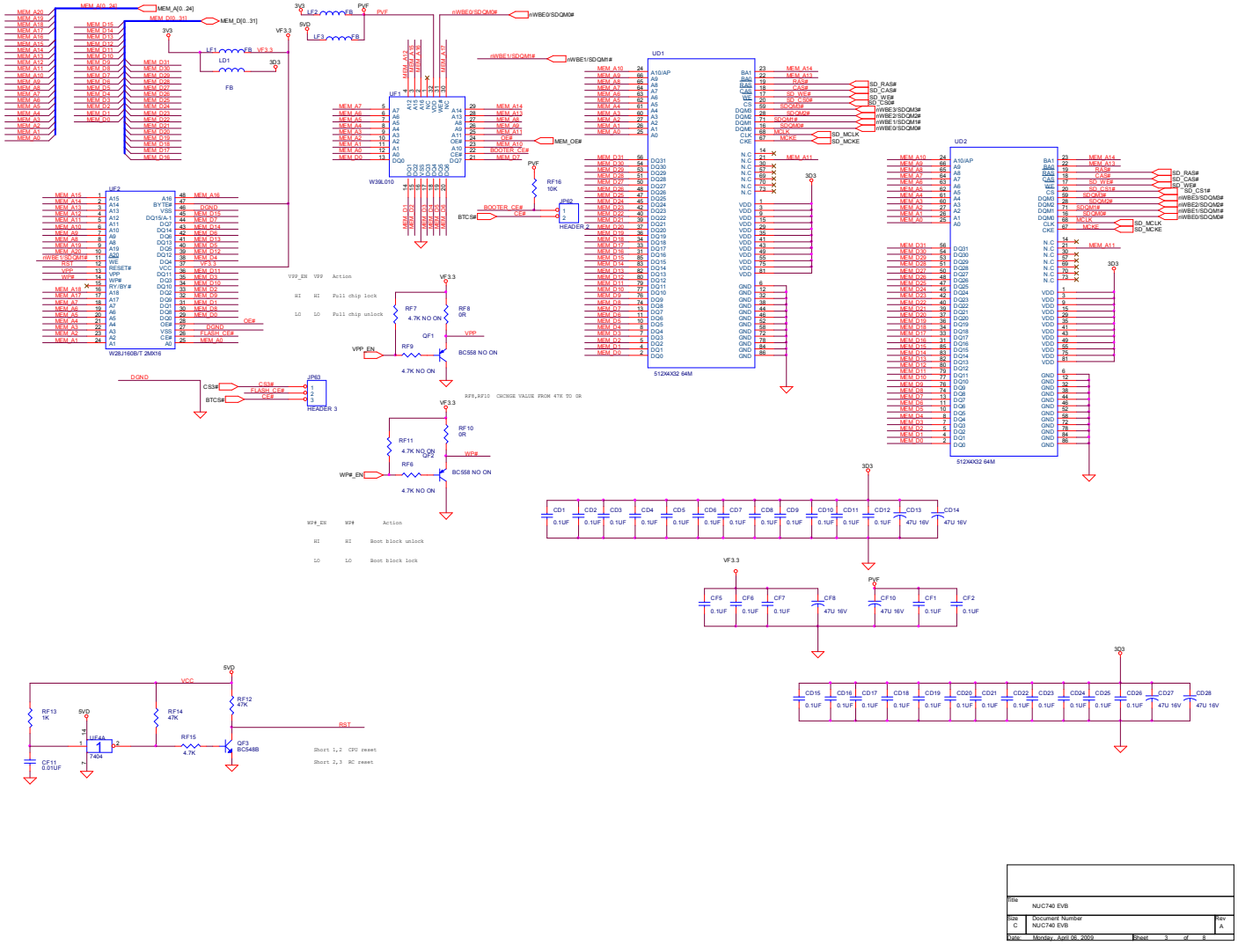

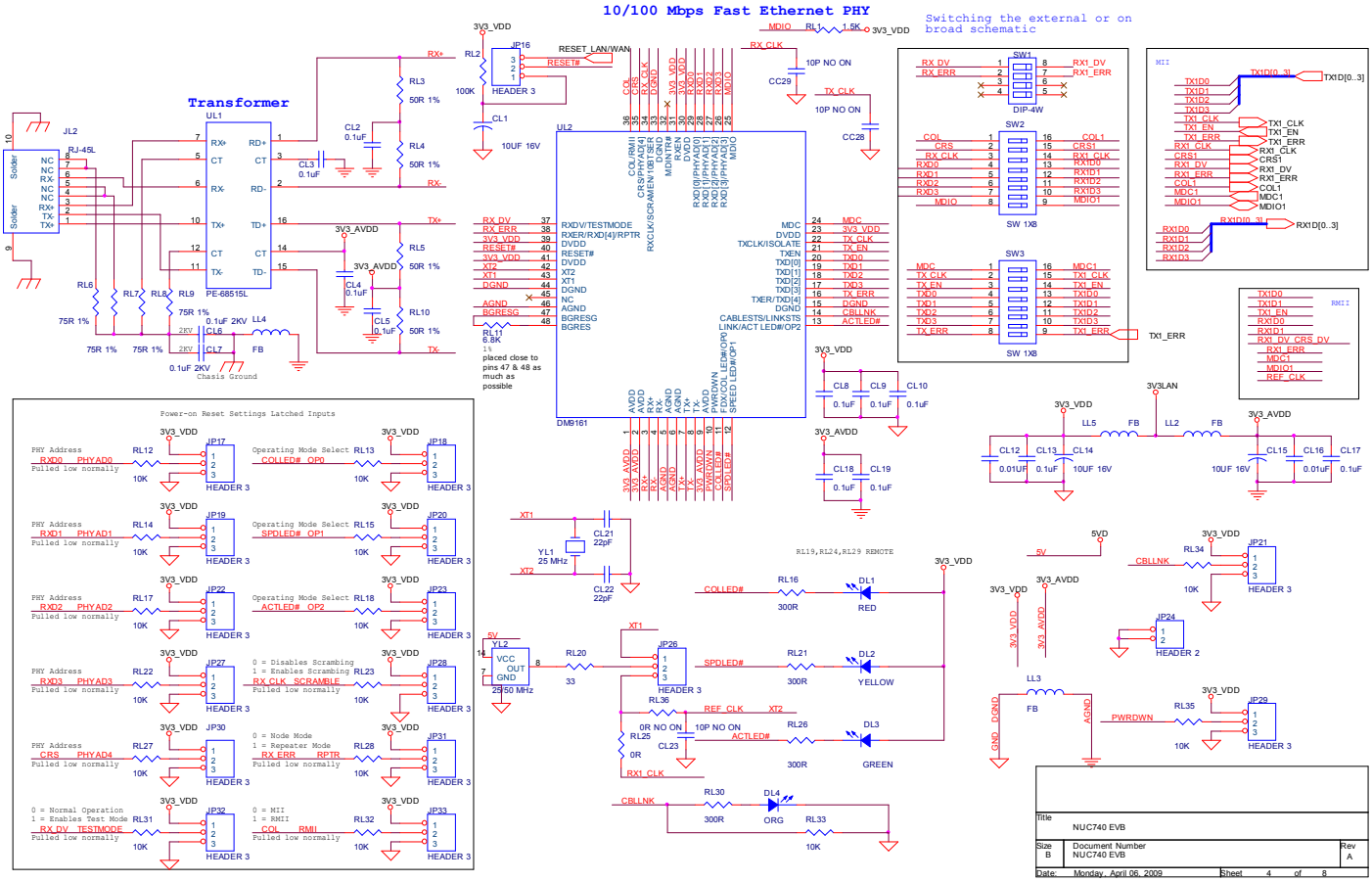
10/100 Mbps Fast Ethernet PHY
Switching the external or on broad schematic
Transformer
UL1
PE-68515L
UL2
DM9161
JL2
RJ-45L
JP16
HEADER 3
RESET_LAN/WAN
RESET#
3V3_VDD
3V3_AVDD
MDIO
RL1
1.5K
RX_CLK
TX_CLK
10P NO ON
CC29
CC28
10UF 16V
CL1
RL2
100K
RL3
RL4
RL5
RL10
50R 1%
CL2
CL3
CL4
CL5
0.1uF
RL6
RL7
RL8
RL9
75R 1%
0.1uF 2KV
CL6
CL7
LL4
FB
Chasis Ground
RL11
6.8K
placed close to pins 47 & 48 as much as possible
SW1
SW2
SW3
DIP-4W
SW 1X8
TX1_ERR
MII
RMII
Power-on Reset Settings Latched Inputs
PHY Address
Pulled low normally
Operating Mode Select
HEADER 3
HEADER 2
YL1
25 MHz
YL2
25.50 MHz
RL19,RL24,RL29 REMOTE
DL1
RED
DL2
YELLOW
DL3
GREEN
DL4
ORG
LL3
LL5
LL2
3V3LAN
5VD
5V
CBLLNK
PWRDWN
REF_CLK
Title
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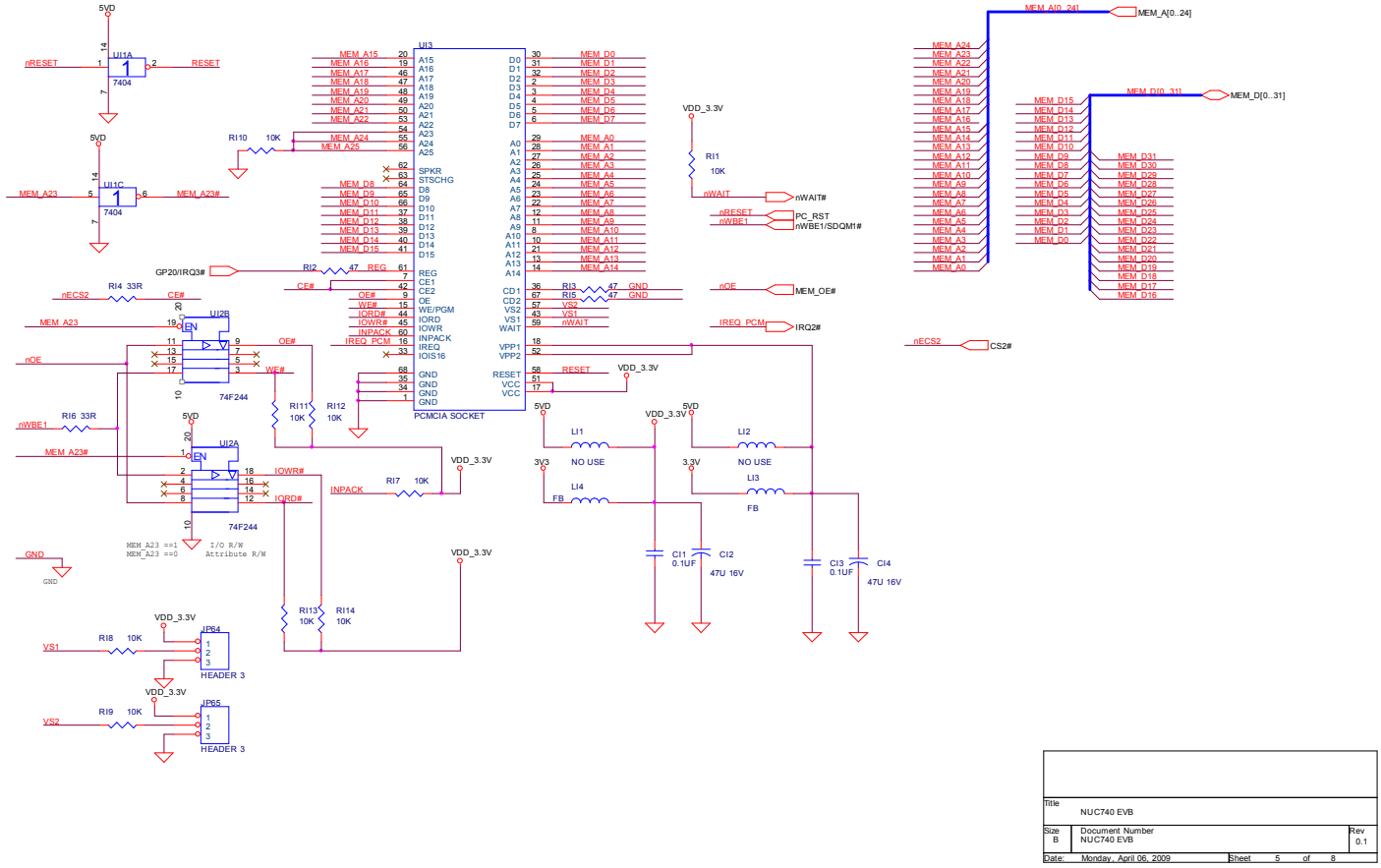
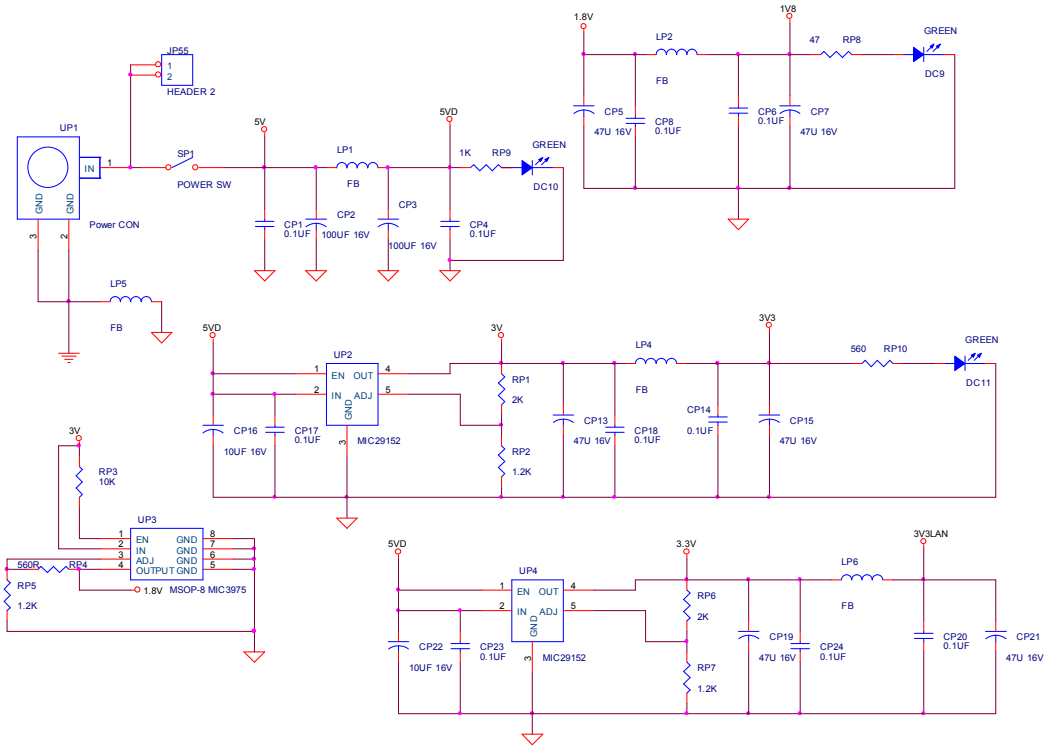


Title	NUC740 EVB	
Size B	Document Number NUC740 EVB	Rev 0.1
Date: Monday, April 06, 2009	Sheet 5 of 8	



Title	NUC740 EVB	
Size B	Document Number NUC740 EVB	Rev 0.1
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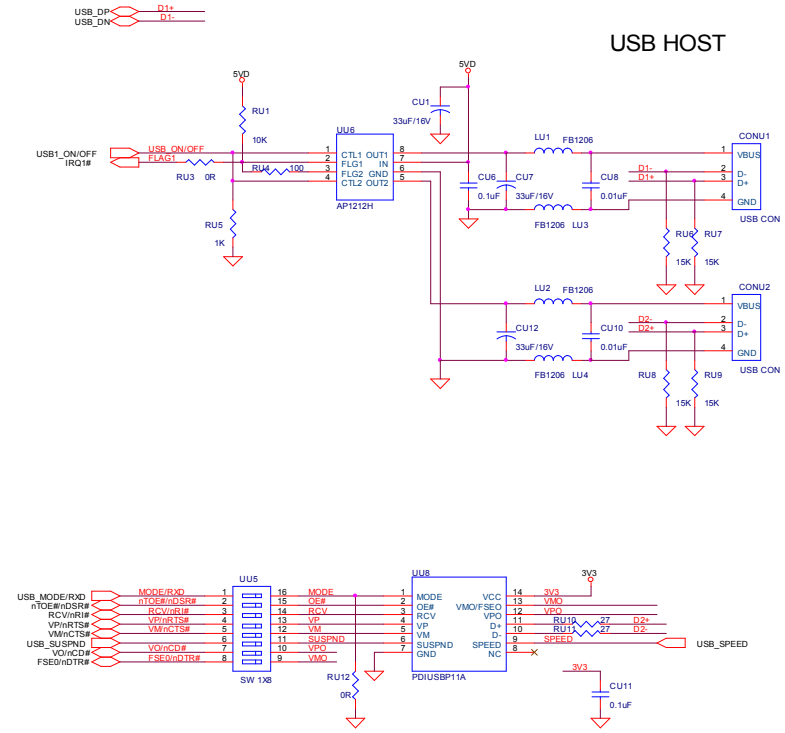

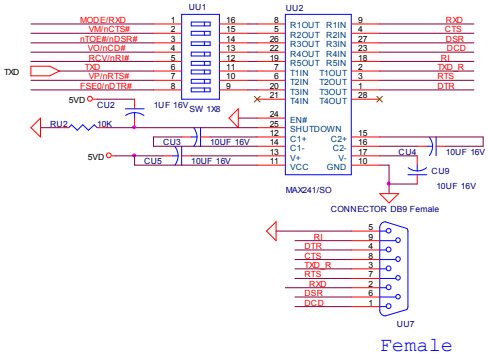

Title	NUC740 EVB	
Size B	Document Number NUC740 EVB	Rev 0.1
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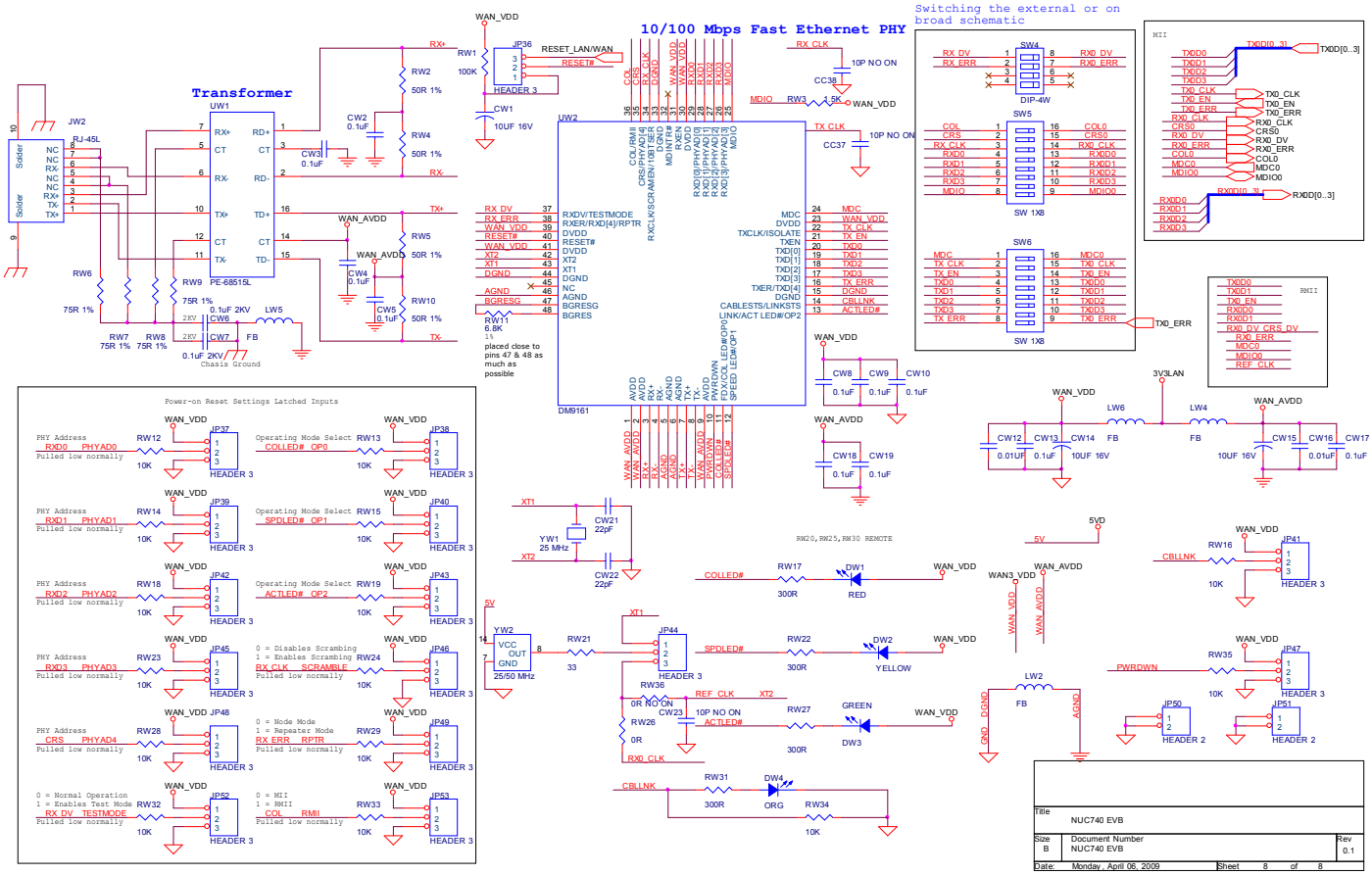
10/100 Mbps Fast Ethernet PHY
Transformer
Switching the external or on broad schematic
Power-on Reset Settings Latched Inputs
Title
NUC740 EVB
Size
B
Document Number
NUC740 EVB
Rev
0.1
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