Addendum

MCF5407UMAD/D
Rev. 2, 2/2003

Errata to MCF5407 Integrated Microprocessor User's Manual, rev 0

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This errata describes corrections and updates to rev 0 of the *MCF5407 ColdFire Integrated Microprocessor User's Manual*, Motorola document order number MCF5407UM/D. The General MCF5407 Changes section contains information that needs to be changed throughout the book. Please check the world wide web at http://www.motorola.com/semiconductors for the latest updates.

1. General MCF5407 Changes

The MCF5407 is offered with the temperature and frequency specifications shown in Table 1.

Table 1. MCF5407 Temperature and Frequency Specifications

Package	Operating Temperature	Frequency	MIPS Rating
208 plastic QFP	0 to 70° C	54 MHz max CLIN/ 220 MHz max PCLK	316 Dhrystone MIPS at 220 MHz
208 plastic QFP	-40 to 85 ° C	54 MHz max CLKIN/ 162 MHz max PCLK	233 Dhrystone MIPS at 162 MHz

NOTE

These specifications further amend the electrical characteristics described in Section 1., “General MCF5407 Changes.”

The following section “Chapter 20, Electrical Specifications” replaces Chapter 20 of the *MCF5407 ColdFire Integrated Microprocessor User’s Manual.*

Chapter 20
Electrical Specifications

This chapter describes the AC and DC electrical specifications and thermal characteristics for the MCF5407. Note that this information was correct at the time this book was published. As process technologies improve, there is a likelihood that this information may change. To confirm that this is the latest information, see Motorola's ColdFire webpage, http://www.motorola.com/coldfire.

20.1 General Parameters

Table 20-1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 20-1. Absolute Maximum Ratings

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	EV_{cc}	-0.3 to +4.0	V
Internal logic supply voltage	IV_{cc}	-0.5 to +2.0 [1, 2]	V
PLL supply voltage	PV_{cc}	-0.5 to +2.0 [2, 3]	V
Internal logic supply voltage, input voltage level	V_{in}	-0.5 to +3.6 [4]	V
Storage temperature range	T_{stg}	-55 to +150	^{o}C

1 IV_{cc} must not exceed EV_{cc}
2 IV_{cc} and PV_{cc} must not differ by more than 0.5 V
3 PV_{cc} must not exceed EV_{cc}
4 V_{in} must not exceed EV_{cc}

Table 20-2 lists junction and ambient operating temperatures.

Table 20-2. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T_j	95	^{o}C
Maximum operating junction temperature (Extended Temperature Device)	T_j	110	^{o}C
Maximum operating ambient temperature	T_{Amax}	70 [1]	^{o}C
Maximum operating ambient temperature (Extended Temperature Device)	T_{Amax}	85 [1]	^{o}C
Minimum operating ambient temperature	T_{Amin}	0	^{o}C
Minimum operating ambient temperature (Extended Temperature Device)	T_{Amin}	-40	^{o}C

1 This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

Table 20-3 lists thermal resistances.

Table 20-3. Thermal Resistance

Characteristic	Symbol	Value	Units
Junction to ambient	θ_{JA}	26.1	$^{o}C/W$
Junction to top reference	ψ_j	1.9	$^{o}C/W$

Table 20-4 lists DC electrical specifications. This table is based on an operating voltage of EVcc = 3.3 Vdc ± 0.3 Vdc and IVcc of 1.8 ± 0.10 Vdc.

Table 20-4. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
External (I/O pads) operation voltage range	EV_{cc}	3.0	3.6	V
Internal logic operation voltage range [1]	IV_{cc}	1.7	1.9	V
PLL operation voltage range [1]	PV_{cc}	1.65	1.95	V
Input high voltage [2]	V_{IH}	2.4	3.6	V
Input low voltage[2]	V_{IL}	-0.5	0.5	V
Input signal undershoot	—	—	0.8	V
Input signal overshoot	—	—	0.8	V
Input leakage current @ 0.5/2.4 V during normal operation	I_{in}	—	20	µA
High impedance (three-state) leakage current @ 0.5/2.4 V during normal operation	I_{TSI}	—	20	µA
Signal low input current, V_{IL} = 0.8 V [3]	I_{IL}	0	1	mA
Signal high input current, V_{IH} = 2.0 V [3]	I_{IH}	0	1	mA
Output high voltage I_{OH} = 6 mA [4], 12 mA [5]	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 6 mA [4], 12 mA [5]	V_{OL}	—	0.5	V
Load capacitance (all outputs)	C_L	—	50	pF
Capacitance [6], V_{in} = 0 V, f = 1 MHz	C_{IN}	—	TBD	pF

1 IV_{cc} and PV_{cc} should be at the same voltage.

2 All pins except MTMOD. For MTMOD V_{IH} = 2.6V, V_{IL} = 0.4V.

3 $\overline{\text{BKPT}}$/TMS, DSI/TDI, DSCLK/$\overline{\text{TRST}}$

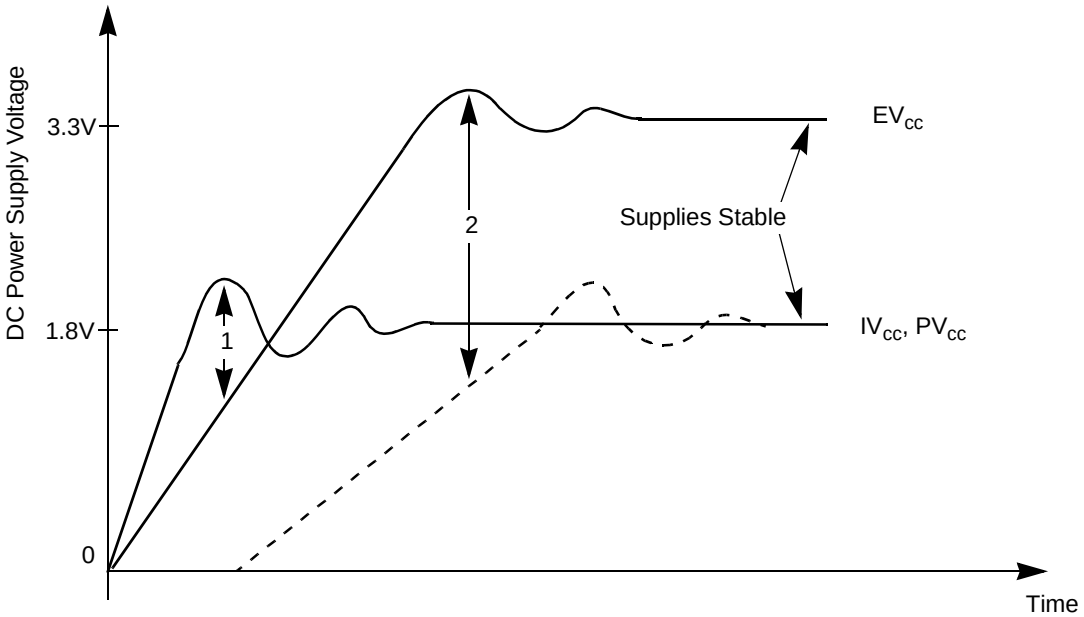
4 D[31:0], A[23:0], PP[15:0],$\overline{\text{TS}}$, $\overline{\text{TA}}$, SIZ[1:0], R/$\overline{\text{W}}$, $\overline{\text{BR}}$, $\overline{\text{BD}}$, $\overline{\text{RSTO}}$, $\overline{\text{AS}}$, $\overline{\text{CS}}$[7:0], $\overline{\text{BE}}$[3:0], $\overline{\text{OE}}$, PSTCLK, PSTDDATA[7:0], DSO, TOUT[1:0], SCL, SDA, $\overline{\text{RTS}}$[1:0], TXD[1:0]

5 BCLKO, $\overline{\text{RAS}}$[1:0], $\overline{\text{CAS}}$[3:0], $\overline{\text{DRAMW}}$, SCKE, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$

6 Capacitance C_{IN} is periodically sampled rather than 100% tested.

20.1.1 Supply Voltage Sequencing and Separation Cautions

Figure 20-1 shows two situations to avoid in sequencing the IV_{cc} and EV_{cc} supplies.



Notes:

1 IV_{cc}, PV_{cc} rising before EV_{cc}

2 EV_{cc} rising much faster than IV_{cc}, PV_{cc}

Figure 20-1. Supply Voltage Sequencing and Separation Cautions

IV_{cc} should not be allowed to rise early (1). This is usually avoided by running the regulator for the IV_{cc} supply (1.8 V) from the voltage generated by the 3.3-V EV_{cc} supply (Figure 20-2). This keeps IV_{cc} from rising faster than EV_{cc}.

IV_{cc} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies as shown in Figure 20-2. The series diodes forward bias when the difference between EV_{cc} and IV_{cc} reaches approximately 2.1V, causing IV_{cc} to rise as EV_{cc} ramps up. When the IV_{cc} regulator begins proper operation, the difference between supplies should not exceed 1.5 V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to: EV_{cc} Š IV_{cc} Š (EV_{cc} - 2.1 V). The PLL Vdd (PV_{cc}) supply should comply with these constraints just as IV_{cc} does. In practice, PV_{cc} is typically connected directly to IV_{cc} with some filtering.

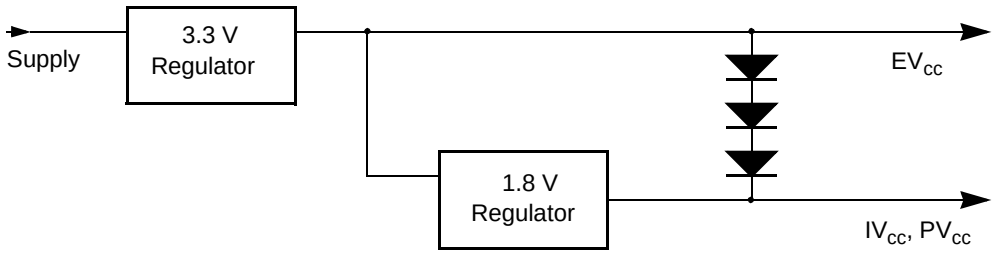


Figure 20-2. Example Circuit to Control Supply Sequencing

20.2 Clock Timing Specifications

Table 20-5 shows the MCF5407 PLL encodings. Note that they differ from the MCF5307 DIVIDE[1:0] encodings.

Table 20-5. Divide Ratio Encodings

D[2:0]/DIVIDE[2:0]	Input Clock (MHz)		Multiplier	Core Clock (MHz)		PSTCLK (MHz)	
	162 MHz	220 MHz		162 MHz	220 MHz	162 MHz	220 MHz
00x–010	Reserved						
011	40.0–54.0	40.0–55.0	3	120.0–162	120.0–165	60.0–81.0	60.0–82.5
100	25.0–40.5	25.0–55.0	4	100.0–162	100.0–220	50.0–81.0	50.0–110
101	25.0–32.4	25.0–44.0	5	125.0–162	125.0–220	67.5–81.0	67.5–110
110	25.0–27.0	25.0–36.6	6	150.0–162	150.0–220	75.0–81.0	75.0–110
111	Reserved						

Figure 20-3 correlates CLKIN and core clock frequencies for the 3x–6x multipliers.

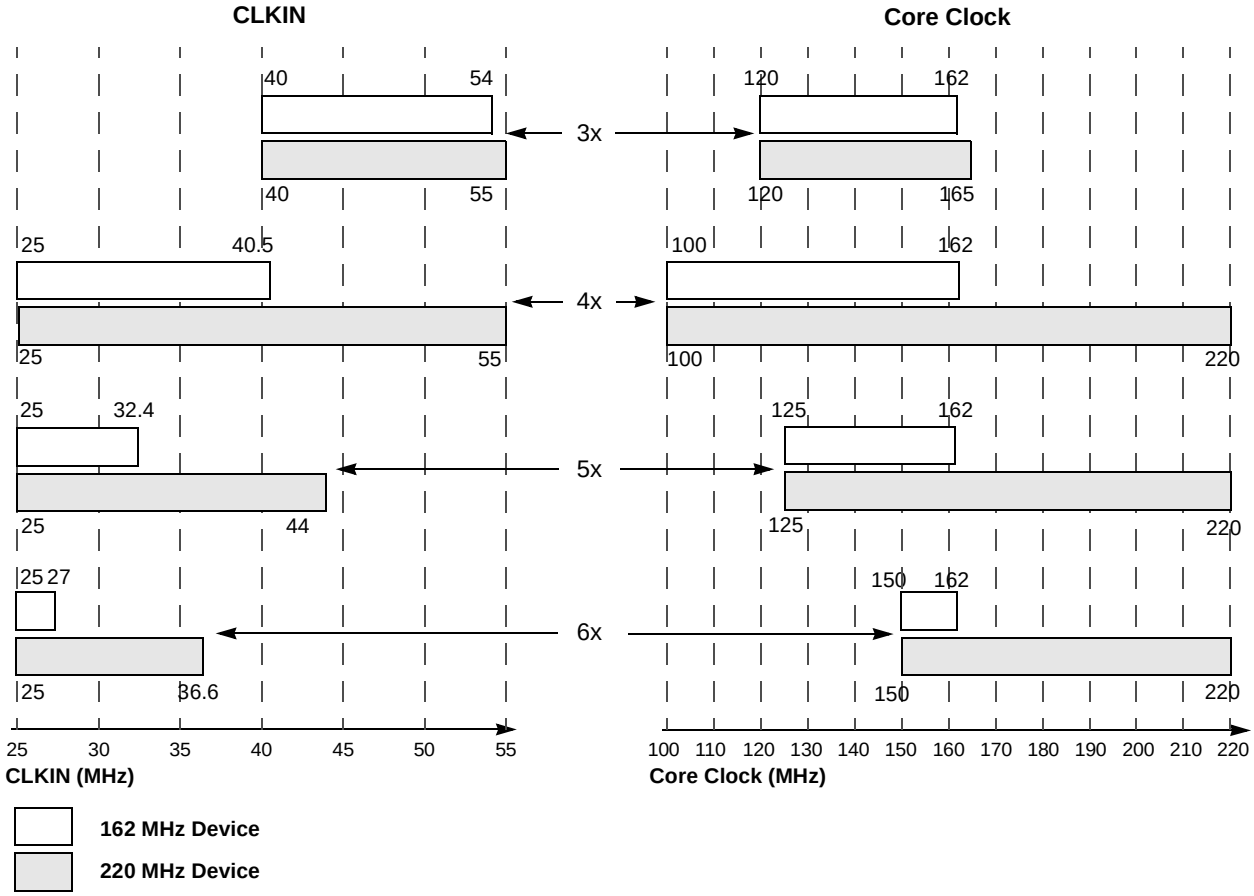


Figure 20-3. CLKIN-to-Core Clock Frequency Ranges

Table 20-6 lists specifications for the clock timing parameters shown in Figure 20-4 and Figure 20-5. Motorola recommends that CLKIN be used for the system clock. BCLKO is provided only for compatibility with slower MCF5307 designs. Regardless of the CLKIN frequency driven at power-up, CLKIN (and BCLKO) have the same ratio value to the PCLK. Although either signal can be used as a clock reference, CLKIN leaves more room to meet the bus specifications than BCLKO, which is generated as a phase-aligned signal to CLKIN.

Table 20-6. Clock Timing Specification

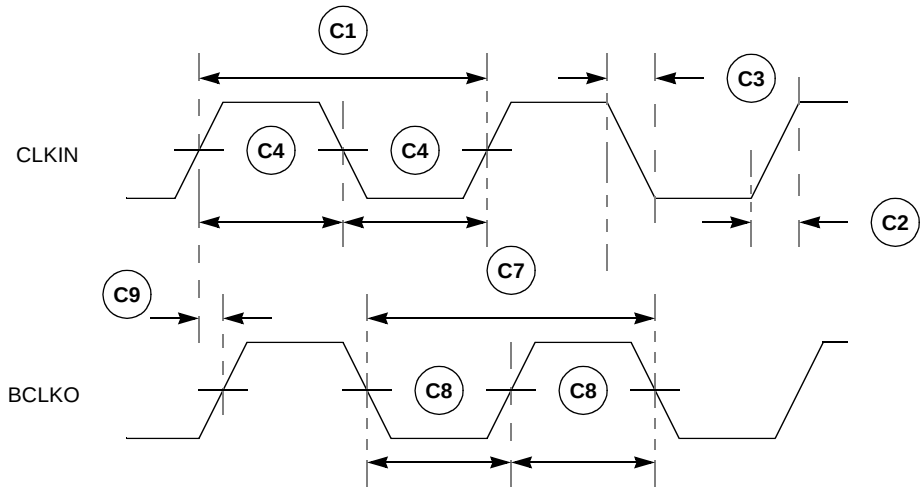
Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
C1	CLKIN cycle time	18.5	Note [1]	18.18	Note [1]	nS
C2	CLKIN rise time (0.5V to 2.4 V)	—	2	—	2	nS
C3	CLKIN fall time (2.4V to 0.5 V)	—	2	—	2	nS
C4	CLKIN duty cycle (at 1.5 V)	40	60	40	60	%
C5	PSTCLK cycle time	12.3	Note [1]	9.1	Note [1]	nS

Table 20-6. Clock Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
C6	PSTCLK duty cycle (at 1.5 V)	40	60	40	60	%
C7	BCLKO cycle time	18.5	Note [1]	18.18	Note [1]	nS
C8	BCLKO duty cycle (at 1.5 V)	45	55	45	55	%
C9	CLKIN to BCLKO	-1.5	1.5	-1.5	1.5	nS

[1] The PLL low-frequency limit depends on the clock divide ratio chosen. See Table 20-5.

Figure 20-4 shows timings for the parameters listed in Table 20-6.



Note: Input and output AC timing specifications are measured to CLKIN with a 50-pF load capacitance (not including pin capacitance).

Figure 20-4. Clock Timing

Figure 20-5 shows PSTCLK timings for parameters listed in Table 20-6.

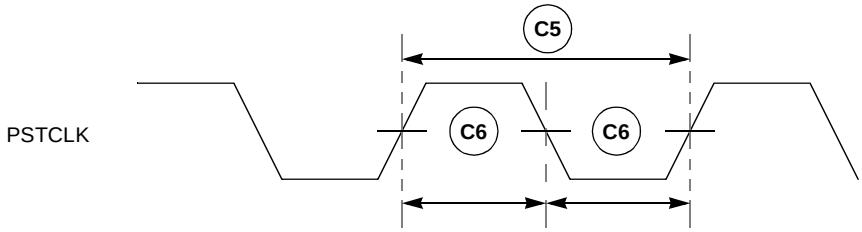


Figure 20-5. PSTCLK Timing

20.3 Input/Output AC Timing Specifications

Table 20-7 lists specifications for parameters shown in Figure 20-6 and Figure 20-7. Note that inputs $\overline{\text{IRQ}}$[7,5,3,1], $\overline{\text{BKPT}}$, and $\overline{\text{AS}}$ are synchronized internally; that is, the logic level

is validated if the value does not change for two consecutive rising CLKIN edges. Setup and hold times must be met only if recognition on a particular clock edge is required.

Table 20-7. Input AC Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
B1	Valid to CLKIN rising (setup)	7.5 [1], 8.5 [2]	—	7.5[1], 8.5[2]	—	nS
B2 [1]	CLKIN rising to invalid (hold)	1.0	—	1.0	—	nS
B3 [3]	Valid to CLKIN rising (setup)	0	—	0	—	nS
B4 [3]	CLKIN rising to invalid (hold)	0.5(C1) + 1.3	—	0.5(C1) + 1.3	—	nS
B5 [4]	CLKIN to input high impedance	—	2	—	2	Bus clock
B6	CLKIN to EDGESEL delay	0	5.0	0	5.0	nS

1 Inputs: $\overline{BG}$, $\overline{TA}$, A[23:0], PP[15:0], SIZ[1:0], R/$\overline{W}$, $\overline{TS}$, EDGESEL, D[31:0], and $\overline{BKPT}$

2 $\overline{Inputs\ IRQ}$[7,5,3,1]

3 Inputs: $\overline{AS}$

4 Inputs: D[31:0]

Table 20-8 lists specifications for timings in Figure 20-6, Figure 20-7, and Figure 20-13. Although output signals that share a specification number have approximately the same timing, due to loading differences, they do not necessarily change at the same time. However, they have similar timings; that is, minimum and maximum times are not mixed.

Table 20-8. Output AC Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
B10 [1, 2, 3]	CLKIN rising to valid	—	10.5 [4]	—	10.5[4]	nS
		—	12.5 [5]	—	12.5 [5]	nS
B11 [3,4,5]	CLKIN rising to invalid (hold)	1.0 [5]	—	1.0 [5]	—	nS
B12 [6, 7]	CLKIN to high impedance (three-state)	—	10	—	10	nS
B13 [8,2,3]	CLKIN rising to valid	—	0.5(C1) +10.5 [9]	—	0.5(C1) +10.5[9]	nS
		—	0.5(C1) +12.5 [10]	—	0.5(C1) +12.5[10]	nS
B14 [8,2,3]	CLKIN rising to invalid (hold)	0.5(C1) + 1.0	—	0.5(C1) + 1.0	—	nS
B15 [2,3]	EDGESEL to valid	—	12	—	12	nS
B16 [2,3]	EDGESEL to invalid (hold)	2	—	2	—	nS
H1	$\overline{HIZ}$ to high impedance	—	60	—	60	nS
H2	$\overline{HIZ}$ to low Impedance	—	60	—	60	nS

1 Outputs that change only on rising edge of CLKIN: $\overline{RSTO}$, $\overline{TS}$, $\overline{BR}$, $\overline{BD}$, $\overline{TA}$, R/$\overline{W}$, SIZ[1:0], PP[7:0] (and PP[15:8] when configured as parallel port outputs).

2 Outputs that can change on either CLKIN edge depending only on EDGESEL: D[31:0], A[23:0], SCKE, $\overline{SRAS}$, $\overline{SCAS}$, and $\overline{DRAMW}$ and on PP[15:8] when individually configured as A[31:24] outputs.

3 Outputs that can change on either CLKIN edge depending upon EDGESEL and the interface operating mode (DRAM/SDRAM): $\overline{RAS}$[1:0], $\overline{CAS}$[3:0]

4 $\overline{SRAS}$, $\overline{SCAS}$, $\overline{DRAMW}$, $\overline{RAS}$[1:0], $\overline{CAS}$[3:0]

5 D[31:0], A[23:0], TM[2:0], TT[1:0], SIZ[1:0], R/$\overline{W}$, $\overline{TIP}$, $\overline{TS}$, $\overline{BR}$, $\overline{BD}$, and $\overline{TA}$ and PP[15:8] when individually configured as A[31:24] outputs.

6 High impedance (three-state): D[31:0]

7 Outputs that transition to high impedance due to bus arbitration: A[23:0], R/$\overline{W}$, SIZ[1:0], $\overline{TS}$, $\overline{AS}$, and $\overline{TA}$, and PP[15:8] when individually configured as A[31:24] outputs.

8 Outputs that change only on falling edge of CLKIN: $\overline{AS}$, $\overline{CS}$[7:0], $\overline{BE}$[3:0], $\overline{OE}$

9 $\overline{SRAS}$, $\overline{SCAS}$, $\overline{DRAMW}$, $\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{AS}$, $\overline{CS}$[7:0], $\overline{BE}$[3:0], $\overline{OE}$

10 D[31:0], A[23:0], TM[2:0], TT[1:0], SIZ[1:0], R/$\overline{W}$, $\overline{TIP}$, and $\overline{TS}$ and on PP[15:8] when individually configured as A[31:24] outputs.

Note that these figures show two representative bus operations and do not attempt to show all cases. For explanations of the states, S0–S5, see Section 18.4, “Data Transfer Operation.” Note that Figure 20-7 does not show all signals that apply to each timing specification. See the previous tables for a complete listing.

Figure 20-6 shows AC timings for normal read and write bus cycles.

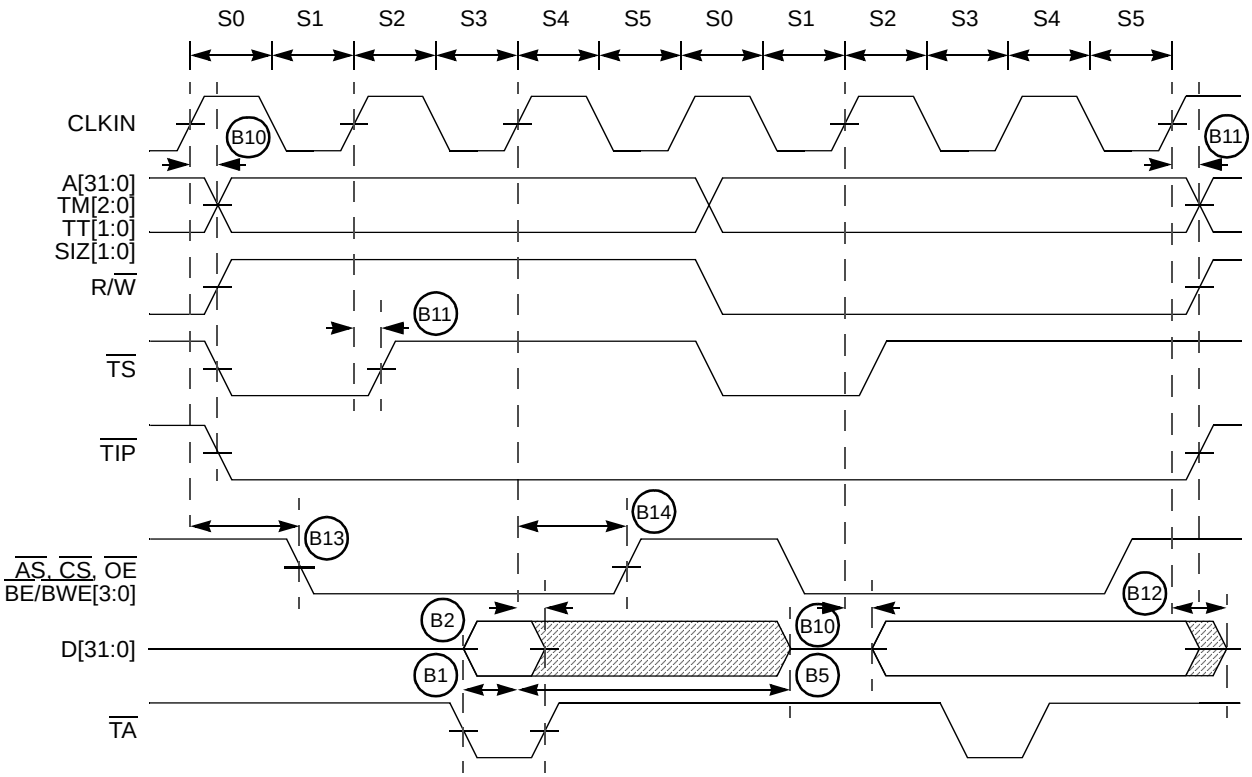


Figure 20-6. AC Timings—Normal Read and Write Bus Cycles

Figure 20-7 shows timings for a read cycle with EDGESEL tied to buffered CLKIN.

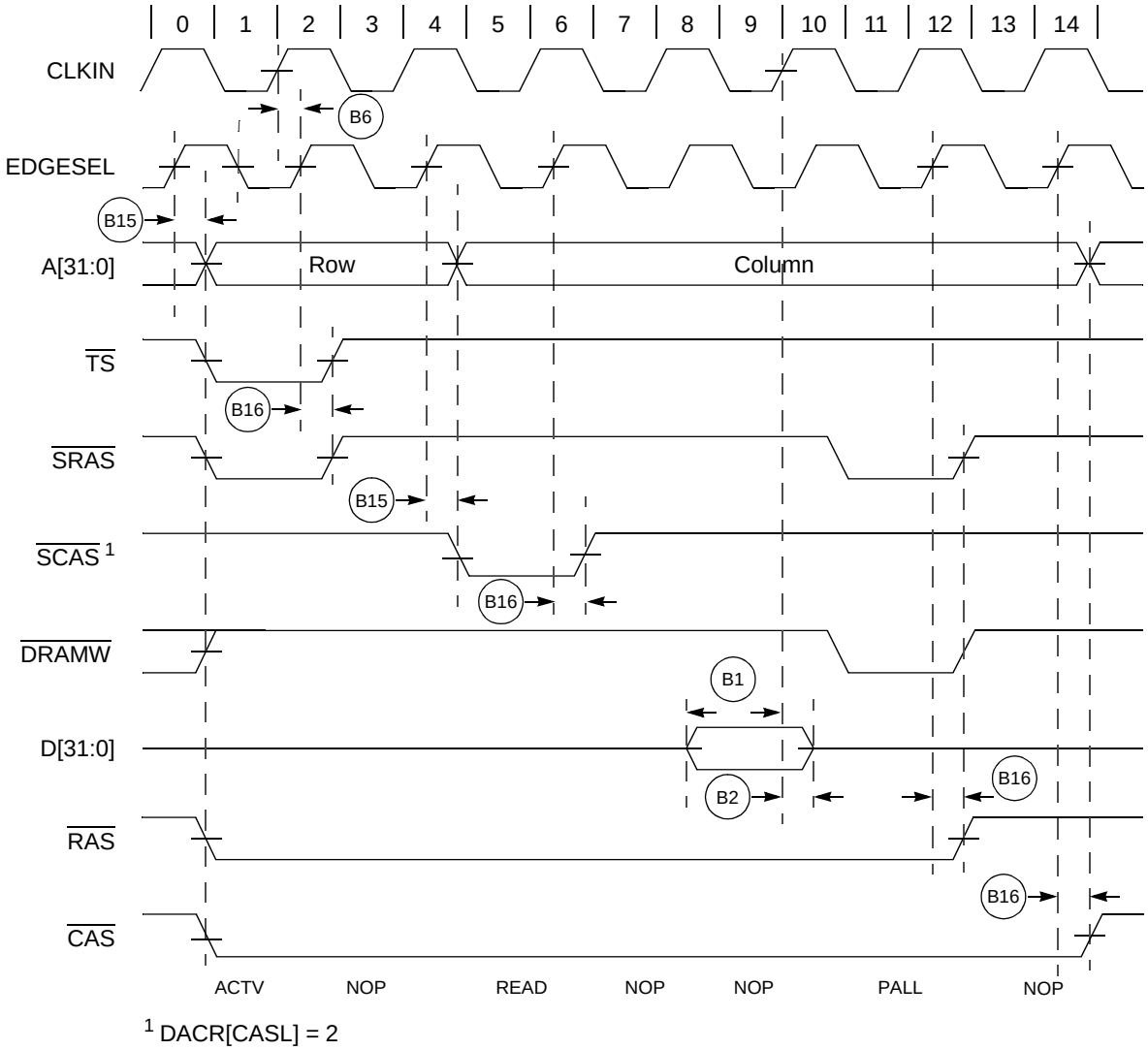


Figure 20-7. SDRAM Read Cycle with EDGESEL Tied to Buffered CLKIN

Figure 20-8 shows an SDRAM write cycle with EDGESEL tied to buffered CLKIN.

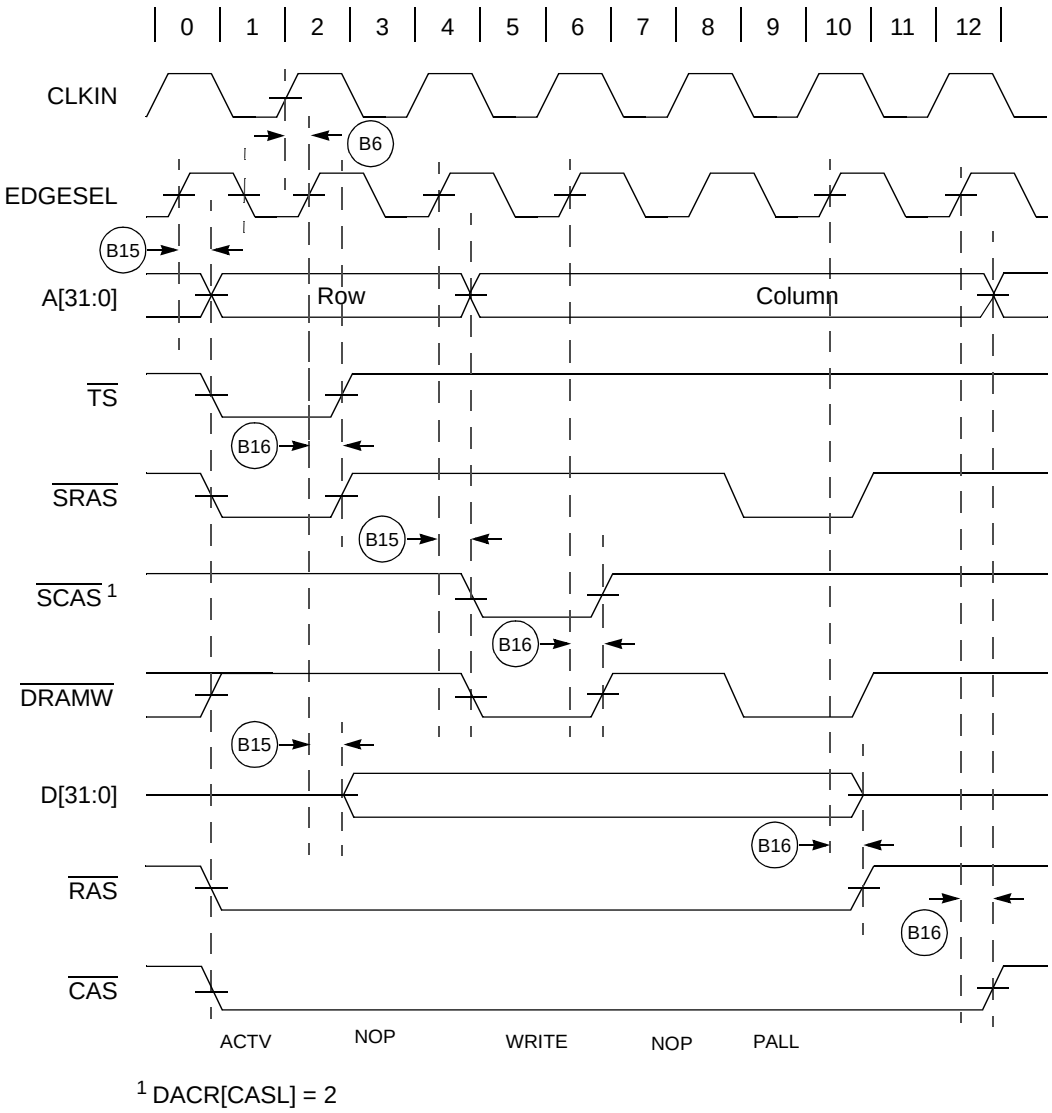


Figure 20-8. SDRAM Write Cycle with EDGESEL Tied to Buffered CLKIN

Figure 20-9 shows an SDRAM read cycle with EDGESEL tied high.

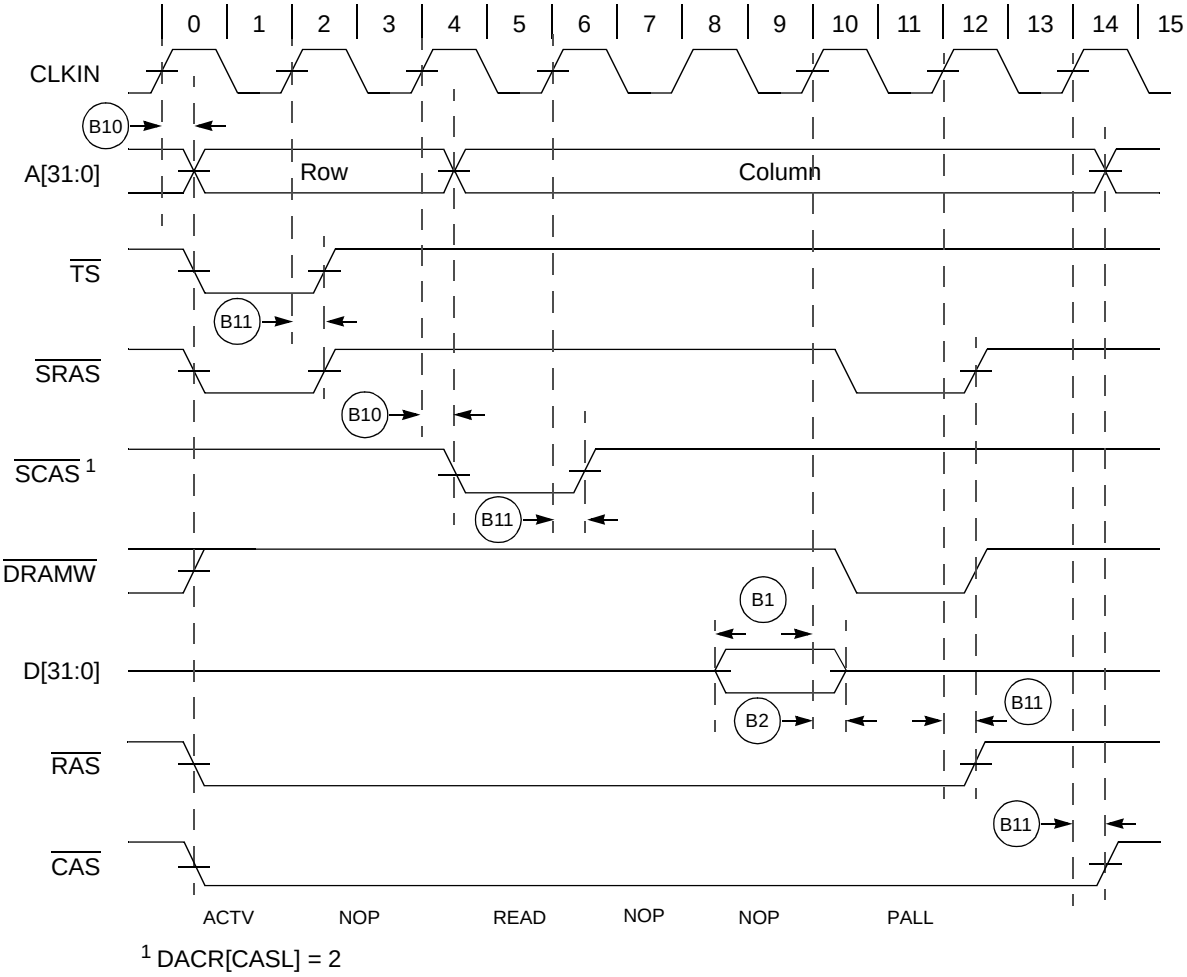


Figure 20-9. SDRAM Read Cycle with EDGESEL Tied High

Figure 20-10 shows an SDRAM write cycle with EDGESEL tied high.

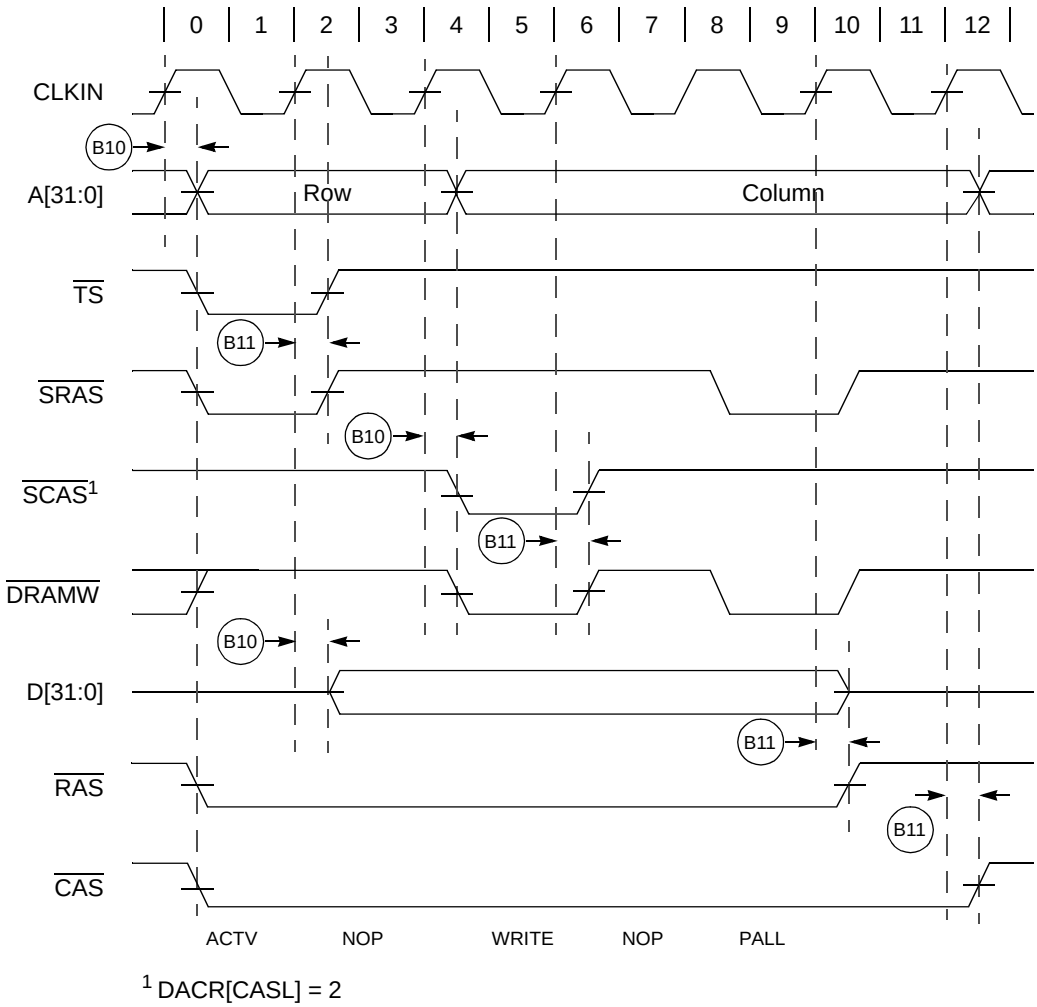
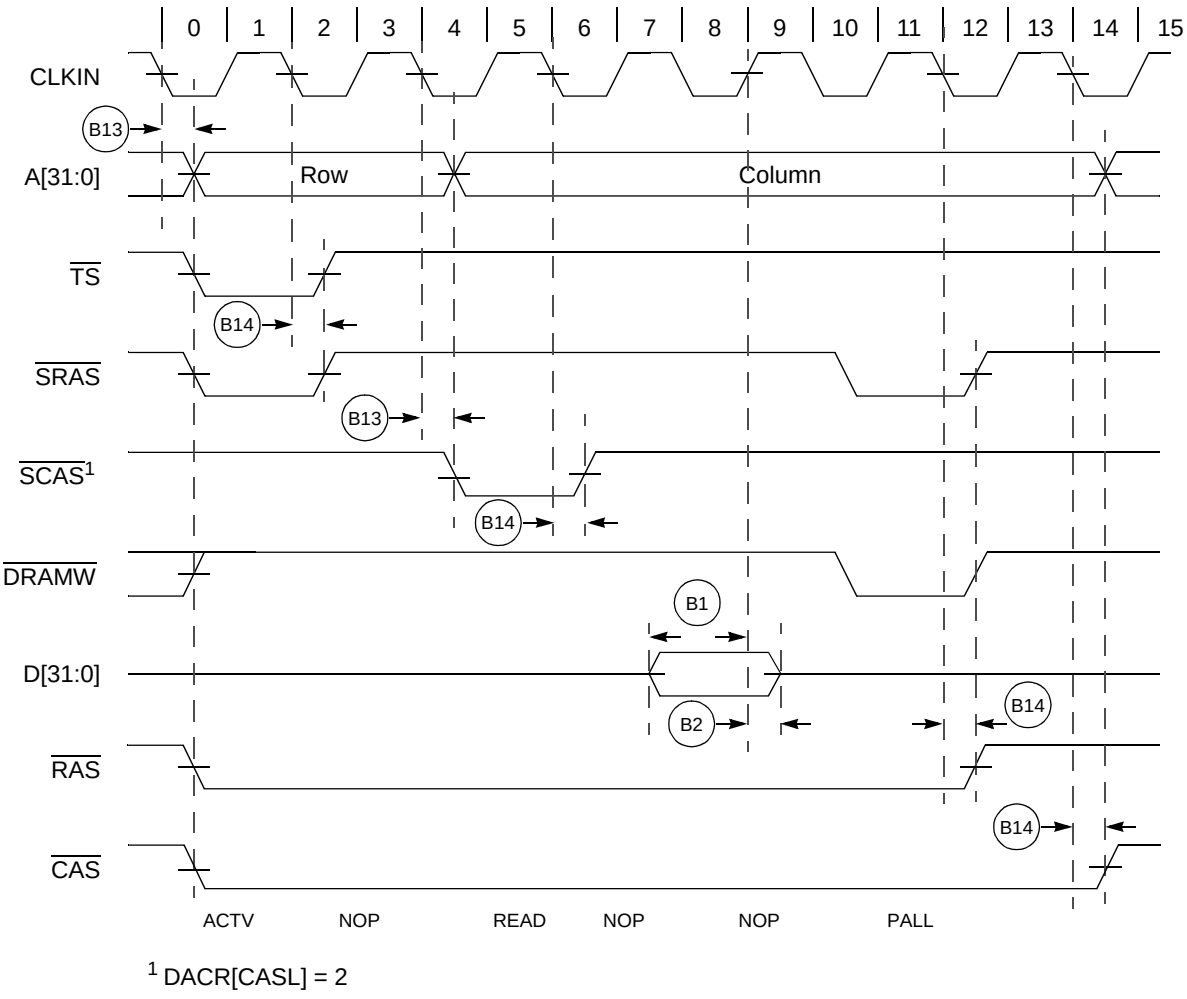


Figure 20-10. SDRAM Write Cycle with EDGESEL Tied High

Figure 20-11 shows an SDRAM read cycle with EDGESEL tied low.



[1] DACR[CASL] = 2

Figure 20-11. SDRAM Read Cycle with EDGESEL Tied Low

Figure 20-12 shows an SDRAM write cycle with EDGESEL tied low.

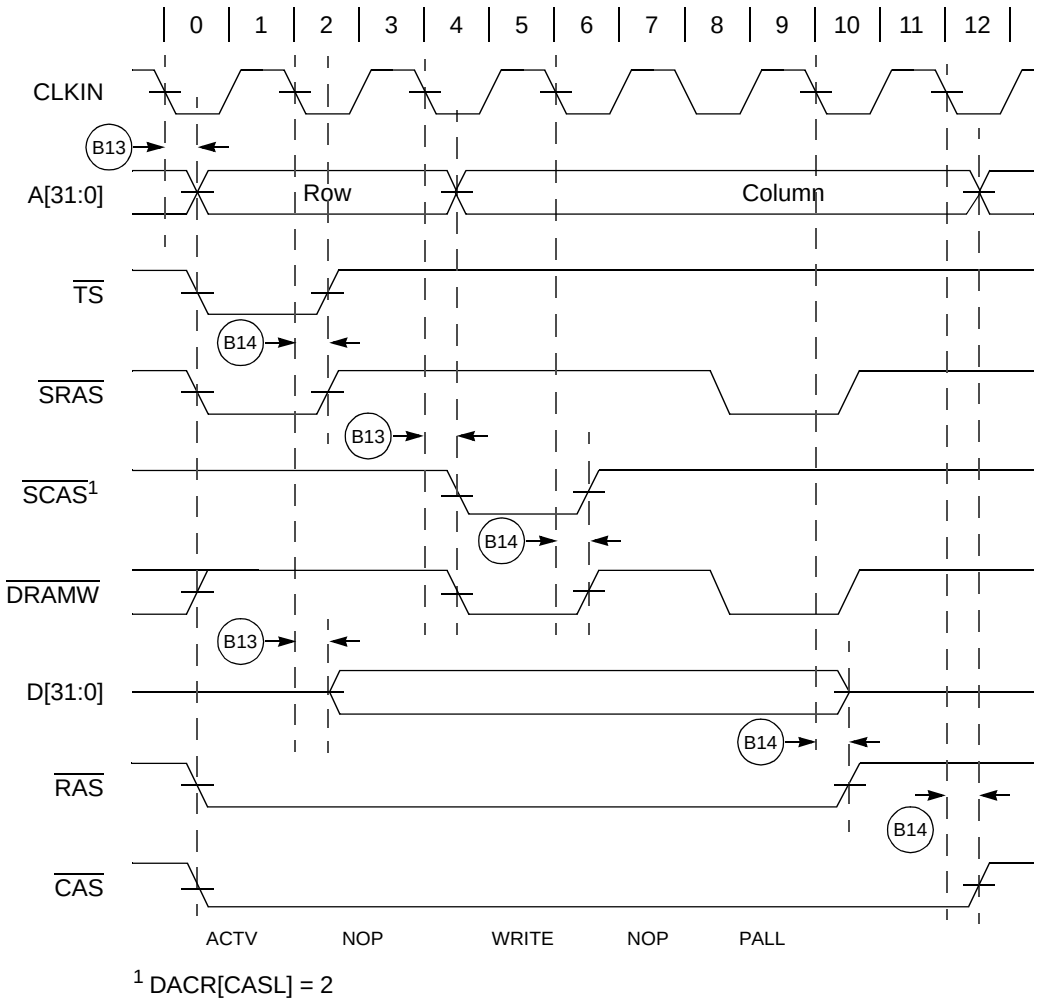


Figure 20-12. SDRAM Write Cycle with EDGESEL Tied Low

Figure 20-13 shows AC timing showing high impedance.

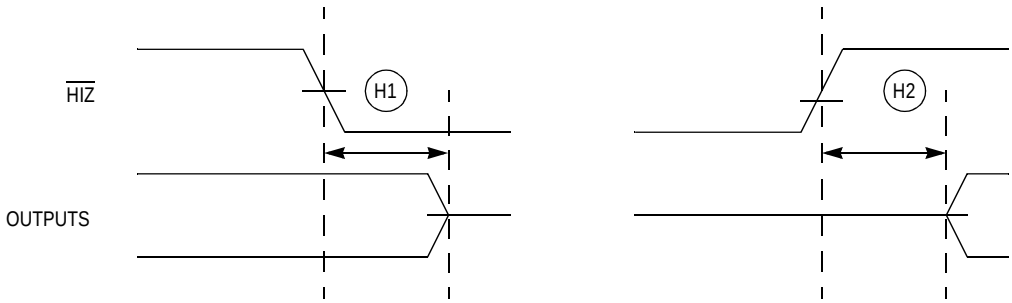


Figure 20-13. AC Output Timing—High Impedance

20.4 Reset Timing Specifications

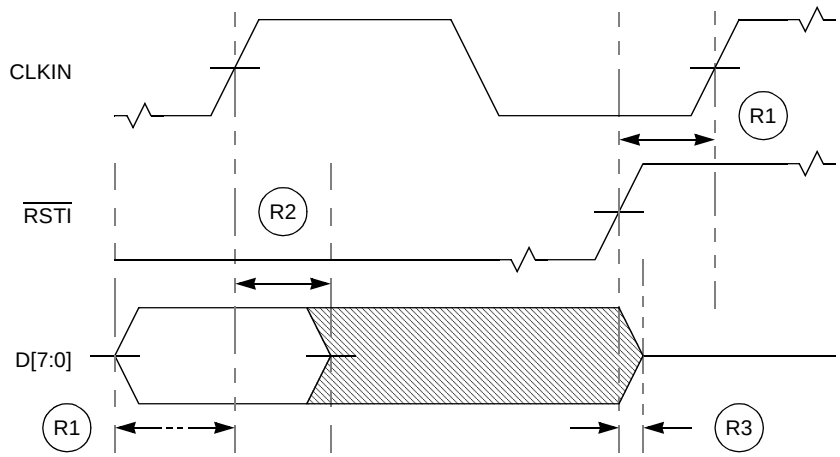
Table 20-9 lists specifications for the reset timing parameters shown in Figure 20-14.

Table 20-9. Reset Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
R1 [1]	Valid to CLKIN (setup)	7.5	—	7.5	—	nS
R2	CLKIN to invalid (hold)	1.0	—	1.0	—	nS
R3	$\overline{\text{RSTI}}$ to invalid (hold)	1.0	—	1.0	—	nS

[1] $\overline{\text{RSTI}}$ and D[7:0] are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 20-14 shows reset timing for the values in Table 20-9.



Note: Mode selects are registered on the rising CLKIN edge before the cycle in which $\overline{\text{RSTI}}$ is recognized as being negated.

Figure 20-14. Reset Timing

20.5 Debug AC Timing Specifications

Table 20-10 lists specifications for the debug AC timing parameters shown in Figure 20-16.

Table 20-10. Debug AC Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
D1	PSTDDATA to PSTCLK setup	—	4.5	—	3	nS
D2	PSTCLK to PSTDDATA hold	—	4.5	—	3	nS
D3	DSI-to-DSCLK setup	1	—	1	—	PSTCLKs
D4 [1]	DSCLK-to-DSO hold	4	—	4	—	PSTCLKs
D5	DSCLK cycle time	5	—	5	—	PSTCLKs

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 20-15 shows real-time trace timing for the values in Table 20-10.

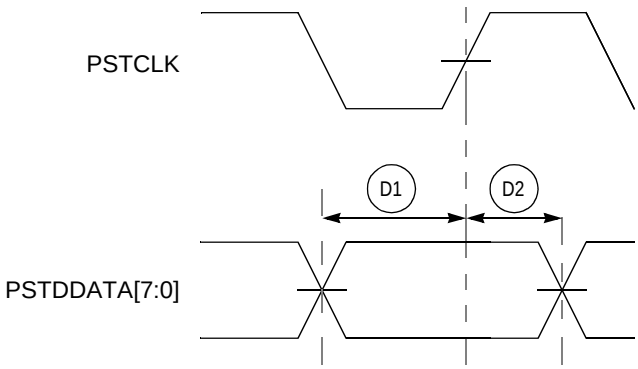


Figure 20-15. Real-Time Trace AC Timing

Figure 20-16 shows BDM serial port AC timing for the values in Table 20-10.

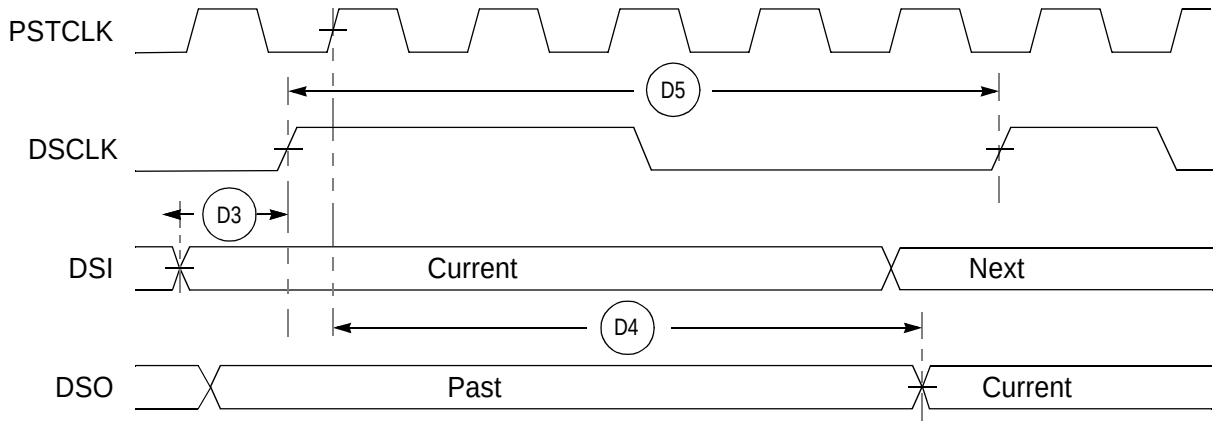


Figure 20-16. BDM Serial Port AC Timing

20.6 Timer Module AC Timing Specifications

Table 20-11 lists specifications for timer module AC timing parameters shown in Figure 20-17.

Table 20-11. Timer Module AC Timing Specification

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
T1	TIN cycle time	3	—	3	—	Bus clocks
T2	TIN valid to CLKIN (input setup)	7.5	—	7.5	—	nS
T3	CLKIN to TIN invalid (input hold)	1.0	—	1.0	—	nS
T4	CLKIN to TOUT valid (output valid)	—	12	—	12	nS
T5	CLKIN to TOUT invalid (output hold)	1.0	—	1.0	—	nS
T6	TIN pulse width	1	—	1	—	Bus clocks
T7	TOUT pulse width	1	—	1	—	Bus clocks

Figure 20-17 shows timings for Table 20-11.

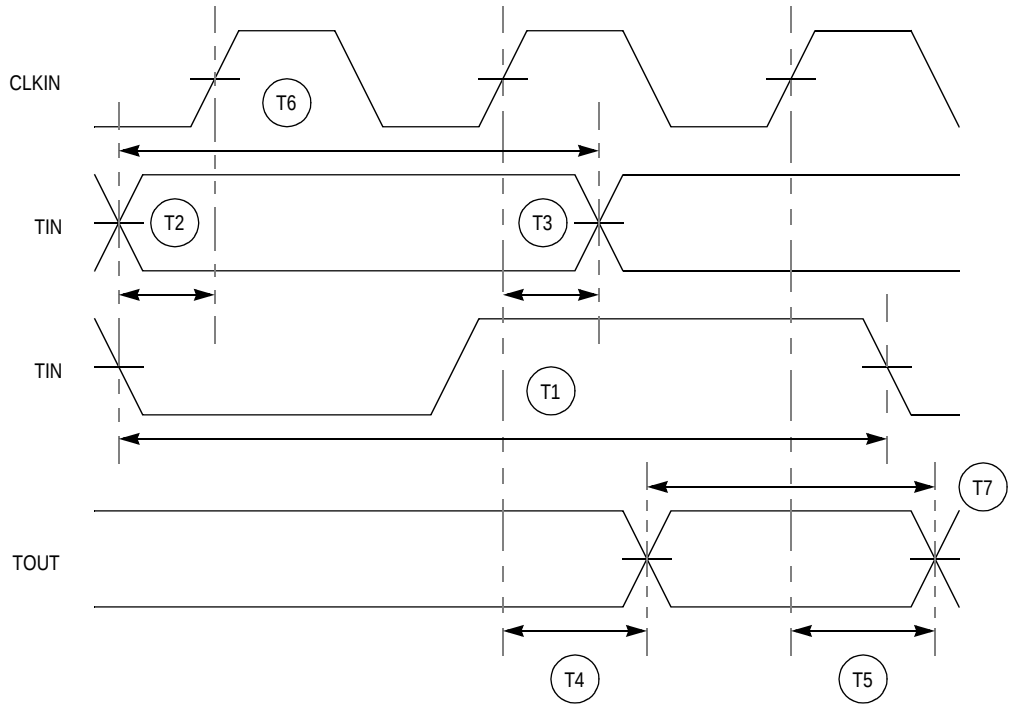


Figure 20-17. Timer Module AC Timing

20.7 I²C Input/Output Timing Specifications

Table 20-12 lists specifications for the I²C input timing parameters shown in Figure 20-18.

Table 20-12. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
I1	Start condition hold time	2	—	2	—	Bus clocks
I2	Clock low period	8	—	8	—	Bus clocks
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	—	1	mS
I4	Data hold time	0	—	0	—	nS
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	—	1	mS
I6	Clock high time	4	—	4	—	Bus clocks
I7	Data setup time	0	—	0	—	nS
I8	Start condition setup time (for repeated start condition only)	2	—	2	—	Bus clocks
I9	Stop condition setup time	2	—	2	—	Bus clocks

Table 20-13 lists specifications for the I²C output timing parameters shown in Figure 20-18.

Table 20-13. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
I1 [1]	Start condition hold time	6	—	6	—	Bus clocks
I2[1]	Clock low period	10	—	10	—	Bus clocks
I3 [2]	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	Note 2	Note 2	Note 2	Note 2	
I4 [1]	Data hold time	7	—	7	—	Bus clocks
I5 [3]	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	—	3	nS
I6 [1]	Clock high time	10	—	10	—	Bus clocks
I7 [1]	Data setup time	2	—	2	—	Bus clocks
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	20	—	Bus clocks
I9 [1]	Stop condition setup time	10	—	10	—	Bus clocks

1 Programming IFDR with the maximum frequency (IFDR = 0x20) results in the minimum output timings listed here. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 20-18 shows timing for the values in Table 20-12 and Table 20-13.

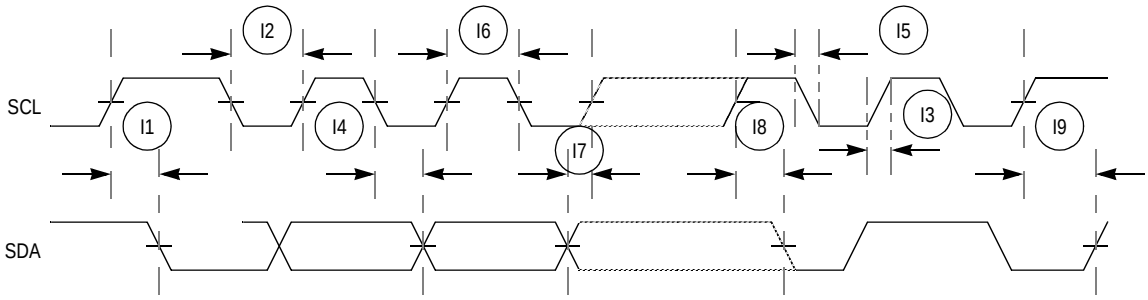


Figure 20-18. I^2C Input/Output Timings

20.8 UART Module AC Timing Specifications

Table 20-14 lists specifications for UART module AC timing parameters in Figure 20-19.

Table 20-14. UART Module AC Timing Specifications

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
U1	RXD valid to CLKIN (input setup)	7.5	—	7.5	—	nS
U2	CLKIN to RXD invalid (input hold)	1.0	—	1.0	—	nS
U3	$\overline{CTS}$ valid to CLKIN (input setup)	7.5	—	7.5	—	nS
U4	CLKIN to $\overline{CTS}$ invalid (input hold)	1.0	—	1.0	—	nS
U5	CLKIN to TXD valid (output valid)	—	12	—	12	nS
U6	CLKIN to TXD invalid (output hold)	1.0	—	1.0	—	nS
U7	CLKIN to $\overline{RTS}$ valid (output valid)	—	12	—	12	nS
U8	CLKIN to $\overline{RTS}$ invalid (output hold)	1.0	—	1.0	—	nS
U9	$\overline{CTS}$ high time	38	—	38	—	nS
U10	$\overline{CTS}$ low time	38	—	38	—	nS
U11	$\overline{CTS}$ rising to TxD valid	—	20	—	20	nS
U12	RxD setup to $\overline{CTS}$ falling	10	—	10	—	nS
U13	RxD hold from $\overline{CTS}$ falling	—	5	—	5	nS
U14	TxD to RxD (remote loop back)	—	15	—	15	nS
U15	TIN1 setup to $\overline{CTS}$ falling	10	—	10	—	nS
U16	TIN1 hold from $\overline{CTS}$ falling	—	5	—	5	nS
U17	$\overline{CTS}$ rising to $\overline{RTS}$ asserted	—	20	—	20	nS

Figure 20-19 shows UART0 and UART1 timing for the values in Table 20-14.

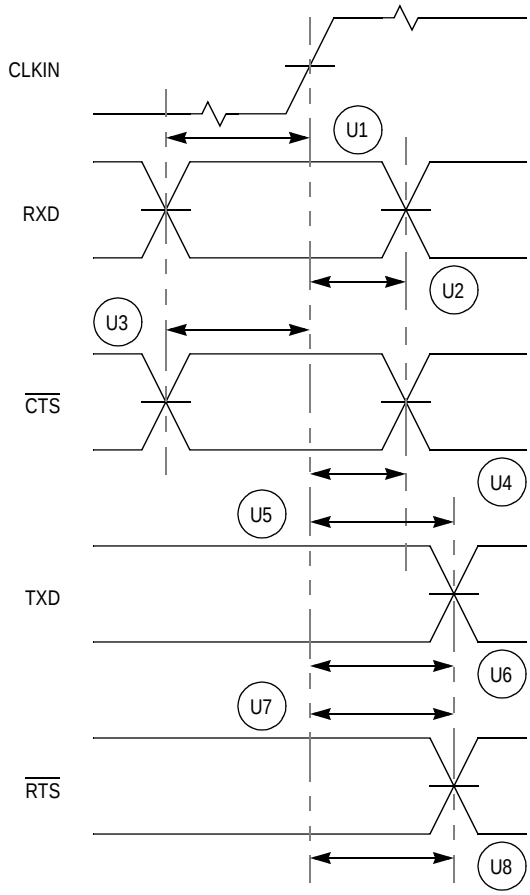


Figure 20-19. UART0 and UART1 Module AC Timing—UART Mode

Figure 20-19 shows timing for UART1 in 8- and 16-bit CODEC mode.

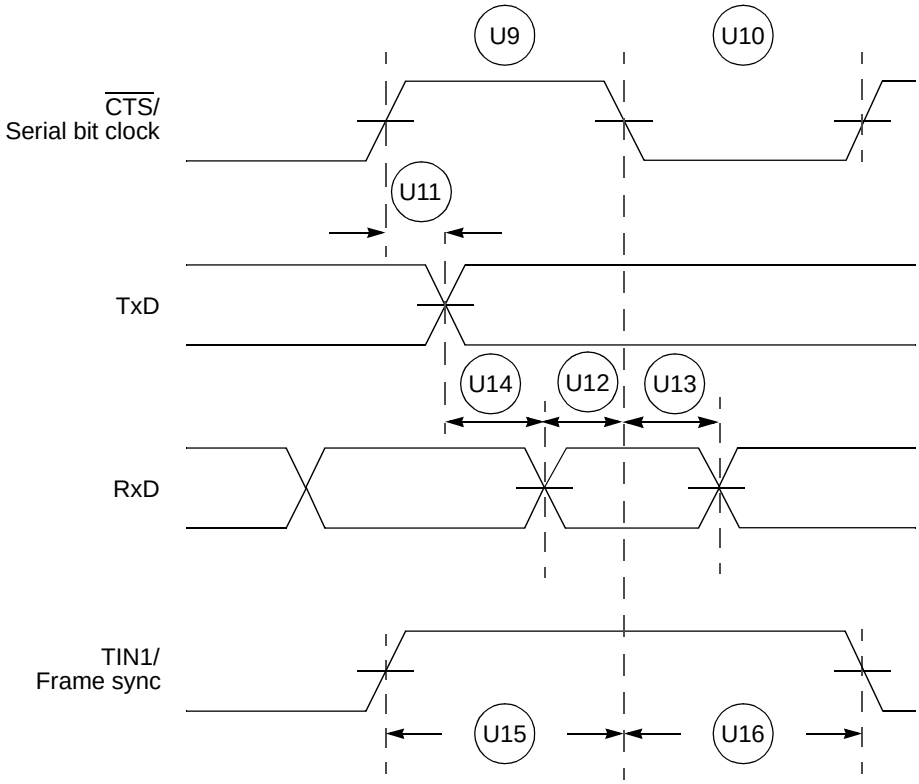


Figure 20-20. UART1 in 8- and 16-bit CODEC Mode

Figure 20-21 shows timing for UART1 in AC ‘97 mode.

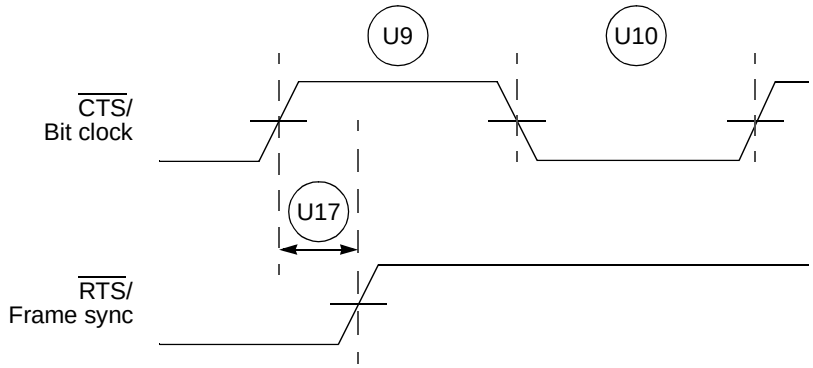


Figure 20-21. UART1 in AC ‘97 Mode

20.9 Parallel Port (General-Purpose I/O) Timing Specifications

Table 20-15 lists specifications for general-purpose I/O timing parameters in Figure 20-22.

Table 20-15. General-Purpose I/O Port AC Timing Specifications

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
P1	PP valid to CLKIN (input setup)	7.5	—	7.5	—	nS
P2	CLKIN to PP invalid (input hold)	1.0	—	1.0	—	nS
P3	CLKIN to PP valid (output valid)	—	12.5	—	12.5	nS
P4	CLKIN to PP invalid (output hold)	1.0	—	1.0	—	nS

Figure 20-22 shows general-purpose I/O timing.

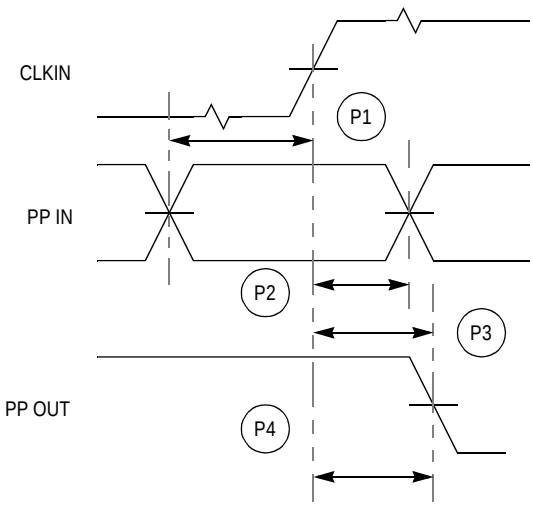


Figure 20-22. General-Purpose I/O Timing

20.10 DMA Timing Specifications

Table 20-15 lists specifications for DMA timing parameters shown in Figure 20-22.

Table 20-16. DMA AC Timing Specifications

Num	Characteristic	162 MHz		220 MHz		Units
		Min	Max	Min	Max	
M1	DREQ valid to CLKIN (input setup)	7.5	—	7.5	—	nS
M2	CLKIN to DREQ invalid (input hold)	1.0	—	1.0	—	nS
M3	CLKIN to DACK valid (output valid)	—	10	—	10	nS
M4	CLKIN to DACK invalid (output hold)	1.0	—	1.0	—	nS

Figure 20-23 shows DMA AC timing.

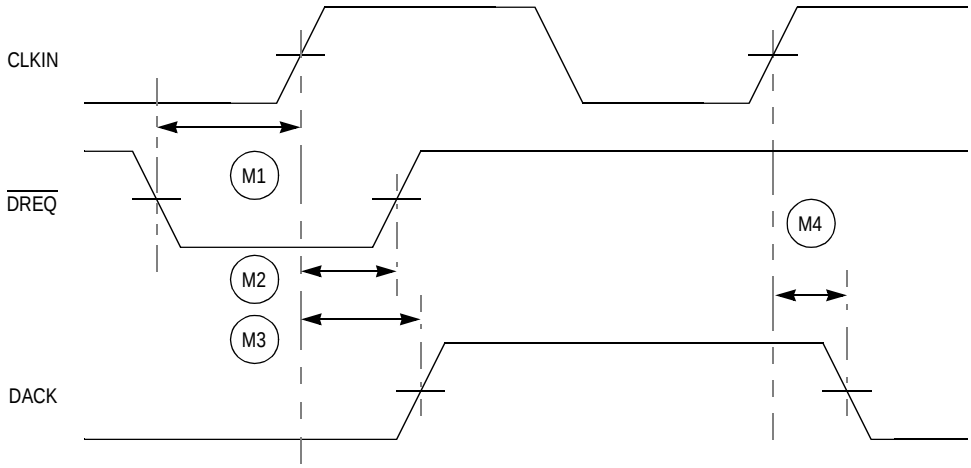


Figure 20-23. DMA Timing

20.11 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 20-17 lists specifications for JTAG AC timing parameters shown in Figure 20-24.

Table 20-17. IEEE 1149.1 (JTAG) AC Timing Specifications

Num	Characteristic	All Frequencies		Units
		Min	Max	
—	TCK frequency of operation	0	10	MHz
J1	TCK cycle time	100	—	nS
J2a	TCK clock pulse high width (measured at 1.5 V)	40	—	nS
J2b	TCK clock pulse low width (measured at 1.5 V)	40	—	nS
J3a	TCK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5V)	—	5	nS
J3b	TCK rise time (V_{IL} = 0.5v to V_{IH} = 2.4V)	—	5	nS
J4	TDI, TMS to TCK rising (input setup)	10	—	nS
J5	TCK rising to TDI, TMS invalid (hold)	15	—	nS
J6	Boundary scan data valid to TCK (setup)	10	—	nS
J7	TCK to boundary-scan data invalid (hold)	15	—	nS
J8	$\overline{\text{TRST}}$ pulse width (asynchronous to clock edges)	15	—	—
J9	TCK falling to TDO valid (signal from driven or three-state)	—	30	nS
J10	TCK falling to TDO high impedance	—	30	nS
J11	TCK falling to boundary scan data valid (signal from driven or three-state)	—	30	nS
J12	TCK falling to boundary scan data high impedance	—	30	nS

Figure 20-24 shows JTAG timing.

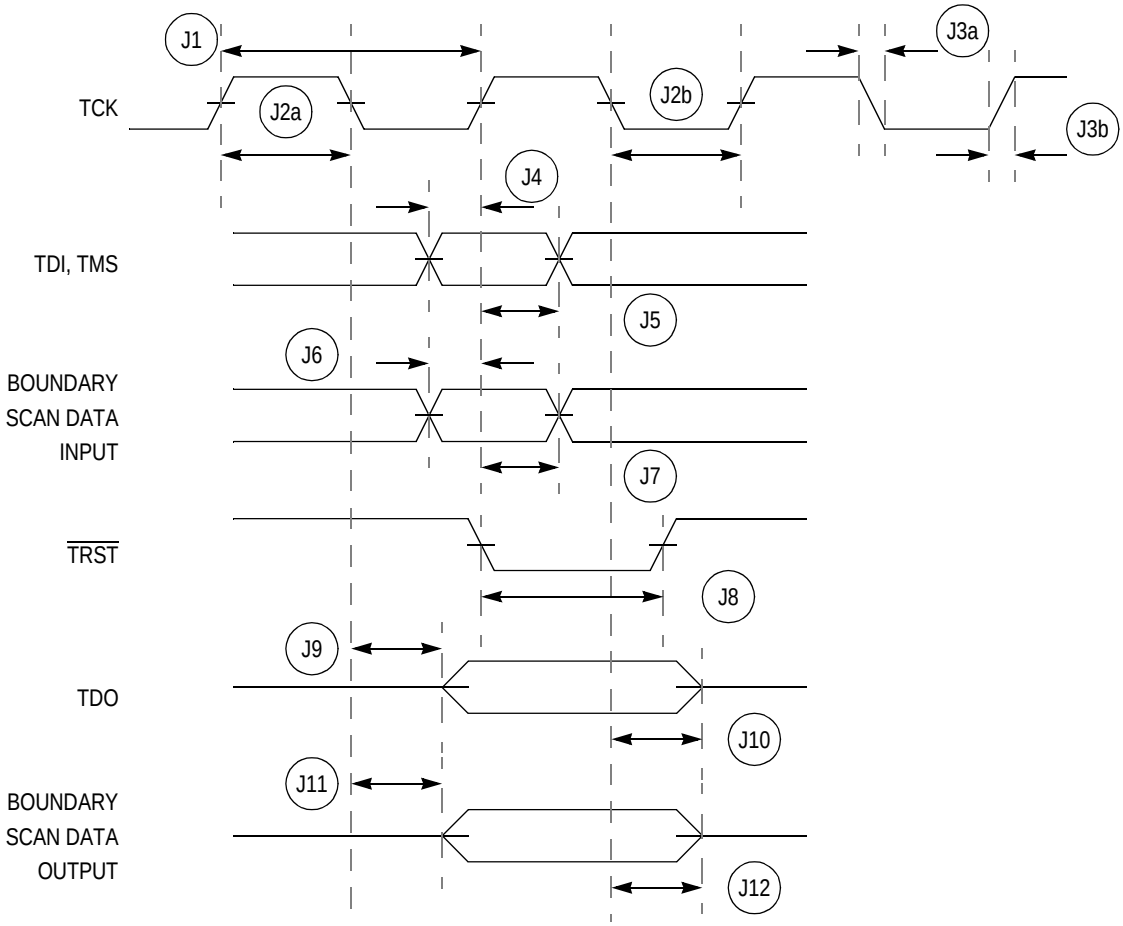


Figure 20-24. IEEE 1149.1 (JTAG) AC Timing

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