DigiAudio

Digital Audio Development and I/O Board

User Manual

coreworks, lda
http://www.coreworks.pt

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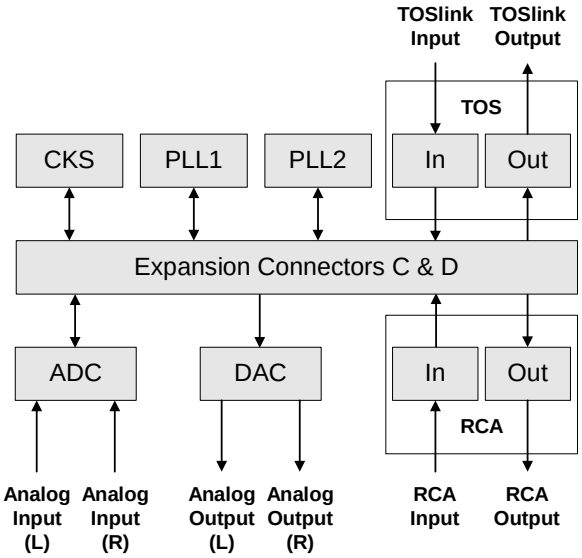
Block Diagram of the DigiAudio Board



FEATURES

- **Designed to mate with Coreworks FPGA BasicBoard (FPGA Development and Evaluation Board) by means of two 40-pin expansion connectors.**
- **Uses a standard ATX power supply.**
- **Supports SPDIF-AES/EBU and ADAT interface formats.**
- **One input/output pair of digital optical connectors (TOS) for SPDIF-AES/EBU or ADAT digital interface signals.**
- **One input/output pair of digital RCA connectors for unbalanced SPDIF-AES/EBU digital interface signals.**
- **One DAC circuit featuring 24-bit/192-kHz CS4396 DAC chips with interface circuits for unbalanced RCA outputs.**
- **One ADC circuit featuring 24-bit/96-kHz CS5333 ADC chips, with respective external circuitry, and interface to unbalanced RCA inputs.**
- **Two PLL circuits featuring high performance TLC2932 chips for clock synthesis, clock recovery, jitter rejection, etc.**
- **One MPEG audio clock synthesizer (MK1412) for supporting the most common sample rates: 32, 44.1, 48, 88.2, 96 and 192 kHz.**
- **Applications: CD, SACD, DVD and DVD audio circuits, digital audio standard I/O interfaces, format converters, sample rate converters, audio effects processors, etc.**

DESCRIPTION

The DigiAudio Digital Audio Development Board is designed to mate with the Coreworks FPGA Development and Evaluation Board, BasicBoard.

The DigiAudio board provides an assortment of the most frequently used consumer and professional audio I/O interfaces and physical connectors, both analog and digital. A simplified layout of the board is shown in Figure 1.

DigiAudio contains a clock synthesizer for producing master clocks for the most commonly used sample rates in digital audio: 32, 44.1, 48, 88.2, 96 and 192 kHz. It also has two PLL circuits that can be used for clock recovery, jitter rejection, etc., in a variety of applications.

Together with BasicBoard, which features a Xilinx XC2S300E-6PQ208 FPGA, the DigiAudio board can be used to implement projects ranging from simple digital audio interfaces to complete systems for digital audio signal processing of complexity up to 300K system gates. Implementing systems with an FPGA platform offers extreme flexibility and greatly speeds up the development time. FPGAs can be used to prototype a system, or even be used competitively in the final system if the production volumes are low. Moreover, FPGAs are becoming the solution of choice for systems that require field re-programmability.

This document describes the circuits and input/output interfaces in the DigiAudio board. When needed, manufacturer part numbers are provided so that further reference material can be obtained from their websites.

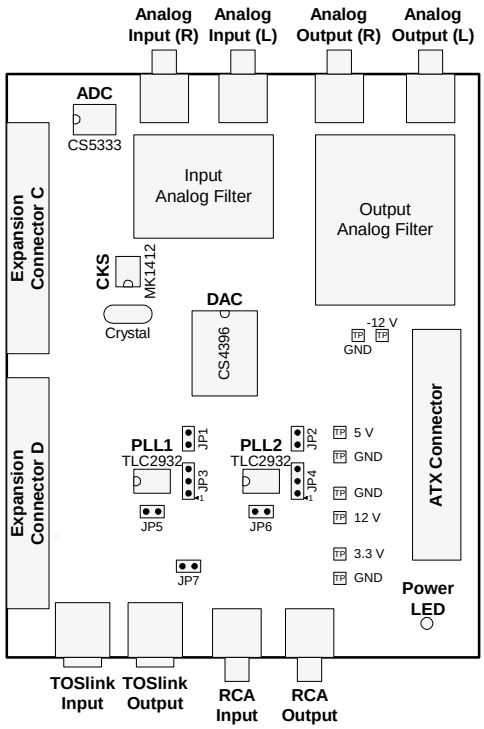


Figure 1: Simplified layout of the DigiAudio Board.

POWER SUPPLY

DigiAudio uses a standard ATX socket to connect to a standard ATX power supply. The variety of analog and digital ICs that are present in DigiAudio demands the following DC supply voltages: 3.3, 5 and ±12 V. The 5 and ±12 V voltages are provided by the ATX power supply. When the BasicBoard and the DigiAudio boards are connected, the 3.3 V voltage is provided by BasicBoard in pin C03 of expansion connector C.

The board is properly powered when Power LED is turned on.

JUMPER SETTINGS

The DigiAudio board includes 7 jumpers (3 jumpers to control the PLL1 operation, 3 jumpers to control the PLL2 operation and 1 jumper for the RCA circuit). The purpose of each jumper is described in Table 1 and Table 2. Their default arrangement is also shown in the tables.

PLL1	PLL2	DESCRIPTION	DEFAULT
JP1	JP2	VCO inhibit control. A jumper must be inserted for normal operation of the VCO. When the jumper is not present, VCOx_OUT remains low.	ON
JP3	JP4	When the jumper is not present, the external loop filter input is floating. When a jumper is inserted between positions 1 and 2, PFD OUT is connected to the Loop Filter input (regular PLL mode). When the jumper is inserted between positions 2 and 3, the Loop Filter is controlled by the FPGA (VCO mode).	ON between positions 1 and 2
JP5	JP6	VCO output frequency select. When jumper is not present, the VCOx_OUT frequency is divided by 2; when jumper is present, the VCOx_OUT frequency is unchanged.	ON

Table 1: Jumpers for PLL control.

RCA	DESCRIPTION	DEFAULT
JP7	When the jumper is not present, the RCA input signal is disconnected	ON

Table 2: Jumper for the RCA input control.

MPEG AUDIO CLOCK SYNTHESIZER (CKS)

The DigiAudio board has an MPEG Audio Clock Synthesizer to generate master clocks for the most commonly used sample frequencies in digital audio: 32, 44.1, 48, 88.2, 96 and 192 kHz. The IC used is the MK1412 from ICS, Inc., which produces master clock frequencies that are

256 and 512 times faster than the sample rate frequencies mentioned (Figure 2). For more information on this chip please refer to the manufacturer website at http://www.ics.com. The signals of the MK1412 that can be observed/controlled by the FPGA are connected to expansion connector C and listed in Table 3.

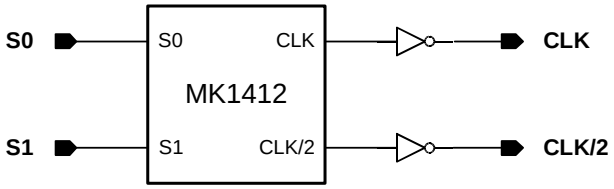


Figure 2: Block diagram of the MPEG Audio Clock Synthesizer.

SIGNAL	DESCRIPTION
CLK	Audio Clock: its frequency is 512x the sample rate.
CLK/2	Audio Clock Divided by 2: its frequency is 256x the sample rate.
S0, S1	Frequency Select Bits: determines *CLK* and *CLK/2* according to Table 4.

Table 3: Audio clock synthesizer interface signals.

S1	S0	CLK	CLK/2	ACCURACY
0	0	16.384	8.192	1 ppm
0	1	22.5792	11.2896	25 ppm
1	0	24.576	12.288	1 ppm
1	1	49.152	24.576	1 ppm

Table 4: MK1412 frequency selection.

PLL CIRCUITS (PLL1 and PLL2)

DigiAudio has 2 Phase Locked Loop (PLL) circuits that can be used by the digital audio circuits and systems implemented in the FPGA. Typical applications include clock recovery, clock synthesis and jitter rejection. The ICs used are the TLC2932 from Texas Instruments, Inc. More information on these chips can be found at the manufacturers website at http://www.ti.com.

PLL1 has R_{BIAS} = 3.3 kΩ (see the TLC2932 datasheet), in order to be better able to synchronize with the master clocks (256x or 512x) of the highest sample frequencies: 88.2, 96 and 192 kHz. PLL2 has R_{BIAS} = 1.5 kΩ to better synchronize with the master clocks of the lowest sample frequencies: 32, 44.1 and 48 kHz.

The block diagram of the PLL circuits is shown in Figure 3. The jumper purpose is described in the section “Jumper Settings” above. The signals of the TLC2932 are connected to the FPGA via the expansion connectors described in Table 5.

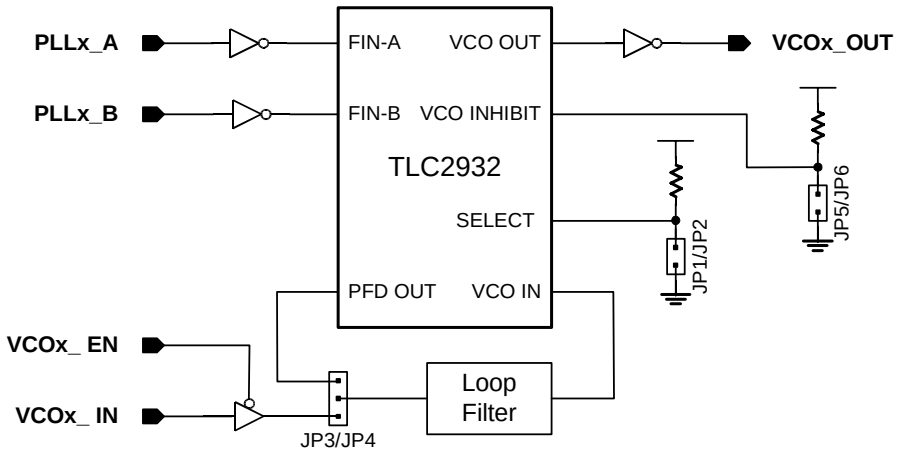


Figure 3: Block diagram of the PLL circuits.

SIGNAL	DESCRIPTION
PLLx_A	Reference input frequency.
PLLx_B	Feedback from external counter (in FPGA) used to divide the frequency of VCOx_OUT by a factor of N.
VCOx_OUT	VCO output.
VCOx_EN	Controls a tri-state buffer whose input is the VCOx_IN signal.
VCOx_IN	VCO control voltage input. The external loop filter input is connected to the FPGA. Jumpers JP3 or JP4 must be inserted between positions 2 and 3 (see Table 1). In this operation mode, the output of the Phase Frequency Detector (PFD) is floating. Inputs FIN-A and FIN-B do not control the VCO frequency.

Table 5: PLL interface signals.

TOS CIRCUITS

The DigiAudio board has 2 Thermal Optical Switch (TOS) circuits equipped with optical connectors for receiving (*TOS_IN*) and sending out (*TOS_OUT*) digital optical signals using fiber cables (see Figure 4). Optical connections are common in digital audio equipment because of their reliability and immunity to electrical effects such as noise and parasitic effects that may cause signal degradation. The signals of the TOS circuits that are connected to the FPGA via the expansion connector D are listed in Table 6.

Figure 4: Block diagram of the TOS circuits.

SIGNAL	DESCRIPTION
TOS_IN	Signal received from the optical fiber cable.
TOS_OUT	Signal to be transmitted in the optical fiber cable.

Table 6: TOS interface signals.

RCA CIRCUITS

The DigiAudio board has 2 RCA circuits for receiving (*RCA_IN*) and sending out (*RCA_OUT*) digital electrical signals using 75 Ω coaxial cables (see Figure 4). RCA cables have long been used for analog audio and video, and are now being widely used for conveying digital audio signals. The signals of the RCA circuits that are connected to the FPGA via the expansion connector D are described in Table 7.

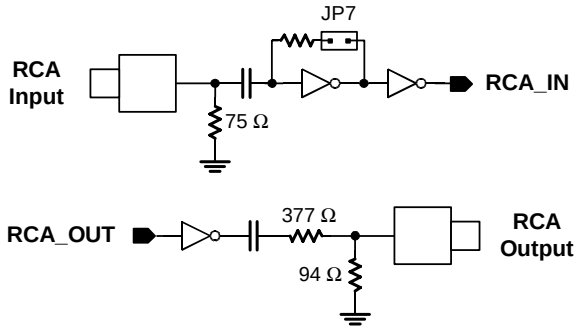


Figure 5: Block diagram of the RCA circuits.

SIGNAL	DESCRIPTION
RCA_IN	Signal received from the coaxial cable. Jumper JP7 must be inserted for proper operation.
RCA_OUT	Signal to be transmitted in the coaxial cable.

Table 7: RCA interface signals.

DAC CIRCUIT

The DigiAudio board has one stereo Digital-to-Analog Converter (DAC) circuit to produce high quality analog signals for audio reproduction. The DAC circuit produces a pair of analog outputs, *Analog Output (L)* and *Analog Output (R)*. The block diagram of the DAC circuit is presented in Figure 6.

The DAC circuit contains a CS4396 chip from Cirrus Logic, Inc., whose main features are:

- 24-bit resolution
- Up to 192KHz sample rates
- 120 dB dynamic range
- –100dB total harmonic distortion plus noise (THD+N)

For more information on the CS4396 chip, please refer to the manufacturer's datasheet at http://www.cirrus.com.

The DAC circuit provides an analog consumer audio unbalanced output using RCA connectors. The signals of the CS4396 that can be observed/controlled by the FPGA are connected to expansion connector C. The most relevant signals are described in Table 8.

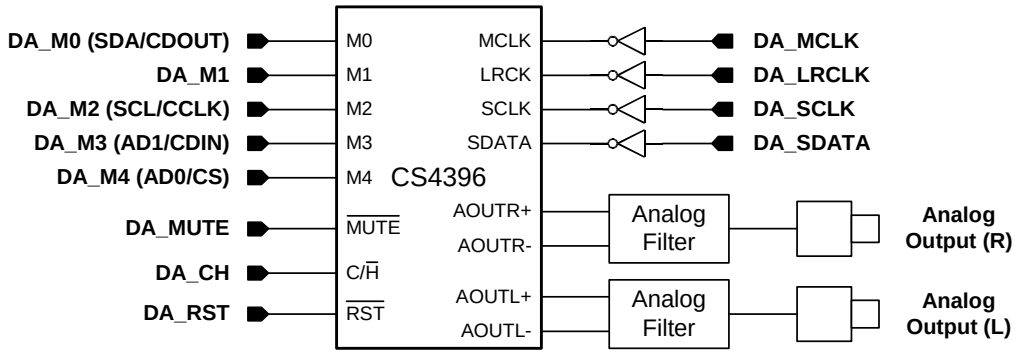


Figure 6: Block diagram of the DAC circuit.

SIGNAL	DESCRIPTION
DA_RST	Reset signal.
DA_MCLK	Master Clock: its frequency is usually 256x, 384x, 512x or 768x the input sample rate, though other multiply factors are also possible.
DA_SCLK	Serial Clock: used for clocking individual bits of serial data into the *SDATA* pin. The required relationship between *SCLK*, *LRCK* and *SDATA* is defined by the *M4* down to *M0* pins.
DA_LRCLK	The Left/Right clock determines which channel is currently being output to *SDATA*. The frequency of *LRCK* is the sample rate frequency. The required relationship between *SCLK*, *LRCK* and *SDATA* is defined by the *M4* down to *M0* pins.
DA_SDATA	Serial Audio Data: 2's complement MSB-first serial data. The data is clocked into *SDATA* by the serial clock *SCLK* and the channel is selected by the Left/Right clock *LRCK*.
DA_MUTE	Soft Mute: the analog outputs will ramp to a muted state when enabled.
DA_CH	Control Port/Hardware Mode Select Pin (C/$\overline{H}$): determines if the device will operate in the Hardware Mode or the Control Port Mode. See the explanation below.

Table 8: DAC interface signals.

The Hardware Mode is selected when DA_CH = 0. In this mode, the inputs DA_M0 to DA_M4 provide a simple interface to configure the CS4396 chip. Table 9 describes the main options controlled in the Hardware Mode.

HARDWARE MODE

SIGNAL	DESCRIPTION
DA_M0 to DA_M4	Mode Select: the mode select pins determine the operation mode of the device as detailed in the CS4396 datasheet. The options include: ▪ Selection of the Digital Interface Format that determines the relationship among the SCLK, SDATA and SDATA signals. ▪ Selection of the standard digital de-emphasis filter. ▪ Selection of the appropriate clocking mode to match the input samples. ▪ Selection of the appropriate clocking mode to match the input samples.

Table 9: CS4396 Hardware Mode.

The Control Port Mode is selected when DA_CH = 1. Compared to Hardware Mode, the Control Port Mode provides access to additional operation modes, but a more complex interface is required. Table 10 describes the control signals.

The control port is used to load all the internal settings of the CS4396. The operation of the control port may be completely asynchronous to the audio sample rate.

The control port has 2 modes: SPI and I^2C, with the CS4396 operating as a slave device in both modes. If I^2C operation is desired, AD0/CS should be tied to VD or DGND. If the CS4396 ever detects a high to low transition on AD0/CS after power-up, SPI mode will be selected.

CONTROL PORT MODE

SIGNAL	DESCRIPTION
AD0/CS	Address Bit 0/Chip Select: in I^2C mode, *AD0* is a chip address bit; in SPI mode, *CS* is the enable of the control port interface. This pin is the same pin as the *DA_M4* pin in the Hardware Mode.
AD1/CDIN	Address bit 1/Control Data Input: in I^2C mode, *AD0* is a chip address bit; in SPI mode, *CDIN* is the control data input line of the control port interface. This pin is the same pin as the *DA_M3* pin in the Hardware Mode.
SCL/CCLK	Serial Control Interface Clock: in I^2C mode, *SCL* clocks the serial control data into or from the *SDA/CDOUT* signal; in SPI mode, *CDIN* is the control data input line of the control port interface. This pin is the same pin as the *DA_M2* pin in the Hardware Mode.
SDA/CDOUT	Serial Control Data Input/Output: in I^2C mode, *SCA* is the data I/O; in SPI mode, *CDOUT* is the control data output line of the control port interface. This pin is the same pin as the *DA_M0* pin in the Hardware Mode.
DA_M1	Select: this pin is not used in the Control Port Mode, and should be set to low.

Table 10: CS4396 Control Port Mode.

ADC CIRCUIT

The DigiAudio board has one stereo Analog-to-Digital Converter circuit to produce high quality digital signals for audio processing or recording. The ADC circuit has a pair of analog inputs, *Analog Input (L)* and *Analog Input (R)*. The block diagram of the ADC circuit is presented in Figure 7.

The IC used is the CS5333 from Cirrus Logic, Inc., whose main features are:

- 24-bit resolution
- Up to 96KHz sample rates
- 98 dB dynamic range
- –88 dB total harmonic distortion plus noise (THD+N)

For more information on the CS5333 IC, please refer to the manufacturer's datasheet at http://www.cirrus.com.

The ADC circuit provides an analog consumer audio unbalanced input using RCA connectors. The signals of the CS4396 that can be observed/controlled by the FPGA are connected to expansion connector C. The relevant signals are listed in Table 11.

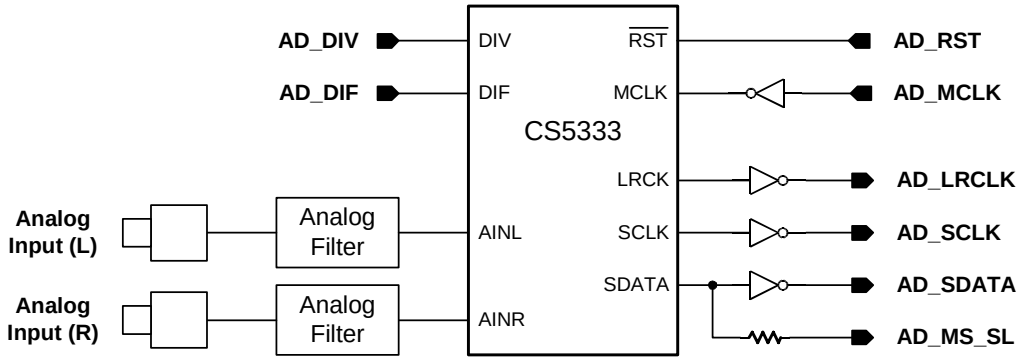


Figure 7: Block diagram of the ADC circuit.

SIGNAL	DESCRIPTION
AD_RST	Reset signal.
AD_MCLK	Master Clock: its frequency is usually *MCLK* is 256x, 384x, 512x, 768x or 1024x the input sample rate, though other multiply factors are also possible.
AD_SCLK	Serial Clock: used for clocking individual bits of serial data out of the *SDATA* pin. The required relationship between *SCLK*, *LRCK* and *SDATA* is defined by the *DIF* pin, as explained below.
AD_SDATA	Serial Audio Data: 2's complement MSB-first serial data. The data is clocked into *SDATA* by the serial clock *SCLK* and the channel is selected by the Left/Right clock *LRCK*.
AD_MS_SL	Master/Slave Select: selects Master (high) or Slave (low) operation.

AD_LRCLK	Left/Right Clock: determines which channel is currently being output on *SDATA.* The frequency of *LRCK* is the sample rate frequency. The required relationship between *SCLK*, *LRCK* and *SDATA* is defined by the *DIF* pin, as explained below.
AD_DIV	MCLK Divide Enable. This pin serves different functions in Master or Slave modes. In Master mode: when high, High Rate Mode is defined; when low, Base Rate Mode is defined. In Slave mode: when high, *MCLK* is divided internally by 2; when low, *MCLK* is not changed.
AD_DIF	Digital Interface Format: defines the required relationship between *SCLK*, *LRCK* and *SDATA*. When low, DIF defines the I^2S format up to 24-bit data; when high, DIF defines the Left Justified format up to 24-bit data.

Table 11: ADC interface signals.

EXPANSION CONNECTORS (Connector C and Connector D)

The DigiAudio board has two expansion connectors to mate with BasicBoard. For further information on BasicBoard please download the datasheet from our website at http://www.coreworks.pt/products/BasicBoard.pdf.

The connector pins have a pitch (spacing) of 100 mils (or 2.54 mm). A 3.3 V DC voltage must be provided at pin 3 of connector C (C03) and a reference ground level voltage (GND) must be connected to pin C01. All other pins in connectors C and D are routed directly to the FPGA.

Three pins of the expansion connectors are connected to dedicated FPGA clock pins. The selected DigiAudio clock outputs are:

- Clock output of the Audio Clock Synthesizer circuit (**CLK**)
- VCO output of PLL1 (**VCO1_OUT**)
- VCO output of PLL2 (**VCO2_OUT**)

Table 12 shows the mapping between the FPGA pins and the expansion connectors C and D. The table is organized in two sub-tables, one for connector C and the other for connector D. The table rows correspond to an ordered list of the connector pins, and the four columns give, in the following order, the following information: (1) the connector pin, (2) the signal name, (3) the FPGA pin to which the connector pin is routed to the BasicBoard, and (4) the direction (input/output) of the signal.

Connector C				Connector D			
Pin	**Name**	**FPGA pin**	**Direction**	**Pin**	**Name**	**FPGA pin**	**Direction**
C01	GND	N/C	N/A	D01		45	
C02		N/C	N/A	D02		44	
C03	VDD	N/C	N/A	D03		46	
C04		16		D04		125	
C05	**CLK**	**185**	**O**	D05		122	
C06	CLK/2	17	O	D06		123	
C07		175		D07	PLL1_A	47	I
C08	AD_RST	174	I	D08	PLL1_B	121	I
C09		173		D09		115	
C10	AD_MCLK	169	I	D10		23	
C11	AD_SCLK	168	O	D11		113	
C12	AD_SDATA	167	O	D12	PLL2_A	114	I
C13	AD_LRCLK	166	O	D13	PLL2_B	111	I
C14	AD_MS_SL	165	I	D14		112	
C15	AD_DIV	164	I	D15		109	
C16	AD_DIF	163	I	D16		110	
C17		162		D17		102	
C18		20		D18		48	
C19	**VCO2_OUT**	**182**	**O**	D19		100	
C20		154		D20		101	
C21		152		D21		98	
C22		151		D22		99	
C23	S1	150	I	D23	VCO1_ EN	96	I
C24	S0	149	I	D24	VCO1_ IN	97	I
C25		148		D25	VCO2_ EN	94	I
C26		147		D26	VCO2_ IN	95	I
C27	DA_RST	146	I	D27		89	
C28		21		D28		93	
C29	**VCO1_OUT**	**77**	**O**	D29		87	
C30	DA_M4 (AD0/CS)	140	I	D30		88	
C31	DA_M3 (AD1/CDIN)	139	I	D31		84	
C32	DA_M2 (SCL/CCLK)	138	I	D32		86	
C33	DA_M1	136	I	D33		82	
C34	DA_M0 (SDA/CDOUT)	22	I	D34		83	
C35	DA_MCLK	134	I	D35	RCA_IN	75	O
C36	DA_SCLK	133	I	D36	RCA_OUT	81	I
C37	DA_LRCLK	132	I	D37		73	
C38	DA_SDATA	129	I	D38		74	
C39	DA_CH	127	I	D39	TOS_IN	70	O
C40	DA_MUTE	43	I	D40	TOS_OUT	71	I

Table 12: Pinout of the expansion connectors C and D.