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Design Considerations for Interfacing SDRAM with MC68VZ328

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Contents

The MC68VZ328 (DragonBall™ VZ) adds support for Synchronous DRAM (SDRAM) directly in its DRAM controller. This application note provided information to setup and use the DragonBall VZ to access SDRAM. This application note discusses all aspects of the DragonBall VZ operation as it relates to the SDRAM.

1 Introduction

This application note provides information to users who are preparing to use Synchronous DRAM (SDRAM) with the MC68VZ328.

The following topics are discussed:

1. Physical interface between SDRAM and MC68VZ328
2. Relevant control registers for SDRAM operation in the MC68VZ328 memory controller
3. SDRAM initialization sequences
4. SDRAM power control features
5. SDRAM logic analyzer screen captures

It is assumed that users have a basic understanding of the DragonBall processors and SDRAM operation. A large amount of abbreviations are used throughout this application note. Please refer to MC68VZ328 User's Manual (order number MC68VZ328UM/D) for details if needed.

1.1 Terminology

Unless otherwise specified within the document, the following terms and abbreviation are as defined in Table 1.

Table 1. Terminology

Terms	Description
CPU	The 68K core in the DragonBall processor
LCDC	LCD Controller module in the DragonBall processor
$\overline{\text{UDS}}$	Upper Data Strobe signal from the 68K core, muxed with Port K3 (PK3/$\overline{\text{UDS}}$)
$\overline{\text{SDCS0}}$	SDRAM Chip-select 0, muxed with Port B4 (PB4/$\overline{\text{CSD0}}$/$\overline{\text{CAS0}}$/$\overline{\text{SDCS0}}$)
$\overline{\text{SDCAS}}$	SDRAM CAS signal, muxed with Port B3 (PB3/$\overline{\text{CSC1}}$/$\overline{\text{RAS1}}$/$\overline{\text{SDCAS}}$)
$\overline{\text{SDRAS}}$	SDRAM RAS signal, muxed with Port B2 (PB2/$\overline{\text{CSC0}}$/$\overline{\text{RAS0}}$/$\overline{\text{SDRAS}}$)
$\overline{\text{SDWE}}$	SDRAM Write Enable signal, muxed with Port B1 (PB1/$\overline{\text{CSB1}}$/$\overline{\text{SDWE}}$)
SDCLK	SDRAM Clock signal, muxed with Port M0 (PM0/SDCLK)
SDCE	SDRAM Clock Enable signal, muxed with Port M1 (PM1/SDCE)
SDA10	SDRAM Address Line 10 signal, muxed with Port M4 (PM4/SDA10)

2 Physical Interface Between SDRAM and MC68VZ328

The recommended pin connections between the DragonBall VZ to SDRAM are shown Figure 1.

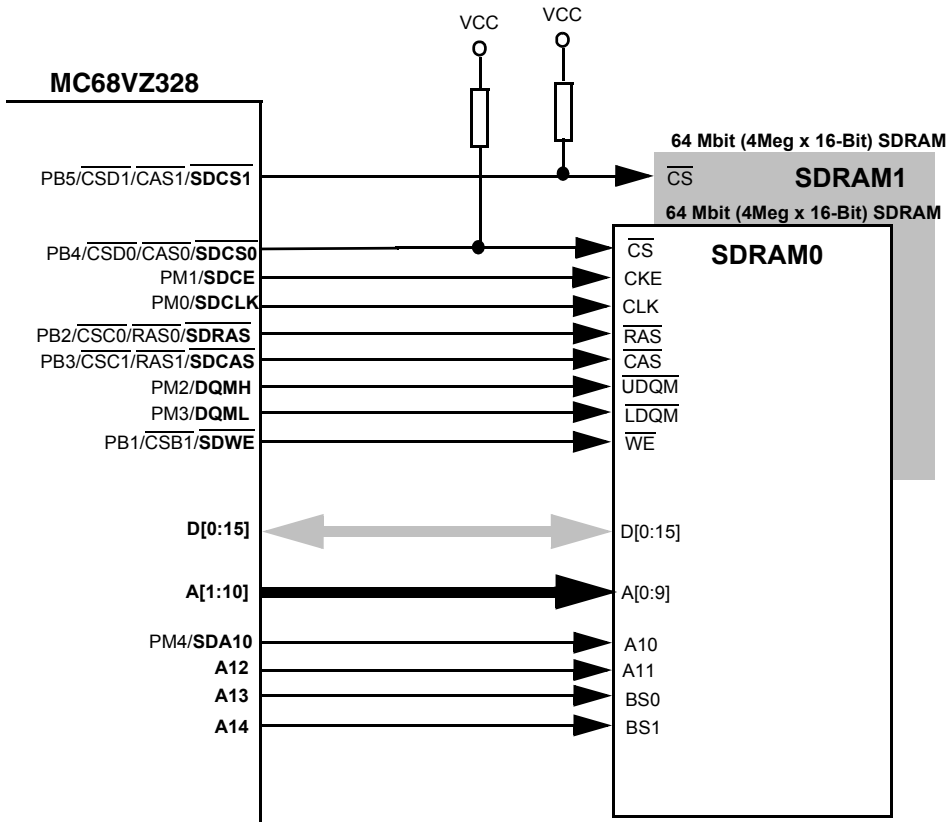

Figure 1. Pin Connection from MC68VZ328 to SDRAM

The configuration shown in Figure 1 was derived from the DragonBall VZ Application Development System (ADS) which provides for two 64 Mbit SDRAM (4 M × 16-bit).

Each chip-select line can address up to 16 Mbytes of memory. Chip-select D0 can be configured to use the address space of chip-select D1 for a total address space of 32 Mbytes. See Section 3.1.2, "Chip-Select Register D (CSD) and Chip-Select Control Register 1 (CSCTRL1)" on page 5 for details on using 32 Mbyte SDRAM.

2.1 Address Lines

One of the more intricate steps in the MC68VZ328 to SDRAM interface is connecting the SDRAM to the address lines. Most importantly, the address line PM4/SDA10 must always be connected to A10 on the SDRAM memory chip to ensure proper SDRAM operation.

NOTE:

SDA10 can be kept high during the precharge command to direct the SDRAM to precharged all banks.

Table 2 provides examples of address line configurations for different sizes of SDRAM.

Table 2. Address Line Configurations (8-Bit or 16-Bit)

	MC68VZ328 Pins			
SDRAM Pins	**16 Mbit**	**64 Mbit**	**128 Mbit**	**256 Mbit**
A[0:9]	A[1:10]	A[1:10]	A[1:10]	A[1:10]
A10	SDA10	SDA10	SDA10	SDA10
A11[1]	A12	A12	A13	A12
A12	X[2]	X	X	A13
BS0	X	A13	A12	A15
BS1	X	A14	A15	A16

1. For 16Mbit SDRAM, A11 is used for Bank Select and maybe labeled as such.
2. X = "No Connect"

These configurations apply to both 8-bit and 16-bit SDRAM, the differences of which, can be configured by setting the DRAM Memory Configuration Register (DRAMMC). Section 7.3 of the DragonBall VZ user's manual provides the details to configure this register. For details on address bus signals, see Section 2.4 of the DragonBall VZ user's manual.

2.2 Data Lines

The data bus for 8-bit SDRAMs must have the data signals connected to D[15:8]. For details on data bus signals, see Section 2.5 of the DragonBall VZ user's manual.

2.3 Interface Lines

For details on SDRAM interface signals, see Section 2.15 of the DragonBall VZ user's manual.

3 SDRAM Control Registers

This section discusses the relevant registers used in SDRAM operations. The following registers have an effect on SDRAM operation.

Table 3. SDRAM Registers

Name	Address	Description	DragonBall VZ Manual
CSGBD	0x(FF)FFF106	Chip-Select Group D Base Address	Table 6-5
CSD	0x(FF)FFF116	Chip-Select Register D	Table 6-10
CSCTRL1	0x(FF)FFF10A	Chip-Select Control Register 1	Table 6-12
CSCTRL2	0x(FF)FFF10C	Chip-Select Control Register 2	Table 6-13
DRAMMC	0x(FF)FFFC00	DRAM Memory Configuration Register	Table 7-6
DRAMC	0x(FF)FFFC02	DRAM Control Register	Table 7-7
SDCTRL	0x(FF)FFFC04	SDRAM Control Register	Table 7-8
SDPWDN	0x(FF)FFFC06	SDRAM Power-down Register	Table 7-10

For certain registers, only some of the fields are relevant to SDRAM operation. Table 4 lists the relevant fields for each register.

Table 4. SDRAM Registers Relevant Fields

Name	Description	Relevant Fields
CSD	Chip-Select Register D	COMB, DRAM, BSW, WS3-1, SIZ, EN
CSCTRL1	Chip-Select Control Register 1	DSIZ3
CSCTRL2	Chip-Select Control Register 2	ECDD, ECDT
DRAMC	DRAM Control Register	EN, RM, CLK, PGSZ, LSP, RST

3.1 Chip-Select Registers

When the DragonBall VZ is configured to use SDRAM, chip-select group D[1:0] is used for SDRAM chip-selects. At the same time, chip-select group C[1:0] becomes the $\overline{\text{SDCAS}}$ and $\overline{\text{SDRAS}}$ signals. During this time, all chip-select group C registers are ignored.

3.1.1 Chip-Select Group D Base Address Register (CSGBD)

This register holds the base address for SDRAM. The value in this register represents A[28:14] of the address bus. A value of 0x0800 puts the SDRAM at 0x01000000.

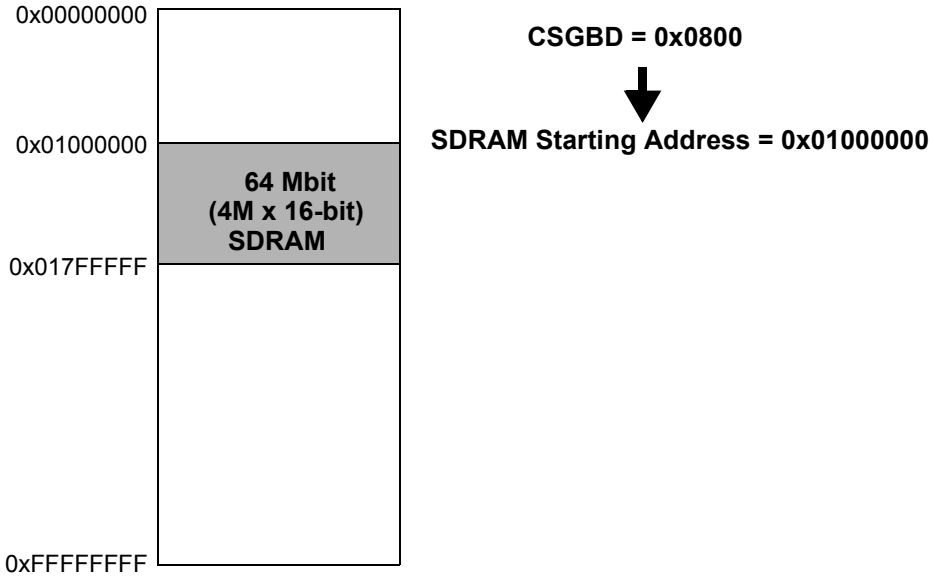

Figure 2. Chip-Select Base Address Register

3.1.2 Chip-Select Register D (CSD) and Chip-Select Control Register 1 (CSCTRL1)

The CSD register is used to determine three things:

- If chip-select group C will be used as CAS and RAS
- Bus width of the SDRAM
- Size for each SDRAM chip-select
  (With the influence of CSCTRL1)

By default, CSD register is set to use the CAS[1:0] and RAS[1:0] functions muxed to PB[5:4] and PB[3:2], respectively. This is determined by the **DRAM bit (bit 9)** of the CSD register.

The **BSW bit (bit 7)** is 0 for 8-bit SDRAM and 1 for 16-bit SDRAM.

The size of each SDRAM chip-select determines the **SIZ field (bits[3:1])**. The values represented by these bits need to be combined with the DSIZ3 bit of the CSCTRL1 register to configure the chip-select size.

Table 5. SDRAM Chip-Select Size

DSIZ3[1]	SIZ [3:1]			SDRAM Size
0	0	0	0	32 kbyte
0	0	0	1	64 kbyte
0	0	1	0	128 kbyte
0	0	1	1	256 kbyte
0	1	0	0	512 kbyte
0	1	0	1	1 Mbyte
0	1	1	0	2 Mbyte

Table 5. SDRAM Chip-Select Size (Continued)

DSIZ3[1]	SIZ [3:1]			SDRAM Size
0	1	1	1	4 Mbyte
1	0	0	0	8 Mbyte
1	0	0	1	16 Mbyte[2]

1) This bit resides in the CSCTRL1 register.
2) Use this setting for 32 Mbyte SDRAM as well.

NOTE:

For 32 Mbyte SDRAM, first set the chip-select size to 16 Mbyte and then set the COMB bit (bit10) of the CSD register to 1. The COMB bit effectively combines the memory space of CSD1 to that of CSD0 allowing CSD0 to address a full 32 Mbyte.

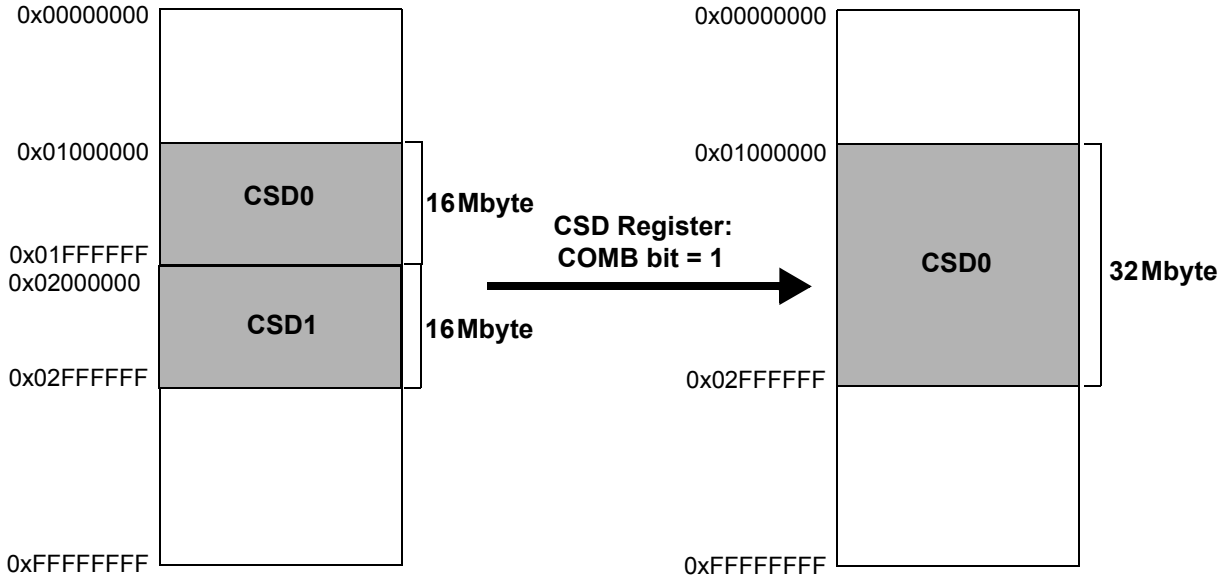

Figure 3. Combining CSD0 and CSD1 for 32 Mbyte SDRAM

The **EN bit** of the CSD register should be set to one to enable this chip-select. Also, the WS3-1 bits can be used to introduce a number of wait states if required.

3.1.3 Chip-Select Control Register 2 (CSCTRL2)

The DragonBall VZ chip-select module incorporates an Early Cycle Detect (ECD) feature for dynamic memory. In a normal chip-select scenario (without ECD), the chip-select signal is proceeded by an internal address strobe (ASB) signal from the 68K core. The ECD feature works from the fact that the ASB is itself proceeded by an "early" ASB signal from the 68K core. By using the early ASB signal to derive the chip-select signal, both read and write cycles to SDRAM can be shortened by one clock cycle.

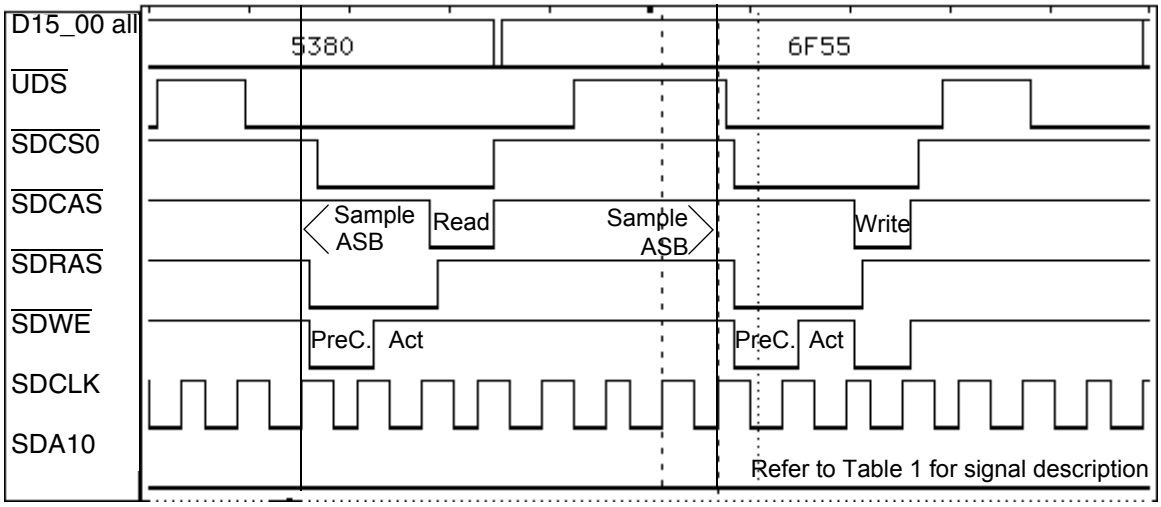

Figure 4. Normal SDRAM Read/Write

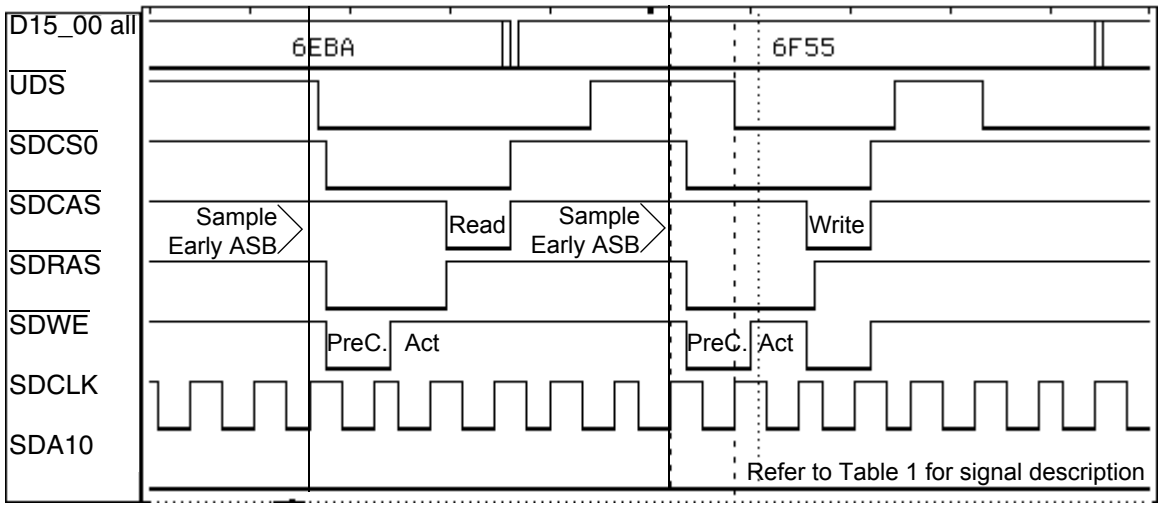

Figure 5. SDRAM Read/Write with ECD

Using the PK3/UDS signal as a reference, as shown in Figure 4 and Figure 5, setting the ECDD bit can improve SDRAM operation during CPU access to the SDRAM by asserting SDCSx early. LCDC DMA access is not affected by the ECD feature because the CPU is not involved during the access.

For more information on ECD settings, see Section 6.3.6 in the DragonBall VZ user's manual

3.2 DRAM Controller Registers

The DragonBall VZ DRAM controller is designed to support SDRAM up to 32 Mbytes. Four registers are used for the configuration and operation of SDRAM.

3.2.1 DRAM Memory Configuration Register (DRAMMC)

The DRAM controller uses address multiplexing to support different types of SDRAM. For recommendations on how address lines must be configured with the SDRAM, use Tables 7-1 through 7-5 in the DragonBall VZ user's manual.

The DRAMMC register also controls the refresh cycle timing, see Section 7.2.3 in the DragonBall VZ user's manual for details. For typical applications, the default value for the REF bits is sufficient.

3.2.2 DRAM Control Register (DRAMC)

The DRAMC contains the following features that apply to SDRAM operations:

- Master DRAM controller enable
- Page size of SDRAM
- SDRAM refresh mode
- Light sleep option
- Reset burst refresh option

Of these features, the first two options require consideration before the SDRAM is initialized.

After the DRAM controller is enabled through the **EN bit (bit15)** of the DRAMC register, the page size of the SDRAM should be set in the **PGSZ field (bits 9-8)**. The page size of a particular SDRAM can be found by the number of column addresses for each bank. The amount of memory space covered by the column addresses is the page size. For 8-bit SDRAM, the number must be divided by two before applying it to the PGSZ field.

Example:

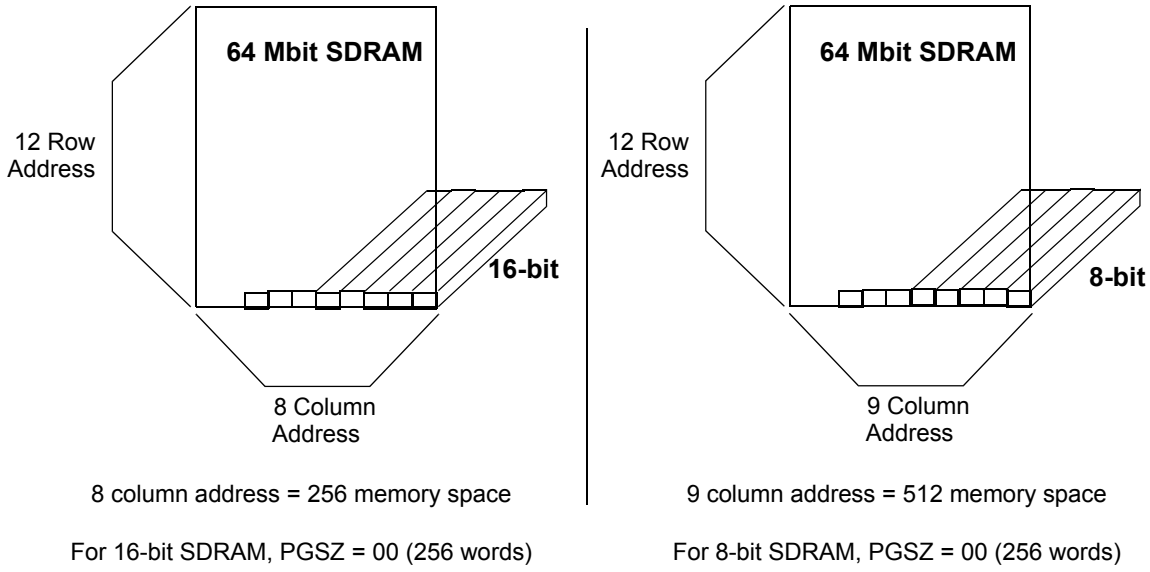

Figure 6. Calculating Page Size

The **RM bit** controls the SDRAM refresh mode between auto-refresh and self-refresh modes. See Section 7.3.2 in the DragonBall VZ user's manual for details on other options.

3.2.3 SDRAM Control Register (SDCTRL)

The SDRAM control register provides features specific to SDRAM operation. This section discusses those features in detail.

The first register bit in the SDCTRL register is the **SDEN bit (bit 15)**. This bit must be set for SDRAM to be used and it must be set before the EN bit is set in the DRAMC to ensure SDRAM support after the controller is enabled.

In addition to the SDEN bit, other settings must be checked as well. These settings include the CAS latency, or **CL bit,** and the bank address line settings (BNKADDH and BNKADDL).

The CAS latency of a SDRAM should always be set in the SDRAM's mode register before using the SDRAM. The DragonBall VZ supports CAS latency of 1 or 2 cycles.

NOTE:

Although most SDRAM does not specify support for CAS latency below 2 clock counts, testing shows that a number of those SDRAM have no problem running in CAS latency 1 mode.

The number of SDRAM banks is defined using the BNKADDH and BNKADDL bits. This "bank" refers to the internal arrangement of the SDRAM chip.

Figure 7 depicts the internal structure of the logic. Two multiplexors derive the bank address based on the setting of the SDCTRL register bits BNKADDH[1:0] and BNKADDL[1:0]. The controller supports 4 banks, therefore there are two lines of bank addresses. However, bnkaddH and bnkaddL signals are used by the internal bank register and the page hit detection logic to track whether the current access is on the same page of the previous access in the same bank. Each individual bank has its own logic.

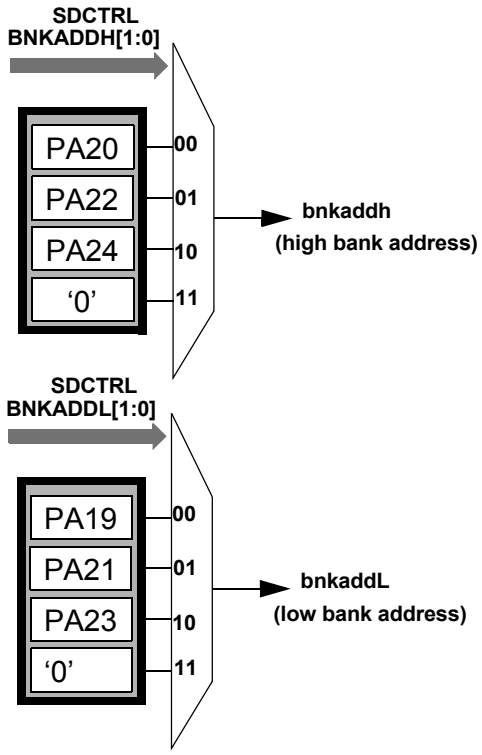

Figure 7. BNKADDH and BNKADDL Model

For a 2 bank device, only one mux from the pair is used. The other mux is programmed to 11 (output 0). This results in the appearance of only two possible bank registers present. For a 4 bank device, two muxes are used to form a two line bank address (bnkaddH and bnkaddL) therefore all four bank registers are used. Users may want to treat a multibank device as a 1 bank device. In this case the user should program both BNKADDH and BNKADDL to 11 (output 0). The logic sees only a one bank register. Table 7-9 in the DragonBall VZ user's manual provides information on how to set these bits.

NOTE:

It is recommended that *all BNKADDH/L bits be set to 1* for SDRAM to appear as one single bank. This is because of a silicon bug documented in the DragonBall VZ design. Multibank settings under CAS latency 2 can cause the DragonBall VZ to stop responding to commands if the LCD and the CPU are accessing separate banks. The erratum is listed in an errata document available at: www.freescale.com/dragonball

The continuous page mode, or **CPM bit,** in the SDCTRL register can also be enabled at this time. The CPM feature can accelerate SDRAM read/write cycles by eliminating unneeded precharge cycles. With CPM enabled, access to a page for the first time generates a page-miss flag which sends a precharge and then a read/write command. Subsequent access to the page generates a page-hit flag which is followed immediately by the read/write command. Setting CPM is another method in circumventing the multibank issue mentioned above.

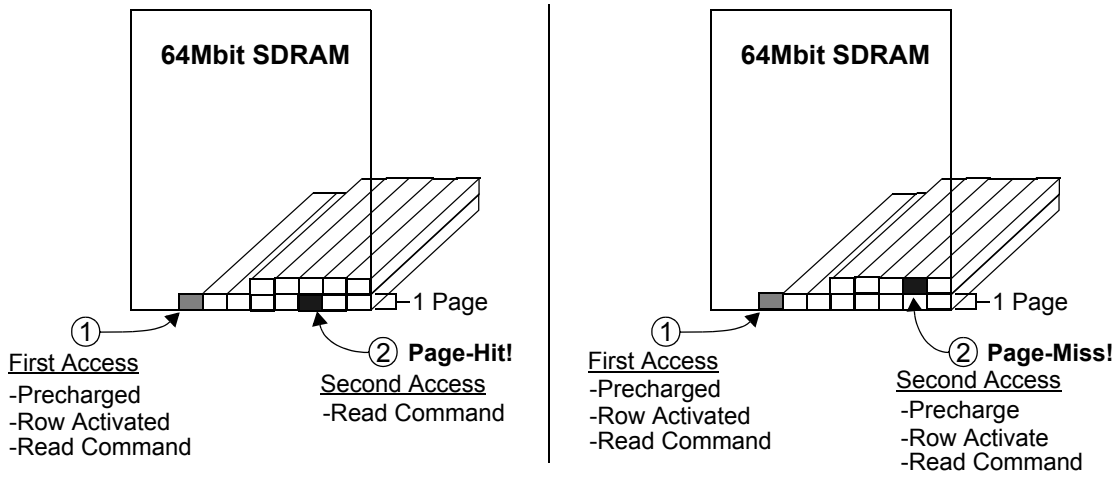

Figure 8. Continuous Page Mode

Before the SDRAM is fully operational, its has to go through the following initialization sequence:

1. Initiate an all bank precharge with the IP bit

   IP = 1, RE = 0, MR = 0

2. Start SDRAM refresh cycles using the RE bit in the SDCTRL register

   IP = 0, RE = 1, MR = 0

3. Set the mode register of the SDRAM with the MR bit

   IP = 0, RE = 1, MR = 1

   The **MR bit** passes the CAS latency setting to the mode register of the SDRAM. The load mode register command programs the SDRAM to CAS latency 1 or 2 depending on the CL bit. The CL bit should be set to the proper latency period prior to setting the MR bit.

The steps above must be completed in sequence followed by a number of no-ops to allow the SDRAM to initialize properly.

See the Section 4, “SDRAM Initialization Sequences” on page 13 for example code on SDRAM initialization.

3.2.4 SDRAM Power-Down Register (SDPWDN)

The SDPWDN register controls how the SDRAM enters power-down mode. The power-down mode can reduce SDRAM power consumption by negating the SDCE signal when SDRAM is not being accessed. During power-down mode, refresh cycles continue to be issued to the SDRAM by the DRAM controller.

3.2.4.1 Active Power-Down Mode

When the APEN bit is set, the SDCE is negated after every access to the SDRAM.

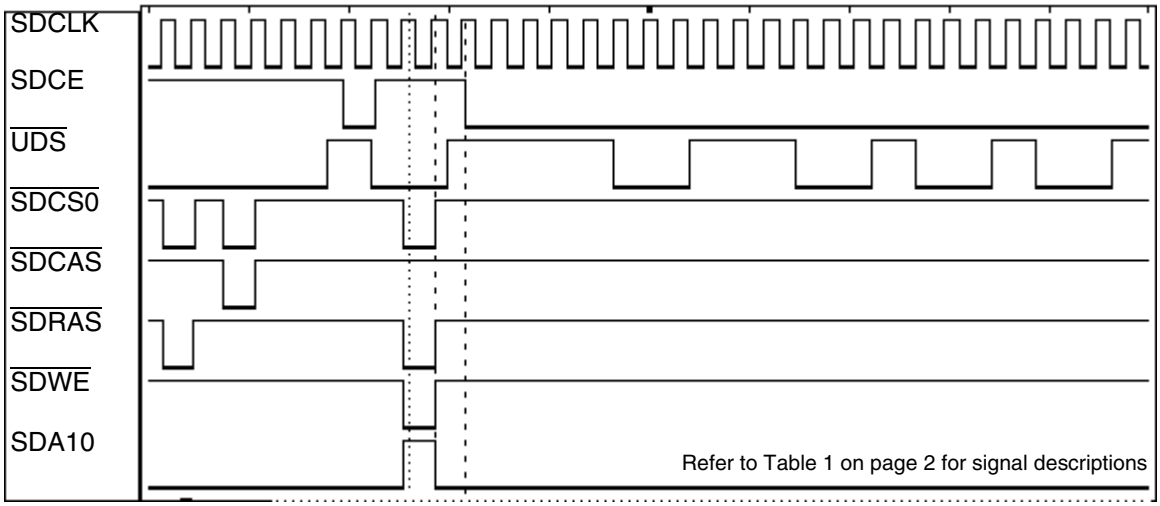

Figure 9. Active Power-Down Mode

3.2.4.2 Precharge Power-Down Mode

When the PDEN bit is set, the SDCE signal is negated when the SDRAM has been precharged and the PDTOUT time-out condition has been met.

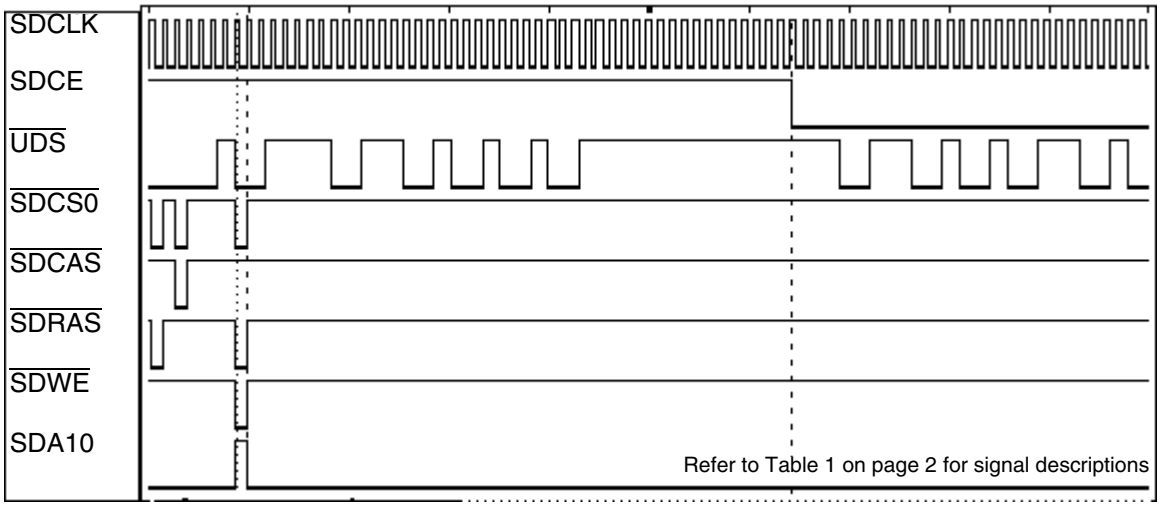

Figure 10. Precharge Power-Down Mode

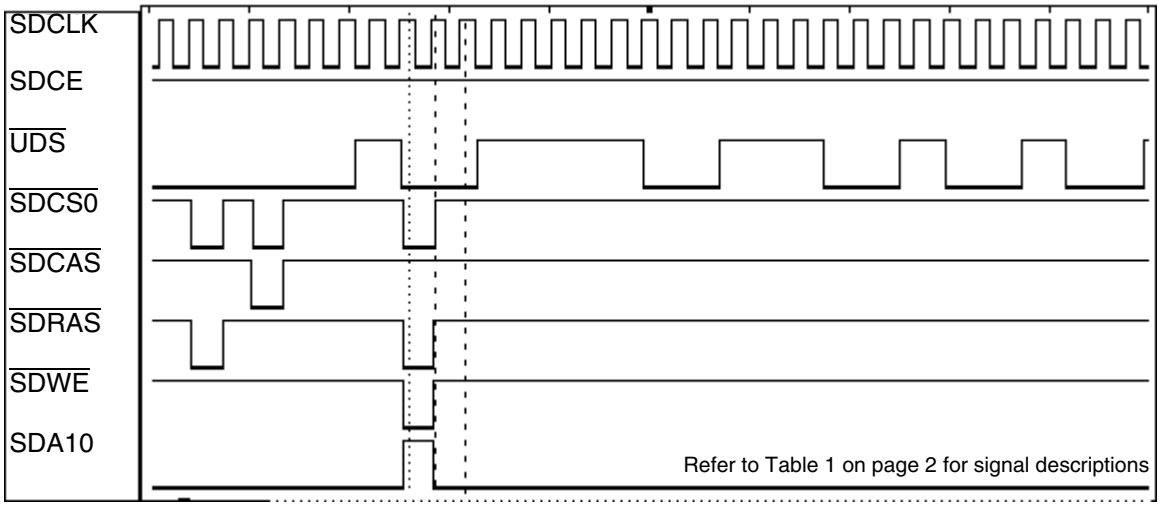

Figure 11. Power-Down Mode Disabled

4 SDRAM Initialization Sequences

Code Listing 1 provides the initialization sequences used by the DragonBall VZ ADS board.

Code Listing 1. SDRAM Initialization Sequences

```
    ;*************************************
    ; SDRAM 64M-bit, Single Band, Latency 2
    ;*************************************
    move.w  #$0000,GRPBASED      ; Set SDRAM base address to 0x0
    move.w  #$0281,CSD
    move.w  #$0040,CSCR         ; Chip Sel Control Reg

    move.w  #$0000,DRAMC        ; Disable DRAM Controller
    move.w  #$C03F,SDCTRL                   ; Set CPM, CL1, Single Bank
    move.w  #$4020,DRAMMC                   ; Multiplexing for 64Mbyte SDRAM
    move.w  #$8000,DRAMC                    ; Enable DRAM Controller

    clr.w   d0                              ; Delay period for SDRAM
delay
    addi.w  #1,d0
    cmp.w   #$FFFF,d0
    bne     delay

    move.w  #$C83F,SDCTRL       ; Issue precharge comm
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    move.w  #$D03F,SDCTRL       ; Enable refresh
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    move.w  #$D43F,SDCTRL       ; Issue mode command
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
```

5 SDRAM Power Control Features

The DRAM controller can initiate the following two types of power control features:

- Self-refresh mode
- Power-down mode

SDRAM self-refresh mode is controlled by the RE bit in the DRAMC register. By setting the RE bit to 1, the DRAM controller issues a self-refresh mode command.

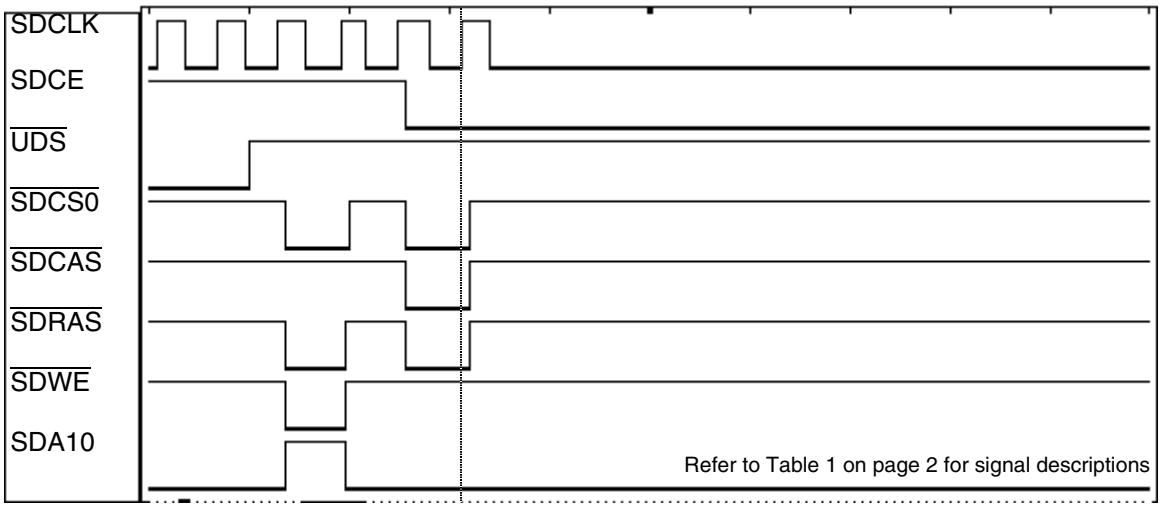

Figure 12. Self-Refresh Event

The SDRAM draws the minimum amount of power when it is in self-refresh mode. The DRAM controller can also be disabled after the SDRAM enters self-refresh mode.

Power-down modes allows the SDRAM to be suspended when not in use. It differs from self-refresh mode in that it does not require a wake-up period when access occurs. See Section 3.2.4 of this document for details on power-down modes.

6 SDRAM Logic Analyzer Screen Captures

The logic analyzer screen captures in this section show the SDRAM read and write cycles generated by the DragonBall VZ ADS.

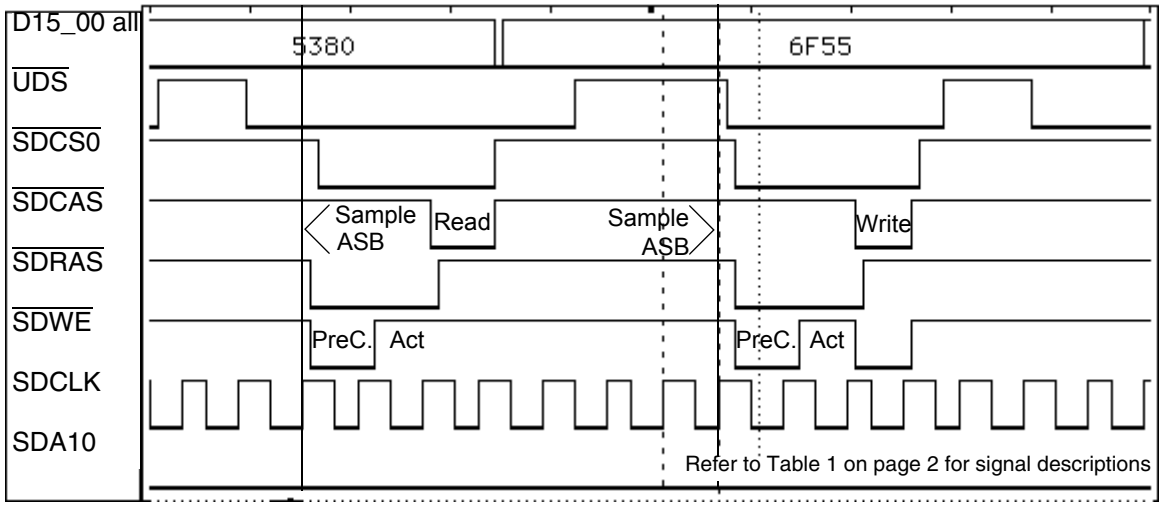

Figure 13. SDRAM Read/Write; CAS Latency = 1; Page-Miss Condition

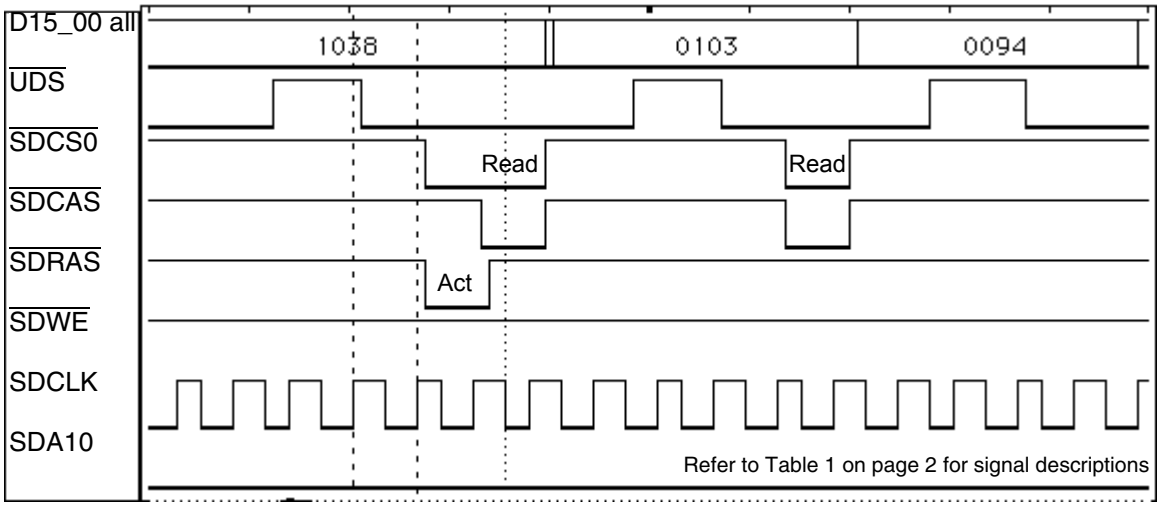

Figure 14. SDRAM Read; CAS Latency = 1; Page-Hit Condition

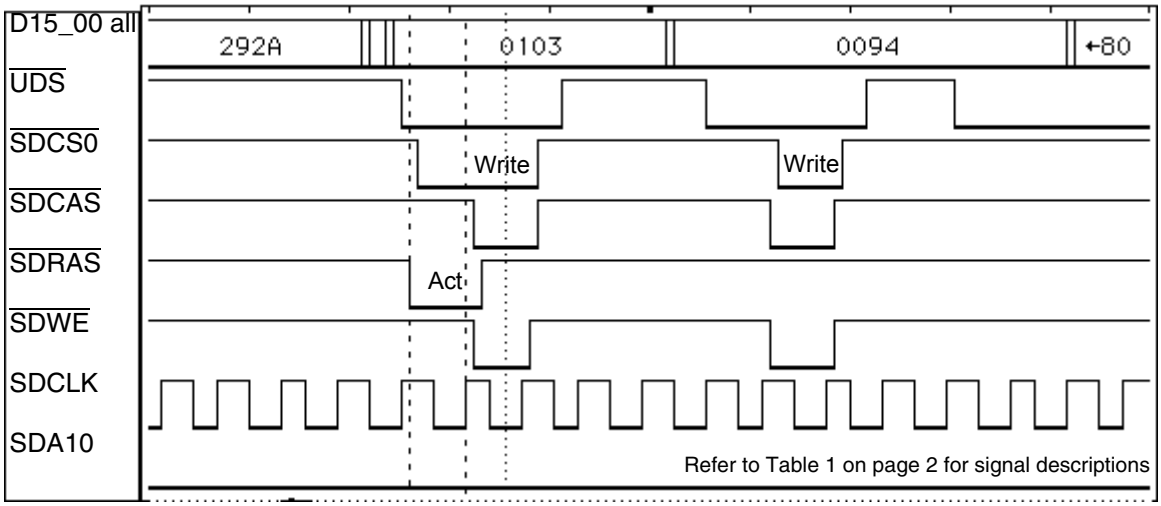

Figure 15. SDRAM Write; CAS Latency = 1; Page-Hit Condition

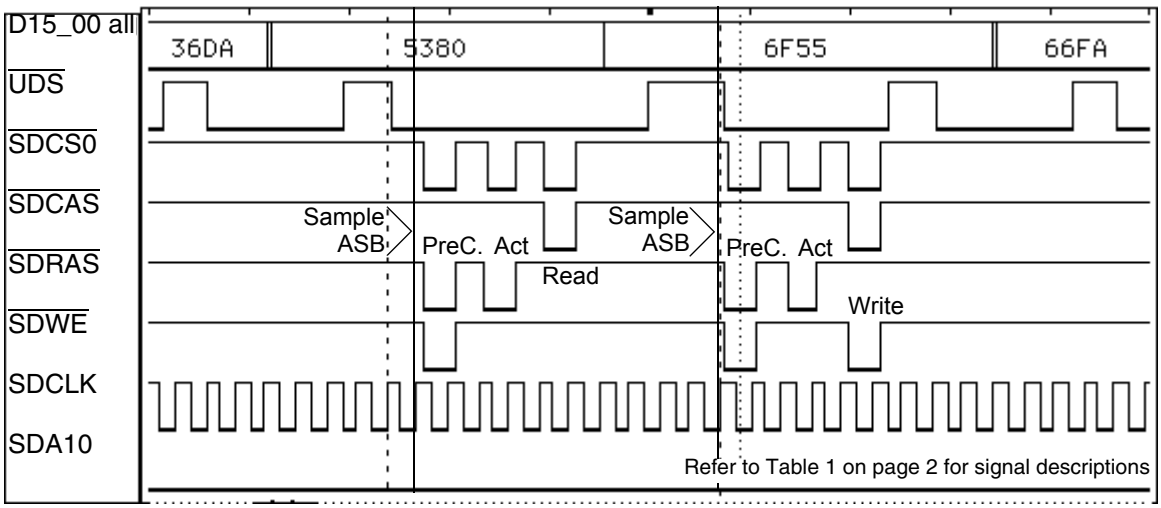

Figure 16. SDRAM Read/Write; CAS Latency = 2; Page-Miss Condition

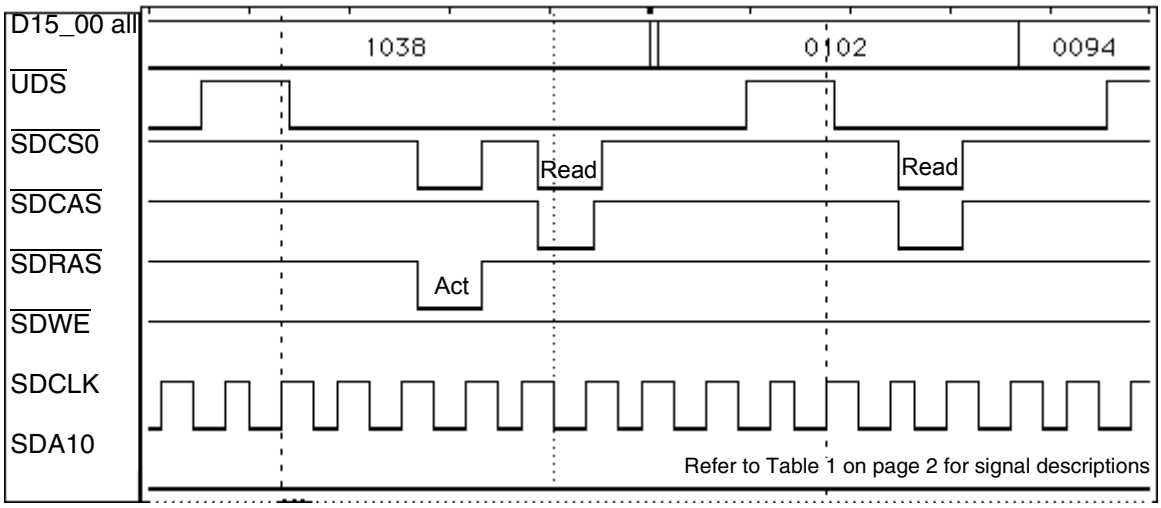

Figure 17. SDRAM Read; CAS Latency = 2; Page-Hit Condition

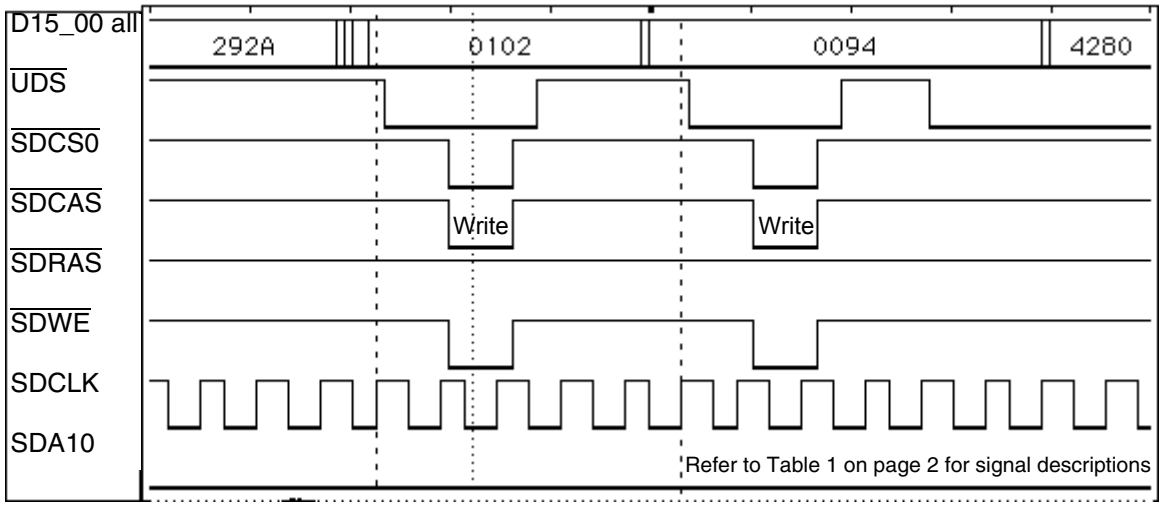

Figure 18. SDRAM Write; CAS Latency = 2; Page-Hit Condition

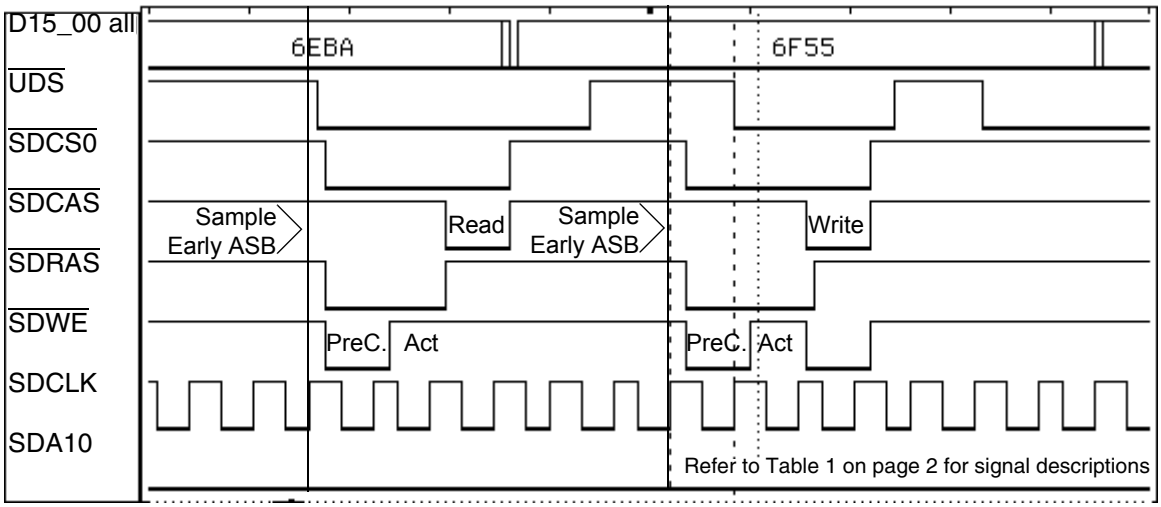

Figure 19. SDRAM Read/Write; CAS Latency = 1; Page-Miss Condition; with ECD

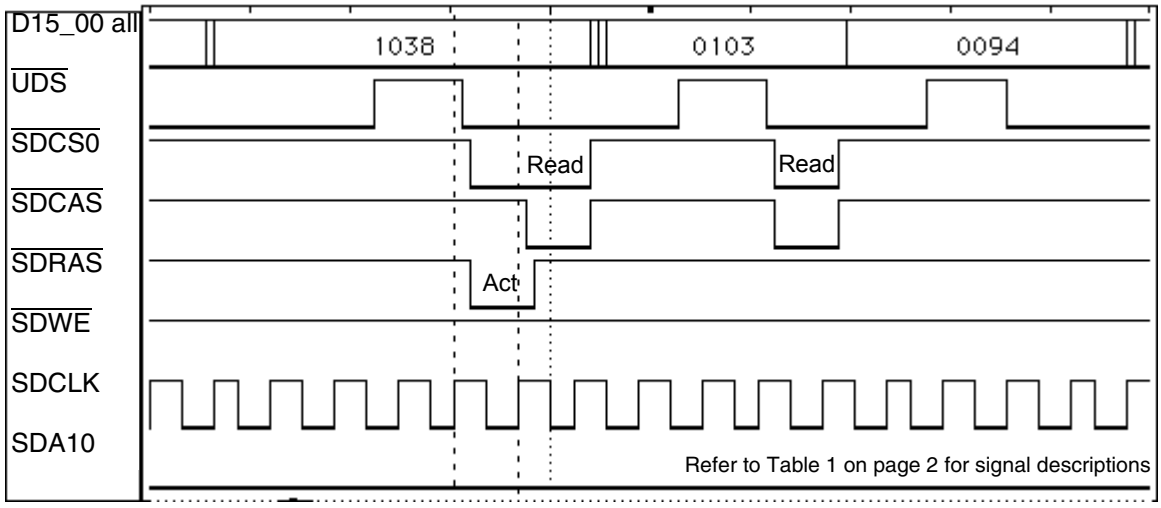

Figure 20. SDRAM Read; CAS Latency = 1; Page-Hit Condition; with ECD

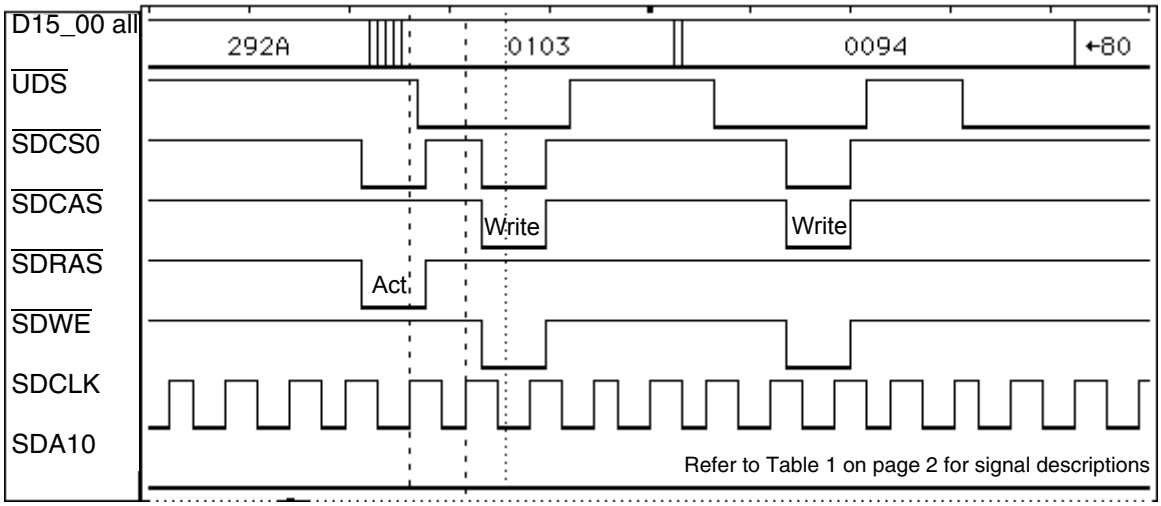

Figure 21. SDRAM Write; CAS Latency = 1; Page-Hit Condition; with ECD

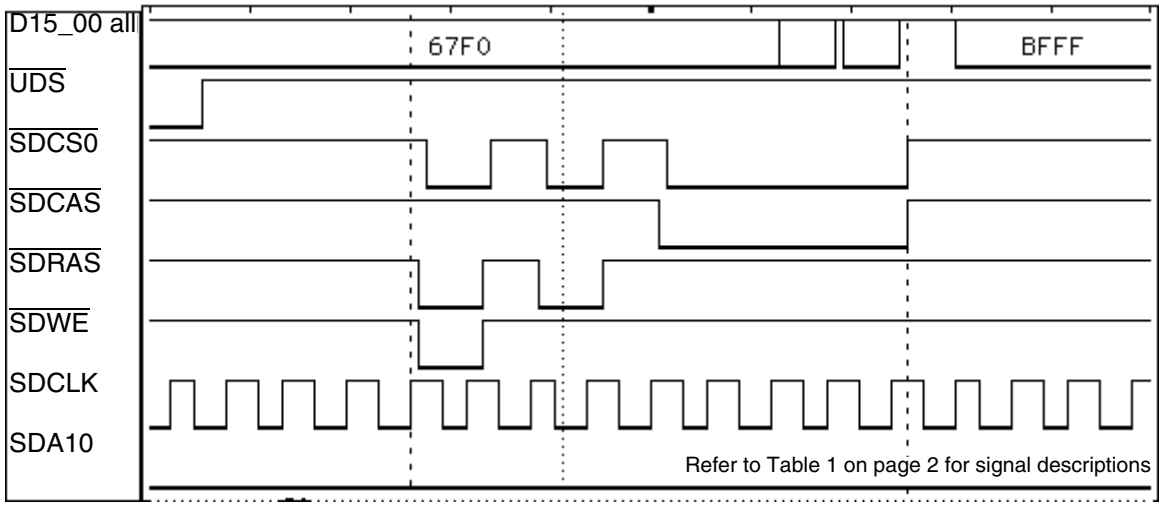

Figure 22. LCD DMA Read; CAS Latency = 2; Burst Length = 4

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