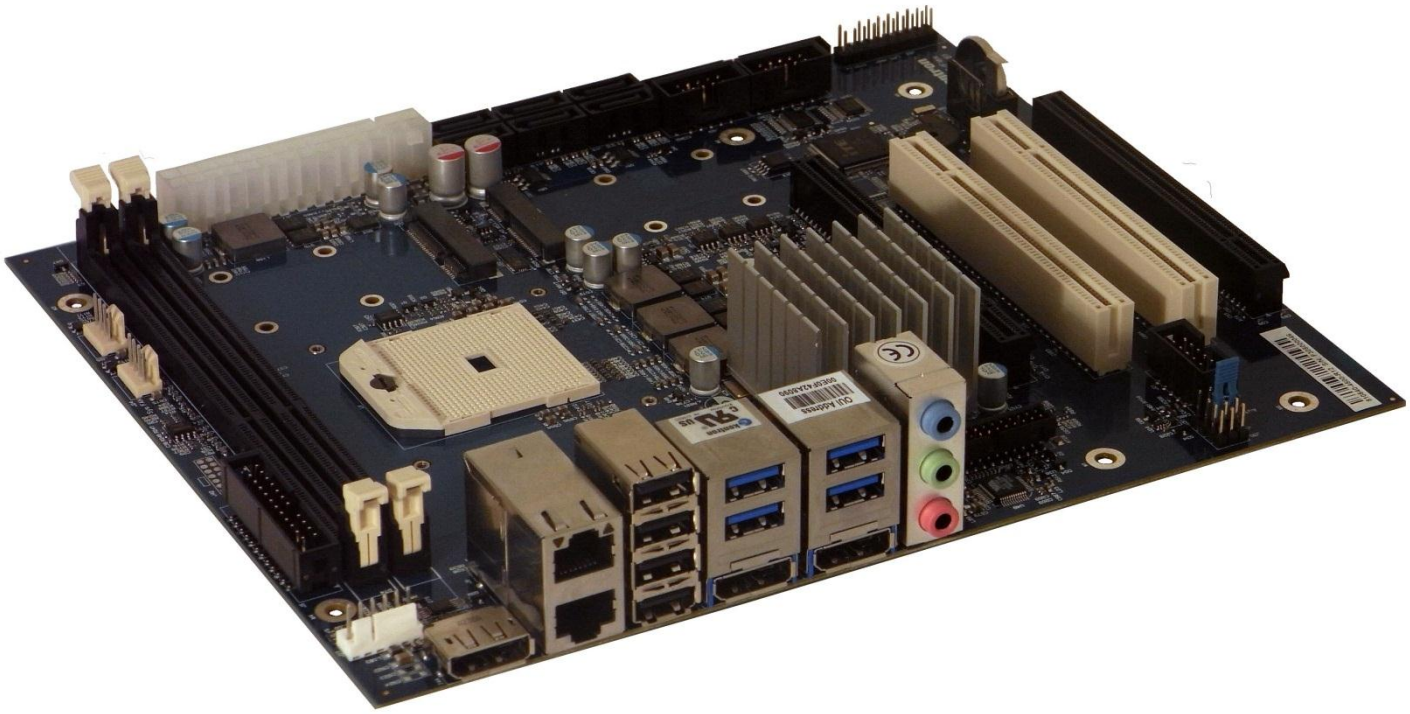
kontron

» Kontron User's Guide «



PRELIMINARY

KTA75/Flex

KTD-N0876-0

» Table of Contents «

Document Revision History

Rev.	Date	By	Comment
0	Mar 21th 2013	MLA	Preliminary version ofKTA75/Flex.

Copyright Notice

Trademark Acknowledgement

Brand and product names are trademarks or registered trademarks of their respective owners.

Disclaimer

KONTRON Technology A/S reserves the right to make changes without notice to any product, including circuits and/or software described or contained in this manual in order to improve design and/or performance.
Specifications listed in this manual are subject to change without notice. KONTRON Technology assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this manual are for illustration purposes only. KONTRON Technology A/S makes no representation or warranty that such application will be suitable for the specified use without further testing or modification.

Life Support Policy

KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein:
Life support devices or systems are devices or systems which (a) are intended for surgical implant into body or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labelling can be reasonably expected to result in significant injury to the user.
A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

KONTRON Technology Technical Support

If you have questions about installing or using your KONTRON Technology Product, then check this User's Manual first – you will find answers to most questions here. To obtain support please contact your local Kontron Sales Partner or Kontron Field Application Engineer (FAE).

Before Contacting Support: Please be prepared to provide as much information as possible:

- CPU Board

  1. Type and P/N (Part Number), find label like:

  2. S/N (Serial Number), find label like:

- Configuration (if relevant)
  1. CPU Type and Clock speed
  2. DRAM Type and Size.
  3. BIOS Revision (find the version info in the BIOS Setup Menu).
  4. BIOS Settings different than *Default* Settings.

- System (if relevant)
  1. OS (Operating System) Make and Version.
  2. Driver Version numbers: Graphics, Network, and Audio etc.
  3. Attached Hardware: Harddisks, CD-Rom, Display Panels etc.

Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period KONTRON Technology will, at its sole option, repair or replace the product with a similar product.
Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning or other acts of nature, unauthorized product modification or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

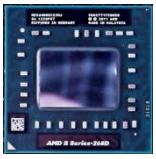
1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCON- VENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

1 Introduction

This manual describes the KTA75/Flex family of boards made by KONTRON Technology A/S. These board will also be denoted KTA75 within this Users Guide.

The KTA75 is designed to support the listed APU variants (uPGA 722pin processors) and AMD A75 Fusion Controller Hub (FCH) A75 on a Flex form factor. See the chapter *System Specifications* for more specific details.

APU variants	AMD PN	Processor data
R-464L	RE464LDEC44HJE	2.3 GHz – Quad Core – 35W
R-460H	RE460HDEC44HJE	1.9 GHz – Quad Core – 35W
R-272F	RE272FDEC23HJE	2.7 GHz – Dual Core – 35W
R-268D	RE268DDEC23HJE	2.5 GHz – Dual Core – 35W



The 4 versions have the same type of active CPU cooler (the cooler is by default not premounted, but can be ordered with this obtion).

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTA75 board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the *Installation Procedure* stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus. Only exceptions are the *Clear CMOS jumper* and the *Always On jumper*.

2 Installation Procedure

2.1 Installing the Board

To get the board running, follow these steps. If the board shipped from KONTRON has already components like RAM mounted, then relevant steps below can be skipped.

1. Turn off the PSU (Power Supply Unit)

Warning: Turn off PSU (Power Supply Unit) befor configuring the board and do not hot plug power supply, otherwise

2. Insert the DDR3 UDIMM 240 Pin module(s)

Be careful to push it in the slot(s) before locking the tabs.

3. Connecting Interfaces and PSU

Insert all external cables for hard disk, keyboard etc. A display/monitor must be connected in order to be able to change BIOS settings. Connect a standard ATX/BTX PSU to the board by the inserting power cables into 24-pin ATX and the 4-pin ATX+12V PWR plugs connectors.

4. Power Button

Turn on mains power to the PSU. If board doesn't boot, then PWRBTN_IN must be toggled; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description), by use of a "normally open" switch etc.

5. BIOS Setup

Enter the BIOS setup by pressing the <Del> key during boot up. Enter Exit Menu and Load Optimal Defaults. Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

Note: To clear all BIOS settings, including Password protection, activate *Clear CMOS* Jumper for ~10 sec (without power connected).

6. Mounting the board to chassis

It is recommended using screws with integrated washer and having diameter of approx. 7mm.

Warning: please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all. Do not use

2.2 Requirements IEC60950

Users of KTA75 should take care when designing chassis interface connectors in order to fulfil the IEC60950 standard.

When an interface or connector has a VCC (or other power) pin which is directly connected to a power plane like the VCC plane:
To protect the external power lines of the peripheral devices the customer has to take care about:

- That the wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

Lithium battery precautions

CAUTION! Danger of explosion if battery is incorrectly re- placed. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instruc- tions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Anga- ben des Herstellers.
ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.	**PRECAUCION!** Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.
ADVARSEL! Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL!** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING! Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS!** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3 System Specifications

3.1 Component main data

The table below summarizes the features of the KTA75/Flex embedded motherboards.

Form factor	Flex: 190,5 x 228,6 mm / 7,5 x 9,0”
ocessor	AMD eTrinity FP2 processor: • Quad-Core 2.3 GHZ with R-464L APU 35W • Quad Core 1.9 GHz with R-460H APU 35W • Dual Core 2.7 GHz with R-272F APU 35W • Dual Core 2.5 GHz with R-268D APU 35W • Compatible with Existing 32-Bit x86 and 64-bit AMD64 Code Base • AMD64 64-bit ISA • High Performance Floating-Point Unit • SSE 4.1 & 4.2, AVX 1.0 &1.1, AES, XOP, FMA4 • Secure advanced Virtualization Features • 64-bit DDR3 SDRAM Controller (1333MT/s,666MHz): PC3-10600 / (1600MT/s,800MHz): PC3-12800 • Compliant with JEDEC DDR3 1.5V and LV-DDR3 1.35V/1.25V SDRAM specification. Note:LV-DDR3 modules not validated • PCIe® Technology • Integrated Memory Controller • Integrated Graphics AMD Radeon™ HD 7000G Series graphics. • Dedicated graphics memory controller • 2D Acceleration Features • Open GL 4.2 & 2.0 • DirectX® 11 compliant 3D Acceleration Features • Adaptive Anti Aliasing, Shader Model 5 • Motion Video Acceleration Features • Dedicated hardware (UVD 3) for H.264 • VC-1, DivX and MPEG2 decode • HDCP (High-bandwidth Digital Content Protection) supported on DisplayPort Interface. • Display Port 1.2 • Support DVI/HDMI via passive adapter.

Companion Device	AMD A75 (Hudson)Fusion Controller Hub • Unified Media Interface (UMI) (5.0 GT/s) • PCI Express® 2.0 Controller • PCI Host Bus Controller • USB Controllers with up to 14 USB ports • SMBus Controller • SATA Controller with RAID 0,1,10 support • High Definition Audio • Real Time Clock (RTC) • Integrated Clock controller • ACPI 3.0 compliant
Memory	Memory controller is integrated in the AMD eTrinity FS1r2 uPGA 722pin processor. Features are: • Compliant with JEDEC DDR3 1.5V and *(LV-DDR3 1.35V / 1.25 SDRAM, not verified)* specifications • Supports DDR3 UDIMM 240pin Using up to 8GB DRAM technology • DDR3 1333/1600MT/s (PC3-10600/PC3-12800) • From 1GB to 2x 8GB maximum (16GB in total) Notes: Less than 4GB displayed in System Properties using 32bit OS (Shared Video Memory/PCI resources is subtracted) ECC not supported
Flash (BIOS)	32Mbit SPI Flash for dual System BIOS.
Security	Intel® Integrated TPM 1.2 support Infineon TPM SLB9635TT1.2 (FW 3.17)
IT8516E Embedded Controller	KT Feature Connector. 15 Multiplexed (GPIO, DAC, ADC, PWM & TIMER) Possible 152 GPIO expansion. Software Watchdog.
Audio Codec	Audio, 7.1 Channel High Definition Audio Codec using the VIA VT1708S codec
Seriel ATA	6x SATA port J9 – J13 & J39, SATA 3.0 1x mSATA J39 (mechanically sharing space with mPCIe slot J38), SATA 3.0 • RAID 0,1,10 support
Frontpanel	2xUSB, HDD-LED, SYSRST#, SUSLED, PWRBTN#, AUDIO Line/MIC output.
PCI	2x PCI slots (PCI Local Bus Specification revision 2.3 32bit/33MHz)

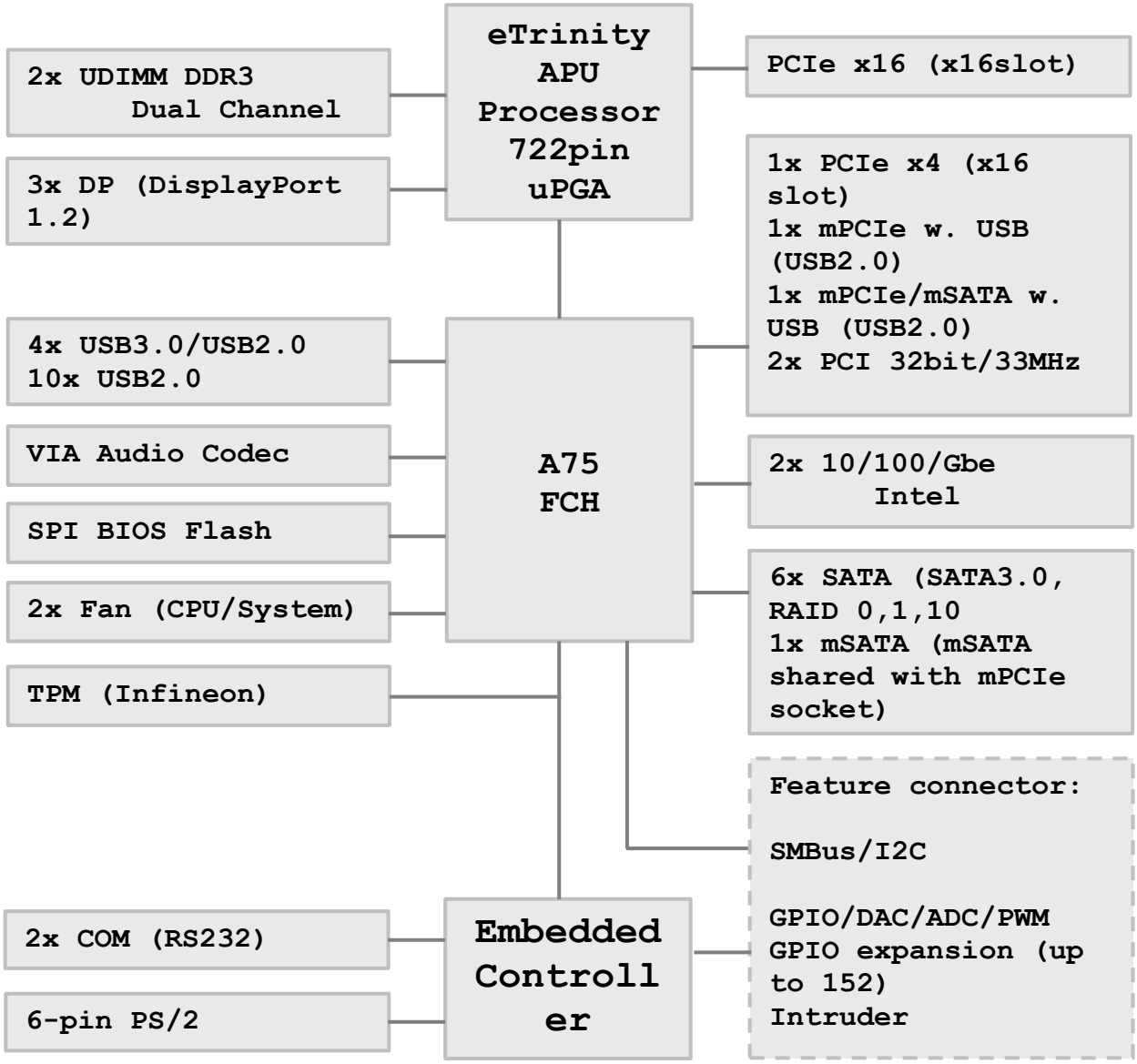
PCIe	1x PCI Express x16 Slot 1x PCI Express x4 Slot (in mechanically x16 slot) 1x mPCIe Slot J38 1x mPCIe/mSATA J43 (mechanically sharing between mSATA and mPCIe) The mSATA interface will be selected when a mSATA card are inserted into the mPCIe socket (J43)
DisplayPort	3x DisplayPort connector (in REAR-IO area) DP1 J43 DP2 J3 DP0 J4 Optionally Add-On card with 1x DisplayPort
LVDS	Optionally Add-On card (TBD)
Audio Jack	3x Audiojacks stack J40 (in REAR-IO area) Blue Line-In Green Speaker Pink Mic
Audio	Audio Pin header J41 Line-out Line-in Surround output: SIDE, LFE, CEN, BACK and FRONT Microphone: MIC1 SPDIF-OUT (electrical Interface only)
LAN	Two RJ45 connectors J8 (in REAR-IO area) • 2x 10/100/1000Mbits/s LAN (ETH1/ETH2) using Intel® Pearsonville xGB PCI Express Ethernet controller (WGI211ATSLJXZ). • PXE Netboot supported. • Wake On LAN (WOL) supported
USB	14x USB ports (9x USB2.0 & 4x USB2.0/USB3.0): 2x USB2.0 in Frontpanel Connector J5 2x USB2.0 in USB Internal USB Connector J16 4x USB2.0, USB stack J20 (in REAR-IO area) 2x USB 2.0/USB3.0, Right USB stack J14 (in REAR-IO area) 2x USB 2.0/USB3.0, left USB stack J15 (in REAR-IO area) 1x USB 2.0 in mPCIe socket J38 1x USB 2.0 in mSATA/mPCIe socket J43
Serial port	2x RS232 pin header (+12V, -12V supply generated by driver circuit) COM1 2x 5 Pin row J23 COM2 2x 5 Pin row J22
LPC	LPC connector J29

FAN	CPUFAN 4 pin row J25 12V PWM SYSFAN 4 pin row J24 12V PWM
PS2 Kbd/Mse	1x 6 Pin row Keyboard / Mouse PS2 cable kit interface J27
Power Plug	1x 4 pole Internal connector J19 ATX core power (+12V Single Supply , Max 260W) 1x 24 pole connector J17 ATX/BTX power
Battery	Exchangeable 3.0V Lithium battery for on-board Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032N/BN or CR-2032L/BE. Approximate 6 years retention. Current draw is 4 µA when PSU is disconnected and 0 µA in S0 – S5. CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.
Speaker	On-board Speaker Piezo On-board speaker (Electromagnetic Sound Generator like Hycom HY-05LF)

Environmental	Operating: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) Storage: -20°C – 70°C; lower limit of storage temperature is defined by specification restriction of on-board CR2032 battery. Board with battery has been verified for storage temperature down to -40°C by Kontron. 5% - 95% relative humidity (non-condensing) Electro Static Discharge (ESD) / Radiated Emissions (EMI): All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. Safety: EN 60950-1: 2006/ A11:2009/ A1:2010/A12:2011 IEC 60950-1(ed.2) CSA C22.2 No. 60950-1 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 (E194252-A21-CB-1) Theoretical MTBF: 314.614 / 153.436 hours @ 40°C / 60°C Restriction of Hazardous Substances (RoHS): All boards in the KTA75 family are RoHS/RoHS-II compliant. Capacitor utilization: No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100 °C used on board
BIOS	AMI EFI SPI Connector J21 (for BIOS Recovery) Clear CMOS J34 Always On J37

OS (planned)	Windows 7 (32 and 64bit) Windows 8 (32 and 64bit) Windows XP (32 bit) DOS Windows Embedded 7

3.2 KTA75/Flex Block Diagram



3.3 USB ports overview

The KTA75 board contains two pairs of EHCI (Enhanced Host Controller Interface) and OHCI (Open Host Controller Interface) in order to support up to 10 USB1.1/USB2.0 devices and further more two xHCI (Extensible Host Controller Interface) to support up to 4 USB3.0 devices.

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).

The EHCI controllers support USB2.0, High-Speed (480Mbps).

The xHCI controllers support USB3.0, USB2.0 and USB 1.1, Super-Speed (5.0Gbps), High-Speed (480Mbps), Full-Speed (12Mbps) and Low-Speed (1.5Mbps)

Legacy Keyboard/Mouse and wakeup from sleep states are supported. Over-current detection on all USB ports except USB2.

USB #	USB standard	Connector location	HCI	Note
USB0 USB1	USB2.0 /USB1.1	Frontpanel (J5)	OHCI1/EHCI1	
USB2	USB2.0 /USB1.1	mPCIe (J38)	OHCI1/EHCI1	No over current detection
USB3	USB2.0 /USB1.1	mSATA/mPCIe (J43)	OHCI1/EHCI1	No over current detection
USB4	USB2.0 /USB1.1	Pin row (J16)	OHCI1/EHCI1	
USB5	USB2.0 /USB1.1	Pin row (J16)	OHCI2/EHCI2	
USB6 USB7 USB8 USB9	USB2.0 /USB1.1	USB quad stack (J20) Rear IO	OHCI2/EHCI2	
USB10 USB11	USB3.0/USB2.0/USB1.1	USB3.0 dual stack (J15) Left - Rear IO	xHCI1	
USB12 USB13	USB3.0/USB2.0/USB1.1	USB3.0 dual stack (J14) Right - Rear IO	xHCI2	

Notes: ***In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.***

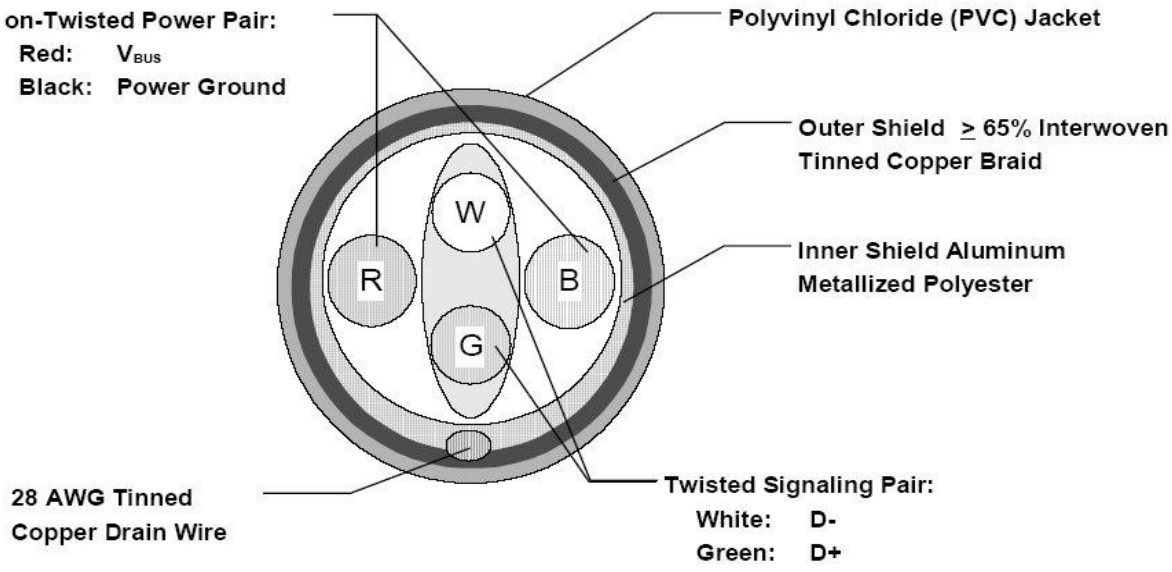
The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that

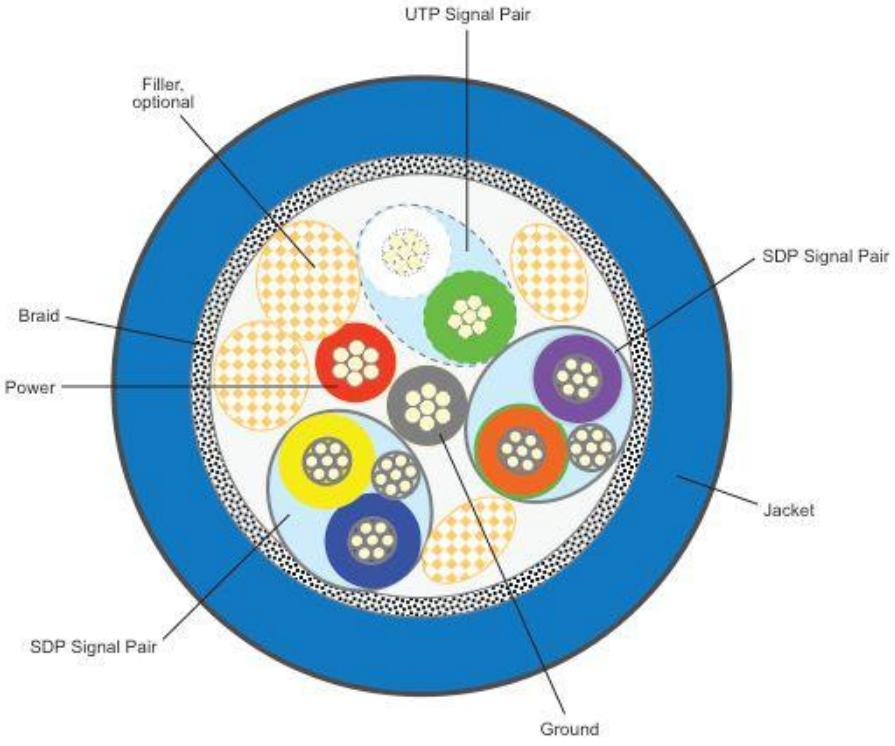
- the wires have the right diameter to withstand the maximum available current.

- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

For USB2.0 cabling it is required to use only HiSpeed USB cable, specified in USB2.0 standard:

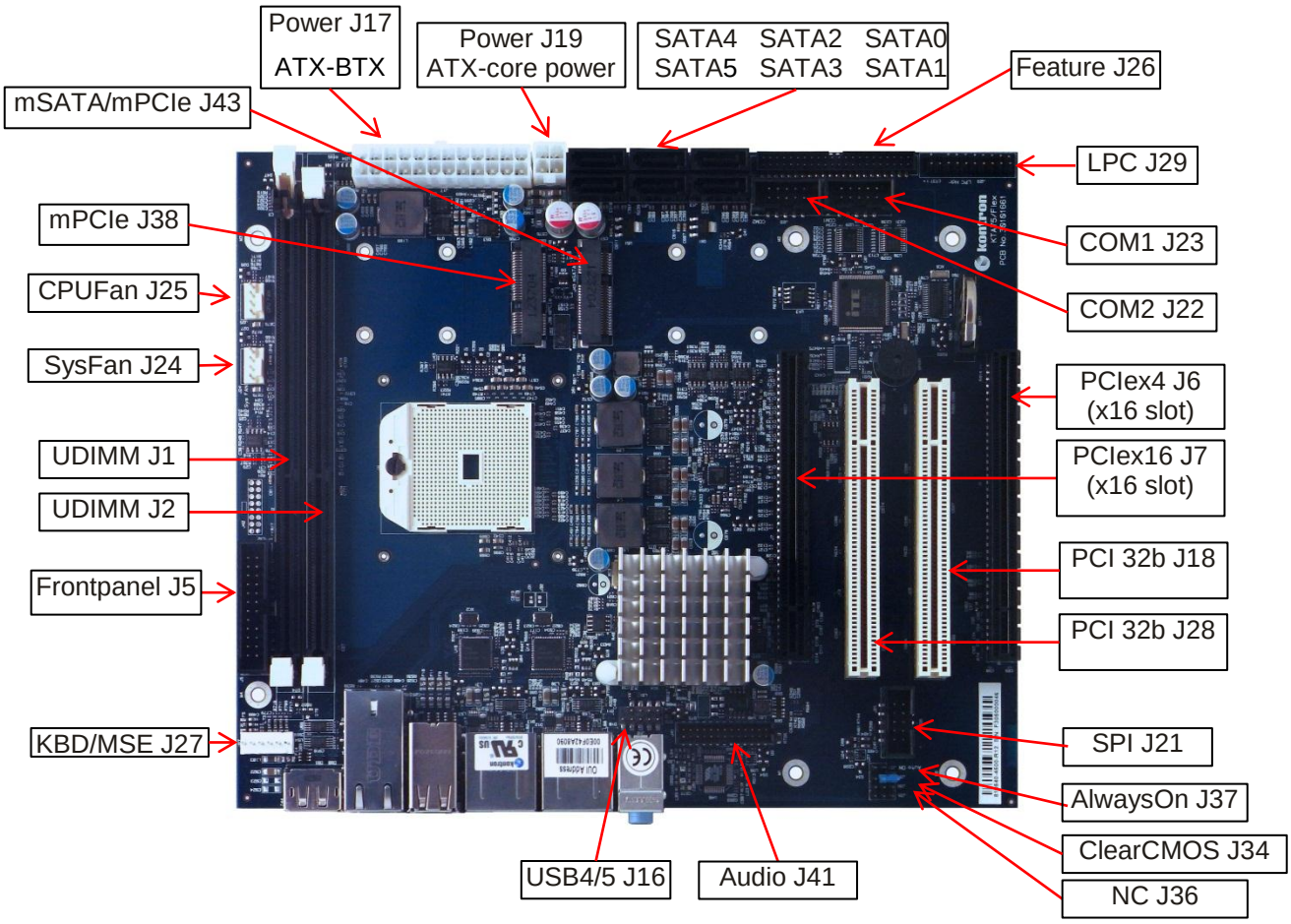


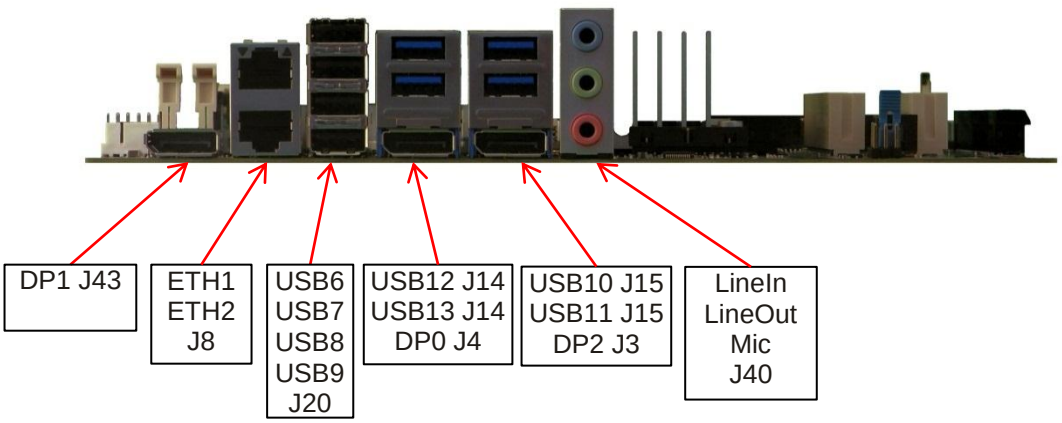
For USB3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:



4 Connectors Locations

4.1 KTA75/Flex Topview





5 Connector Signal Definitions

The following sections provide pin definitions and detailed description of all onboard connectors.
The connector definitions follow the following notation:

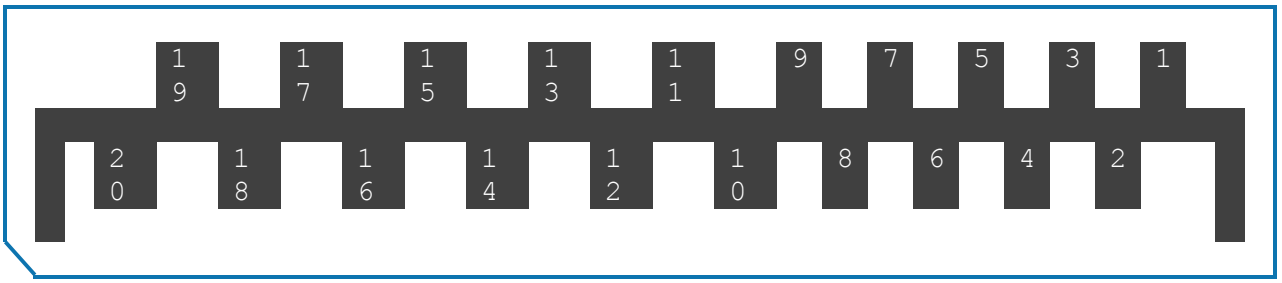
Column Name	Description
Pin	Shows the pin numbers in the connector.
Signal	The mnemonic name of the signal at the current pin. The notation "#" states that the signal is active low.
Type	AI: Analogue Input AO: Analogue Output I: Digital Input IO: Digital Input / Output IOD: Input / Open Drain output O: Digital Output DSO: Differential Signaling Output with complementary signals on two paired wires DSI: Differential Signaling Input with complementary signals on two paired wires DSIO: Differential Signaling Input / Output (combined DSO and DSI) PWR: PoWeR supply or ground reference pins NC: Pin Not Connected Additional notations: -5.0 +5.0V signal voltage level, e.g. I-5.0 -3.3 +3.3V signal voltage level, e.g. O-3.3 -1.8 +1.8V signal voltage level, e.g. IO-1.8
Ioh/Iol	Ioh: Typical current in mA flowing out of an output pin through a grounded load while the output voltage has high level. Iol: Typical current in mA flowing into an output pin from a VCC connected load while the output voltage has low level.

The abbreviation tbd is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

6 Rear IO Connectors

6.1 DisplayPort (DP0/DP1/DP2)(J3/J4/J44)

The DP (DisplayPort) connectors are based on standard DP type Foxconn 3VD11203-H7AB-4H or similar.



Pin	Signal	Description	Type	Note
1	Lane 0 (p)		LVDS	
2	GND		PWR	
3	Lane 0 (n)		LVDS	
4	Lane 1 (p)		LVDS	
5	GND		PWR	
6	Lane 1 (n)		LVDS	
7	Lane 2 (p)		LVDS	
8	GND		PWR	
9	Lane 2 (n)		LVDS	
10	Lane 3 (p)		LVDS	
11	GND		PWR	
12	Lane 3 (n)		LVDS	
13	Config1	Aux or DDC selection	I	Internally pull down (1Mohm). Aux channel on pin 15/17 selected as default (when NC) DDC channel on pin 15/17, If HDMI adapter used (3.3V)
14	Config2	(Not used)	O	Internally connected to GND
15	Aux Ch (p)	Aux Channel (+) or DDC Clk		AUX (+) channel used by DP DDC Clk used by HDMI
16	GND		PWR	

17	Aux Ch (n)	Aux Channel (-) or DDC Data		AUX (-) channel used by DP DDC Data used by HDMI
18	Hot Plug		I	Internally pull down (100Kohm).
19	Return		PWR	Same as GND
20	3.3V		PWR	Fused by 1.5A resetable PTC fuse, common for DP0 and DP1

Note: ***To protect the external power lines of peripheral devices make sure that***
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

The 3 DisplayPorts (DP0, DP1 and DP2) can be used in 3 independt display configurations. By use of DP Adapter Converters it is possible to implement a mix of DP, VGA, HDMI and DVI-D outputs and still support 3 independt display configuration.

Available DP adapters:

DP to VGA	DP to HDMI	DP to DVI-D
PN 1045-5779	PN 1045-5781	PN 1045-5780

DP Extention Cable:

In order to prevent mechanical conflicts the above DP adapters can be connected to DP#0, DP#1 and DP#2 via the 1051-7619 Cable DP Extender cable 200mm.

The DP to VGA adapter is an “active” converter, meaning that seen from the graphics controller it looks like a DP. The HDMI and DVI converters are passive converters, meaning that they inform the graphics controller about its type and the graphics controller then replace the DP signals with TMDS signals (used in HDMI and DVI).

The HDMI interface supports the HDMI 1.4a specification including audio codec. Limitations to the resolution apply: 2048x1536 (VGA), 1920x1200 (HDMI and DVI).

4 independt (simultaneously) displays (without using PCIe Graphics cards) is a possible configuration under the following conditions:

1. A PCIe-DP passive card must be used in the outermost PCIe slot.
2. All DP must be converted to DP-DVI-D or DP-HDMI via passive adapters like above adapters. (Restriction, only one adapter can be HDMI type)
3. Two of the panels must have the same timing (meaning two display monitors have to be exact same type).

6.2 USB3.0 Connectors (USB10/USB11/USB12/USB13) (J15/J15/J14/J14)

The USB3.0 connectors are based on standard USB3.0 connectors type Lotes ABA-USB-104-K01 or similar.

Thease 4 USB3.0 ports are controlled by the xHCI controllers supporting USB3.0, USB2.0 and USB 1.1, Super-Speed (5.0Gbps), High-Speed (480Mbps), Full-Speed (12Mbps) and Low-Speed (1.5Mbps)

USB Ports 10 and 11 (mounted on top of the DP#2 port):

Note	Type	Signal	PIN	Signal	Type	Note
	DSIO-3.3		USB10-	USB10+	DSIO-3.3	
1	PWR	5V/SB5V	1 2 3 4	GND	PWR	
	DSIO-3.3	RX10-	5 6 7 8 9	TX10+	DSIO-3.3	
	DSIO-3.3		RX10+	TX10-	DSIO-3.3	
	PWR		GND			
	DSIO-3.3		USB11-	USB11+	DSIO-3.3	
1	PWR	5V/SB5V	1 2 3 4	GND	PWR	
	DSIO-3.3	RX11-	5 6 7 8 9	TX11+	DSIO-3.3	
	DSIO-3.3		RX11+	TX11-	DSIO-3.3	
	PWR		GND			

Signal	Description
USB10+ USB10- RX10+ RX10- TX10+ TX10- USB11+ USB11- RX11+ RX11- TX11+ TX11-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external device. SB5V is supplied during powerdown to allow wakeup on device activity. Protected by current limited power distribution switch,1A for each port.

USB Ports 12 and 13 (mounted on top of the DP#0 port):

Note	Type	Signal	PIN					Signal	Type	Note
	DSIO-3.3	USB12-						USB12+	DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4		GND	PWR	
	DSIO-3.3	RX12-	5	6	7	8	9	TX12+	DSIO-3.3	
	DSIO-3.3	RX12+						TX12-	DSIO-3.3	
	PWR	GND								
	DSIO-3.3	USB13-						USB13+	DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4		GND	PWR	
	DSIO-3.3	RX13-	5	6	7	8	9	TX13+	DSIO-3.3	
	IO	RX13+						TX13-	DSIO-3.3	
	PWR	GND								

Signal	Description
USB12+ USB12- RX12+ RX12- TX12+ TX12- USB13+ USB13- RX13+ RX13- TX13+ TX13-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external device. SB5V is supplied during powerdown to allow wakeup on device activity. Protected by current limited power distribution switch,1A for each port.

Notes: ***In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.***

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that

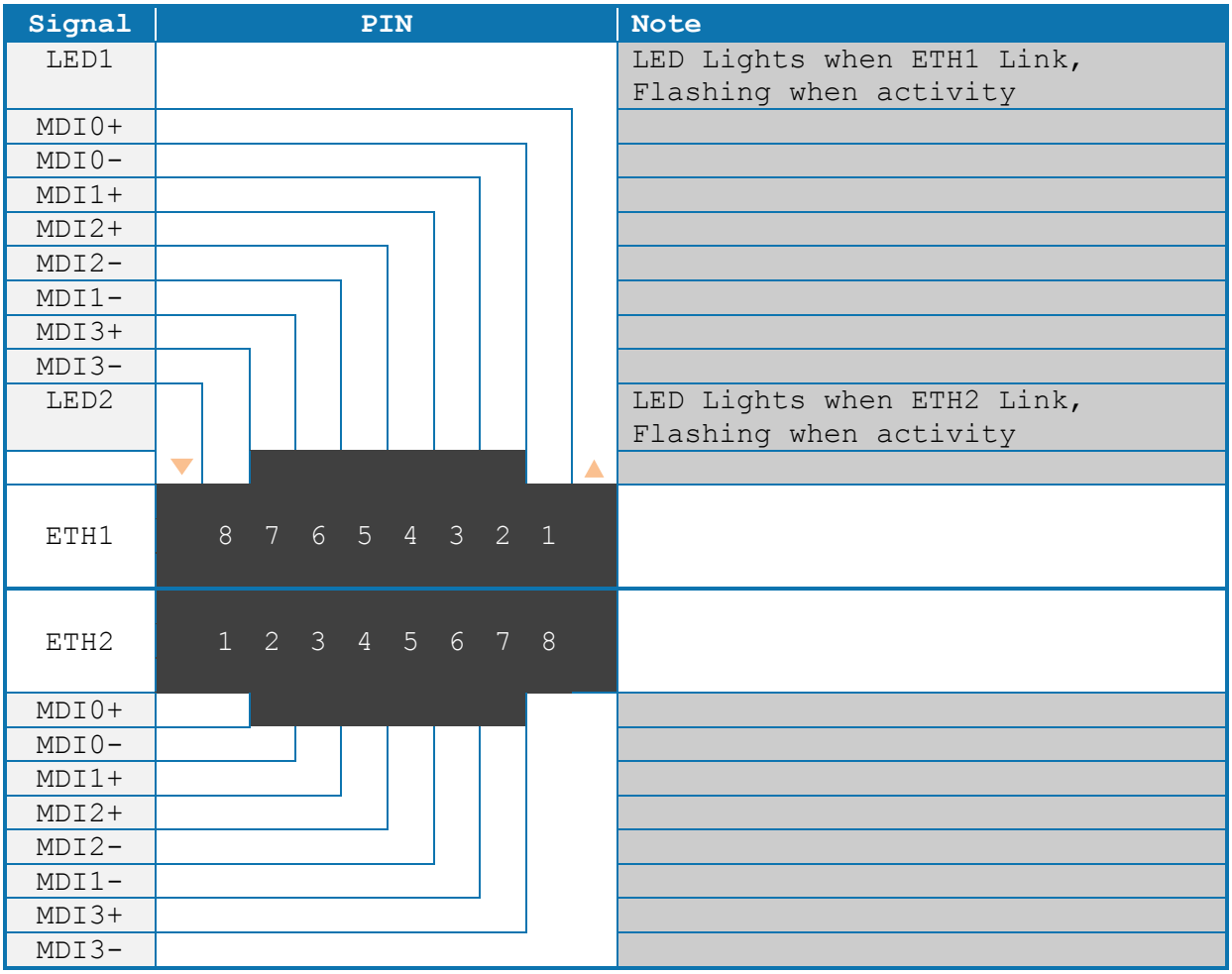
- the wires have the right diameter to withstand the maximum available current.

- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

6.3 Ethernet Connectors (ETH1/ETH2) (J8)

The KTA75 supports two 10/100/1000Mb Ethernet RJ45 connetors in a stacked dual LAN connector, type Ude RMT-123AGF1F or sililar. Both ports are driven by Intel® Pearsonville WGI211AT PCI Express controller.

Ethernet connector 1 (ETH1) is mounted above Ethernet connector 2 (ETH2).



In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

Signal	Description
MDI[0]+ / MDI[0]-	MDI mode: first pair in 1000Base-T (i.e. the BI_DA+/- pair), transmit pair in 10/100Base-T. MDI crossover mode: acts as the BI_DB+/- pair, receive pair in 10/100Base-TX.
MDI[1]+ /	MDI mode: second pair in 1000Base-T (i.e. the BI_DB+/- pair), receive pair in 10/100Base-T.

MDI[1]-	MDI crossover mode: acts as the BI_DA+/- pair, transmit pair in 10/100Base-T.
MDI[2]+ / MDI[2]-	MDI mode: third pair in 1000Base-T (i.e. the BI_DC+/- pair). MDI crossover mode: acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	MDI mode: fourth pair in 1000Base-T (i.e. the BI_DD+/- pair). MDI crossover mode: acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

6.4 USB x4 Stack Connector (USB6/USB7/USB8/USB9) (J20)

USB Ports 6, 7, 8 and 9 are mounted in a single stack in the IO Area type Foxconn UB11123-Q8DF-4F or similar. The USB ports are controlled by a single set of OHCI and EHCI controllers (also shared by USB5).

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).
The EHCI controllers support USB2.0, High-Speed (480Mbps).

Note	Type	Signal	PIN	Signal	Type	Note
	PWR	5V/SB5V	1 2	GND	PWR	
	DSIO-3.3	USB6-	3 4	USB6+	DSIO-3.3	
	PWR	5V/SB5V	1 2	GND	PWR	
	DSIO-3.3	USB7-	3 4	USB7+	DSIO-3.3	
	PWR	5V/SB5V	1 2	GND	PWR	
	DSIO-3.3	USB8-	3 4	USB8+	DSIO-3.3	
	PWR	5V/SB5V	1 2	GND	PWR	
	DSIO-3.3	USB9-	3 4	USB9+	DSIO-3.3	

Signal	Description
USB6+ USB6- USB7+ USB7- USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by individual resettable 1A fuse.

Notes: ***In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.***

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these

pinsTo protect the external power lines of peripheral devices make sure that
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

6.5 Audio Interface (J40)

The on-board Audio circuit, based on Via VT1708S, implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs. The Following Audio connector is available in IO Area.

Audio Speakers, Line-in and Microphone are available in the stacked audiojack connector type Lotes ABA-JAK-028-K03

	Signal	Type	Note
TIP	LINE1-L	IA	
RING	LINE1-R	IA	
SLEEVE	GND	PWR	
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	
RING	MIC1-R	IA	
SLEEVE	GND	PWR	

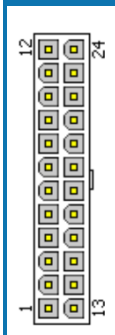
Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
MIC1-L	Microphone 1 - Left	Shared with Audio Header
MIC1-R	Microphone 1 - Right	Shared with Audio Header
LINE1-L	Line 1 signal - Left	Shared with Audio Header
LINE1-R	Line 1 signal - Right	Shared with Audio Header

7 Pin Connectors

7.1 DC Power ATX-BTX Connector (J17)

The KTA75 boards are designed to be supplied from a standard ATX (or BTX) power supply. Use of BTX supply is not required for operation, but may be required to drive high-power PCIe cards.

ATX-BTX Power Connector (J17):

Header	Note	Type	Signal	PIN		Signal	Type	Note
		PWR	3V3	12	24	GND	PWR	
		PWR	+12V	11	23	5V	PWR	
		PWR	+12V	10	22	5V	PWR	
		PWR	SB5V	9	21	5V	PWR	
		I	P_OK	8	20	-5V	PWR	1
		PWR	GND	7	19	GND	PWR	
		PWR	5V	6	18	GND	PWR	
		PWR	GND	5	17	GND	PWR	
		PWR	5V	4	16	PSON#	OC	
		PWR	GND	3	15	GND	PWR	
		PWR	3V3	2	14	-12V	PWR	
		PWR	3V3	1	13	3V3	PWR	

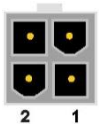
Note 1: -5V supply is not used on-board.

See chapter "Power Consumption" regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised on-board.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

7.2 DC Power Internal Connector (J19)

The KTA75/Flex has an internal power input connector for supplying voltage in the range from +11.4V to +12.6V. The power connector is a 4 pin 12V ATX connector type Lotes ABA-POW-003-K02 or similar.

Header	Pin	Signal	Description
	1	GND	Ground
	2	GND	Ground
	3	12V	Power supply +12V
	4	12V	Power supply +12V

Warning: Hot Plugging power supply is not supported. Hot plugging might damage the board.

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of all KTQ67 board versions.

Notes: ***To protect the external power lines of peripheral devices make sure that***
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

Alternatively the DC Power External Connector can be used

7.3 Audio Header Connector (J41)

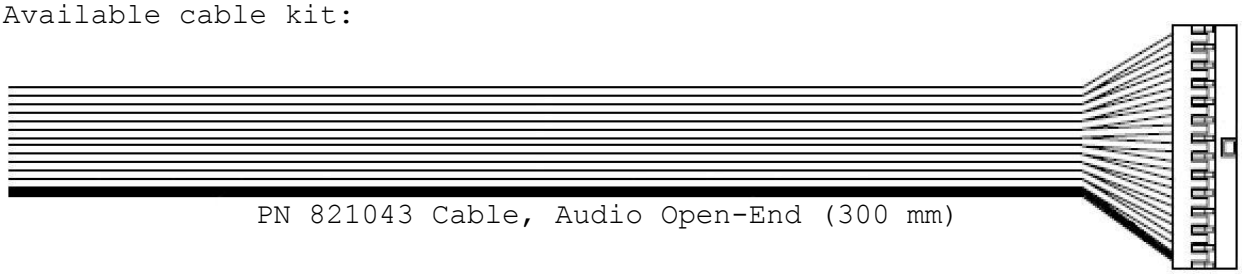
The Audio Header connector is a 26 pin connector type Molex 87832-2620 or similar.

Note	Type	Signal	PIN		Signal	Type	Note
	AO	LFE-OUT	1	2	CEN-OUT	AO	
	PWR	AAGND	3	4	AAGND	PWR	
1	AO	FRONT-OUT-L	5	6	FRONT-OUT-R	AO	1
	PWR	AAGND	7	8	AAGND	PWR	
	AO	REAR-OUT-L	9	10	REAR-OUT-R	AO	
	AO	SIDE-OUT-L	11	12	SIDE-OUT-R	AO	
	PWR	AAGND	13	14	AAGND	PWR	
1	AI	MIC1-L	15	16	MIC1-R	AI	1
	PWR	AAGND	17	18	AAGND	PWR	
1		LINE1-L	19	20	LINE1-R		1
	NC	NC	21	22	AAGND	PWR	
	PWR	GND	23	24	NC	NC	
	O	SPDIF-OUT	25	26	GND	PWR	

Note 1: Shared with Audio Stack connector (in Rear IO area).

Signal	Description
FRONT-OUT-L	Front Speakers (Speaker Out Left).
FRONT-OUT-R	Front Speakers (Speaker Out Right).
REAR-OUT-L	Rear Speakers (Surround Out Left).
REAR-OUT-R	Rear Speakers (Surround Out Right).
SIDE-OUT-L	Side speakers (Surround Out Left)
SIDE-OUT-R	Side speakers (Surround Out Right)
CEN-OUT	Center Speaker (Center Out channel).
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).
NC	No connection
MIC1	MIC Input 1
LINE1	Line 1 signals
F-SPDIF-OUT	S/PDIF Output
AAGND	Audio Analogue ground

Available cable kit:



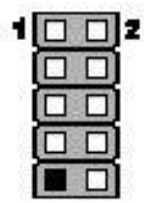
PN 821043 Cable, Audio Open-End (300 mm)

7.4 USB4/5 Connector (J16)

USB Ports 4 and 5 are available via Pin Row connector type Foxconn HS1105F-RNP9 or similar.

The USB4 port is controlled by a set of OHCI and EHCI controllers (also shared by USB0/1/2).
The USB5 port is controlled by a set of OHCI and EHCI controllers (also shared by USB6/7/8/9).

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).
The EHCI controllers support USB2.0, High-Speed (480Mbps).

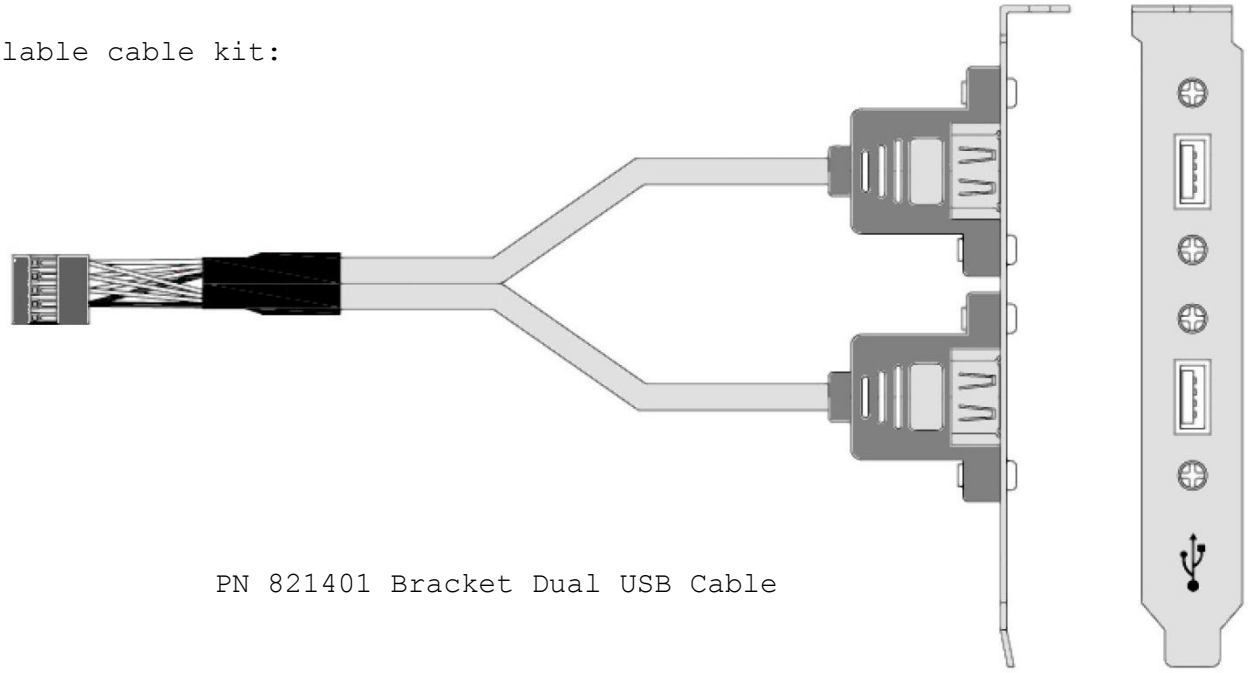
Header	Pin	Signal	Description	Type
	1	5V/SB 5V	5V (always) protected by separate 1A resettable fuse	PWR
	2	5V/SB 5V	5V (always) protected by separate 1A resettable fuse	PWR
	3	USB4-	Differential pair 4 -	DSIO-3.3
	4	USB5-	Differential pair 5 -	DSIO-3.3
	5	USB4+	Differential pair 4 +	DSIO-3.3
	6	USB4+	Differential pair 5 +	DSIO-3.3
	7	GND	Ground	PWR
	8	GND	Ground	PWR
	-		(pin not mounted -Used for keying)	
	10	KEY		NC

Notes: ***In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.***

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

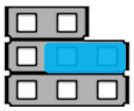
Available cable kit:



PN 821401 Bracket Dual USB Cable

7.5 Jumper area (J34, J35, J36, J37)

The KTA75 has a jumper area containing pin connectors 2.54mm pitch, for up to four jumpers, but normally only one jumper is used (jumper in the J34 pin 2-3 position, as indicated below).

Function	J#	Jumper in position 1-2	Pin 1 2 3	Jumper in position 2-3
Always On	J37	-		Always On
Clear CMOS	J34	Clear CMOS		Normal (Default)
Audio Short circuit test	J36	Front Right		Front Left
Not mounted	J35	-		-

Clear CMOS: is used to erase all customised BIOS settings located in the CMOS RAM storage. If the board has a booting problem or is unstabile, then Clearing CMOS by moving the Jumper from default position to the Clear CMOS position for approx. 10 sec. might solve the problem.

Audio Short Circuit Test: is only used in manufacturing test. No jumper should be installed.

Warning: Don't leave the Clear CMOS jumper in position 1-2, otherwise if power is disconnected, the battery will fully deplete within a few weeks.

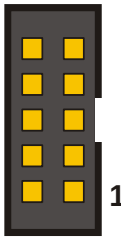
7.6 SPI Connector (J21)

The KTA75 provides one synchronous full duplex SPI (Serial Peripheral Interface) Bus in a 10 pin header connector. The connector is type Pinrex 512-90-10GBE5 or similar.

Two things should be considered:

1. An onboard SPI™ flash coexists on the same interface lines. You must disable this component with a 3.3V power connection to the ADDIN signal (e.g. a short circuit jumper between pin 2 and 4).

2. The four SPI™ lines are protected with an additional bus driver and the ISOLATE# signal controls the output enable pin. For normal operation this signal should be high.

Header	Pin	Signal	Description	Type
	1	SPI_CLK	SPI clock	O-3.3
	2	3.3V	Power +3.3V	PWR
	3	SPI_CS#	SPI slave select, active low	O-3.3
	4	ADDIN	Disable onboard SPI flash	I-3.3
	5	RSVD	Reserved (10k pullup to 3.3V)	PWR
	6	N.C.	Not connected	NC
	7	SPI_MOSI	SPI master output, Slave Input	IO-3.3
	8	ISOLATE#	Disable the SPI interface	I-3.3
	9	SPI_MISO	SPI master input, Slave Output	IO-3.3
	10	GND	Ground	PWR

Signal	Further description
SB3V3	3.3V Standby Voltage power line. Normally output power, but when Motherboard is turned off then the on-board SPI Flash can be 3.3V power sourced via this pin.
ISOLATE#	The ISOLATE# input, active low, is normally NC, but must be connected to GND when loading SPI flash. Power Supply to the Motherboard must be turned off when loading SPI flash. The pull up resistor is connected via diode to 5VSB.

7.7 COM1/COM2 (J23/J22)

Two serial ports provide asynchronous serial communication via RS-232 interfaces. The connector is type Pinrex 512-90-10GBE5 or similar.

The pinout of Serial ports COM1 and COM2 is as follows:

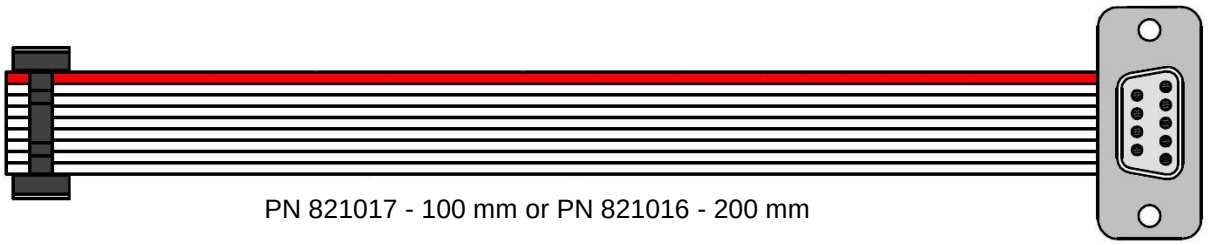
Note	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Note
	-	I	DCD	1 2	DSR	I	-	
	-	I	RxD	3 4	RTS	O		
		O	TxD	5 6	CTS	I	-	
		O	DTR	7 8	RI	I	-	
	-	PWR	GND	9 10	5V	PWR	-	1

Note 1: The COM1 and COM4 5V supply is fused with a common 1.1A resettable fuse.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

Available cable kit (DB9 adapter cables):



PN 821017 - 100 mm or PN 821016 - 200 mm

7.8 LPC Connector (J29)

The LPC connector is unsupported. The connector is type Foxconn HC11101-P0 or similar.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	NC				

7.9 Front Panel Connector (J5)

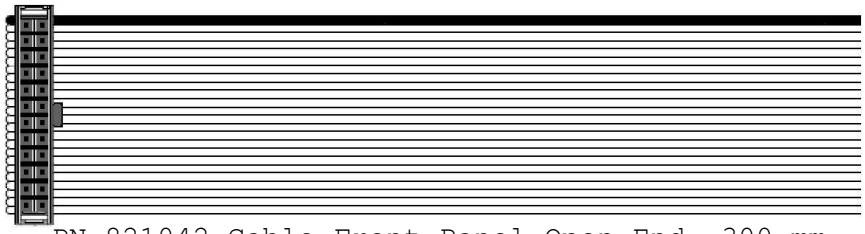
The Front Panel connector is a 24 pin connector type Wieson G2120HT0038-016 or similar.

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN	Signal	Type	Ioh / Iol	Pull U/D	Note
	-	-	PWR	USB0_5V	1 2	USB1_5V	PWR	-	-	
	-	-		USB0-	3 4	USB1-		-	-	
	-	-		USB0+	5 6	USB1+		-	-	
	-	-	PWR	GND	7 8	GND	PWR	-	-	
	-	-	NC	NC	9 10	LINE2-L		-	-	
	-	-	PWR	+5V	11 12	+5V	PWR	-	-	
	-	25/25mA	O	SATA_LED#	13 14	SUS_LED	O	7mA	-	
	-	-	PWR	GND	15 16	PWRBTN_IN#	I		1K1	
	4K7	-	I	RSTIN#	17 18	GND	PWR	-	-	
	-	-	PWR	SB3V3	19 20	LINE2-R		-	-	
	-	-	PWR	AGND	21 22	AGND	PWR	-	-	
	-	-	AI	MIC2-L	23 24	MIC2-R	AI	-	-	

Signal	Description
USB0_5V/USB1_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by independed resettable 1.1A fuse.
USB0+/USB0-	Universal Serial Bus Port 0 Differentials: Bus Data/Address/Command Bus.
USB1+/USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A if using IDC connector or 2A if using crimp terminals .
SATA_LED#	SATA Activity LED (active low signal). 3V3 output when passive.
SUS_LED	Suspend Mode LED (active high signal). Output 3.3V via 470Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2	Line2 is second stereo Line signals
MIC2	MIC2 is second stereo microphone input.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

Note: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

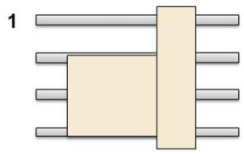
Available cable kit:



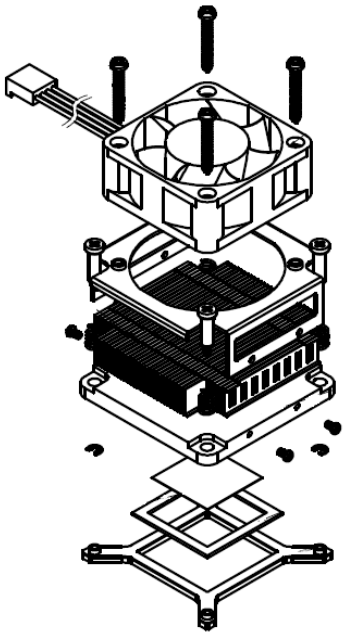
PN 821042 Cable Front Panel Open-End, 300 mm

7.10 CPU/System Fan Connectors (J25, J24)

The CPU Fan connector and the System Fan connector are identical 4 pin type connectors. The type is Tyco 1470947-1 or similar.

Header	Pin	Signal	Description	Type
	1	PWM	PWM output	O-3.3
	2	TACHO	Tacho signal (open drain)	I
	3	12V	Power +12V	PWR
	4	GND	Ground	PWR

Signal	Description
PWM	PWM is output signal used to control the fan speed (only for 4-wire Fans).
Tacho	Tarcho input signal is used to monitor the rotation speed RPM (Rotation Per Minute). Prepared for to pulses per turn.



The CPU Fan (PN 1044-9447) can be premounted on the KTA75/Flex.

The fan is a 12V, Ball Bearing type.
PWM 0 – 100% control making speed in range 0 – 8000 RPM ±10%
(Max. startup PWM is 35%)
Power consumption up to 3,6W
MTBF 70000 Hours @ 40°C

7.11 Feature Connector (J26)

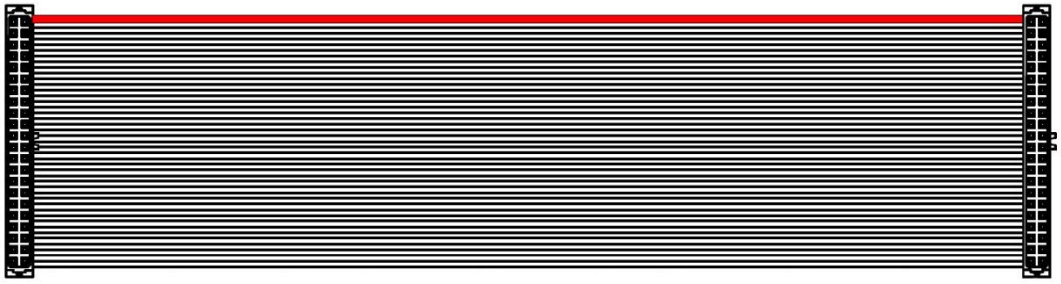
The Feature Connector is a 44 pin connector, 2 mm pitch, type Foxconn HS5422F or similar.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	CASE_OPEN#	1 2	SMBC		/4mA	10K/	1
	-	25/25mA	O	S5#	3 4	SMBD		/4mA	10K/	1
	-	25/25mA	O	PWR_OK	5 6	EXT_BAT	PWR	-	-	
4	-		O	FAN3OUT	7 8	FAN3IN	I	-	10K/	4
	-	-	PWR	SB3V3	9 10	SB5V	PWR	-	-	
	-		IOT	GPIO0	11 12	GPIO1	IOT		-	
	-		IOT	GPIO2	13 14	GPIO3	IOT		-	
	-		IOT	GPIO4	15 16	GPIO5	IOT		-	
	-		IOT	GPIO6	17 18	GPIO7	IOT		-	
	-	-	PWR	GND	19 20	GND	PWR	-	-	
	-		I	GPIO8	21 22	GPIO9	I		-	
3	-		NC	GPIO10	23 24	GPIO11	NC		-	3
	-		I	GPIO12	25 26	GPIO13	IOT		-	
	-		IOT	GPIO14	27 28	GPIO15	IOT		-	
	-		IOT	GPIO16	29 30	GPIO17	NC		-	3
	-	-	PWR	GND	31 32	GND	PWR	-	-	
	-	8/8mA	O	EGCLK	33 34	EGCS#	O	8/8mA	-	
	-	8/8mA		EGAD	35 36	TMA0	O			
	-		PWR	+12V	37 38	GND	PWR	-	-	
4	-		O	FAN4OUT	39 40	FAN4IN	I	-	10K/	4
	-	-	PWR	GND	41 42	GND	PWR	-	-	
	-	-	PWR	GND	43 44	S3#	O	25/25mA	-	

Notes:

1. Pull-up to SB3V3.
2. Pull-up to on-board Battery.
3. Not connected, used for onboard feature.
4. Not supported.

Available cable kit:



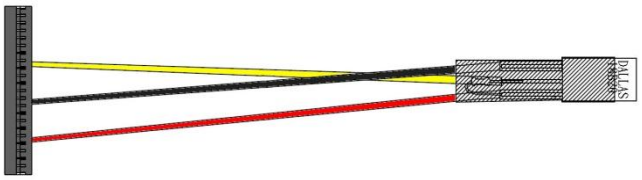
PN 1052-5885 Cable, Feature 44pol 1 to1, 300mm

Signal	Description
CASE_OPEN#	CASE OPEN, used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
SMBC	SMBus Clock signal
SMBD	SMBus Data signal
S3#	S3 sleep mode, active low output, optionally used to deactivate external system.
S5#	S5 sleep mode, active low output, optionally used to deactivate external system.
PWR_OK	PoWeR OK, signal is high if no power failures are detected. (This is not the same as the P_OK signal generated by ATX PSU).
EXT_BAT *	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 - 4.0 V) (- terminal connected to GND). The external battery is protected against charging and can be used with/without the on-board battery installed.
FAN3OUT	Not Supported
FAN3IN	Not Supported
FAN4OUT	Not Supported
FAN4IN	Not Supported
SB3V3	+3.3V StandBy voltage, max. load 1 Amp
SB5V	+5V StandBy voltage
GPIO0..17	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface). Note: GPIO11 not available (internaly used as 12V monitor)
EGCLK	Extend GPIO Clock signal
EGAD	Extend GPIO Address Data signal
EGCS#	Extend GPIO Chip Select signal, active low
TMA0	Timer Output
+12V	+12V, max. load 1 Amp.

(*) = Not verified.

Available Temperature Sensor cable kit (for System Fan Temperature Cruise, selected in BIOS):

Based on Maxim DS18B20, Accurate to ±0.5°C over the range of -10°C to +85°C
Feature connector 3.3V (Pin 9), GND (Pin 19) and GPIO16 (Pin 29)



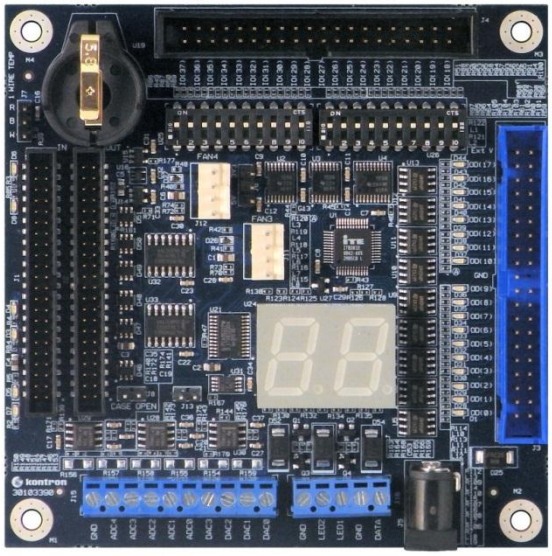
PN1053-4925 Cable Temperature Sensor - 44P, 400 mm

GPIO in more details:

The GPIO's are controlled via the ITE IT8516F Embedded Controller. Each GPIO has 100pF to ground, clamping Diode to 3V3 and has multiplexed functionality. Some pins can be DAC (Digital to Analogue Converter output), PWM (Pulse Width Modulated signal output), ADC (Analogue to Digital Converter input), TMRI (Timer Counter Input), WUI (Wake Up Input), RI (Ring Indicator Input) or some special function.

Signal	IT8516F pin name	Type	Description
GPIO0	DAC0/GPJ0	AO/IOS	
GPIO1	DAC1/GPJ1	AO/IOS	
GPIO2	DAC2/GPJ2	AO/IOS	
GPIO3	DAC3/GPJ3	AO/IOS	
GPIO4	PWM2/GPA2	O8/IOS	
GPIO5	PWM3/GPA3	O8/IOS	
GPIO6	PWM4/GPA4	O8/IOS	
GPIO7	PWM5/GPA5	O8/IOS	
GPIO8	ADC0/GPI0	AI/IS	
GPIO9	ADC1/GPI1	AI/IS	
GPIO10	ADC2/GPI2	AI/IS	
GPIO11	ADC3/GPI3	AI/IS	Reserved, used for +12V monitoring
GPIO12	ADC4/WUI28/GPI4	AI/IS/IS	
GPIO13	RI1#/WUI0/GPD0	IS/IS/IOS	
GPIO14	RI2#/WUI1/GPD1	IS/IS/IOS	
GPIO15	TMRI0/WUI2/GPC4	IS/IS/IOS	
GPIO16	TMRI1/WUI3/GPC6	IS/IS/IOS	Optionally for Cable Temperature sensor
GPIO17	L80HLAT/BAO/WUI24/GPE0	O4/O4/IS/IOS	

Feature Break-out board:



PN 820978 Feature BOB (Break-Out-Board)

7.12 KBD/MSE (J27)

Attachment of a PS/2 keyboard/mouse can be done through the pinrow connector KBDMSE (J27) type Molex 22-23-2061 or similar.

Both interfaces utilize open-drain signalling with on-board pull-up.

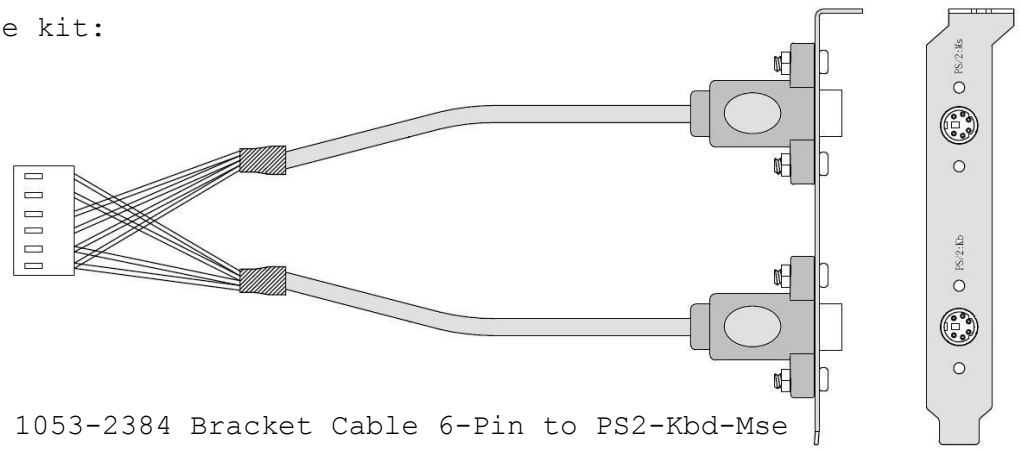
The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOD	/14mA	2K7	
2	KBDDAT	IOD	/14mA	2K7	
3	MSCLK	IOD	/14mA	2K7	
4	MSDAT	IOD	/14mA	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

Available cable kit:



PN 1053-2384 Bracket Cable 6-Pin to PS2-Kbd-Mse

8 Slot Connectors (PCI-Express, miniPCIe, PCI, SATA, mSATA)

8.1 PCIex16 (in x16 slot) (J7)

The PCIex16 (16-lane PCI Express) is available through a PCIe x16 slot and support PCIe 2.0. The slot can be used for external PCI Express cards inclusive graphics card and dedicated TMDS passive card. The slot is located nearest the edge of the board. Maximum theoretical bandwidth using 16 lanes is 8 GB/s.

Note	Type	Signal	PIN	Signal	Type	Note
		+12V	B1 A1	GND via 0 Ohm		
		+12V	B2 A2	+12V		
		+12V	B3 A3	+12V		
		GND	B4 A4	GND		
		SMB_CLK	B5 A5	NC		
		SMB_DATA	B6 A6	SCL5-AUX5P		
		GND	B7 A7	SCA5-AUX5N		
		+3V3	B8 A8	NC		
		DP5 HP	B9 A9	+3V3		
		SB3V3	B10 A10	+3V3		
		WAKE#	B11 A11	RST#		
		NC	B12 A12	GND		
		GND	B13 A13	PCIE_x16 CLKP		
		PEG_TXP[0]	B14 A14	PCIE_x16 CLKN		
		PEG_TXN[0]	B15 A15	GND		
		GND	B16 A16	PEG_RXP[0]		
		CLKREQ	B17 A17	PEG_RXN[0]		
		GND	B18 A18	GND		
		PEG_TXP[1]	B19 A19	NC		
		PEG_TXN[1]	B20 A20	GND		
		GND	B21 A21	PEG_RXP[1]		
		GND	B22 A22	PEG_RXN[1]		
		PEG_TXP[2]	B23 A23	GND		
		PEG_TXN[2]	B24 A24	GND		
		GND	B25 A25	PEG_RXP[2]		
		GND	B26 A26	PEG_RXN[2]		
		PEG_TXP[3]	B27 A27	GND		
		PEG_TXN[3]	B28 A28	GND		
		GND	B29 A29	PEG_RXP[3]		
		NC	B30 A30	PEG_RXN[3]		
		CLKREQ	B31 A31	GND		
		GND	B32 A32	NC		
		PEG_TXP[4]	B33 A33	NC		
		PEG_TXN[4]	B34 A34	GND		

		GND	B35 A35	PEG_RXP[4]		
		GND	B36 A36	PEG_RXN[4]		
		PEG_TXP[5]	B37 A37	GND		
		PEG_TXN[5]	B38 A38	GND		
		GND	B39 A39	PEG_RXP[5]		
		GND	B40 A40	PEG_RXN[5]		
		PEG_TXP[6]	B41 A41	GND		
		PEG_TXN[6]	B42 A42	GND		
		GND	B43 A43	PEG_RXP[6]		
		GND	B44 A44	PEG_RXN[6]		
		PEG_TXP[7]	B45 A45	GND		
		PEG_TXN[7]	B46 A46	GND		
		GND	B47 A47	PEG_RXP[7]		
		CLKREQ	B48 A48	PEG_RXN[7]		
		GND	B49 A49	GND		
		PEG_TXP[8]	B50 A50	NC		
		PEG_TXN[8]	B51 A51	GND		
		GND	B52 A52	PEG_RXP[8]		
		GND	B53 A53	PEG_RXN[8]		
		PEG_TXP[9]	B54 A54	GND		
		PEG_TXN[9]	B55 A55	GND		
		GND	B56 A56	PEG_RXP[9]		
		GND	B57 A57	PEG_RXN[9]		
		PEG_TXP[10]	B58 A58	GND		
		PEG_TXN[10]	B59 A59	GND		
		GND	B60 A60	PEG_RXP[10]		
		GND	B61 A61	PEG_RXN[10]		
		PEG_TXP[11]	B62 A62	GND		
		PEG_TXN[11]	B63 A63	GND		
		GND	B64 A64	PEG_RXP[11]		
		GND	B65 A65	PEG_RXN[11]		
		PEG_TXP[12]	B66 A66	GND		
		PEG_TXN[12]	B67 A67	GND		
		GND	B68 A68	PEG_RXP[12]		
		GND	B69 A69	PEG_RXN[12]		
		PEG_TXP[13]	B70 A70	GND		
		PEG_TXN[13]	B71 A71	GND		
		GND	B72 A72	PEG_RXP[13]		
		GND	B73 A73	PEG_RXN[13]		
		PEG_TXP[14]	B74 A74	GND		
		PEG_TXN[14]	B75 A75	GND		
		GND	B76 A76	PEG_RXP[14]		
		GND	B77 A77	PEG_RXN[14]		
		PEG_TXP[15]	B78 A78	GND		
		PEG_TXN[15]	B79 A79	GND		
		GND	B80 A80	PEG_RXP[15]		
		CLKREQ	B81 A81	PEG_RXN[15]		
		NC	B82 A82	GND		

8.2 PCIex4 (J6)

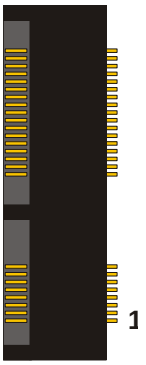
The PCIex4 (4-lane PCI Express) is available through a PCIe x16 slot and support PCIe 2.0. The slot can be used for external PCI Express cards inclusive graphics card. The slot is located nearest the CPU of the board. Maximum theoretical bandwidth using 4 lanes is 4 GB/s.

Note	Type	Signal	PIN	Signal	Type	Note
		+12V	B1 A1	GND via 0 ohm		
		+12V	B2 A2	+12V		
		+12V	B3 A3	+12V		
		GND	B4 A4	GND		
		SMB_CLK	B5 A5	NC		
		SMB_DATA	B6 A6	NC		
		GND	B7 A7	NC		
		+3V3	B8 A8	NC		
		NC	B9 A9	+3V3		
		SB3V3	B10 A10	+3V3		
		WAKE#	B11 A11	RST#		
		NC	B12 A12	GND		
		GND	B13 A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14 A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15 A15	GND		
		GND	B16 A16	PEG_RXP[0]		
		CLKREQ	B17 A17	PEG_RXN[0]		
		GND	B18 A18	GND		
		PEG_TXP[1]	B19 A19	NC		
		PEG_TXN[1]	B20 A20	GND		
		GND	B21 A21	PEG_RXP[1]		
		GND	B22 A22	PEG_RXN[1]		
		PEG_TXP[2]	B23 A23	GND		
		PEG_TXN[2]	B24 A24	GND		
		GND	B25 A25	PEG_RXP[2]		
		GND	B26 A26	PEG_RXN[2]		
		PEG_TXP[3]	B27 A27	GND		
		PEG_TXN[3]	B28 A28	GND		
		GND	B29 A29	PEG_RXP[3]		
		NC	B30 A30	PEG_RXN[3]		
		CLKREQ	B31 A31	GND		
		GND	B32 A32	NC		
		NC	B33 A33	NC		
		NC	B34 A34	GND		
		GND	B35 A35	NC		
		GND	B36 A36	NC		
		NC	B37 A37	GND		
		NC	B38 A38	GND		

		GND	B39 A39	NC		
		GND	B40 A40	NC		
		NC	B41 A41	GND		
		NC	B42 A42	GND		
		GND	B43 A43	NC		
		GND	B44 A44	NC		
		NC	B45 A45	GND		
		NC	B46 A46	GND		
		GND	B47 A47	NC		
		CLKREQ	B48 A48	NC		
		GND	B49 A49	GND		
		NC	B50 A50	NC		
		NC	B51 A51	GND		
		GND	B52 A52	NC		
		GND	B53 A53	NC		
		NC	B54 A54	GND		
		NC	B55 A55	GND		
		GND	B56 A56	NC		
		GND	B57 A57	NC		
		NC	B58 A58	GND		
		NC	B59 A59	GND		
		GND	B60 A60	NC		
		GND	B61 A61	NC		
		NC	B62 A62	GND		
		NC	B63 A63	GND		
		GND	B64 A64	NC		
		GND	B65 A65	NC		
		NC	B66 A66	GND		
		NC	B67 A67	GND		
		GND	B68 A68	NC		
		GND	B69 A69	NC		
		NC	B70 A70	GND		
		NC	B71 A71	GND		
		GND	B72 A72	NC		
		GND	B73 A73	NC		
		NC	B74 A74	GND		
		NC	B75 A75	GND		
		GND	B76 A76	NC		
		GND	B77 A77	NC		
		NC	B78 A78	GND		
		NC	B79 A79	GND		
		GND	B80 A80	NC		
		CLKREQ	B81 A81	NC		
		NC	B82 A82	GND		

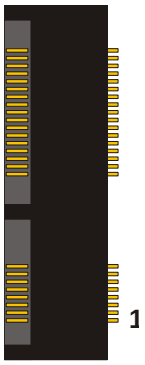
8.3 mPCIe connector (J38)

The mPCIe (mini PCI Express) port is PCIe 2.0 compliant and it supports USB (port USB2).

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
	1	Wake#	Wake event	I-3.3	2	3.3V	Power +3.3V	PWR
	3	N.C.	-	NC	4	Gnd	Ground	PWR
	5	N.C.	-	NC	6	1.5V	Power +1.5V	PWR
	7	Clkreq#	Clock request	I-3.3	8	N.C.	-	NC
	9	GND	Ground	PWR	10	N.C.	-	NC
	11	PE_Clk-	PCIe® clock-	DSO	12	N.C.	-	NC
	13	PE_Clk+	PCIe® clock+	DSO	14	N.C.	-	NC
	15	GND	Ground	PWR	16	N.C.	-	NC
	17	N.C.	-	NC	18	Gnd	Ground	PWR
	19	N.C.	-	NC	20	W_Disable#	Wireless disable	O-3.3
	21	GND	Ground	PWR	22	PE_RST#	PCIe® reset	O-3.3
	23	PE_RX-	PCIe® receive-	DSI	24	3.3V	Power +3.3V	PWR
	25	PE_RX+	PCIe® receive+	DSI	26	Gnd	Ground	PWR
	27	Gnd	Ground	PWR	28	1.5V	Power +1.5V	PWR
	29	Gnd	Ground	PWR	30	I2C_Clk	I2C™ clock	O-3.3
	31	PE_TX-	PCIe® transmit-	DSO	32	I2C_Data	I2C™ data	IO-3.3
	33	PE_TX+	PCIe® transmit+	DSO	34	Gnd	Ground	PWR
	35	Gnd	Ground	PWR	36	USB2-	Diff. pair USB2 -	DSIO 0.4V
	37	Gnd	Ground	PWR	38	USB2+	Diff. pair USB2 +	DSIO-0.4V
	39	3.3V	Power +3.3V	PWR	40	Gnd	Ground	PWR
	41	3.3V	Power +3.3V	PWR	42	N.C.	-	NC
	43	Gnd	Ground	PWR	44	N.C.	-	NC
	45	N.C.	-	NC	46	N.C.	-	NC
	47	N.C.	-	NC	48	1.5V	Power +1.5V	PWR
	49	N.C.	-	NC	50	Gnd	Ground	PWR
	51	N.C.	-	NC	52	3.3V	Power +3.3V	PWR

8.4 mSATA/mPCIe Connector (J43)

The mSATA/mPCIe interface comply with SATA 3.0 and it supports USB (port USB2)

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
 1	1	Wake#	Wake event	I-3.3	2	3.3V	Power +3.3V	PWR
	3	N.C.	-	NC	4	Gnd	Ground	PWR
	5	N.C.	-	NC	6	1.5V	Power +1.5V	PWR
	7	Clkreq#	Clock request	I-3.3	8	N.C.	-	NC
	9	Gnd	Ground	PWR	10	N.C.	-	NC
	11	PE_CLK-	PCIe® clock-	DSO	12	N.C.	-	NC
	13	PE_CLK+	PCIe® clock+	DSO	14	N.C.	-	NC
	15	Gnd	Ground	PWR	16	N.C.	-	NC
	17	N.C.	-	NC	18	Gnd	Ground	PWR
	19	N.C.	-	NC	20	W_Disable#	Wireless disable	O-3.3
	21	Gnd	Ground	PWR	22	PE_RST#	PCIe® reset	O-3.3
	23	SATA_RX+	S-ATA® receive+	DSI	24	3.3V	Power +3.3V	PWR
	25	SATA_RX-	S-ATA® receive-	DSI	26	Gnd	Ground	PWR
	27	Gnd	Ground	PWR	28	1.5V	Power +1.5V	PWR
	29	Gnd	Ground	PWR	30	I2C_Clk	I2C™ clock	IO-3.3
	31	SATA_TX-	S-ATA® transmit-	DSO	32	I2C_Data	I2C™ data	IO-3.3
	33	SATA_TX+	S-ATA® transmit+	DSO	34	Gnd	Ground	PWR
	35	Gnd	Ground	PWR	36	USB3-	Diff. pair USB3 -	DSIO-0.4V
	37	Gnd	Ground	PWR	38	USB3+	Diff. pair USB3 +	DSIO-0.4V
	39	3.3V	Power +3.3V	PWR	40	Gnd	Ground	PWR
	41	3.3V	Power +3.3V	PWR	42	N.C.	-	NC
	43	Gnd	Ground	PWR	44	N.C.	-	NC
	45	N.C.	-	NC	46	N.C.	-	NC
	47	N.C.	-	NC	48	1.5V	Power +1.5V	PWR
	49	N.C.	-	NC	50	Gnd	Ground	PWR
	51	Sel_SATA#	S-ATA® identification	I-1.8	52	3.3V	Power +3.3V	PWR

8.5 PCI slot connectors (J18 & J28)

KTA75/Flex support 2 PCI slots PCI0 – PCI1 (J18 – J28).

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
NC	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
NC	-	-	F09	E09	-	-	NC
NC	-	-	F10	E10	+5V (I/O)	PWR	
NC	-	-	F11	E11	-	-	NC
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
NC	-	-	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0/1#	OT	
	I	REQ0/1#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

8.5.1 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the risingedge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
PME#	Power Management Event interrupt signal. Wake up signal.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY#

	and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 55signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s

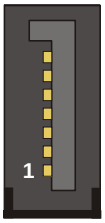
	to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

8.6 SATA0, SATA1, SATA2, SATA3, SATA4 & SATA5 (J12, J13, J9, J11, J10 & J39)

The six SATA ports comply with SATA 3.0 and supports IDE emulation mode, AHCI (Advanced Host Controller Interface) 1.3 mode and RAID mode (RAID 0, RAID 1 and RAID10) across all 6 ports.

The SATA 3.0 supports transfer rates up to 6 Gbit/s, but also SATA 1.0 and SATA 2.0 transfer rates are supported, 1.5 Gbit/s and 3.0 Gbit/s respectively.

The S-ATA® interface is available through standard L-type connector (7 pins).

Header	Pin	Signal	Description	Type
	1	GND	Ground	PWR
	2	TX+	Transmit (positive)	DSO
	3	TX-	Transmit (negative)	DSO
	4	GND	Ground	PWR
	5	RX-	Receive (negative)	DSI
	6	RX+	Receive (positive)	DSI
	7	GND	Ground	PWR

Available cable kit:

PN 821035 Cable SATA 500mm

Appendix: Mating Connectors

The Mating connectors / Cables are connectors or cable kits which are fitting the On-board connector.

Connector		Onboard Connectors		Mating Connectors	
		Manufacturer	P/N	Manufacturer	P/N
DisplayPort	J3/J4/J43	Foxconn	3VD11203-H7AB-4H		
USB10/USB11/USB12/USB13	J14/J15	Lotes	ABA-USB-104-K01		
ETH1/ETH2	J8	Ude	RMT-123AGF1F		
USB6/USB7/USB8/USB9	J20	Foxconn	UB11123-Q8DF-4F		
Audio stack	J40	Lotes	ABA-JAK-028-K03		
Power ATX-BTX	J17	Molex	44206-0002	Molex	5557-24R
Power ATX-core	J19	Lotes	ABA-POW-003-K02	Molex	39-01-2045
Audio Header	J41	Molex	87832-2620	Molex	51110-2651
USB4/USB5	J16	Foxconn	HS1105F-RNP9		
SPI	J21	Pinrex	512-90-10GBE5		
COM1/COM2	J22/J23	Pinrex	512-90-10GBE5	Molex	90635-1103
LPC	J29	Foxconn	HC11101-P0		
Frontpanel	J5	Wieson	G2120HT0038-016	Molex	90635-1243
CPU Fan/System Fan	J24/J25	Tyco	1470947-1	Molex	47054-1000
Feature	J26	Pinrex	52C-90-44GB00	Don Connex	A05c-44-B-G-A-1-G
		Foxconn	HS5422F		
KBD/MSE	J27	Molex	22-23-2061	Molex	22-01-2065

Cable & Driver Kit KTA70M/KTA75 (PN 826600-R11) contains:

- 2x PN 821017 Cable, COM, 2.54mm, 100mm
- 1x PN 1052-5885 Cable, Feature 44pol 1 to1, 300mm
- 1x PN 1053-2384 Bracket Cable 6-Pin to PS2-Kbd-Mse
- 1x PN 821042 Cable, Front Panel Open-End
- 1x PN 821043 Cable, Audio Open-End
- 6x PN 821035 Cable, SATA, 500mm
- 1x PN 1052-5814 Cable, ATX Power for KTA70M
- 1x PN 1027-3669 Cable Power Out
- 1x PN 821401 Cable+Bracket, USB, 10poled
- 1x PN 1052-5818 SW,Man&Driver CD,KA70M/KTA75

Appendix: OS Setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTA7x Driver CD or they can be downloaded from the homepage http://www.kontron.com/

For some OS like Win7 when installing OS via USB DVD, USB Keyboard/Mouse, please connect the USB DVD, USB Keyboard/Mouse to USB2.0 ports only or disable USB3.0 in BIOS.

Corporate Offices

Europe, Middle East & Africa

Oskar-von-Miller-Str. 1
85386 Eching/Munich
Germany
Tel.: +49 (0) 8165/ 77 777
Fax: +49 (0) 8165/ 77 219
info@kontron.com

North America

14118 Stowe Drive
Poway, CA 92064-7147
USA
Tel.: +1 888 294 4558
Fax: +1 858 677 0898
info@us.kontron.com

Asia Pacific

17 Building,Block #1,ABP
188 Southern West 4th Ring Road
Beijing 100070, P.R.China
Tel.: + 86 10 63751188
Fax: + 86 10 83682438
info@kontron.cn