User's Manual

Model XLM72
Universal Logic Module
for
VME Systems

Revision A

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JTEC Model XLM72
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1. OVERVIEW

JTEC Model XLM72 is a highly versatile, general-purpose, programmable universal logic module for use in VME-based systems. The desired logic operations are performed by a Xilinx XCS40XL Field Programmable Gate Array (FPGA), while more elaborate numeric operations are performed by a Texas Instruments 900-Mflops/s floating-point Digital Signal Processor (DSP) TMS320C6711. It communicates with external devices via 72 programmable, front-panel ECL ports, which can be configured in quartets either as input or output ports. The ECL ports are mapped onto the ports of the user FPGA. On the other end, XLM72 communicates with computers via the VMEBus, utilizing 32-bit addressing and 32-bit and 16-bit data transfer, including 32-bit block transfer at rates of up to 40 Mbytes/s. Further, XLM72 features two banks of fast asynchronous static random access memory (ASRAM), 2 Mbytes each, accessible to VMEBus, FPGA, and DSP, and it features an on-board 2 Mbyte EEPROM or flash memory allowing one to store up four FPGA configuration files.

Few digital applications are out of XLM72 range.

1.1. SUMMARY OF FEATURES

- 72 programmable front-panel ECL ports, configurable in quartets as either inputs or outputs, organized in four 34-pi and one 8-pin headers. Four ports can be configured as external clock ports supporting rates of up to 110 MHz.
- One user-programmable FPGA, XCS40XL-5PQ208C by Xilinx, inc.
- One user-programmable, floating point DSP, TMS320C6711 by Texas instruments, rated at 900 Mflops/s.
- 2 banks of fast asynchronous SRAM, 2 Mbytes each, addressable in 32-bit, 16-bit and 8-bit words.
- A custom, programmable, in-system reconfigurable VMEBus interface and bus router/arbitrator.
- One 2-Mbyte programmable erasable read-only memory holding up to four FPGA configuration files.
- Four front-panel LEDs, one indicating VMEBus operation and the remaining three being user-programmable, mapped onto ports of the user FPGA.

1.2. POSSIBLE APPLICATIONS

- FERA Controller/Data Buffer
- Intelligent Data Buffer
- Scalers, Prescalers, Coincidence Registers, Time Stampers
- Multilevel Trigger Logics
- Digital Delay and Gate Generators
- Detector Readout Processor
- Histogramming Memory

Due to the ultimate parallelism of an FPGA, XLM72 can be programmed to perform multiple functions simultaneously, whether related or completely unrelated. For example, part of XLM72 may be programmed to function as an Intelligent FERA Controller/Buffer, while other parts execute trigger logic, yet another parts serving as a block of gated and ungated scalers, and yet another part serving as digital delay and gate generators.

2. SPECIFICATIONS

Formfactor: 6U VME.

PC Board: 8-layer, double-sided mixed surface-mount and through-hole.

VME Connectors: 96-pin J1, J2, and 30-pin JAUX implementing CERN extensions.

ECL Ports: 72, mapped onto the user FPGA.

LEDs: one to indicate VMEBus operations, three user-programmable, via the FPGA configuration.

Clocks: one 80 MHz - shared by the VMEBus interface and FPGA; one 37.5 MHz for DSP.

External Clock Inputs: up to four, rated at 110 MHz.

FPGA: XCS40XL-5PQ208 by Xilinx.

DSP: TMS320C6711 by Texas Instruments.

ASRAMs: 16 CY7C1024B-15CV, organized in two banks of 2-Mbyte 32-bit memory.

FPGA Configuration Memory: 2-Mbyte AT29C020 by Atmel.

VMEBus Addressing: 32-bit, geographic.

VMEBus Data Transfer: 32-bit and 16-bit; 32-bit block transfer at rates of up to 40 Mbytes/s.

Front Panel: Black, anodized, with white silk-screen labeling; two ejector handles with anodized blue ID plates.

Power Requirements: +5V at approximately 1.5 A; -5.2V at approximately 600 mA; -2V at approximately 100 mA. Depends on ECL port usage.

3. ARCHITECTURE

XLM72 features a number of distinct devices, interconnected by address, data, and control buses in star-like topology. Two devices, the FPGA and the DSP may serve, along with the VMEBus, as bus masters, assuming and releasing control of the buses according to user-programmable routines. A block-diagram of XLM72 is illustrated in Fig. 1.

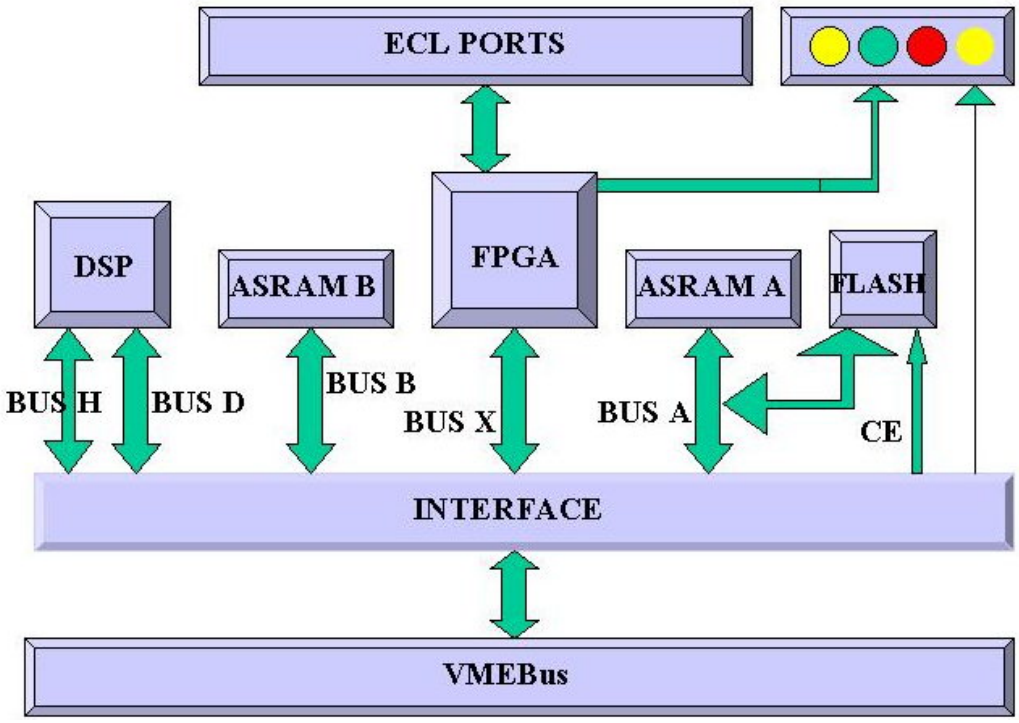

Fig. 1. Block-diagram of XLM72.

Interaction of devices and routing of buses is discussed in Sections 3.1 and 3.2, further below.

3.1. DEVICES

XLM72 features eight distinct devices, five of which are addressable via VMEBus. The addressable devices include:

(i, ii) two banks of fast asynchronous static random access memories (ASRAM),
(iii) one Field-Programmable Gate Array (FPGA),
(iv) one floating-point digital signal processor (DSP) (more accurately, the host processor interface, HPI, of this processor), and

(v) a VMEbus Interface and Bus Arbiter/Router Array (Interface).

The non-addressable (by VMEBus) devices are accessible to the user FPGA and include:

(vi) one flash memory to store configuration data for the FPGA,
(vii) an array of 72 ECL ports, and
(viii) an array of four front-panel diagnostic light-emitting diodes.

3.1.1. ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY

XLM72 features two banks of fast asynchronous static random access memory, referred to as ASRAM A and ASRAM B. Both banks are identical and consist of four CY7C1024B-15VC ICs manufactured by Cypress Semiconductor, Inc., providing for 2 Mbytes of storage capacity, each. They are configured as 32-bit wide memory, but can be also accessed in half-words by both, VMEBus and by the DSP, and by half-words and byte-wise by the FPGA.

3.1.2. FIELD PROGRAMMABLE GATE ARRAY

The desired logical operations of XLM72 are to be programmed by user into a Xilinx XCS40XL-5PQ208C field programmable gate array chip (FPGA). Any logic that can be implemented as synchronous state machine or combinatorial equation may be programmed, subject only to the availability of resources of the XCS40XL chip, which are quite vast. These resources include, among other things:

(i) 1862 logic cells,
(ii) 40,000 system gates,
(iii) 784 complex logic blocks,
(iv) 2,016 flip-flops, and
(v) Fast Carry Logic.

The FPGA is clocked at 80 MHz from an on-board clock, but can be also clocked externally via one of four special ECL ports at rates of up to 110 MHz.

The FPGA can access Interface registers, and both banks of ASRAM. Further, it has exclusive control of Flash Memory, of all ECL ports, and of three out of four front-panel diagnostic LEDs.

3.1.3. DIGITAL SIGNAL PROCESSOR

To allow one to perform more complex numerical operations on data that are beyond the capabilities of the user FPGA, XLM72 is equipped with a Texas Instruments TMS320C6711 floating-point digital signal processor. The processor is clocked at 150 MHz and, given its 6 parallel processors, is rated at 900 MFlops. The DSP can access

select registers of the Interface and both banks of ASRAM, in either 32-bit data words or in 16-bit words. VMEBus can access the DSP via the Host Port Interface (HPI) of the latter.

3.1.4. VMEBUS INTERFACE AND BUS ROUTER/ARBITER

The communication between VMEBus and various devices of XLM72 is mediated by an interface and bus router/arbiter array implemented in four Xilinx Complex Programmable Logic Devices (Interface). The Interface is comprised of one XC95216-10PQ160C and three XC95288XL-7TQ144C chips. Individual CPLDs can be reprogrammed in-system via the on-board JTAG port, allowing one to alter the functionality of the Interface should a need arise. The Interface serves also as a multiple-master bus router and arbiter, such that it may route in parallel bus needs by more than one master. Since XLM72 features three masters, VMEBus, FPGA, and DSP, there is a need not only for bus routing but also for bus arbitration. The needed arbitration scheme is also implemented in the Interface array.

Furthermore, some of the registers of the Interface serve the role of mail boxes for sending messages between the VMEBus, DSP, and the FPGA. In particular, such registers are used to implement interrupt and polling schemes required by various data acquisition systems.

3.1.5. FLASH MEMORY

To provide for the storage of the FPGA configuration data, XLM72 is equipped with one 2 MBit Programmable Erasable Read-Only Memory (Flash Memory), an ATMEL AT29C020-15JC. The size of this memory is sufficient to accommodate up to four configuration files, one of which is a default boot configuration. The Flash Memory is socketed, but can be reprogrammed in system. The chip is rated for 10,000 programming cycles and 20-year data retention.

3.1.6. ECL PORTS

XLM72 is equipped with 72 ECL ports organized in four 34-pin and one 8-pin header. The ports are controlled exclusively by the FPGA and can be configured in quartets as either inputs or outputs, but always unidirectional. Four ECL ports serve special role, as they are associated with clock inputs of the FPGA. As such they can serve as inputs for external clock signals to the FPGA.

3.1.7. DIAGNOSTIC LEDs

XLM72 is equipped with four front-panel light-emitting diodes (LED), one of which (yellow) signals VMEBus operations by the Interface and the remaining three (red, green, and yellow) controlled by the FPGA and, hence, by the user configuration. Every LED is

driven via a pulse-length extender such that even short, 20ns-long pulses produce robust flashes, while long pulses or DC levels are transmitted to the LED unaltered.

3.2. BUSES

Devices of XLM72 and the VMEBus communicate with each other via the VMEBus and five internal buses. All communications are mediated by the Interface, which routes addresses and data generated by the three masters, VMEBus, FPGA, and DSP, to the respective target devices. The Interface allows for a concurrent access of several buses by several masters and performs at the same time the function of the bus arbitrator.

3.2.1. INTERFACE-TO-ASRAM BUSES

The two ASRAMs, ASRAM A and ASRAM B, communicate with the Interface via their respective buses, named Bus A and Bus B, respectively. Each of these buses has 19 address, 32 data, and 3 control lines. Bus A is shared with the Flash Memory, with the exception of one control line, for which the Flash Memory has its individual counterpart.

Buses A and B can be controlled, by any of the three masters, VMEBus, FPGA, and DSP. Which, in practical terms, means that any one of these three masters can write to or read from either of the two banks of ASRAMs.

3.2.2. INTERFACE-TO-FPGA BUS

The FPGA communicates with the Interface via a bus named Bus X, featuring 19 address, 32 data, and 26 control lines. Bus X can be controlled by either the VMEBus or the FPGA.

3.2.3. INTERFACE-TO-DSP BUS

The DSP communicates with the Interface via a bus named Bus D, featuring 19 address, 32 data, and 11 control lines. Bus D is controlled exclusively by the DSP.

3.2.4. INTERFACE-TO-HPI BUS

The Host Processor Interface (HPI) of the DSP communicates with the Interface via a bus named Bus H, featuring 16 data and 7 control lines. Bus H is controlled exclusively by the VMEBus.

3.2.5. BUS ARBITRATION SCHEME

Buses A, B, and X can be controlled by more than one master and, consequently, an arbitration scheme is executed by the Interface to guarantee each of the three masters, the

VMEBus, FPGA, and DSP equal access to these buses, while avoiding bus contention. The arbitration scheme is based on the "first-come-first-serve-release-when-done" principle, where the masters are granted control of buses on first-come-first-serve principle and required to release the control upon completion of a given task.

Masters post their bus requests in the respective bus request registers of the Interface. The requests are placed on the queues associated with individual buses and are granted as soon as the bus involved becomes available. The grant of the bus control is signaled to the requesting master by the content of the respective bus grant register. The requesting master, upon detection of the bus grant signal, takes control of the bus, performs the intended task, and removes its request from the request register, making the bus available to the master that is first in the queue.

3.2.6. INHIBIT OF BUS ACCESS BY FPGA AND DSP

The Interface provides the VMEBus with the unique power to inhibit the control of buses by the remaining two masters, the FPGA and the DSP. In other words, the VMEBus can, at will, "snatch" the bus control already in progress from the FPGA and/or DSP, so as to allow it to perform urgent or emergency tasks of its own. The response of the FPGA and the DSP to the bus "snatching" is at the discretion of the user and is to be programmed into the FPGA and the DSP, respectively. A reasonable programming is assumed to detect the occurrence of "snatching" and provide for its smooth handling, e.g., the abortion of the current operation and release of the request or, when feasible, suspension of the current operation and its resumption upon removal of the bus grant inhibit.

3.3. ADDRESS SPACE

The address spaces of the five addressable devices of XLM72 are defined by 24 bits, A0 – A23 of the complete VMEbus address, bits A24 - A26 being disregarded and bits A27 - A31 carrying the geographical address of XLM72.

ASRAM A	000000h - 1FFFFCh
ASRAM B	200000h - 3FFFFCh
FPGA	400000h - 5FFFFCh, used freely at user's discretion
DSP/HPI	600000h - 7FFFFCh, most of which is unused
INTERFACE	800000h – 9FFFFCh, most of which is unused

4. OPERATING INSTRUCTIONS

Successful operation of XLM72 requires its proper hardware setup, the programming of its user FPGA and/or DSP, and the computer-access of its five addressable devices via VMEBus.

4.1. HARDWARE SETUP

The hardware setup of XLM72 includes (i) configuring its front-panel ECL ports for operation in conjunction with the intended FPGA configuration and (ii) making sure that the three blocks of jumpers, JP34 – JP36 are configured properly. Furthermore, one is expected to connect respective ECL ports to external devices with twisted-pair or flat ribbon cables. The ECL ports are configurable in quartets either as inputs or outputs. The four ports identified by silk-screen labels (on the front panel and on the XLM72 board) as E1-E4 play a special role as they connect via ECL-to-TTL translators (MC10125) to primary (PGCK) clock inputs (E1-E3) and secondary (SGCK) inputs (E4) of FPGA. These FPGA inputs can be used to drive intrinsic clock nets of FPGA. Accordingly, ports E1-E4 can and should be used to supply external clock signals, up to 110 MHz, to XLM72.

4.1.1. IMPORTANT WARNINGS

Improper configuring of ECL ports may lead to the damage of translator ICs or a costly damage of the XLM72 board or of the user FPGA. A special care should be taken to correctly identify and populate the sockets with translator ICs. When not sure, please consult JTEC Support service.

Warning 1: Only one translator IC (either input or output) is allowed for any single port. Which, in practical terms, means that in any horizontal pair of sockets at most one should be filled.

Warning 2: When configuring input ports (MC10125), it must be ascertained that the corresponding ports of the FPGA are configured, indeed, as input ports and not as output ports. In particular, this applies to the default "boot" configuration of the FPGA active upon power-up.

To avoid ports conflict right upon power-up, it is recommended to keep as the default "boot" configuration the general Utility Configuration supplied originally with XLM72, or its possible update. This Utility Configuration has no FPGA ports configured as outputs and, hence, guarantees that there is no conflict with any translator IC.

Warning 3: XLM72 requires differential ECL inputs and will not function properly (no damage will occur, though) with single-ended ECL signals. Which means, among other things, that these inputs cannot be driven by an ECL bus connected to ECL outputs of multiple external devices.

Warning 4: When configuring output ports, make sure that the input-polarizing resistor arrays for the particular quartets of ECL ports, are removed from their respective sockets.

4.1.2. CONFIGURING ECL PORTS

ECL-to-TTL conversion (input) and TTL-to-ECL conversion (output) is accomplished by 16-pin MC10125 and MC10124 ICs, respectively. Each converter IC is capable of interfacing up to four differential ECL ports to respective four TTL ports of the user FPGA. Differential inputs of these ICs are directly connected to respective pairs of pins of front-panel headers. The headers are identified (going from top to bottom) by labels A, B, C, D, and E, respectively while individual ports within a header are identified by numbers 1 through 17 (ports A – D) or 1 through 4 (port E). It is important to note that (as indicated on the front panel of XLM72) port 1 of each of the five headers is represented by the bottom pair of pins of the header and, thus, for example, ports A1-A4 are the four bottom pairs of pins of the top-most 34-pin header.

As indicated by silk-screen labels printed right below each of the two columns of 18 16-pin sockets, the input translators are to be placed into sockets in the right-most column while the output translators are to be inserted into sockets of in the left-most column. The correspondence between the sockets and the ECL ports is indicated by silk-screen labels printed between the two columns of 16-pin sockets. Note that 17-th ports (top-most) of headers A – D are associated with the pair of sockets labeled A17-D17 – 9-th pair from top.

In addition to translator ICs, proper functioning of ECL ports requires either impedance-matching resistor arrays of 8 x 50Ω (input ports) or pull-down resistor arrays of 8 x 470Ω (output ports). These two types of arrays share "Zig-Zag" sockets, with the exception of their first (common) pins, marked by dots. The correspondence between the ECL ports and the (10-position) rows of the "Zig-Zag" sockets is indicated by silk-screen labels printed on both sides of these sockets.

Figure 2 illustrates placement of translator chips and resistor arrays for ECL ports D1-D4 configured as output ports and ports E1-E4 as input ports. Dots indicate pins #1.

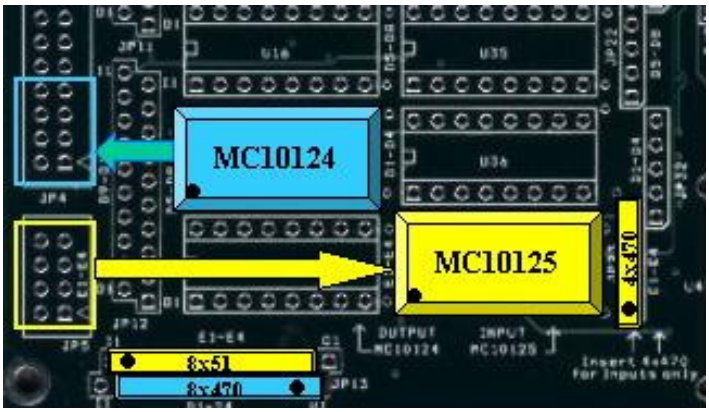

Fig. 2. Placement of ECL port components for inputs (yellow) and outputs (blue).

4.1.2.1. CONFIGURING IMPEDANCE-MATCHING RESISTOR ARRAYS FOR ECL INPUT PORTS

As noted in subsection 4.1.2 further above, to avoid reflections of incoming signals from the ECL input ports, 8 x 50Ωresistor arrays are to be inserted into proper rows of the "Zig-Zag" sockets. Note that each (differential) ECL input is associated with two signal lines and that both these lines need to be terminated. Which is why for one quartet of inputs eight terminating resistors are needed. The 8 x 50Ω arrays are to be inserted with their common pins entering sockets marked as I1 (top-most sockets in the case of the 7 vertical Zig-Zag sockets and left-most sockets in the case of the 2 horizontal Zig-Zag sockets).

Warning: Even though each row of a 20-pin Zig-Zag socket is capable of accommodating a typical commercial 9 x 50Ω resistor array with ten pins, one should use only 8 x 50Ω arrays. This is so, because the pins on the opposite end (with respect to I1) of the Zig-Zag sockets, labeled as O1, are connected to –5.2V, to supply pull-down voltage for output port resistor arrays (8 x 470Ω) (see also sub-section 4.1.2.3).

Note that general rules for bussing of ECL input ports require that only the last port on the bus to have its terminating resistor installed.

4.1.2.2. CONFIGURING INPUT POLARIZING RESISTORS

To guarantee a default logical zero at ECL input ports that are not externally driven, XLM72 provides sockets for respective polarizing (pull-down of complementary ECL input line) resistor arrays. These sockets are located next to the input translator sockets and are associated directly with the adjacent socket. This association is also reflected in the silk-screen label printed next to the socket. Position of the pin 1 (common) is in this case indicated by the "cut corner" of the silk-screen socket outline (bottom). The input-polarizing resistors should be removed when the particular ports are configured as output ports.
Note, that the use of polarizing resistors is not mandatory, unless the user configuration of FPGA relies on a definite polarization. It may be, however, a sound practice to use these resistors with every input translator.

Note that general rules for bussing of ECL input ports require that only the last port on the bus to have its polarizing resistor installed.

4.1.2.3. CONFIGURING OUTPUT PULL-DOWN RESISTORS

For a proper operation of ECL output ports, 8 x 470Ω pull-down resistor arrays are to be inserted into proper rows of the "Zig-Zag" sockets. Note that each (differential) ECL output is associated with two signal lines and that both these lines need to be pulled down, via resistors, to V_{EE}=-5.2V. Which is why for one quartet of outputs, eight pull-down resistors are needed. The 8 x 470Ω arrays are to be inserted with their common

pins entering sockets marked as O1 (bottom sockets in the case of the 7 vertical Zig-Zag sockets and right-most sockets in the case of the 2 horizontal Zig-Zag sockets).

Warning: Even though each row of a 20-pin Zig-Zag socket is capable of accommodating a typical commercial 9 x 470Ω resistor array with ten pins, one should use only 8 x 470Ω arrays. This is so, because the pins on the opposite end (with respect to O1) of the Zig-Zag sockets, labeled as I1, are connected to ECL bias voltage, to supply terminating voltage for input port resistor arrays (8 x 50Ω) (see also sub-section 4.1.2.1).

Note that general rules for bussing of ECL output ports require that only the last port on the bus to have its pull-down resistor installed.

4.1.3. JUMPER SETTINGS

There are three jumper blocks on the XLM72 board that must be properly configured for a normal operation of the module. These are the 3-pin JP34 on the top of the board (front-panel facing left), the 6-pin JP35 close to the upper left corner of DSP (TMS320C6711), and the 3-pin JP36 right below JP35.

4.1.3.1. JP34 SETTINGS – FPGA DEFAULT BOOT SOURCE

JP34 has two positions identified by silk-screen labels “SPROM” and “JTAG”, respectively. For normal operation, the jumper should be placed in the “SPROM” position, i.e., connecting the two left-most pins of JP34. This allows FPGA to boot upon power-up from the default “boot” sector of the flash memory (socketed AT29C020 to the left of JP34). The “JTAG” position of JP34 is intended primarily for in-system-programming/reprogramming, in conjunction with the 6-pin JP33 JTAG header, of the four complex programmable logical devices (CPLDs) constituting the Interface. Since the user FPGA is in a common JTAG chain with the Interface CPLDs, it can be programmed via the JTAG port too, when JP34 is set to “JTAG”.

4.1.3.2. JP35 SETTINGS – DSP BOOT SOURCE AND DATA SIZE

JP35 is used to select the boot source and the size of the boot data for DSP. It has three pairs of pins, with one pair serving only as a storage bin. The significance of various jumper settings is described by the silk-screen label located right to JP35. It is replicated in Table 1 below

Table 1. Settings of DSP boot mode jumpers.

1-2	3-4	Boot Source/DataWord Size
OFF	OFF	ASRAM A/8-bits
ON	OFF	ASRAM A/32-bits
OFF	ON	HPI/16-bit (Default)

ON	**ON**	**ASRAM A/16-bits**

4.1.3.3. SETTINGS OF JP36 – DSP ENDIANNESS

JP36 selects endianness of DSP, as indicated by the silk-screen labels to its right. With a jumper in the lower position "LE", DSP operates in little-endian, while with a jumper in the upper position "BE", DSP operates in big-endian.

4.2. ADDRESSING AND DATA FORMATTING CONVENTIONS

Further below, the role of individual bits in various address and data words will be discussed, as well as the significance of various addresses and values of data words stored at these address locations. The rules adopted to identify individual bits and to interpret address and data words are presented in sub-sections 4.2.1. – 4.2.3. below.

4.2.1. BIT NUMBERING IN ADDRESS AND DATA WORDS

Whenever the role of individual bits, either in address or data words is discussed, it will be assumed further below that the least significant bit has index zero. Accordingly, the most significant bit in a 32-bit word is bit 31.

4.2.2. ADDRESS REPRESENTATION

XLM72 allows only 32-bit addressing, with the five most significant bits of this address representing the slot number occupied by XLM72 or, in other words, its geographic address. To address the total of five addressable internal devices XLM72 implements a 24-bit scheme, where the 3 most significant bits identify the device of interest and the remaining 21 bits identify the internal register or memory location of the device. Note that 21 bits are needed to make use of the full capacity of individual ASRAM banks. Therefore, further below, for the sake of simplicity, all addresses are expressed in the form of 5-digit hexadecimal numbers, with a tacit understanding that a full VMEBus address has always bits 24 through 26 set to zero and that bits 27 through 31 encode geographic address.

4.2.3. ENDIANNESS

Endian is a term commonly used to describe the way multi-byte data words are stored in memory. VMEBus is inherently big-endian, such that bytes of increasing hierarchy are stored at memory locations of decreasing addresses. Which means that the most significant byte of a multi-byte word is stored at lowest memory location and the least significant byte at highest memory location. Accordingly, data bytes of highest significance are transferred over VMEBus data lines of lower indices. And so, in 32 bit transfers, the most significant byte is transferred over data lines D0-D7, the second most

significant byte, over data lines D8-D15, the second least significant byte, over data line D16-D24, and the least significant byte, over data lines D25-D31. Similarly, in 16-bit transfers, the most significant byte is transferred over data lines D0-D7 and the least significant byte, over data lines D8-D15.

On the other hand, modern PC's are mostly little-endian, such that higher hierarchy bytes occupy higher memory locations. Also, modern VME crate controllers often offer the capability of a fast hardware conversion between the big- and little-endian formats. With this in mind, the present manual uses little-endian format, i.e., all data discussed further below are represented in little endian format.

4.3. SOFTWARE ACCESS OF INTERNAL DEVICES

4.3.1. ACCESSING INTERFACE REGISTERS

The use of the memory space of the Interface is fixed by the Interface firmware at the design or upgrade time. The VMEbus must write to proper locations of this space to accomplish the following tasks:

(i) Request control of any of the three, shared internal buses that are subject to bus arbitration, Bus A, Bus B, and Bus X (see also Section 3.2).
(ii) Issue interrupt signals to the DSP and FPGA and toggle reset lines for these devices.
(iii) Select the "warm" boot source for the FPGA, which is either one of the 4 banks of the Flash Memory, or ASRAM A (See also Section X).
(iv) Snatch the bus control from the FPGA and the DSP.
(v) Program the 6 most significant bits of an 8-bit ID word identifying XLM72 to the VMEBus IRQ controller, when the latter responds to the interrupt set by XLM72 (on the VMEbus IRQ3 line). The 2 least significant bits of this ID word identify to the IRQ controller the internal source of the request received from XLM72 – either FPGA (00 and 01) or DSP (10).
(vi) Reset the FPGA and DSP Interrupt Service Registers and Flags.

The VMEbus must read from proper locations of the address space to accomplish the following tasks:

(i) Check if the requested control of any of the buses has been, indeed, granted.
(ii) Check what the actual FPGA boot source is.
(iii) Check the actual ownership of the three arbitrated buses.
(iv) Read back the content of the XLM72 IRQ ID bits 2 – 7.
(v) Poll the Interrupt Service Registers of the FPGA and DSP for the presence of service requests.

Addressing of the Interface registers appears somewhat peculiar, due to the fact that the Interface is implemented in four Complex Programmable Logical Devices (CPLDs), each

of which has access only to a portion (non-contiguous) of the VMEBbus address bus. For example, the "Master" CPLD controlling the Interface logics has access only to the VMEbus data lines D0, D1, D16, and D17, as well as to the address lines A1, A2, A3, A16, and A17. Which is why, with few exceptions, accessing of the Interface is accomplished over the data lines D0, D1, D16, and D17 and address lines A2, A3, A16, and A17, accounting for the apparent peculiarity of the Interface addressing and data scheme.

Addresses of the Interface registers are shown in Table 2 below. Note that bit 23 is always set to "1", to select the Interface as the target device. Note also that to form a complete VMEbus address, the 24-bit addresses shown in Table 2, must be pre-pended by a 5-bit geographical address, followed by three "don't" care bits.

Table 2. Use of the Interface address space.

Address bits A0-A23	Registers accessed
800000h	Bus control request register (write) and bus grant register (read)
800004h	FPGA and DSP interrupt and reset register (write-only)
800008h	FPGA boot source register (write/read)
80000Ch	Inhibit flag for the bus control by FPGA and DSP
810000h	Bus A ownership register (read-only)
810004h	Bus B ownership register (read-only)
810008h	Bus X ownership register (read-only)
820000h	IRQ ID register (write/read) and XLM72 serial number (read-only)
820024h	FPGA and DSP ISR Registers (read-only + "clear")
820024h	FPGA and DSP ISR Registers (read-only + "clear")

The significance of data written to or read from the valid locations of the Interface address space is discussed in detail in sub-sections 4.3.1.1-4.3.1.9 below.

4.3.1.1. BUS CONTROL REQUEST REGISTER AT 800000h

The bus control register located at 800000h is a 3-bit register mapped onto bits 0, 1, and 16 of the 32-bit VMEBus word. When set by a "Write" operation, they indicate to the bus arbitrator the request by the VMEBus of the control of an arbitrated bus:

Request Bus A REQA = 00000001h
Request Bus B REQB = 00000002h
Request Bus X REQX = 00010000h

To release a bus, its respective request bit must be set to 0. Note that the Interface will always simultaneously set and/or release requests of all three buses, depending on which of the three bits, 0,1, and 16 are set and which are reset.

Example: a combined request of all three buses of XLM72 is achieved by writing (REQA OR REQB OR REQX) = 00010003 to the address 800000. To release all these three buses at the same time, one simply writes 0 to the same address.

4.3.1.2. FPGA AND DSP INTERRUPT AND RESET REGISTER AT 800004h

The FPGA and DSP interrupt and reset register at 800004h is a 4-bit write-only register mapping onto bits 0, 1, 16, and 17 of the 32-bit VMEBus word. Depending on what data are written into these four bits, the Interface will set or release the reset signal of the FPGA or DSP and/or strobe the interrupt of the FPGA or DSP. The action is always simultaneous on all four register bits involved.:

Set Reset for the FPGA	RESFPGA	= 00000001h
Set Reset for the DSP	RESDSP	= 00000002h
Strobe the interrupt for the FPGA	IRQFPGA	= 00010000h
Strobe the interrupt for the DSP	IRQDSP	= 00020000h

Reset signals are released by setting the associated bits to 0. Interrupts are only strobed for a duration of approx. 36 ns and do not require resetting.

Example:
To only set the Reset for the FPGA, one must write (RESFPGA OR RESDSP OR IRQFPGA OR IRQDSP) = 1 to the memory location 800004. To release this reset one writes 0 to this memory location. Note that the latter causes then the FPGA to boot from the selected boot source.

4.3.1.3. FPGA BOOT SOURCE SELECTOR REGISTER at 800008

The FPGA boot source selector register is a write/read 4-bit register mapping onto bits 0, 1, 16, and 17 of the 32-bit VMEBus word. At most one bit can be set at a time:

Select sector 0 of flash memory	BOOT0	= 00000000h
Select sector 1 of flash memory	BOOT1	= 00000001h
Select sector 2 of flash memory	BOOT2	= 00000002h
Select sector 3 of flash memory	BOOT3	= 00000003h
Select ASRAM A	BOOTA	= 00010000h

The BOOTA bit overrides the other BOOT bits that might be set.

Example:
To select ASRAM A as a boot source of the FPGA, one must write BOOTA=00010000h to the memory location 800008.

4.3.1.4. BUS CONTROL INHIBIT FLAG FOR FPGA AND DSP at 80000Ch

Writing "1" to 80000Ch inhibits bus control by the FPGA and DSP, and makes all buses A, B, and X unconditionally available to the VMEBus. To actually gain the control of the desired bus, VMEBus must still request control of the bus. Writing "0" to 80000Ch removes inhibit and allows the FPGA and DSP to compete for the bus control.

4.3.1.5. OWNERSHIP REGISTERS OF BUSES A, B, AND X AT 810000h, 810004h, AND 810008h

Bus ownership registers at 810000h, 810004h, and 810008h are 2-bit read-only registers storing data identifying the actual owner of Bus A, B, and X respectively. The returned values of 0, 1, 2, and 3 indicate free status, and control by the VMEBus, FPGA, and DSP, respectively.

4.3.1.6. XLM72 IRQ ID AND SERIAL NUMBER REGISTERS AT 820000h

The IRQ ID register at 820000h is a combined 6-bit write/read and 2-bit read-only register storing the programmable IRQ ID of XLM72 and the ID of the internal source of an IRQ3 request (FPGA or DSP), respectively. The internal source ID values of 1, and 2 represent the FPGA, while the value of 3 represent the DSP. The content of this register is returned by XLM72 over data line D0-D7 in the process of IRQ handling and, also, when reading from memory location 820000h. Additionally, in response to a read 820000h command, the Interface returns the XLM72 serial number, encoded in bits 16 – 25 of the 32-bit data word. Understandably, the serial number register has the read-only attribute.

To program the 6-bit IRQ ID, one must write the desired bits 2 – 7 to 820000h, with remaining bits being "don't care".

4.3.1.7. FPGA AND DSP ISR REGISTERS AT 820024h

While IRQ3 mechanism provided by XLM72 is quite adequate for requesting service by the VMEBus, in some data acquisition environments a polling-based mechanism may prove faster. To implement such an alternative service request mechanism, the Interface contains two 6-bit "mail box" register, one for the FPGA and the other one for the DSP, that can be only read and reset by the VMEBus, but can be written to by the FPGA and the DSP, respectively. The intended use of these registers is for the FPGA and/or the DSP to post in them their coded service requests. When a request is posted, an associated "Dirty" flag is set, signaling to the requestor the status of its request. In the process of the register polling by the VMEBus, a returned non-zero value is then used to trigger the appropriate action by the VMEBus, terminated by the clearing of the respective "requestor" register. Both registers share the same 820024h address and, hence, their

content is returned in one 32-bit data word. Bits 2 – 7 of this word are allocated to FPGA, while bits 18 – 23, to DSP.

To clear the FPGA ISR register and the associated "Dirty" flag, one must write 24h into location 820024h. To clear the DSP ISR register and its associated "Dirty" flag, one must write 240000h into location 820024h.

4.3.2. ACCESSING ASRAMs

One accesses either of the two ASRAMs by writing to or by reading from a desired memory location mapped onto the respective VMEBus address space of the ASRAM of interest. As discussed in Section 3.3, the VMEBus address space for ASRAM A extends from 0h to 1FFFFCh and that of ASRAM B, from 200000h to 3FFFFCh.

The use of the address spaces of the two banks of ASRAMs is straightforward and involves writing of desired data into, or reading data from, the desired memory address. For example, writing data to the address 000008h causes this data to be stored in the memory location 8h of ASRAM A. As a second example, reading from memory location 200010h, will retrieve the content of the memory location 10h of ASRAM B.

4.3.3. ACCESSING FPGA

The use of the address space of the FPGA remains at discretion of the user and is to be determined at the design time of the user FPGA code. One would expect here only a few low memory locations to be utilized with, perhaps, a suggestion to dedicate always the same location 0 for storing a read-only 32-bit ID of the particular user firmware.

4.3.4. ACCESSING DSP

The DSP can be accessed via its Host Port Interface (HPI).

4.4. PROGRAMMING OF THE USER FPGA

With Interface being an integral and tested part of XLM72, any further successful use of XLM72 hinges critically on the quality of the user code loaded into the FPGA of XLM72. To write such a code, the user must know the role of all pins of the FPGA used in the design of XLM72 and must know or establish safe timing patterns for interacting with other internal devices via write/read operations. The interaction mechanism of the FPGA with other Devices is described in detail below.

4.4.1. ECL PORTS

As described in Section 4.1, XLM72 features a total of 72 ECL ports organized in four 34-pin and one 8-pin header, named A-E, respectively.

Ports E1-E4 are connected (via the ECL<->TTL level translator) to secondary global clock pin SGCK3, and primary global clock pins PGCK3, PGCK1, and PGCK4 of the FPGA, respectively. They can be used to send dedicated clock signals to the FPGA, but also as standard I/O's.

For the actual numbers of the FPGA pins associated with individual ECL ports see Table 3 below and also Appendix A. This appendix lists, with abundant comments, the relevant section of a user constraint file (*.ucf) that can be used at the implementation time of the FPGA code. Note, that the user has no particular interest in knowing the pin associations, as the UCF file takes care of this task automatically, provided the design uses the proposed naming scheme.

Table 3. Association between ECL ports, physical FPGA pad numbers, and their respective UCF names

ECL Port	FPGA Pad #	UCF Name of FPGA Pad		ECL Port	FPGA Pad #	UCF Name of FPGA Pad
A1	107	ECLAPD<1>		C1	150	ECLCPD<1>
A2	101	ECLAPD<2>		C2	149	ECLCPD<2>
A3	100	ECLAPD<3>		C3	148	ECLCPD<3>
A4	99	ECLAPD<4>		C4	147	ECLCPD<4>
A5	98	ECLAPD<5>		C5	146	ECLCPD<5>
A6	97	ECLAPD<6>		C6	145	ECLCPD<6>
A7	96	ECLAPD<7>		C7	144	ECLCPD<7>
A8	95	ECLAPD<8>		C8	142	ECLCPD<8>
A9	94	ECLAPD<9>		C9	141	ECLCPD<9>
A10	93	ECLAPD<10>		C10	139	ECLCPD<10>
A11	92	ECLAPD<11>		C11	138	ECLCPD<11>
A12	90	ECLAPD<12>		C12	137	ECLCPD<12>
A13	89	ECLAPD<13>		C13	136	ECLCPD<13>
A14	88	ECLAPD<14>		C14	135	ECLCPD<14>
A15	87	ECLAPD<15>		C15	134	ECLCPD<15>
A16	85	ECLAPD<16>		C16	133	ECLCPD<16>
A17	127	ECL17PD<1>		C17	129	ECL17PD<3>
B1	126	ECLBPD<1>		D1	175	ECLDPD<1>
B2	125	ECLBPD<2>		D2	174	ECLDPD<2>
B3	124	ECLBPD<3>		D3	172	ECLDPD<3>
B4	123	ECLBPD<4>		D4	171	ECLDPD<4>
B5	122	ECLBPD<5>		D5	169	ECLDPD<5>
B6	120	ECLBPD<6>		D6	168	ECLDPD<6>
B7	119	ECLBPD<7>		D7	167	ECLDPD<7>
B8	117	ECLBPD<8>		D8	166	ECLDPD<8>
B9	116	ECLBPD<9>		D9	165	ECLDPD<9>

B10	115	ECLBPD<10>		D10	164	ECLDPD<10>
B11	114	ECLBPD<11>		D11	163	ECLDPD<11>
B12	113	ECLBPD<12>		D12	162	ECLDPD<12>
B13	112	ECLBPD<13>		D13	161	ECLDPD<13>
B14	111	ECLBPD<14>		D14	159	ECLDPD<14>
B15	110	ECLBPD<15>		D15	152	ECLDPD<15>
B16	109	ECLBPD<16>		D16	151	ECLDPD<16>
B17	128	ECL17PD<2>		D17	132	ECL17PD<4>
E1	102 (SGCK3)	ECLEPD<1>		E3	2 (PGCK1)	ECLEPD<3>
E2	108 (PGCK3)	ECLEPD<2>		E4	160 (PGCK4)	ECLEPD<4>

4.4.2. LED PORTS

XLM723 is equipped with three front-panel user-programmable LEDs, red, green, and yellow, controlled by FPGA configuration via expanding drivers. These drivers extend the duration of short pulses (of at least 2 clock cycle duration) to approx. 25 ms to provide for a robust flash of the associated LED, while not affecting the action of longer pulses. All LED ports are active high. A non-configured FPGA will provide high at all pins and, consequently, will cause all three LED to turn on – a state that can be taken as indicative of a failure of FPGA to boot. Conversely, successful configuring of the FPGA will be indicated by user LEDs displaying the pattern foreseen by the user code.

In the UCF file (See Appendix 5.1) LED pads are named LEDOPD<1>-LEDOPD<3>, respectively. Their association with physical pads of the FPGA is shown in Table 4.

Table 4. Front-panel LED control pads of the FPGA

LED	FPGA Pad #	UCF Name of FPGA Pad	LED	FPGA Pad #	UCF Name of FPGA Pad	LED	FPGA Pad #	UCF Name of FPGA Pad
Red	84	LEDOPD<1>	Green	82	LEDOPD<2>	Yellow	83	LEDOPD<3>

4.4.3. DSP INTERRUPT PORTS

There are two lines connecting two pins of the FPGA to two interrupt pins of the DSP. One of them (NMIDX) is used by the FPGA to drive the non-maskable interrupt NMI of the DSP (pad C13 of the DSP), while the other one (INT6DX) drives the EXT_INT6 pad D2 of the DSP. Both DSP interrupts are edge-driven by a low-to-high transition, with a requirement for the level to be low for at least two system clock cycles and then high for at least two cycles.

In the UCF file (see Appendix 5.1), the above two pins of the FPGA are labeled NMIDXOPD and INT6DXOPD, respectively. Their association with physical pins of the FPGA is shown in Table 5 below.

Table 5. DSP Interrupt pads of the FPGA

Interrupt	FPGA pin	Interrupt	FPGA pin
NMIDX	177	INT6DX	176

4.4.4. INTERFACE PORTS

With exception of the two DSP interrupt signals discussed above, the FPGA communicates with all internal devices, as well as with the VMEbus, via the Interface, i.e., has direct connections only with pins of the constituent CPLDs of the Interface. These are 19 local address lines, labeled in the UCF as LOCADPD<2>-LOCADPD<20>, 32 local data lines, labeled in the UCF as LOCDAPD<0>-LOCDAPD<31>, and 20 control lines supplying signals necessary for executing various operations. The address and data signals, when accompanied by proper combination of control signals, propagate via Interface to address and data pins of a desired ASRAM or Flash Memory, while the Interface provides the output enable (OE) chip enable (CE), and write (WR) signals necessary for accessing any device. It is important to appreciate that the local address and data lines are bi-directional and, therefore, bi-directional pads and tri-state buffers must be used by the FPGA to connect to these lines. It is then up to the user to provide for proper enable signals for these buffers to achieve the desired result and, more importantly, not to cause a prolonged bus contention.

4.4.4.1. BUS ARBITRATION PORTS

Since internal devices of XLM72 can be accessed by up to three different masters, VMEbus, FPGA, and DSP, the presence of a reliable arbitration scheme is absolutely necessary. The user FPGA code must comply with the simple rules of bus arbitration not to cause prolonged bus contention that can lead to a destruction of components of XLM72. The arbitration scheme of XLM72 is based on the first-come-first-serve-release-when-done principle. Therefore, every access of any internal device of XLM72 by the FPGA (in fact, by any master) must be preceded by a request (issued to the Interface) for exclusive control over the needed bus(es) followed by a verification that such an access has been, indeed, granted. Naturally, grant of control over a bus to one master automatically denies control over this bus to competing masters. At the conclusion of access, the FPGA must remove the request, which releases the bus for subsequent arbitration. There are three bus request lines associated with the three internal buses subject to arbitration. These three buses are (i) Bus A, interconnecting Interface and ASRAM A, (ii) Bus B, interconnecting Interface and Bus B, and (ii) Bus X, interconnecting Interface and the FPGA. The bus interconnecting Interface and the DSP is owned exclusively by the DSP and is, hence, not subject to arbitration. The bus request

signals are active low (so, a non-configured FPGA does not generate a false request). With each of the three bus request lines associated is a respective bus grant signal, active high. The bus grant signals are synchronized to the leading edge of the system clock. It is absolutely essential that the user configuration of the FPGA conditions enabling of local address lines of the FPGA by the presence of high on the Bus X grant line, as the Interface cannot here provide protection from a contention on bus X. Also, the user configuration must make sure that the local data buffers are not enabled when Interface is writing into the FPGA registers.

Since control of the FPGA over bus A or over bus B always involves its control also over bus X, a request for bus X for the FPGA is generated automatically by the Interface itself whenever the FPGA requests either bus A or bus B.

In UCF (see Appendix 5.1), the bus A, B, and X request pads are labeled NREQAOPD, NREQBOPD, and NREQXOPD, respectively, while the associated grant pins are labeled ACKAIPD, ACKBIPD, and ACKXIPD. The association between the above arbitration signals and the FPGA pad numbers is shown in Table 6 below.

Table 6. Bus arbitration pins of the FPGA

Bus Request	FPGA pin	Bus Grant	FPGA pin
A	46	A	75
B	45	B	70
X	62	X	57

4.4.4.2. LOCAL ADDRESS PORTS

Local address lines are used to transmit address bits between the FPGA and the Interface, under assumption that these address bits will propagate via the Interface to the target device. The association between the local address bits and the FPGA pins is shown in Table 7 below.

Table 7. Local Address pads of the FPGA

Address bit	FPGA Pad #	Address bit	FPGA Pad #	Address bit	FPGA Pad #	Address bit	FPGA Pad #
2	35	7	11	12	186	17	73
3	32	8	14	13	185	18	40
4	31	9	15	14	190	19	43
5	10	10	42	15	189	20	39
6	12	11	184	16	74		

In UCF (see Appendix 5.1), local address pins are labeled LOCADPD<2>-<20>.

4.4.4.3. LOCAL DATA PORTS

Local data lines are used to transmit data bits between the FPGA and the Interface, under assumption that these data bits will propagate via the Interface to the target device. The association between the local data lines and the FPGA pins is shown in Table 8 below.

Table 8. Local Data pads of the FPGA

Data line	FPGA Pad #	Data line	FPGA Pad #	Data line	FPGA Pad #	Data line	FPGA Pad #
0	58	8	200	16	61	24	9
1	64	9	19	17	65	25	24
2	41	10	30	18	28	26	27
3	36	11	194	19	37	27	196
4	29	12	179	20	23	28	178
5	21	13	193	21	22	29	181
6	198	14	191	22	197	30	180
7	20	15	187	23	199	31	188

In the UCF (see Appendix 5.1), local data pins are labeled LOCDAPD<0>-<31>.

4.4.4.4. BYTE ENABLE PORTS

While the data are addressed in XLM72 in 32-bit words, there is a mechanism in place that allows one to access any arbitrary combination of bytes, without affecting the remaining bytes. One simply asserts a proper combination of data byte enable signals (active low), NDBEO<0>-NDBEO<3>. Note that since the index 0 refers to low data lines, it refers in fact to high data byte numbers (Big-Endian). For the most common and fastest 32-bit data transfer, all four NDBEO<0>-NDBEO<3> signals may be set permanently to 0, as they will be ultimately qualified within the Interface additionally by an appropriate device select signal to be generated by the FPGA. In the UCF (see Appendix 5.1), the data byte enable pins are labeled NDBEOPD<0>-NDBEOPD<3>. The correspondence between these signals and FPGA pins is shown in Table 9.

Table 9. Data Byte Enable pins

Byte	FPGA pin	Byte	FPGA pin	Byte	FPGA pin	Byte	FPGA pin
0	72	1	44	2	63	3	81

4.4.4.5. WRITE OPERATION PORTS

The FPGA signals to the Interface a write operation by asserting one or both of its NWRA and NWRB lines (active low). NWRA low indicates that the operation upon

ASRAM A, the Interface, or the Flash Memory is a write operation. The target of the operation is in this case determined by the Interface based on the state of the NSEL lines discussed below. NWRA low indicates that the operation upon ASRAM B is a write operation. Note that the two NWR signals are not strobes. They are to be asserted at the time of the placement of the address and data on their respective local buses and de-asserted upon completion of operation. They should be kept constant for the duration of a block transfer. In the UCF, the NWRA and NWRB pins are labeled NWRAOPD and NWRBOPD, respectively. Their association with physical pins of the FPGA is shown in Table 10 below.

Table 10. Write enable (output) pins of the FPGA

NWR signal	FPGA pin	NWR signal	FPGA pin
NWRA	69	NWRB	59

4.4.4.6. DEVICE SELECTION PORTS

The FPGA signals to the Interface the intended target of its operation over three lines, NSELA, NSELB, and NSELV, named in UCF as NSELAOPD, NSELBOPD, and NSELVOPD. All these lines are active low and have dual functionality, depending on whether the operation is “write” or “read”.

In write operations, NSEL signals serve as write strobes and, hence, must be asserted so as to allow the address to propagate to the target device prior to their own reaching of the target (via the Interface). It was found that a safe way to write to ASRAMs is to assert the relevant NSEL signal for one system clock cycle, two system clock cycles after the FPGA has placed the address and data on their respective local buses. In a block transfer, this results then in a 3-cycle transfer and in an overall throughput of 107Mbyte/s (80MHz clock). The Interface makes here use of the data byte enable signals (NDBEO<0>-<3>) to strobe only the desired memory chips (storing individual bytes).

In read operations, NSEL signals serve as chip enable signals, which in conjunction with the (ASRAM) output enable signals cause the target device to output the addressed data on the data bus. In this case, NSEL is to be asserted at the time of the placement of address on the local address bus and can be kept constantly low for the entire duration of a block transfer. The ASRAM output enable signals are generated by the Interface when the latter detects the presence of an NSEL signal in the absence of the associated NWR signal (NWR high).

There are following valid combinations of the asserted NSEL signals:

(i) NSELA alone,
(ii) NSELB alone,
(iii) NSELV alone,
(iv) NSELA and NSELV,
(v) NSELA and NSELB, and

(vi) NSELA and NSELB and NSELV.

(i) and (ii) are used to achieve transfer of data between the FPGA and the individual ASRAMs. (iii) is used to access the FPGA interrupt service register and the associated flag in Interface. The combination (iv) is used (e.g., by Utility Configuration) to write data into the Flash Memory. The combination (v) allows simultaneous write by the FPGA into both ASRAMS or a transfer of data between the two ASRAMs, while the combination (vi) is intended for data transfer operations between ASRAM B and the Flash Memory (programming of the Flash Memory with a configuration file stored in ASRAM B or read-back of the content of the Flash Memory into ASRAM B). Note that an access of the Flash Memory involves asserting both NSELA and NSELV. For operations on the Flash Memory, the user is encouraged to use the default cold-boot Utility Configuration residing in bank 0 of the Flash Memory.

Note that ASRAM A shares NWRA line and the Output Enable line with the Flash Memory, which precludes transfer of data between ASRAM A and the Flash Memory. These two devices have, however, separate chip enable signals, which allows one to access any one of them individually.

The correspondence between the NSEL lines and the physical pins of the FPGA is shown in Table 11.

Table 11. Device selection pins of the FPGA

Signal	FPGA pin	Signal	FPGA pin	Signal	FPGA pin
NSELA	76	NSELB	68	NSELV	47

4.4.4.7. INTERRUPT PORTS

There are three “interrupt” lines interconnecting the FPGA and the Interface, one dedicated for transmitting interrupt signals sent from the VMEbus to the FPGA (NIRQXV), one for transmitting interrupt signals sent from the FPGA to the VMEbus (NIRQVX), and one for transmitting interrupt signals sent by the DSP to the FPGA (NIRQXD). All three are active low strobes but only the functionality of the NIRQVX is fully determined by the Interface. User has full freedom to utilize the 3-cycle NIRQXV and NIRQXD strobes any way he deems useful. For example, the general cold-boot Utility Configuration utilizes the NIRQXV signal to trigger operations by the FPGA, such as transfer of data between the two banks of ASRAMs, programming of the Flash Memory and the readback of its content into ASRAM B. In this case, prior to issuing the interrupt, user writes a proper code identifying the desired operation into a 3-bit IRQ register of the FPGA set up in the configuration for this express purpose. Upon the receipt of the NIRQXV, the FPGA checks the content of this register and then executes the desired operation.

The Interface is designed to recognize two types of VMEbus interrupt requests received from the FPGA over the same line NIRQVX. The distinction is here made based on the duration of the received NIRQVX strobe, with a single-cycle strobe resulting in "Level 0" interrupt and longer durations resulting in "Level 1" interrupt. The level ID is then encoded in bit 0 of the XLM72 IRQ ID, for a readout by the VMEbus IRQ handler. Both interrupt levels cause the Interface to generate VMEbus interrupt request on the VMEbus IRQ3 line.

The above two-level mechanism allows the FPGA to identify to the VMEbus the nature of the request in more detail with just one-cycle (12.5 ns) overhead. For example, Levels 0 and 1 may be used to signal readiness of data in ASRAM A and ASRAM B, respectively. Should there be more than 2 types of requests, one may use, for example, Level 0 to indicate type 1 and Level 2 to direct the VMEbus to inspect the content of a special IRQTYPE register set up in the FPGA configuration to hold the IRQ type code. Obviously, there is some additional (however small) overhead involved in the latter case, as the VMEbus must first obtain grant of Bus X, then read the IRQTYPE register and, finally, execute the desired operation.

In the UCF, the NIRQXV, NIRQVX, and NIRQXD pins are labeled NIRQXVIPD, NIRQVXOPD, and NIRQXDIPD, respectively.

The association between the NIRQ signals and the physical pins of the FPGA is shown in Table 12.

Table 12. Interrupt pins of the FPGA

IRQ	FPGA pin	IRQ	FPGA pin	IRQ	FPGA pin
NIRQXV	49	NIRQVX	67	NIRQXD	80

4.4.4.8. WRITE/READ CONTROL PORTS

The Interface controls writing and reading of data into/from the FPGA registers by means of two signals NSELXV and NWRX. The mechanism is here very much the same as the one used by the FPGA to execute read and write operations.

In a write operation NWRX is low for the duration of the operation (e.g., for the duration of block transfer), while the NSELXV (active low) plays a role of the write strobe. User configuration may then utilize the leading edge of the NSELXV to register the local data LOCDA0-31 into registers identified by the local address LOCAD2-20.

In read operations, NWRX is high and NSELX is low for the duration of the operation. User configuration must then respond by placing the content of the addressed register on the local data bus and enabling the associated tri-state drivers. In this case, it is the Interface that is in control of the timing.

In UCF, the NWRX and NSELX pads are named NWRXIPD and NSELXIPD, respectively. Their association with physical pins of the FPGA is shown in Table 13 below.

Table 13. Write/read to/from FPGA control pads

Control line	FPGA Pad #	Control line	FPGA Pad #
NWRX	34	NSELX	48

4.4.5. CONFIGURING FPGA

XLM72 offers three ways of configuring FPGA:

(i) via the JTAG port (see Section 4.1.3.1),
(ii) from Flash Memory, and
(iii) from ASRAM A.

Programming via the JTAG port is intended primarily for debugging purposes and requires dedicated equipment (software and download cable) and, therefore, is not discussed in this manual.

4.4.5.1. CONFIGURATION DATA FILE

When configuring FPGA from ASRAM A or programming Flash Memory, a properly formatted configuration data file is needed. FPGA programming software allows one to generate binary configuration data as an array of 8-bit words. These 8-bit data words have to be properly mapped onto 32-bit words to be loaded into ASRAM A or ASRAM B (in the case of Flash Memory programming – see Section 4.5). The mapping is shown in Table 14 below.

Table 14. Mapping of 8-bit "raw" configuration data bytes onto 32-bit words

Bit # in "Raw" 8-bit Word	0	1	2	3	4	5	6	7
Bit # in 32-bit "XLM" Word	2	3	4	10	18	19	20	26

Note that a "raw" byte FFh converts to a 32-bit 41C041Ch "XLM" configuration word.

Furthermore, the header part of the "raw" data file has to be skipped and only the configuration data proper converted and loaded into target ASRAM. To perform this stripping, one has to rely on the fact that the first data word to be converted is FFh (decimal 255), which means that a conversion program must skip all bytes read from a "raw" configuration file until it encounters FFh (255). Note also that second valid byte is always 0.

4.4.5.2. CONFIGURING FPGA FROM FLASH MEMORY

Upon power-up, FPGA attempts to boot (configure itself) from the default, "boot" sector of Flash Memory. Whether such a boot is successful or unsuccessful, one may force FPGA to boot from a desired different sector of Flash Memory. To this end, one must:

(i) select the desired boot sector by writing its ID (0 – 3, for the four sectors available) into location 800008h (see Section 4.3.1.3),
(ii) set reset for FPGA by writing 1 into location 800004h (Section 4.3.1.2) , and
(iii) release reset for FPGA by writing 0 into location 800004h (Section 4.3.1.2).

Upon release of reset, FPGA will attempt to boot from the selected sector of Flash Memory.

4.4.5.3. CONFIGURING FPGA FROM ASRAM A

To reconfigure FPGA from ASRAM A, one must:

(i) select ASRAM A as the FPGA boot source by writing 10000h into location 800008h (Section 4.3.1.3),
(ii) acquire control of Bus A by writing 1 into 800000h (Section 4.3.1.1)
(iii) load the desired configuration file into ASRAM A
(iv) release control of Bus A by writing 0 into 800000h (Section 4.3.1.1)
(v) set reset for FPGA by writing 1 into location 800004h (Section 4.3.1.2) , and
(vi) release reset for FPGA by writing 0 into location 800004h (Section 4.3.1.2).

Upon release of reset, FPGA will attempt to boot from ASRAM A.

The above procedure has to be somewhat altered when FPGA is not yet configured. In such a case, in order to be able to acquire Bus A, one must first inhibit the bus access by FPGA and DSP by writing 1 into location 80000Ch (see Section 4.3.1.4) and then set reset for FPGA as in (v) above. Subsequently, one would have to perform (i), (ii), (iii), (vi), and cancel inhibition of bus access by FPGA (by writing 0 into 80000Ch).

4.5. OPERATIONS ON THE FLASH MEMORY

4.5.1. FPGA UTILITY CONFIGURATION

XLM72 is released with a general FPGA utility program loaded into the default boot sector 0 of the flash memory. This program guarantees that there is no bus contention on the ECL ports of the FPGA upon power-up, as it has all respective pads defined as bi-directional with outputs being disabled. Among other things, this Utility Configuration allows one to program the flash memory, set and reset its software protection, and read-back the FPGA configuration files stored in the flash memory.

The various actions of the utility program are triggered by the interrupt signal by the VMEbus, which is generated by writing of 10000h into read-only Interface location 800004h (see also Section 4.3.1.2). The utility program identifies the nature of the request by inspecting the content of its data register at VMEBus address 40000Ch. Thus, to induce the general utility program to perform any of its operations, the user must:

(i) acquire control of Bus X by writing 10000h into location 800000h (Interface),
(ii) write the code of the desired operation into location 40000Ch (FPGA),
(iii) release control of Bus X by writing 0 into location 800000 (Interface)
(iv) write 10000h into location 800004h (Interface).

Valid codes for operations relevant to the programming of Flash Memory are shown in Table 15 below.

Table 15. Operation codes relevant for Flash Memory operations.

Code	Action by the FPGA
0	Program Flash Memory with the content of ASRAM B
5	Read data from Flash Memory into ASRAM B
6	Transfer content of ASRAM A into ASRAM B
8	Reset software protection of Flash Memory
9	Set software protection of Flash Memory

4.5.1.1. SOFTWARE PROTECTION OF FLASH MEMORY

The data stored in Flash Memory may be protected from an inadvertent corruption by setting of software data protection. The protection is achieved by writing a sequence of proper bytes into proper memory locations of Flash memory. To induce Utility Configuration to execute such a sequence, one must:

(i) acquire control of Bus X (by writing 10000h into 800000h),
(ii) write 9 to location 40000Ch, and
(iii) issue the FPGA interrupt by writing 10000h into location 800004h.

Reset of the software protection is achieved in a similar manner, except in (ii) one would write 8, rather than 9, into location 40000Ch.

4.5.1.2. PROGRAMMING OF FLASH MEMORY

FPGA has exclusive control of Flash Memory and, thus, in-system programming of this memory is possible only via FPGA. Utility Configuration can be induced to program any sector of Flash Memory with the content of ASRAM B. To program Flash Memory using Utility Configuration, one must:

(i) Reset software protection of Flash memory (see Section 4.5.1.1)

(ii) acquire control of Buses B and X by writing 10002h into 800000h,
(iii) select sector to be programmed by writing its ID (1-3) into location 800008h,
(iv) load configuration data into ASRAM B,
(v) write 0 into 40000Ch,
(vi) release control of Buses B and X by writing 0 into 800000h,
(vii) issue the FPGA interrupt by writing 10000h into 800004h.
(viii) set software protection (recommended).

5. APPENDICES

5.1. USER CONSTRAINTS FILE, UCF

The usage of FPGA pads is defined in the user constraints file UCF. Part of such a file, used by Utility Configuration is reproduced below:

```
NET "ECLEPD<1>" LOC="P102";     # SGCK3
NET "ECLEPD<2>" LOC="P108";     # PGCK3
NET "ECLEPD<3>" LOC="P2";       # PGCK1
NET "ECLEPD<4>" LOC="P160";     # PGCK4
#
NET "ECL17PD<1>" LOC="P127";
NET "ECL17PD<2>" LOC="P128";
NET "ECL17PD<3>" LOC="P129";
NET "ECL17PD<4>" LOC="P132";
#
NET "ECLAPD<1>" LOC="P107";
NET "ECLAPD<2>" LOC="P101";
NET "ECLAPD<3>" LOC="P100";
NET "ECLAPD<4>" LOC="P99";
#
NET "ECLAPD<5>" LOC="P98";
NET "ECLAPD<6>" LOC="P97";
NET "ECLAPD<7>" LOC="P96";
NET "ECLAPD<8>" LOC="P95";
#
NET "ECLAPD<9>" LOC="P94";
NET "ECLAPD<10>" LOC="P93";
NET "ECLAPD<11>" LOC="P92";
NET "ECLAPD<12>" LOC="P90";
#
NET "ECLAPD<13>" LOC="P89";
NET "ECLAPD<14>" LOC="P88";
NET "ECLAPD<15>" LOC="P87";
NET "ECLAPD<16>" LOC="P85";
#
NET "ECLBPD<1>" LOC="P126";
NET "ECLBPD<2>" LOC="P125";
NET "ECLBPD<3>" LOC="P124";
NET "ECLBPD<4>" LOC="P123";
#
NET "ECLBPD<5>" LOC="P122";
NET "ECLBPD<6>" LOC="P120";
NET "ECLBPD<7>" LOC="P119";
NET "ECLBPD<8>" LOC="P117";
#
NET "ECLBPD<9>" LOC="P116";
NET "ECLBPD<10>" LOC="P115";
NET "ECLBPD<11>" LOC="P114";
NET "ECLBPD<12>" LOC="P113";
#
```

```
NET "ECLBPD<13>" LOC="P112";
NET "ECLBPD<14>" LOC="P111";
NET "ECLBPD<15>" LOC="P110";
NET "ECLBPD<16>" LOC="P109";
#
NET "ECLCPD<1>" LOC="P150";
NET "ECLCPD<2>" LOC="P149";
NET "ECLCPD<3>" LOC="P148";
NET "ECLCPD<4>" LOC="P147";
#
NET "ECLCPD<5>" LOC="P146";
NET "ECLCPD<6>" LOC="P145";
NET "ECLCPD<7>" LOC="P144";
NET "ECLCPD<8>" LOC="P142";
#
NET "ECLCPD<9>" LOC="P141";
NET "ECLCPD<10>" LOC="P139";
NET "ECLCPD<11>" LOC="P138";
NET "ECLCPD<12>" LOC="P137";
#
NET "ECLCPD<13>" LOC="P136";
NET "ECLCPD<14>" LOC="P135";
NET "ECLCPD<15>" LOC="P134";
NET "ECLCPD<16>" LOC="P133";
#
NET "ECLDPD<1>" LOC="P175";
NET "ECLDPD<2>" LOC="P174";
NET "ECLDPD<3>" LOC="P172";
NET "ECLDPD<4>" LOC="P171";
#
NET "ECLDPD<5>" LOC="P169";
NET "ECLDPD<6>" LOC="P168";
NET "ECLDPD<7>" LOC="P167";
NET "ECLDPD<8>" LOC="P166";
#
NET "ECLDPD<9>" LOC="P165";
NET "ECLDPD<10>" LOC="P164";
NET "ECLDPD<11>" LOC="P163";
NET "ECLDPD<12>" LOC="P162";
#
NET "ECLDPD<13>" LOC="P161";
NET "ECLDPD<14>" LOC="P159";
NET "ECLDPD<15>" LOC="P152";
NET "ECLDPD<16>" LOC="P151";
#
# Bidirectional data bus connecting FPGA to the VME interface/bus router
NET "LOCDAPD<0>" LOC="P58";
NET "LOCDAPD<1>" LOC="P64";
NET "LOCDAPD<2>" LOC="P41";
NET "LOCDAPD<3>" LOC="P36";
NET "LOCDAPD<4>" LOC="P29";
NET "LOCDAPD<5>" LOC="P21";
NET "LOCDAPD<6>" LOC="P198";
NET "LOCDAPD<7>" LOC="P20";
NET "LOCDAPD<8>" LOC="P200";
NET "LOCDAPD<9>" LOC="P19";
NET "LOCDAPD<10>" LOC="P30";
```

```
NET "LOCDAPD<11>" LOC="P194";
NET "LOCDAPD<12>" LOC="P179";
NET "LOCDAPD<13>" LOC="P193";
NET "LOCDAPD<14>" LOC="P191";
NET "LOCDAPD<15>" LOC="P187";
NET "LOCDAPD<16>" LOC="P61";
NET "LOCDAPD<17>" LOC="P65";
NET "LOCDAPD<18>" LOC="P28";
NET "LOCDAPD<19>" LOC="P37";
NET "LOCDAPD<20>" LOC="P23";
NET "LOCDAPD<21>" LOC="P22";
NET "LOCDAPD<22>" LOC="P197";
NET "LOCDAPD<23>" LOC="P199";
NET "LOCDAPD<24>" LOC="P9";
NET "LOCDAPD<25>" LOC="P24";
NET "LOCDAPD<26>" LOC="P27";
NET "LOCDAPD<27>" LOC="P196";
NET "LOCDAPD<28>" LOC="P178";
NET "LOCDAPD<29>" LOC="P181";
NET "LOCDAPD<30>" LOC="P180";
NET "LOCDAPD<31>" LOC="P188";
#
#Bidirectional address bus connecting FPGA to the VME interface/bus
router
NET "LOCADPD<2>" LOC="P35";
NET "LOCADPD<3>" LOC="P32";
NET "LOCADPD<4>" LOC="P31";
NET "LOCADPD<5>" LOC="P10";
NET "LOCADPD<6>" LOC="P12";
NET "LOCADPD<7>" LOC="P11";
NET "LOCADPD<8>" LOC="P14";
NET "LOCADPD<9>" LOC="P15";
NET "LOCADPD<10>" LOC="P42";
NET "LOCADPD<11>" LOC="P184";
NET "LOCADPD<12>" LOC="P186";
NET "LOCADPD<13>" LOC="P185";
NET "LOCADPD<14>" LOC="P190";
NET "LOCADPD<15>" LOC="P189";
NET "LOCADPD<16>" LOC="P74";
NET "LOCADPD<17>" LOC="P73";
NET "LOCADPD<18>" LOC="P40";
NET "LOCADPD<19>" LOC="P43";
NET "LOCADPD<20>" LOC="P39";
#
# Data byte select pins, to be used in conjunction with device select
# signals ASRAMA and ASRAMB
# Connect to the interface. Active low.
NET "NDBEOPD<0>" LOC="P72";     # most significant byte in 32-bit Big-
Endian-formatted data
NET "NDBEOPD<1>" LOC="P44";
NET "NDBEOPD<2>" LOC="P63";
NET "NDBEOPD<3>" LOC="P81";
#
# Select internal device of XLM72 (more than one may be selected at
# time): ASRAMA, ASRAMB,
# Interface Registers, or Flash Memory. Active low.
NET "NSELAOPD" LOC="P76";
```

```
# NSELA selects ASRAM A when alone or when in conjunction with NSELB;
# selects Flash Memory
# when in conjunction with NSELV
NET "NSELBOPD" LOC="P68";
# NSELB selects ASRAM B when alone or when in conjunction with NSELA or
# NSELV
NET "NSELVXOPD" LOC="P47";
# NSELV selects Interface when alone or when in conjunction with NSELB;
#  selects
# Flash Memory when in conjunction with NSELA.
# Reasonable combinations are NSELA, NSELB, NSELV, (NSELA and NSELB)
# (used for simultaneous writes
# to both ASRAM banks and transfers of data between these banks), and
# (NSELA and NSELB and NSELV),
# (used to program Flash Memory from ASRAM B and to read back the Flash
# Memory data into ASRAM B).
# The combination (NSELB and NSELV) does not seem to have a reasonable
# application.
#
# Define Read/Write operation for ASRAMA/Interface/Flash Memory and
# ASRAMB. Active low
NET "NWRAOPD" LOC="P69";
# When NWRA is low, operations on ASRAM A, Interface, and Flash Memory
# are write operations and
# the data byte select signals (NDBE0-3) must be 1-cycle write strobes.
# Else NDBE are 3-cycle
# chip-enable (ASRAM output enable signals are generated by the
# Interface).
NET "NWRBOPD" LOC="P59";
# When NWRB is low, operations on ASRAM B are write operations and the
# NDBE signals are
# 1-cycle write strobes. Else NDBE are 3-cycle chip-enable(ASRAM output
# enable signals are
# generated by the Interface).
#
# Timing of the write operations: Place address and data on address and
# data buses X
# and pull the relevant NWRA and/or NWRB low. After one clock cycle,
# pull the relevant NSEL
# low for one clock cycle (write strobe). For the write access to Flash
# Memory, NSELV is to be asserted
# together with NWRA. Address and data change (i.e. clock address
# counter) at the trailing edge of
# NSEL strobe.
# For block transfers (most common use), NWR can be kept continuously
# low. Also NSELV is continuously
# low in block transfers to/from the Flash Memory. Note that one
# transfer takes 3 clock cycles, resulting
# in a transfer rates of up to 107 MBytes/s.
#
#Timing for read operations: Place address on address buse X and assert
# the relevant NSEL.
# Keep NWR continuously high. The data is ready at the data bus after 2
# cycles. In block transfers,
# keep control signals continuously asserted, while clocking  (for one
# cycle) the address every
# third cycle.
```

```
#
#Request bus mastership of ASRAMA, ASRAMB, or Interface only. Active
low.
NET "NREQAOPD" LOC="P46";  # requests bus A and bus X
NET "NREQBOPD" LOC="P45";  # requests bus B and bus X
NET "NREQXOPD" LOC="P62";  # requests bus X alone for the access to
# Interface.
# Note that to acces ASRAM A or ASRAM B, the FPGA must control bus X
also, # as it supplies both
# data and address to ASRAM banks via bus X.
#
# Bus mastership granted for operations on ASRAMA, ASRAMB, or Interface
# only. Clocked
# by LE of the system clock.
NET "ACKAIPD" LOC="P75";
NET "ACKBIPD" LOC="P70";
NET "ACKXIPD" LOC="P57";
# The FPGA must check if bus(es) are granted, before proceeding with
# ASRAM and Interafce
# access operations
#
# Interrupts from VME and DSP; functionality is user-defined. Active
# low, 3-cycle strobes.
# Clocked by LE of the system clock.
# Recommended way of use - latch the leading edge.
NET "NIRQXVIPD" LOC="P49";
NET "NIRQXDIPD" LOC="P80";
#
#Select FPGA from Interface. Active low, clocked by LE of the system
# clock.
NET "NSELXVIPD" LOC="P48"; # for an explanation look after the
# description of NWRI.
#
#Signal used by the Interface to define Write/Read operation to/from the
# FPGA.
# Clocked by LE of the system clock.
NET "NWRXIPD" LOC="P34";
# In write-to-FPGA operations by the Interface, NWRI is low and NSELX is
# a 2-cycle write strobe.
# In read-from-FPGA operations by the Interface, NWRI is high and NSELX
# is a 4-cycle
# data output enable signal.
#
# Interrupt VME (on VMEbus IRQ3). Active low strobe of two different
# durations. To be clocked by LE of the system clock.
NET "NIRQVXOPD" LOC="P67";
# A 2-cycle strobe generates in the Interface an XLM72 IRQ ID with bit 0
# = 0, while a 3-cycle strobe
# generates an ID with bit 0 = 1, a mechanism to inform the IRQ service
# routine of the nature of the
# request (e.g., "data ready in ASRAM A" or "data ready in ASRAM B").
#
# Control of three front-panel LEDs. Active high. Minimum duration 2
# clock cycles to produce
# a robust blink. Continuous on, keeps LED on.
NET "LEDOPD<1>" LOC="P84";
NET "LEDOPD<3>" LOC="P82";
```

```
NET "LEDOPD<2>" LOC="P83";
#
# Unmasked and masked interrupt of DSP. Low-to-high leading-edge
# strobes; require at least a 2-cyclelow followed by at least a 2-cycle
# high.
NET "NMIDXOPD" LOC="P177";  # nonmaskable interrupt (NMI), connected
# directly to pad C13 of the DSP.
NET "INT6DXOPD" LOC="P176";  # masked interrupt EXT_INT6, connected
# directly to pad D2 of the DSP.
#
```

5.2. USING UTILITY CONFIGURATION OF FPGA

As discussed in Section 4.5.1, XLM72 is released with a Utility Configuration of FPGA loaded into sector 0 of Flash Memory, which is loaded into FPGA upon power-up. This configuration can be used to perform operations on Flash Memory, but it offers also other functions useful for diagnostic purposes.

As discussed in Section 4.5.1, the various actions of the utility program are triggered by by writing of 10000h into read-only Interface location 800004h (see also Section 4.3.1.2) and that the utility program identifies the nature of the request by inspecting the content of its data register at VMEBus address 40000Ch. Thus, to induce the general utility program to perform any of its operations, the user must:

(v) acquire control of Bus X by writing 10000h into location 800000h (Interface),
(vi) write the code of the desired operation into location 40000Ch (FPGA),
(vii) release control of Bus X by writing 0 into location 800000 (Interface)
(viii) generate FPGA interrupt by writing 10000h into ISR register.

In Table 16 below are listed all IDs of all operations that are performed by the utility program.

Table 16. Valid operation codes of Utility Configuration.

Code	Action by the FPGA
0	Program Flash Memory with the content of ASRAM B
3	Transfer content of ASRAM B into ASRAM A
4	Fill ASRAM A with data pattern A
5	Read data from Flash Memory into ASRAM B
6	Transfer content of ASRAM A into ASRAM B
7	Fill ASRAM B with data pattern A
8	Reset software protection of Flash Memory
9	Set software protection of Flash Memory
Ah	Write to ISR register of the Interface
24h	Fill ASRAM A with data pattern B
44h	Fill ASRAM A with data pattern C
64h	Fill ASRAM A with data pattern D

Table 16. Continuation

Code	Action by the FPGA
64h	Fill ASRAM A with data pattern D
84h	Fill ASRAM A with data pattern E
24h	Fill ASRAM B with data pattern B
44h	Fill ASRAM B with data pattern C
64h	Fill ASRAM B with data pattern D
84h	Fill ASRAM B with data pattern E

5.2.1. WRITING TO ISR REGISTER OF INTERFACE

Utility Configuration allows also one to test the functioning of the interrupt service request system in which the FPGA communicates its request by writing a code into the ISR register within Interface. VMEBus detects this request by periodically polling this register, executes the desired operation, and clears the register and its "dirty" flag (see Section 4.3.1.7).

To write into the FPGA ISR register, one must issue FPGA interrupt with operation ID=Ah (decimal 10). Upon interrupt, FPGA waits until the "Dirty" flag of the Interface ISR register is cleared (indicating that previous request is completed) and then writes bits 2 – 7 of utility register at 400004h into the Interface ISR register (bits 2 – 7 of this register are allocated to the FPGA). Writing of these bits sets also the "Dirty" flag of this ISR register.

5.2.2. TEST DATA PATTERNS

Utility Configuration allows one to write various test data patterns into ASRAMs using operation IDs as indicated in Table 15 above.

Pattern A consists of bits 2 – 17 of the address, placed in both, lower and upper 16 bits of data words.

Pattern B is equal to the content of the Utility Configuration register at 400004h. The desired pattern must be entered into this register prior to executing the FPGA interrupt.

Pattern C is similar to B except alternating with 00000000h for consecutive addresses.

Pattern D is similar pattern A except upper 16 bits being 0000h.

Pattern E is similar to pattern A except lower 16 bits being 0000h.