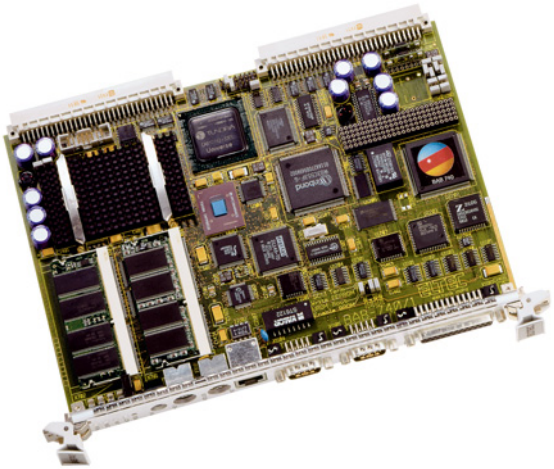
ELTEC systems

BAB 740

Basic Automation Board with PowerPC 740



MANUAL

Revision 2C

ELTEC systems

Revision

Revision	Changes	Date / Name
1A	First Edition, Valid for Hardware revision 1A	03.01.2000 AR
2A	Valid for Hardware revision 3A	24.04.2001 G.M.
2B	Valid for Hardware revision 3A Valid for Software revision W-O9B7-106C - I/O-Address-Map changed -	26.09.2001 rae
2C	Disclaimer new	08.11.06 hh

DISCLAIMER

Copyright

Federal communications commission statement

- This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:
- This device may not cause harmful interference, and
- This device must accept any interference received including interference that may cause undesired operation.
- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with

manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try correct the interference by one or more of the following measures:

- ↪ Reorient or relocate the receiving antenna.
- ↪ Increase the separation between the equipment and receiver.
- ↪ Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- ↪ Consult the dealer or an experienced radio/TV technician for help.
- ↪ The us of shielded cables for connection of the monitor to the graphics card is required to assure compliance with FCC regulations. Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Canadian department of communications statement

- ↪ This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.
- ↪ This class B digital apparatus complies with Canadian ICES-003

SAFETY INFORMATION

Electrical safety

- ↪ To prevent electrical shock hazard, disconnect the power cable from the electrical outlet before reloading the system.

- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add device.
- Before connecting or removing signals cables from motherboard, ensure that all power cables are unplugged.
- Make sure that your power supply is set to the correct voltage in your area. If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If the power supply is broken, do not try to fix it by yourself. Contact a qualified service technician or your retailer.

Operation safety

- Before installing the motherboard and adding devices on it, carefully read the manuals that came with the package.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you detect any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not place the product in any area where it may become wet.
- Place the product on a stable surface.
- If you encounter technical problems with the product, contact a qualified service technician or your retailer.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

IMPROTANT INFORMATION

This product is not an end user product. It was developed and manufactured for further processing by trained personnel.

RECYCLING

Please recycle packaging environmentally friendly:
Packaging materials are recyclable. Please do not dispose packaging into domestic waste but recycle it.

Please recycle old or redundant devices environmentally friendly:
Old devices contain valuable recyclable materials that should be reutilized. Therefore please dispose old devices at collection points which are suitable.

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1 Specification

1.1 Main Features

- VMEbus board with two PMC daughter card slots (opt.). Two VMEbus slots used.
- PowerPC CPU 740 with 266 MHz.
- RAM: 8..256 MB DRAM (2 * 64-bit SO DIMMs) EDO/SDRAM 50ns.
- Cache: 512kB on-board.
- PCI host bridge: Motorola MPC106.
- PCI-ISA-Bridge: W83C553.
- PCI-to-VME bridge Universe II for fast, global VMEbus transfers, decoupled from board-internal PCI transfers.
- Flash Eprom: 2 MB onboard, Flash programmable, byte access implemented in hardware.
- Network interface: Ethernet using DEC21143 (10/100 Mbps) with PCI-DMA, 10BaseT connector at front panel.
- Serial synchronous (optional): 2 * RS422 / 3 Mb/s synchronous using Zilog 85230 ESCC.
- Serial asynchronous: 2 * RS232 with PC97307.
- Real-time clock: MK48T59
- SCSI (optional): Symbios 860
- OS-9 operating system with FasTrak cross development system. - VxWorks operating system with Tornado cross development system.
- I/O-compatible with BAB-40/60 where applicable.

1.2 Specification Details

1.2.1 CPU Kernel

The CPU kernel consists of the PowerPC-740 CPU with clock rates of 266 MHz and host bus clocks of 66 MHz. The CPU contains two parallel 32-bit integer execution units with an additional floating point unit for 8 SPECint95 and 6.2 SPECfp95 at 200 MHz. It has an external second-level cache (2-1-1- 1 clocks) and main memory attached directly to the CPU's host bus. Memory is controlled by the host bridge MPC106 which contains the bridge between host bus and on-board PCI itself as well as the memory interface for EDO or SDRAM modules in SO DIMM format (144-pin SO DIMM modules; 64-bit data bus). Memory size can be anywhere between 8 and 128 MB, depending on the DIMM modules used. Two sockets can be equipped with SO DIMM modules but the board is also running with only one module.

1.2.2 Flash Memory

Up to 2 MB of user flash memory are supplied for storing user-generated programs. Thus, diskless systems can be built.

1.2.3 PCI Devices

The board-internal PCI bus is used for all I/O devices as well as the PCI-to-VME bridge. The PCI bus is of the master/slave type, capable of DMA transfers as source and target.

Two single-size PMC slots allow for flexible interfacing, e.g. using a VGA display adapter PMC module and additionally a frame grabber interface. Due to the bus-master DMA capabilities of the PMC implementation of the PCI standard, frame grabber can be implemented efficiently without frame buffers.

An Ethernet controller for either 10 Mbps or 100 Mbps Ethernet with PCI DMA capabilities is provided on-board. Front panel interface is 10/100BaseT.

The last interface on the local PCI bus is the ISA bridge (Winbond W83C553), interfacing to the internal ISA bus with additional on-board components. Additionally, there are the standard PC components real-time clock, keyboard controller, dual serial I/O and parallel controller.

1.2.4 VMEbus Interface

The VMEbus interface uses the Universe II bridge controller, connecting the internal PCI bus and the external VMEbus. It supports 8-, 16-, and 32-bit data transfers in master and slave mode. Additionally, bus controller (arbiter) functionality is available.

Use of the BAB 740 without VMEbus is possible; only power must be supplied through VME connectors.

1.2.5 Mechanical

The board format is double Eurocard (6HU) using two VMEbus slots. The VMEbus connectors are mounted at the position of the second VMEbus slot (the slot on the right) of the two slots the board is using. Two slots for single-size PMC modules are available.

1.2.6 I/O

8-bit SCSI is routed over the VME P2 connector. Additionally, the serial I/O channels 2 .... 4 and the parallel I/O are also routed via P2.

On the front panel the Ethernet 10BaseT connector is located as well as the separate front panel for PMC I/O signals. The keyboard connector and two serial RS232 channel are also routed to the front panel (9-pin D connector).

1.2.7 Software

The standard operating system is OS-9/VxWorks for the PowerPC. The development environment is FasTrak for Windows, so that the user can write and debug programs on the Windows 95 or Windows NT platform. Debug and program download can be done via Ethernet or through the PCI bus.

BIOS functionality is supplied in the form of the boot program, used to start the operating system OS-9/VxWorks. It also contains power-on self test routines and PCI device address setup.

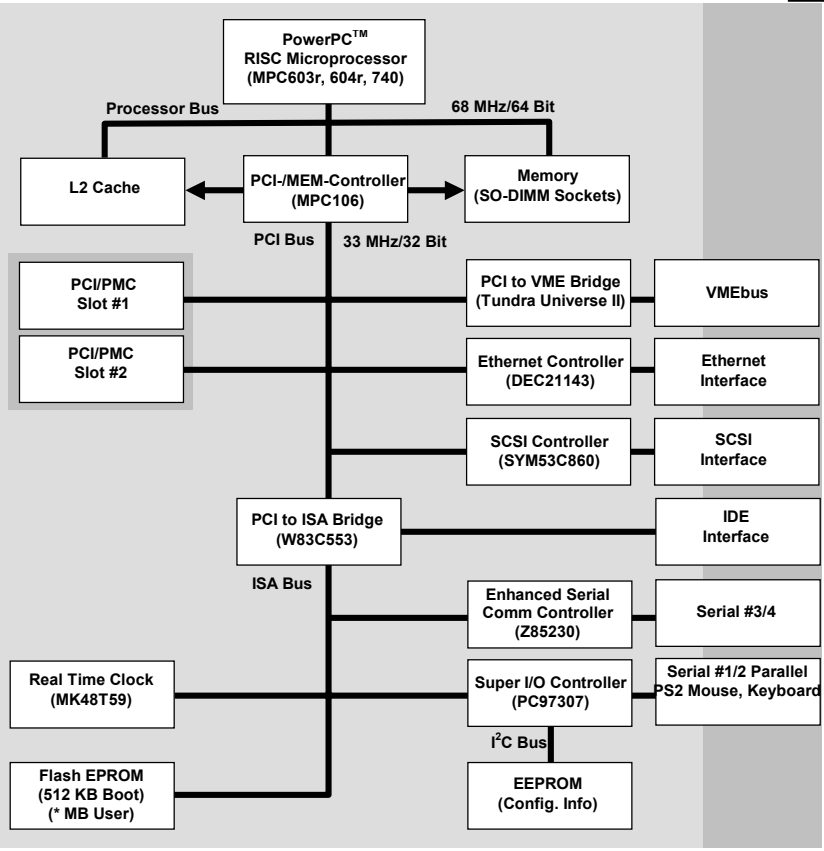
1.2.8 Compatibility

The BAB 740 has been designed to be software-compatible to the PowerPC reference platform (“Yellowknife”) as much as possible.

1.2.9 Related Documents

PowerPC 750 Programmer's Reference: This is the CPU manufacturer's description of the PowerPC itself and the assembly language command set.

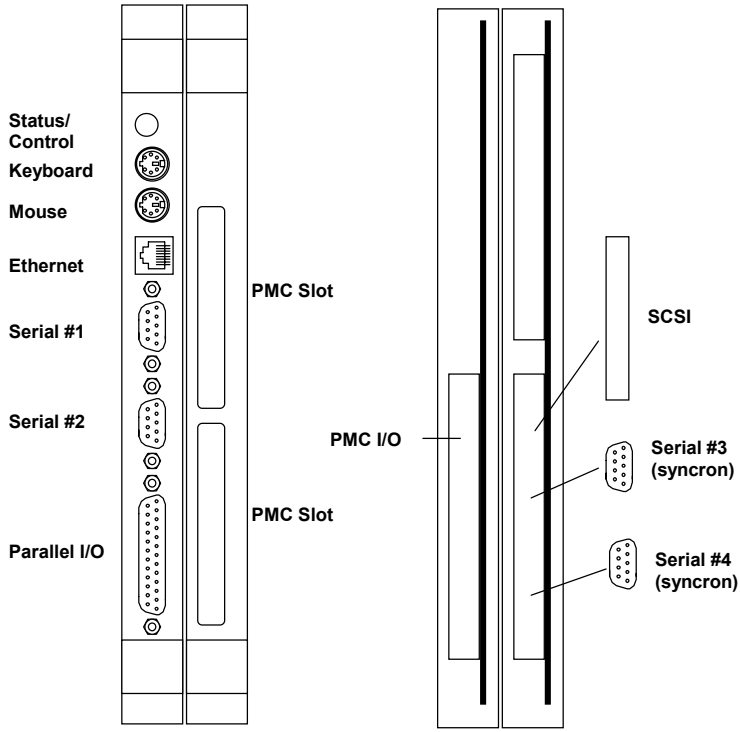
Figure 1: Block Diagram



2 Installation

2.1 BAB 740 I/O

Figure 2: Connection Diagram



2.1.1 VMEbus Installation

WARNING: *Due to the power dissipation of the MPC740 CPU it is not recommended to operate the BAB 740 without forced air cooling.*

The BAB 740 needs two VMEbus slots, when used with the PMCE carrier board. Since the two boards (BAB 740 and PMCE) have an internal connection, be sure to install resp. remove the two-board package carefully and simultaneously!

2.1.2 What‘s needed for Installation

The BAB 740 must be installed into a 32-bit VMEbus rack. A terminal (or a PC with a terminal emulator program), set to 9600 baud, 8 bit, no parity, is needed to check boot messages and to change boot settings. A SCSI hard disk must be attached via an ADAP-200/220 if the operating system is booted from disk; if it is booted from Ethernet, this network connection is needed.

2.1.3 SODIMM Installation

All 144-pin SO-DIMMs up to 64 MByte and some 128 Mbyte SO-DIMMs that fit into X701 and X702 can be used with the BAB 740. The firmware reads the type and size of the SO-DIMM from the SPD (Serial Presence Detect) EEPROM installed on the memory module. However there are some restrictions and recommendations:

- SDRAMs should be 100 MHz or faster.
- FPMODE or EDO RAMs should be 60 ns or faster.
- X701 must be populated with a memory module.
- If two memory modules are installed they should be of the same type but may have different size. Otherwise the firmware uses only the module installed in X701.
- Due to performance reasons the use of SDRAM is strongly recommended (50% advantage).

After reset the firmware tests the memory modules. If the test fails or the firmware reports the wrong size - the module may not be suitable for the BAB 740.

2.1.4 Activity LEDs

There are four activity LEDs on the front panel of the BAB 740. The LEDs have a pulse stretcher to make short pulses visible.

Table 1: Activity LEDs

LED	Color	Description
RUN	Green	CPU data bus in usage
DISK	Yellow	access to IDE or SCSI bus
LNK	Green/Yellow	green = 100 Mbit link pulses present yellow = 10 Mbit link pulses present
ACT	Yellow	network activity

3 Connector Assignments

Please check the connector assignments before making any connections!

3.1 On-board Connectors

3.1.1 Keyboard and Mouse Connector

Table 2: KEYB (6-pin miniature circular connector)

Pin	Signal
1	KBDATA
2	nc
3	GND
4	+5V
5	KBCLK
6	nc

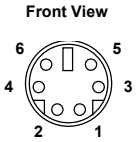
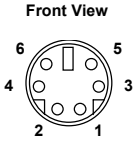


Table 3: MOUSE (6-pin miniature circular connector)

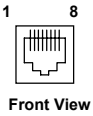
Pin	Signal
1	MDATA
2	nc
3	GND
4	+5V
5	MCLK
6	nc



3.1.2 Ethernet Connector

Table 4: ETHERNET (8-pin telephone jack connector)

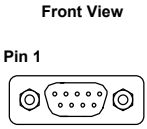
Pin	Signal
1	TXD+
2	TXD-
3	RXD+
4	nc
5	nc
6	RXD-
7	nc
8	nc



3.1.3 Serial Ports 1 and 2 Connectors

Table 5: COM1, COM2 (9-pin min-D connector)

Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

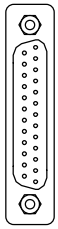


3.1.4 Parallel I/O Connector

Table 6: PRN (25-pin min-D connector)

Pin	Signal
1	/STROBE
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	D8
10	/ACK
11	BUSY
12	PE (Paper End)
13	SLCT
14	/AUTO FEED
15	/ERROR
16	/INIT
17	/SLCT IN
18-25	GND

Front View



Pin 1

3.1.5 VMEbus Connector P1

Table 7: VMEbus Connector P1 (X2001)

Pin	Row A	Row B	Row C
1	D00	/BBSY	D08
2	D01	/BCLR	D09
3	D02	/ACFAIL	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	SYSCLK	/BG3IN	/SYSFAIL
11	GND	/BG3OUT	/BERR
12	/DS1	/BR0	/SYSRESET
13	/DS0	/BR1	/LWORD
14	/WRITE	/BR2	AM5
15	GND	/BR3	A23
16	/DTACK	AM0	A22
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	(SERCLK)	A17
22	/IACKOUT	(SERDAT)	A16
23	AM4	GND	A15
24	A07	/IRQ7	A14
25	A06	/IRQ6	A13
26	A05	/IRQ5	A12
27	A04	/IRQ4	A11
28	A03	/IRQ3	A10
29	A02	/IRQ2	A09
30	A01	/IRQ1	A08
31	-12 V	+5STDBY	+12 V
32	+ 5 V	+ 5 V	+ 5 V

Signals in parentheses are not connected

Table 8: Pin Assignment of Connector P2 (X2002)

Pin	Signal Row A	Signal Row B	Signal Row C
1	SPKROUT	+ 5 V	SCSIDB1
2	SCSIDB0	GND	SCSIDB3
3	SCSIDB2	Reserved	SCSIDB5
4	SCSIDB4	A24	SCSIDB7
5	SCSIDB6	A25	IDEDB(8)
6	SCSIDBP0	A26	IDEDB(9)
7	SCSIDP	A27	IDEDB(10)
8	IDEDA(0)	A28	IDEDB(11)
9	IDEDA(1)	A29	IDEDB(12)
10	IDEDA(2)	A30	DENSEL
11	IDEDB(13)	A31	/DSKCHG
12	/IDEIOCS16	GND	/MTR0
13	/INDEX	+ 5 V	/DR0
14	/DR1	D16	/DIR
15	/STEP	D17	/SCSIATN
16	/WGATE	D18	IDEDB(14)
17	IDEDB(15)	D19	/SCSIBSY
18	/SCSIACK	D20	/SCSIRST
19	/SCSIMSG	D21	/SCSISEL
20	/SCSIC/D	D22	/SCSIREQ
21	/SCSII/O	D23	C4GND4
22	C4GND1	GND	C4DTR
23	C4CTS	D24	C4TXD
24	C4RTS	D25	C4RXD
25	C4DCD	D26	C3GND4
26	C3GND1	D27	C3DTR
27	C3CTS	D28	C3TXD
28	C3RTS	D29	C3RXD
29	C3DCD	D30	+ 5 V
30	/WP	D31	/WDATA
31	/HDSEL	GND	/TRK0
32	DRATE0	+ 5 V	/RDATA

Lines on rows A and C are TTL-level, except Cx signals which have RS 232C level (SILC-200 used). Pin assignment changes for RS 422 configuration. Row B is reserved for 32-bit VMEbus extension

3.2 ADAP-200 Connectors

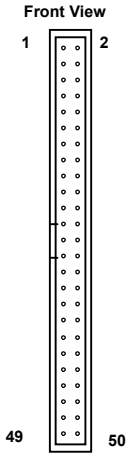
3.2.1 8-bit SCSI

Single-ended 8-bit SCSI signals are fed into row A and C of the VMEbus P2 connector (X2002). An ADAP-200 is plugged onto the rear side of the backplane to interface to standard 8-bit SCSI connectors (a 50-pin flat cable connector)

If the BAB 740 is located at either end of the SCSI bus. J1601 must be installed for signal termination, otherwise J1601 must be removed.

Table 9: SCSI Connector 8-bit X103 (on ADAP-200)

Pin	Description	Pin	Description
2	DB0	28	GND
4	DB1	30	GND
6	DB2	32	ATN
8	DB3	34	GND
10	DB4	36	BSY
12	DB5	38	ACK
14	DB6	40	RST
16	DB7	42	MSG
18	DB8	44	SEL
20	GND	46	CIO
22	GND	48	REQ
24	GND	50	I/O
26	TERM-PWR		



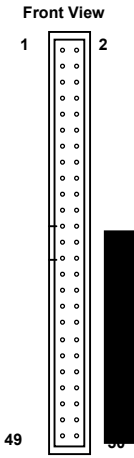
All odd pins of the 50-pin SCSI connector except pin 25 are connected to ground. Pin 25 is left open.

Pin 26 is connected to +5 V via a Shottky diode to supply power to an external SCSI terminator.

3.2.2 Additional I/O

Table 10: 50-Pin I/O Connector X102 (on ADAP-200)

Pin	Dir	Description	Remark	
1..23	I/O	reserved		
24	-	Serial Channel 4	GND2	(may be changed if a non standard level-converter board SILC is installed)
25	-	Serial Channel 4	GND1	
26	-	Serial Channel 4	nc	
27	I	Serial Channel 4	CTS	
28	O	Serial Channel 4	TXD	
29	O	Serial Channel 4	RTS	
30	I	Serial Channel 4	RXD	
31	-	not connected		
32	-	not connected		
33	-	Serial Channel 3	GND2	(may be changed if a non standard level-converter board SILC is installed)
34	-	Serial Channel 3	GND1	
35	-	Serial Channel 3	nc	
36	I	Serial Channel 3	CTS	
37	O	Serial Channel 3	TXD	
38	O	Serial Channel 3	RTS	
39	I	Serial Channel 3	RXD	
40	-	not connected		
41	-	not connected		
42..50	-	reserved		



3.3 CONV-300 Connectors

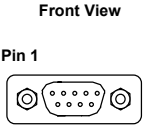


Table 11: COM3, COM4 (9-pin min-D connector)

Pin	RS232 async.Signal (default)	RS232 sync.Signal	RS422 async. Signal	RS422 sync. Signal
1	DCD	DCD	CTS-	RCLK-
2	RXD	RXD	RXD+	RXD+
3	TXD	TXD	TXD+	TXD+
4	DTR	DTR	RTS-	TCLK-
5	GND	GND	TXD-	TXD-
6	nc	nc	nc	nc
7	RTS	TCLK	RTS+	TCLK+
8	CTS	RCLK	CTS+	RCLK+
9	nc	nc	RXD-	RXD-

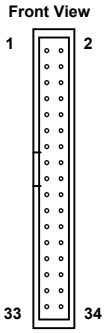
3.4 ADAP-740 Connectors

3.4.1 Floppy Disk

The floppy cable is connected between floppy drive and the adapter connector. The power supply cable for the floppy drive must be connected directly to the power supply.

Table 12: Pinout Floppy Connector X101 (on ADAP-740)

Pin	Name	Name	Pin
1	Gnd	DRVDEN0	2
3	Gnd	nc	4
5	Gnd	DRVDEN1	6
7	Gnd	/INDEX	8
9	Gnd	/MTR0	10
11	Gnd	/DS1	12
13	Gnd	/DS0	14
15	Gnd	MTR1	16
17	Gnd	/DIR	18
19	Gnd	/STEP	20
21	Gnd	/WDATA	22
23	Gnd	/WGATE	24
25	Gnd	/TRK0	26
27	Gnd	/WRTPRT	28
29	Gnd	/RDATA	30
31	Gnd	/HDSEL	32
33	Gnd	/DSKCHG	34



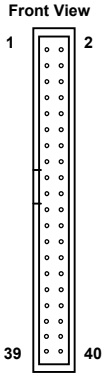
3.4.2 EIDE

Like the floppy disk drive an EIDE drive is connected with its flat cable to the adapter. The power supply cable of the EIDE device must be directly connected to the power supply.

Up to two EIDE drives (harddisk, CD-ROM) can be connected. Cable length should not exceed 40 cm to avoid instable operation. EIDE is only available on board versions with EIDE option.

Table 13: Pinout EIDE Connector X105 (on ADAP-740)

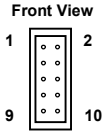
Pin	Name	Name	Pin
1	/RST	GND	2
3	D7	D8	4
5	D6	D9	6
7	D5	D10	8
9	D4	D11	10
11	D3	D12	12
13	D2	D13	14
15	D1	D14	16
17	D0	D15	18
19	GND	nc	20
21	REQ	GND	22
23	/IOW	GND	24
25	/IOR	GND	26
27	IORDY	nc	28
29	/ACK	GND	30
31	IRQ14	nc	32
33	A1	nc	34
35	A0	A2	36
37	/CS1	/CS3	38
39	/ACT	GND	40



3.4.3 COM3 and COM4

Table 14: COM3 and COM4 Connectors X103 and X104 (on ADAP-740)

Pin	RS232 async. Signal (default)	RS232 sync. Signal	RS422 async. Signal	RS422 sync. Signal
1	DCD	DCD	CTS-	RCLK-
2	nc	nc	nc	nc
3	RXD	RXD	RXD+	RXD+
4	RTS	TCLK	RTS+	TCLK+
5	TXD	TXD	TXD+	TXD+
6	CTS	RCLK	CTS+	RCLK+
7	DTR	DTR	RTS-	TCLK-
8	nc (+5V)	nc (+5V)	RXD-	RXD-
9	GND	GND	TXD-	TXD-
10	nc	nc	nc	nc

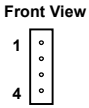


The pinout of X103 and X104 on ADAP-740 is such that a crimped cable with a 10 pin edge connector and a 9 pin Min-D male connector results in the same pinout as Table 11.

3.4.4 Speaker

Table 15: Speaker Connector X106 (on ADAP-740)

Pin	
1	+5V
2	nc
3	nc
4	Speaker



3.5 PMCE-740 Connectors

Via the PMC Extension Board (PMCE-740) the BAB 740 can be expanded by two PMC Modules.

3.5.1 PMCE-740 VMEbus Connector P1

Only GND, +5V and +12V are routed from the VMEbus Connector P1 to the Power Connector X403. No VMEbus Signals are used.

Table 16: PMCE-740 VMEbus Connector P1 (X402)

Pin	Row A	Row C
1...8	nc	nc
9	GND	GND
10	nc	nc
11	GND	nc
12..14	nc	nc
15	GND	nc
16	nc	nc
17	GND	nc
18..30	nc	nc
31	nc	+ 12 V (Cam)
32	+ 5 V (Cam)	+ 5 V (Cam)

3.5.2 PMCE-740 PCI Mezzanine Card Connectors

Table 17: PMCE-740 PCI Mezzanine Card Connectors Jn11, Jn12, Jn21, Jn22 (X101, X102, X201, X202).

X101, X201			
Pin	Signal Name	Signal Name	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	GND	PCI-RSVD*	12
13	CLK	GND	14
15	GND	GNT'	16
17	REQ#	+5V	18
19	V(I/O)	AD(31)	20
21	AD(28)	AD(27)	22
23	AD(25)	GND	24
25	GND	C/BE(3)#	26
27	AD(22)	AD(21)	28
29	AD(19)	+5V	30
31	V(I/O)	AD(17)	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	Signal	+5V	38
39	GND	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	GND	44
45	V(I/O)	AD(15)	46
47	AD(12)	AD(11)	48
49	AD(9)	+5V	50
51	GND	C/BE(0)#	52
53	AD(6)	AD(5)	54
55	AD(4)	GND	56
57	V(I/O)	AD(3)	58
59	AD(2)	AD(1)	60
61	AD(0)	+5V	62
63	GND	REQ64#	64

X102, X202			
Pin	Signal Name	Signal Name	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI-RSVD	8
9	PCI-RSVD*	PCI-RSVD	10
11	BUSMODE2#	+3,3V	12
13	RST#	BUSMODE3#	14
15	+3,3V	BUSMODE4#	16
17	PCI-RSVD	GND	18
19	AD(30)	AD(29)	20
21	GND	AD(26)	22
23	AD(24)	+3,3V	24
25	IDSEL	AD(23)	26
27	+3,3V	AD(20)	28
29	AD(18)	GND	30
31	AD(16)	C/BE(2)#	32
33	GND	PMC-RSVD	34
35	TRDY#	+3,3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3,3V	SERR#	42
43	C/BE(1)#	GND	44
45	AD(14)	AD(13)	46
47	GND	AD(10)	48
49	AD(8)	3,3V	50
51	AD(7)	PMC-RSVD	52
53	+3,3V	PMC-RSVD	54
55	PMC-RSVD	GND	56
57	PMC-RSVD	PMC-RSVD	58
59	GND	PMC-RSVD	60
61	ACK64#	+3,3V	62
63	GND	PMC-RSVD	64

3.5.3 PMCE-740 PCI Mezzanine Card I/O Routing

Table 18 shows the routing of the PMC I/O Connectors to the VMEbus P2 Connector

Table 18: PCI Mezzanine Card Back Plane I/O Routing

(X203) Host Jn24	(X103) Host Jn14	(X401) VMEbus P2	(X103) Host Jn14	(X401) VMEbus P2
33	1	1C	33	17C
34	2	1A	34	17A
35	3	2C	35	18C
36	4	2A	36	18A
37	5	3C	37	19C
38	6	3A	38	19A
39	7	4C	39	20C
40	8	4A	40	20A
41	9	5C	41	21C
42	10	5A	42	21A
43	11	6C	43	22C
44	12	6A	44	22A
45	13	7C	45	23C
46	14	7A	46	23A
47	15	8C	47	24C
48	16	8A	48	24A
49	17	9C	49	25C
50	18	9A	50	25A
51	19	10C	51	26C
52	20	10A	52	26A
53	21	11C	53	27C
54	22	11A	54	27A
55	23	12C	55	28C
56	24	12A	56	28A
57	25	13C	57	29C
58	26	13A	58	29A
59	27	14C	59	30C
60	28	14A	60	30A
61	29	15C	61	31C
62	30	15A	62	31A
63	31	16C	63	32C
64	32	16A	64	32A

3.5.4 PMCE-740 Power Connector

Table 19: PMCE-740 Power Connector (X403)

Pin	Description
1	+5V out
2	GND
3	GND
4	+12V out

4 Board Parameters

4.1 Host Bus

66MHz

4.2 VMEbus

VMEbus interface according to specification ANSI/IEEE STD 1014-1987 (Rev. D1.4)

VMEbus Master/Slave Capabilities:

Single cycle:
A16/A24/A32/A64:D08(EO)/D16/D32/UAT
A40:D08(EO)/D16/MD32

RMW (Master only):
A16/A24/A32:D08(EO)/D16/D32
A40:D08(EO)/D16/MD32

BLT: A24/A32/A64:D08(EO)/D16/D32
A40:D08(EO)/D16/MD32

MBLT: A24/A32/A64:D64

ADO: A16/A24/A32/A40/A64/CR/CSR

ADOH: A16/A24/A32/A40/A64

System Controller Options:

Arbiter: BTO(16/32/64), forever

IACK daisy-chain driver

SYSCLK driver

Arbiter Options:

PRI, RRS, SGL

BBSY filter

Requester Options:

Any one of BR(0-3)

RWD, ROR, ROC

Bus ownership timer 16 µs... 1024 µs, forever

Interrupt Handler Options:

IH(1-7)

D08(O), D16, D32

Interrupter Options:

I(1-7)

D08(O), D16, D32

Auto Configuration:

FSD, ASI

Address Range:

Four PCI target/VME master windows: base and size programmable, 64 KB to 4 GB window size, any of specified address capabilities or user-defined.

Four VME slave/PCI initiator windows: base and size programmable, 64 KB to 4 GB window size, any of specified address capabilities or user-defined.

4.3 PCI Local Bus

CPU to PCI Transfer Options:

Write post buffer

Max. 120 MB/s (peak)

PCI to Memory Transfer Options:

Max. 120 MB/s (peak)

Clock Speed:

33.3 MHz

IRQs:

Four PCI interrupts rerouted to selectable ISA interrupts

4.4 Network

10BaseT/100BaseTx (twisted-pair)

Transfer Speed:

max. 10/100 Mbit/s

4.5 SCSI

Ultra SCSI (8 bit)

Transfer Speed:

asynchronous transfer 7 MB/s

synchronous transfer 20 MB/s (ultra SCSI)

4.6 Serial I/O

2 Channels (PC97307):

Full duplex, asynchronous

50 b/s - 115,2 KB/s

RS232 level

2 Channels (Z85230 ESCC):

Full duplex

50 b/s - 230,4 KB/s asynchronous

up to 3 MB/s synchronous

RS232 or RS422 level

4.7 Keyboard:

MF2/AT mode

PS/2 mode

4.8 Mouse

PS/2 mode

Serial mouse at channel 1 or channel 2

4.9 Parallel I/O

Centronics bidirectional, unbuffered TTL

Transfer Rate: max. 2 MB/s

4.10 MTBF Values

Includes one 64 Mbyte SODIMM:

18900 h (computed after MIL HDBK-217E)

253270 h (realistic value from industry stand experience)

4.11 ESD Values

2 kV (Human body method)

4.12 Environmental Conditions

Storage Temperature: -40° C - +70° C (non condensing)

Operating Temperature: 0° C - +50° C (1 m/s forced air cooling)

4.13 Maximum Operating Humidity:

85% relative

4.14 Power Requirements

Total Power Requirements (without PCI extensions)

3,8 A max. 3.0 A typ. +5 VDC +/-5%

100 mA max. 30 mA typ. +12 VDC +/-10%

100 mA max. 10 mA typ. -12 VDC +/-10%

Battery

Type M4T28-BR12SH1

Approx. 8 years life time

5 Jumpers

5.1 On-board Jumpers

Figure 3: Parts Side Jumpers

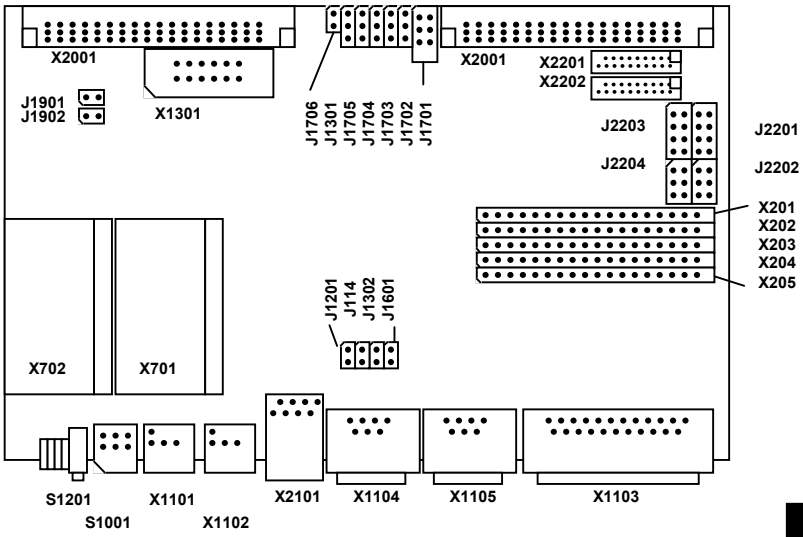
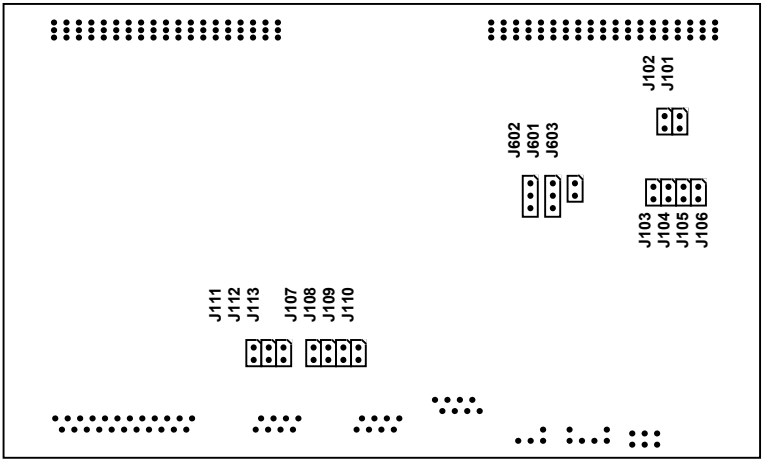


Figure 4: Solder Side Jumpers



5.1.1 User-settable Jumpers

Table 20: Boot ROM Select (J114)

J114	Description
open	Boot from Boot-ROM
Short	Boot from User-ROM (default)

Table 21: SCSI Termination (J1601)

J1601	Operation
Open	disable termination
short	enable termination (default)

Table 22: SMI Interrupt Routing (J1701)

J1701	Function
-	no SMI interrupt
1-3	route Universe INT0 to SMI
2-4	route Universe INT0 to SMI
4-6	route Universe INT0 to SMI
3-5	route Universe INT0 to SMI
7-8	route SMITICK to SMI (default)

Table 23: Universe PCI Interrupt Routing (J1702...J1705)

J1702	Function
-	no Universe INT0, INT1 on PCI
1-2	route Universe INT0 to PCI IRQ A
2-3	route Universe INT1 to PCI IRQ A

J1703	Function
-	no Universe INT2, INT3 on PCI
1-2	route Universe INT2 to PCI IRQ B
2-3	route Universe INT3 to PCI IRQ B

J1704	Function
-	no Universe INT4, INT5 on PCI
1-2	route Universe INT4 to PCI IRQ C
2-3	route Universe INT5 to PCI IRQ C

J1705	Function
-	no Universe INT6, INT7 on PCI
1-2	route Universe INT6 to PCI IRQ D
2-3	route Universe INT7 to PCI IRQ D (default)

Table 24: VMEBus SYSRESET (J1706, J1902)

J1706	J1902	Function
-	-	no VMEbus SYSRESET
short	-	VMEbus SYSRESET is input
-	short	VMEbus SYSRESET is output (default)
Short	Short	not allowed

Table 25: VMEBus SYSFAIL (J1901)

J1901	Function
Open	no VMEbus SYSFAIL
short	VMEbus SYSFAIL output enable (default)

Table 26: COM3 Configuration (J2201, J2202, X2201)

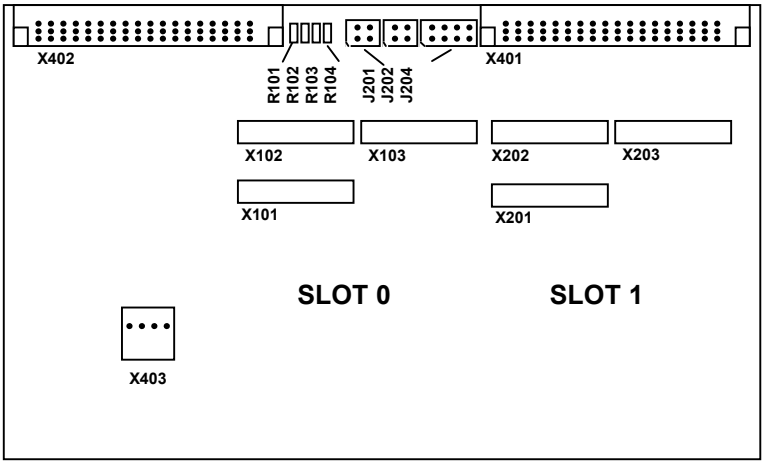
J2201	J2202	X2201	Configuration
1-2 3-5 6-8	1-2 5-6	SILC-200	RS232 async. (default)
2-4 6-8	1-2 4-6	SILC-200	RS232 sync.
6-8	1-2	SILC-300	RS422 async.
4-6	2-4	SILC-300	RS422 sync.

Table 27: COM4 Configuration (J2203, J2204, X2202)

J2203	J2204	X2202	Configuration
1-2 3-5 6-8	1-2 5-6	SILC-200	RS232 async. (default)
2-4 6-8	1-2 4-6	SILC-200	RS232 sync.
6-8	1-2	SILC-300	RS422 async.
4-6	2-4	SILC-300	RS422 sync.

5.2 PMCE-740 Jumpers

Figure 5: PMCE-740 Jumpers



5.2.1 PMCE-740 User-settable Jumpers

Table 28: PMC Slot 1 PCIREQ and PCIGNT Routing

J201	J202	Description
1-2	1-2	Use PCIREQ, PCIGNT of PMC Slot 0
3-4	3-4	Use PCIREQ, PCIGNT of BAB 740 Onboard SCSI Controller

Warning: PCIREQ and PCIGNT of PMC Slot 0 or SCSI Controller can only be used, if the corresponding device is not equipped!

Table 29: PMC Slot 1 Interrupt Routing

J204	Description
1-2	Route PMC IRQ A to PCI IRQ A
3-4	Route PMC IRQ A to PCI IRQ B
5-6	Route PMC IRQ A to PCI IRQ C
7-8	Route PMC IRQ A to PCI IRQ D

6 Booting

6.1 Printout of Boot Screen

This chapter shows how the terminal screen looks like on a BAB 740 after power-on.

```
 *** ELTEC Elektronik, Mainz ***

BAB-PPC Monitor Version 1.2/2

Init MPU/MSR/FPU/Segment registers.
Init SuperIO (polled output on COM1).
Activating 1st level cache ..................... OK
Setting MPC106 register ........................ OK
Reading SPD of bank0/1 ......................... OK
        RAM-Type: SDRAM
Reading SPD of bank2/3 ..................... FAILED
Activating  64 MByte.

PowerPC 74x/75x Ver.0008 Rev.3202 at 292 / 83 MHz

PCI devices on local bus ...
No. VendorId  DeviceId  Device Class     Sub-Class
_____________________________________________________
00  1057      0002      Bridge device           00
0B  10AD      0565      Bridge device           01
0D  1000      000F      Mass storage controller 00
0E  1011      0019      Network controller      00
13  1011      0024      Bridge device           04

Press any key to skip memory test :    65536 KByte
```

After this screen output, the standard VxWorks monitor will be started. To modify boot parameter follow the instructions provided by VxWorks development documentation.

6.2 Booting OS-9

6.2.1 Entering Boot Parameters

The BAB 740 is prepared for booting over Ethernet using BOOTP protocol.

6.2.2 Printout of Boot Screen

```
*** ELTEC Elektronik GmbH, Mainz ***
BAB 740 Monitor Version 1.0/1
Init MPU/MSR/FPU/Segment registers.
Init SuperIO (polled output on COM1).
Activating 1st level cache ---------------------------     OK
Setting MPC106 register ------------------------------     OK
Reading SPD of bank0/1 -------------------------------     OK
        RAM-Type: SDRAM
Reading SPD of bank2/3 -------------------------------     FAILED
Activating 32 MByte.

OS-9000 Bootstrap for the PowerPC(tm)
Ethernet 10 Mbit selected
BOOTING PROCEDURES AVAILABLE -------------------------      <INPUT>
Boot loaded system in-place (copy User-ROM to RAM) --      <bo>
Boot over Ethernet (DEC 21143) -----------------------      <eb>
Scan SCSI devices ------------------------------------      <ioi>
PCI View Utility -------------------------------------      <pciv>
Enter ROM Debugger -----------------------------------      <break>
Restart the System -----------------------------------      <q>
Select a boot method from the above menu:
(Booting procedure up to boot menu may take about half a minute in
this release.)
```

6.2.3 Ethernet Boot Printout

If a BOOTP server is available in the local network and the BAB 740 is known by this server, the BAB 740 will boot over Ethernet after entering ‚eb' at the boot menu prompt.

Note: The BOOTP server must send the response directly to the BAB 740. Broadcasts will not be analyzed by the BAB 740 in this case.

```
Select a boot method from the above menu: eb
Bootp: sending bootp request for Address 00:00:5b:00:37:39
Bootp: Got Response from server: c2.00.00.38
My IP Address will be: c2.00.00.b8
My Bootfile is: /tftpboot/B740/os9boot
Bootp: My bootfile size is: 00000cc3 (512-byte) blocks
My subnet mask is: ff.ff.ff.00 <<no timeoffset tag>>
Tftp: Sending tftp Request...
.............................................................
                          o
                          o
                          o
.............................................................
.............................................................
Tftp: received file with 0019840c bytes
Bootfile received from server c2.00.00.38
Now searching for an OS-9000 Kernel...
A valid OS-9000 bootfile was found.
[1]$
```

After the boot file is transferred, OS-9 is booting.

7 Appendix

7.1 Description of On-board Devices

This chapter describes how the on-board devices are accessed by operating system drivers. When an operating system, such as OS-9 and VxWorks, is used, there should be no need to address these devices with user-written code.

7.1.1 SMI Ticker

The output of counter/timer 2 of the W83C553F may be routed to the System Management Interrupt input of the CPU when J1701 is set to position 7-8. This can be used to generate a periodic interrupt with higher priority than normal interrupts. A negative edge of the PC-Speaker output triggers the SMI when enabled via bit 7 of I/O address $809.

Writing to I/O address $808 clears the SMI.

Table 30: SMI Status Register read/write

Register								
SMI Status register	D7	D6	D5	D4	D3	D2	D1	D0
	SMIPE							

Read:

SMISR: I/O Address: $808
SMIPE = 0: no SMI pending
SMIPE = 1: SMI pending

Write:

Clears pending SMI

Register								
SMI Status register	D7	D6	D5	D4	D3	D2	D1	D0
	SMIPE							

Write:

SMICR: I/O Address: $809

ENSMI = 0: disable SMI

ENSMI = 1: enable SMI

7.1.2 Enhanced Serial Communications Controller (ESCC)

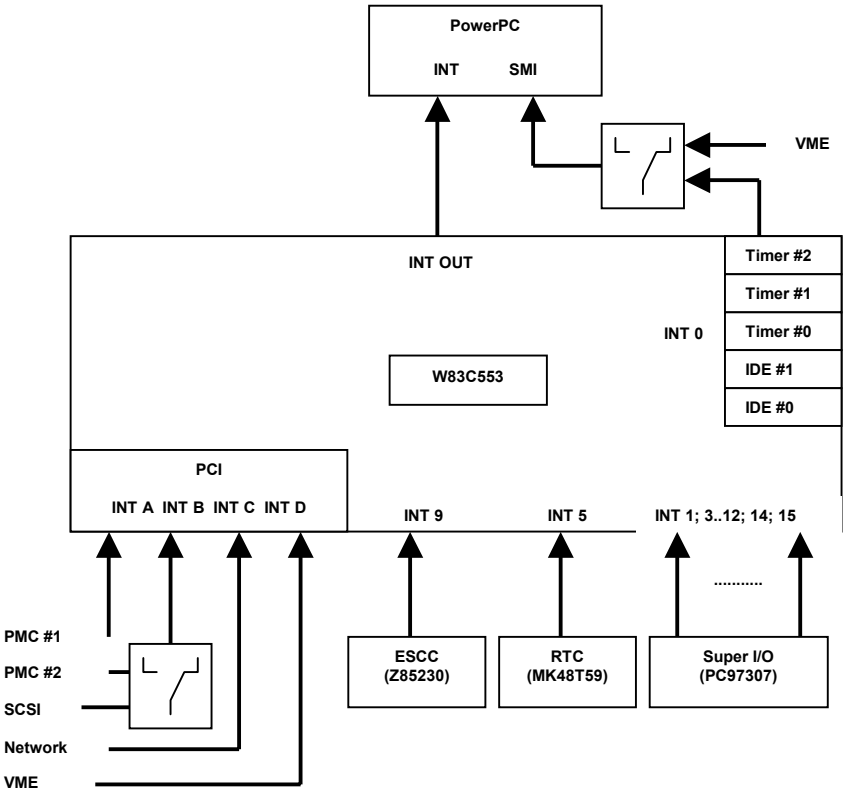
In addition to the two serial controllers COM1 and COM2 that are incorporated in the PC97307 Super-I/O the BAB 740 features another two serial lines that are realized with a Z85230 ESCC. The ESCC is clocked with 12 MHz or 14.7456 MHz. This allows transfer rates up to 3 MBaud synchronous and 230.4 KBaud asynchronous. Channel A can be operated with DMA to reduce interrupt load of the CPU for synchronous block protocols. DMA channel 0 is used for receive and Channel 1 for transmit. The DMA controller must be programmed to type A or B mode. The Interrupt request of the ESCC is connected to INT9 input of the interrupt controller.

Table 31: ESCC Address Assignment:

I/O Address	Description
$800	ESCC Channel B Control
$801	ESCC Channel A Control
$802	ESCC Channel B Data
$803	ESCC Channel A Data

7.1.3 Interrupt Controller

Figure 6: BAB 740 Interrupt Diagram



This diagram shows how the on-board interrupt sources are connected to the interrupt controller, located logically in the W83C553 chip. This chip then prioritizes and drives the two CPU interrupt inputs. The priority scheme used is shown below:

Table 32: Interrupt

Priority	ISA IRQ	PCI IRQ	Source
1	INT 0		Timer 0 (Ticker)
2	INT 1		Keyboard
3	INT 8		
4	INT 9		ESCC
5	INT10	INT A	PMC #1
6	INT 11	INT B	SCSI or PMC #2
7	INT 12		
8	INT 13		
9	INT 14	INT C	Ethernet
10	INT 15	INT D	VME
11	INT 3		Serial #2
12	INT 4		Serial #1
13	INT 5		RTC
14	INT 6		Floppy
15	INT 7		Parallel Port

7.1.4 SRAM/RTC

A indirect addressing scheme is used to access the M48T59Y SRAM/RTC. To access the SRAM/RTC the desired address first must be written to I/O address $70 and $71. Then the data can be accessed via I/O address $76. The interrupt output of the M48T59Y is connected with the INT5 input of the interrupt controller. It may be used to generate periodic interrupts or watchdog interrupts.

Table 33: SRAM/RTC Address Assignment

I/O Address	Description
$070	SRAM/RTC LSB Address
$071	SRAM/RTC MSB Address
$076	SRAM/RTC Data

7.1.5 GPIO Use

The GPIOs of the Super-I/O are used for the following purposes:

Table 34: GPIO Usage

Name	Type	Function
GPIO10	-	not used
GPIO11	I	CPU Bus Speed (0 = 83 MHz; 1 = 66MHz)
GPIO12	I	L2 Cache Size (0 = 256 KByte; 1 = 512KByte)
GPIO13	I/O	I2C Data for SPD of 2nd SODIMM
GPIO14	O	I2C Clock for SPD of 2nd SODIMM
GPIO15	I/O	I2C Data for SPD of 1st SODIMM, ELTEC Revision EEPROM
GPIO16	O	I2C Clock for SPD of 1st SODIMM, ELTEC Revision EEPROM
GPIO17	-	not used
GPIO20	-	not used
GPIO21	-	not used
GPIO22	-	not used
GPIO23	-	not used
GPIO24	I	HEX Switch LSB
GPIO25	I	HEX Switch
GPIO26	I	HEX Switch
GPIO27	I	HEX Switch MSB

7.1.6 Super-I/O Power-on Strappings

The Super-I/O wakes up in the following configuration:

Table 35: Super-I/O Wake Up Configuration:

Pin	Configuration
CFG0	FDC, KBC and RTC inactive
CFG1	No X-Bus Data Buffer
CFG3,2	Clock source is 24 MHz fed via X1 Pin
BADDR1,0	PnP Motherboard, Wake in Config state, Index 015Ch
SELCS	/CS0 on /CS0 pin

7.1.7 I/O Address Map

After initialization the following I/O address map becomes effective:

Table 36: I/O Address Map

I/O Address	Device	Description
$000-$00F	W83C553F	DMA Controller 1
$020-$021	W83C553F	Interrupt Controller 1
$040-$043	W83C553F	Counter/Timer
$060	PC97307	Keyboard Data
$061	W83C553F	Port B
$064	PC97307	Keyboard Control
$070	M48T59Y	SRAM/RTC LSB Address
$071	M48T59Y	SRAM/RTC MSB Address
$076	M48T59Y	SRAM/RTC Data
$078-$07B	W83C553F	BIOS Timer
$081-$082	W83C553F	DMA Page
$087	W83C553F	DMA Page
$089-$08B	W83C553F	DMA Page
$092	W83C553F	Port 92
$0A0-$0A1	W83C553F	Interrupt Controller 2
$0C0-$0DE	W83C553F	DMA Controller 2
$15C	PC97307	SuperI/O Index
$15D	PC97307	SuperI/O Data
$220-$223	PC97307	GPIO Port 1
$224-$227	PC97307	GPIO Port 2
$278-$27F	PC97307	Parallel Port
$2F8-$2FF	PC97307	COM2
$3F0-$3F7	PC97307	Floppy
$3F8-$3FF	PC97307	COM1
$3C2-$3C9	SM810	VGA Controller
$3CE-$3CF	SM810	VGA Controller
$3D4-$3D5	SM810	VGA Controller
$4D0-$4D1	W83C553F	Interrupt Mode
$808	MACH210	SMI Status Register
$809	MACH210	SMI Control Register
$800	Z85230	ESCC Channel B Control
$801	Z85230	ESCC Channel A Control
$802	Z85230	ESCC Channel B Data
$803	Z85230	ESCC Channel A Data

7.1.8 Memory Address Map

The BAB 740 uses address map B (CHRP) of the MPC106. After initialization the following address map becomes effective:

Table 37: Memory Address Map (default used by VxWorks)

CPU Address	PCI Address	Device
$0000.0000-$07FF.FFFF	-	local RAM
$0800.0000-$7FFF.FFFF	-	reserved
$8000.0000-$F9FF.FFFF	$8000.0000-$F9FF.FFFF	PCI memory space
$FA00.0000-$FAFF.FFFF	$FA00.0000-$FAFF.FFFF	PCI memory space (PMVIEW)
$F903.0000-$F903.EFFF	$F903.0000-$F903.EFFF	PCI memory space (PMGRAB)
$F904.0000-$F904.FFFF	$F904.0000-$F904.FFFF	PCI memory space (UniverseII)
$FB00.0000-$FCFF.FFFF	$FB00.0000-$FCFF.FFFF	PCI memory space (VMEbus)
$FD00.0000-$FDFF.FFFF	$0000.0000-$00FF.FFFF	PCI/ISA memory space
$FE00.0000-$FE00.FFFF	$0000.0000-$0000.FFFF	PCI/ISA I/O space
$FE01.0000-$FE7F.FFFF	-	reserved
$FE80.0000-$FE80.FFFF	$0080.0000-$0080.FFFF	PCI I/O space
$FE81.0000-$FE81.FFFF	$0081.0000-$0081.FFFF	PCI I/O space (SCSI Controller)
$FE82.0000-$FE82.FFFF	$0082.0000-$0082.FFFF	PCI I/O space (LAN Controller)
$FE83.0000-$FEBF.FFFF	$0083.0000-$00BF.FFFF	PCI I/O space
$FEC0.0000-$FEDF.FFFF	CONFIG_ADDR	PCI configuration address register
$FEE0.0000-$FEEF.FFFF	CONFIG_DATA	PCI configuration data register
$FEF0.0000-$FEFF.FFFF	$FEF0.0000-$FEFF.FFFF	PCI interrupt acknowledge
$FF00.0000-$FF7F.FFFF	-	reserved
J114 open:		
$FF80.0000-$FF9F.FFFF	$FF80.0000-$FF9F.FFFF	User Flash EPROM
$FFA0.0000-$FFBF.FFFF	$FFA0.0000-$FFBF.FFFF	Mirrored User Flash EPROM
$FFC0.0000-$FFC7.FFFF	$FFC0.0000-$FFC7.FFFF	System Flash EPROM
$FFC8.0000-$FFFF.FFFF	$FFC8.0000-$FFFF.FFFF	Mirrored System Flash EPROM
J114 closed:		
$FF80.0000-$FF87.FFFF	$FF80.0000-$FF87.FFFF	System Flash EPROM
$FF88.0000-$FFBF.FFFF	$FF88.0000-$FFBF.FFFF	Mirrored System Flash EPROM
$FFC0.0000-$FFDF.FFFF	$FFC0.0000-$FFDF.FFFF	User Flash EPROM
$FFE0.0000-$FFEF.FFFF	$FFE0.0000-$FFEF.FFFF	2nd MByte User Flash EPROM
$FFF0.0000-$FFFF.FFFF	$FFF0.0000-$FFFF.FFFF	2nd MByte User Flash EPROM

7.1.9 PCI IDSEL

The IDSEL input of each PCI device is connected to one of the PCI address/data lines for individual addressing in configuration space. Table XX shows the connection of the IDSEL signal for the various devices on the BAB 740 and the PMC carrier board.

Table 38: IDSEL Connection

Device Number	IDSEL	Device
0	-	MPC106
11	AD(11)	W83C553F
13	AD(13)	SYM53C860
14	AD(14)	21143
15	AD(15)	PMC Slot 0
16	AD(16)	PMC Slot 1
30	AD(30)	Universe II

Note that the device numbers differ from Intel convention where number 0 corresponds to AD(11) and number 20 corresponds to AD(31). Configuration cycles with device number 0 are handled internally in the MPC106 and therefore don‘t correspond with a address/data line.

7.2 Factory-settable Jumpers

Table 39: CPU Drive Strength Configuration (J101, J102)

J102	J101	Description
short	short	disabled
short	-	normal (default)
-	short	strong
-	-	herculean

SMD jumper for factory use only

Note: Implementation specific settings; do not change!

Table 40: CPU PLL Configuration (J103...J106)

J106	J105	J104	J103	Bus Mult.	Bus Clock
short	short	short	short	x 7	25-33
short	short	short	-	-	-
short	short	-	short	-	-
short	short	-	-	bypass	-
short	-	short	short	x 2	60-83
short	-	short	-	x 6,5	25-40
short	-	-	short	x 2,5	50-83
short	-	-	-	x 4,5	33-60
-	short	short	short	x 3	40-83
-	short	short	-	x 5,5	25-40
-	short	-	short	x 4	33-66 (default)
-	short	-	-	x 5	25-50
-	-	short	short	-	-
-	-	short	-	x 6	25-40
-	-	-	short	x 3,5	40-75
-	-	-	-	off	off

SMD jumper for factory use only

Note: Implementation specific settings; do not change!

Table 41: System Clock (J111, J112, J113)

J111	J112	J113	CPU Bus Clock	PCI Bus Clock
short	short	short	30	25
short	short		60	30
short		short	62,5	25
short			66	33 (default)
	short	short	75	37,5
	short		83	33

SMD jumper for factory use only!

Note: Implementation specific settings; do not change!

Table 42: MPC106 PLL Configuration (J110...J107)

J110	J109	J108	J107	Mult.	Bus Clock	PCI Clock
short	short	short	short	-	-	-
short	short	short	-	x 1	33	33
short	short	-	short	x 1	16-25	16-25
short	short	-	-	bypass	-	-
short	-	short	short	x 2	66	33 (default)
short	-	short	-	x 2	33-50	16-25
short	-	-	short	x 2,5	83	33
short	-	-	-	x 2,5	41-50	16-20
-	short	short	short	x 3	75-100	25-33
-	short	short	-	x 3	50	16
-	short	-	short	-	-	-
-	short	-	-	-	-	-
-	-	short	short	-	-	-
-	-	short	-	-	-	-
-	-	-	short	-	-	-
-	-	-	-	off	-	-

SMD jumper for factory use only

Note: Implementation specific settings; do not change!

Table 43: Cache Size (J601, J602, J603)

J601	J602	J603	PCI Bus Clock
1-2	1-2	open	512 Cache (default)
2-3	2-3	short	256 Cache

SMD jumper for factory use only!

Note: Implementation specific settings; do not change!

Table 44: Hardware Debugger Configuration (J1301)

J1301	Operation
1-2	normal operation (default)
2-3	enable COP

Note: Implementation specific settings; do not change!

Table 45: Revision EEPROM Write Protection (J1302)

J1302	Operation
open	write protect
short	write enable (default)

BAB 740 Revision	
BAB 740 version:	
Memory size:	
Hardware revision:	
Serial number:	
BSP revision:	
System monitor revision:	
BAB 740 Configuration	
BAB 740 IP address:	
Host IP address:	
User name:	
Ftp password:	
Boot file:	
Boot configuration (ftp, bootp, ...)	
Host Configuration	
Ethernet IP address:	
Development tool revision (VxWorks, OS-9, ...)	
Operating system and revision (WinNT, ...)	
Error Description What must be done to reproduce the error:	
Editional configuration (VxWorks: config.h)	

Send the completed form to:
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NOTES: