Microcontroller Technical Information

8-Bit Microcontroller μPD78F0714 Usage Restrictions	Document No.	ZBG-CC-07-0014		1/1
	Date issued	July 18, 2007		
	Issued by	2nd Product Solution Group Multipurpose Microcomputer Systems Division Microcomputer Operations Unit NEC Electronics Corporation		
Related documents μPD78F0714 User's Manual: U16928EJ	Notification classification	√	Usage restriction	
			Upgrade	
			Document modification	
			Other notification	

1. Affected product

μPD78F0714

2. Restriction details

A new restriction (No. 1) has been added.

- No. 1 Restriction on interrupt signals generated by low-voltage detector
  Masking of interrupt sources to be masked is not available and interrupts operate as non-maskable interrupts.

3. Workaround

The following workaround is available for this restriction. See the attachment for details.

- No. 1 When using the low-voltage detector, be sure to include into interrupt servicing a program routine that judges the validity of interrupts generated by the low-voltage detector. (This also applies when interrupts generated by the low-voltage detector are used as reset.)

4. Modification schedule

Device modification for restrictions is not planned. Regard the restriction added in this document as a usage restriction.

The descriptions concerning this issue in the user's manual will be corrected in the next revision.

(Chapters in question: *Chapter 19 Interrupt Functions* and *Chapter 23 Low-Voltage Detector*)

5. List of restrictions

The restriction history and detailed information is described in the attachment.

6. Document revision history

8-Bit Microcontroller μPD78F0714 Usage Restrictions

Document Number	Date Issued	Description
ZBG-CC-07-0014 (latest version)	July 18, 2007	No. 1

List of Restrictions in μPD78F0714

1. Product Version

μPD78F0714: Rank K

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

No.	Usage Restrictions	Rank
		K
1	Restriction on interrupt signals generated by low-voltage detector	Δ

○: Not applicable, Δ: Applicable

3. Details of Usage Restrictions

No. 1 Restriction on interrupt signals generated by low-voltage detector

[Description]

The following two operating modes are available for the low-voltage detector (LVI).

1. Used as reset
2. Used as interrupts

An LVI interrupt may occur when the LVI operation is enabled, in both of the above modes.

In other products, interrupts generated by the LVI operate as maskable interrupts and can therefore be masked. In this product, however, they operate as non-maskable interrupts and therefore cannot be masked.

The program of LVI interrupt service routines must therefore be included, even if interrupts generated by the LVI are used for reset.

When they are used as interrupts, whether the interrupt is caused by low-voltage detection or it is an interrupt generated when the LVI operation is enabled must be identified with respect to the interrupt service routine.

Concerning the use as the interrupt function, the μPD78F0714 user's manual (document number: U16928JJ1V0UD00, U16928EJ1V0UD00) and the actual device differ in the following three points.

1. Zero is always read from bit 0 of the interrupt request flag register (IF0L).
2. Interrupts cannot be masked with bit 0 of the interrupt mask flag register (MK0L).
3. The interrupt priority order cannot be changed with bit 0 of the priority flag register (PR0L).
   The interrupt with the highest priority is always serviced.

[Conditions under which this issue does not occur]

When the LVI function is not used.

[Workaround]

Implement any of the following workarounds.

1. When using the LVI for generating reset

   Add an interrupt routine.

   (1) Wait for 0.2 ms or longer, using software.

   (2) Wait until after confirming that the power supply voltage (V_{DD}) is higher than the detection voltage (V_{LVI}), using bit 0 (LVIF) of the LVIM register.

   (3) Set bit 1 (LVIMD) of the LVIM register to "1".

2. When using the LVI for generating interrupts

(1) Define the flag as a global variable.

(2) Set the flag before enabling the LVI operation.

The meanings of this flag are as follows.

0: It is confirmed that the power supply voltage (V_{DD}) is higher than the detection voltage (V_{LVI}) after the LVI operation.

1: It has not been confirmed that the power supply voltage (V_{DD}) is higher than the detection voltage (V_{LVI}) after the LVI operation.

(3) Enable the LVI operation.

(4) Wait for 0.2 ms or longer, using software.

(5) Wait until after confirming that the power supply voltage (V_{DD}) is higher than the detection voltage (V_{LVI}), using bit 0 (LVIF) of the LVIM register.

(6) Clear the flag.

Add the following processing at the beginning of interrupts.

(1) Check the flag (0: Normal processing, 1: Implement the following steps)

(2) Wait for 0.2 ms or longer, using software.

(3) Wait until after confirming that the power supply voltage (V_{DD}) is higher than the detection voltage (V_{LVI}), using bit 0 (LVIF) of the LVIM register.

(4) Clear the flag.

(5) Return to the main routine.

Remark In addition to the above code, processing to wait for the voltage variation period is required in a system in which the power supply voltage (V_{DD}) varies around the LVI detection voltage.

Contact an NEC Electronics sales representative if you have any questions or concerns regarding this issue.