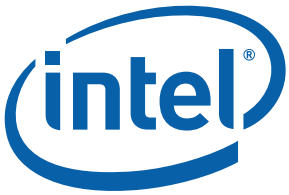

Intel® IXP435 Multi-Service Residential Gateway Reference Platform

User's Guide

June 2007

Document Number: 316848; Revision: 001US

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June 2007
Document Number: 316848; Revision: 001US

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Revision History

Date	Revision	Description
June 2007	001	Initial release

1.0 Introduction

1.1 Purpose

This document provides detailed design information for the Intel® IXP435 Multi-Service Residential Gateway Reference Platform.

The IXP435 reference platform includes the basic blocks of an Intel® IXP43X Product Line of Network Processor-based system, DDR memory, PCI, and connectors through which UTOPIA level 2, MII, FXS, FXO, T1/E1 and power devices are connected. Several mezzanine cards designed (used in IXDP465 platform) in conjunction with the IXP435 multi-service residential gateway reference platform plug-in through the UTOPIA level 2 or MII connector.

1.2 Intended Audience

The intended audience for this document includes hardware architects and developers who are developing both hardware and software for applications based on the Intel® IXP43X Product Line. The IXP435 reference platform is designed to meet the market requirements for a flexible customer-oriented platform. This platform demonstrates the capabilities of the IXP43X product line of network processors in a system and enables software development of the IXP43X product line of network processors. Customers can base their designs on portions of the IXP435 reference platform design.

1.3 Prerequisites

The Intel® IXP435 Multi-Service Residential Gateway Reference Platform supports all available features of the Intel® IXP43X Product Line of Network Processors. Many features, such as the network processor engine (NPE) functions, are enabled by a specific revision of the Intel-supplied software.

Refer to Table 2, "Related Intel Documentation" on page 8 for a list of hardware, software, and platform documents that will assist in the development process. In particular, the following documents provide details on available features:

- *Intel® IXP43X Product Line of Network Processors Datasheet* has a complete list of available product features.
- *Intel® IXP400 Software Programmer's Guide* provides information on the features that are enabled in a particular software release.

The IXP435 reference platform features that require enabling by software supplied by Intel are summarized in Table 1.

Table 1. Intel® IXP435 Multi-Service Residential Gateway Reference Platform Features Summary

Features that do not require enabling software	Features that require enabling software from Intel
Intel XScale® Processor -- up to 667 MHz	Encryption/Authentication (AES/AES-CCM/3DES/DES/ SHA-1/SHA-256/SHA-384/SHA-512/MD-5
PCI v. 2.2 33 MHz (Host/Option)	One High-Speed Serial (HSS) interface
Two USB 2.0 Host Controller	Two Network Processor Engines (NPEs)
DDRII/DDRI SDRAM interface	Up to two MII interfaces
Slave Interface Expansion bus	One UTOPIA Level 2 interface
One UART	
Internal Bus Performance Monitoring Unit	
16 GPIOs	
Four internal timers	
Synchronous Serial Protocol (SSP) port	

Note: It is recommended that users have access to the documents listed in Table 2 and refer to them when necessary. This document does not explore the IXP43X product line internal architecture, but describes the processor's interfaces to peripherals that are used on the IXP435 reference platform. Schematics and a bill of materials are available in the IXP435 reference platform Documentation Kit (zip file) that can be obtained through your local Intel sales representative.

1.4 Related Documentation

Table 2 and Table 3 list the documentation from Intel and other sources that provide additional information for the development of hardware and software based on the IXP43X product line.

Table 2. Related Intel Documentation (Sheet 1 of 2)

Title	Document #	Location
Intel® IXP435 Multi-Service Residential Gateway Reference Platform Documentation Kit	N/A	Through your local Intel sales representative
Intel® IXP43X Product Line of Network Processors Developer's Manual	316843	Through your local Intel sales representative
Intel® IXP43X Product Line of Network Processors Datasheet	316842	Through your local Intel sales representative
Intel® IXP400 Software Programmer's Guide	252539	IXP4XX Documentation Web Page†
Intel® IXP400 Software Specification Update	307310	IXP4XX Documentation Web Page†
Designing Embedded Networking Applications - Essential Insights for Developers of Intel® IXP4XX Network Processor Systems	N/A	http://www.intel.com/intelpress/sum_ixp4.htm
NX1702 Nexperia Media Processor of Philips*	N/A	http://www.semiconductors.philips.com

† This document is available at: http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm

Table 2. Related Intel Documentation (Sheet 2 of 2)

Title	Document #	Location
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor: *Customizing RedBoot* Application Note*	254308	IXP4XX Documentation Web Page†
Intel® IXDP465 Development Platform User's Manual		IXP4XX Documentation Web Page†
Intel® XScale™ Core Developer's Manual	273473	IXP4XX Documentation Web Page†

† This document is available at: http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm

Table 3. Related External Documentation

Title and Revision	Location
PCI Bus Specification, Rev. 2.2	http://www.pcisig.com/
MiniPCI Specification, 1.0	http://www.pcisig.com/
UTOPIA Level 2 Specification, Revision 1.0	http://www.atmforum.com/
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/
JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79D	http://www.jedec.org

1.5 Terminology

Table 4 lists the acronyms and common terms used in this manual.

Table 4. List of Terminology (Sheet 1 of 2)

Acronym	Description
ADSL	Asymmetric Digital Subscriber Line
Assert	Logically active value of a signal or bit
ATM	Asynchronous Transfer Mode
CPE	Customer Premise Equipment
DDR	Double-Data Rate
DMA	Direct Memory Access
DSL	Digital Subscriber Line
E1	Euro 1 trunk line
FXO	Foreign Exchange Office
FXS	Foreign Exchange Subscriber
GPIO	General-Purpose Input/Output
HSS	High-Speed Serial (port)
IP	Internet Protocol
IXP	Internet Exchange Processor
LAN	Local Area Network
LSB	Least-Significant Byte
MAC	Media Access Controller
MDIO	Management Data Input/Output
mezzanine card	A circuit board that attaches to the development platform baseboard and provides additional functionality. Mezzanine cards may be stackable. Also called daughtercard.

Table 4. List of Terminology (Sheet 2 of 2)

Acronym	Description
MII	Media-Independent Interface
MSB	Most-Significant Byte
NPE	Network Processor Engine
PCI	Peripheral Component Interface
PHY	Physical Layer (Layer 1) Interface
Reserved	A field that may be used by an implementation. Software should not modify reserved fields or depend on any values in reserved fields.
RX	Receive (HSS is receiving from off-chip)
SDRAM	Synchronous Dynamic Random Access Memory
T1	Type 1 trunk line
TX	Transmit (HSS is transmitting off-chip)
UART	Universal Asynchronous Receiver-Transmitter
UTOPIA	Universal Test and Operation PHY Interface for ATM
DVI	Digital Video Interface
CVBS	Composite Video Baseband Signal
LCD	Liquid Crystal Display
CCIR 656	CCIR Recommendation 656
WAN	Wide-Area Network

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2.0 Intel® IXP435 Multi-Service Residential Gateway Reference Platform Hardware Design

This chapter provides detailed design information of all interfaces, components and features contained on the Intel® IXP435 Multi-Service Residential Gateway Reference Platform.

The Intel® IXP43X Product Line of Network Processors is positioned to enable both cost sensitive Gateways and Converged Access Platforms (CAP). The platform has integrated SLIC codecs and DAA circuitry for VoIP and Philips* PNX1702 Nexperia media processor to support media centric applications such as triple-play.

2.1 Overview of the Intel® IXP435 Multi-Service Residential Gateway Reference Platform

Figure 1 shows the block diagram of the IXP435 reference platform. The IXP435 reference platform comprises the following:

- Memory subsystem
- Networking subsystem
- I/O subsystem
- Power and reset subsystem
- VoIP subsystem
- Media subsystem

The following sections describe the high level design of each subsystem respectively.

- Intel® IXP43X Product Line of Network Processors
- Media processor (Philips* PNX1702)
- NOR Flash Memory (16 MB for IXP43X network processors)
- NAND Flash Memory (64 MB for IXP43X network processors)
- DDRII (128 MB for IXP43X network processors)
- DDR Memory (64 MB for Media processor)
- Video encoder (Philips* SAA7104H)
- Audio DAC (Philips* UDA1334)
- Video decoder (Philips* SAA7118)
- Audio ADC (Philips* UDA1361)
- Two SLIC/CODEC (Silicon Laboratories* Si3216 and Si3201)
- Voice/Data DAA (Silicon Laboratories* Si3050 and Si3019)
- Ethernet Switch (Kendin* 8995M)
- USB 2.0 host connector (Two ports)
- Two Mini-PCI slots

- One PCI Slot
- One 120 pin MII connector
- One 120 pin UTOPIA connector
- Infrared remote control (use GPIO of IXP43X network processors)
- S-Video, composite video and YCbCr/YPbPr for Video outputs
- S-Video, and composite video for Video inputs
- I2S and S/PDIF stereo audio outputs and input
- Two JTAG (for IXP43X network processors and Media processor)
- Two FXS RJ11 Port (VoIP function)
- One FXO RJ11 Port
- One 10/100 Mbps Ethernet port for WAN
- Four 10/100 Mbps Ethernet ports for LAN
- One 2KByte EEPROM for Media processor
- One Serial port for debug used

Mezzanine cards that are optional and that can be purchased separately include:

- Intel® IXPDSM465 ADSL UTOPIA level 2 mezzanine card
- Intel® IXPVM465 Analog Voice mezzanine card (4-FXS, 1-FXO)
- Intel® IXPFRM465 Quad T1/E1 mezzanine card
- Intel® IXPETM465 Ethernet PHY mezzanine cards

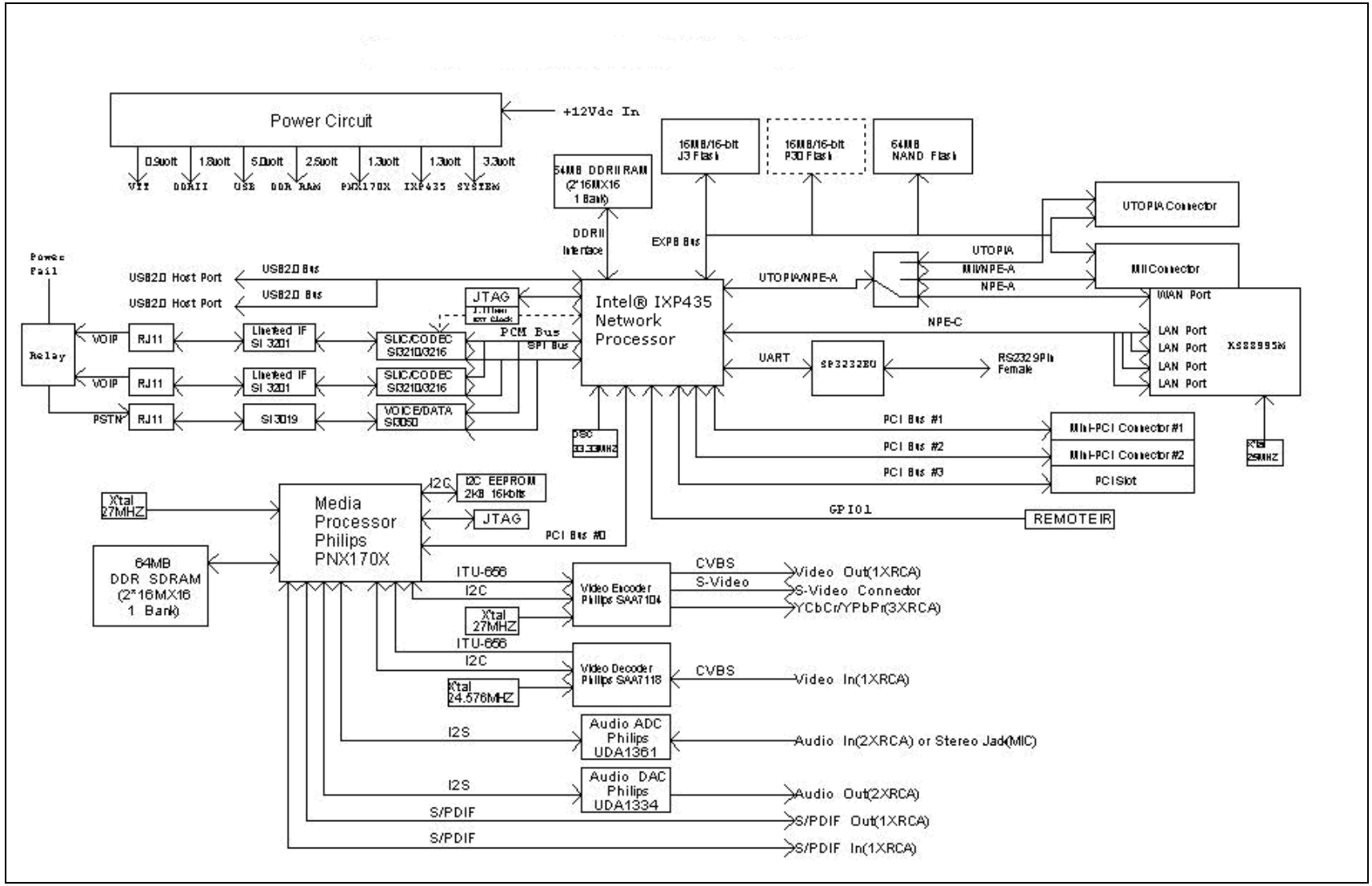
The listed mezzanine cards have the same design as the one for the Intel® IXDP465 Development Platform.

Note: This document will not describe information on the above mezzanine cards. Refer to the Intel® IXDP465 Development Platform User's Guide for features and description of the mezzanine card hardware design.

2.2 Functional and Physical Layout of the Intel® IXP435 Multi-Service Residential Gateway Reference Platform

The connections between the devices on the baseboard and mezzanine cards are shown in Figure 1. Details of the devices are described in the following sections .

Figure 1. Intel® IXP435 Multi-Service Residential Gateway Reference Platform Functional Block Diagram



2.3 Component Placement

The component layout of the Intel® IXP43X Product Line of Network Processors is shown in Figure 2 and Figure 3.

Figure 2. Intel® IXP435 Multi-Service Residential Gateway Reference Platform Primary Side Placement

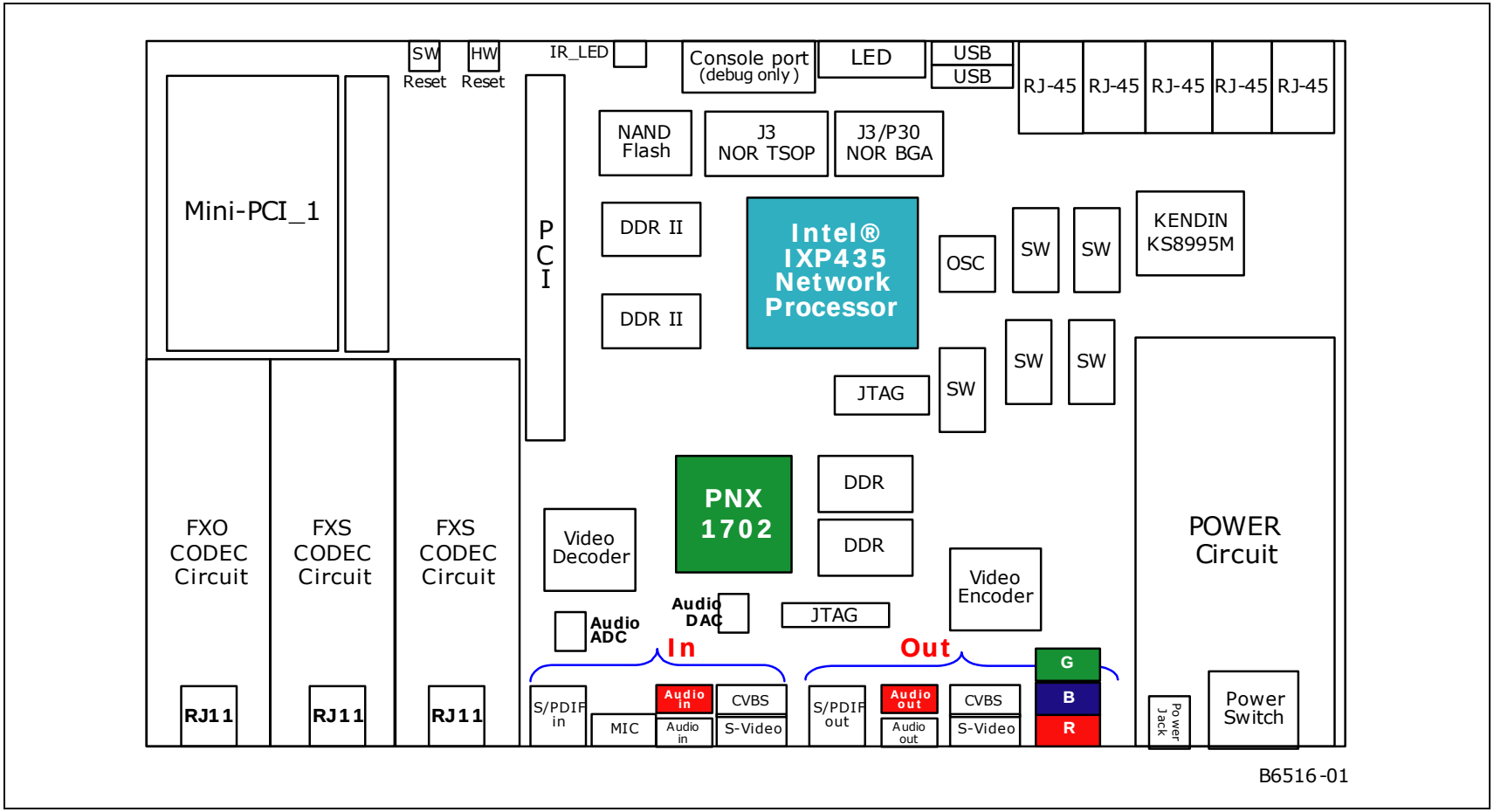
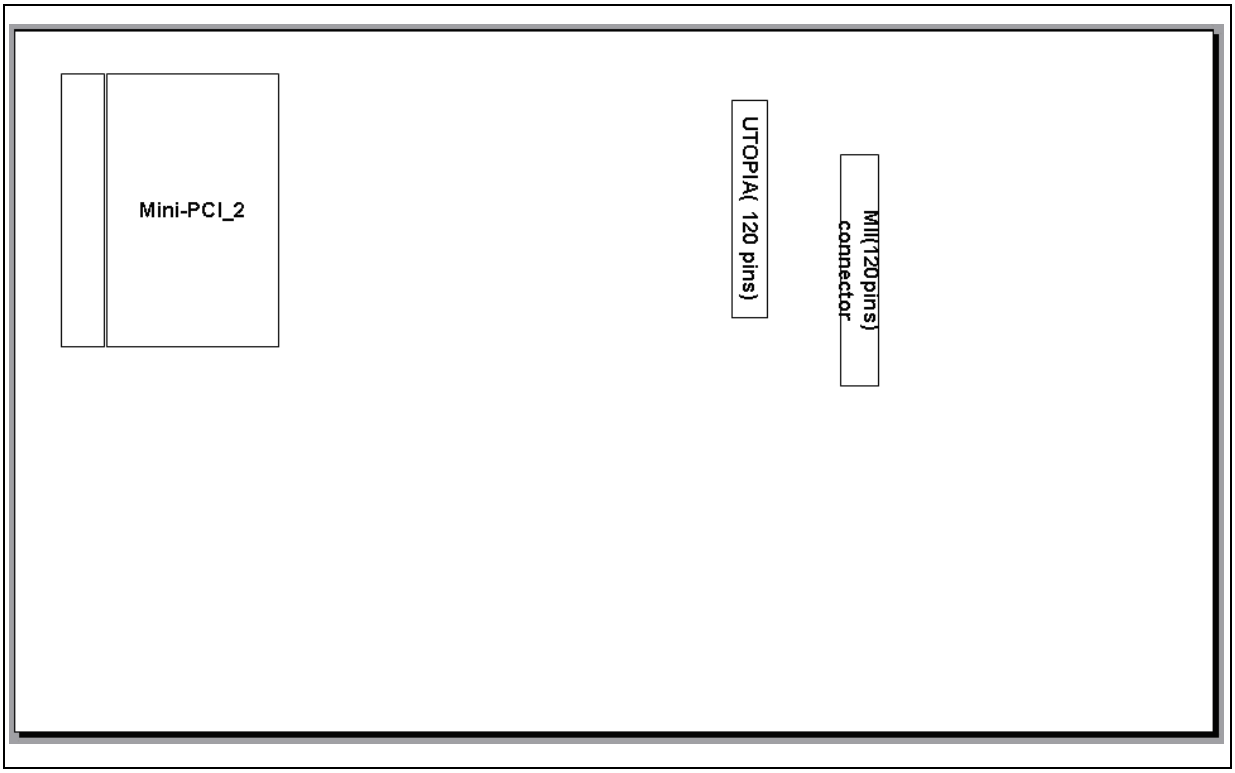


Figure 3. Intel® IXP435 Multi-Service Residential Gateway Reference Platform Bottom Side Placement



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3.0 Design Solution Description

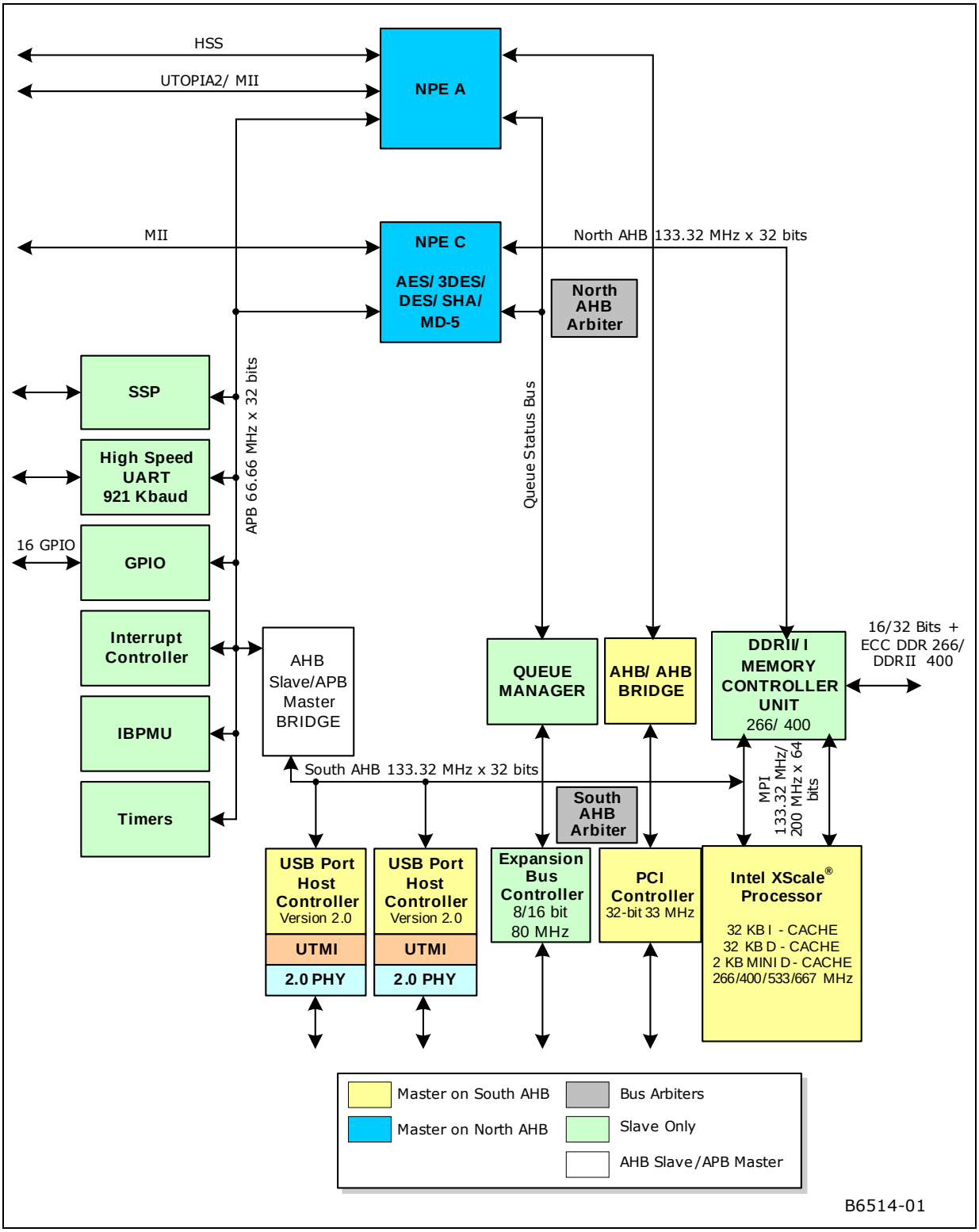
3.1 Intel® IXP43X Product Line of Network Processors

The Intel® IXP435 Multi-Service Residential Gateway Reference Platform is populated with 667 MHz IXP43X network processors. Jumpers are provided to configure the default core execution speed through the hardware strapping configurations.

A 33.33 MHz oscillator acts as the input clock signal to the IXP43X network processors.

The high-level view of the IXP43X network processors is shown in Figure 4.

Figure 4. Intel® IXP43X Product Line Functional Block Diagram



3.2 PCI Interface

The IXP435 reference platform supports the following four PCI devices as shown in Figure 1.

- PCI Device #0: Media Processor
- PCI Device #1: Mini-PCI #1 connector
- PCI Device #2: Mini-PCI #2 connector
- PCI Device #3: PCI Slot

The IXP43X network processors act as the PCI host and all other devices act as PCI targets. The IXP435 reference platform supports only PCI 33 MHz bus operation with PCI 2.2 compliance.

The IXP435 reference platform supports two external 32-bit Mini-PCI devices (3.3V only) and allows capabilities such as wireless LAN (for example, 802.11 a/b/g) and PCI version 2.2 is used.

Table 5 describes the IDSEL mapping and GPIO mapping on the PCI devices of the IXP435 reference platform. The IDSEL signals are connected to the PCI_AD bus and these GPIO pins are for interrupt function.

See the following tables for pin assignment details:

Table 5. IDSEL and GPIO Mapping on the PCI Devices

SLOT ID	Device	Interrupt GPIO	IDSEL
Slot 0	Media Processor PNX1702	GPIO11	PCI_AD31
Slot 1	Mini-PCI #1	GPIO10	PCI_AD30
Slot 2	Mini-PCI #2	GPIO9	PCI_AD29
Slot 3	PCI slot	GPIO8	PCI_AD28

3.2.1 PCI Clocking

The 33 MHz is generated by the IXP43X network processors through the GPIO 14 and a four-port zero delay buffer (Cypress CY2305*) drives the four PCI devices' clocks and the network processor PCI clock.

Table 6. PCI Host Slot Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	PCI_HST_TRST_N0	A33	3.3 V	B1	PCI_-12V_N0	B33	PCI_HST_CBE_N2
A2	12.0 V	A34	PCI_HST_FRAME_N	B2	PCI_HST_TCK0	B34	GND
A3	PCI_HST_TMS0	A35	GND	B3	GND	B35	PCI_HST_IRDY_N
A4	PCI_HST_TDI0	A36	PCI_HST_TRDY_N	B4	PCI_HST_TDO0	B36	3.3 V
A5	5.0 V	A37	GND	B5	5.0 V	B37	PCI_HST_DEVSEL_N
A6	PCI_HST_INTA_N	A38	PCI_HST_STOP_N	B6	5.0 V	B38	GND
A7	PCI_HST_INTC_N	A39	3.3 V	B7	PCI_HST_INTB_N	B39	PCI_HST_LOCK_N
A8	5.0 V	A40	PCI_HST_SMBCLK0	B8	PCI_HST_INTD_N	B40	PCI_HST_PERR_N
A9	-	A41	PCI_HST_SMBDAT0	B9	PCI_HST_PRSNT1_N0	B41	3.3 V
A10	3.3 V	A42	GND	B10	-	B42	PCI_HST_SERR_N
A11	-	A43	PCI_HST_PAR	B11	PCI_HST_PRSNT2_N0	B43	3.3 V
A14	-	A44	PCI_HST_AD15	B14	-	B44	PCI_HST_CBE_N1
A15	PCI_HST_RST_N	A45	3.3 V	B15	GND	B45	PCI_HST_AD14
A16	3.3 V	A46	PCI_HST_AD13	B16	PCI_HST_CLK0	B46	GND
A17	PCI_HST_GNT_N0	A47	PCI_HST_AD11	B17	GND	B47	PCI_HST_AD12
A18	GND	A48	GND	B18	PCI_HST_REQ_N0	B48	PCI_HST_AD10
A19	-	A49	PCI_HST_AD9	B19	3.3 V	B49	PCI_HST_M66EN0
A20	PCI_HST_AD30	A50	GND	B20	PCI_HST_AD31	B50	GND
A21	3.3 V	A51	GND	B21	PCI_HST_AD29	B51	GND
A22	PCI_HST_AD28	A52	PCI_HST_CBE_N0	B22	GND	B52	PCI_HST_AD8
A23	PCI_HST_AD26	A53	3.3 V	B23	PCI_HST_AD27	B53	PCI_HST_AD7
A24	GND	A54	PCI_HST_AD6	B24	PCI_HST_AD25	B54	3.3 V
A25	PCI_HST_AD24	A55	PCI_HST_AD4	B25	3.3 V	B55	PCI_HST_AD5
A26	PCI_HST_IDSEL0	A56	GND	B26	PCI_HST_CBE_N3	B56	PCI_HST_AD3
A27	3.3 V	A57	PCI_HST_AD2	B27	PCI_HST_AD23	B57	GND
A28	PCI_HST_AD22	A58	PCI_HST_AD0	B28	GND	B58	PCI_HST_AD1
A29	PCI_HST_AD20	A59	3.3 V	B29	PCI_HST_AD21	B59	3.3 V
A30	GND	A60	PCI_HST_REQ64_N0	B30	PCI_HST_AD19	B60	PCI_HST_ACK64_N0
A31	PCI_HST_AD18	A61	5.0 V	B31	3.3 V	B61	5.0 V
A32	PCI_HST_AD16	A62	5.0 V	B32	PCI_HST_AD17	B62	5.0 V

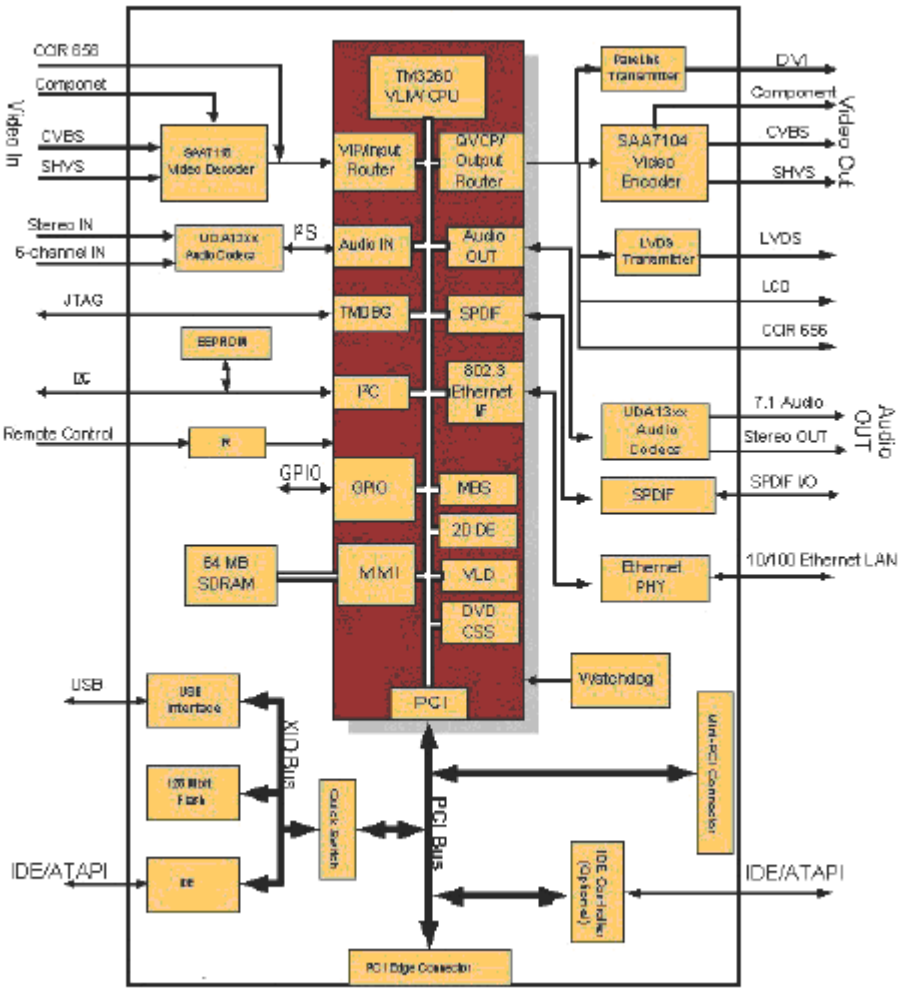
3.3 Media Processor

The audio/video function is controlled by PNX1702 Nexperia Media Processor of Philips*, which interfaces with the IXP43X network processors through the PCI interface. The PNX1702 Media Processor is a complete Audio/Video/Graphics system on a chip that contains a high-performance 32-bit VLIW processor, the TriMedia* TM3260.

The TriMedia* TM3260 is capable of software video and audio signal processing, and general purpose control processing. It is capable of running a pSOS* operating system with real-time signal processing tasks in a single programming and task scheduling environment. An abundance of interfaces make the PNX1702 suitable for networked

audio/visual products. The processor is assisted by several image and video processing accelerators that support image scaling and compositing. The high-level view of the PNX1702 Media Processor is shown in Figure 5.

Figure 5. Philips* PNX1702 Media Processor Functional Block Diagram



The Video/data in function is provided on a connector for S-Video and CVBS input. The Video/data out function supports S-Video, Component, DVI, CVBS, CCIR 656 and LCD operation. The CVBS and S-Video OUT and Y/Cb/Cr are provided on a connector plate provided with the board.

An SPDIF output unit outputs a high-speed serial data stream, primarily used to transmit digital SPDIF-formatted audio data to an external audio equipment.

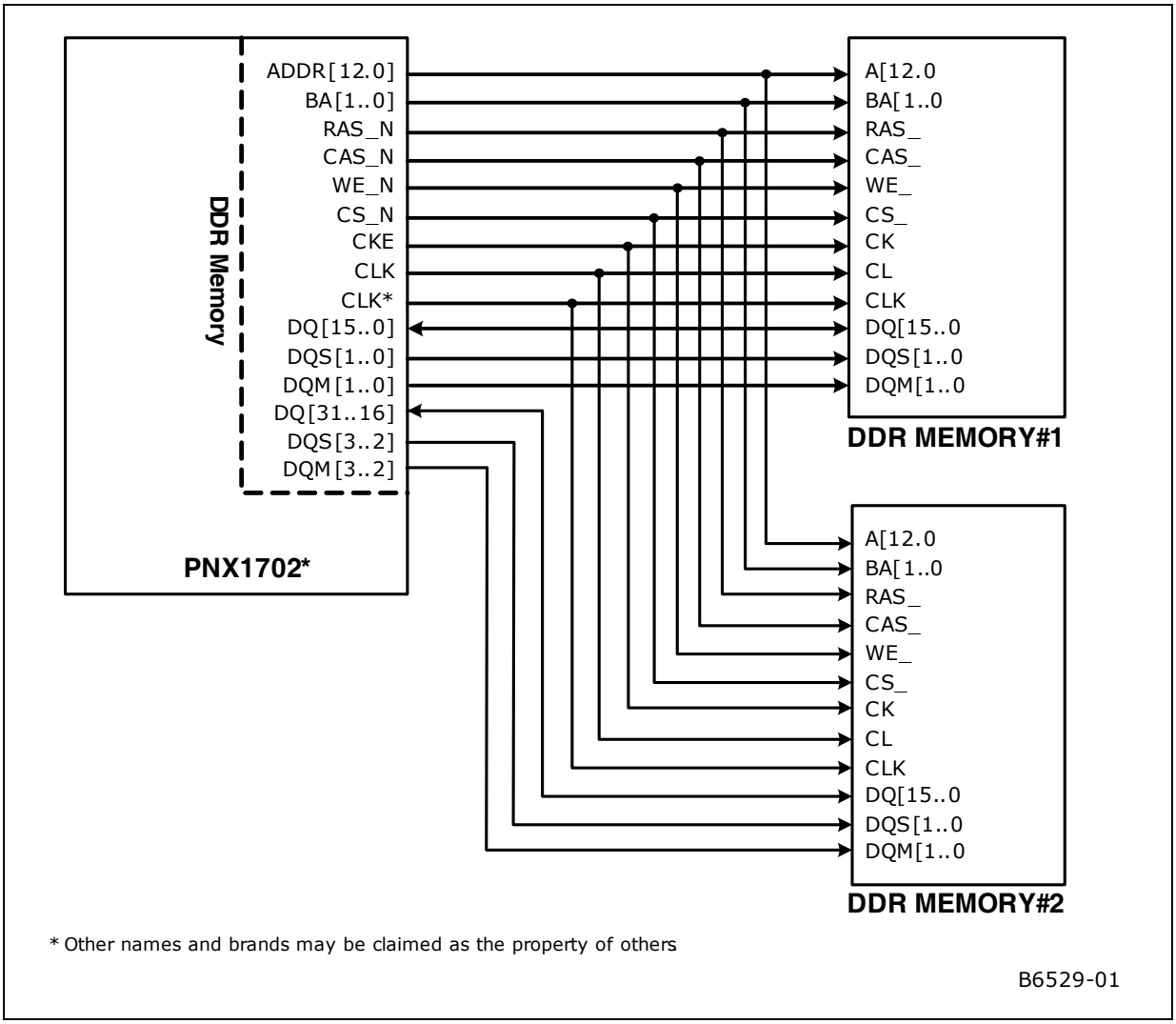
The Media Processor has a JTAG port that can be used for debugging. The Media Processor supports 64 Mbytes DDR memory using two chips each of 16M x 16 configuration. Bus frequency can be up to 200 MHz.

The Media Processor does not need any Flash memory for implementation. The I2C EEPROM of 2 Kbytes is implemented for the Media Processor.

Table 7. Supported Memory Configuration for Media Processor

DDR Memory Technology	DDR Memory Arrangement	Number of Chips	Number of Banks (system)	Total Memory Size	Suggested Memory Device
256 MBit	16M x 16	2	1	64 MB	Samsung (K4H561638D)

Figure 6. PNX1702 and DDR Memory Topology



The boot modes are defined by the state of the BOOT_MODE[7:0] pins at reset time.

Place adequate pull-ups and pull-downs on the system board to select the correct mode. The different boot modes based on the state of the BOOT_MODE[7:0] pins are described in Table 8:

Table 8. PNX1702 Configuration Strapping Boot Mode Settings

Boot mode bits	GPIO Pins	Default value upon bootup	Function	Description
7	11	0	EN_PCI_ARB	1 - Enables the internal PCI system arbiter 0 - Disables the internal PCI system arbiter
6:4	10:8	101	MEM_SIZE	Informs the boot scripts of the total memory size available on the system board. This information is crucial to set-up properly the PCI configuration management in host-assisted mode. The pin code is as follows: 000 - 256 MB (Reserved, recommended not to use) 001 - 256 MB (Reserved, recommended not to use) 010 - 8 MB 011 - 16 MB 100 - 32 MB 101 - 64 MB 110 - 128 MB 111 - 256 MB
3	3	0	CAS_LATENCY	DDR SDRAM devices support different types of CAS latencies. However they do not support all the combinations. PNX1702 offers the possibility to program the MMI (and therefore the DDR SDRAM devices) with the appropriate CAS latency at boot time. This is crucial for standalone boot from Flash memory devices since 8 KB of data is stored into the main memory during the execution of the boot scripts. 0 - 2.5 clock periods 1 - 3 clocks periods
2	2	1	ROM_WIDTH/ IIC_FASTMODE	This pin has a double functional mode: If BOOT_MODE[1:0] = "00", "01", or "10" (Boot from Flash memory) 0 - 8-bit data wide ROM 1 - 16-bit data wide ROM If BOOT_MODE[1:0] = "11" (Boot from I2C EEPROM) 0 - 100 KHz 1 - 400 KHz
1:0	1	11	BOOT_MODE	The main boot mode is determined as follows: 00 - Set up the system and start the TM3260 CPU from a 8- or 16-bit NOR Flash memory or ROM attached to the PCI-XIO bus. 01 - Set up the system and start the TM3260 CPU from a 8- or 16-bit NAND Flash memory or ROM attached to the PCI-XIO bus. 10 - Set up the PNX1702 system in host-assisted mode and allows the host CPU to finish to configure the PNX1702 system and start the TM3260 CPU. 11 - Boot from an I2C EEPROM attached to the I2C interface. EEPROMs of 2 to 64 KB are supported. The entire system can be initialized in a custom fashion by the boot commands contained in the EEPROM. This mode can be used for standalone or host-assisted boot mode when the other internal boot scripts are not meeting the specific requirements of the application. In this mode the boot script is in the EEPROM to define and understand the EEPROM content.

The default state of the BOOT_MODE[3:0] pins are determined by the internal pull-ups and pull-downs present in the I/Os of PNX1702. The BOOT_MODE[7:4] pins must be pulled up or down at board level to ensure proper boot operation.

3.4 Video Encoder

Philips* SAA7104H component is used as the video output circuit on the IXP435 reference platform.

The SAA7104H is an advanced next-generation video encoder that converts PC graphics data at a maximum 1280 X 1024 resolution (optionally 1920 X 1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

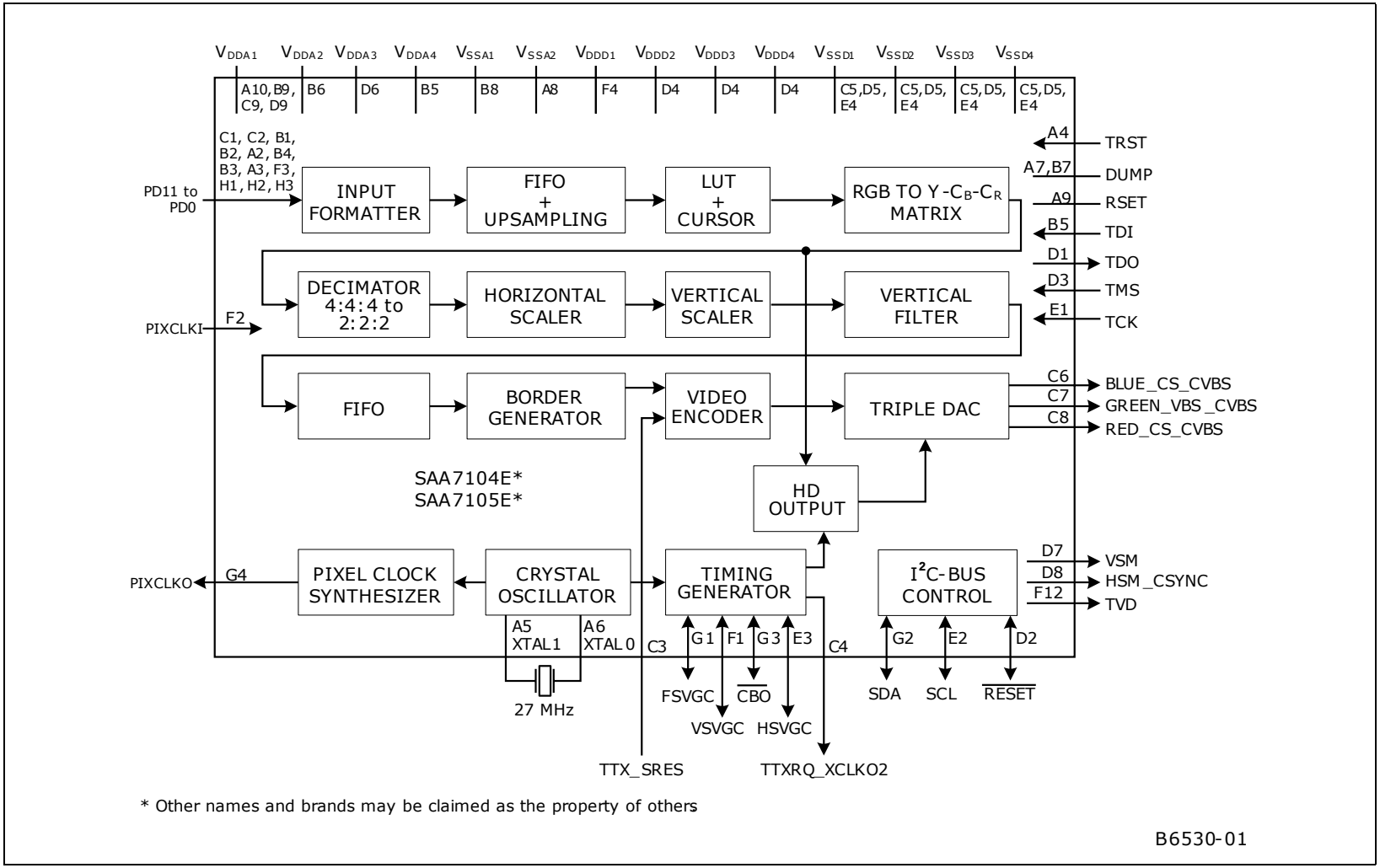
Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs also, thus serving as an auxiliary monitor at maximum 1280*1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively, this port can provide Y, PB, and PR signals for HDTV monitors.

The device includes a sync/clock generator and on-chip DACs.

All inputs intended to interface with the host graphics controller are designed for low-voltage signals between down to 1.1 V and up to 3.6 V. The high-level view of the Video Encoder SAA7104E is shown in Figure 7.

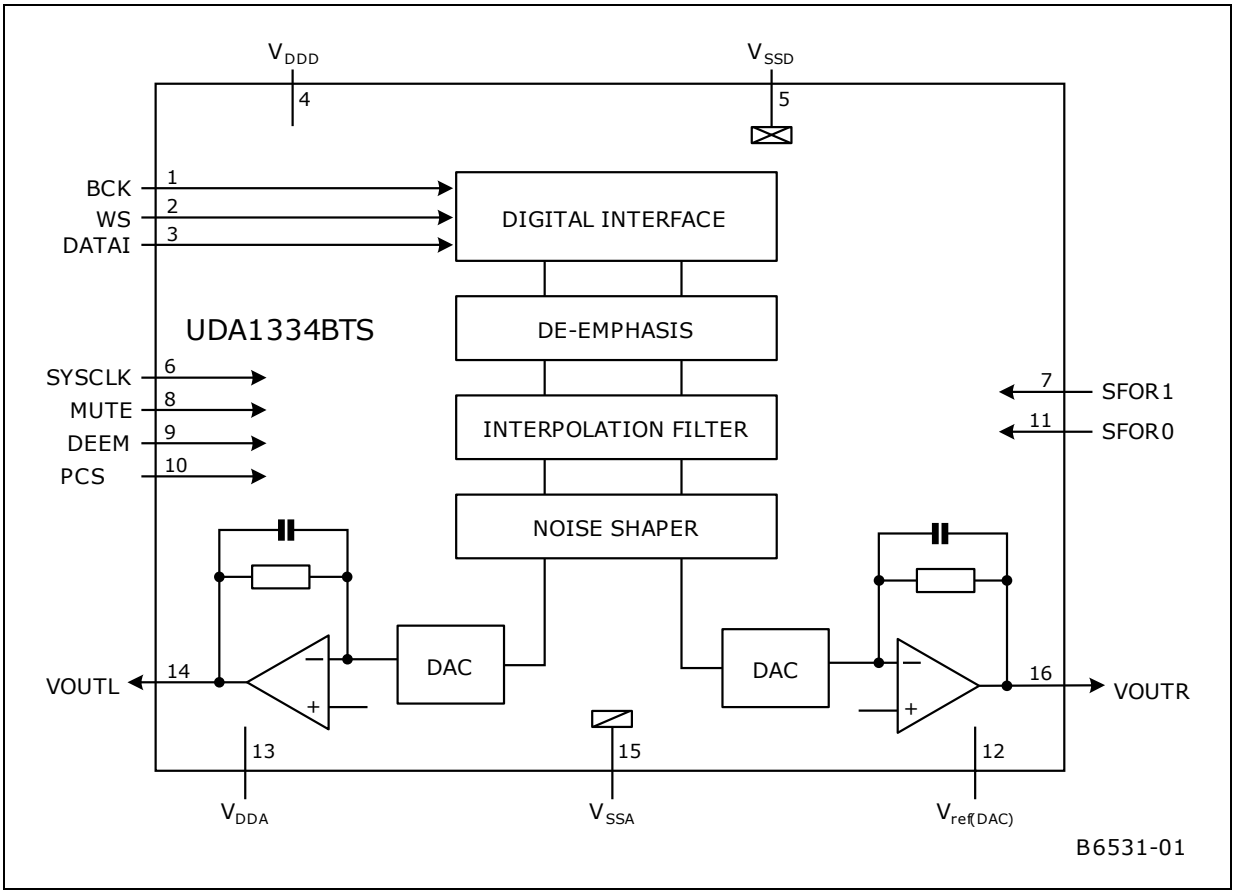
Figure 7. Video Encoder Functional Block Diagram



3.5 Audio DAC

Philips* UDA1334BTS component is used as the audio output circuit. The UDA1334BTS supports the I²S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits. The UDA1334BTS has basic features such as de-emphasis at 44.1 KHz sampling rate and mute. The high-level view of the UDA1334BTS Audio DAC is shown in Figure 8.

Figure 8. Audio DAC Block Diagram



3.6 Expansion Bus Loading

The IXP435 reference platform is tuned to drive up to 4 loads, yet the devices on the expansion bus may not be able to quickly drive such a large load. To compensate for this, the timings on the expansion bus are adjusted using network processor internal registers. If an edge rises slowly due to low drive strength, the IXP43X network processors must wait an extra cycle before the value is read. There are no buffers to increase drive strength on the expansion bus, although customers can choose to add buffers in their own designs.

3.6.1 Expansion Bus Configuration Straps

The expansion bus address lines (EX_ADDR23 - EX_ADDR0) are used for configuration strapping options during boot-up. At the de-assertion of reset, the values on these lines are read to determine the board configuration. The default configuration strapping is shown in Table 9.

Only address bits EX_ADDR[23:21] are connected to the DIP switch. The strapping options are connected through pull-down resistors. If the line is not pulled down, the weak pull-up internal to the IXP43X network processors will pull the line high.

Table 9. Configuration Strapping Options

EX_ADDR Bit	Name	Description
23-21	Clock Setting	See Table 10 for details.
20-17	Customer	Customer-defined bits
16-12	Reserved	Reserved
11	DDR_Mode	DDRI or DDRII mode selection: 0 - DDRII mode (400 MHz) (Default) 1 - DDRI mode (266 MHz)
10	IOWAIT_CS0	1 = EX_IOWAIT_N is sampled during the read/write Expansion bus cycles. (Default) 0 = EX_IOWAIT_N is ignored for read and write cycles to Chip select 0 if EXP_TIMING_CS0 is configured to Intel mode. Typically, IOWAIT_CS0 must be pulled down to Vss when attaching a Synchronous Intel StrataFlash® on Chip select 0. If EXP_TIMING_CS0 is reconfigured to Intel Synchronous mode during boot-up, the Expansion bus controller only ignores EX_IOWAIT_N during write cycles.
9	EXP_MEM_DRIVE	See the values defined for Bit 5, EXP_DRIVE
8	USB CLOCK	Controls the USB clock select 1 = USB Host clock is generated internally (Default) 0 = USB Host clock 48 MHz is generated from GPIO[1]
7	Reserved	Reserved
6	Reserved	Reserved
5	EXP_DRIVE	Expansion bus low/medium/high drive strength. The drive strength depends on the configuration of EXP_DRIVE and EXP_MEM_DRIVE (Bit 9) 00 = Reserved 01 = Medium drive 10 = Low drive (Default) 11 = High drive
4	Reserved	Reserved
3	Reserved	Reserved
2	PCI_ARB	Enables the PCI Controller arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled (Default)
1	PCI_ HOST	Configures the PCI Controller as PCI bus host 0 = PCI as non-host 1 = PCI as host (Default)
0	8/16	Specifies the data bus width of the Flash memory device found on Chip Select 0. 0 = 16-bit data bus (Default) 1 = 8-bit data bus

Table 10. Configuration Strapping Clock Settings (JP3) (Sheet 1 of 2)

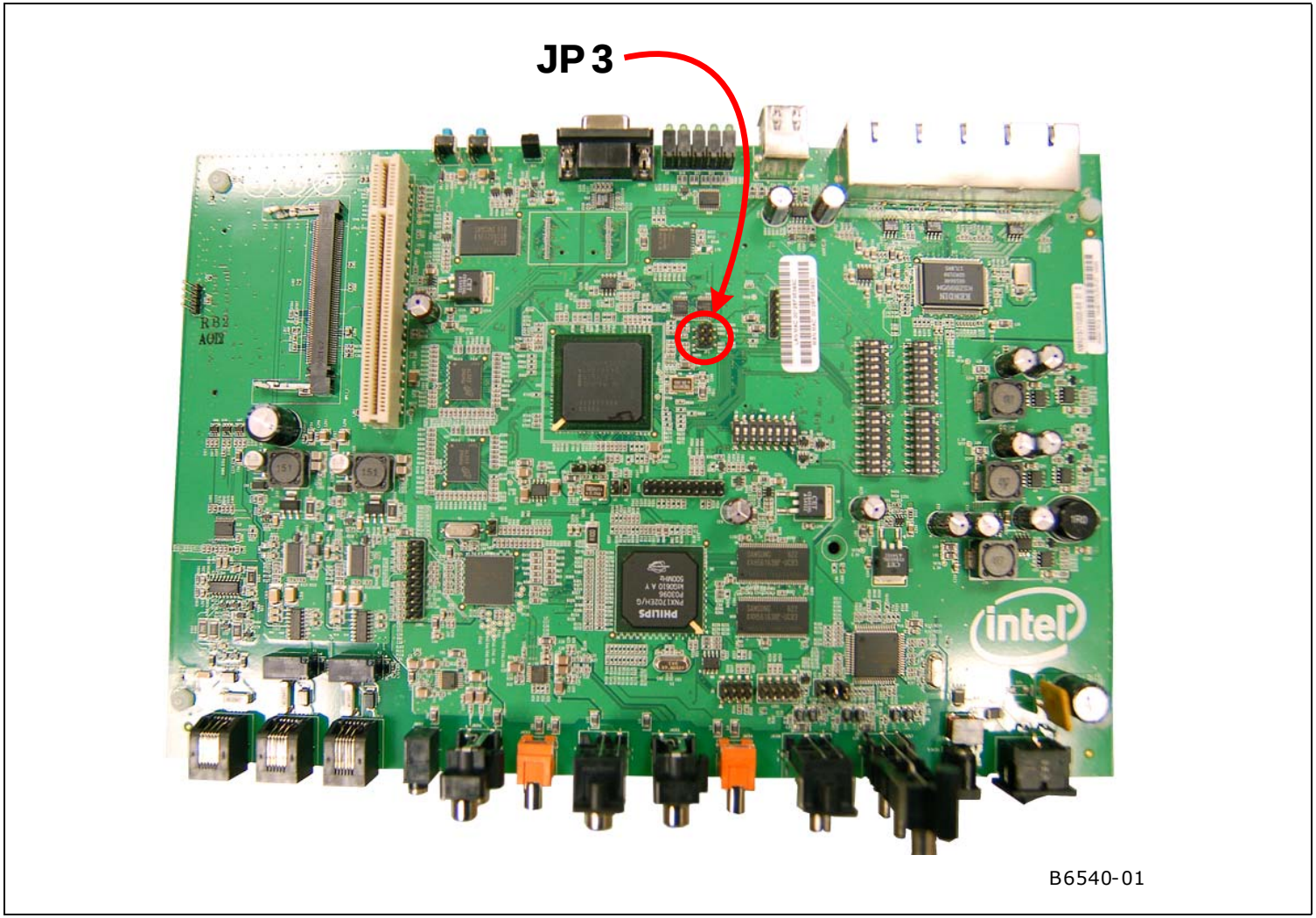
Speed (Factory Part Speed)	EX_ADDR(23)	EX_ADDR(22)	EX_ADDR(21)	Actual Core Speed
667 MHz	1	X	X	667 MHz
667 MHz	0	0	0	667 MHz
667 MHz	0	0	1	533 MHz
667 MHz	0	1	0	266 MHz

Table 10. Configuration Strapping Clock Settings (JP3) (Sheet 2 of 2)

Speed (Factory Part Speed)	EX_ADDR(23)	EX_ADDR(22)	EX_ADDR(21)	Actual Core Speed
667 MHz	0	1	1	400 MHz
533 MHz	1	X	X	533 MHz
533 MHz	0	0	0	533 MHz
533 MHz	0	0	1	533 MHz
533 MHz	0	1	0	266 MHz
533 MHz	0	1	1	400 MHz
400 MHz	1	X	X	400 MHz
400 MHz	0	0	0	400 MHz
400 MHz	0	0	1	400 MHz
400 MHz	0	1	0	266 MHz
400 MHz	0	1	1	400 MHz
266 MHz	X	X	X	266 MHz

Figure 9 shows the location and default settings of all Expansion Bus Address Strap Switches.

Figure 9. JP3 - Switch Location



3.6.2 Expansion Bus Clock Generation

The expansion bus clock is generated from a GPIO 15, and its frequency is software-selectable by writing to the GPIO Clock Register.

3.6.3 Expansion Bus Chip Selects

The IXP435 reference platform supports up to 4 devices on the expansion bus. The expansion bus chip selects listed in Table 11 are assigned to allow for support of the Intel® IXDP465 Development Platform mezzanine cards (that is, legacy support). Also, the connectors used are identical in size and pinout as those used on the Intel® IXDP465 Development Platform. A second connector on each mezzanine card allows for expansion of the expansion data bus to 32 bits and future expansion.

3.7 Memory Subsystem

Table 11. Expansion Bus Chip Select Assignments

Chip Select	Device Assignment
CS0	P30 NOR Flash
CS1	UTOPIA-2 and MII connector
CS2	LED circuit
CS3	For test only

The IXP435 reference platform has 128 Mbytes DDRII memory, 16 Mbytes NOR Flash memory, and 64 Mbytes NAND Flash memory.

3.7.1 BootROM

You can install either an Intel StrataFlash® Embedded Memory (P30) or PC28F128J3D memory on the IXP435 reference platform.

The flash is connected to the expansion bus of the IXP43X network processors. The IXP435 reference platform supports 8 Mbytes to 16 Mbytes of flash and ships with 16 Mbytes.

The FLASH_STS pin on the flash is unused. It is pulled up through a 4.7 KΩ resistor since it is an open drain output.

A 0.1 µF ceramic capacitor is connected between each of the three V_{CC} pins of the device and the ground. In addition, a 4.7 µF electrolytic capacitor is placed between **VCC** and GND at the array's power supply connection.

3.7.2 NAND Flash

The IXP435 reference platform has integrated 64 MB NAND type Flash memory for storing persistent image and data larger than 16M bytes. The R/B pin should be pulled high. GPIO12 is used as the chip select for the NAND Flash. The NAND Flash is connected on the expansion bus, EX_D[7:0]. Expansion bus addresses 0 and 1 are assigned for the ALE (address latch enable) and CLE (command latch enable) function accordingly.

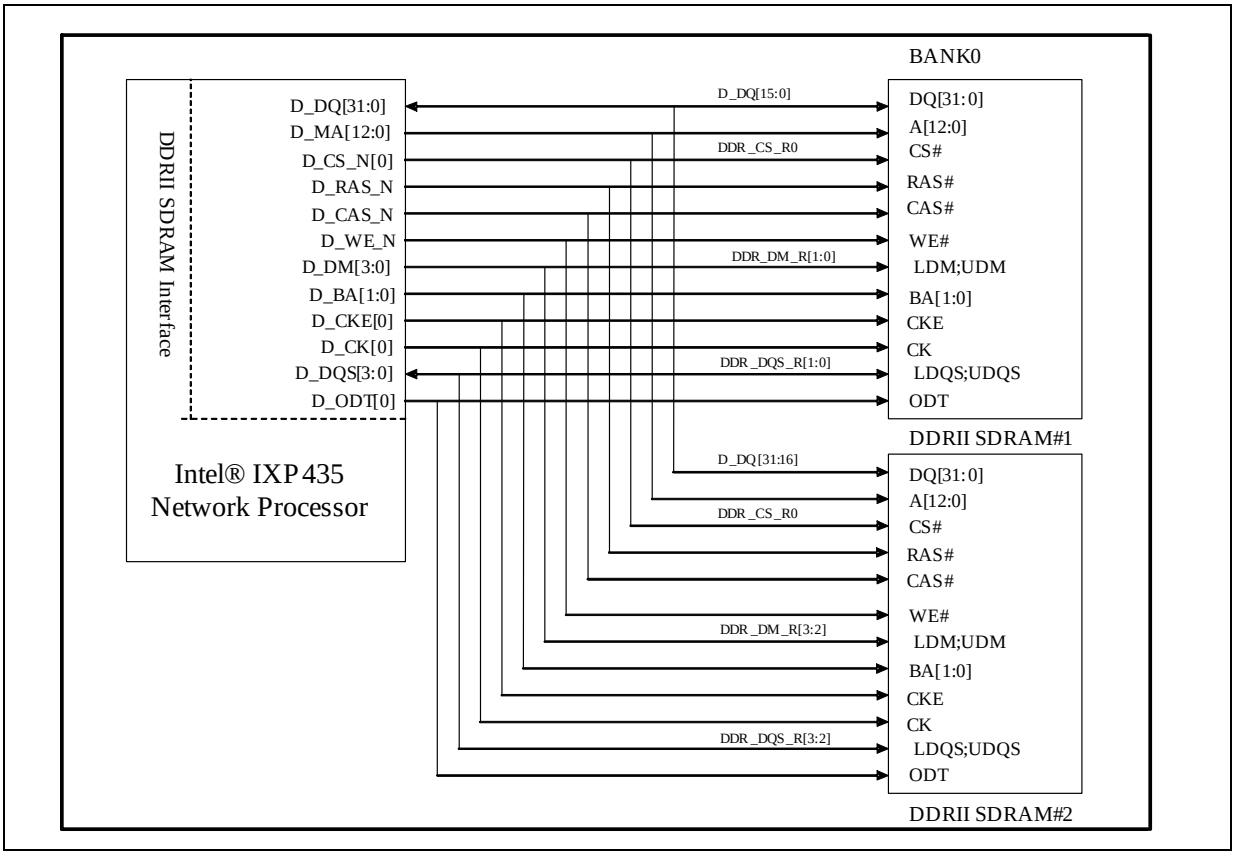
3.7.3 DDRII Memory

The memory controller of the IXP43X network processors support 128/256/512-Mbit, 1-Gbit DDR SDRAM and 256/512-Mbit DDRII SDRAM technologies. The total memory size supported are 32 Mbytes to 1 Gbytes for 32-bit DDR SDRAM, and 64 MBytes to 512 MBytes for DDRII SDRAM. The IXP435 reference platform is populated with 128 MB DDRII 400 MHz memory (Two MT47H32M16CC-5E, 32M x 16bit). The DDRII implementation on the IXP435 reference platform is solder-on board.

Table 12. Supported DDRII Memory Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	32M * 8	1	13	10	ADDR[27]	ADDR[26]	128 MB	4 KB
		2					256 MB	4 KB
	16M * 16	1	13	9	ADDR[26]	ADDR[25]	64 MB	2 KB
		2					128 MB	2 KB
512 Mbit	64M * 8	1	14	10	ADDR[28]	ADDR[27]	256 MB	4 KB
		2					512 MB	4 KB
	32M * 16	1	13	10	ADDR[27]	ADDR[26]	128 MB	4 KB
		2					256 MB	4 KB

Figure 10. DDRII Memory Topology



3.8 MII Interface

The IXP435 reference platform supports four 10/100 Mbps Ethernet LAN ports and one 10/100Mbps WAN port. Both the LAN and WAN ports are supported by the Kendin* KS8995M 10/100Mbps Ethernet switch through the two MII buses that connect to the IXP43X network processors. See Table 13 for the WAN port switch setting. The auto-MDI/MDIX feature must be available for all LAN ports. This interface uses a 5-gang RJ-45 connector with integrated magnetics.

The Kendin KS8995M component is used in the IXP435 reference platform *design. The KS8995M contains five physical-layer transceivers and five MAC units with an integrated Layer-2 switch. The Port 5 of KS8995M is configured to a single PHY mode. See Table 13 for the WAN port switch settings.

Figure 11. NPE Function Connections

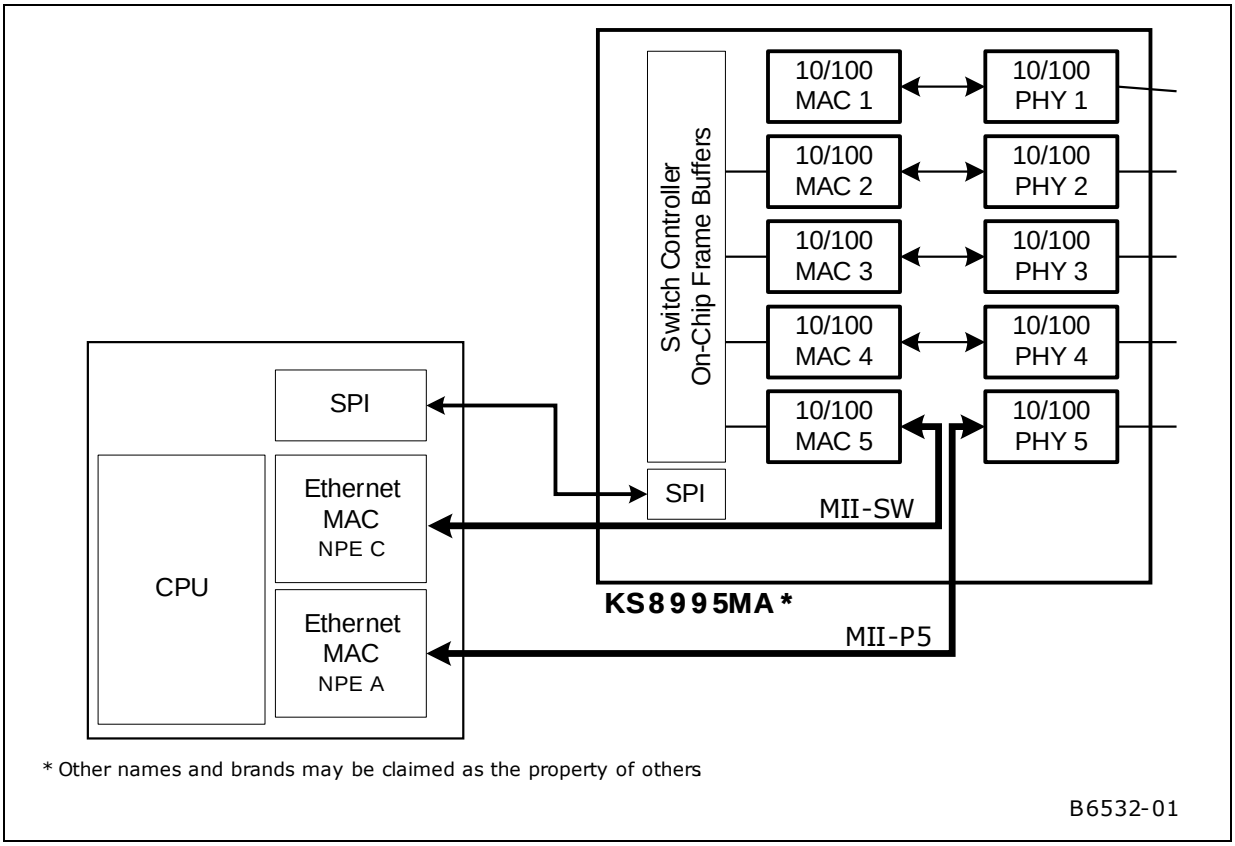


Figure 12. NPE-A/UTOPIA/MII Pin Switches Topology

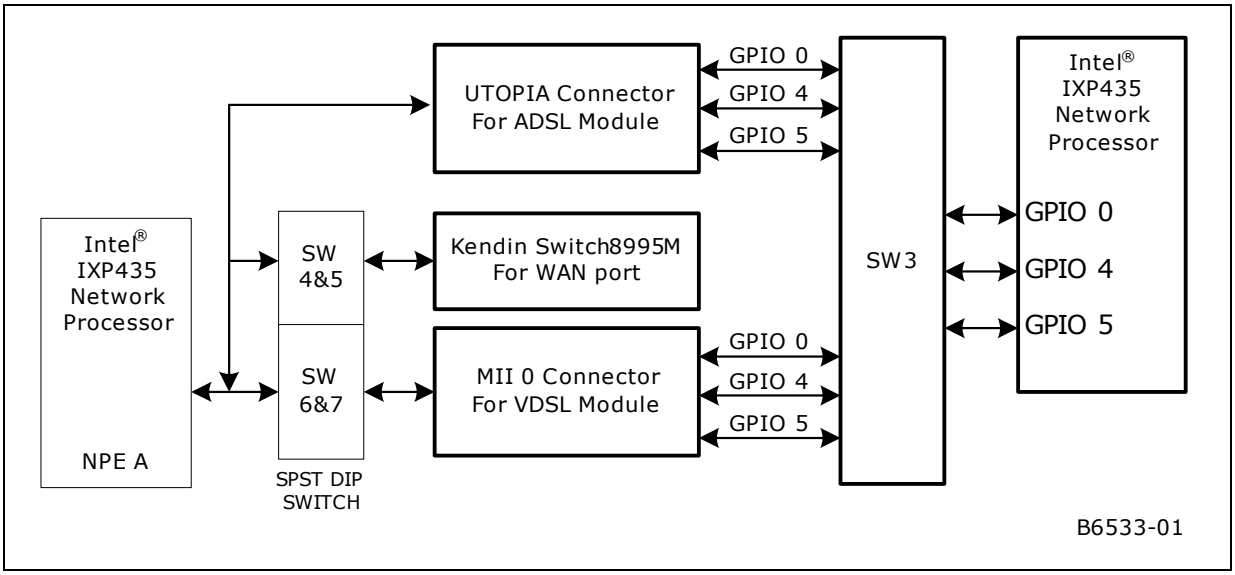
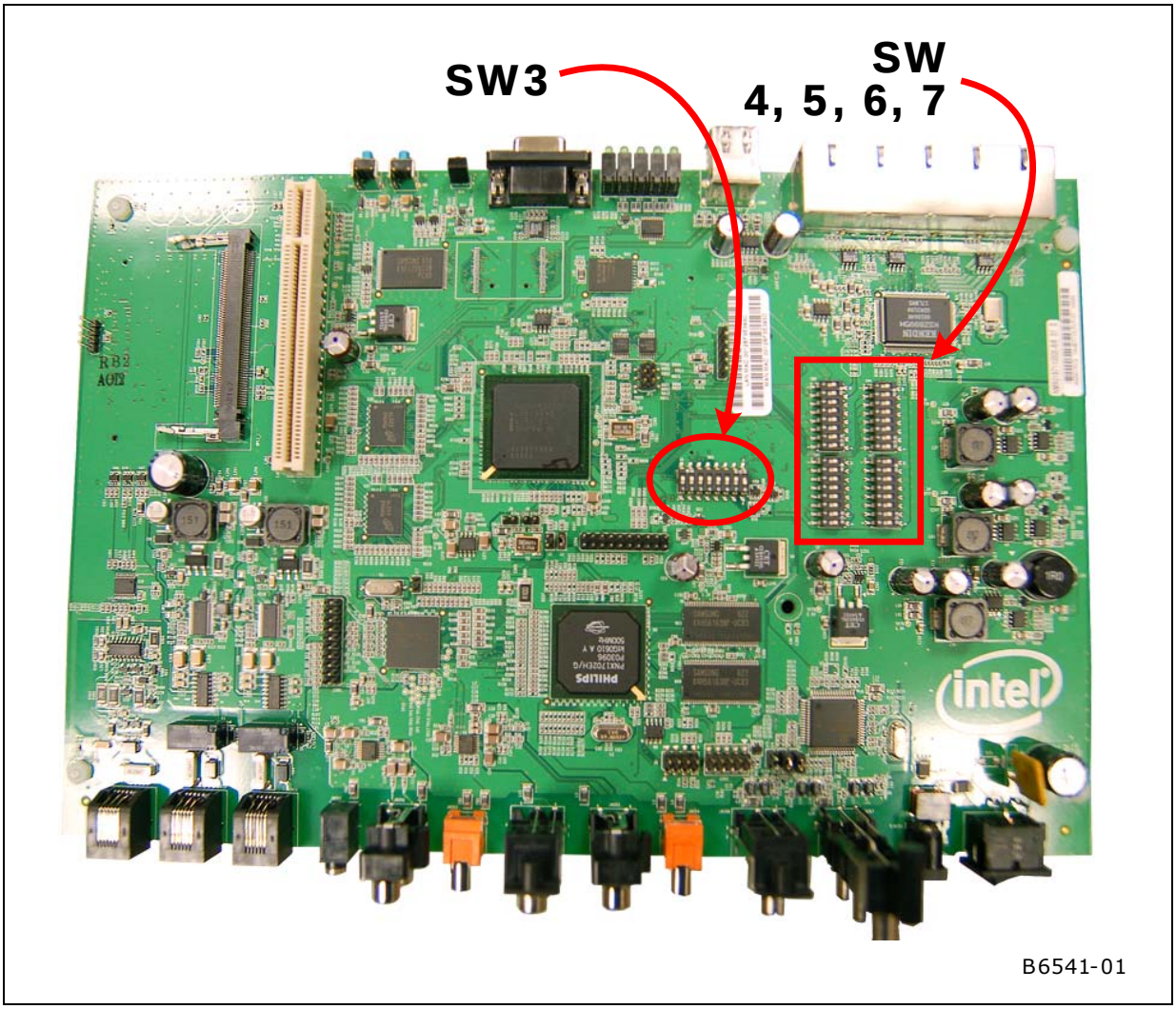


Table 13. WAN Port Multi-function Switch Settings

Function	SW 4	SW 5	SW 6	SW 7	SW 3 (for GPIO 0, 4, 5)
Ethernet switch (Kendin 8995M) WAN port	All ON	Pin 3 OFF, others ON	All OFF	All OFF	Pin 1, 2, 3 ON Pin 4, 5, 6 OFF Pin 7 ON Pin 8 OFF
MII Connector (for Intel LXT972 LAN module)	All OFF	All OFF	Pin3 OFF Others ON	All ON	Pin 1, 2, 3 ON Pin 4, 5, 6 OFF Pin 7 ON Pin 8 OFF
UTOPIA Connector (for ADSL module)	All OFF	Pin3 ON Others OFF	Pin3 ON Others OFF	All OFF	Pin 1, 2, 3 ON Pin 4, 5, 6 OFF Pin 7 ON Pin 8 OFF

Figure 13. UTOPIA/MII Pin Switches Location



Enabling of HSS and Ethernet coprocessors in NPE-A may have a performance impact to the Ethernet throughput; thus the LAN and the WAN port are connected to NPE-C and NPE-A respectively.

In addition to the Ethernet WAN port, one WAN MII mezzanine interface (that is, NPE-A) is available for connectivity to the other transport module. Hardware dip switch is used to disable the WAN connection to the KS8995M Ethernet switch. Table 14 shows the pin definition of the WAN MII mezzanine interface; this interface is compatible with the MII mezzanine interfaces on the Intel® IXDP465 Development Platform baseboard.

Note: The MII and UTOPIA signal pins are shared; the hardware dip switch should be configured to select the proper signal set. The MII signal, Expansion Bus signals and three GPIO pins (GPIO 0, 4 & 5) are routed to the MII mezzanine connector.

Table 14. Intel® IXP435 Multi-Service Residential Gateway Reference Platform MII Mezzanine Connector Pin Definition (Sheet 1 of 2)

Signal	Pin #		Signal	Pin #		Signal	Pin #
-	1		EX_ADDR11	41		5.0V	81
-	2		EX_ADDR10	42		3.3V	82
-	3		EX_ADDR13	43		TEST	83
-	4		EX_ADDR12	44		VDSL_RST_N1 (GPIO 4 of the IXP43X network processors)	84
EX_DATA1	5		EX_ADDR15	45		GND	85
EX_DATA0	6		EX_ADDR14	46		GND	86
EX_DATA3	7		GND	47		-	87
EX_DATA2	8		GND	48		VDSL_RLS (GPIO 5 of the IXP43X network processors)	88
MII0_GPIO0	9		EX_ADDR17	49		-	89
MII0_GPIO1	10		EX_ADDR16	50		RST_N	90
EX_DATA5	11		EX_ADDR19	51		-	91
EX_DATA4	12		EX_ADDR18	52		ETHB_TXEN	92
EX_DATA7	13		EX_ADDR21	53		-	93
EX_DATA6	14		EX_ADDR20	54		ETHB_RXDV	94
GND	15		EX_ADDR23	55		GND	95
GND	16		EX_ADDR22	56		ETHB_RXCLK	96
EX_DATA9	17		GND	57		ETHB_RXDATA3	97
EX_DATA8	18		GND	58		GND	98
EX_DATA11	19		EX_CLK_MII0	59		ETHB_RXDATA2	99
EX_DATA10	20		EX_RD_N	60		ETHB_TXCLK	100
-	21		GND	61		ETHB_RXDATA1	101
-	22		EX_WR_N	62		ETHB_COL	102
EX_DATA13	23		EX_ALE	63		ETHB_RXDATA0	103
EX_DATA12	24		EX_RDY_N0	64		ETHB_TXDATA3	104
EX_DATA15	25		EX_IOWAIT_N	65		GND	105
EX_DATA14	26		ETHB_INT_N(GPIO 0)	66		ETHB_TXDATA2	106
GND	27		EX_CS_N4	67		ETH_MDC	107
GND	28		3.3V	68		GND	108
EX_ADDR1	29		-	69		ETH_MDIO	109
EX_ADDR0	30		3.3V	70		ETHB_TXDATA1	110
EX_ADDR3	31		5.0V	71		ETHB_CRS	111
EX_ADDR2	32		3.3V	72		ETHB_TXDATA0	112
EX_ADDR5	33		5.0V	73		12V	113
EX_ADDR4	34		3.3V	74		2.5V	114
EX_ADDR7	35		5.0V	75		12V	115
EX_ADDR6	36		3.3V	76		2.5V	116

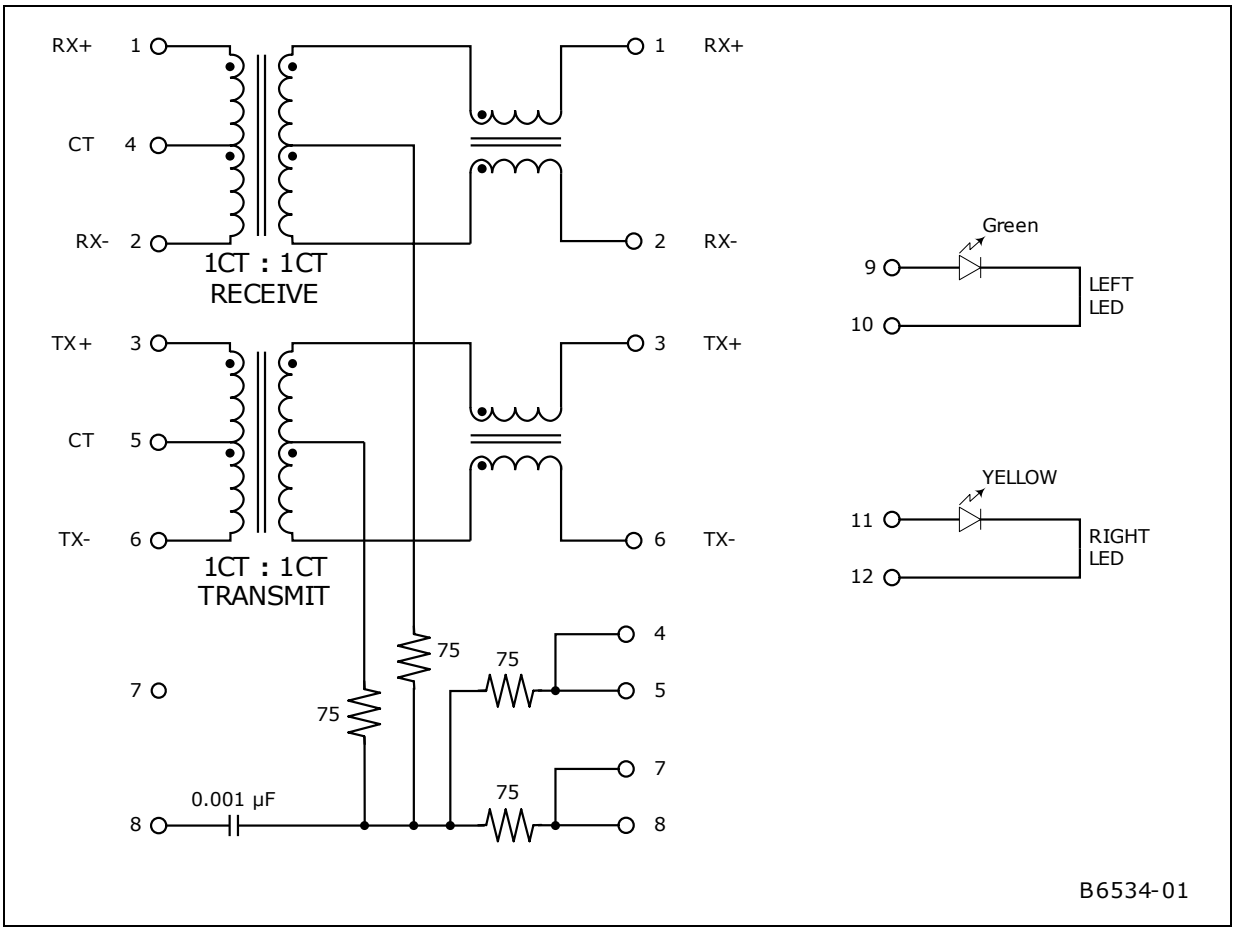
Table 14. Intel® IXP435 Multi-Service Residential Gateway Reference Platform MII Mezzanine Connector Pin Definition (Sheet 2 of 2)

Signal	Pin #		Signal	Pin #		Signal	Pin #
GND	37		5.0V	77		12V	117
GND	38		3.3V	78		2.5V	118
EX_ADDR9	39		5.0V	79		12V	119
EX_ADDR8	40		3.3V	80		2.5V	120

3.8.1 Multi-Gang Jack

The IXP435 reference platform contains a 5-port RJ-45 gang jack with integrated magnetics. Each port has two LEDs (one green, one yellow) controlled by the PHY. The software programs the PHY (through the MII interface) to illuminate the LEDs according to certain events such as activity, half-full duplex, 10/100 MHz and so on. Figure 14 shows the integrated magnetics within the gang jack.

Figure 14. RJ-45 Jack with Integrated Magnetics



3.9 UTOPIA-2 Interface

The IXP435 reference platform supports UTOPIA level 2 interface through a 2x60-pin mezzanine card connector (Amp 5-179010-5). The pins of the UTOPIA-2 interface are multiplexed with MII interface (NPE A). The UTOPIA level 2 and Expansion Bus signals are routed to this connector to allow a variety of DSL PHY modules to be configured, including PHY modules from the Intel® IXDP465 Development Platform. See Table 15 for the connector pin definitions.

Note: All the IXP43X product line of network processors engine (NPE) functions require Intel-supplied software. For information about using this software, see the *Intel® IXP400 Software Programmer's Guide*. For information about the availability of this enabling software, contact your Intel sales representative.

Table 15. Utopia Mezzanine Connector Pin Definition (Sheet 1 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
1	+12VD	Power	2	+12VD	Power
3	DGND	Ground	4	DGND	Ground
5	UTP_INT_N(GPIO 0)	O	6	EXPB_A0	I
7	DGND	Ground	8	EXPB_A2	I
9	EXPB_A1	I	10	DGND	Ground
11	EXPB_A3	I	12	EXPB_A4	I
13	DGND	Ground	14	EXPB_A6	I
15	EXPB_A5	I	16	EXPB_A8	I
17	EXPB_A7	I	18	DGND	Ground
19	EXPB_A9	I	20	EXPB_CLK	I
21	DGND	Ground	22	DGND	Ground
23	EXPB_D0	I/O	24	EXPB_D2	I/O
25	EXPB_D1	I/O	26	EXPB_D4	I/O
27	ADSL_RST_N(GPIO 4)		28	ADSL_GPIO1 (GPIO 5)	
29	EXPB_D3	I/O	30	EXPB_D6	I/O
31	EXPB_D5	I/O	32	EXPB_D7	I/O
33	DGND	Ground	34	DGND	Ground
35	EXPB_WR_N	I	36	EXPB_RD_N	I
37	RESERVED		38	RESERVED	
39	RST_N	I	40	UTP_CS_N	I
41	DGND	Ground	42	DGND	Ground
43	EXPB_ALE	I	44	+3.3 VD	Power
45	TDI	I	46	+3.3 VD	Power
47	TDO	O	48	+3.3 VD	Power
49	DGND	Ground	50	DGND	Ground
51	+3.3 VD	Power	52	+3.3 VD	Power
53	TCK	I	54	TMS	I
55	+2.5 VD	Power	56	+2.5 VD	Power
57	DGND	Ground	58	DGND	Ground
59	EXPB_A21	I	60	EXPB_A22	I

Table 15. Utopia Mezzanine Connector Pin Definition (Sheet 2 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
61	DGND	Ground	62	DGND	Ground
63	+3.3 VD	Power	64	DSL_IOWAIT_N	O
65	+3.3 VD	Power	66	DGND	Ground
67	DGND	Ground	68	EXPB_A23	I
69	UTP_RX_CLK	I	70	DGND	Ground
71	DGND	Ground	72	UTP_TX_CLK	I
73	UTP_RXD1	O	74	DGND	Ground
75	RESERVED		76	UTP_TXD2	I
77	UTP_RXD0	O	78	UTP_TX_EN	I
79	UTP_RXD2	O	80	DGND	Ground
81	UTP_RX_CLAV	O	82	UTP_TXD0	I
83	DGND	Ground	84	UTP_TXD1	I
85	UTP_TXD7	I	86	UTP_TXD3	I
87	UTP_TXD4	I	88	UTP_TXD5	I
89	UTP_TXD6	I	90	DGND	Ground
91	DGND	Ground	92	UTP_TX_CLAV	O
93	UTP_RXD7	O	94	UTP_TX_SOC	I
95	UTP_RXD3	O	96	DGND	Ground
97	UTP_RXD5	O	98	UTP_RXD4	O
99	UTP_RX_SOC	O	100	UTP_RXD6	O
101	UTP_RX_EN	I	102	RESERVED	
103	DGND	Ground	104	DGND	Ground
105	UTP_RXA4	I/O	106	UPT_TXA4	I/O
107	UTP_RXA3	I/O	108	UTP_TXA3	I/O
109	DGND	Ground	110	UTP_TXA2	I/O
111	UTP_RXA2	I/O	112	DGND	Ground
113	UTP_RXA1	I/O	114	UTP_TXA1	I/O
115	UTP_RXA0	I/O	116	UTP_TXA0	I/O
117	RESERVED		118	RESERVED	
119	5 VD	Power	120	5 VD	Power

3.10 USB 2.0

Two Type-A USB "host" receptacles are provided at the board edge; the USB host interface is compliant with USB2.0. The interface is capable of operation at 1.5 Mbits/s, 12 Mbits/s and 480 Mbits/s.

3.11 Serial Port

One asynchronous serial I/O port (UART) with flow control is provided. The port is routed to 9-pin DB connectors with RTS and CTS flow control. The system supports baud rates of 115200.

The port is wired according to the RS-232 specification for data communication equipment. Straight serial cable connects to the host PC. Table 16 shows the pin definitions for the serial port DB-9 connector.

Table 16. Serial Port DB-9 Connector Pin Definitions

UART	Signal
1	UART0_DCD_B_L
2	UART0_TXD_B_L
3	UART0_RXD_B_L
4	UART0_DTR_B_L
5	UART0_GND_B_L
6	UART0_DSR_B_L
7	UART0_CTS_B_L
8	UART0_RTS_B_L
9	UART0_RI_B_L

3.11.1 Serial Port Pull-Ups/Pull-Downs

The Receive signal lines are pulled down through a 5KΩ resistor on the RS-232 side within the transceiver. Since data signals are inverted, the IXP43X network processors might see a pull-up on these lines. An unpopulated pull-up shall be placed on the IXP43X network processors side receive signals to allow additional signal conditioning in case the internal pull-down is not strong enough. A 10KΩ resistor strength is suggested in the *Intel® IXP43X Product Line of Network Processors Datasheet* for these pull-ups. Table 17 shows the serial port resistor signal and values.

Table 17. Serial Port Resistors

Signal	Pull to Value	Resistor Value
URT_CTS0_N	+3.3 V	10 KΩ
URT_RXD0	GND	10 KΩ
URT_CTS1_N	+3.3 V	10 KΩ
URT_RXD1	GND	10 KΩ

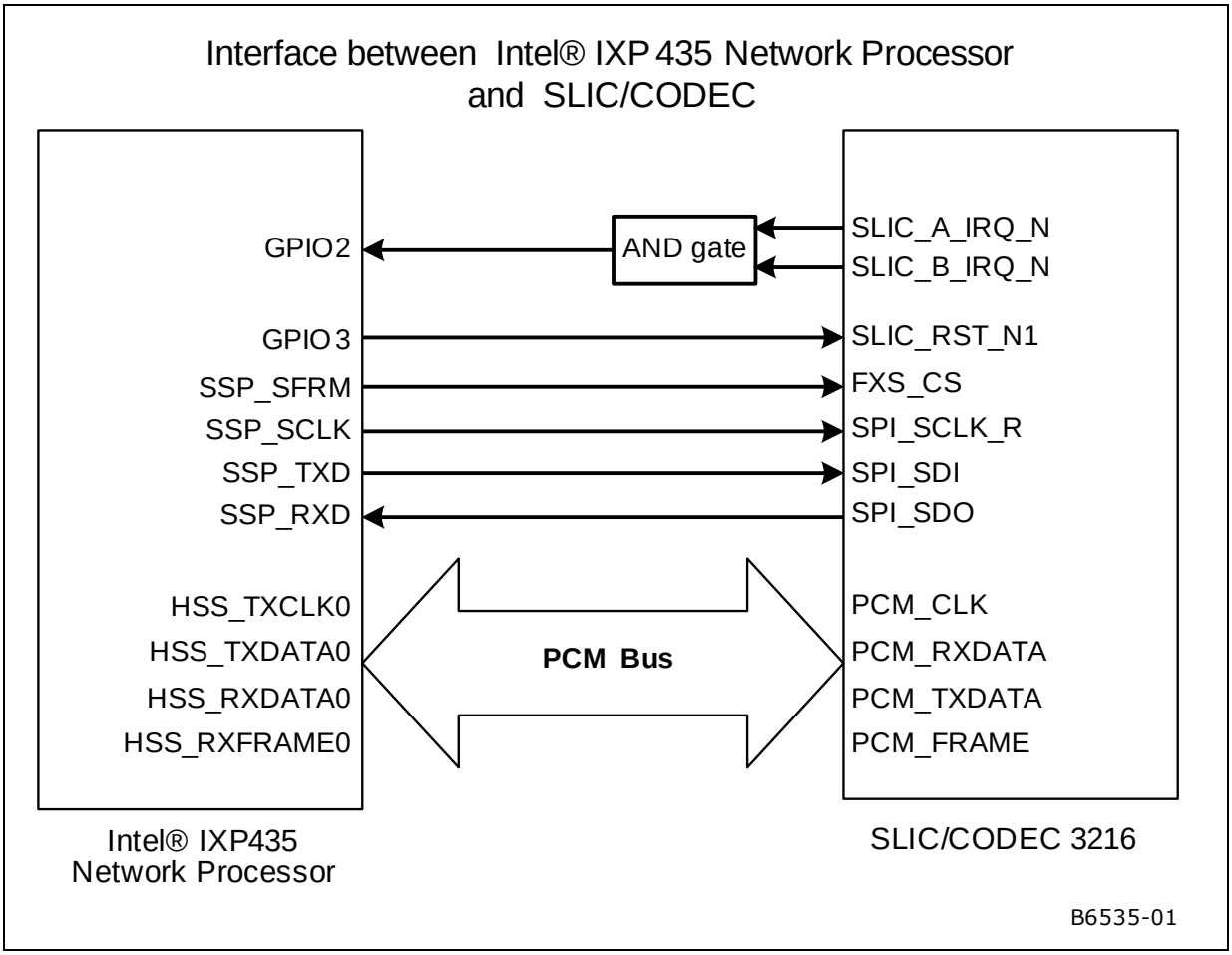
3.12 FXS and FXO Functions

3.12.1 FXS Ports

The IXP435 reference platform has integrated two Si3216 wideband SLIC codecs from Silicon Laboratories to support two FXS ports in the VoIP applications. The Si3216 is a dual mode wideband (50 Hz – 7 KHz)/narrowband (200 Hz – 3.4 KHz) codec with 16-bit 16 KHz sampling. Both the Si3216 SLIC/Codecs are connected to the HSS port of the IXP43X network processors; the SPI control interface of SLICs are also driven by the SPI port of the IXP43X network processors. Two GPIOs are used for SLICs interrupts.

The Si3216 chips are used as the linefeed interface, and two RJ11 ports are provided for connection to the telephone.

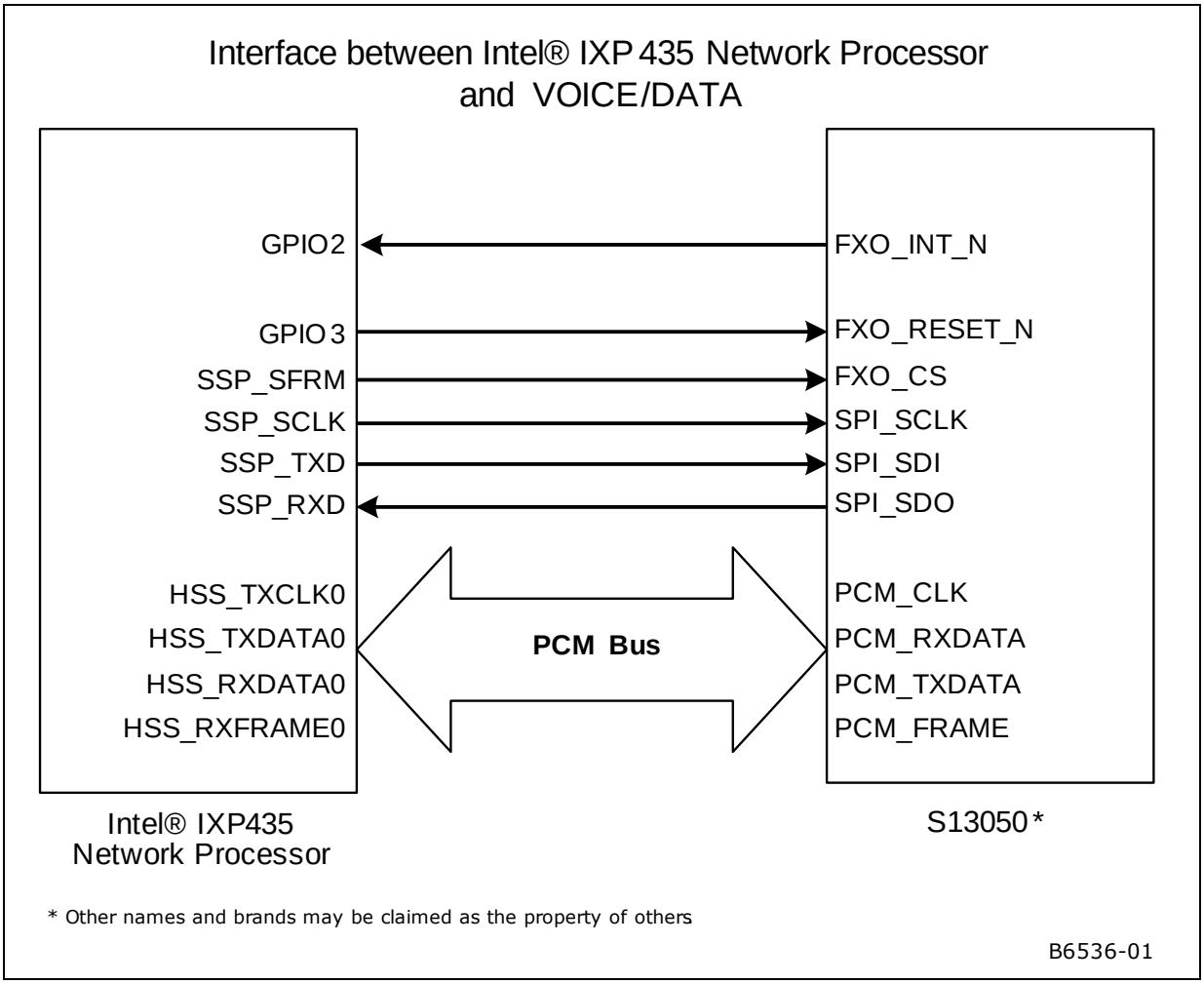
Figure 15. Intel® IXP43X Product Line of Network Processors and SLIC/CODEC Topology



3.12.2 FXO Port and Failover Port

The FXO port of the IXP435 reference platform is designed with Si3050 from Silicon Laboratories for compliance with the regulations set by the major Telcos. The failover relay will route the FXS ports to the telephone line in the power failure condition.

Figure 16. Intel® IXP43X Product Line of Network Processors and Voice/DAA Topology



The FXS and FXO circuit has an external PCM Clock source that is implemented on 2.048 MHz Oscillator circuit (20ppm). The jumpers J8 and J9 are used to select the required PCM Clock source, internal PCM Clock source or external PCM Clock source. The default value is set for internal PCM Clock source, which comes from the HSS interface of the IXP43X network processors. The default value for J8 and J9 are opened.

The FXO reset signal is controlled in the same way as FXS reset signal that originates from GPIO 3. The FXO interrupt signal is controlled in the same way as the FXS interrupt signal that originates from GPIO 2.

The Ethernet switches, FXS and FXO are shared with one SPI bus of the IXP43X network processors; two Demultiplexers and two GPIOs (GPIO6 and GPIO7) are used to do these control. Refer to Table 18 for setting these values.

Table 18. Ethernet/FXS and FXO Control

Description	SSP_CS0 (GPIO 6)	SSP_CS1 (GPIO 7)
Ethernet switch	1	X
FXS select	0	0
FXO select	0	1

Warning: Do not connect the FXS, FXO, and Failover to the PSTN. These ports must be connected in the laboratory environment only.

3.13 GPIO

The GPIOs are mapped to many purposes on the IXP435 reference platform. The GPIO signals are used as interrupt and clock source to some peripherals. The default state for GPIO 14 and 15 are user-programmable output with the default state being a 33 MHz output. The clocks are supplied to the Expansion bus clock (GPIO 14) and PCI clock (GPIO 15) respectively. Refer to Table 19 for GPIO assignment.

Note: Because of hardware limitations, some GPIOs are shared with the mezzanine card for NPE-A. These shared signals involve installing 0Ω resistors that do not come factory installed. For further information, refer the baseboard schematics for exact resistor installation options that support different NPE-A related platform configurations.

Table 19. Intel® IXP43X Product Line of Network Processors GPIO Assignment

GPIO Pin	Intel® IXP4XX Product Line of Network Processors Net Name	Description
GPIO0	DSL_INT_N	VDSL Interrupt (MII connector used) or ADSL Interrupt (UTOPIA connector used)
GPIO1	REMOTE_IR/SW_KEY_N	IR remote receive data / SW_KEY reset
GPIO2	SLIC_IRQ_N	Interrupt for FXS and FXO
GPIO3	SLIC_RST_N	FXS Reset and FXO Reset
GPIO4	VDSL_RST/ADSL_RST_N	VDSL Reset / ADSL SW Reset
GPIO5	VDSL_RLS/ADSL_GPIO1	VDSL Release / ADSL Test
GPIO6	SSP_CS0	SPI Chip Select for DMUX (VOIP and Switch)
GPIO7	SSP_CS1	SPI Chip Select for DMUX (FXS and FXO)
GPIO8	PCI3_IRQ_N	PCI Slot IRQ
GPIO9	PCI2_IRQ_N	Mini-PCI IRQ
GPIO10	PCI1_IRQ_N	Mini-PCI IRQ (WiFi used)
GPIO11	DSP_IRQ_N	For Media Processor PNX1702 (PCI interface)
GPIO12	NAND_CS_N	NAND Flash chip select
GPIO13	IO_RESET_N	All of peripheral Reset
GPIO14	PCI_CLK	PCI Clock
GPIO15	EXP_CLK	Expansion Bus Clock

3.14 LED Indicators

Expansion bus and latch circuit are used for LED indicators function. Refer to Table 20 for LED indicator.

Table 20. LED Indicators

LED	LED Indication when on	LED part number	Color
Reset	System is in reset	D9-1	Green
Power LED	+12V powered up	D9-2	Green
Wireless LAN (Mini-PCI_1)	activity / Link-active	D10-1	Green / Blinking Green
Wireless LAN (Mini-PCI_2)	activity / Link-active	D10-2	Green / Blinking Green
PCI Slot	activity / Link-active	D11-1	Green / Blinking Green
USB port 1	activity / Link-active	D11-2	Green / Blinking Green
USB port 2	activity / Link-active	D12-1	Green / Blinking Green
VoIP port 1	activity / Link-active	D12-2	Green / Blinking Green
VoIP port 2	activity / Link-active	D13-1	Green / Blinking Green
FXO port 1	activity / Link-active	D13-2	Green / Blinking Green

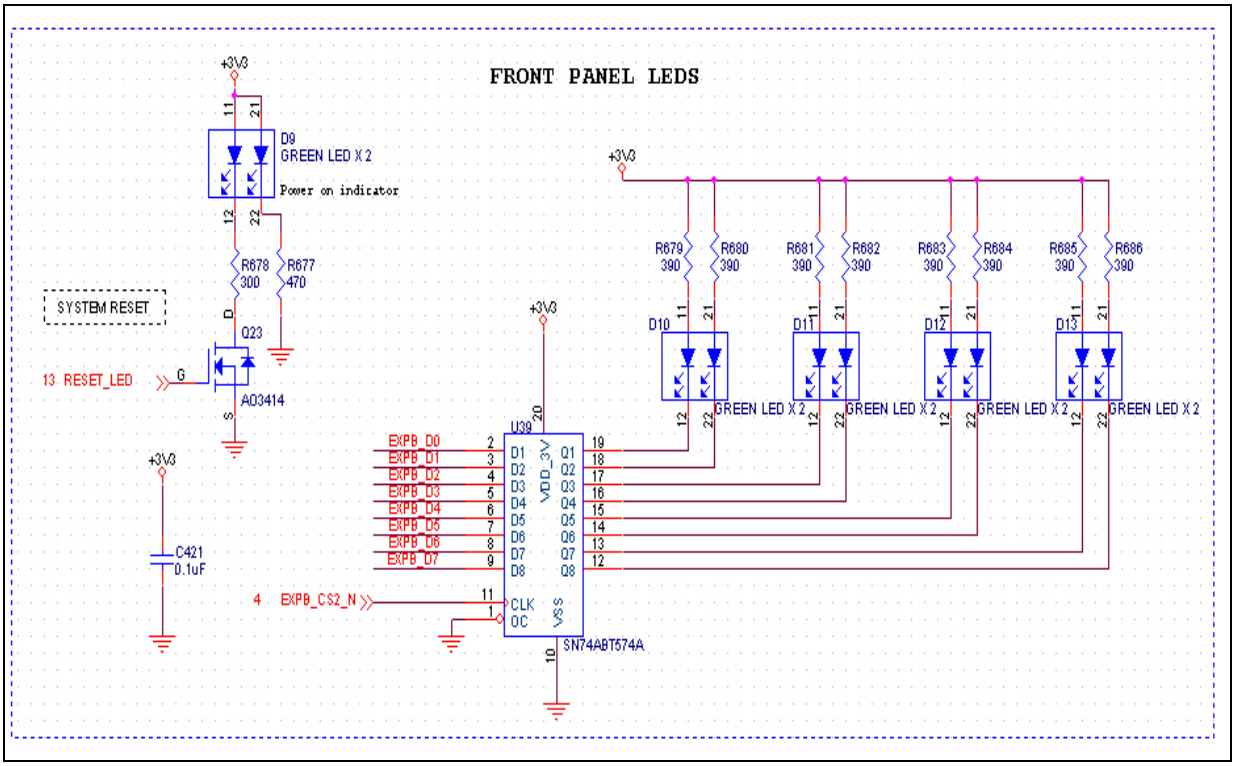
Table 21 provides indication for the RJ45 Jack.

Green: Link/activity, Yellow: 10/100 Mbps; illuminates when connected to a 100-Mbps network.

Table 21. Ethernet LED Indicators

LEDs of RJ45 Jack	LED Indication when on	Color
5 Ethernet LEDs	Traffic status: Link/activity	Green
5 Ethernet LEDs	Traffic status: 10/100 Mbps	Yellow

Figure 17. Expansion Bus and LED Circuit Topology



3.15 Debug Circuitry

An Intel® 10/100 EthernetPro Adapter card using the Intel® 82559 Ethernet PHY component can be plugged into a PCI slot and used as the debug Ethernet port.

3.16 visionICE* / Raven* Emulator Interface

The Intel® IXP43X Product Line of Network Processors can be controlled during debug through a JTAG interface to the processor. The Macraigor* Raven* and Wind River Systems visionPROBE*/ visionICE* systems can plug into the JTAG interface through a 20-pin connector (CON4).

The main difference between the Raven and visionICE systems is the specific implementation of nTRST for each debugger. The Macraigor Raven implementation actively drives nTRST (high and low). The Wind River Systems visionPROBE / visionICE can configure nTRST active or open collector (only drive low). The application note, Recommended JTAG Circuitry for Debug with Intel XScale® Microarchitecture (Doc. Number: 273538-001) located at http://www.intel.com/design/iio/applnots/273538.htm.

The Macraigor Raven and Wind River Systems visionPROBE / visionICE systems will plug into the JTAG interface through a 20-pin connector defined in Table 22.

Table 22. JTAG Connectors

Pin #	Pin Name	Connect To	Pin #	Pin Name		Connect To
1	VTREF	3 V3	2	VSUPPLY	+3V3	
3	TRST_N	10KΩ pull-up for ICE debug used, 10KΩ pull-down for normal operation - TRST also generated from reset circuit whenever system reset asserted and from Corelis* test equipment	4	GND	GND	
5	TDI	10KΩ pull-up	6	GND	GND	
7	TMS	10KΩ pull-up	8	GND	GND	
9	TCK	10KΩ pull-up	10	GND	GND	
11	RTCK	GND	12	GND	GND	
13	TDO	10KΩ pull-up	14	GND	GND	
15	SRST_N	Reset circuitry (/BDMR)	16	GND	GND	
17	DBGRQ		18	GND	GND	
19	DGBACK		20	GND	GND	

Note: The J2 must be ON for ICE mode and J3 must be ON for normal mode.

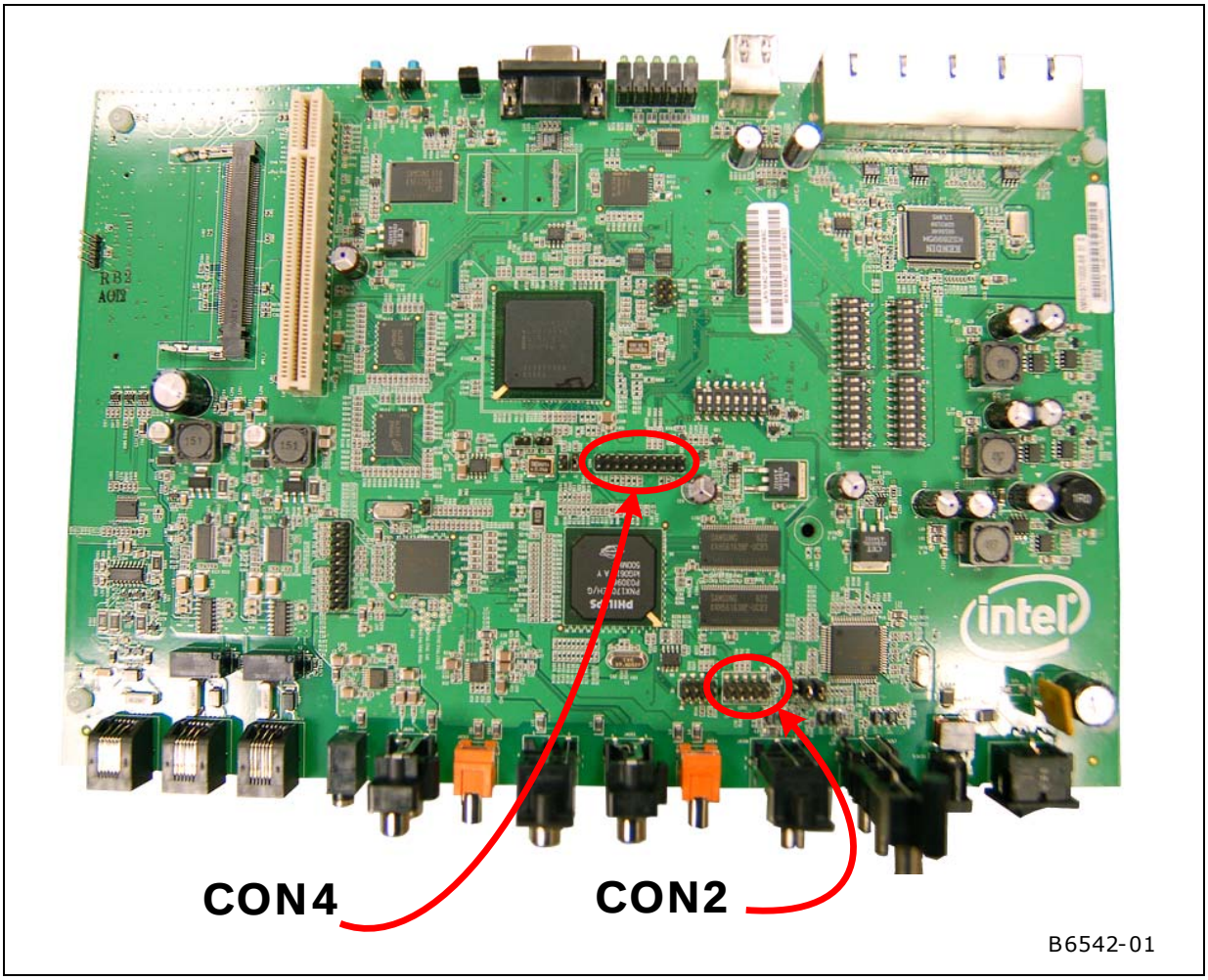
3.17 Additional JTAG Connectors

As debug/development tools for Media Processor, JTAG connectors (CON2) are provided as shown in Table 23.

Table 23. Additional JTAG Connectors

Pin #	Pin Name	Connect To	Pin #	Pin Name		Connect To
1	DBG_RST_N	10KΩ pull-up	2	GND	GND	
3	TDI	10KΩ pull-up, option for 10KΩ pull-down (DNP)	4	GND	GND	
5	TDO	10KΩ pull-up	6	GND	GND	
7	TMS	10KΩ pull-up	8	GND	GND	
9	TCK	10KΩ pull-up, option for 10KΩ pull-down (DNP)	10	GND	GND	

Figure 18. JTAG Interface Locations



3.18 Power

Power rails are generated on the IXP435 reference platform. The following voltages are provided: 12V, 3.3V, 1.3V, 1.4V, 1.8V, 0.9V, 2.6V, 5V and GND. The power sequences are mentioned below:

(1) 12V-> 3.3V-> 1.8V ->0.9V->1.3V (IXP43X network processors)

(2) 12V->3.3V->1.4VDSP->2.6V

(3)12V->5V

The 3.3-V I/O voltage (VCCP) and the 1.8-V I/O voltage (VCCM) are powered up at least 1 µs before the core voltage (VCC). The core voltage (VCC) of the IXP43X network processors must not become stable prior to 3.3-V I/O voltage (VCCP) or the 1.8-V I/O voltage (VCCM). Sequencing between VCCP and VCCM can occur in any order with respect to one another:

- VCCP prior to VCCM
- VCCM prior to VCCP

- VCCP simultaneously to VCCM

The VUSBAUPLL, VUSBCORE, VCCA (1.3V) follow the VCC voltage power up pattern. The VCCP_OSC, Vccpusb and Vccaubg voltage (3.3V) follows the VCCP voltage power-up pattern.

The value for TPOWER_UP should be at least 1 µs after the later of VCCP and VCCM reaches stable power.

The TPOWER_UP timing parameter is measured between the later of the I/O power rails (VCCP at 3.3 V or VCCM at 1.8 V) and VCC at 1.3 V.

The USB ports of IXP43X network processors have a special requirement on power up sequence if USB_V5ref is connected to a 5V power supply. The USB_V5ref ports to be powered up are:

- USB_V5ref prior to VCCP
- If USB_V5ref is powered up simultaneously to VCCP, Voltage level at pin USB_V5ref must be equal to or higher than VCCP

No special power sequence is required for the Media Processor PNX1702. To enable MM_CKE remain low at power up, it is required to have the 1.3VDSP come up before the 2.5V. This is a JEDEC DDR specification requirement.

The total maximum power based on worst case estimates is +12V/3.5A though it is unlikely that this much power will actually be used. The external power adapter should supply 12Vdc/3.5A on the IXP435 reference platform.

A power on/off switch may be implemented for the flexibility to turn on/off the input power supply.

The input power to the platform is +12Vdc, 3.5A nominal.

There are eight power regulators on board. The power consumption estimation and power circuit topology for the IXP435 reference platform is shown in Figure 19 and Table 24.

- Regulator 1: RT9214, +12Vdc input, +3.3Vdc output
- Regulator 2: RT9214, +12Vdc input, +5Vdc output (USB)
- Regulator 3: RT9194, +12Vdc input, +3.3V control for output +1.8Vdc (DDRII)
- Regulator 4: RT9173, +1.8Vdc input, +0.9V output. (DDRII VTT)
- Regulator 5: RT9167, +3.3Vdc input, +1.8V output (Kendin switch)
- Regulator 6: RT9214, +12Vdc input,+ 1.8V(DDRII) control for output +1.3Vdc (IXP43X network processors)
- Regulator 7: RT9194, +12Vdc input, +3.3V control for output +1.4Vdc (DSP)
- Regulator 8: RT9194, +12Vdc input, +1.3V control for output +2.6Vdc (DDR)

Figure 19. Power Circuit Topology

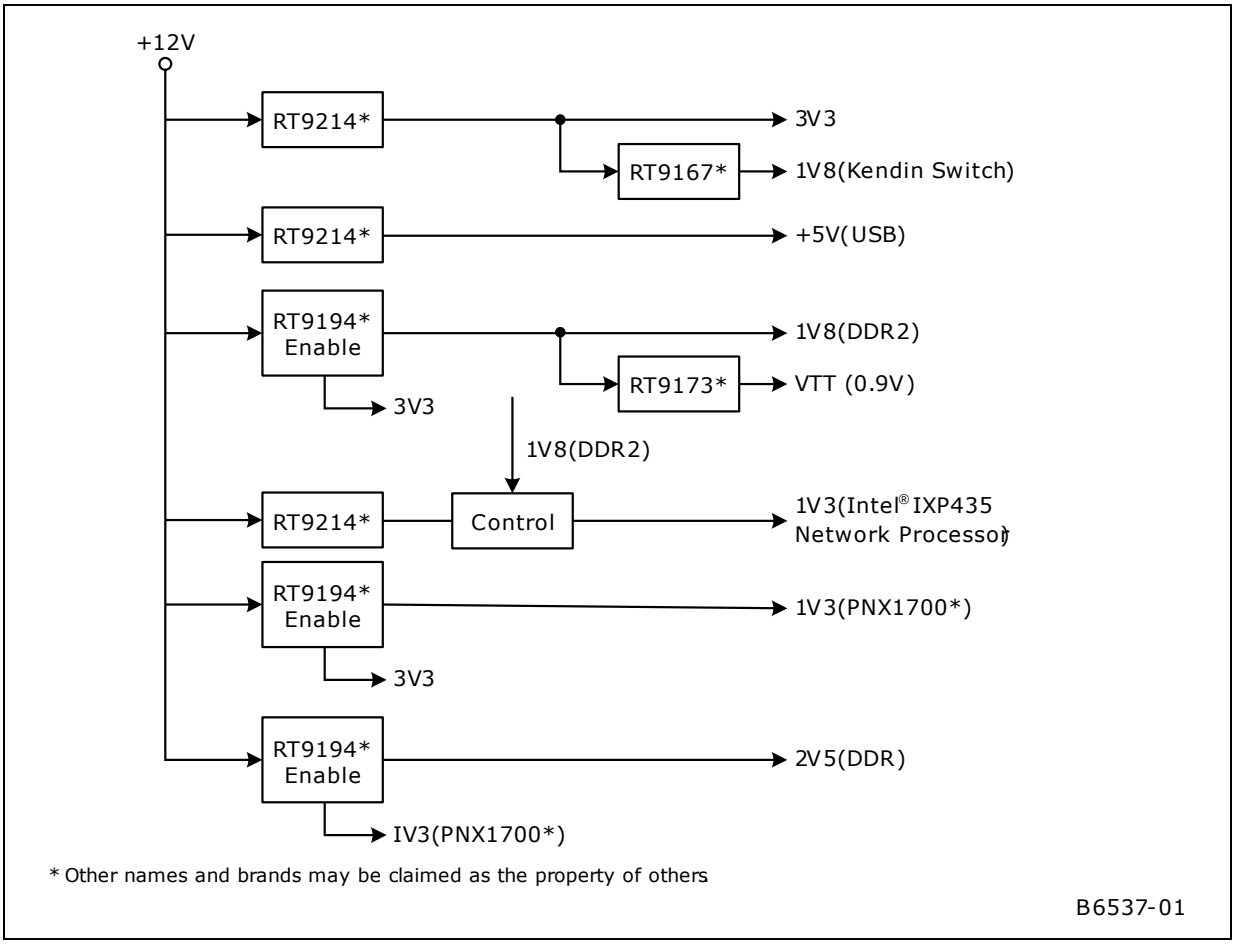


Table 24. Power Consumption Estimation (Sheet 1 of 2)

	Intel® IXP435 Multi-Service Residential Gateway Reference Platform, power consumption estimation--standby mode				
Legend	**Device Name**	**Device Part #**	**Volts**	**Current (in milliamps)**	**Power (mW)**
(mA)	Power				
(mW)					
A	CPU	IXP43X network processors-667 MHz (core)	1.3	610	793
	Memory-Subsystem	IXP43X network processors-667 MHz (I/O)	3.3	327	1079
		MT47H32M16CC-5E*2			
		Flash 28F128J3A			
B	Ethernet Switch	KSZ8995M	2.5	100	250
C	Misc. Logic	Clock Buffer, LED, Logic, …	3.3	50	165

Table 24. Power Consumption Estimation (Sheet 2 of 2)

	Intel® IXP435 Multi-Service Residential Gateway Reference Platform, power consumption estimation--standby mode				
Legend	**Device Name**	**Device Part #**	**Volts**	**Current (in milliamps)**	**Power (mW)**
D	ProSLIC CODEC(FXS)	Si3216+Si3201	3.3	47	155
E	DC/DC (RING)	Si3216	12	0	0
F	Media system	PNX1702	3.3	400	1240
		DDR	2.5		
		Video and Audio In/Out	3.3		
G	FXO	SI3050	3.3	40	132
?	Total				3814

3.19 Reset Logic

The IXP435 reference platform implements the following reset scenarios:

1. Power switch (Power on reset Key): This logic will reset all internal logic of the IXP43X network processors to a known state after the PLL has achieved a locked state. The Power on the reset signal is 1.3V.
2. HW Push button reset (Hardware reset Key): This logic will reset the IXP43X network processors and all the peripheral devices on board.
3. SW Push button reset (Software reset Key): This reset logic will output the reset signal to the GPIO 1 of the IXP43X network processors. The IXP43X network processors will reload and configure some parameters.
4. JTAG reset (from JTAG connector of the IXP43X network processors for any debug probe like EPI* MAJIC probe): This reset logic will reset the IXP43X network processors and all the peripheral devices on board.
5. IO reset (GPIO 13): This will reset all the peripheral devices. This is implemented through GPIO 13 on the IXP43X network processors. Software is able to control this reset logic.

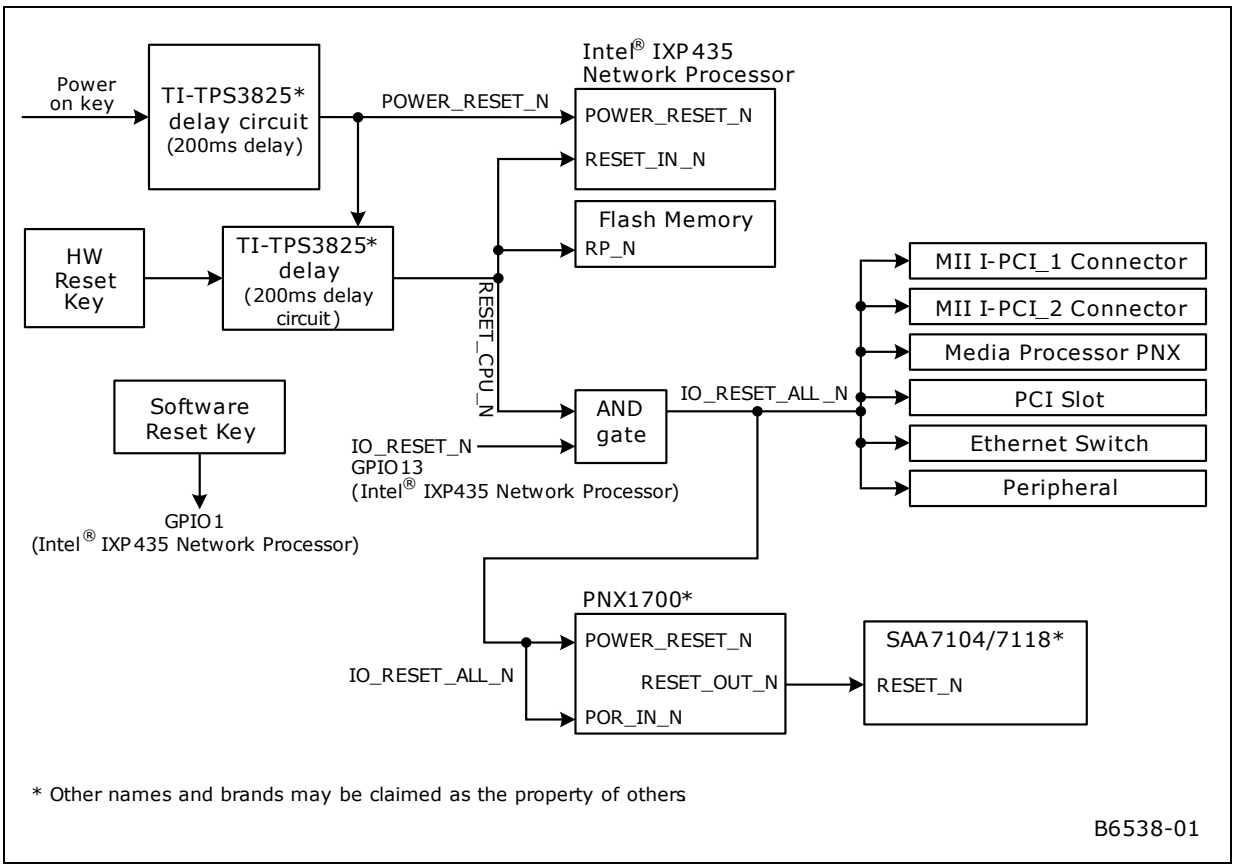
Note: The SW Push button reset (Software reset key) output is shared with IR_Remote_receive signal to output the reset signal to GPIO 1 of the IXP43X network processors.

Following are the reset sequencing requirements for the IXP435 reference platform:

1. VCC and VCC33 power supplies must reach steady state
2. Hold PWRON_RST_N and RESET_IN_N asserted for 2000 ns
3. De-assert PWRON_RST_N (signal goes high with the help of a pull-up resistor)
4. Continue to hold RESET_IN_N asserted for at least 10nSec more after releasing PWRON_RST_N
5. De-assert RESET_IN_N (signal goes high with the help of a pull-up resistor)
6. The network processor asserts PLL_LOCK indicating that the processor has successfully come out of Reset.

Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for further information.

Figure 20. Reset Circuit Topology



3.20 Clocking

The IXP435 reference platform implements the following clock schemes:

1. 33 MHz oscillator is used to provide 33 MHz clock input to the IXP43X network processors
2. GPIO14 is used to generate the 33 MHz PCI clock. A clock buffer is used to distribute this PCI clock to all the PCI devices
3. GPIO15 is used to generate the Expansion bus clock
4. 25 MHz crystal is used to provide the input clock for the Ethernet Switch Kendin 8995M.
5. 27 MHz crystal is used to provide the input clock for the Media Processor, Philips* PNX1702.
6. 27 MHz crystal is used to provide the input clock for the video encoder, Philips* SAA7104.
7. 24.576 MHz crystal is used to provide the input clock for the video decoder, Philips* SAA7118
8. 2.048 MHz oscillator is used to provide to the HSS Clock of the IXP43X network processors (optional)

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4.0 Key Components of the Intel® IXP435 Multi-Service Residential Gateway Reference Platform

The Intel® IXP435 Multi-Service Residential Gateway Reference Platform is implemented with the following key components:

Table 25. Overview of the Key Components

Component	Description	Package	QTY	Manufacturer
Intel® IXP43X Product Line of Network Processors	Intel's network processor	460-Pin PBGA	1	Intel
MT47H32M16CC-5E	DDRII SDRAM (400MHz)	84-ball FBGA	2	Micron
K4H561638F-UC/LB3	DDR Memory	66 TSOP-II	2	Samsung*
KSZ8995M	5-Port 10/100 Managed Switch	128-Pin PQFP	1	Micrel
PC28F128J3D-75	NOR Flash Memory	64-Ball Easy BGA	1	Intel
PC28F128P30T85	NOR Flash Memory	64-Ball Easy BGA	1	Intel
K9F1208U0M-PCB0	NAND Flash	48-Pin TSOP	1	Samsung*
PNX1702EH/G(500MHz)	Media processor	BGA456	1	Philips*
SAA7104H	Video encoder	QFP64	1	Philips
SAA7118E	Video decoder	BGA156	1	Philips
UDA1334TS	Audio DAC	SSOP16	1	Philips
UDA1361TS	Audio ADC	SSOP16	1	Philips
Si3216-FT	SLIC/CODEC	TSSOP-38	2	Silicon Laboratories
Si3201-FS	Linefeed IF	SOIC-16	1	Silicon Laboratories
Si3050-FT	Voice/Data Direct Access Arrangement	TSSOP-20	1	Silicon Laboratories
Si3019-FS	Line Side	SOIC-16	1	Silicon Laboratories
RT9214PS	Power	SOP-8	3	Richtek
RT9194PE	Power	SOT-23-6	3	Richtek
RT9167A18PS	Power	SOP-8	1	Richtek
RT9173PS	Power	SOP-8	1	Richtek
CY2305SZ-1H	Clock buffer	SOIC-8	2	Cypress
TPS3825-33DBVR	Processor supervisory circuit	SOT23-5	2	Ti*

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5.0 Mechanical and PCB Stack Up

The Intel® IXP435 Multi-Service Residential Gateway Reference Platform Printed Circuit Board (PCB) is 12"x8". The PCB board uses a 6-layer (3 signals, 2 grounds and 1 power) FR4 PCB construction. The PCB stack up is listed in Table 26.

Table 26. PCB Stack Up

Layer	Description
1	Top - Signal_1
2	GND_1
3	Signal_2
4	GND_2
5	PWR_1
6	Bottom -Signal_2

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6.0 Regulatory Guidelines

The Intel® IXP435 Multi-Service Residential Gateway Reference Platform complies with the following regulatory conditions:

- EMI: FCC Part 15 and CISPR 22 (EN55022) for Class B
- PTT: USA FCC TIA-968-A Issue 8, Industry Canada CS-03, Japan JATE, EU TBR-21, Taiwan PSTN 01, Korea RLL, and China Telecom YD/T 514
- Immunity: CISPR 24 (EN55024)
- Safety: IEC 60950-1

This product contains encryption logic and must meet all applicable export regulations for sale outside the United States of America. The IXP435 reference platform complies with the requirements of the RoHS Directive.

6.1 Environmental Guidelines

The IXP435 reference platform complies with the environmental conditions defined in Table 27.

Table 27. Environmental Ranges

	Temperature Range	Humidity Range	As Measured From....
Operational	0 - 50ºC (Ambient temp. external to System containing product)	0% - 80% non-condensing	Measured from the component with maximum power consumption on the board (processor). Must be less than 70ºC with ambient of 50ºC. Ambient temperature must be maintained at 50ºC as measured at least 2 inches from the system under test.

6.2 Quality Requirements

The IXP435 reference platform meets the Quality and Reliability requirements defined by 25GS3000 and IQUAL for Product Type: "Boards", Product Sub-type: "Reference Design /Development Platform", Usage Segment: "Home Network".

Appendix A Updating the Intel® IXP435 Multi-Service Residential Gateway Reference Platform Flash Memory

RedBoot* is the primary bootloader and it is used to boot Linux*. RedBoot is also used to update RedBoot.

Note: The IXP435 reference platform is shipped with RedBoot v2.02 installed. It reports its version as follows:

```
RedBoot(tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.02 - built 15:43:18, Nov 23 2005
Platform: IXP435 reference platform(XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.
```

Once the IXP435 reference platform is running with your OS set up, you may want to organize the flash content for your particular design. Leaving the RedBoot image in place is recommended.

A host system connects through a network or serial port to provide the images. The procedures in this section assume that you have a host system set up to support loading images from a TFTP server. The Host system setup and installation are beyond the scope of this document. For detailed information on using the RedBoot* v2.02 software and host system requirements, refer to the Intel® IXP400 Software: RedBoot* v2.02 Software Release Notes.

This appendix provides the following procedures that are required to maintain the boot images in flash:

- Updating flash: Generic steps that apply to any bootloader or image to be placed into flash and made available at system Start Up to run.
- Creating a backup copy of RedBoot
- Using RedBoot to update RedBoot
- Using the VisionICE* to load RedBoot

These procedures cover typical scenarios for using the IXP435 reference platform.

Note: RedBoot commands entered at the RedBoot command prompt are prefaced with an ">" and appear in boldface type.

A.1 Generic Flash Updating Using RedBoot*

1. Place the image to be loaded in the tftp root directory. On Linux, this is /tftpboot
2. Switch off the power to the board
3. Connect the board to the network and serial console
4. Switch on the power to the board
5. Boot to the RedBoot prompt:
   Press ^C (Ctrl-C) if necessary to cancel the boot script execution.
   The default fconfig setting has no boot script
6. Use the fis list command to view the existing flash partitions and their content

If you are updating an existing image that is in the FIS partition list, then you must unlock the partition before you can update it, using the command **fis unlock <NAME>.**

If there was no previous image, then it is not possible to give NAME as an argument for the fis unlock command, so it is recommended to unlock it using the command
`fis unlock -f <FLASH-ADDRESS> -l <IMAGE LENGTH>`

When the update is complete, lock the partition using the command **fis lock <NAME>**.

7. Load the image into RAM using the RedBoot load command:

```
> load -r -v -b 0x01600000 image.bin
```

8. Check the output of the load command for the image length.
   RedBoot reports this address range: 0x00100000-0x00181234.
   The image length to store is `0x00181234` minus `0x00100000`.
   This value is used when storing the image to flash.
9. Use the `fis unlock` command to prevent the occurrence of an error report which states
   "Illegal command "Not a String" 0x25DB8"

   ```
   > fis unlock -f <FLASH-ADDRESS> -l <IMAGE_LENGTH>
   ```

10. Use the fis create command to store the image to flash.

    ```
    > fis create <IMAGE-NAME> -b 0x01600000 -l <IMAGE_LENGTH> -f <FLASH-ADDRESS> -e
    0x00000000
    ```

Note: The `fis create` command is entered on a single line:

<IMAGE-NAME>, <IMAGE-LENGTH>, and <FLASH_ADDRESS> are placeholders for arguments that are required by the fis create command.

- <IMAGE-NAME>: The name that identifies the image in flash. A corresponding load command can use this name
- <IMAGE-LENGTH>: The length in bytes of the image previously loaded into RAM. Use the length as determined in step 8.
- <IMAGE-ADDRESS>: The location in flash where the image will be written. Check the output of the fis list command to see the segments that have been programmed as available.

Note: Flash updates using JTAG tool EPI Majic*, BDI2000* and VisionICE* are supported. Contact your Intel sales representative for additional information.

A.2 Creating a Backup Copy of RedBoot

As a precaution before updating the primary RedBoot image, create a backup RedBoot image in flash. The backup version can be used in case there is a problem updating the primary RedBoot image and/or the new image fails to operate properly.

Follow the steps mentioned below to load an additional copy of RedBoot into flash:

1. Load the redboot_ROM.bin image into flash:
   > load -r -v -b 0x00160000 redboot_ROM.bin
   > fis create Redboot.bak -b 0x00100000 -l 0x0007A000 -f 0x51000000 -e 0x00000000

Note: The fis create command is entered on a single line.

2. Switch off the power to the board.
3. Verify that RedBoot boots. The following information is displayed:

   ```
   Trying NPE-C...success. Using NPE-C with PHY 1
   ```

```
Ethernet eth0: MAC address 00:07:e9:16:34:72
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254
Default server: 192.168.200.254

RedBoot (tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.02 - built 15:43:18, Nov 22 2006

Platform: IXP435 reference platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x0002a350-0x07fc1000] available
FLASH: 0x50000000 - 0x51000000, 128 blocks of 0x00020000 bytes each.
== Executing boot script in 3.000 seconds - enter ^C to abort
```

Once you have verified that the RedBoot image is functional, you can update the primary image.

A.3 Using RedBoot to Update RedBoot

Note: RedBoot must execute from RAM to program the image into flash, since the primary RedBoot image runs from flash.

Follow the steps mentioned below to update the primary image:

1. Load and execute redboot_RAM.srec:

```
> load -v redboot_RAM.srec
Using default protocol (TFTP)
Entry point: 0x00100040, address range: 0x00100000-0x001761d4

> go

Trying NPE-C...success. Using NPE-C with PHY 1
Ethernet eth0: MAC address 00:07:e9:16:34:72
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254
Default server: 192.168.200.254

RedBoot(tm) bootstrap and debug environment [RAM]
Red Hat certified release, version 2.02 - built 15:43:18, Nov 23 2006

Platform: IXP435 reference platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x00196c68-0x07fd1000] available
FLASH: 0x50000000 - 0x51000000, 128 blocks of 0x00020000 bytes each.

== Executing boot script in 3.000 seconds - enter ^C to abort
```

2. Load the primary RedBoot image to overwrite the current image in flash:

```
> load -r -v -b 0x00200000 redboot_ROM.bin
Using default protocol (TFTP)
\
Raw file loaded 0x00200000-0x00278edb, assumed entry at 0x00200000
> fis unlock RedBoot
... Unlock from 0x50000000-0x50080000:....
> fis create RedBoot -b 0x00200000 -l 0x0007A000 -f 0x50000000 -e 0x00000000
An image named 'RedBoot' exists - continue (y/n)? y
... Erase from 0x50000000-0x50080000:....
```

```
... Program from 0x00200000-0x0027a000 at 0x50000000:....
... Unlock from 0x51fe0000-0x52000000: .
... Erase from 0x51fe0000-0x52000000: .
... Program from 0x07fe0000-0x08000000 at 0x51fe0000: .
... Lock from 0x51fe0000-0x52000000: .
> fis lock RedBoot
... Lock from 0x50000000-0x50080000: ....
```

3. Reset the board by powering it off and on and verify that RedBoot starts up.

```
> +
Trying NPE-C...success. Using NPE-C with PHY 1.
Ethernet eth1: MAC address 00:03:47:df:32:aa
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254 Default server:
192.168.200.254

RedBoot(tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.02 - built 15:43:18, Nov 23 2006
Platform: IXP435 reference platform (Intel XScale processor) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x0002a350-0x07fc1000] available
FLASH: 0x50000000 - 0x51000000, 128 blocks of 0x00020000 bytes each.
RedBoot>
```

4. Use the RedBoot fis list command to review the flash segment content as known to RedBoot.

```
Example
RedBoot> fis list
Name              FLASH addr  Mem addr    Length      Entry point
RedBoot           0x50000000  0x50000000  0x00080000  0x00000000
redboot.bak       0x50800000  0x50800000  0x00080000  0x00000000
FIS directory     0x51FE0000  0x51FE0000  0x0001F000  0x00000000
RedBoot config 0x51FFF000  0x51FFF000  0x00001000  0x00000000
```

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