

# **XR-T6164/T6165/T6166**

## **Evaluation System User Manual**

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## OVERVIEW

This demo board is an evaluation system for the XR-T6164 LIU (Line Interface Unit) and XR-T6165/6166 Codirectional Digital Data Processor integrated circuits that simplifies both functional tests and comprehensive measurements on these devices. Test equipment requirements are minimized because a built-in pattern generator supplies PCM test data, and all timing signals are derived from an on-board crystal oscillator. Board operation requires only a 5V power source and an oscilloscope for observing data and timing waveforms.

Mechanically, the unit is a 5.75 by 7.75 inch mother board that accepts a pair of 2 inch by 2 inch daughter boards. The mother board contains timing logic, option selection switches, and I/O connections. One daughter board has the socket for either the XR-T6165 or the XR-T6166 device while the other holds the complete XR-T6164 LIU circuit. Programmable logic devices (PALS) are used for all mother board logic to make the unit electrically as well as mechanically versatile.

## MECHANICAL DESCRIPTION

*Figure 1* shows the mother board component marking. Option selection dip switches are located along the front edge. Directly behind them are five PALS that generate timing signals, an 8.192MHz crystal oscillator module that provides system clock, and a 74HC00 device that de-bounces the RESET switch, and buffers PCM frame sync outputs. Daughter boards for the XR-T6165 or XR-T6166 IC socket and for the XR-T6164 LIU are behind the PALS. *Figure 2*, *Figure 3*, and *Figure 4* show daughter board component markings. BNC connectors that are located along the mother board right edge are used for sync and timing signal outputs, and for external clock inputs. Two RJ-11 and a spare RJ-45 modular connector for 64 KBT/S I/O connections, and test points for XR-T6165/6166 output signals are located on the board rear edge. The test point signals are also present at small pads that are under the daughter boards. Therefore, any two of these signals may be easily connected with short jumper wires to the spare BNC connectors that are between the daughter boards. Power connections are made through two banana jacks that are located on the board left edge.

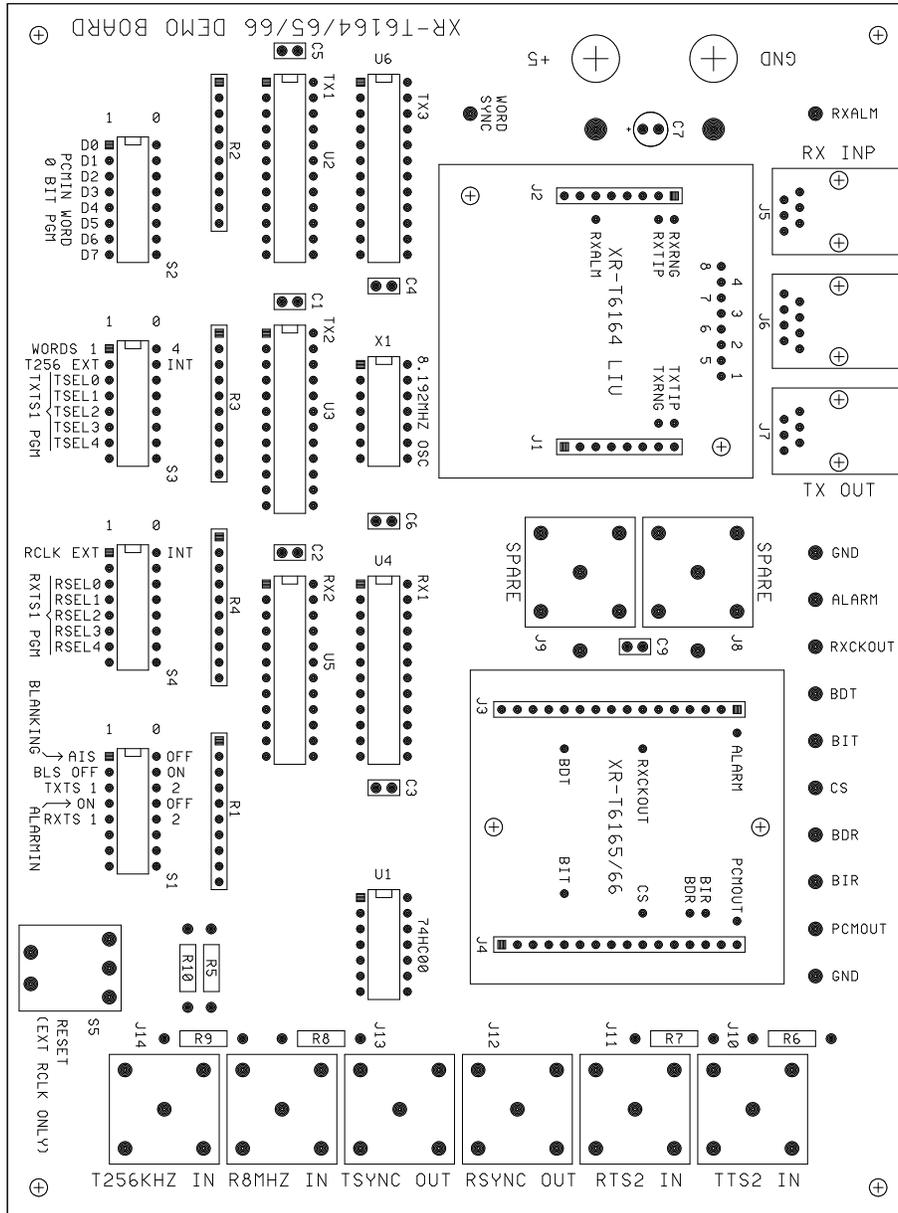
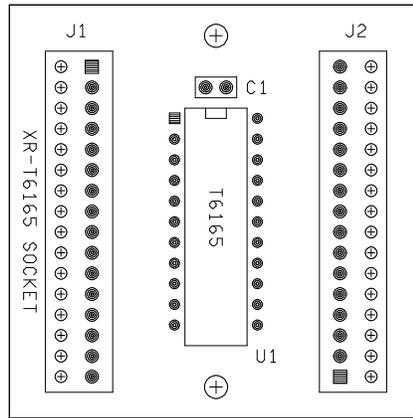
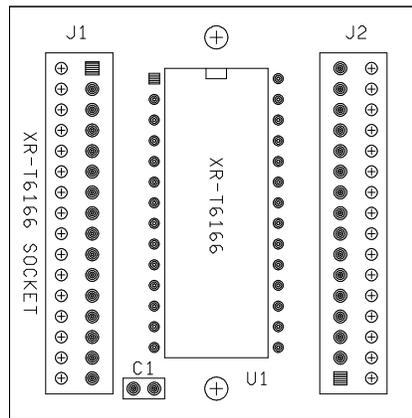


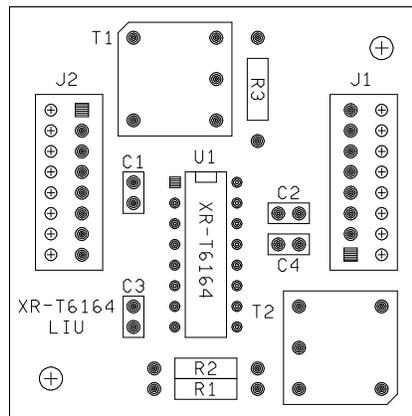
Figure 1. Mother Board Component Marking



**Figure 2. XR-T6165 Daughter Board Component Marking**



**Figure 3. XR-T6166 Daughter Board Component Marking**



**Figure 4. XR-T6164 LIU Daughter Board Component Marking**

## ELECTRICAL DESCRIPTION

This description refers to *Figure 5* and *Table 1* through *Table 8* that are located at the end of this section. Although the following discussion explicitly mentions the XR-T6166, the general information given applies equally well to the XR-T6165. Note that this device does not have the RXCKOUT, CS, BIR, BDR, BIT and BDT outputs that are present on the XR-T6166. Consult the device data sheets for more detailed information on each part.

### Block-level Overview

The block diagram given in *Figure 5* outlines the major demo board functions. It illustrates data and timing signal flow, and shows option selection switch connections to the different functional blocks. The top part of the diagram contains the transmit and the bottom part has the receive sides of the XR-T6166 digital processor and XR-T6164 LIU. Signal flow is clockwise starting with the pattern generator. The pattern generator supplies 8 bit bursts of 2.048MBT/Sec serial PCM data to the XR-T6166 transmitter PCMIN input. The XR-T6166 transmitter T+R and T-R outputs feed continuous, dual-rail, 64 KBT/Sec encoded data into the XR-T6164 LIU. The bipolar signal produced by the LIU transmitter is connected to the LIU receiver input by a short modular cable. The LIU receiver output dual-rail data is connected to the XR-T6166 receiver S+R and S-R inputs. The XR-T6166 receiver PCMOUT output provides 8 bit bursts of 2.048 MBT/Sec PCM data. The signal at this test point may be observed on an oscilloscope.

### Timing Generation Logic

The timing generation logic uses synchronous counters clocked at 8.192MHz rate to produce all the control signals necessary for XR-T6166 operation. Separate counters are used for generating the transmit and receive timing signals for maximum versatility. The transmit and receive time slot signals (TS1T and TS1R) are obtained by decoding the respective counter outputs, and then using the 8.192MHz clock and a D-type flip flop to re-time the signal. Thus, these outputs are glitch-free. The transmit and receive clocks (TX2MHZ and RX2MHZ) come from a single counter output and are retimed to preserve alignment with the time slot edges. The 256kHz transmit clock (TX256kHz), transmit frame sync (TSYNC OUT), receive frame sync (RSYNC OUT) and pattern generator WORD SYNC also come from single counter outputs, but are not retimed because alignment with a

time slot edge is not required. Therefore, these signals arrive one 8.192MHz clock period before the retimed signals.

The transmit counter is always clocked by the on-board 8.192MHz crystal oscillator module. However, the receive counter may be clocked either by this oscillator, or by an external 8.192MHz source. The 2 input to 1 output receive clock multiplexer that is controlled by S4, section 1, does this selection. Receive counter reset is performed through the 2 input to 1 output reset multiplexer. When the on-board oscillator is used to clock both counters, the receive counter is synchronously reset every four PCM frames by the transmit counter CLROUT pulse. Thus, synchronization is automatically obtained between the two counters. When an external receive clock source is used, the push button reset switch, S5, will initially synchronize the transmit and receive counters. S5 is non-functional when the on-board oscillator clocks both counters.

Any of the 32 possible transmit and receive time slot positions are user-selectable by binary coded settings on S3 and S4 respectively. S3 also selects pattern generator sequence length and XR-6166 transmitter 256kHz clock source. S4 also selects receive timing logic 8.192MHz clock source. *Table 1* and *Table 2* summarize S3 and S4 functions respectively. *Table 3* lists the binary settings for S3 and S4 for all 32 time slots.

### Pattern Generator

The pattern generator produces 8-bit bursts of data at a 2.048 MBT/Sec rate. This data, which may be either a repetitive one-word (8 bit) or four-word (32 bit) sequence, simulates the information that is taken from a PCM system buss and applied to the XR-6166 transmit side serial input (PCMIN). The pattern generator produces one user-programmable word (WORD 0) followed by three fixed words that are determined by PAL programming. It operates by decoding transmit timing logic counter outputs, anding this signal with the decoded signal that becomes the transmit time slot, and then retiming the result with the 8.192MHz clock and a D-type flip flop. The option of sending either WORD 0 repetitively, or the entire four-word sequence repetitively is available. *Table 4* shows WORD 0 programming by S2, and *Table 5* lists the bit patterns for all four words. The distinctive patterns with a single "one" bit were chosen for words 1, 2, and 3 because they make it easy to observe the delay through the looped-back system on an

oscilloscope. This procedure is explained in more detail in the section on board operation.

### *XR-T6165/6166 Time Slot Selection and Alarm Control*

The XR-T6165/6166 contains internal 2 input to 1 output multiplexers that select one of two available transmit and receive time slot sources. Both transmit and receive time slot 1 are generated on-board while time slot 2 is obtained from an external source. Also, three transmit and receive alarms options are available. *Table 6* summarizes the functions controlled by S1.

### **Demo Board Power Requirements**

A well-regulated +5.0V  $\pm 5\%V$  source of at least 1 Ampere is necessary for board operation. Power connections are made through red (+5) and black (Ground) banana jacks.

### **Input/Output Connections**

#### *64 KBT/Sec Signal Connections*

The LIU transmitter output and receiver input 64 KBT/S signal connections are made through RJ-11 jacks located

at the rear of the board. The short jumper cable supplied with the board is used to connect the transmitter output to the receiver input during testing. This jumper does not contain a "twist" like a modular telephone cord. A standard modular cord will give a tip-ring reversal between transmitter output and receiver input.

An unconnected RJ-45 jack that may be used for both input and output functions is also provided. This jack may be easily connected as required since all eight pins are brought out to PC board pads.

#### *BNC Connections*

Inputs for external clocks and timing signals as well as transmit and receive sync outputs are made through BNC connectors. Two extra connectors are provided for use as needed. *Table 7* lists the connector functions.

#### *Test Points*

Test points provide access to a number of different XR-T6166 output signals and circuit ground. Their functions are listed in *Table 8*. For convenience, the test point signals are also connected to small PC board pads that are located under the XR-T6166 daughter board.

## BLOCK DIAGRAM

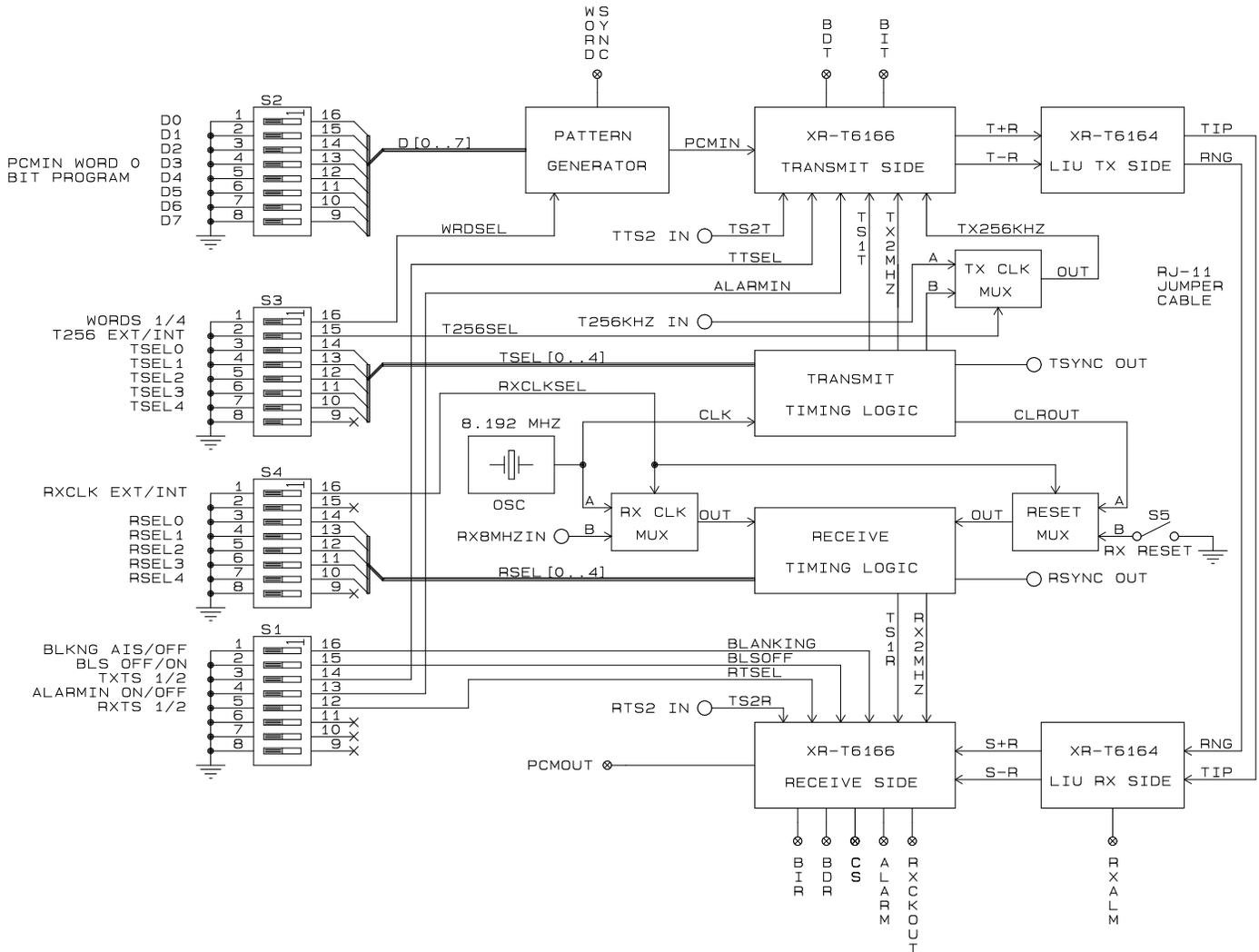


Figure 5. Demo Board Block Diagram

Section Number and Name	Function	Switch Setting	Option
1 WORDS - 1/4	Selects Repetitive 1 or 4 Word Sequence	OFF	Repeats 8-Bit PCMIN Word 1 (Pattern Set By S2)
		ON	Repeats 32 Bit Sequence Composed of PCMIN Word 1 Followed By 3 Built-in Words
2 T256 - EXT/INT	Selects 256kHz Transmit Clock Source	OFF	External Transmit Clock Applied to T256kHz IN Input Used
		ON	Clock Generated Internally By Demo Board Used
3 Through 7 TXTS1 PGM	Selects Transmit Time Slot 1 Position (5 Bit Binary Code is Time Slot Number)	OFF	Bit is a Logic 1
		ON	Bit is a Logic 0
8	(Section Not Used)		

**Table 1. DIP Switch S3 Functions**

Section Number and Name	Function	Switch Setting	Option
1 RXCLK - EXT/INT	Selects 8.192MHz Receive Clock Source	OFF	External Clock Applied to R8MHZ IN Input Used
		ON	Clock Generated Internally By Demo Board Used
2	(Section Not Used)		
3 Through 7 RXTS1 PGM	Selects Receive Time Slot 1 Position (5 Bit Binary Code is Time Slot Number)	OFF	Bit is a Logic 1
		ON	Bit is a Logic 0
8	(Section Not Used)		

**Table 2. Dip Switch S4 Functions**

Time Slot Position	Dip Switch Setting (S3 and S4)				
	SEL0	SEL1	SEL2	SEL3	SEL4
0	ON	ON	ON	ON	ON
1	OFF	ON	ON	ON	ON
2	ON	OFF	ON	ON	ON
3	OFF	OFF	ON	ON	ON
4	ON	ON	OFF	ON	ON
5	OFF	ON	OFF	ON	ON
6	ON	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON	ON
8	ON	ON	ON	OFF	ON
9	OFF	ON	ON	OFF	ON
10	ON	OFF	ON	OFF	ON
11	OFF	OFF	ON	OFF	ON
12	ON	ON	OFF	OFF	ON
13	OFF	ON	OFF	OFF	ON
14	ON	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF	ON
16	ON	ON	ON	ON	OFF
17	OFF	ON	ON	ON	OFF
18	ON	OFF	ON	ON	OFF
19	OFF	OFF	ON	ON	OFF
20	ON	ON	OFF	ON	OFF
21	OFF	ON	OFF	ON	OFF
22	ON	OFF	OFF	ON	OFF
23	OFF	OFF	OFF	ON	OFF
24	ON	ON	ON	OFF	OFF
25	OFF	ON	ON	OFF	OFF
26	ON	OFF	ON	OFF	OFF
27	OFF	OFF	ON	OFF	OFF
28	ON	ON	OFF	OFF	OFF
29	OFF	ON	OFF	OFF	OFF
30	ON	OFF	OFF	OFF	OFF
31	OFF	OFF	OFF	OFF	OFF

**Table 3. TXTS1 and RXTS1 Selection Options**

Section Number and Name	Function	Switch Setting	Option
1 through 8 PCMIN WORD 0 BIT PGM	Programs 8 bit PCMIN Word 1	OFF	Sets Bit in PCMIN Word 1 (Transmitter Input Data) to a High Level (Logic 1)
		ON	Sets Bit in PCMIN Word 1 (Transmitter Input Data) to a Low Level (Logic 0)

**Table 4. Dip Switch S2 Functions**

Word	Bit Pattern	Notes
0	1 0 1 0 1 0 0 1	User-Programmable with S2
1	0 0 0 0 0 0 0 1	Programmed in PAL
2	1 0 0 0 0 0 0 0	Programmed in PAL
3	0 0 0 1 0 0 0 0	Programmed in PAL

**Table 5. Pattern Generator Bit Patterns**

Section Number and Name	Function	Switch Setting	Option
1 Blanking - AIS/OFF	Controls PCMOUT Data Blanking (Sets T6166 Pin 6 Logic Level)	OFF	Receiver Data at PCMOUT Always Forced to all Ones Condition (AIS Signal)
		ON	Normal Receiver Output Data Present at PCMOUT
2 BLS - OFF/ON	Controls Byte Lock Supervision (Sets T6166 Pin 4 Logic Level)	OFF	BLS (Byte Lock Supervision) Not Active, Data at PCMOUT is Always Receiver Input Data
		ON	BLS (Byte Lock Supervision) Active, PCMOUT Blanked When AIS Received
3 TXTS - 1/2	Selects Transmit Time Slot (Sets T6166 Pin 15 Logic Level)	OFF	Transmit Time Slot 1 (Internally Generated on Demo Board) Used
		ON	Transmit Time Slot 2 (Externally Applied to TTS2 IN Input) Used
4 ALARMIN - ON/OFF	Provides Alarm Input Signal (Sets T6166 Pin 16 Logic Level)	OFF	Violations Used for Octet Timing in Transmitter Output Signal are Inhibited (Alarm Condition)
		ON	Violations Used for Octet Timing are Present in Transmitter Output Signal (Normal Operation)
5 RXTS - 1/2	Selects Receive Time Slot (Sets T6166 Pin 27 Logic Level)	OFF	Receive Time Slot 1 (Internally Generated On Demo Board) Used
		ON	Receive Time Slot 2 (Applied To RTS2 In Input) Used
6, 7, 8	(Section Not Used)		

**Table 6. Dip Switch S1 Functions**

BNC Conn.	Signal Description
TTS2 IN	Transmit Time Slot 2 Input (Connected to T6166 Pin 12)
RTS2 IN	Receive Time Slot 2 Input (Connected to T6166 Pin 24)
RSYNC OUT	Buffered 8kHz Receive Frame Sync Signal Output
TSYNC OUT	Buffered 8kHz Transmit Frame Sync Signal Output
R8MHZ IN	External 8.192MHz Receive Timing Logic Clock Input
T256kHz IN	External 256kHz Transmit Clock Input (Connected to T6166 Pin 17)
SPARE	Uncommitted Connector
SPARE	Uncommitted Connector

**Table 7. BNC Connector Functions**

Test Point	Signal Description
RXALM	LIU Loss of Signal Alarm Output (T6164 Pin 3)
GND	Circuit Ground
ALARM	Octet Timing Alarm Output (T6166 Pin 1)
RXCKOUT	Extracted 128kHz Receive Clock Output (T6166 Pin 7)
BDT	Transmitter Byte Deletion Flag Output (T6166 Pin 11)
BIT	Transmitter Byte Insertion Flag Output (T6166 Pin 18)
CS	Clock Seek Output from Receiver Clock Recovery Circuit (T6166 Pin 22)
BDR	Receiver Byte Deletion Flag Output (T6166 Pin 25)
BIR	Receiver Byte Insertion Flag Output (T6166 Pin 26)
PCMOUT	Receiver PCM Data Output (T6166 Pin 28)
GND	Circuit Ground
WORD SYNC	2kHz Sync Signal Output for Pattern Generator 4-Word Sequence

**Table 8. Test Point Functions**

## BOARD OPERATION

This description refers to *Table 9* and *Figure 6* through *Figure 14* which are located at the end of this section.

### Start-up Procedure

Perform the following steps to operate the demo board.

1. Preset the four dip switches in the positions indicated in *Table 9*.
2. Connect TX OUT to RX IN RJ-11 connectors together with the short modular cable supplied with the board. This operation loops the XR-T6164 LIU transmitter line-side output to receiver line-side input.

3. Power the board by connecting a regulated power supply capable of supplying 5V  $\pm$ 5% at least 1 Ampere to the red (+5V) and black (Ground) banana jacks.

### Waveform Measurements

The board is now in operation, and *Figure 6*, *Figure 7*, and *Figure 8* are examples of some of the waveforms that may be observed. *Figure 6* shows the acquisition of a byte of 2.048MBT/Sec data by XR-T6166 transmit-side. While the transmit time slot (TS1T) is high, the 2.048MHz transmit clock (TX2MHZ) clocks the 8-bit pattern 1 0 1 0 1 0 0 1 into the serial data input (PCMIN). The clock, data, and time slot edges are all aligned since these signals,

which are derived from the transmit timing logic synchronous counters, are all re-timed by the 8.192MHz system clock. The bottom trace in *Figure 6* shows the 256kHz transmitter output clock (TX256kHz). As described in the timing logic section, this clock does not have edge alignment with the other three waveforms because it is not retimed. Note that there is not a phase alignment requirement constant but not a specific phase alignment is necessary between the XR-T6166 transmitter input timing signals and output clock. If this phase changes because of input or output clock frequency changes, data slips will occur.

*Figure 7* shows the XR-T6166 receive-side output process for a byte of 2.048MBT/Sec data. While the receive time slot (TS1R) is high, the 2.048MHz receive clock (RX2MHZ) clocks the 8-bit pattern 1 0 1 0 1 0 0 1 out the serial data output (PCMOUT). Note that the relationship between the bottom trace (RSYNC OUT) and the receive time slot (TS1R) indicates that this time slot is in position 0.

*Figure 8* shows the XR-T6164 LIU transmitter-side bipolar output signal. For this photograph the looped connection between TX OUT and RX INP was removed and TX OUT was terminated with 120Ω. The top trace, which is TSYNC OUT, represents one PCM frame and therefore has a 125μS period. The bottom trace shows the encoded bipolar signal that represents the repetitive 1 0 1 0 1 0 0 1 bit pattern that was applied to the PCMIN input. Annotation located on the picture below the bottom trace summarizes the coding process for each bit position, and indicates the bipolar violations that are used for octet timing.

*Figure 9* is a timing diagram that contains more information than can be shown on a 4 trace oscilloscope. It shows both the XR-T6166 receive-side PCMIN input data and the transmit-side PCMOUT data for the repetitive 1 0 1 0 1 0 0 1 bit pattern. Note that this fixed relationship exists between the XR-T6166 receiver and transmitter because the demo board is operating in the mode where all timing is derived from the on-board 8.192MHz oscillator. With the exception of changing TS1R (receive time slot 1) from position 0 to position 1 by placing S4, section 3 (RSEL0) in the “OFF” position, conditions for this diagram are the same as for the photographs described previously. Although this diagram indicates the relationship between transmitting in time slot position 0 and receiving in time slot position 1, it provides no information about the delay through the

loopedback system. However, this delay can be measured by using a repetitive 4-word sequence.

### Operation With A Repetitive 4-Word Sequence

A repetitive 4-word (32 bit) sequence allows the measurement of the XR-T6166 serial PCM input (PCMIN) to output (PCMOUT) delay. The timing diagrams given in *Figure 10* through *Figure 14* show PCMIN and PCMOUT data as WORD 0 through WORD 3 are sequentially applied to the PCMIN input. (To change the pattern generator from a 1-word to 4-word sequence, place S3, section 1, in the “ON” position.) This operation is summarized below.

Figure 10 - Frame 1:	1 0 1 0 1 0 0 1	Sent
	0 0 0 0 0 0 0 1	Received
Figure 11 - Frame 2:	1 0 0 0 0 0 0 0	Sent
	0 0 0 1 0 0 0 0	Received
Figure 12 - Frame 3:	0 0 0 0 0 0 0 1	Sent
	1 0 1 0 1 0 0 1	Received
Figure 13 - Frame 4:	0 0 0 1 0 0 0 0	Sent
	1 0 0 0 0 0 0 0	Received
Figure 14 - Frame 5:	1 0 1 0 1 0 0 1	Sent
	0 0 0 0 0 0 0 1	Received

Thus, for the loopbacked condition, data applied to the PCMIN input arrives at the PCMOUT output two frames later. This may be verified by oscilloscope measurements made using the delayed sweep and triggering from the WORD SYNC test point.

### Advanced Capabilities

Many different timing measurements may be made by applying externally generated clocks and timing signals to the demo board. The frame sync reference signals TSYNC OUT and RSYNC OUT may be used to trigger external signal sources. These outputs are buffered with a 74HC00 NAND gate, but if more drive capability is required, a regular TTL part may be easily substituted since the device is in a socket.

### Receive Buffer Tests

The XR-T6166 transmitter and receiver sides may be operated at slightly different frequencies if an external 8.192MHz clock source is used for the receive timing logic. Therefore, the effects resulting from the receive buffer either becoming empty or overflowing may be observed. The XR-T6166 data sheet should be consulted for more information regarding this buffer. To use an

external clock, place S4, section 1 (RCLK), in the EXT (OFF) position and connect a stable, adjustable 8.192MHz source with a TTL compatible output to the R8MHz IN BNC connector. Momentarily pressing the RESET switch (S5) will now synchronize the transmit and receive timing logic counters, and all control signals that are derived from them. However, if the external and internal clock sources are not exactly the same frequency, synchronization will be lost and a receiver slip will ultimately occur.

### *Transmit Buffer Tests*

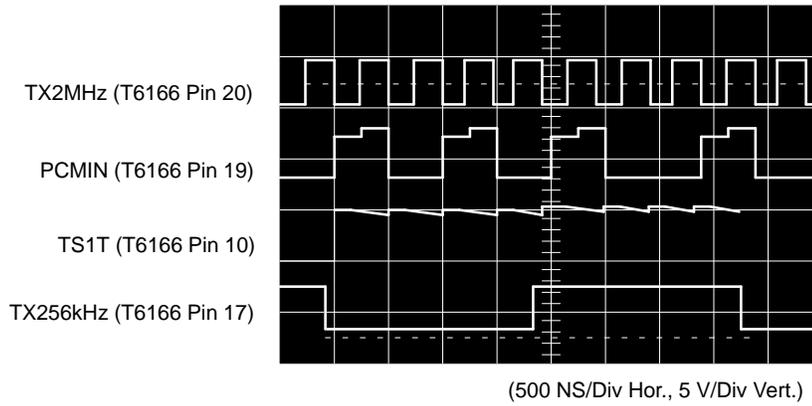
The effects of an empty or overflow condition in the XR-T6166 transmit may be observed by operating the transmitter with an external 256kHz transmit clock. To use an external clock, place S3, section 2 (T256) in the EXT (OFF) position and connect a stable, adjustable 256kHz source with a TTL compatible 50% duty cycle square wave output to the T256kHz IN BNC connector. The frequency of this external source must be carefully adjusted to obtain the desired results. Note that no initial synchronization is necessary, because no transmit time slot to 256kHz transmit clock phase alignment is required.

### *Timing Alignment Tests*

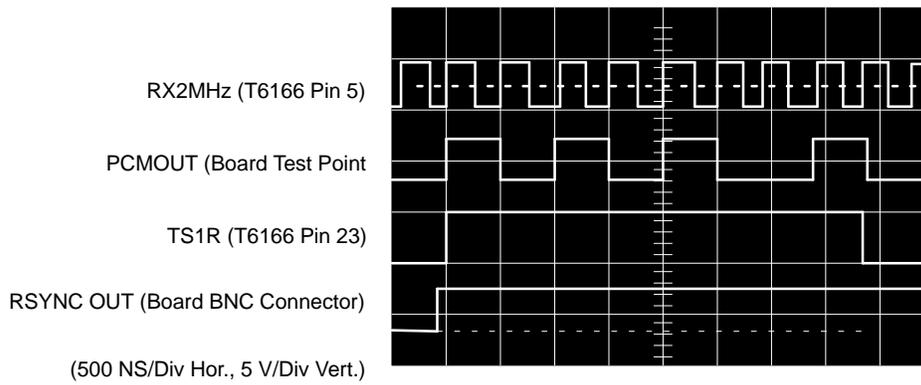
Many different timing alignment tests are possible if a laboratory pulse generator with external trigger, adjustable delay between trigger and pulse output, and adjustable output pulse width is available. The basic procedure is to trigger the generator from TSYNC OUT or RSYNC OUT as required, and then use the generator output to provide the transmit or receive time slot signal. This externally generated time slot is applied by selecting time slot 2 with S1, and then feeding the signal directly into the XR-T6166 through TTS2 IN or RTS2 IN as appropriate. The generator trigger delay determines the time slot position, and the output pulse width control sets the time slot width. Although the internally generated time slot with ideal timing is not being used, it is still present at the XR-T6166 time slot 1 input. Therefore, it may be conveniently monitored with an oscilloscope, and used as a reference for adjusting the externally produced time slot position and width. The effects of moving the time slot position relative to the XR-T6166 transmit or receive 2.048MHz clock may now be investigated. Note that since the pattern specified for WORD 0 (1 0 1 0 1 0 0 1) has a "one" on each end, it is useful when testing for dropped bits. A pattern with a "zero" on each end should be used when testing for added bits.

DIP Switch	Section	Switch Setting	Option Selected
S1	1	ON	Normal Receiver Data at PCMOUT (Not AIS)
	2	ON	BLS (Byte Lock Supervision) Active
	3	OFF	Transmit Time Slot 1 Selected
	4	ON	Octet Timing Violations Present in Transmitter Output
	5	OFF	Receive Time Slot 1 Selected
	6-8	Don't Care	Sections Unused
S2	1	OFF	
	2	ON	
	3	OFF	
	4	ON	PCMIN Word 0 Programmed as 1 0 1 0 1 0 0 1
	5	OFF	
	6	ON	
	7	ON	
	8	OFF	
S3	1	OFF	PCMIN Word 0 Sent Repetitively
	2	ON	Internal 256kHz Transmit Clock Selected
	3	ON	
	4	ON	
	5	ON	Transmit Time Slot 1 Programmed as Position 0
	6	ON	
	7	ON	
	8	Don't Care	Section Unused
S4	1	ON	
	2	Don't Care	Section Unused
	3	ON	
	4	ON	
	5	ON	Receive Time Slot 1 Programmed as Position 0
	6	ON	
	7	ON	
	8	Don't Care	Section Unused

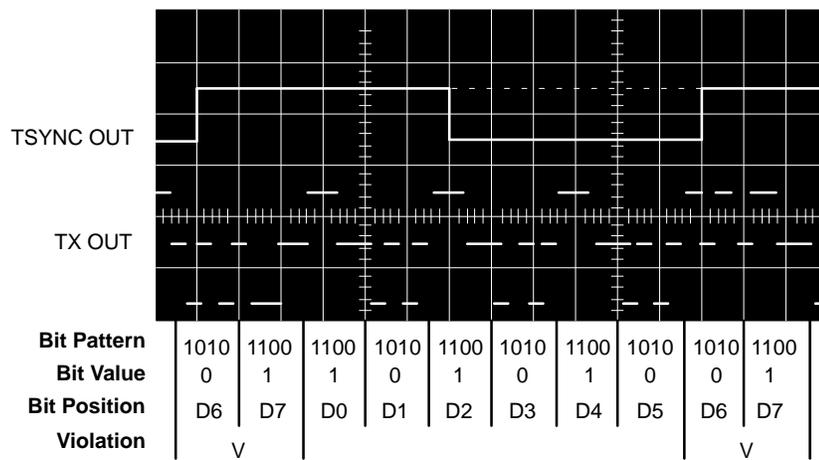
**Table 9. Dip Switch Preset Positions**



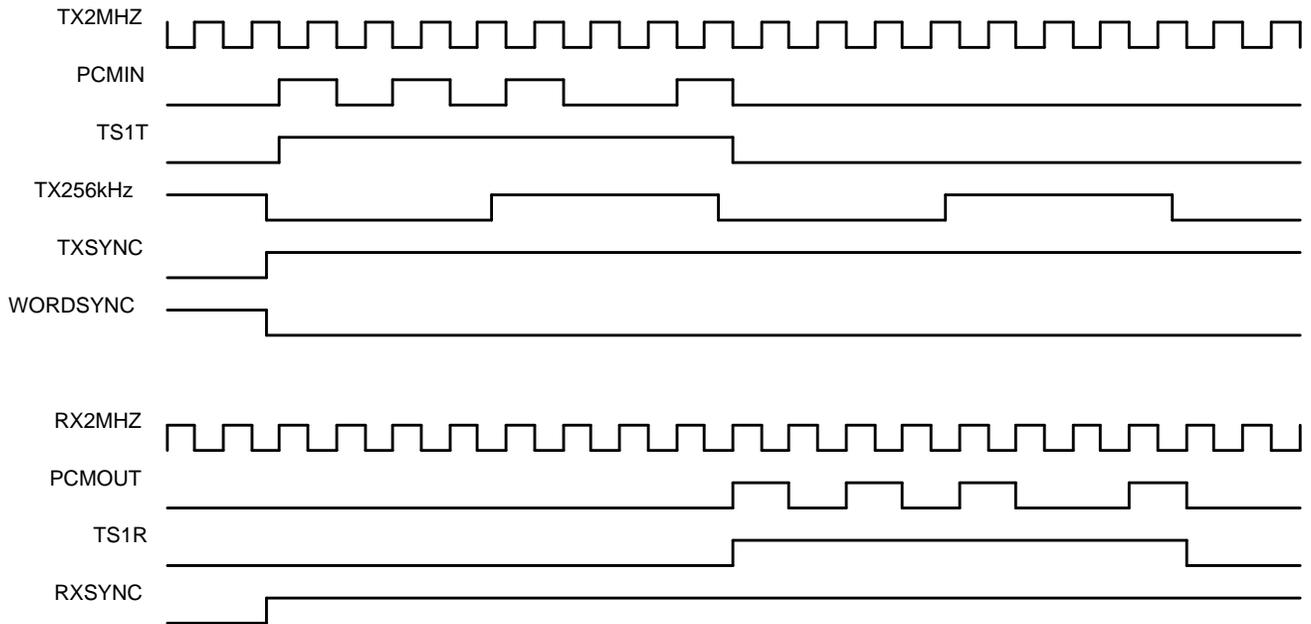
**Figure 6. XR-T6166 Transmitter-side Waveforms**



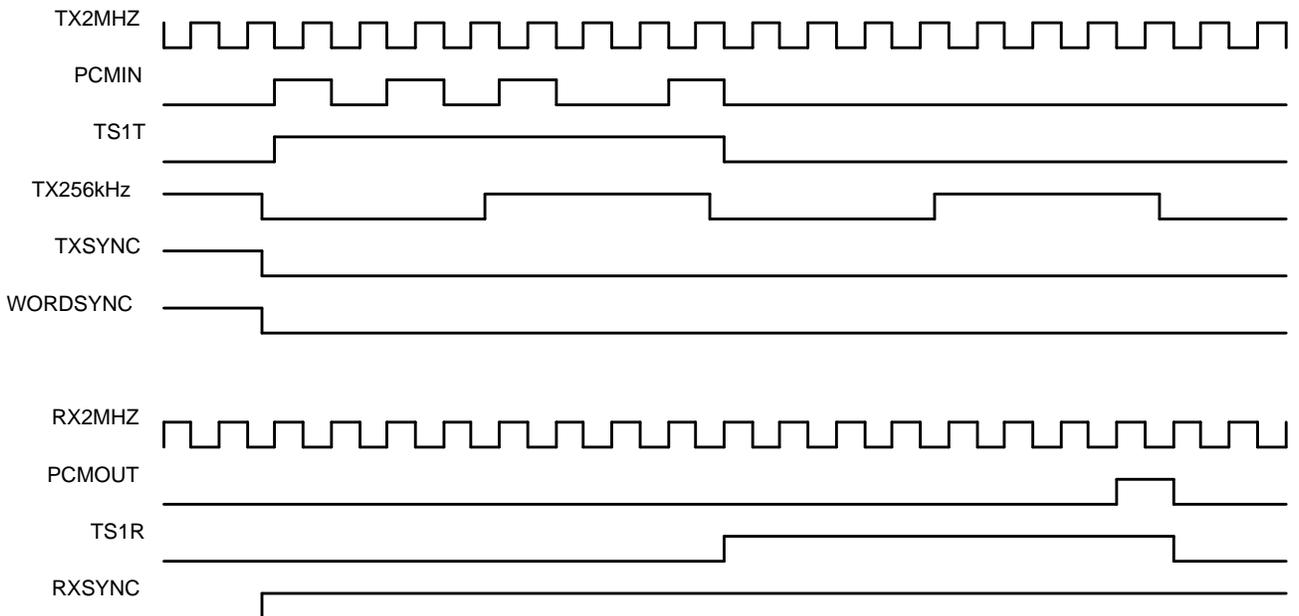
**Figure 7. XR-T6166 Receiver-side Waveforms**



**Figure 8. XR-T6164 Transmitter Output Waveforms**



**Figure 9. Timing with Repetitive Word 0**



**Figure 10. Frame 1 - Timing with 4-Word Sequence**

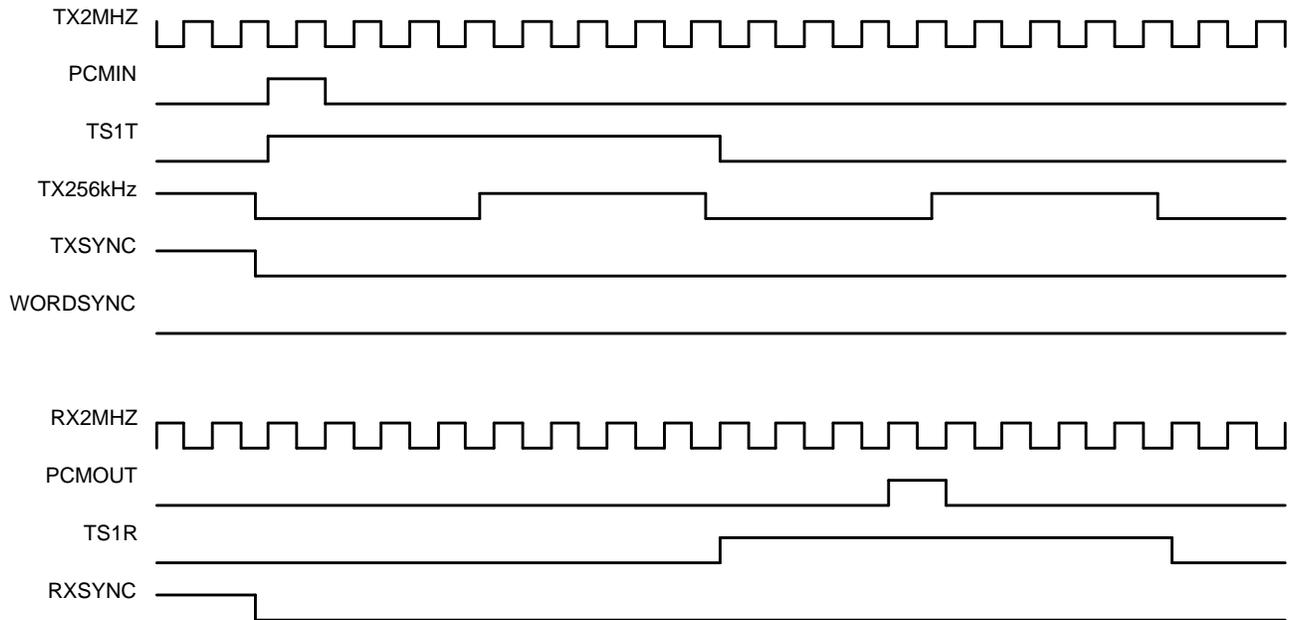


Figure 11. Frame 2 - Timing with 4-Word Sequence

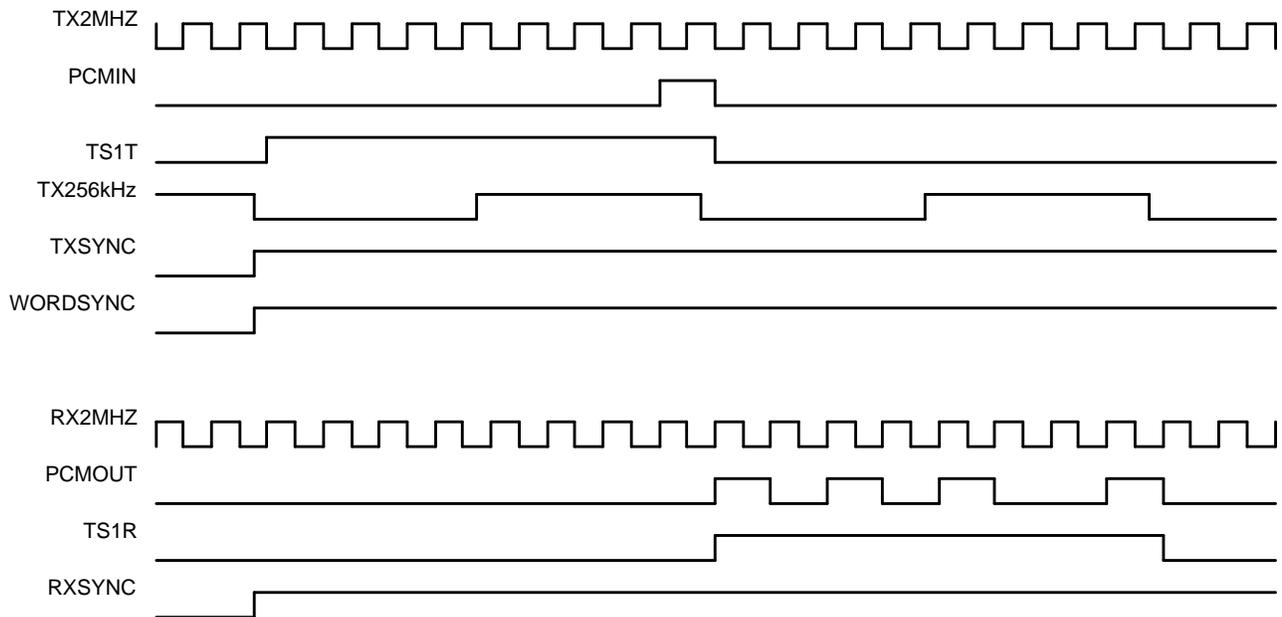
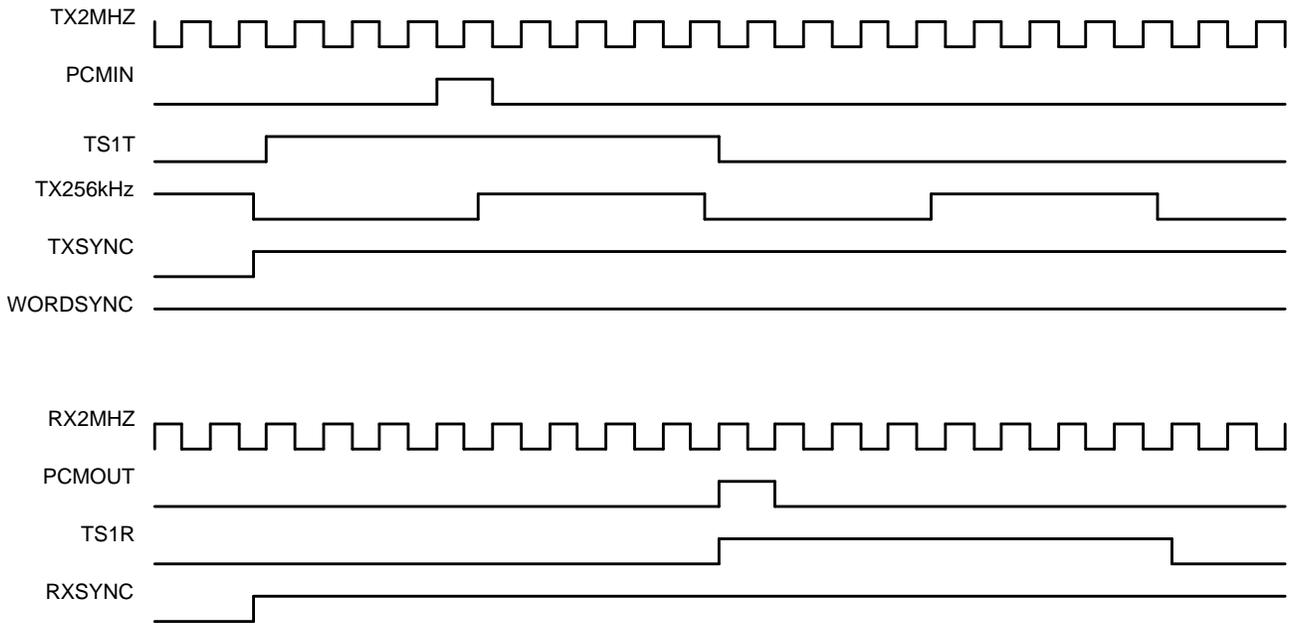
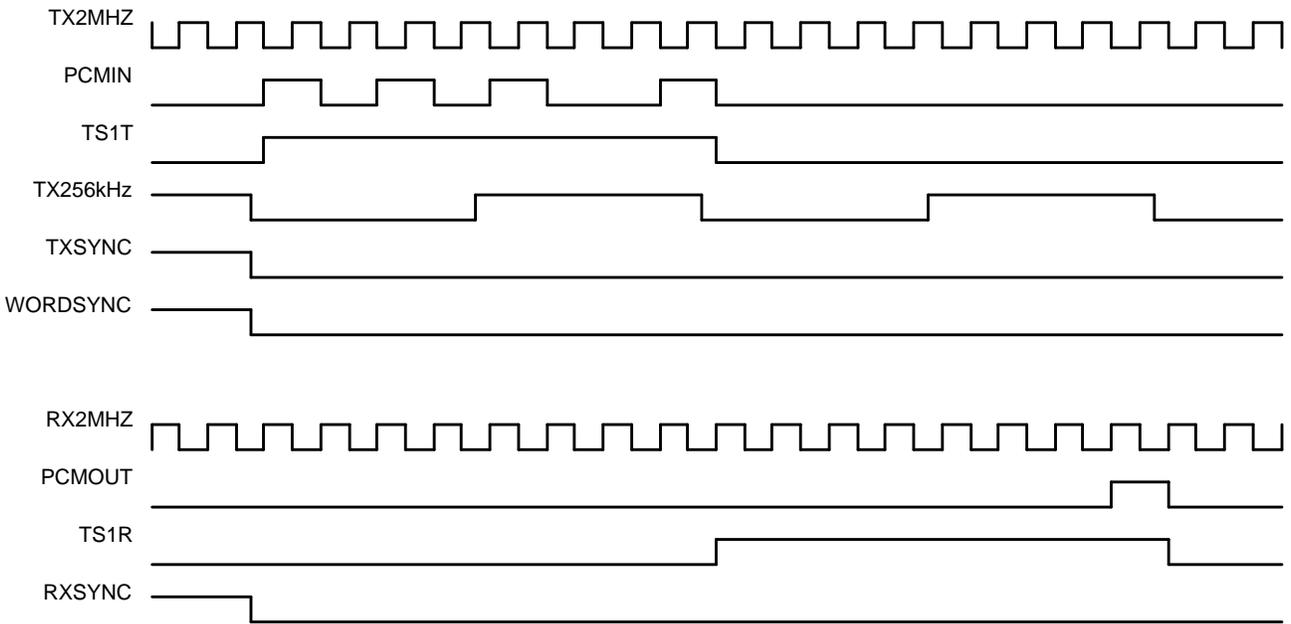


Figure 12. Frame 3 - Timing with 4-Word Sequence



**Figure 13. Frame 4 - Timing with 4-Word Sequence**



**Figure 14. Frame 5 - Timing with 4-Word Sequence**

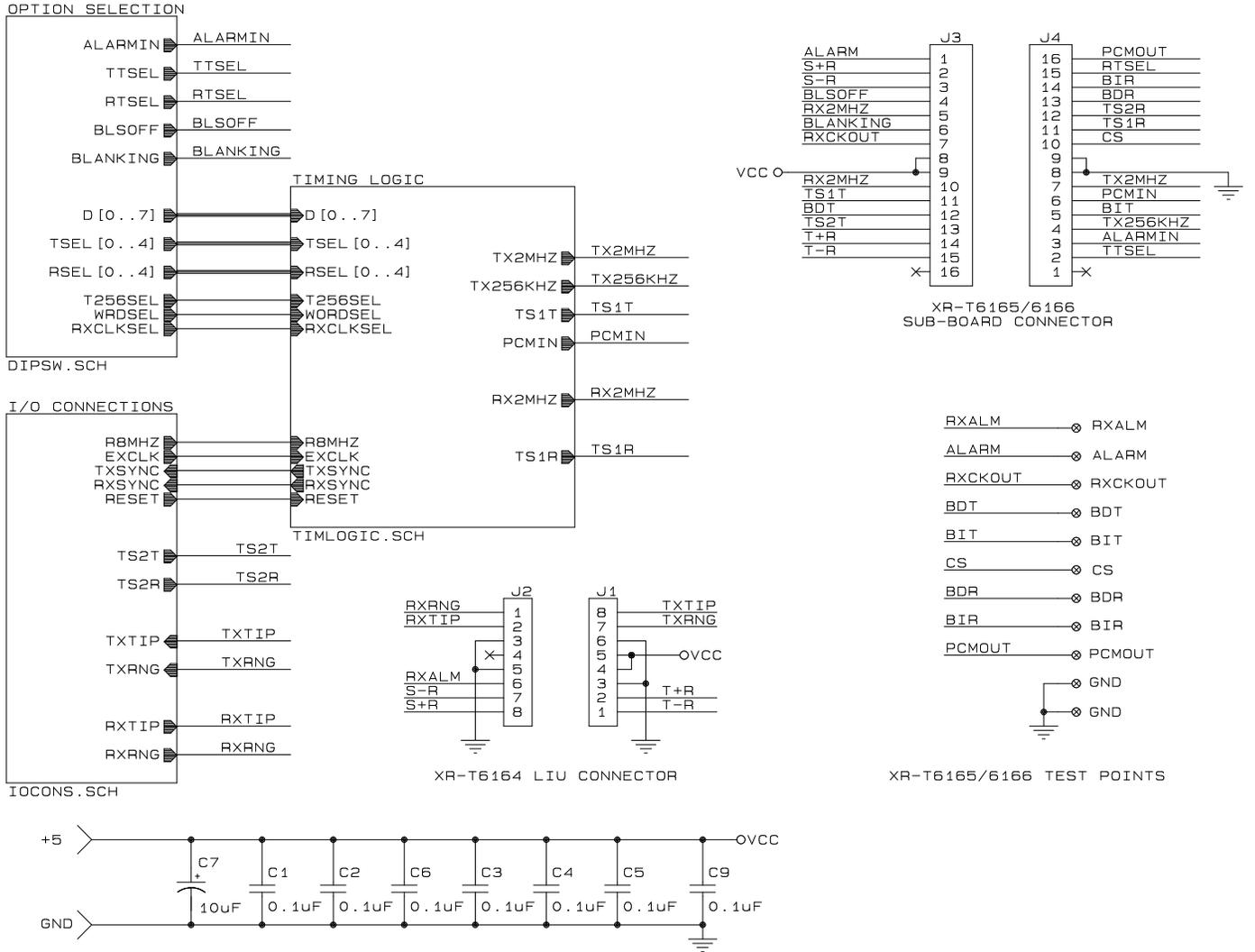
## SCHEMATIC DIAGRAMS

*Figure 15* through *Figure 18* contain the mother board schematic diagrams. *Figure 15* is a top-level diagram, and *Figure 16*, *Figure 17*, and *Figure 18* show the Option Selection, I/O Connections, and Timing Logic details respectively. *Figure 19* contains the XR-T6165 and

XR-T6166 socket daughter boards, and *Figure 20* is the XR-T6164 LIU daughter board diagram.

## LIST OF MATERIALS

*Table 10* through *Table 13* list all components used in the XR-T6164/65/66 evaluation system.



**Figure 15. Demo Board Top Level Schematic**

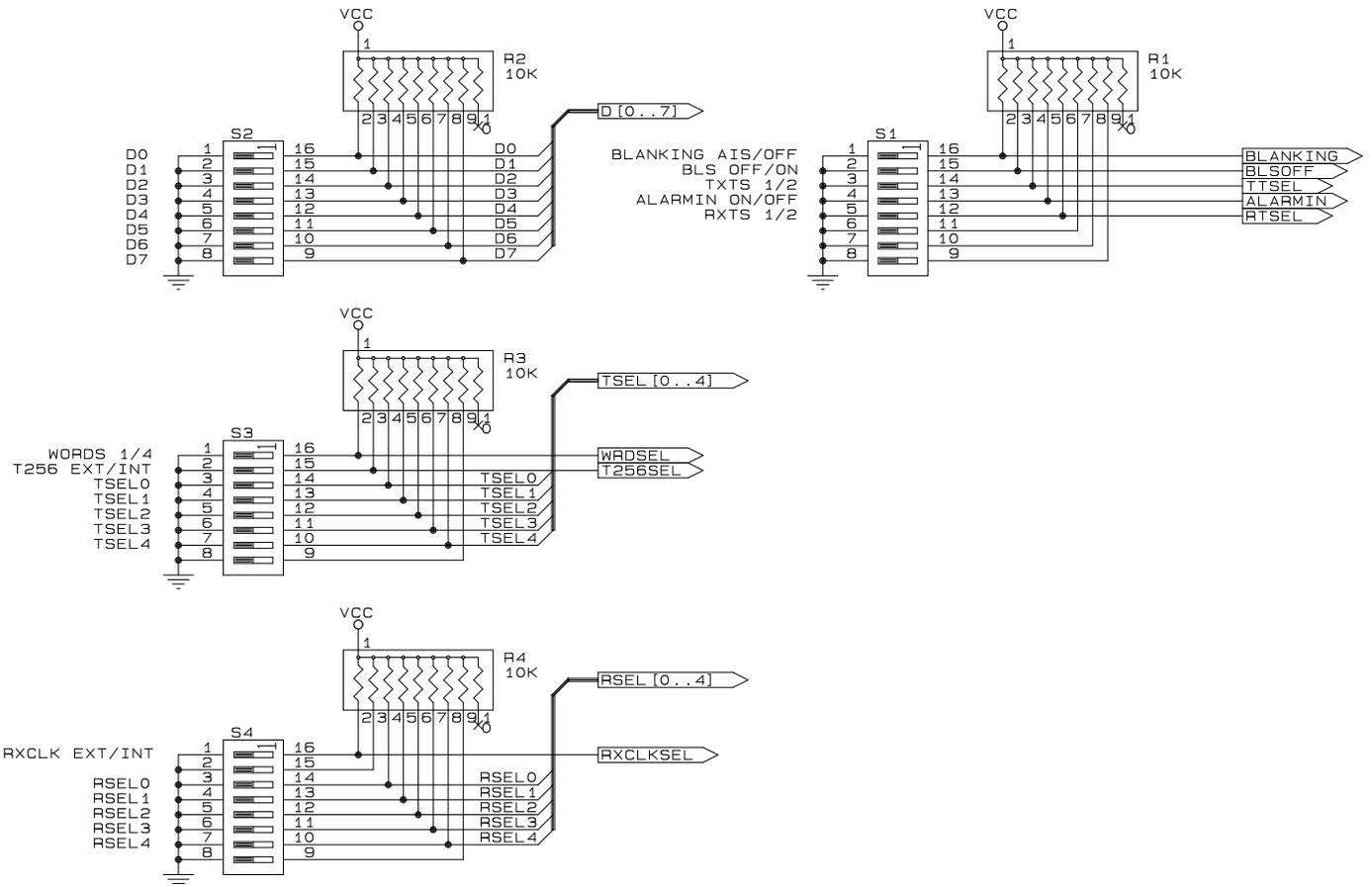
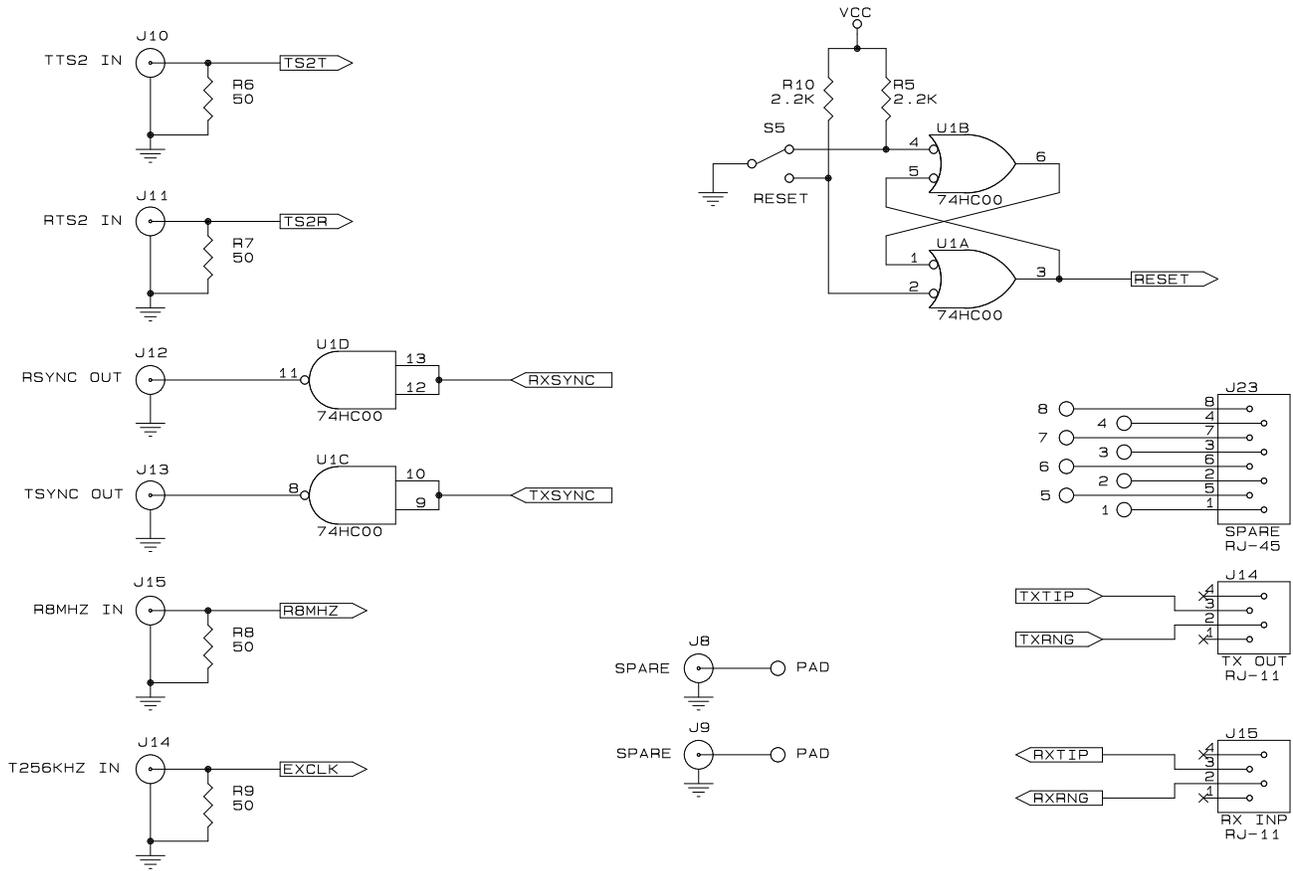


Figure 16. Demo Board Option Selection Switch Schematic



**Figure 17. Demo Board Option Input/Output Connector Schematic**

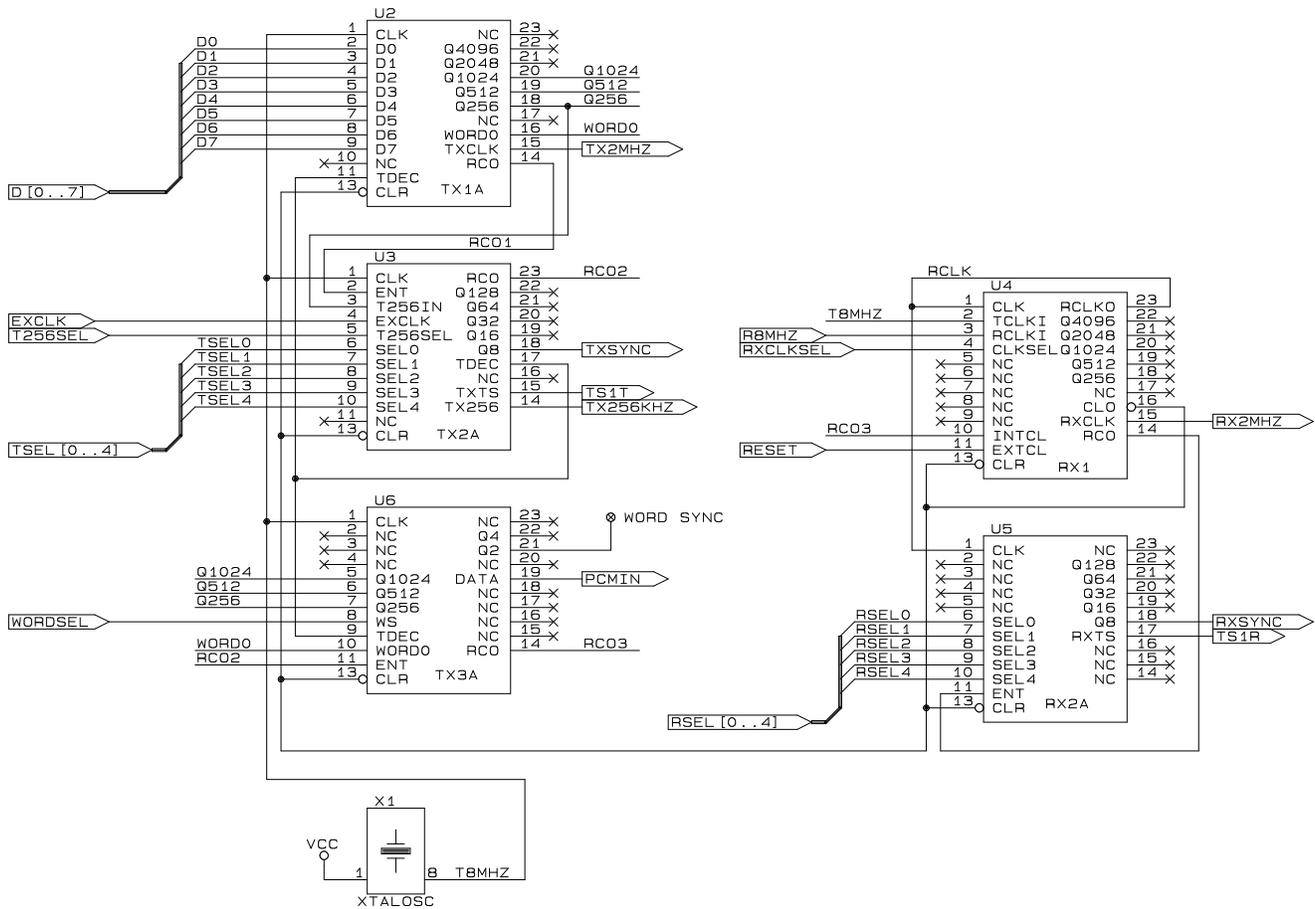


Figure 18. Demo Board Timing Logic Schematic

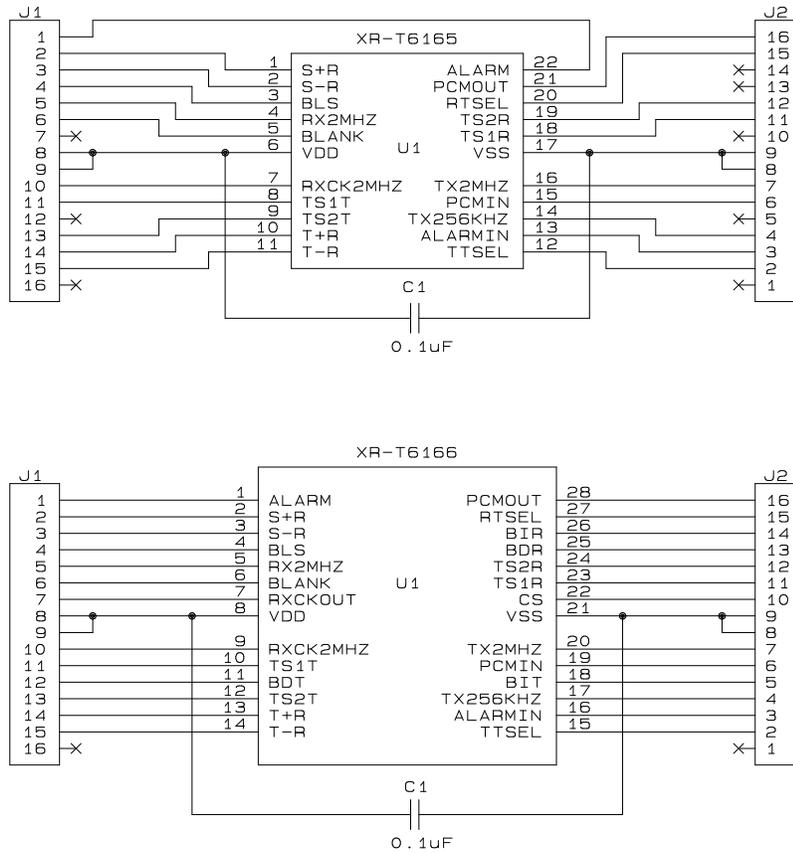


Figure 19. XR-T6165 and XR-T6166 Daughter Board Schematic

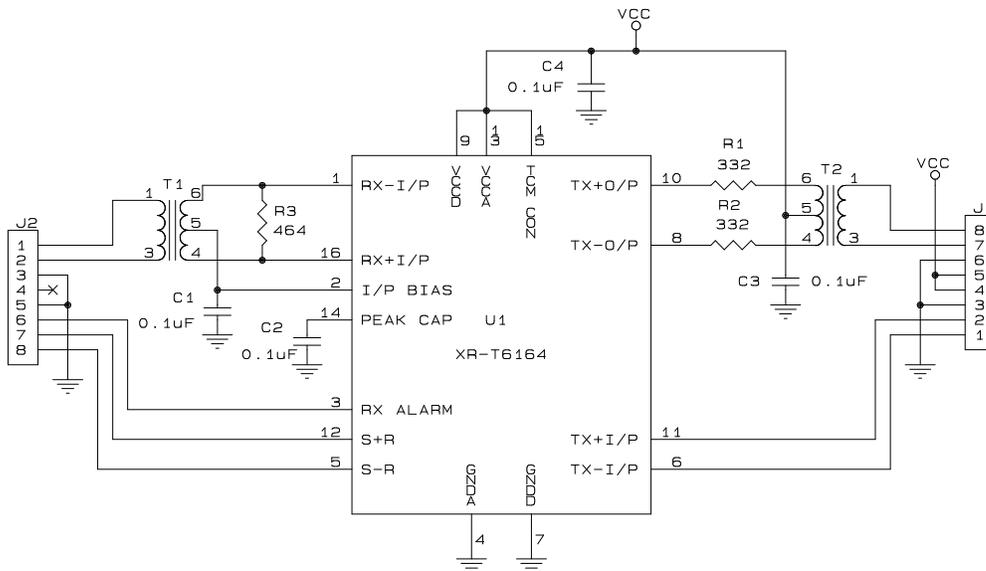


Figure 20. XR-T6164 LIU Daughter Board Schematic

QTY	Reference	Description	Supplier
7	C1,2,3,4,5,6,9	0.1μF, 63V, Z5U Dielectric, Axial lead, 0.1" Spacing	Digi-Key P4917
1	C7	22μF, 16V Electrolytic Cap, Radial Lead, 5mm Dia, 2mm Lead Spacing, Panasonic NHE	Digi-Key P5228-ND
4	R1,2,3,4	10K, 2%, 10 Resistor, Thick-film Network, Panasonic	Digi-Key Q9103-ND
1	R5,10	2.21K, 1/4 W, 1% Resistor	Digi-Key 2.21KBKX-ND
1	R6,7,8	51.1Ω, 1/4 W, 1% Resistor	Digi-Key 51.1BKX-ND
4	S1,2,3,4	8 Position Dip Switch, Amp	Digi-Key A5308-ND
1	S5	SPDT Momentary Push Button Switch, C&K 8125SD9ABE	Digi-Key CKN4014-ND
2	J1,2	8 Pin Header, 0.42" Pins on Top End	Digi-Key S1041-36-ND, (Cut from 36 Pin Strip)
2	J3,4	16 Pin Header, 0.42" Pins on Top End	Digi-Key S1041-36-ND, (Cut from 36 Pin Strip)
2	J5,7	RJ-11 Connector	
1	J6	RJ-45 Connector	
1	J8,9,10,11,12,13,14,15	PC Board Mount Female BNC Connector, KC 79-07-M06	NEWARK Part No. 44F8494
1	U1	74HC00	
1	U2	22V10 PAL, TX1	Custom Programmed Part
1	U3	22V10 PAL, TX2	Custom Programmed Part
1	U4	22V10 PAL, RX1	Custom Programmed Part
1	U5	22V10 PAL, RX2	Custom Programmed Part
1	U6	22V10 PAL, TX3	Custom Programmed Part
1	X1	8.192MHz Oscillator Unit, Epson SG-51P8.192MC	Digi-Key SE1728-ND
12		Pins for Test Points	Digi-Key ED-5052-ND2
2		Banana Jacks (1 Black, 1 Red)	(GND and +5V Connections)
5		24 Pin IC Socket, 0.3" Spacing	Digi-Key ED-3324-ND
2		14 Pin IC Socket	Digi-Key ED-3314-ND
4		Spacers to Elevate Board	
4		4-40 x 5/16" Screws for Spacers	
1		Short Modular (RJ-11) Cord to Loop Board	

**Table 10. XR-T6164/65/66 Mother Demo Board Parts List**

QTY	Reference	Description	Supplier
4	C1,2,3,4	0.1µF, 63V, Z5U Dielectric, Axial lead, 0.1" Spacing	Digi-Key P4917
2	R1,2	332Ω, 1/4 W, 1% Resistor	Digi-Key 332BKX-ND
1	R3	464Ω, 1/4 W, 1% Resistor	Digi-Key 464BKX-ND
1	U1	XR-T6164 IC	EXAR
2	T1,2	Pulse Type 65535 Transformer	Pulse
2	J1,2	0.1" Bottom-Entry Board Connector, 8 Pin, Molex 22-17-3082 (Use 2 Sets for a 16 Pin Connector)	Digi-Key WM3228-ND
1		16 Pin IC Socket	Digi-Key ED-3316-ND

**Table 11. XR-T6164 LIU Daughter Board Parts List**

QTY	Reference	Description	Supplier
1	C1	0.1 µF, 63V, Z5U Dielectric, Axial lead, 0.1" Spacing	Digi-Key P4917
1	U1	XR-T6165 IC	EXAR
1		22 Pin IC Socket, 0.4" Spacing	Digi-Key ED-3422-ND

**Table 12. XR-T6165 Daughter Board Parts List**

QTY	Reference	Description	Supplier
1	C1	0.1 µF, 63V, Z5U Dielectric, Axial lead, 0.1" Spacing	Digi-Key P4917
1	U1	XR-T6166 IC	EXAR
1		28 Pin IC Socket, 0.6" Spacing	Digi-Key ED-3628-ND

**Table 13. XR-T6166 Daughter Board Parts List**

**Magnetic Supplier Information:**

Pulse  
 Telecom Product Group  
 P.O. Box 12235  
 San Diego, CA 92112  
 Tel. (619) 674-8100  
 Fax. (691) 674-8262

Transpower Technologies, Inc.  
 24 Highway 28, Suite 202  
 Crystal Bay, NV 89402-0187  
 Tel. (702) 831-0140  
 Fax. (702) 831-3521

**Notes**

**Notes**



**EXAR** *...the analog plus company<sup>TM</sup>*

EXAR Corporation

48720 Kato Road

Fremont, CA 94538

(510) 668-7000, Fax (510) 668-7017

Worldwide Web Site: <http://www.exar.com>

