PT8

Multi-standard Video Encoder

User Manual

Revision 0.9
9th July 2011

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Introduction

PT8 is a multi-standard video encoder supporting PAL-M/N/B/D/G/H/I and NTSC-M/J outputs.

The intellectual property block accepts BT656 formatted data, in either 8 or 10 bit format, with the associated 27MHz clock, and it encodes this data to a 10 bit, digital composite video signal, also at 27MHz, which can be used to directly drive a digital to analogue converter or other output device.

Control and status registers are written to and read from using a conventional 8 bit wide microprocessor interface.

The intellectual property block is provided as an encrypted 'black box' design for incorporation into an Altera FPGA, as a netlist for Xilinx FPGAs or as RTL compliant Verilog source code for FPGAs from other vendors or for ASICs. Typical resource usage for an Altera FPGA is shown in Table 1.

Logic Elements	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers
7601	12388	4	1	3

Table 1 PT8 Altera FPGA resource requirements

PT8 Module description

The PT8 encoder comprises 8 Verilog modules:

PT8_encoder.v
PT8_BT656_receiver.v
PT8_Chroma_modulator.v
PT8_output_proc.v
PT8_Register_control.v
PT8_SPG.v
PT8_Subcarrier_gen.v
PT8_ROM.v

PT8_encoder.v is the top level module of the hierarchy; six of the other modules are instantiated from it. The sin/cos lookup table, PT8_ROM.v, is called from PT8_Subcarrier_gen.v.

Signal Interconnections

The PT8 signal interconnect diagram is shown in Figure 1.

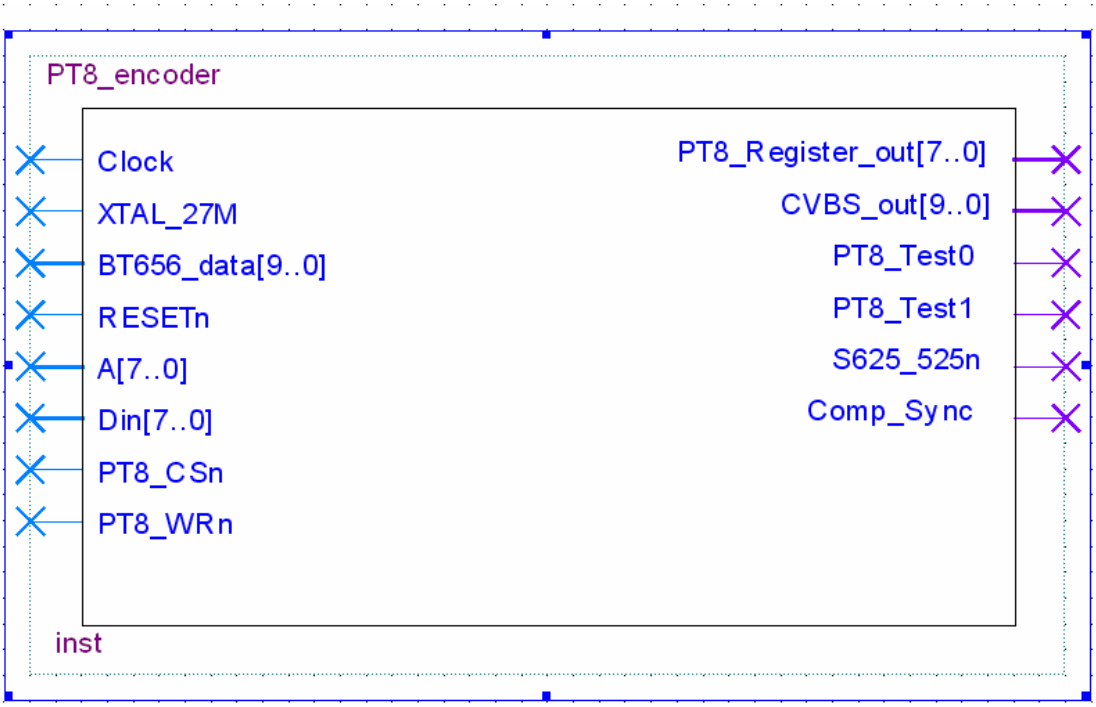

Figure 1 PT8 Interconnection diagram

The signal descriptions are shown in Table 2, below.

Signal	Description
Clock	27MHz clock input synchronous with the BT656 input data. The BT656 data should be stable at the rising edge of this clock.
XTAL_27M	Clock used for writing to the registers only. If 'Clock' is continuous and stable XTAL_27M may be connected to that input.
656_data[9..0]	BT656 compliant input data. If the input is 8-bit the bottom 2 bits should be connected to ground (logic '0').
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all regiisters.
A[7..0]	Control address bus input used to select the control register to be written to/read from.
Din[7..0]	Control data input bus.
PT8_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
PT8_WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers.
PT8_Register_out[7..0]	Control output data bus. Outputs the control/status register data selected by the A[7..0] bus.
CVBS_out[9..0]	The digital composite output. The output format is straight binary with bit 9 being the MSB. The output is valid on the rising edge of the Clock input.
PT8_Test0	Used in combination with control register 2 to select internal test signals.
PT8_Test1	Used in combination with control register 2 to select internal test signals.

S625_525	Output signal signifying the line standard currently selected for the PT8 encoder, (‘1’ = 625 line, ‘0’ = 525 line).
Comp_Sync	Composite sync signal output. (May be buffered and used with monitors that require separate sync inputs).

Table 2 Input/Output signals

The Verilog instantiation of PT8 is shown below:

```
// Instantiate Video encoder (PT8_encoder)

PT8_encoder PT8_encoder(.Clock(Clk_27M), .XTAL_27M(XTAL_27MHz),
                .BT656_data(BT656_data[9:0]), .RESETn(FPGA_RESETn),
                .A(PT8_A), .Din(PT8_Din), .PT8_CSn(PT8_CSn),
                .PT8_WRn(PT8_WRn),

                .PT8_Register_out(PT8_Register_out), .CVBS_out(CVBS_out[9:0]),
                .PT8_Test0(PT8_Test0), .PT8_Test1(PT8_Test1),
                .S625_525n(PT8_S625_525n), .Comp_Sync(Comp_Sync));
```

Signal Levels

The expected signal levels for the BT656 input are shown in Table 3, below.

10-bit YCbCr signal Levels 100/0/100/0			
	Y	**Cb**	**Cr**
White	940	512	512
Yellow	840	64	585
Cyan	678	663	64
Green	578	215	137
Magenta	426	809	887
Red	326	361	960
Blue	164	960	439
Black	64	512	512
10-bit YCbCr signal Levels 75/0/75/0			
	Y	**Cb**	**Cr**
White	940	512	512
Grey	721	512	512
Yellow	646	176	567
Cyan	525	625	176
Green	450	289	231
Magenta	335	735	793
Red	260	399	848
Blue	139	848	457
Black	64	512	512

Table 3 BT656 Signal Levels

The resulting nominal output levels for a 100% PAL colour bar input are shown in Figure 2.

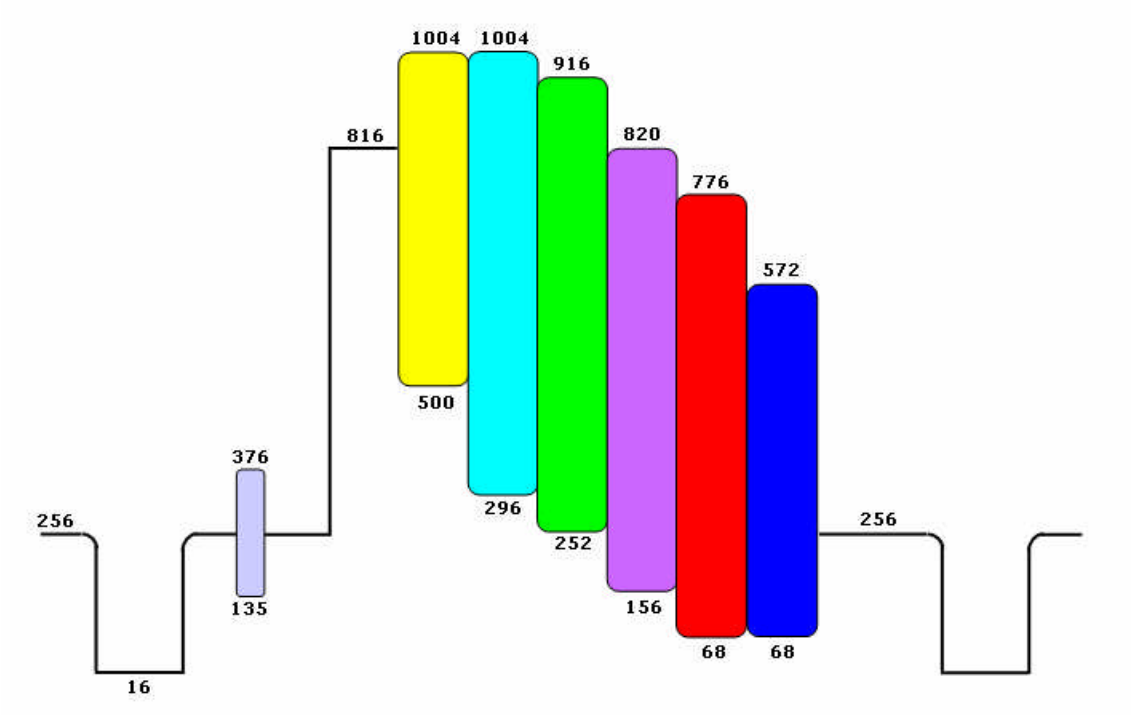

Figure 2 CVBS output levels

Test signals

The PT8 is supplied with BT656 test waveforms to facilitate testing and verification.

The waveforms are supplied as Excel spreadsheets and are 75% saturation colour bars. Other waveforms can be supplied to request for a small charge..

There are four elements to the complete frame of video and each element consists of 1716 (515 line) or 1728 (625 line) samples in a multiplexed Cb,Y,Cr,Y sequence. Each sample of each element should be clocked at 27MHz.

For 525 line the elements need to selected according to the following table:

Line No.s	Pattern	Element
4-19, 264, 265	F0V1	1
1-3, 266-282	F1V1	2
20-263	75% Bars F0	3
283-525	75% Bars F1	4

Table 4 BT656 525 line selection

For 625 lines the elements need to be selected according to Table 5.

Line No.s	Pattern	Element
1-22, 311, 312	Fsync F1	1
313-335, 624, 625	Fsync F2	2
23-310	75% Bars F1	3
336-623	75% Bars F2	4

Table 5 BT656 625 line selection

Technical Overview

A simplified block diagram of the PT8 PAL encoder is shown in Figure 3.

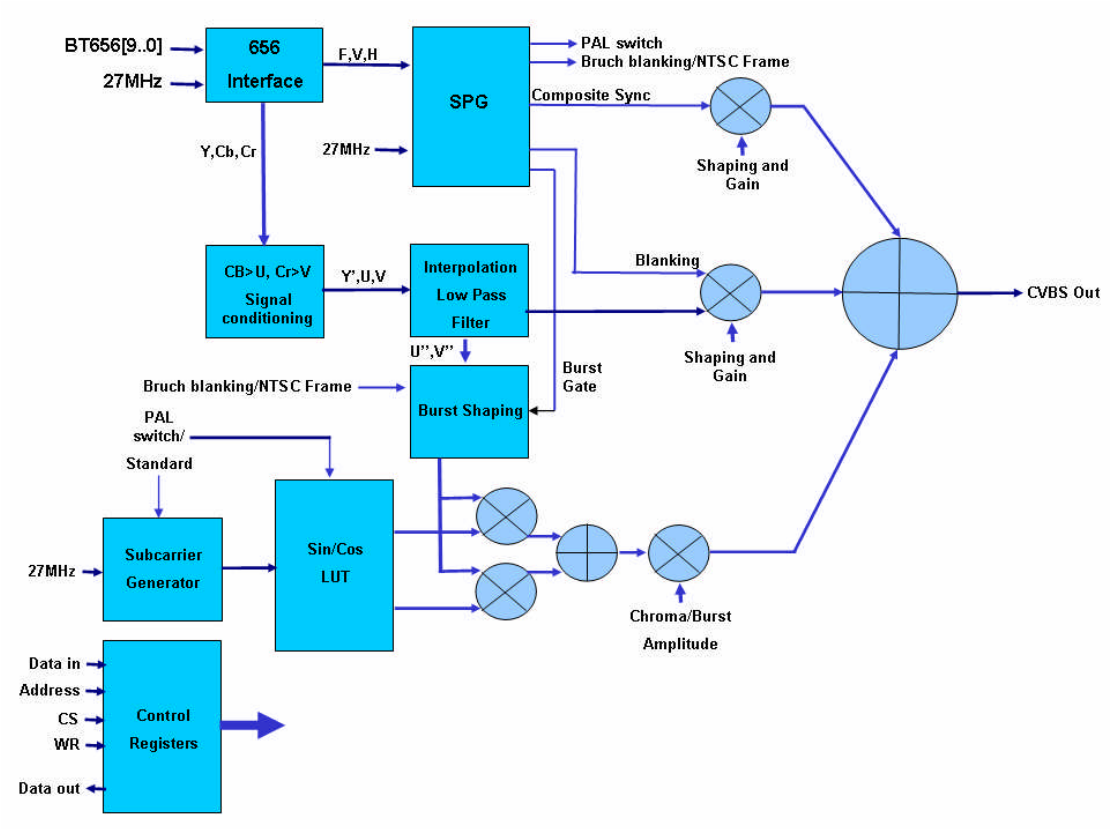

Figure 3 PT8 Block Diagram

The input to the encoder is an 8 or 10 bit BT656 formatted data stream and associated 27MHz clock. If the input is 8 bits the bottom 2 bits should be tied to logic '0'.

The 656 interface block identifies and extracts the TRS codes from the stream and demultiplexes and co-times the Y,Cb,Cr data. The TRS codes are also examined for the correct parity and if an error is found it is flagged and reported to the Status register.

The 27MHz clock and the frame and active video signals are used to synchronise a sync pulse generator (SPG). The principal purpose of the SPG is to generate a compatible composite sync output but it also generates the PAL switch signal (7.8kHz), the Bruch Blanking sequence for PAL burst blanking, the Burst gate signal for inserting the colour burst into the output data and the video blanking pulse.

The Y,Cb,Cr data is conditioned to produce Y,U,V signal amplitudes before being interpolated from 4:2:2 format to 8:8:8 format (27 MHz sample rate). The luminance and chrominance are interpolated using 47 tap FIR filters with a bandwidth of 5.5MHz for the luma and 1.5MHz for the chroma.

The 27MHz clock also drives a 32-bit ratio counter which generates a precise subcarrier frequency for the selected standard. An 11-bit phase word from this ratio counter addresses 12 bit wide Sin and Cos look-up tables. To save on memory only one quadrant of the Sin and Cos tables are stored and the addressing and data is modified to generate the other three quadrants.

The resulting Sin and Cos data is then multiplied by the U and V data during the active video period and a shaped Burst Gate pulse is used to insert the colour burst.

The colour frame output of the SPG ensures the burst is correctly inhibited whilst the PAL switch output of the SPG switches the 135deg and 225deg phase increments in the correct sequence. For NTSC it is possible to add in a phase offset (hue).

The resulting U.sin(2πfsc.t) and V.cos(2πfsc.t) data is added together to create the chrominance signal which has blanking added as well as programmable gain.

The interpolated luminance signal is also blanked (using a shaped clipping waveform) and has programmable gain added, whilst the composite sync signal has an approximation to a 2T wave shape added to ensure rise/fall time conformance to the video specification. The luminance, chrominance and composite sync are then added together to generate the final 10-bit 27MHz digital PAL encoded output.

The encoder can also be set to a freerun mode in which it ignores the BT656 timing information and data and uses the 27MHz clock input to generate a black and burst output.

The vertical blanking interval data may be selected to be stripped, passed flat, (Y channel only), or encoded as per the active video.

Control of the encoder is via a conventional 8 bit wide microprocessor bus. In addition status registers allow the monitoring of internal timing signals.

Two test outputs are also provided that may be programmed to monitor various internal signals.

Register interface

Figure 4 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via an 8 bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT8_CSn (chip select) input must be asserted low. Whilst this is low the PT8_WRn must be taken low. An internal write enable pulse is created at the next rising edge of the XTAL_27M clock and writing occurs at the next clock edge following that enable.

For the write to occur reliably the address (A[7:0]) and data (Din[7:0]) must be stable and valid during the PT8_WRn pulse. The minimum width of the PT8_WRn pulse is 80ns for a 27MHz clock.

The address input also selects the register data that is presented on the PT8_Register_out[7:0] bus. This output is independent of the other control signals or the Clk27 clock.

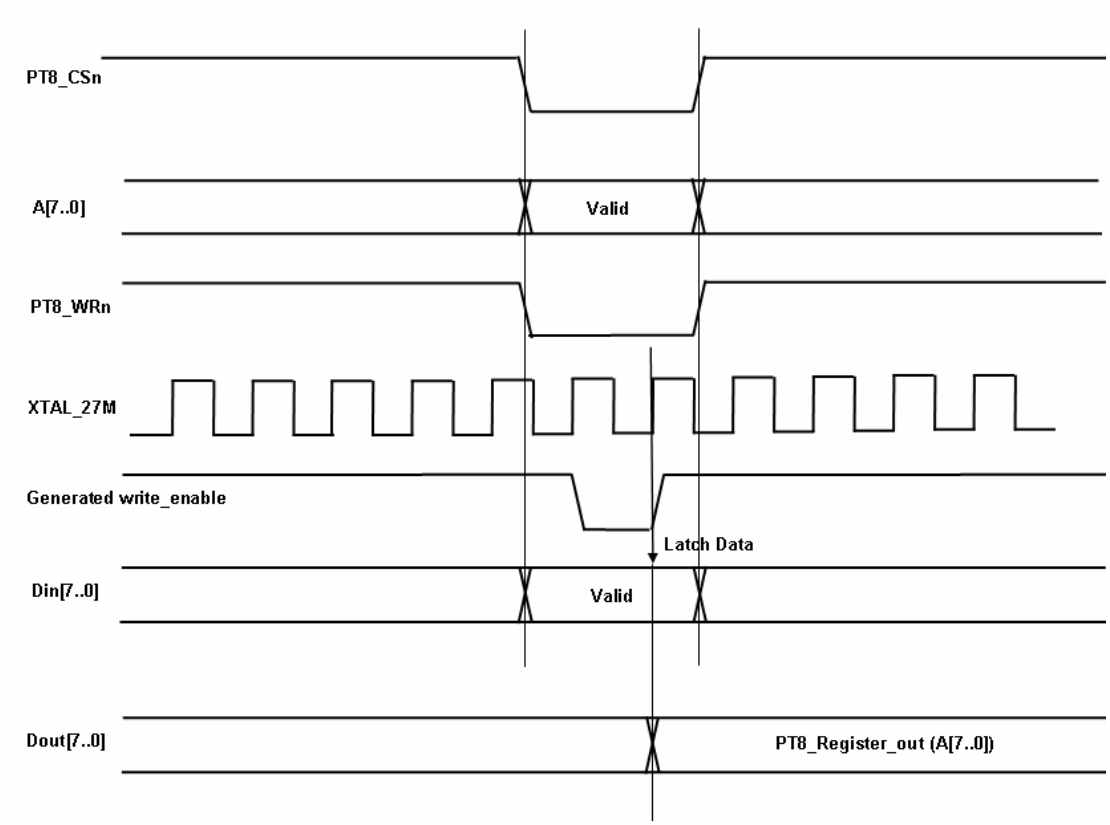

Figure 4 Control interface Timing

Register descriptions

Table 6 lists all of the control and status registers. All of the registers are 8 bit wide although some are concatenated together to create longer words. Unused register bits read back as zeros.

Note that, if Control Register bit 7 is asserted (Auto-standard = '1'), then the hard-wired values for NTSC-M or PAL-B/D/G will be used by PT8 depending on the line standard selected by Control Register 6 and only the Control registers will affect the PT8.

The hard-wired values are those shown in Table 7. The registers may still be written to and read from in Auto Standard condition.

Please note that some registers can be set to values that are illegal and will produce invalid outputs.

Refer to Figures 5 and 6 for details of the horizontal timing register settings.

Asserting the RESETn input sets the PT8 to Auto standard – NTSC-M and the registers are loaded with the default values for NTSC-M.

Register Offset	Register Name	R/W	Bit Value	Description			
$00	**Control 1**	R/W		Control Register			
			7	Auto standard. When set to '1' the hardwired values are used for PT8 control depending on the state of bit 6 (Line standard). When this bit is set to '0' the register values are used for PT8 control. (Default value = '1').			
			6	625 = '1', 525 = '0'	Bit 6	Bit 5	
			5	PALM/N = '1', NTSC/PAL = ,0'	0	0	NTSC-M/J (Default)
					0	1	PAL-M
					1	0	PAL
					1	1	PAL-N
			4-3	Not used			
	Interpolator[1]		1	If set to '1' the 2:1 interpolator is bypassed, else the interpolator is enabled. Note there is a 19ns Y/C delay error when the interpolator is bypassed. (Default value = '1').			
	Interpolator[0]		0	If set to '1' the interpolator is expecting an 18.9375MHz input clock, else a 27MHz input clock. (Default value = '0').			
$01	**Control 2**	R/W		PT8_Test 1/0 output selection			
			7	Not used			
			6	Not used			
			5	Bit 5	Bit 4	Bit 3	Test 1 output
			4	0	0	0	HBlank (Default)
			3	0	0	1	VBlank
				0	1	0	Bruch 1 ID
				0	1	1	Line 6
				1	0	0	Burst Gate
				1	0	1	Line 1
				1	1	0	Line 23
				1	1	1	Horizontal Sync
			2	Bit 2	Bit 1	Bit 0	Test 0 output
			1	0	0	0	Hcount[0] (Default)
			0	0	0	1	Hcount[1]
				0	1	0	Vcount[0]
				0	1	1	Vcount[1]
				1	0	0	Halfline
				1	0	1	PAL_switch
				1	1	0	Equalising
				1	1	1	Broad

Register Offset	Register Name	R/W	Bit Value	Description				
$02	**Control 3**	R/W		Control register				
	Y/C delay		7-4	Bit 7	Bit 6	Bit 5	Bit 4	
				0	0	0	0	0ns
				0	0	0	1	-185ns
				0	0	1	0	-148ns
				0	0	1	1	-111ns
				0	1	0	0	-74ns
				0	1	0	1	-37ns
				0	1	1	0	0ns (Default)
				0	1	1	1	+37ns
				1	0	0	0	+74ns
				1	0	0	1	+111ns
				1	0	1	0	+148ns
				1	0	1	1	+185ns
				1	1	0	0	0ns
				1	1	0	1	0ns
				1	1	1	0	0ns
				1	1	1	1	0ns
	Chroma_off		3	Turns off the colour modulator if set to '1' (monochrome output). (Default = '0')				
	VBI_encode		2	If 0 and VBI_Pass is 1 then the VBI information is pass 'flat' as described in VBI_Pass (Control 1 bit 1). If 1 and VBI_Pass is 1 the BT656 video data is encoded as per the active picture area. The gain control for Y is set by registers $2D and $2E. (Default = '0').				
	VBI_Pass		1	If 0 the vertical blanking is from lines 623.5-23.5 and lines 311-335 for PAL and lines 1-20 and 263.5-283.5 for NTSC. If 1 the vertical blanking is from lines 623.5-4.5 and 311-317 for PAL and lines 1-9 and 263.5-272 for NTSC. During the vertical VBI interval, lines 4.5-23.5 (9-20) and lines 317-335 (272-283.5) data on the BT656 Y input is passed to the output with a gain set by registers $2D and $2E. Data on the Cb and Cr inputs is blanked. (Default = '0').				
	Freerun		0	If '0' BT656 data is encoded. If '1' a free running Black and Burst is generated from the 27MHz clock. (Default = '0').				
Timing registers								
$03	**H Phase 1**	R/W		Delay between BT656 SAV and SPG horizontal counter. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (HPhase2[2:0],HPhase1[7:0]).				
$04	**H Phase 2**	R/W						
$05	**V Phase 1**	R/W		Delay between BT656 1>0 transition of FFlag and SPG vertical counter. Increments of horizontal lines. Maximum value =524 or 624 depending on the line standard. 10 bit value = (VPhase2[1:0],VPhase1[7:0]).				
$06	**V Phase 2**	R/W						
$07	**Active_picture_ start_1**	R/W		Start of the digital blanking. Value '0' is the first active pixel after the TRS SAV. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (Active_picture_start_2[2:0],Active_picture_start1[7:0]).				
$08	**Active_picture_ start_2**	R/W						
$09	**Active_picture_ end_1**	R/W		End of the digital blanking. Nominally set to 1440 active pictures for standard BT656 inputs. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (Active_picture_end_2[2:0],Active_picture_end1[7:0]).				
$0A	**Active_picture_ end_2**	R/W						
$0B	**H Sync start 1**	R/W		Delay between H Phase reset and start of horizontal sync pulse. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (HSyncstart2[2:0],HSyncstart1[7:0]).				
$0C	**H Sync start 2**	R/W						
$0D	**H Sync end 1**	R/W		Delay between H Phase reset and end of horizontal sync pulse. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). H Sync end – H Sync start * 1/27MHz is the horizontal sync pulse width, nominally 4.7us. 11 bit value = (HSyncend2[2:0],HSyncend1[7:0]).				
$0E	**H Sync end 2**	R/W						
$0F	**H blank start 1**	R/W		Delay between H Phase reset and start of horizontal blanking. Increments of 1/27MHz Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (Hblankstart2[2:0],Hblankstart1[7:0]).				
$10	**H blank start 2**	R/W						

Register Offset	Register Name	R/W	Bit Value	Description
$11	**H blank end 1**	R/W		Delay between H Phase reset and end of horizontal blanking. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). H blank end – H blank start * 1/27MHz is the blanking width, nominally 52us. 11 bit value = (Hblankend2[2:0],Hblankend1[7:0]).
$12	**H blank end 2**	R/W		
$13	**Pedestal start 1**	R/W		Delay between H Phase reset and start of pedestal insertion (for 525 line standards only). Increments of 1/27MHz Maximum value = 1715. 11 bit value = (Pedestalstart2[2:0],Pedestalstart1[7:0]).
$14	**Pedestal start 2**	R/W		
$15	**Pedestal end 1**	R/W		Delay between H Phase reset and end of pedestal insertion (for 525 line standards only). Increments of 1/27MHz. Maximum value = 1715. Pedestal end – Pedestal start * 1/27MHz is the pedestal insertion pulse width, nominally 52us. 11 bit value = (Pedestalend2[2:0],Pedestalend1[7:0]).
$16	**Pedestal end 2**	R/W		
$17	**Half line start 1**	R/W		Position of the half line = 32us, referenced to H Phase reset. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). 11 bit value = (Halflinestart2[2:0],Halflinestart1[7:0]). Half line end is H Sync start position.
$18	**Half line start 2**	R/W		
$19	**Equalising1 end 1**	R/W		Width of the first equalizing pulse whose leading edge is HSyncstart. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). HSync start – Equalising 1 end * 1/27MHz is the equalizing pulse width, nominally 2.35us. 11 bit value = (Equalising1end2[2:0],Equalising1end1[7:0])
$1A	**Equalising1 end 2**	R/W		
$1B	**Equalising2 end 1**	R/W		Width of the second equalizing pulse whose leading edge is Half line start. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). Halfline start – Equalising 2 end * 1/27MHz is the equalizing pulse width, nominally 2.35us. 11 bit value = (Equalising2end2[2:0],Equalising2end1[7:0])
$1C	**Equalising2 end 2**	R/W		
$1D	**Broad1 end 1**	R/W		Width of the first broad pulse whose leading edge is HSyncstart. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). HSync start – Broad1 end * 1/27MHz is the broad pulse width, nominally 27.3us. 11 bit value = (Broad1end2[2:0],Broad1end1[7:0])
$1E	**Broad1 end 2**	R/W		
$1F	**Broad2 end 1**	R/W		Width of the second broad pulse whose leading edge is Half line start. Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). Halfline start – Broad 2 end * 1/27MHz is the equalizing pulse width, nominally 27.3us. 11 bit value = (Broad2end2[2:0],Broad2end1[7:0])
$20	**Broad2 end 2**	R/W		
$21	**Burst gate start 1**	R/W		Beginning of the burst gate signal Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively).. Burst gate nominally starts 5.64us after Hsync start. 11 bit value = (Burstgatestart2[2:0],Burstgatestart1[7:0])
$22	**Burst gate start 2**	R/W		
$23	**Burst gate end 1**	R/W		End of the burst gate signal Increments of 1/27MHz. Maximum value = 1715 or 1727 depending on the line standard (525 or 625 respectively). Width of burst gate pulse = Burstgatestart-Burstgateend * 1/27MHz, nominally 2.25us. 11 bit value = (Burstgatestart2[2:0],Burstgatestart1[7:0])
$24	**Burst gate end 2**	R/W		
$25	**FSc1**	R/W		LSB of the 32 bit subcarrier seed word.
$26	**FSc2**	R/W		The subcarrier seed word is calculated by the formula: FSc/27MHz * 2^32. For example for NTSC (FSc = 3.5795455) seed = 569408550_{10} or $21F07C26_{16}$. (FSc4=$21, FSc3=$F0, FSc2=$7C, FSc1=$26).
$27	**FSc3**	R/W		
$28	**FSc4**	R/W		MSB of the 32 bit subcarrier seed word.
$29	**NTSC Hue 1**	R/W		Hue control for NTSC output only. 11 bit value = (NTSCHue2[2:0],NTSCHue1[7:0]). 1 LSB = 0.176deg.
$2A	**NTSC Hue 2**	R/W		
Proc-amp control				
$2B	**Sync Scaling 1**	R/W		Output composite sync level, nominally Sync scaling = 256 results in sync output between 16 (sync bottom) and 256 (sync top). 9 bit value = (SyncScaling2[0],SyncScaling1[7:0]).
$2C	**Sync Scaling 2**	R/W		
$2D	**Burst Scaling 1**	R/W		Burst amplitude.

Register Offset	Register Name	R/W	Bit Value	Description
$2E	**Burst Scaling 2**	R/W		9 bit value = (BurstScaling2[0],BurstScaling1[7:0]).
$2F	**UV Scaling 1**	R/W		Output chrominance level. 11 bit value = (UVScaling2[2:0],UVScaling1[7:0]).
$30	**UV Scaling 2**	R/W		
$31	**Sync Offset 1**	R/W		Offset value for the CVBS output, effectively the level of the sync bottom. 9 bit value = (SyncOffset2[0],SyncOffset1[7:0]).
$32	**Sync Offset 2**	R/W		
$33	**VBI Scaling 1**	R/W		Scaling between BT656 Y data and composite Y output, applied during the VBI interval. 10 bit value = (VBIScaling2[1:0],VBIScaling1[7:0]).
$34	**VBI Scaling 2**	R/W		
$35	**Y Pedestal**	R/W		Pedestal added during active video period (NTSC-M and PAL-M only).
$36	**Y Offset 1**	R/W		Value to be subtracted from the BT656 luma input, normally value 64 (10 bit value). 9 bit value = (YOffset2[0],YOffset1[7:0]).
$37	**Y Offset 2**	R/W		
$38	**Luma Scaling 1**	R/W		Scaling between BT656 Y data and composite Y output, applied during the active picture area, nominally 560/940 * 1023. 10 bit value = (LumaScaling2[1:0],LumaScaling1[7:0]).
$39	**Luma Scaling 2**	R/W		
$3A	**Cb Scaling 1**	R/W		Scaling between BT656 Cb data and U nominally 0.493 * 511. 9 bit value = (CbScaling2[0],CbScaling1[7:0]).
$3B	**Cb Scaling 2**	R/W		
$3C	**Cr Scaling 1**	R/W		Scaling between BT656 Cr data and V nominally 0.877 * 511. 9 bit value = (CrScaling2[0],CrScaling1[7:0]).
$3D	**Cr Scaling 2**	R/W		
$3E	**CVBS gain 1**	R/W		Composite video gain (used for matching to output stage). 9 bit value = (CVBSgain2[0],CVBSgain1[7:0]).
$3F	**CVBS gain 2**			
				Status
$4E	**Parity error**	R		Parity error count from BT656 receiver (number of parity errors per frame: limited at maximum value 255).
$4F	**Version No.**	R	$05	IP core version number.

Table 6 Register descriptions

Horizontal timing registers

Figures 5 and 6 show the timing requirements for NTSC and PAL-BG respectively.

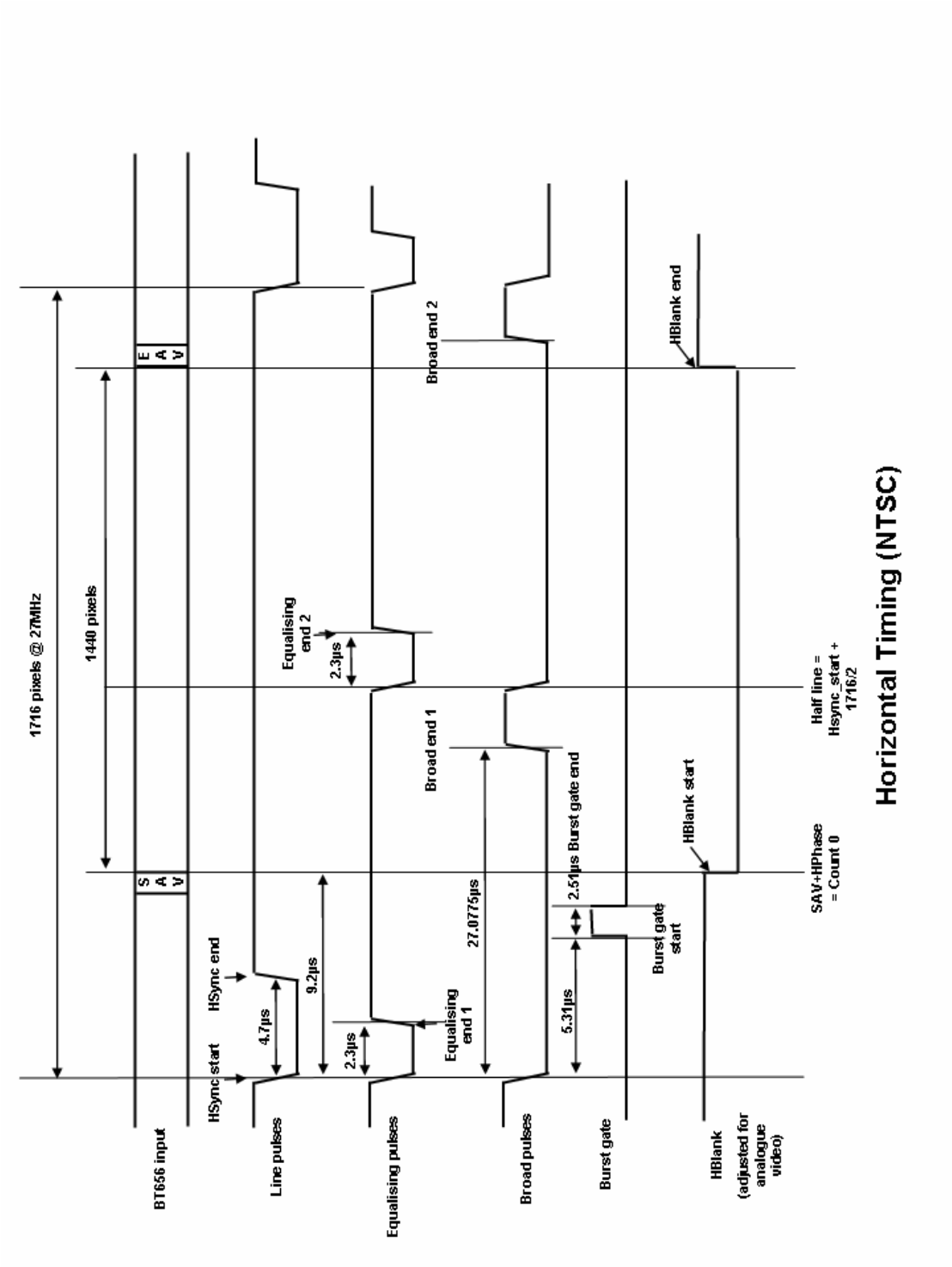

Figure 5 NTSC horizontal timing

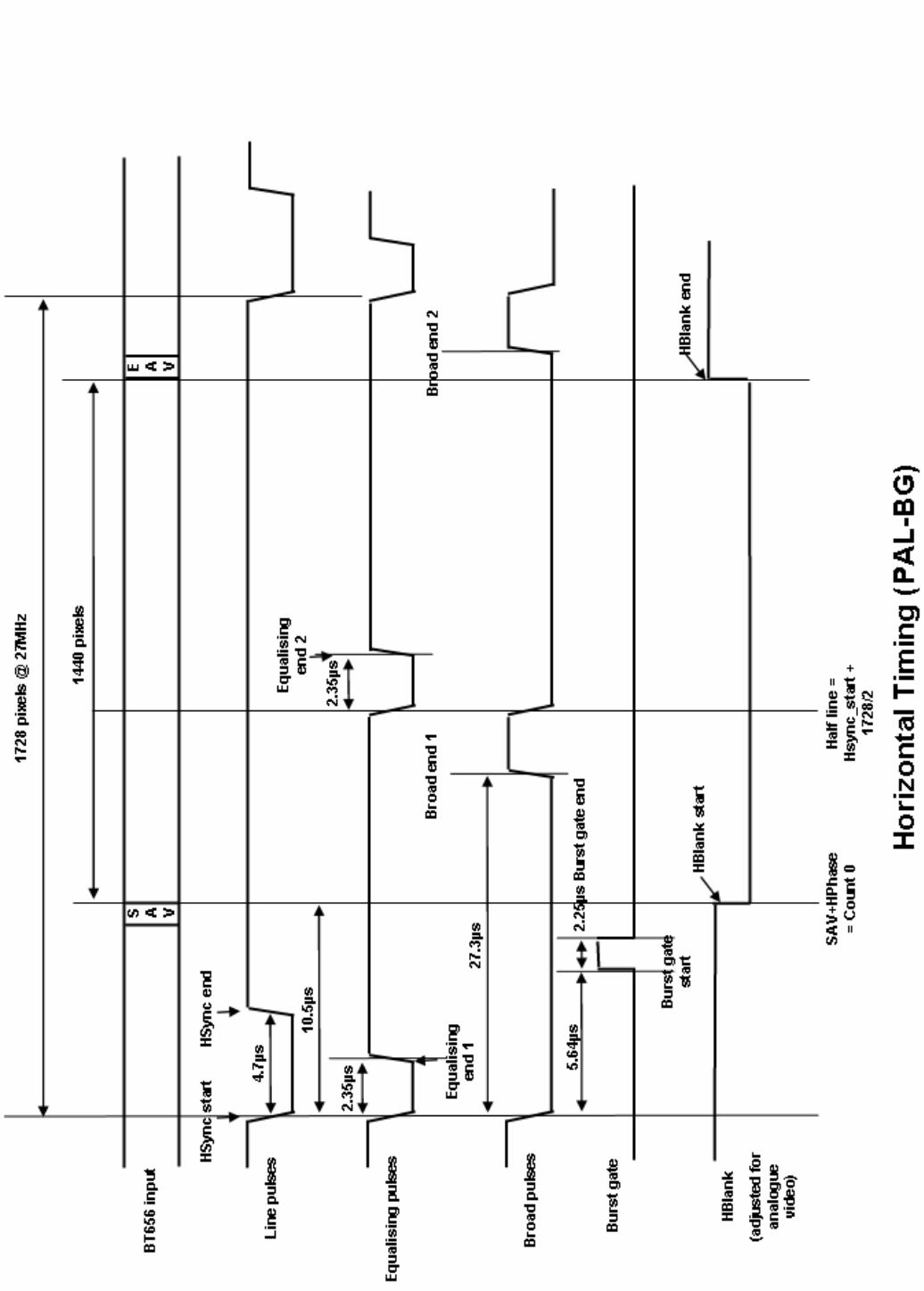

Figure 6 PAL-BG horizontal timing

Default Register Settings

Table 7 shows the default register settings (in hexadecimal) for the video standards supported by PT8. On assertion of RESETn the NTSC-M standard settings are loaded into the registers.

Note that, if Control Register bit 7 is asserted (Auto-standard = '1'), then the hard-wired values for NTSC-M or PAL-B/D/G will be used by PT8 depending on the line standard selected by Control Register 6. The hard-wired values are those shown in Table 7.

Also note that, for the 525 line standard, the horizontal timing values 'wrap' at 1715_{10} ($6B3) and the vertical values at 524_{10} ($20C). For the 625 line standard, the horizontal timing values 'wrap' at 1727_{10} ($6BF) and the vertical values at 624_{10} ($270).

Register Offset	Register Name	PAL-B/D/G	PAL-I	PAL-N	PAL-M	NTSC-M	NTSC-J	Comments
$00	Control 1	$40	$40	$60	$20	$00	$00	
$01	Control 2	$00	$00	$00	$00	$00	$00	
$02	Control 3	$60	$60	$60	$60	$60	$60	
Timing registers								
$03	H Phase 1	$2A	$2A	$2A	$2A	$2A	$2A	
$04	H Phase 2	$00	$00	$00	$00	$00	$00	
$05	V Phase 1	$6E	$6E	$6E	$07	$07	$07	
$06	V Phase 2	$02	$02	$02	$02	$02	$02	
$07	Active_picture_start 1	$00	$00	$00	$00	$00	$00	
$08	Active_picture_start 2	$00	$00	$00	$00	$00	$00	
$09	Active_picture_end1	$A0	$A0	$A0	$A0	$A0	$A0	
$0A	Active_picture_end2	$05	$05	$05	$05	$05	$05	
$0B	H Sync start 1	$B5	$B5	$B5	$B5	$B5	$B5	
$0C	H Sync start 2	$05	$05	$05	$05	$05	$05	
$0D	H Sync end 1	$34	$34	$34	$34	$34	$34	
$0E	H Sync end 2	$06	$06	$06	$06	$06	$06	
$0F	H blank start 1	$14	$14	$14	$04	$04	$04	
$10	H blank start 2	$00	$00	$00	$00	$00	$00	
$11	H blank end 1	$CA	$CA	$CA	$97	$97	$97	PAL-I front porch is 1.65µs
$12	H blank end 2	$05	$05	$05	$05	$05	$05	
$13	Pedestal start 1	$14	$14	$14	$04	$04	$04	
$14	Pedestal start 2	$00	$00	$00	$00	$00	$00	
$15	Pedestal end 1	$CA	$CA	$CA	$97	$97	$97	
$16	Pedestal end 2	$05	$05	$05	$05	$05	$05	
$17	Half line start 1	$58	$58	$58	$5E	$5E	$5E	
$18	Half line start 2	$02	$02	$02	$02	$02	$02	
$19	Equalising1 end 1	$F8	$F8	$F8	$F8	$F8	$F8	
$1A	Equalising1 end 2	$05	$05	$05	$05	$05	$05	
$1B	Equalising2 end 1	$98	$98	$98	$98	$98	$98	
$1C	Equalising2 end 2	$02	$02	$02	$02	$02	$02	
$1D	Broad1 end 1	$D9	$D9	$D9	$D9	$D9	$D9	
$1E	Broad1 end 2	$01	$01	$01	$01	$01	$01	
$1F	Broad2 end 1	$1B	$1B	$1B	$1B	$1B	$1B	
$20	Broad2 end 2	$05	$05	$05	$05	$05	$05	
$21	Burst gate start 1	$52	$52	$49	$49	$49	$49	
$22	Burst gate start 2	$06	$06	$06	$06	$06	$06	
$23	Burst gate end 1	$8F	$8F	$8D	$8D	$8D	$8D	
$24	Burst gate end 2	$06	$06	$06	$06	$06	$06	
$25	FSc1	$CB	$CB	$46	$D5	$26	$26	
$26	FSc2	$8A	$8A	$94	$EF	$7C	$7C	
$27	FSc3	$09	$09	$F6	$E6	$F0	$F0	
$28	FSc4	$2A	$2A	$21	$21	$21	$21	

Register Offset	Register Name	PAL-B/D/G	PAL-I	PAL-N	PAL-M	NTSC-M	NTSC-J	Comments
$29	NTSC Hue 1	$00	$00	$00	$00	$00	$00	
$2A	NTSC Hue 2	$00	$00	$00	$00	$00	$00	
Proc-amp control								
$2B	Sync Scaling 1	$86	$86	$86	$9E	$9E	$9E	
$2C	Sync Scaling 2	$00	$00	$00	$00	$00	$00	
$2D	Burst Scaling 1	$48	$48	$48	$54	$54	$54	
$2E	Burst Scaling 2	$00	$00	$00	$00	$00	$00	
$2F	UV Scaling 1	$8C	$8C	$8C	$1F	$1F	$1F	
$30	UV Scaling 2	$03	$03	$03	$04	$04	$04	
$31	Sync Offset 1	$08	$08	$08	$08	$08	$08	
$32	Sync Offset 2	$00	$00	$00	$00	$00	$00	
$33	VBI Scaling 1	$3F	$3F	$3F	$80	$80	$80	
$34	VBI Scaling 2	$01	$01	$01	$10	$10	$10	
$35	Y Pedestal	$00	$00	$00	$18	$18	$00	The pedestal register only operates for 525 line standards
$36	Y Offset 1	$40	$40	$40	$40	$40	$40	
$37	Y Offset 2	$00	$00	$00	$00	$00	$00	
$38	Luma Scaling 1	$3E	$3E	$3E	$8E	$8E	$9A	
$39	Luma Scaling 2	$01	$01	$01	$01	$01	$01	
$3A	Cb Scaling 1	$60	$60	$60	$5C	$5C	$5C	
$3B	Cb Scaling 2	$01	$01	$01	$01	$01	$01	
$3C	Cr Scaling 1	$E8	$E8	$E8	$EA	$EA	$EA	
$3D	Cr Scaling 2	$01	$01	$01	$01	$01	$01	
$3E	CVBS gain 1	$1B	$1B	$1B	$75	$75	$75	
$3F	CVBS gain 2	$03	$03	$03	$02	$02	$02	

Table 7 Default Register settings

Interfacing to a DAC

The 10-bit digital composite output and the 27MHz clock can directly drive a suitably fast DAC. Figure 7 shows the digital to analogue (DAC) interface that was used for the measurements at the end of the user manual.

Only the top part of the schematic is relevant for the PT8. The DACs used are Analog Devices AD9765 which are dual 12 bit DACs. For the PT8 only the top ten bits should be connected to the CVBS out of the PT8, the bottom 2 bits are then connected to ground.

The Verilog code to use both DACs (the second DAC can be copy of the CVBS information as in this example or other synchronous output video such as the Y component output) is shown below.

```
//          Output DACs
//          Format output to AD9765 DACs

// PT8 output stage
always @ (negedge Clk_54M or negedge RESETn) begin
  if (!RESETn) begin
            pb_pr <= 10'd0;
            cvbs_y <= 10'd0;
            end
            else if (DAC_clk) begin
  cvbs_y <= PT8_CVBS_out[9:0];
                      pb_pr <= 10'd0;
  end
  else begin
  cvbs_y <= PT8_CVBS_out[9:0];
                      pb_pr <= 10'd0;
            end
end

assign dac_iqwrt = Clk_54M;
assign dac_iqclk = Clk_54M;
assign dac_iqsel = DAC_clk;
          assign dac_reset = 1'b0;

always @ (negedge Clk_54M or negedge RESETn) begin
            if (!RESETn) begin
  DAC_clk <= 1'b0;
            end
            else begin
  DAC_clk <= Clk_27M;
            end
end
```

The 54MHz is a 2x version of the 27MHz with the rising edges aligned. If the second DAC is not to be used then the DAC can be clocked with 27MHz and the dac_iqsel is connected to ‘0’ or ‘1’ depending on the DAC to be used.

The current output of the DAC is connected to a resistor to convert it to a voltage and fed to a buffer amplifier, the Analog Devices ADA4412. This device provides a 2x gain so we can drive a series 75Ω resistor for the correct termination and also provides a high performance low pass filter to reconstitute the DAC output and remove out of band components. Resistors VR1 and VR3 provide nominal gain adjustment for the 2 DACs.

Note that the PT8 has no sinx/x correction as it has 27MHz over-sampling on its output. However there is a small droop in the output above 4.8MHz. The over-sampling filters have a bandwidth of 5.5MHz (luma channel) but a small analogue compensation circuit could be needed if the full 5.5MHz flatness is to be achieved.

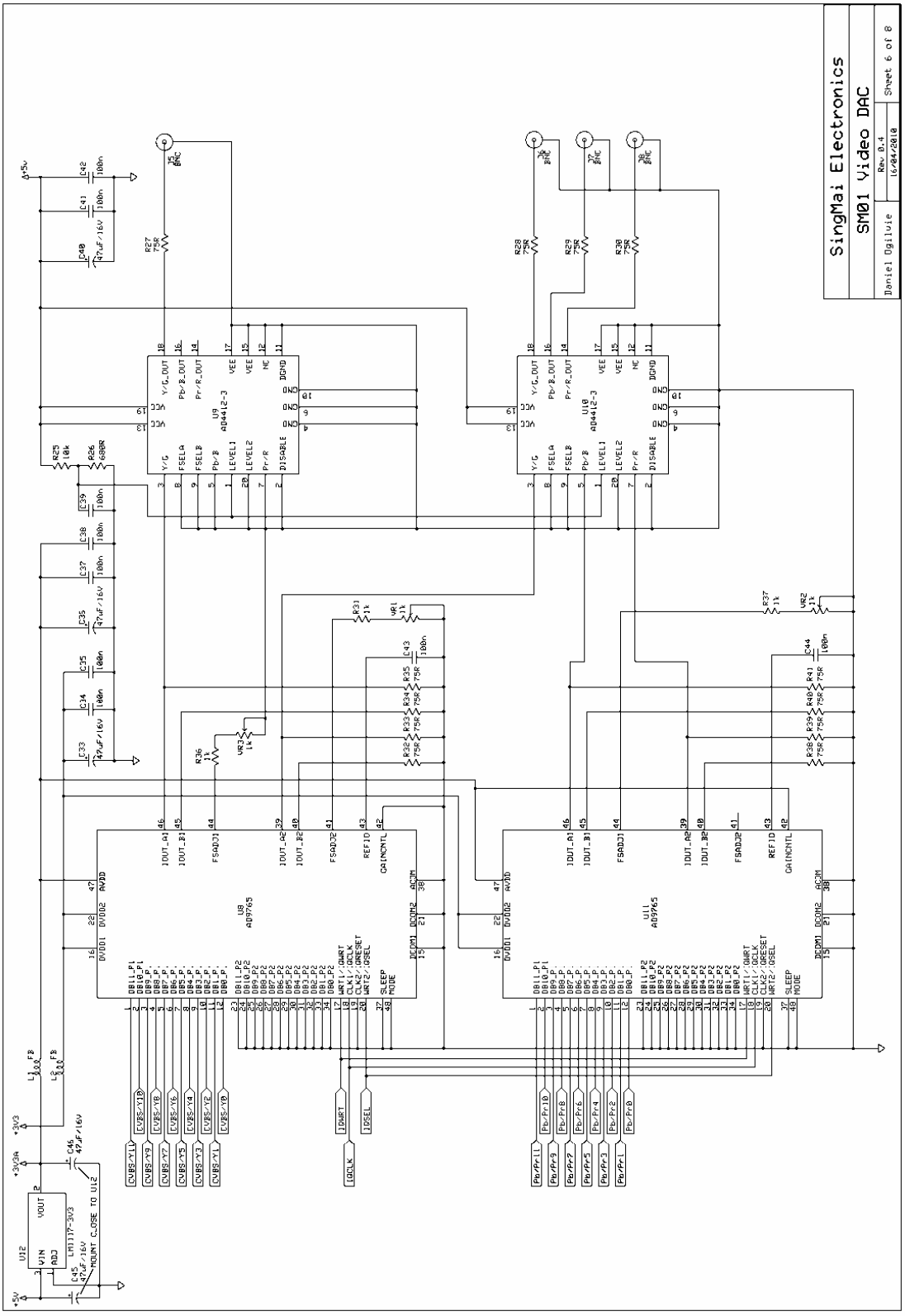

Figure 7 Interfacing to a DAC: Example schematic

Specification

Parameter	Specification		Comments
	PAL B,D,G,H,I,K,N	NTSC-M/J, PAL-M	
Frame Rate/Field Rate	25Hz/50Hz	30Hz/60Hz	
Line Period	64us	63.555555us	
Lines/Frame	625	525	
Line Blanking Interval	12us	10.7us	
Front Porch	1.5us	1.5us	1.65us for PAL-I
Line sync pulse width	4.7us	4.7us	
Back Porch	5.8us	4.5us	
Equalising Pulse width	2.35us	2.3us	
Broad Pulse width	27.3us	27.0775us	
Rise/Fall times of sync edges	250ns	250ns	NTSC/PAL-M rise time should be 140ns and PAL-I rise times should be 250ns
Sync Pulse amplitude	300mV	40IRE	
Luminance white bar amplitude	700mV	100IRE	
Vertical Sync Group	7.5 lines	9 lines	
No. of equalizing pulses	5 + 5	6 + 6	
Chrominance Phase error	<1deg	<1.5deg	
Subcarrier Frequency	4.43361875MHz (PAL) 3.58205625MHz (PAL-N)	3.5795455MHz (NTSC) 3.5756118MHz (PAL-M)	
Colour Frame duration	8 fields	4 fields	8 fields for PAL-M
Burst start	5.64us	5.31us	5.3us for PAL-N
Burst duration	2.25us	2.51us	2.51us for PAL-N
Burst Amplitude	300mV	40IRE	
Differential Gain	<1%	<1%	Sin x/x corrected
Differential Phase	<1deg	<1deg	Sin x/x corrected
K Factor (2T)	<1%	<1%	
Chrominance luminance delay	< +/- 10ns	< +/- 10ns	
Signal to Noise ratio	-65dB (black input), -58dB (luma ramp).	-65dB (black input), -58dB (luma ramp).	Unweighted

Table 8 PT8 Specifications

Measurements

The PT8 multistandard encoder was measured using a Altera Cyclone III development board (with 3C55 FPGA). The source was the PT6 video pattern generator IP core which provided the 10-bit BT656 input to the PT8 encoder.
The composite digital output was converted to analogue using an Analog Devices AD9765 12 bit digital to analogue converter (top 10 bits driven). The output from the DAC was amplified and filtered using an ADA4412 amplifier (with the bandwidth set to 36MHz) and the composite measurements were performed on a Tektronix VM700 measurement set.

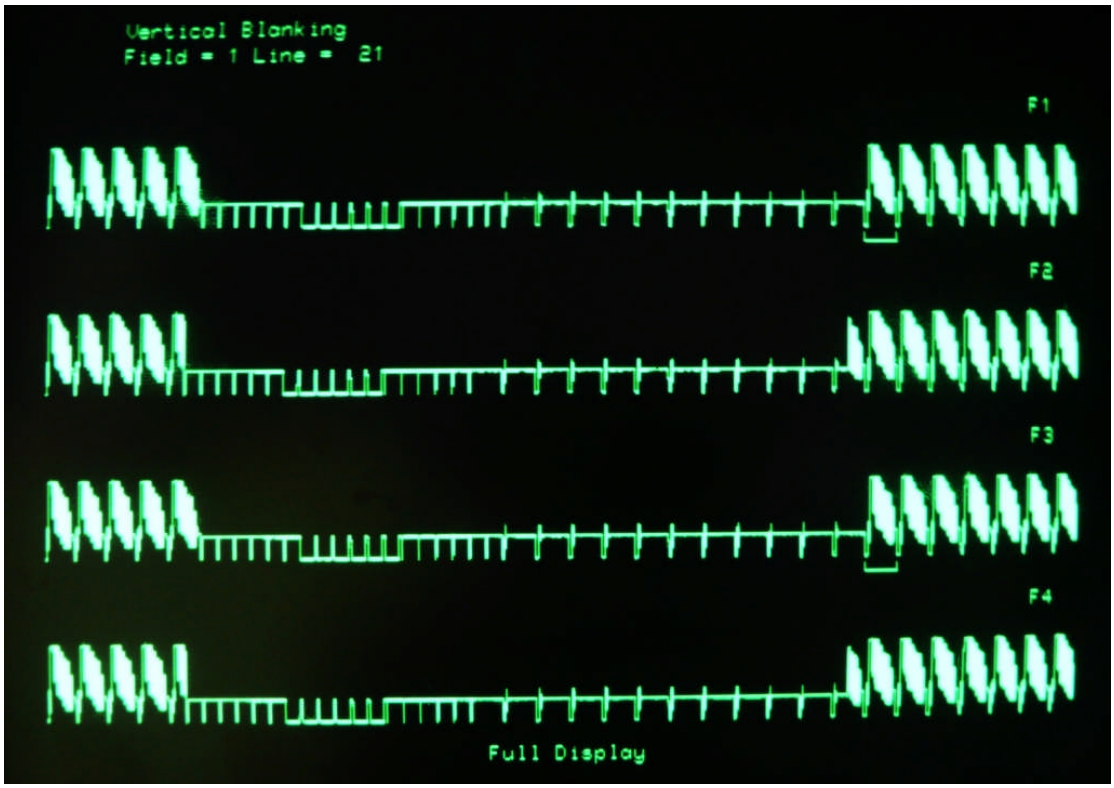

Figure 8 NTSC Vertical blanking interval

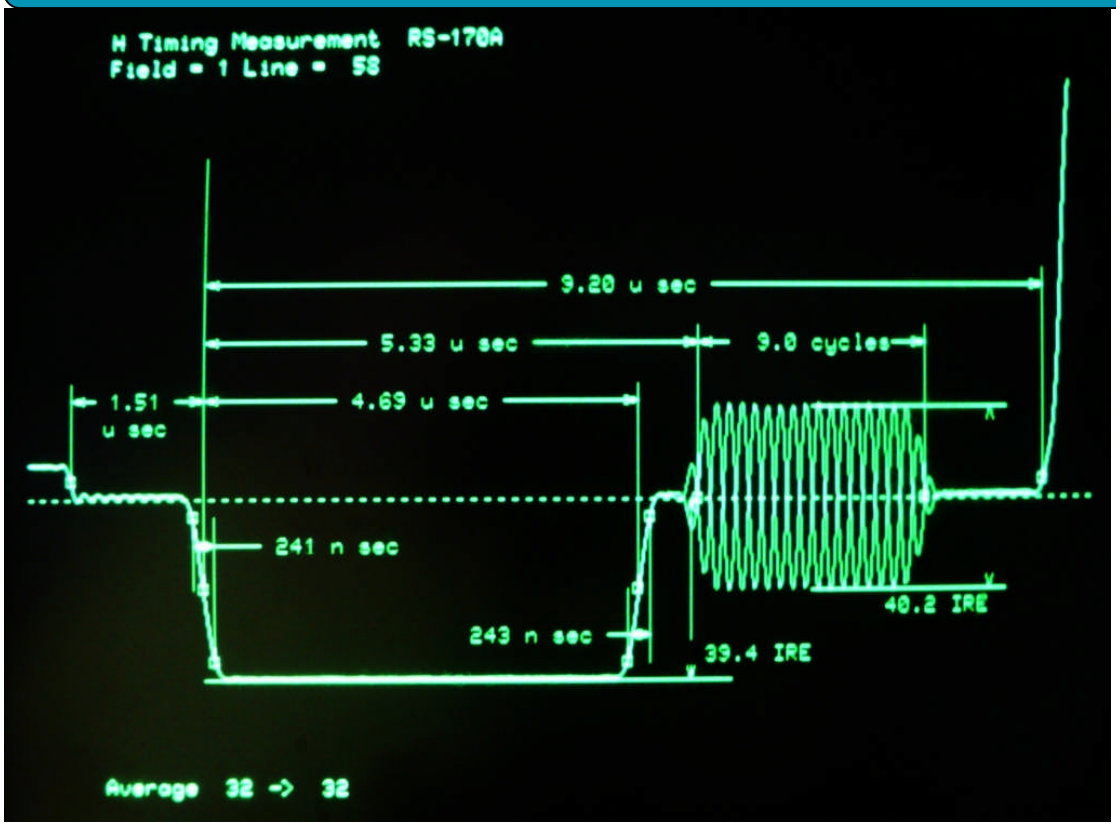

Figure 9 NTSC Horizontal Timing

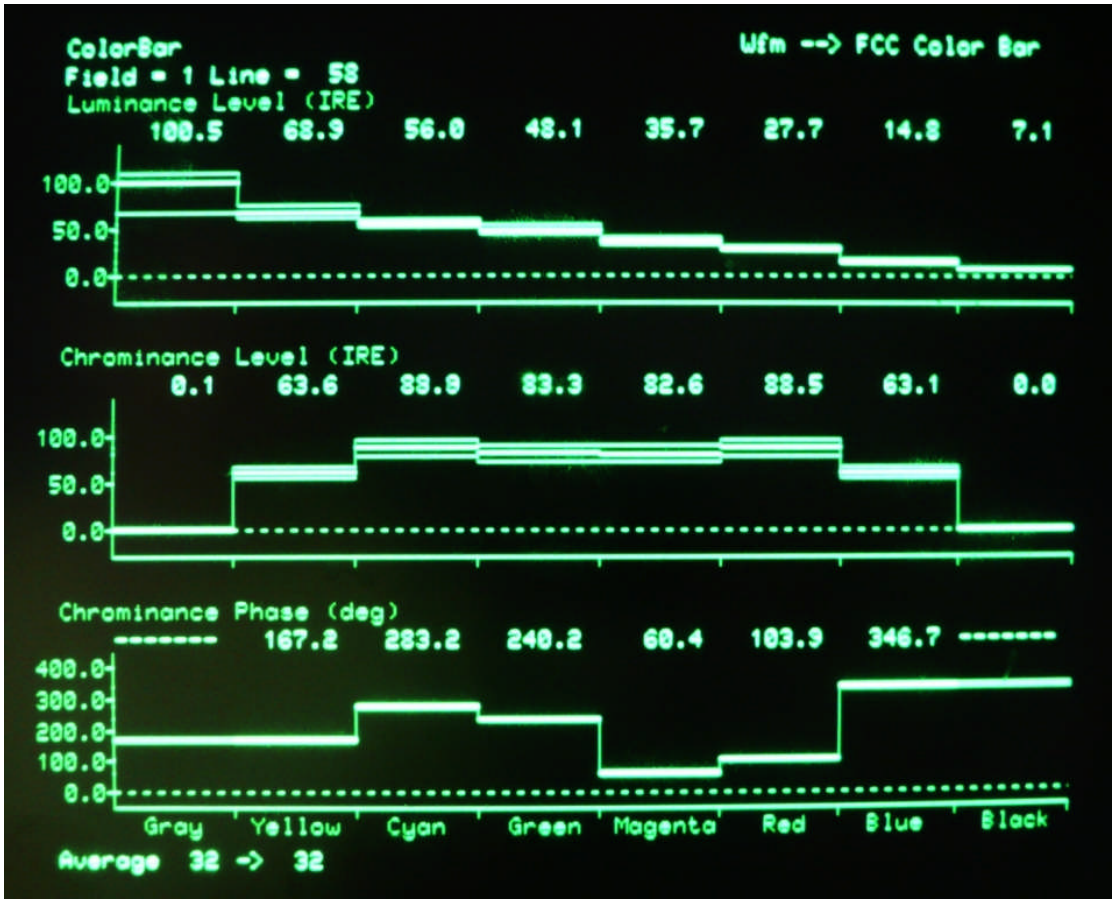

Figure 10 NTSC 75% Colour bar

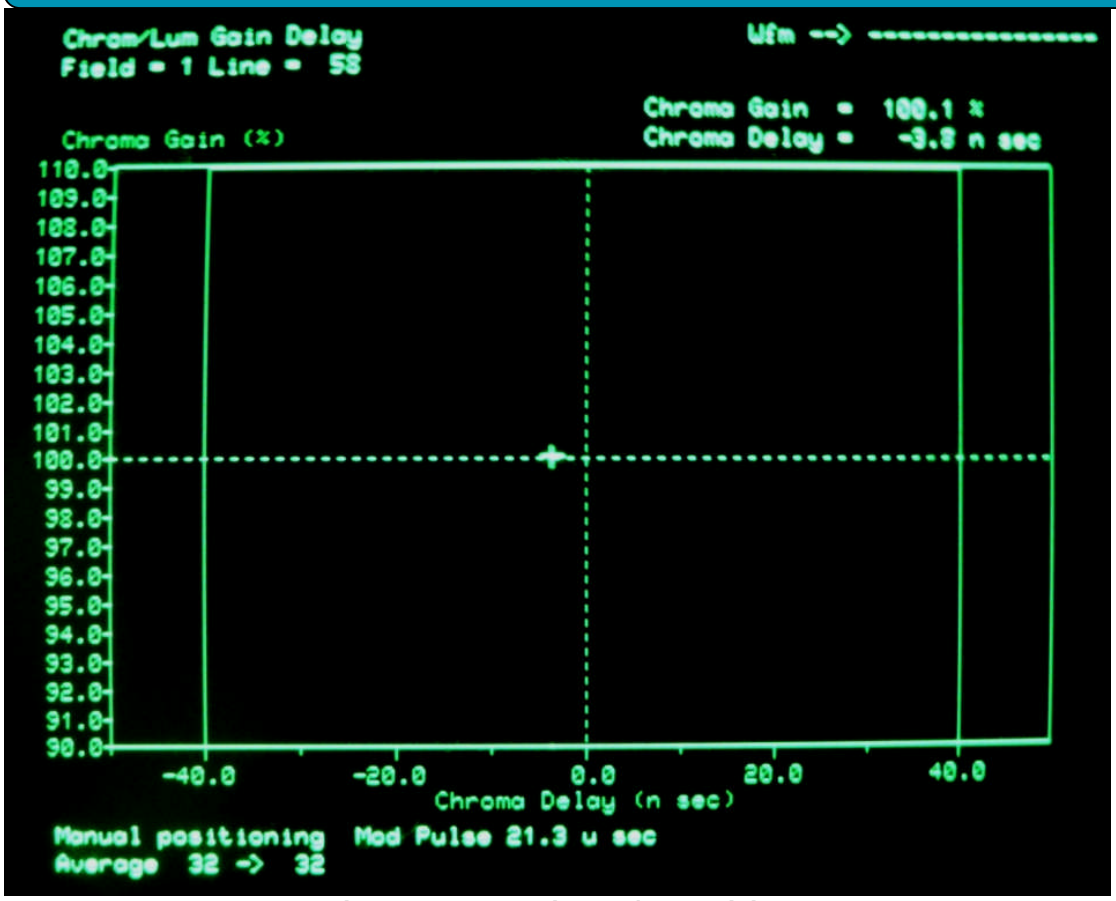

Figure 11 NTSC Chroma/Luma delay

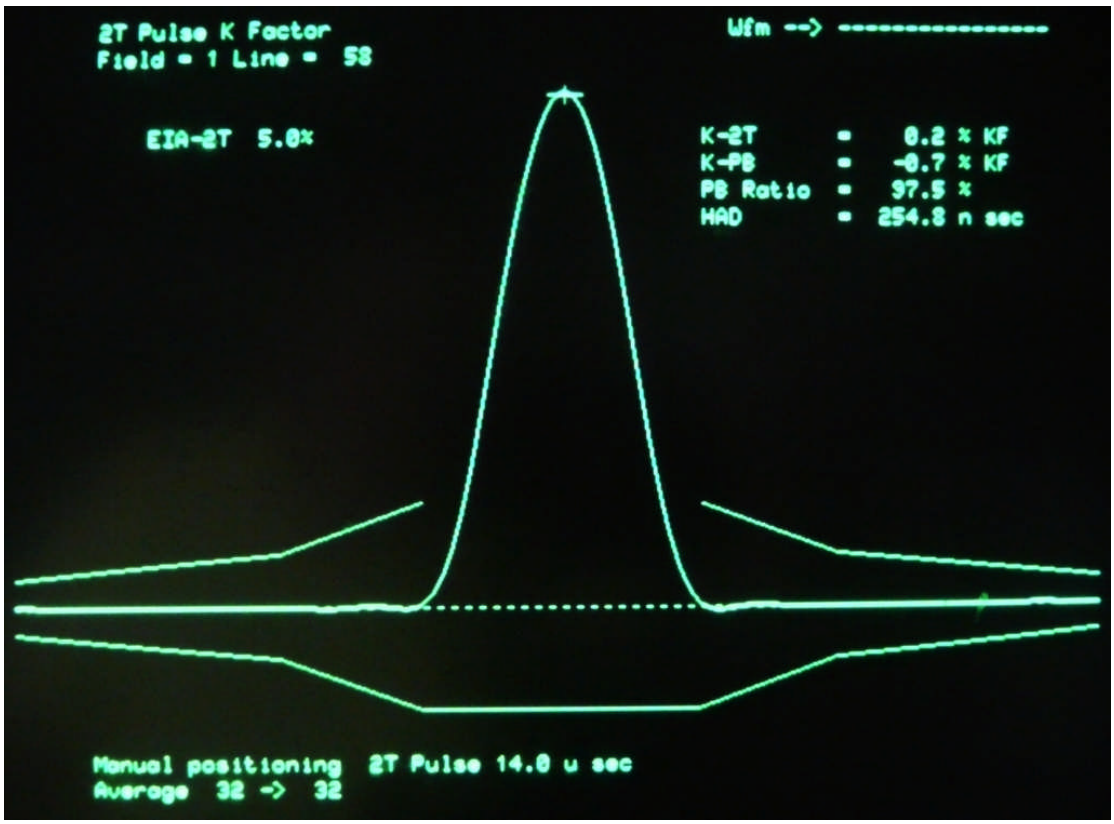

Figure 12 NTSC K Factor

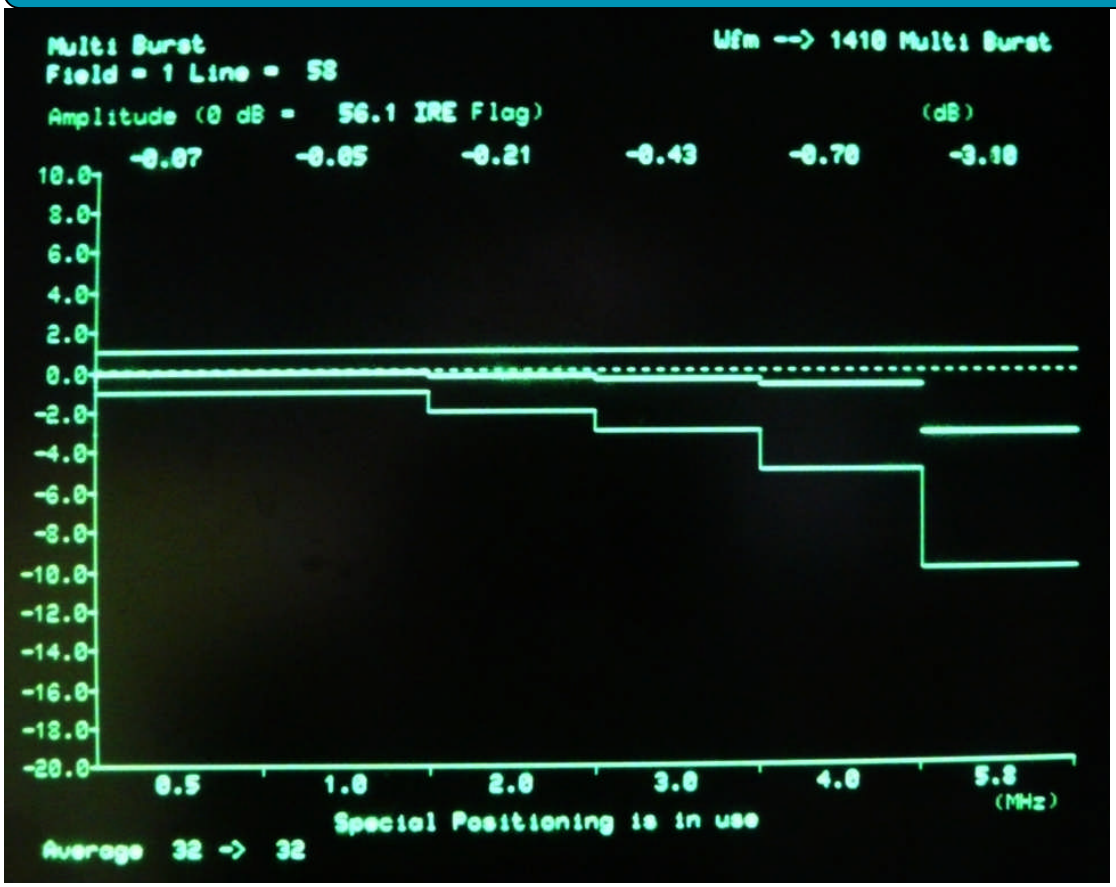

Figure 13 NTSC Multiburst (No sinx/x correction)

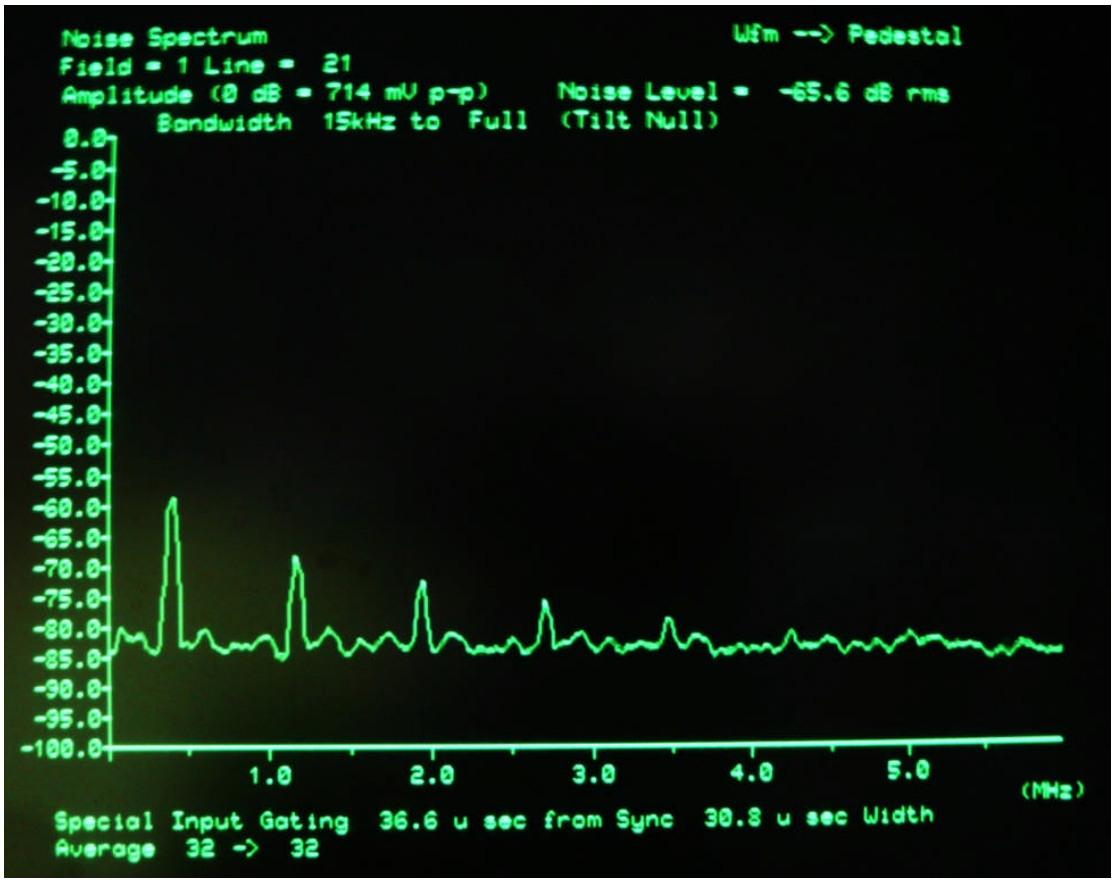

Figure 14 NTSC Noise Spectrum (Black)

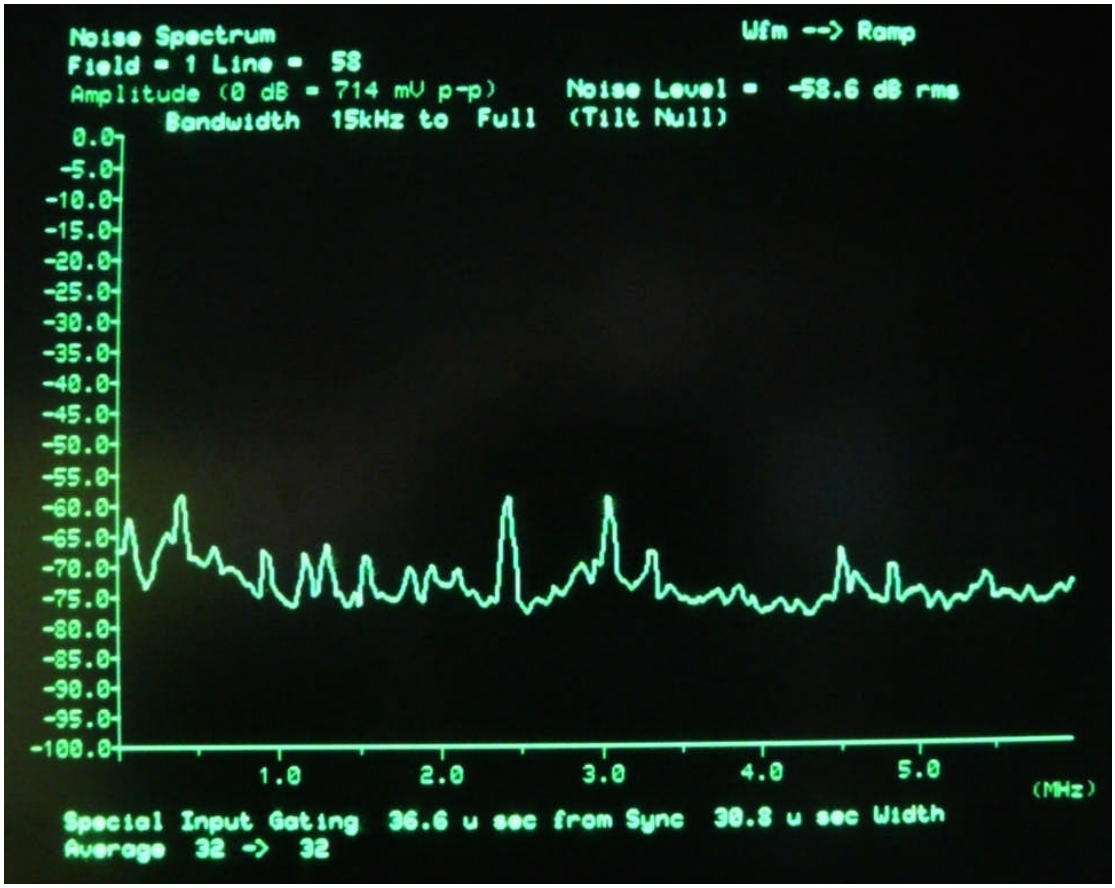

Figure 15 NTSC Noise Spectrum (luma ramp)

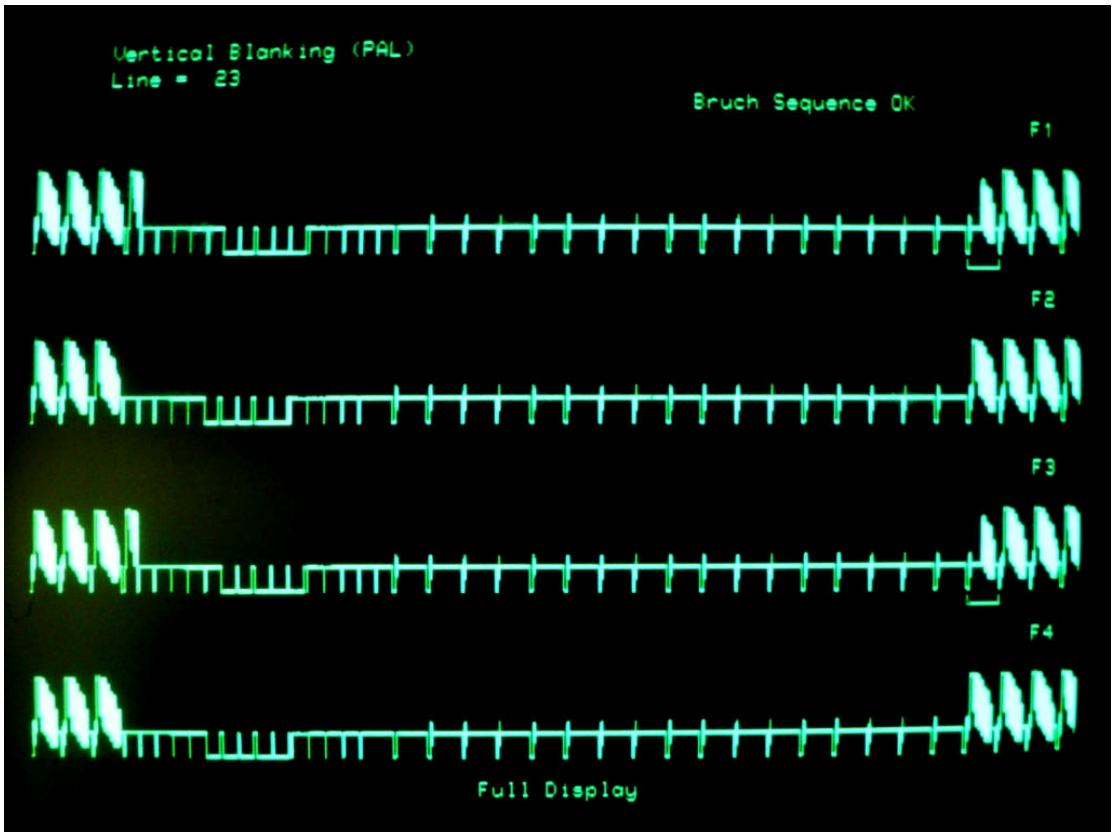

Figure 16 PAL Vertical blanking interval

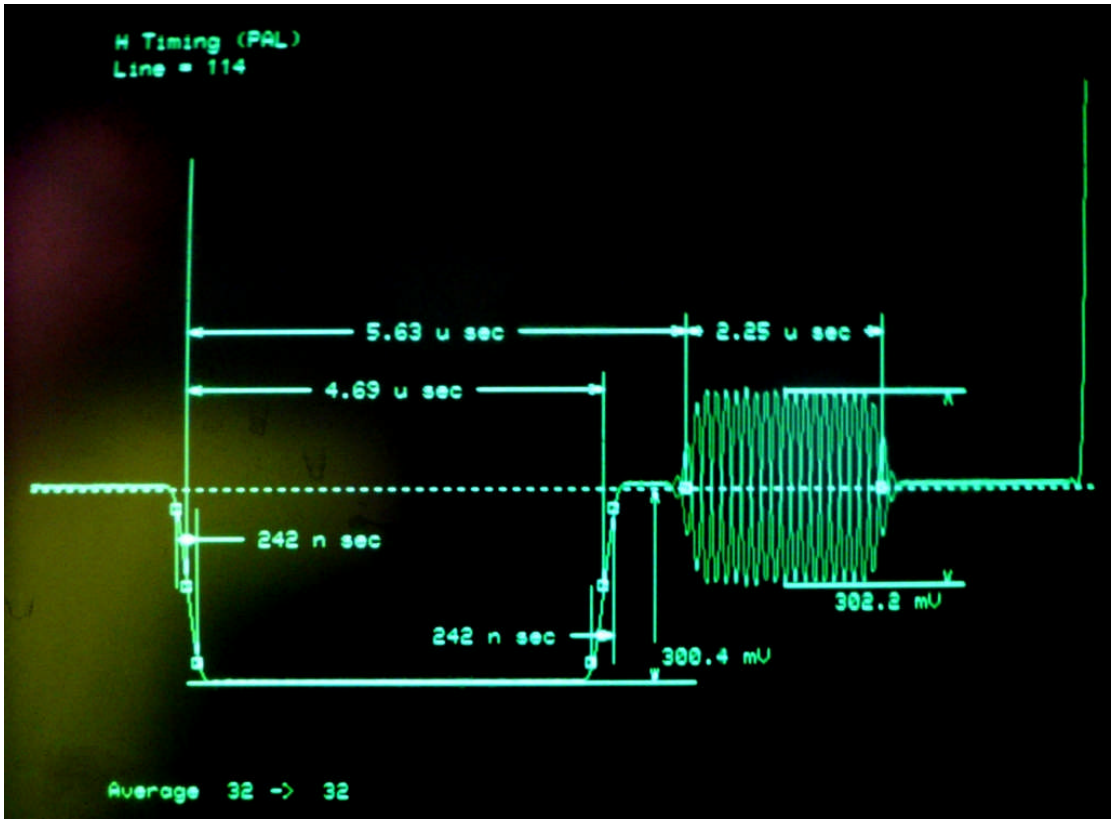

Figure 17 PAL Horizontal timing

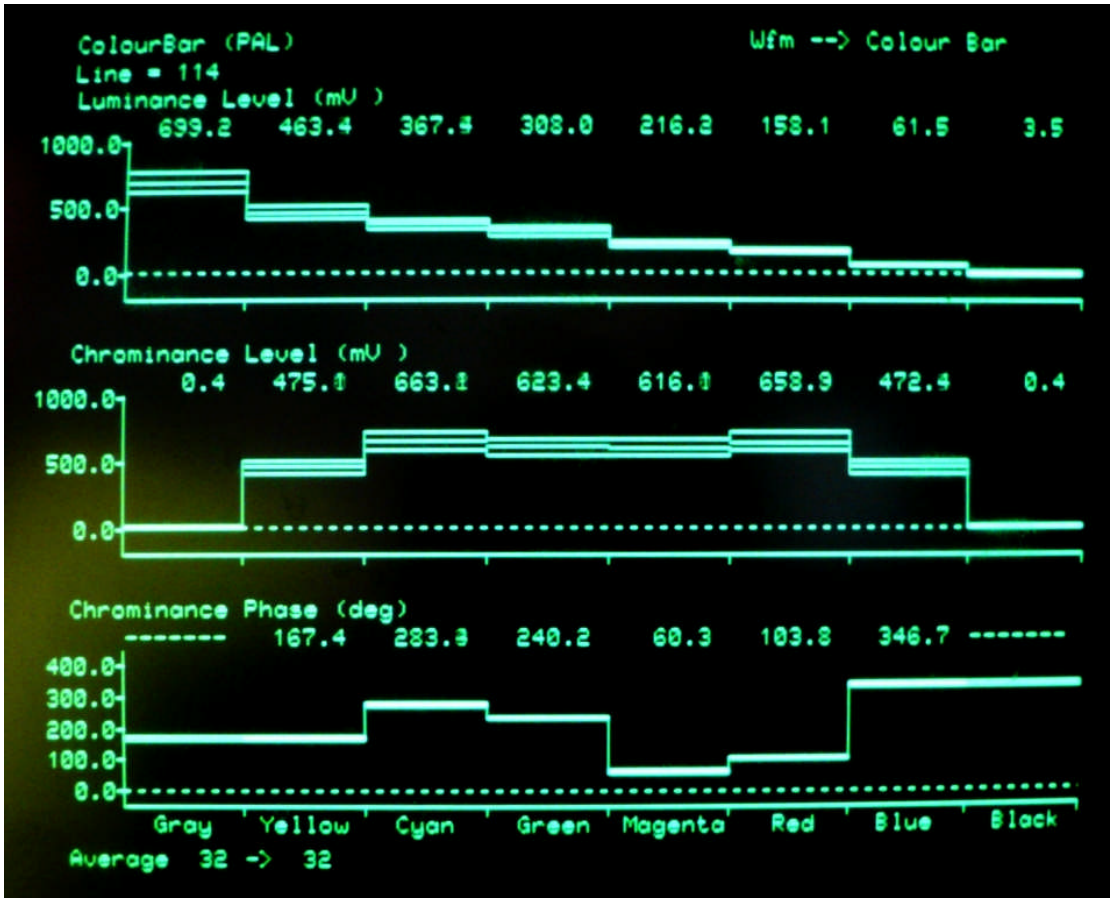

Figure 18 PAL 75% Colour bars

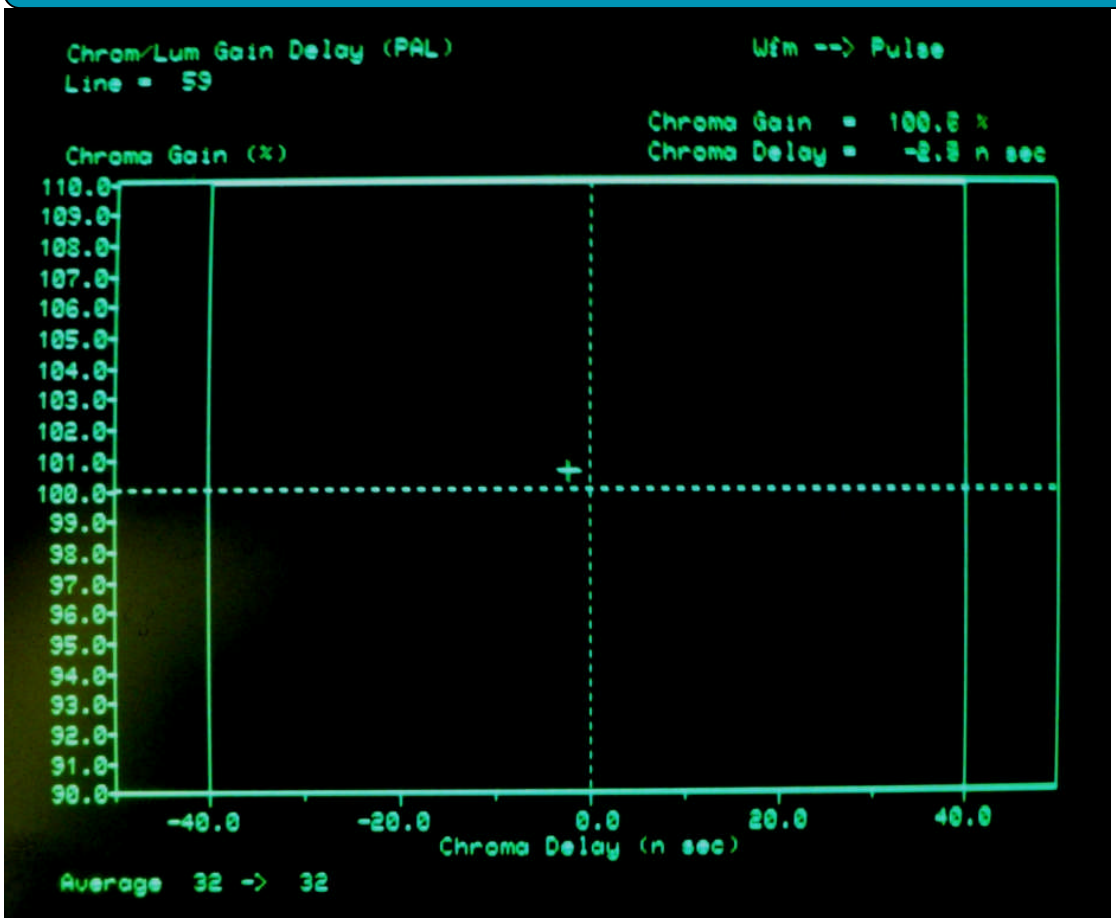

Figure 19 PAL Chroma/Luma delay

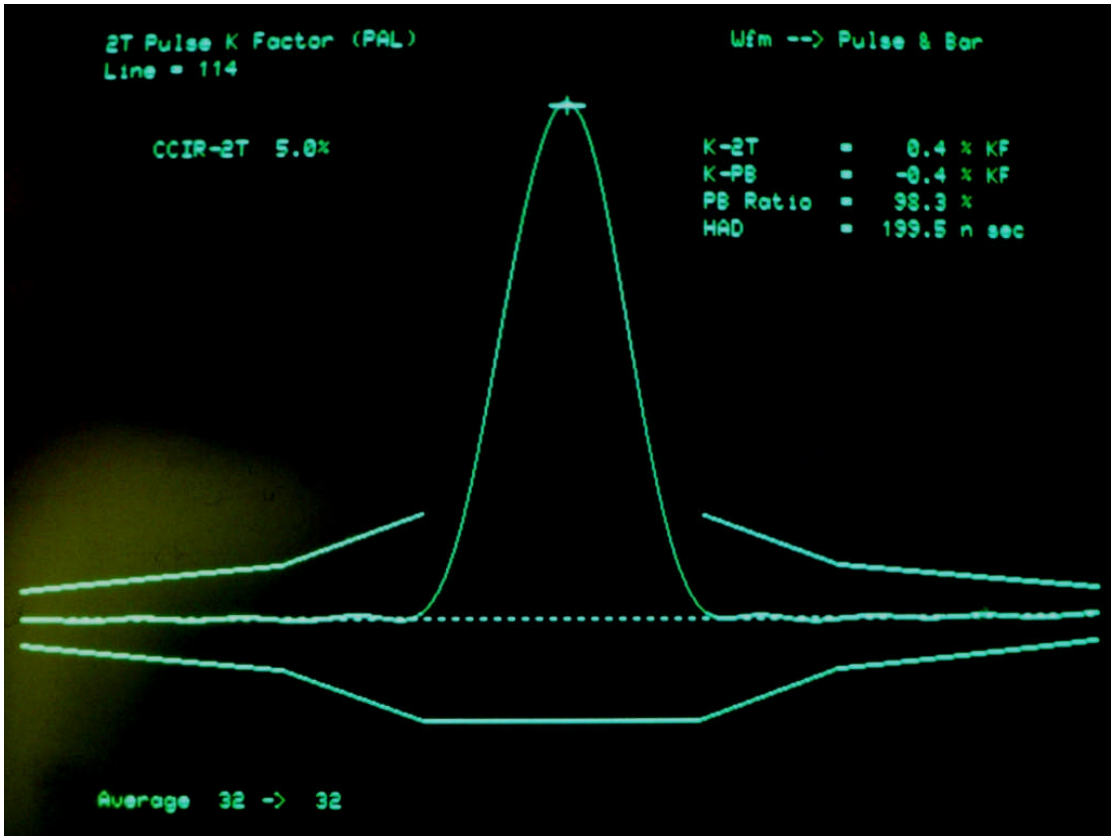

Figure 20 PAL K-factor

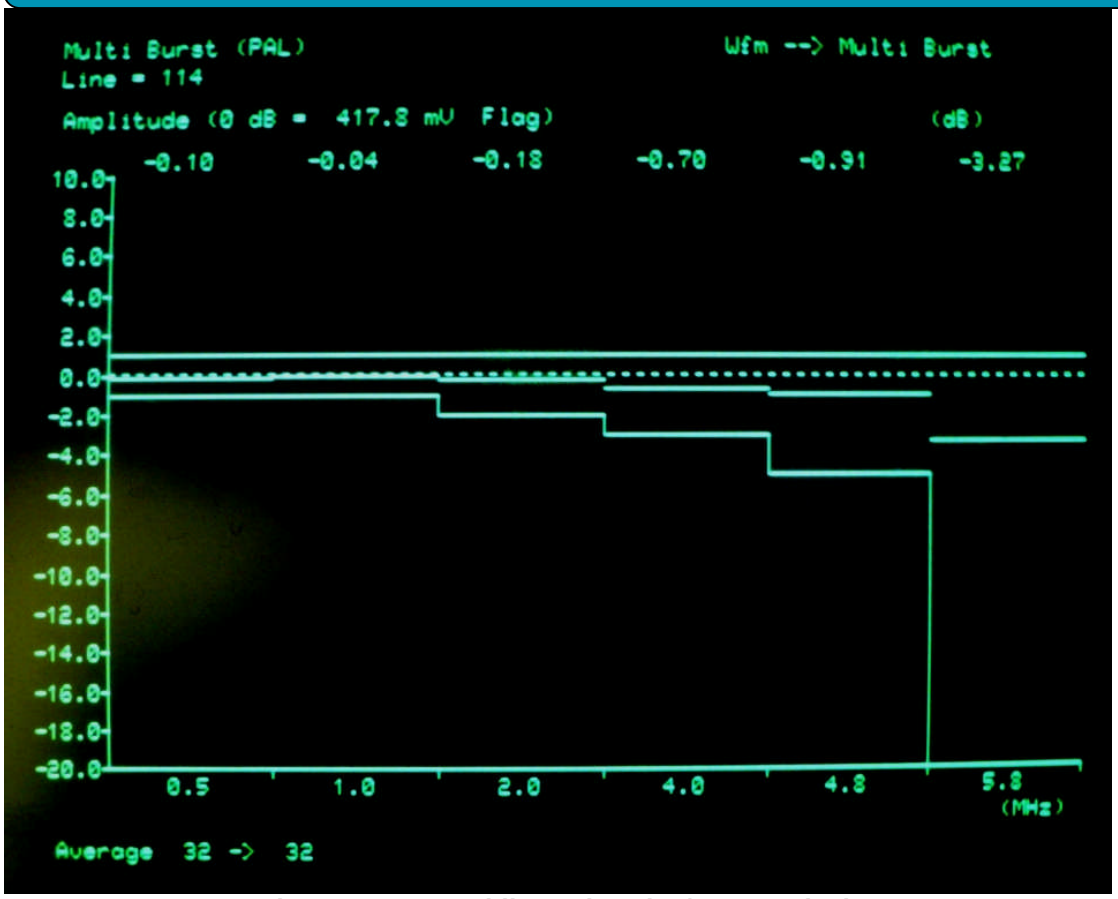

Figure 21 PAL Multiburst (no sinx/x correction)

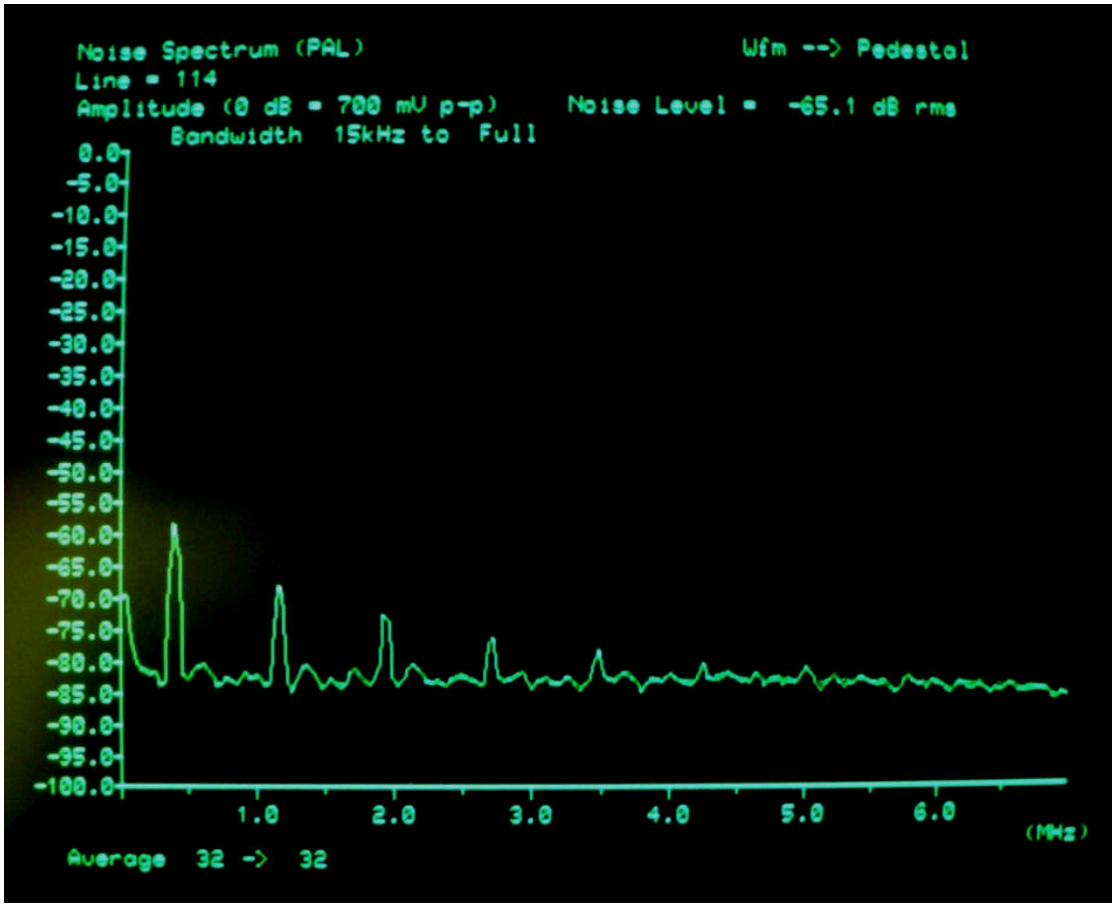

Figure 22 PAL Noise spectrum (black)

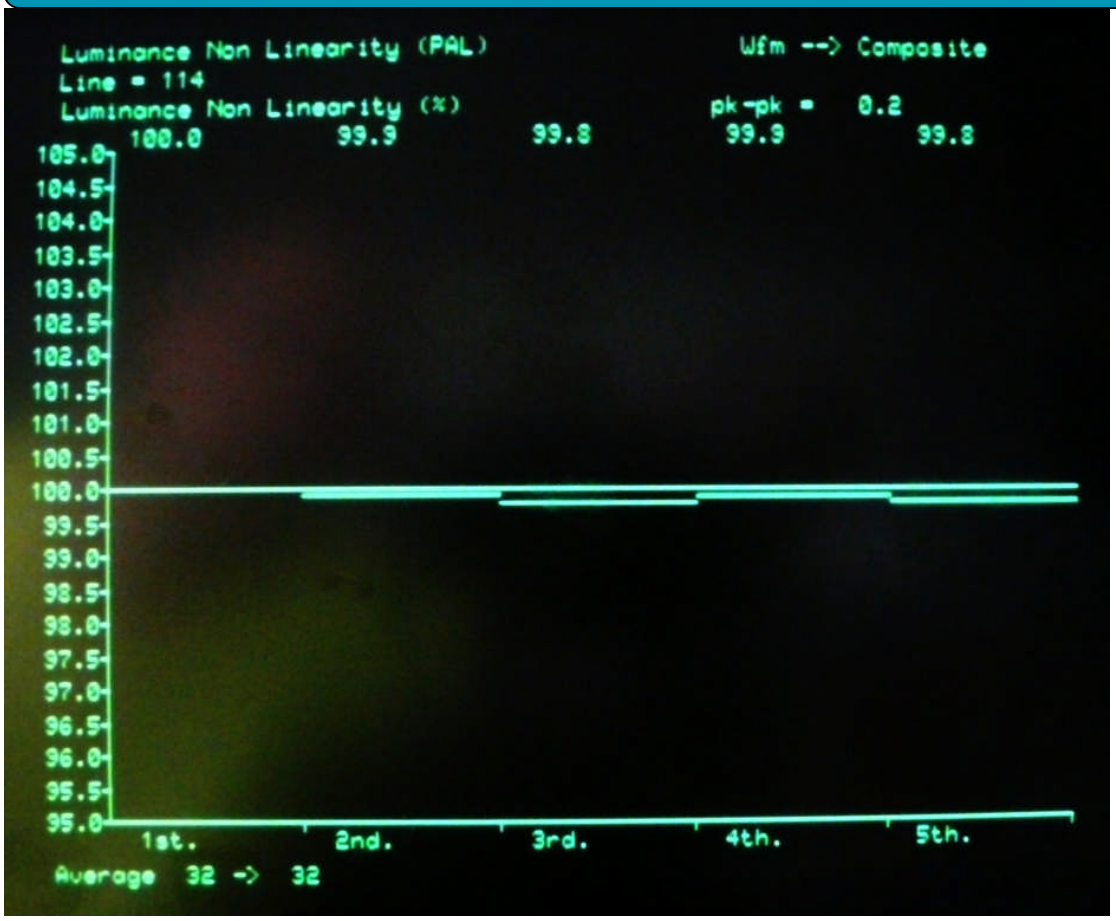

Figure 23 PAL Luma non-linearity