NEC

User's Manual

*start*WARE-GHS-Ravin-E

Ravin-E Add-on Board for *start*WARE-GHS-VR4131 and *start*WARE-GHS-VR4133

Document No. U17316EE1V0UM00
Date Published September 2004

Printed in Germany

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- The information in this document is current as of 14.09.2004. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.

- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.

- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such NEC Electronics products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.

- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC Electronics no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

- NEC Electronics products are classified into the following three quality grades: “Standard”, “Special” and “Specific”.

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated “quality assurance program” for a specific application. The recommended applications of NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is “Standard” unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact NEC Electronics sales representative in advance to determine NEC Electronics 's willingness to support a given application.

Notes: **1.** " NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

2. " NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

M8E 02.10

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics America Inc.
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 1101
Fax: 0211-65 03 1327

Sucursal en España
Madrid, Spain
Tel: 091- 504 27 87
Fax: 091- 504 28 60

Succursale Française
Vélizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

Filiale Italiana
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

Branch The Netherlands
Eindhoven, The Netherlands
Tel: 040-244 58 45
Fax: 040-244 45 80

Branch Sweden
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

United Kingdom Branch
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Singapore
Tel: 65-6253-8311
Fax: 65-6250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

Preface

Readers

This manual is intended for users who want to understand the functions of the *start*WARE-GHS-Ravin-E.

Purpose

This manual presents the hardware manual of *start*WARE-GHS-Ravin-E.

Organization

This system specification describes the following sections:

- Pin function
- CPU function
- Internal peripheral function
- Flash memory

Legend

Symbols and notation are used as follows:

Weight in data notation	:	Left is high-order column, right is low order column
Active low notation	:	$\overline{xxx}$ (pin or signal name is over-scored) or /xxx (slash before signal name)
Memory map address:	:	High order at high stage and low order at low stage
Note	:	Explanation of (Note) in the text
Caution	:	Item deserving extra attention
Remark	:	Supplementary explanation to the text
Numeric notation	:	Binary . . . xxxx or xxxB Decimal . . . xxxx Hexadecimal . . . xxxxH or 0x xxxx

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo) : $2^{10} = 1024$

M (mega) : $2^{20} = 1024^2 = 1,048,576$

G (giga) : $2^{30} = 1024^3 = 1,073,741,824$

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 System Requirements

Motherboard: *start*WARE-GHS-Ravin-E is an add-on board designed for the *start*WARE-GHS-V$_R$4131/33 boards. Running the s*tart*WARE-GHS-Ravin-E board with other mother-boards will require a suitable adapter, which is not part of this package. Such adapters are not available from NEC and therefore have to be provided by the user. Alternatively the *start*WARE-GHS-Ravin-E board can be operated via its PCI interface. That will require a suitable adapter whose schematics are included in chapter 5.4 of this document. Note that the PCI interface uses 3 V signaling only and it can therefore not be operated in a normal PC.

1.2 Package Contents

Please verify that you have received all parts listed in the package contents list attached to the *start*WARE-GHS-Ravin-E package. If any part is missing or seems to be damaged, please contact the dealer from whom you purchased your *start*WARE-GHS-Ravin-E.

Note: Updates to this User Manual, additional documentation and/or utilities for *start*WARE-GHS-Ravin-E, if available, may be downloaded from the NEC WEB page(s): ***http://www.nec.de/support***.

1.3 Related Documents

Ravin-E Preliminary Data Sheet, NEC Doc. Number S15521EJ1V0DS00

*start*WARE-GHS-V$_R$4131 User's Manual, NEC Doc. Number U16417EE1V0UM00

*start*WARE-GHS-V$_R$4133 User's Manual, NEC Doc. Number U16916EE2V0UM00

Application Note: Operation of Ravin-E with V850 Devices
NEC Doc. Number S17194EE1V0AN00

[MEMO]

Chapter 2 Board Features

As the name implies, the *start*WARE-GHS-Ravin-E board employs the Ravin-E display controller (µPD72255) as its centrepiece. Also implemented is an SAA7113H or SAF7113H video processor, which is used to digitize a PAL or NTSC standard video signal and optionally overlay it on the graphics. An analogue display can be connected via a standard 15-pin high density DSUB connector, while a digital display connects through a 30-pin row connector.

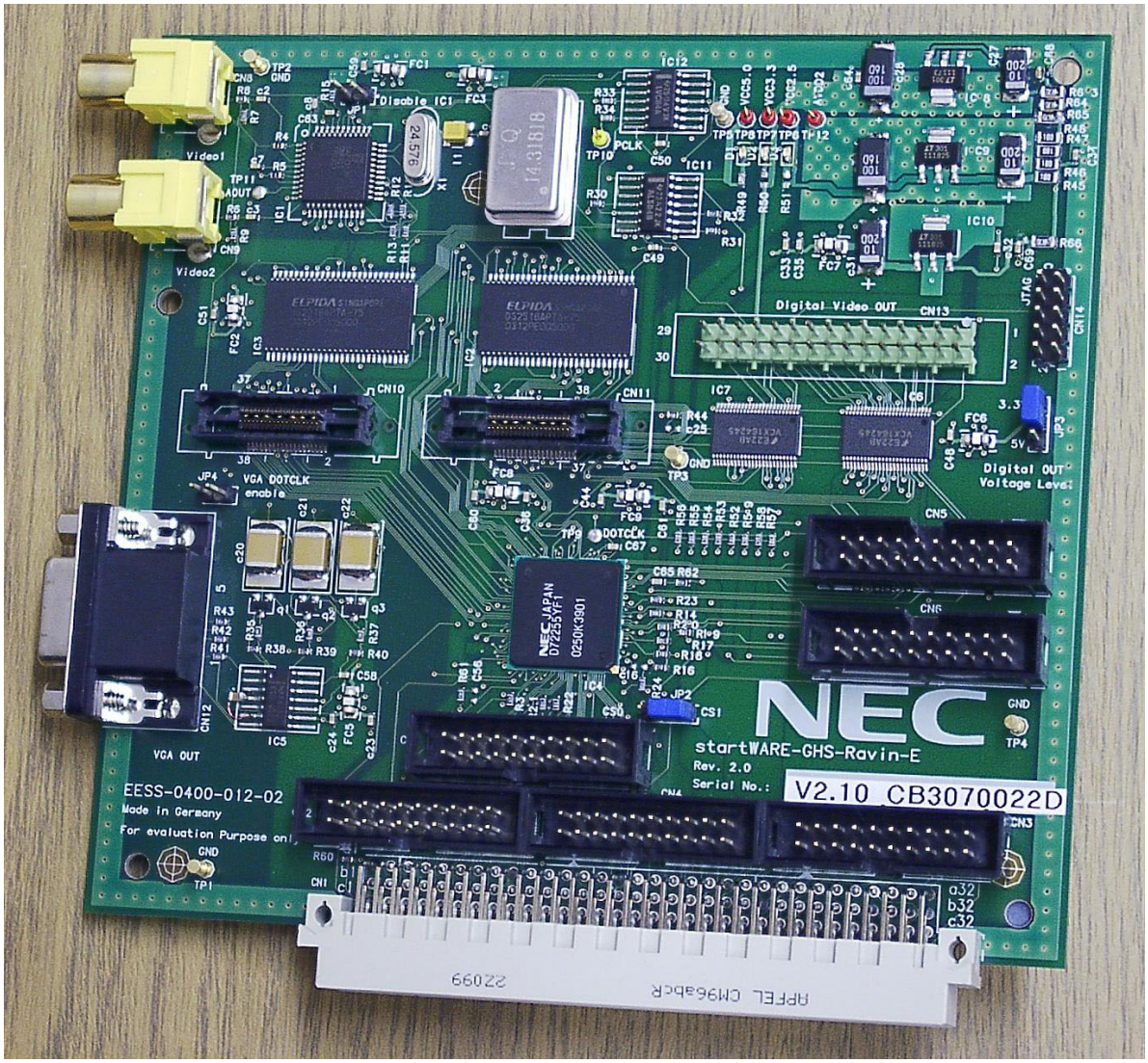
The *start*WARE-GHS-Ravin-E board has been designed as an add-on board for the *start*WARE-GHS-VR4131 or *start*WARE-GHS-VR4133 boards. It connects to these boards through a 96-pin male DIN connector CN1, which also carries the 5 V DC power supply.

2.1 Summary of Features

- Ravin-E (µPD72255) graphics display controller
- 64 MB on board SDRAM frame buffer
- Enhanced SAA7113 video processor for video capture
- Analogue (0.7 V_{PP}) and digital (3.3 V or 5 V) video outputs
- All Ravin-E signals available on standard logic analyzer connectors
- Single 5 V power supply (provided from main board)
- JTAG boundary scan implemented

2.2 Picture of *start*WARE-GHS-Ravin-E Board

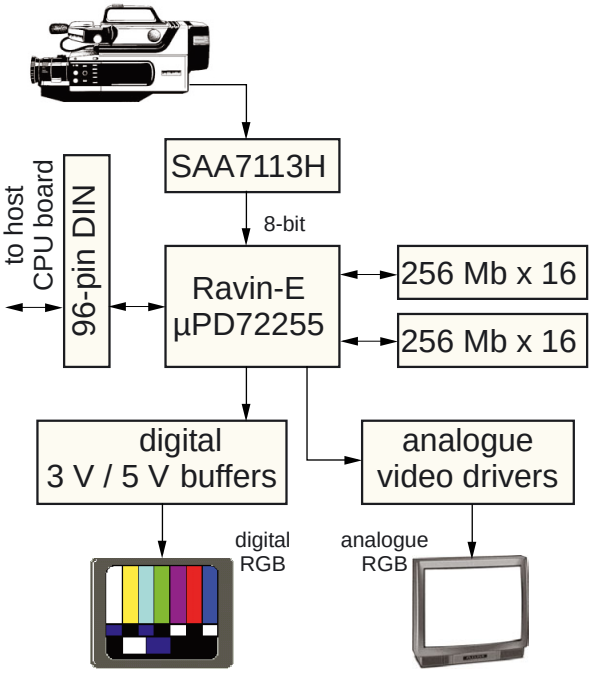
Figure 2-1: startWARE-GHS-Ravin-E Board



Chapter 3 Functional Description

Ravin-E (µPD72255Y) is the successor of the Ravin (µPD72254Y) display controller, designed for use in car navigation, multimedia and passenger entertainment systems. In addition to the original display control and drawing functions of µPD72254Y, Ravin-E supports high quality alpha blending for all window layers. This alpha blending feature is also employed for anti-aliased line drawing. Ravin-E also provides a function for capturing and displaying external video signals as well as a built-in D/A converter for analogue CRT or TFT displays. Ravin-E can be connected to virtually any 32-bit host CPU with an asynchronous SRAM-like bus interface. A second 32-bit wide data bus connects to standard SDRAMs which serve as the frame buffer for the graphics and the video.

Figure 3-1: startWARE-GHS-Ravin-E Block Diagram



As shown in the above block diagram, Ravin-E connects through a 96-pin DIN connector to the host CPU platform. This platform will be typically equipped with a VR41xx MIPS-RISC CPU, but it may be adapted to any other CPU with a suitable SRAM-like interface. The signal levels are 3.3 V LVTTL and the pinout is defined in “Host Connector CN1” on page 24 of the appendix.

Ravin-E is connected to two 256 Mbit SDRAMs, each one of them being 16-bit wide. These SDRAMs are primarily employed as frame buffer for the graphics, as video buffer for the overlaid video and also to store bitmaps, which can then be transferred quickly to the active screen location. The SDRAM also holds the alpha values when alpha blending is used and the z-values in case of 3-D applications. Even though the interface is not bandwidth optimized, the CPU has direct access to all locations in the SDRAM and therefore it might make use of any otherwise unused memory locations.

The SAA7113H or SAF7113H enhanced video processor digitizes one of two incoming analogue composite video signals (PAL or NTSC standard) and converts it to a standard 8-bit wide ITU 656 compliant YUV 4:2:2 signal. That signal can be captured by Ravin-E, optionally scaled up or down and then stored in the SDRAM. In the video output path, the format can be converted on the fly from YUV to RGB. See the SAA7113H Product Specification from Philips and the Ravin-E Data Sheet for details.

The *start*WARE-GHS-Ravin-E board provides two display outputs, each of which conveys the same display contents. 75 Ω RGB video drivers are provided on board, so that a 0.7 V_{PP} monitor can be directly connected to CN12. 5 V TTL compatible sync signals are provided as well on this connector. The dot clock can optionally be enabled on this connector via jumper JP4. Note that this connection is not required for standard VGA monitors and it might even cause problems. Therefore JP4 is normally unconnected. Check your monitor specification before setting JP4. JP4 may be useful when connecting an analog TFT display to this connector.

CN13 connects to a digital display, usually a TFT. Along with the digital colour, CN13 provides the sync and the dot clock signals, as well as a few control signals for the TFT display. JP3 switches the interface voltage between 3.3 V LVTTL and 5.0 V TTL. CN13 also provides the 5 V and 3.3 V operating voltages. See the chapter on power consumption below for details on the current ratings.
Three LEDs are provided to quickly check the operating voltages. D1 connects to the externally supplied 5 V, D2 to the 3.3 V and D3 to the 2.5 V. The 3.3 V and the 2.5 V are locally generated on the *start*WARE-GHS-Ravin-E board. When power is supplied, then all these LEDs should light up with about the same intensity.

CN14 is a connector for JTAG boundary scan equipment. The SAF7113H is the first device in the scan chain, while Ravin-E is the second one.

3.1 Power Consumption

The *start*WARE-GHS-Ravin-E board is supplied with a single +5 V DC operating voltage from the main board. The internally required 3.3 V and 2.5 V are generated by linear voltage regulators on the Ravin-E board. The following table shows the operating currents that have been measured under typical operating conditions (capturing video input and displaying it along with graphics). Note that these are reference values of just one board and that other boards may show slightly different current consumption, even if the conditions are the same.

Table 3-1: Operating Currents under typical operating conditions

Voltage	Measured current	Design limit[Note 2]
5 V	500 mA[Note 1]	1000 mA
$V_{CC}3.3$	160 mA	400 mA
$V_{CC}2.5$	230 mA	300 mA
AV_{DD2}	36 mA	100 mA

Notes: 1. Estimated, not measured (includes current for $V_{CC}3.3$, $V_{CC}2.5$ and AV_{DD2})

2. Do not permanently exceed these limits (e.g. by external loads)

The measured values include the power consumption of the respective voltage regulator, which is negligible. The voltage regulators have shunt resistors at their input voltage pin. These resistors can serve well for current consumption measurements, but their other purpose is to burn away some of the power, so that only part of it is dissipated in the regulator itself.

The $V_{CC}3.3$ voltage regulator (IC8) along with its shunt resistors and its heat sink on the PCB is designed to source up to 400 mA. Therefore it can supply external circuits (e.g. a suitable TFT Display) as long as they do not draw more than about 250 mA. Take care not to couple external noise onto this supply rail.

Chapter 4 Software Description

We have written a few demo programs, which can be found in the “Software\Ravin-E” directory of the *start*WARE-GHS-Ravin-E CD. The programs can be compiled for MIPS RISC devices or for V850E devices. Build files for each of these environments are supplied. We have used Green Hills version 3.5.1 for V850 and version 3.6.1 for MIPS. Make sure to issue a “build all” command, if you change between these tool chains. Otherwise the tools may mix modules of different architectures, which may lead to some weird error messages.

Here is the directory structure of Software\Ravin-E:

Animation
Benchmarks
Bin2C
Datalogger
HW-Test
Include
LibV850
LibVR
MyLib
png
rgl
StartupVR

The individual demo programs and their build files are found in Animation, Benchmarks, Datalogger and HW-Test. Bin2C contains a Windows application program, which converts a file to C-Source code. These programs are described later in this chapter. The Include directory contains a few include files, which are required by the demo programs and the libraries. LibV850 and LibVR contain the compiled libraries for the respective tool chain. MyLib holds the sources of the CPU initialization code and the interface code for the PNG library. png contains the sources of the png library (libpng) and the zlib, which is required for libpng. Both are third party software packages. See **http://www.libpng.org/** for the latest sources. rgl contains the Ravin Graphics Library and StartupVR contains startup code for MIPS devices and defines for the VR4131.

All libraries can be built automatically by the build files in LibVR or LibV850. The libraries are supplied on the CD and ready to use, but it may be useful to download the latest libpng and zlib sources from the internet and recompile them.

All temporary files during the build process are stored in the Tmp subdirectories of the respective module. The files in this path can be deleted after the build process.

4.1 Ravin-E Graphics Library

The Ravin-E graphics library (RGL) provides higher level functions to initialize and operate Ravin-E. Only the function ghs\rgl_custom.c needs to be adapted, when rgl is ported to another target. It defines the addresses of the Ravin-E registers (PhysReg) and of the Ravin-E frame buffer (PhysFB). An os_sleep(n) function is required for delays and timeouts, which delays by roughly n milliseconds. It needs not be very precise. For the V850E/ME2, we have implemented a simple active delay, which delays roundabout 1 ms for a 150 MHz device. If the CPU core frequency differs much from that, it should be adapted accordingly. A built-in timer is used for the VR4131, which generates 1 ms interrupts. The respective code is located in StartupVR\iqueue.c, start.mip and isr.mip.

A detailed description of the RGL can be found in the “Ravin-E Graphics Library Manual” in the rgl\doc directory.

4.2 Display of PNG Files

In order to display png files (Portable Network Graphics), we have ported the free PNG Reference Library libpng (**www.libpng.org**) to the V850. This library requires the zlib compression library (**www.gzip.org**), which has also been ported. These two libraries are documented on their respective websites. Calls to zlib functions are transparent and the libpng user need not bother too much about that zlib library. It should be noted, however, that a certain amount of heap space is required for both libpng and zlib. Also the stack size should not be too small, as these functions seem to use it extensively. They have clearly been written with personal computers in mind and are not optimized for the limited memory resources of embedded applications. Nevertheless there is a limited number of tuning possibilities by defining certain variables that control compilation of the libraries. See the respective documentation for details.

4.3 Bin2C: Converting Binary Files to C-Source Code

A binary file cannot be directly copied to an embedded system. At least it must be converted to a downloadable ASCII file of Intel-Hex or Motorola S-Record format. A slightly more complicated conversion seems to offer the best possible flexibility: converting the binary file to C-Source code. That is exactly what the bin2c utility was made for. The generated C-Source code can be embedded into any project and be located to any required address. bin2c was written for the conversion of .png files, but it does not perform any structural analysis and so it may be used with any file, not just with binary png-files.

bin2c inserts a pragma for the Green Hills compiler to emit the subsequent data into the segment *.images*. That allows for relocation of that data to any target address. bin2c defines an array of unsigned char and names the array with the file name of the input file. A few characters are converted if they are incompatible with the C naming conventions. The best idea is probably to avoid file names, which do not comply with C variable names.

bin2c can convert multiple files at once. For each input file it creates its own array with a name as described before. When the “Generate table of contents” checkbox is enabled, then an array of pointers to unsigned char is allocated and that array is initialized with pointers to the individual arrays. The name of this table is *toc* and the variable *toc_size* is initialized with the number of arrays (=number of files).

Animated sequences are usually created with index numbers in their file names. When the “Sort Input Files” checkbox is enabled, then the files are automatically sorted in ascending file name order.

bin2c was compiled with the free OpenWatcom tool chain, which is downloadable from **http://www.openwatcom.org/**. The sources of bin2c are provided on the CD and may be modified as required.

4.4 Demonstration Programs

Four rather simple demo programs are supplied on the *start*WARE-GHS-Ravin-E CD. They are described in this paragraph.

4.4.1 Animation

Animation is a demo program which displays a rotating image on the screen. This endless movie is simply made by displaying a sequence of 60 PNG images cyclically, so that the impression of a movie is generated. The images were produced by POVRay (**www.povray.org**) and ThumbsPlus (**www.thumbsplus.com**) was used to generate a common palette for all of them. A common palette is required to eliminate the temporal noise, which would otherwise occur due to the asynchronous update of the palette and the display data.

One of two implementations can be selected at compile time. If REALTIME_DECODE is defined, then each individual frame is decoded and the result is directly copied to the Ravin-E frame buffer. That saves RAM space, but the decoding has to be repeated as often as the image is to be displayed. Decoding a png file is rather time consuming. With this option enabled, the rotation of the image is rather slow and not at all smooth.

If the option PRE_DECODE is enabled, then all frames are decompressed before the animation starts. The decompressed data is stored in the heap space, which must therefore be sufficiently large to hold all decoded files. Each image of this example has a size of 240x240 pixels and the images use a colour palette, which means that they use 8 bits per pixel. The required heap space for a single frame is thus 57600 bytes which sums up to almost 3.5 MB for all frames. Therefore the total heap space should be at least 4 MB. Pre-decoding takes a few seconds and when it is done, the animation starts. It merely copies the individual decompressed frames from the heap to the frame buffer, which is very quick. Therefore this version needs a delay after each frame is sent to the frame buffer. We have decided for 15 ms, which makes the rotation rather smooth.

The performance and the required CPU time could be further improved by copying the decompressed individual images into Ravin-E's frame buffer instead of the heap. The total size of the frame buffer on the *start*WARE-GHS-Ravin-E board is 64 MB which is plenty of space outside the current display area. Transfer of the image to the screen location would then be accomplished by a BITBLT command to Ravin-E. For the CPU that is a simple sequence of a few register write operations and as such it would virtually cost no CPU time at all.

4.4.2 Benchmarks

Benchmarks is a program to test the performance of Ravin-E and the bus interface. It tests the speed of vector and filled rectangle drawing as well as the data transfer between the host and Ravin-E. Benchmarks measures certain key performance values under real-life rather than optimized idealistic conditions. The selected screen resolution is 800 x 600 pixel at 60 Hz frame rate and two display layers are enabled, one with 16 bit per pixel and the other one with 8 bit per pixel. In this configuration, the screen refresh uses approximately 25% of the available bandwidth between Ravin-E and its SDRAMs. This is an average bus load calculated for a whole frame and it includes the sync pulses, during which no data transfer takes place at all. The average data rate during the display of a scan line is about twice as high with short periods of essentially 100% bus load when a burst read is issued to fill the video output pipeline.

The times are measured with built-in timers on the V850E/ME2 and on the VR4131. The VR4131 timer does not detect overflows and the arithmetic has been chosen to make a compromise between precision and integer overflow in intermediate results. Therefore when changing the code, especially the number of loops, note that overflows on the VR4131 are not detected and they may return invalid results. Also the timers are configured for the documented operating speeds. Make sure to adapt the initialization, if the clock speed deviates from the reference clock speed. Note that the results of the timing measurements vary in a certain range due to the statistical nature of the accesses on the Ravin-E frame buffer.

The effect of write combining can be tested by defining NO_WC at compile time. Write combining is enabled by default. It enables Ravin-E to combine write transfers to subsequent memory addresses and to make burst accesses instead of single writes. That has a very noticeable effect if data is usually written to subsequent addresses. Writes to random addresses are slowed down, however, because every individual write access is delayed, as it might have to be combined with the next write.

4.4.3 Datalogger

Datalogger is an application, which displays a simple four channel datalogger grid on the foreground layer. This is a pre-defined image that is stored in a PNG-file and extracted once at initialization time into the frame buffer. Four traces are displayed on the background layer, which move from the right side to the left, so that the older values appear on the left and the newer values on the right side. The displayed values are generated from pseudo random numbers which are low pass filtered to make them look like real analogue input data.

Display of the trace lines makes use of Ravin-E's feature to move the viewport freely over the virtual display area. When the display line wraps over, Ravin-E does not actually display the image data from the subsequent line, but the data from the beginning of the current line. This feature permits the impression of a moving image, without actually copying data within the frame buffer. Only the start address of the viewport is constantly updated. In the case of the datalogger demo program, the right most column is updated in addition to the viewport address, as always new data shall be displayed. The display data is erased on the left side of the screen, before it enters the outside of the grid.

The datalogger demo program requires very little CPU performance. Almost all CPU time is spent in the “os_sleep(20)” delay at the end of function main.

4.4.4 HW-Test

HW-Test is a program, which is used by NEC in the *start*WARE-GHS-Ravin-E production test. It performs an initial test of the Ravin-E frame buffer memory, displays some vectors with colour shading on the screen and captures a video via the cinch connectors.

Chapter 5 Appendix

This chapter collects the technical data of the board. Detailed explanations are therefore reduced to a minimum.

Figure 5-1: Board Outline and Component Placement

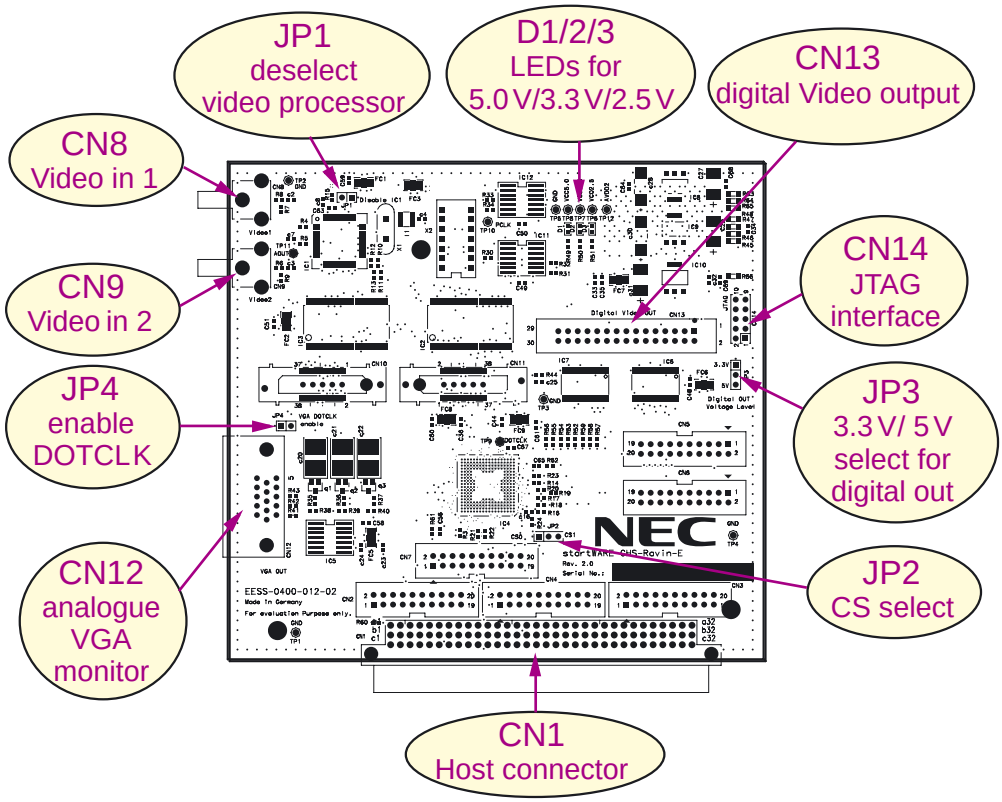


Table 5-1: Technical Data of the Ravin-E Board

Component	See page	Type	Purpose
CN1	page 24	DIN41612, male, 3 × 32 pins	Connector to host CPU board
CN8	page 27	Cinch	Video 1 input
CN9	page 27	Cinch	Video 2 input
CN12	page 28	DSUB15, female, high-density	VGA monitor, analogue video output
CN13	page 29	Row connector, male, 2 × 15 pins	Digital video output
CN14	page 31	Row connector, male, 2 × 5 pins	JTAG interface
JP1	page 32	Row connector, male, 2 pins	De-select video processor
JP2	page 32	Row connector, male, 3 pins	Select one of two chip select inputs
JP3	page 33	Row connector, male, 3 pins	Select digital video interface voltage
JP4	page 33	Row connector, male, 2 pins	Enable DOTCLK output on CN12
D1/D2/D3	-	LED	5.0 V, 3.3 V, 2.5 V operating voltages

5.1 Description of Connectors and Jumpers

5.1.1 Host Connector CN1

The a- and c-rows of the connector are exchanged against each other in the schematics and on the silk screen of the board. Unlike the schematics, the following table lists the real connection of the signals with the pin numbers according to common practice and according to the pin number imprint on the connector.

Figure 5-2: Host Connector CN1

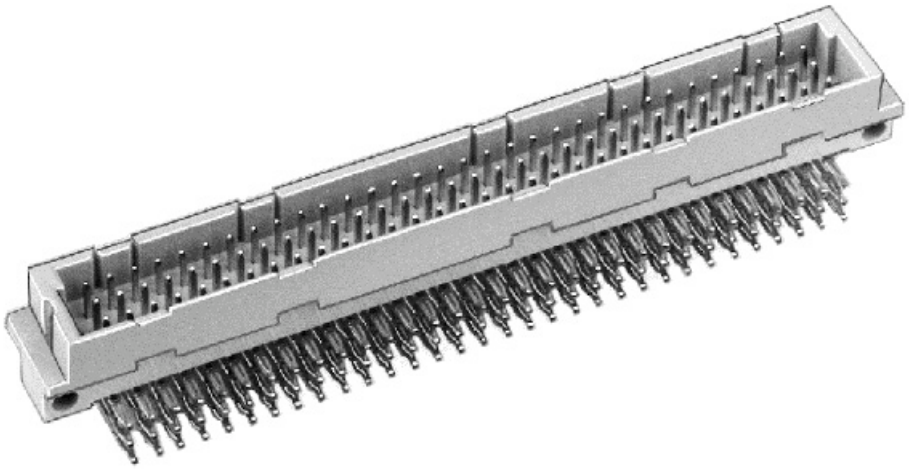


Table 5-2: Host Connector CN1 (1/4)

Number	Name	Direction[Note]	Description
a1	VCC50	in	+5 V DC +/-10% power supply from motherboard
b1	VCC50	in	+5 V DC +/-10% power supply from motherboard
c1	VCC50	in	+5 V DC +/-10% power supply from motherboard
a2	DATA30	in/out	data bus signal 30
b2	DATA31	in/out	data bus signal 31
c2	GND	in	ground
a3	DATA27	in/out	data bus signal 27
b3	DATA28	in/out	data bus signal 28
c3	DATA29	in/out	data bus signal 29
a4	DATA24	in/out	data bus signal 24
b4	DATA25	in/out	data bus signal 25
c4	DATA26	in/out	data bus signal 26
a5	DATA22	in/out	data bus signal 22
b5	DATA23	in/out	data bus signal 23
c5	GND	in	ground
a6	DATA19	in/out	data bus signal 19

Note: Signal direction as seen from *start*WARE-GHS-Ravin-E board (e.g. “in” is an input on this board and must be driven by the main board)

Table 5-2: Host Connector CN1 (2/4)

Number	Name	Direction[Note]	Description
b6	DATA20	in/out	data bus signal 20
c6	DATA21	in/out	data bus signal 21
a7	DATA16	in/out	data bus signal 16
b7	DATA17	in/out	data bus signal 17
c7	DATA18	in/out	data bus signal 18
a8	DATA14	in/out	data bus signal 14
b8	DATA15	in/out	data bus signal 15
c8	GND	in	ground
a9	DATA11	in/out	data bus signal 11
b9	DATA12	in/out	data bus signal 12
c9	DATA13	in/out	data bus signal 13
a10	DATA8	in/out	data bus signal 8
b10	DATA9	in/out	data bus signal 9
c10	DATA10	in/out	data bus signal 10
a11	DATA6	in/out	data bus signal 6
b11	DATA7	in/out	data bus signal 7
c11	GND	in	ground
a12	DATA3	in/out	data bus signal 3
b12	DATA4	in/out	data bus signal 4
c12	DATA5	in/out	data bus signal 5
a13	DATA0	in/out	data bus signal 0
b13	DATA1	in/out	data bus signal 1
c13	DATA2	in/out	data bus signal 2
a14	BEB1	in	Byte Enable 1 (active low)
b14	BEB0	in	Byte Enable 0 (active low)
c14	GND	in	ground
a15	GND	in	ground
b15	BEB3	in	Byte Enable 3 (active low)
c15	BEB2	in	Byte Enable 2 (active low)
a16	n.c.	-	unconnected
b16	n.c.	-	unconnected
c16	RESET	in	Reset signal (active high)
a17	ADD22	in	address bus signal 22
b17	ADD23	in	address bus signal 23
c17	GND	in	ground
a18	ADD19	in	address bus signal 19
b18	ADD20	in	address bus signal 20
c18	ADD21	in	address bus signal 21
a19	ADD16	in	address bus signal 16
b19	ADD17	in	address bus signal 17

Note: Signal direction as seen from *start*WARE-GHS-Ravin-E board (e.g. “in” is an input on this board and must be driven by the main board)

Table 5-2: Host Connector CN1 (3/4)

Number	Name	Direction[Note]	Description
c19	ADD18	in	address bus signal 18
a20	ADD14	in	address bus signal 14
b20	ADD15	in	address bus signal 15
c20	GND	in	ground
a21	ADD11	in	address bus signal 11
b21	ADD12	in	address bus signal 12
c21	ADD13	in	address bus signal 13
a22	ADD8	in	address bus signal 8
b22	ADD9	in	address bus signal 9
c22	ADD10	in	address bus signal 10
a23	ADD6	in	address bus signal 6
b23	ADD7	in	address bus signal 7
c23	GND	in	ground
a24	ADD3	in	address bus signal 3
b24	ADD4	in	address bus signal 4
c24	ADD5	in	address bus signal 5
a25	n.c.	-	unconnected
b25	RDY	out	CPU Ready signal (active high, i.e. low=wait, high=ready); high impedance while Ravin-E is not selected.
c25	ADD2	in	address bus signal 2
a26	LCS1B	in	Chip select 1 (active low)
b26	LCS0B	in	Chip select 0 (active low)
c26	GND	in	ground
a27	RDB	in	CPU read signal (active low)
b27	WRB	in	CPU write signal (active low)
c27	GND	in	ground
a28	n.c.	-	unconnected
b28	n.c.	-	unconnected
c28	n.c.	-	unconnected
a29	DAKB	in	Data acknowledge
b29	DRQB	out	Data request
c29	RDSTSB	out	Read status
a30	n.c.	-	unconnected
b30	CPUSEL	in	Select CPU interface (0=PCI, 1=asynchronous)
c30	n.c.	-	unconnected
a31	GND	in	ground
b31	PCICLK	in	PCI clock (connect to GND if asynchronous interface)
c31	GND	in	ground
a32	n.c.	-	unconnected

Note: Signal direction as seen from *start*WARE-GHS-Ravin-E board (e.g. “in” is an input on this board and must be driven by the main board)

Table 5-2: Host Connector CN1 (4/4)

Number	Name	Direction[Note]	Description
b32	IDSEL/ VSSEL	in	Initialization device select (in PCI mode) CPU interface select (in asynchronous bus mode) 0: VR41xx mode; 1: BEBn inputs are write strobe signals
c32	n.c.	-	unconnected

Note: Signal direction as seen from *start*WARE-GHS-Ravin-E board (e.g. “in” is an input on this board and must be driven by the main board)

5.1.2 Video Connectors CN8 and CN9

Standard Cinch connectors are used to input the composite video signals for the two video channels 1 and 2. The nominal impedance for each video input is 75 Ω. The signals are AC coupled to the video processor via 47 nF capacitors. The nominal video signal voltage level is 1 V_{PP}, but due to the automatic gain adjustment within the video processor, signal levels between 0.5 V_{PP} and 1.4 V_{PP} are acceptable.

Figure 5-3: Video Connectors CN8 and CN9

5.1.3 VGA Connector CN12

CN12 is a 15-pin female high density Sub-D connector. It has a pin configuration so that a standard VGA monitor can be connected. The RGB signal voltages have levels between 0 and 0.7 V_{PP} while the synchronization signals are 5 V TTL compatible.

Figure 5-4: VGA Connector CN12

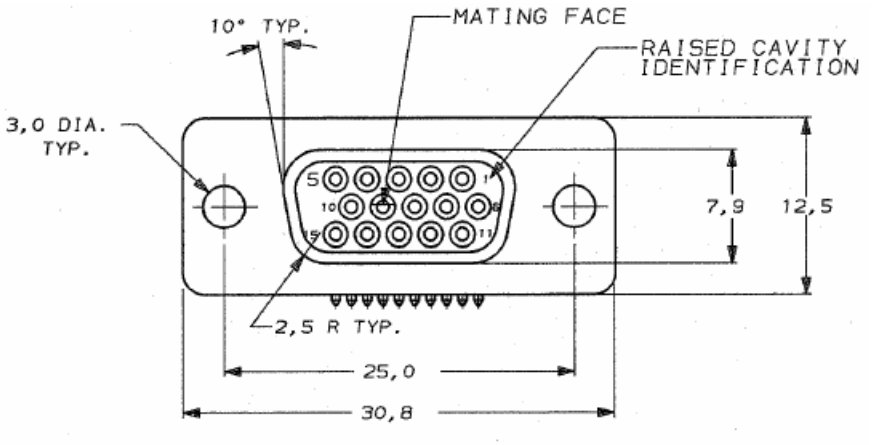


Table 5-3: VGA Connector CN12

Number	Name	Direction	Description
1	Red	out	Red colour component; 0 to 0.7 V_{PP}
2	Green	out	Green colour component; 0 to 0.7 V_{PP}
3	Blue	out	Blue colour component; 0 to 0.7 V_{PP}
4	n.c.	-	unconnected
5	GND	-	Signal ground
6	n.c.	-	unconnected
7	n.c.	-	unconnected
8	n.c.	-	unconnected
9	DOTCLK	out	DOTCLK if JP4 is set, otherwise unconnected
10	n.c.	-	unconnected
11	n.c.	-	unconnected
12	n.c.	-	unconnected
13	HSYNC	out	Active low horizontal sync
14	VSYNC	out	Active low vertical sync
15	n.c.	-	unconnected

5.1.4 Digital video output connector CN13

CN13 carries the signals for a digital TFT display. Its signal output voltages are selectable by JP3 to 3.3 V or 5 V.

Figure 5-5: Digital video output connector CN13

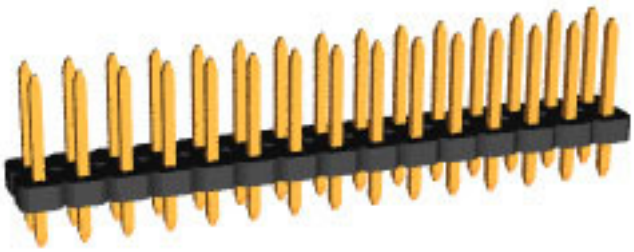


Table 5-4: Digital video output connector CN13

Number	Name	Direction	Description
1	FSC	out	Ravin-E FSC output[Note]
2	PLLREF	out	Ravin-E PLLREF output[Note]
3	VCC33	-	3.3 V power supply
4	VCC50	-	5.0 V power supply
5	VO0	out	Blue 1
6	VO1	out	Blue 2
7	VO2	out	Blue 3
8	VO3	out	Blue 4
9	VO4	out	Blue 5
10	GND	-	Ground
11	VO5	out	Green 0
12	VO6	out	Green 1
13	VO7	out	Green 2
14	VO8	out	Green 3
15	VO9	out	Green 4
16	VO10	out	Green 5
17	GND	-	Ground
18	VO11	out	Red 1
19	VO12	out	Red 2
20	VO13	out	Red 3
21	VO14	out	Red 4
22	VO15	out	Red 5
23	VCC33	-	3.3 V power supply
24	CSYNC	out	Ravin-E CSYNC# output (Note)
25	HSYNC	out	Ravin-E HSYNC# output (Note)
26	VSYNC	out	Ravin-E VSYNC# output (Note)
27	DOTCLK	out	Ravin-E DCLK output (Note)
28	ENABLE	out	Ravin-E ENABLE output (Note)
29	GND	-	Ground
30	GND	-	Ground

Note: These output pins are disabled after reset. The meaning of the output pins can be defined in the Ravin-E register VoSyncSelect at address 0x01FF FB4Ch.

5.1.5 JTAG interface connector CN14

CN14 is the JTAG interface connector. The scan chains of the SAA7113 and Ravin-E are linked, with the SAA7113 being the first in the chain and Ravin-E the second.

Figure 5-6: JTAG interface connector CN14

Table 5-5: JTAG interface connector CN14

Number	Name	Direction	Description
1	TCK	in	JTAG clock
2	GND	-	Signal ground
3	TDO	out	JTAG scan chain output
4	VCC33	-	3.3 V power supply
5	TMS	in	JTAG scan chain mode select
6	n.c.	-	Not connected
7	TRST	in	JTAG scan chain tri-state
8	n.c.	-	Not connected
9	TDI	in	JTAG scan chain input
10	GND	-	Signal ground

5.1.6 Disable Video Processor with JP1

When a jumper is plugged onto JP1, then the video processor is de-selected. This feature has been implemented so that an external video processor can access the video input port of Ravin-E. JP1 is normally not used. Therefore the board is shipped without this jumper and thus the video processor is enabled by default.

Figure 5-7: Jumper JP1

5.1.7 Select CS input with JP2

The host connector CN1 carries two chip select signals, which can be alternatively used to select Ravin-E. JP2 selects the active CS signal.

Figure 5-8: Jumper JP2

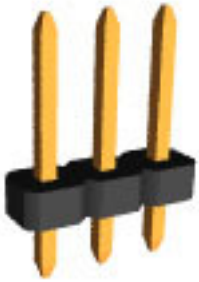


Table 5-6: Jumper Settings with JP2

Jumper setting	Function
1-2 (left[Note])	CS0 input used
2-3 (right[Note])	CS1 input used

Note: Board orientation as depicted in Figure 5-1.

5.1.8 Select digital video signal voltage with JP3

The digital video output signals on CN13 can drive either 3.3 V LVTTL or 5 V TTL compatible devices. JP3 selects between these two voltages.

Figure 5-9: Jumper JP3

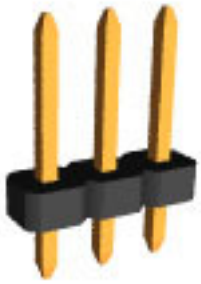


Table 5-7: Jumper Settings with JP3

Jumper setting	Function
1-2 (top[Note])	3.3 V signal output level
2-3 (bottom[Note])	5.0 V signal output level

Note: Board orientation as depicted in Figure 5-1.

5.1.9 Enable DOTCLK for VGA interface with JP4

When a jumper is plugged onto JP4, then the 5 V TTL DOTCLK is connected to pin 9 of CN12. This signal is normally not used and therefore the board is shipped without JP4. Before plugging JP4, please make sure that your monitor can tolerate that signal. There is probably no standard monitor, which can use the DOTCLK. We have implemented it primarily for experimenting with analogue TFT displays.

Figure 5-10: Jumper JP4

5.2 Address Map

Ravin-E occupies 16 MB (when using the SRAM-like bus interface) or 32 MB (when using the PCI-interface) in the address space of the host CPU. In both cases, the upper 8 kB of this range are reserved for the on-chip status and command registers, while the rest of these address spaces is directly mapped to access the frame buffer.

Even though the host interface is limited to 16 or 32 MB access size at a time, Ravin-E can access a total frame buffer of up to 64 MB. The window that is visible from the host CPU can be moved over the total frame buffer by specifying the frame buffer start address in the HostCpuBaseAddr. The start address is aligned to a 2 kB base address.

When the *start*WARE-GHS-Ravin-E board is used together with the *start*WARE-GHS-VR4131 board, then the following address mapping in the VR4131 I/O address space applies:

JP2 selects CS0: 0x0A00 0000 ~ 0x0AFF FFFF
JP2 selects CS1: 0x0C00 0000 ~ 0x0CFF FFFF

See page 32 for JP2 settings.

Note that the sizes of the VR4131 I/O address spaces are 32 MB each, and therefore the above 16 MB address spaces are mirrored at 0x0B00 0000 ~ 0x0BFF FFFF and 0x0D00 0000 ~ 0x0DFF FFFF respectively.

5.3 *start*WARE-GHS-Ravin-E Schematics

Figure 5-11: Ravin-E

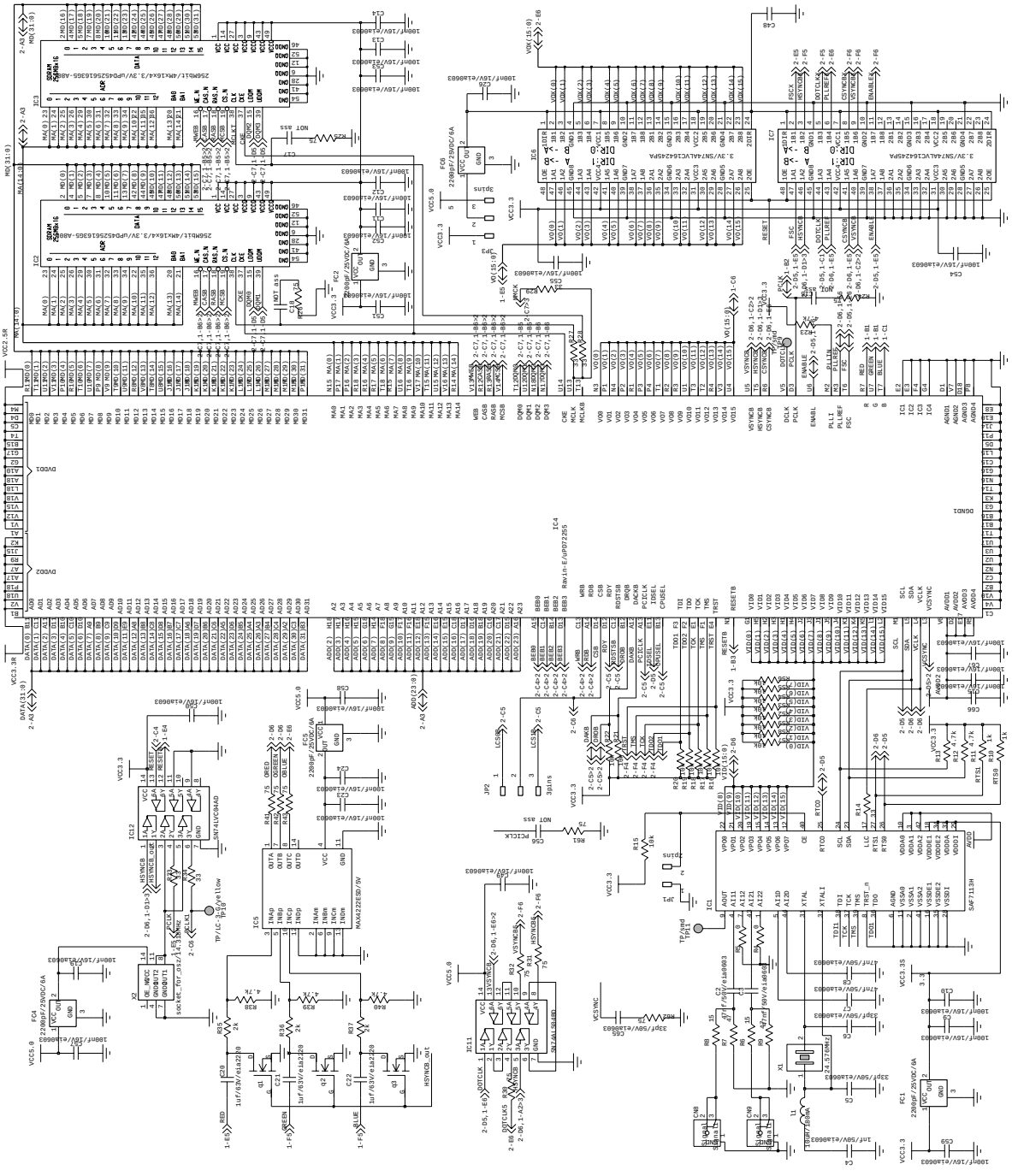
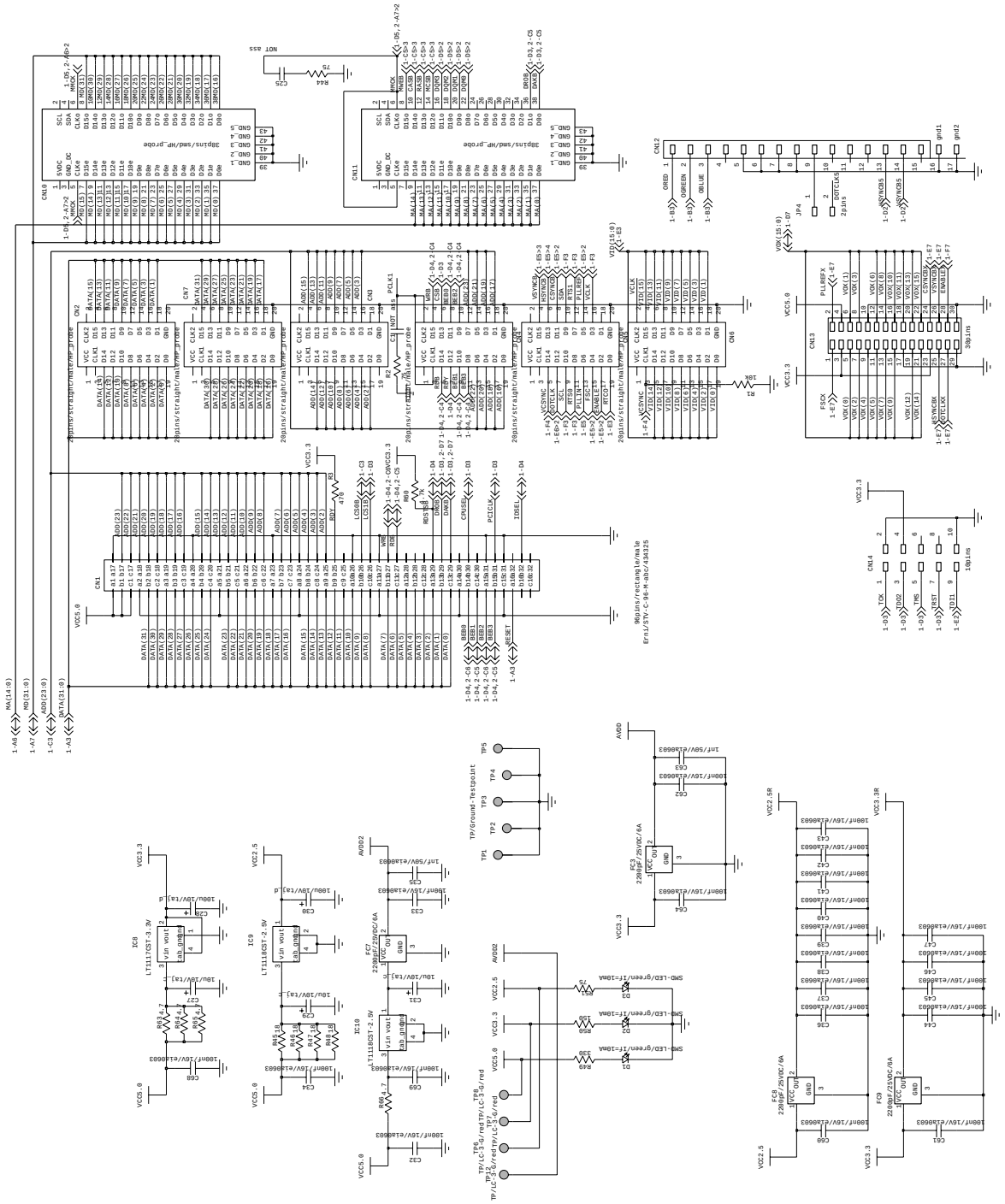


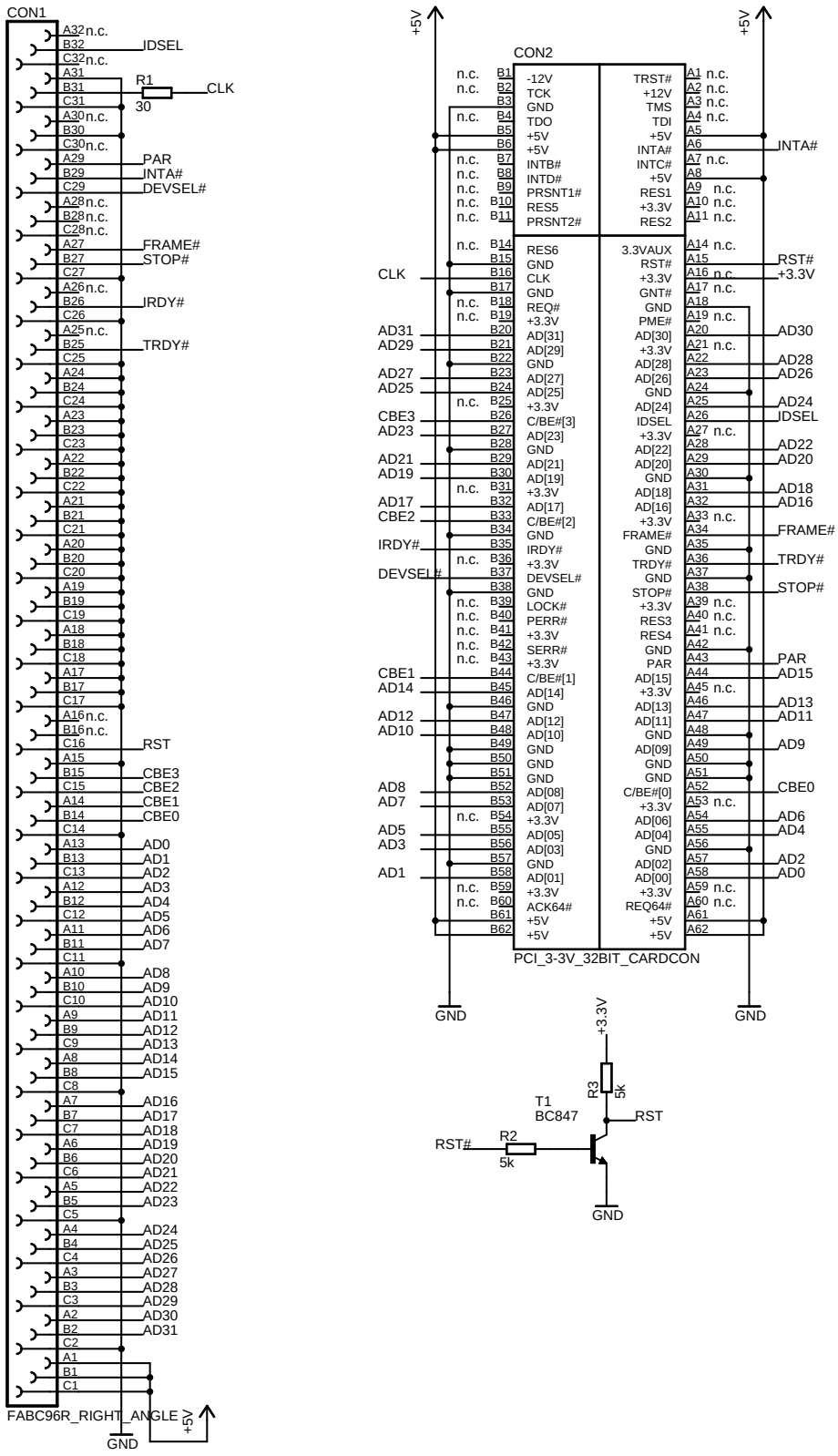
Figure 5-12: Connectors



5.4 PCI Adapter Schematics

This adapter is not included in the *start*WARE-GHS-Ravin-E package.

Figure 5-13: VME-PCI Adapter



[MEMO]

NEC

Facsimile Message

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

From:

Name

Company

Tel. FAX

Address

Thank you for your kind support.

North America
NEC Electronics America Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

Europe
NEC Electronics (Europe) GmbH
Market Communication Dept.
Fax: +49(0)-211-6503-1344

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-6250-3583

Japan
NEC Semiconductor Technical Hotline
Fax: +81- 44-435-9608

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	☐	☐	☐	☐
Technical Accuracy	☐	☐	☐	☐
Organization	☐	☐	☐	☐