ETR XX

ALCAPONE0/1 control chip

TECHNICAL DOCUMENT

LHC / ALICE / Inner Tracker System / Silicon Strip Detector / EndCap modules

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Abstract:

This control chip is designed to control the detector front-end electronics on the hybrids connected to the double-sided Silicon Strip Detectors. The electronics at both sides of the detector module operate at different bias potentials. The main functions are power regulation and signal distribution (buffering). The chip itself is programmable via the IEEE 1149.1 (JTAG Boundary Scan Test) protocol.
The ALCAPONE has integrated features to be able to use AC-coupled signal transfer in order to cross the bias potentials.
The chip is designed in a 0.25µm CMOS process. By using "gate-around" layout techniques, the chip is radiation tolerant.

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Changes in ALCAPONE1

1 Introduction

This ASIC (Application Specific Integrated Circuit) is designed to control the Front-end chips on the detector hybrids of the ALICE Silicon Strip Detector Inner Tracker and is called ALCAPONE, "**AL**ice **C**ontrol **A**nd **PO**wer **NE**xus". The front-end chip is the *HAL25* [1], designed by LEPSI/IRES in Strasbourg.
This chip requires JTAG control signals for the adjustment of internal registers (e.g. bias). In addition timed signals for sample/hold and the readout are required.
These signals must be distributed through the system (**E**nd **C**ap **M**odule [2]), and therefore locally buffered. In addition, local control and monitor functions close to the front-end are required. This includes a power regulator and ADC for monitoring. Error checking and failure "recovery" functions are also required.

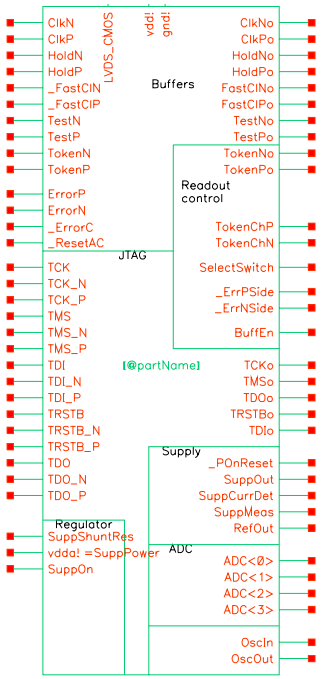


Figure 1 ALCAPONE1 **schematic symbol**

2 Functional description

The ALCAPONE design contains a number of functional blocks:

- LVDS and CMOS buffers/repeaters with AC coupled inputs
- Front-End readout token control
- Power regulator with Latch-up protection and (shunt) regulator for local power
- ADC for monitoring functions

These blocks will be described separately. The Logic and de ADC share the same Power input (Vdd). The (shunt-) regulator for local power and the Power regulator have each a separate power input on the ALCAPONE. A system overview is described in "Design of ladder *EndCap* electronics" [2].

2.1 LVDS and CMOS buffers/repeaters

A number of signals are just feed through the ALCAPONE chip. These are Clk, Hold, FastClr and Test. These signals are received via a Low Power LVDS receiver with positive feedback for AC coupling. The Fast clear (FastClr) signal is also used internal to reset the front-end readout control. This clears the readout cycle during readout.
The Token output can be delayed from the input. This depends to which side of the detector module the token must be sent. The delay is programmable via the JTAG bus.
The 10MHz CLK that must be distributed inside the ECM use LVDS signals. The JTAG signals to the ECM are using LVDS levels, but once received they are distributed with CMOS levels inside the ECM and to the front-end modules. Look in the ALCAPONE Pin descriptions to find which signals are only buffered.

2.1.1 Low Power LVDS AC input

These LVDS receivers have been optimized to work with 10MHz signals (tested up to 50MHz) and have low power consumption (~550uA) [3]. The circuit is also provided with a disable control input. In the situation where the receiver is not needed, it will be disabled to save power.
The receiver is supplied with a positive feedback circuit (level adapter in Figure 2) and has a hysteresis of ±25mV.

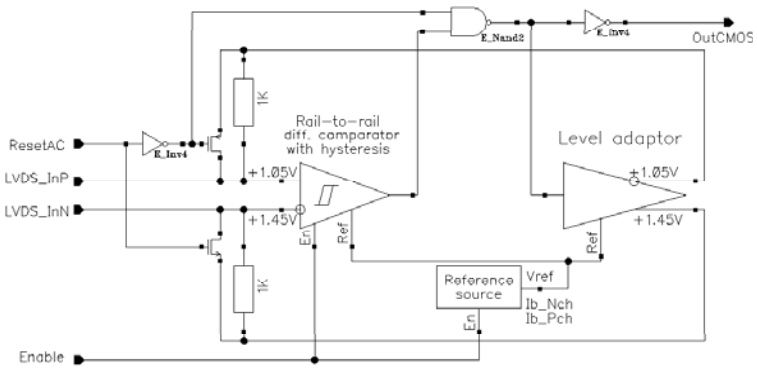


Figure 2 LVDS receiver for AC-coupling diagram

This feedback circuit delivers the DC levels of correct LVDS (~0.9 & 1.3V) to the receiver input (via a high impedance circuit) to ensure that the receiver works well when the inputs are AC coupled with 47pF capacitors. A reset signal ensures that the total circuit can be reset to the required initial state. This is necessary when AC-coupled signals are used, after power is switched on.

2.1.2 LVDS driver with disable function

Once the signals are received, they are directly connected to LVDS output drivers. These drivers are modified drivers from the cmos6sf25PadLib from RAL/CERN. The drivers deliver ~3.6mA through 100Ω. The modification is that a disable function is added, where the outputs become high impedant when the circuit is disabled. This is necessary for the Latch-up protection method, when the power for the hybrids is switched off, no current should flow through the signal connections.

2.1.3 CMOS AC input

The CMOS input circuit is basically a standard cell from the cmos6sf25Pad library. The difference is a positive feedback via a ±50kΩ resistor. This is necessary to receive AC coupled signals. In addition, a RESET function is added to determine the initial state after the power is switched on. Low active inputs are RESET to 'High'. Since these circuits do not dissipate power when they are not used, there is no disable function.

2.1.4 CMOS output

The buffered CMOS outputs are slightly modified. A disable function is added in such a way that the outputs have high impedance when the drivers are disabled. This is for the Latch-up protection.
Most outputs can drive 8mA and some have slew rate limited output stages. Outputs that have to drive more inputs have a 20mA output drive capability.

2.2 Readout and Token (delays)

The readout control for the front-end chip, the HAL25, is done using 4 signals:

- The **HOLD**, this signal activates the sampling of the input amplifier value of the HAL25 (sample and hold).
  This signal only needs to be buffered. It is not used inside the ALCAPONE
- The **CLK** activates the logic for the readout. It is only available during the readout cycle. The ALCAPONE requires 4 CLK cycles *before* TokenIn, and 4 cycles *after* the ReturnToken.
  The CLK signal is buffered by the ALCAPONE, and used to generate the delayed token signal.
- This is followed by a **Token**; this signal determines when a specific data sample is multiplexed to the output of the HAL25 chip. The Token is sent first to one side of the detector module, and delayed to the second side of the module.
  The ALCAPONE generates the delay based on a fixed number of CLK cycles, dependant of the number of HAL25 chips to be read out. This number is programmable.
- To clear an on going readout cycle the **FastClear** signal must be activated (low active).
  This signal is used by the ALCAPONE to clear the internal token readout sequence.

- The **Test** signal is used to simulate a hit in the analogue front-end of the HAL25. The Hold signal must be delayed from 'Test' according to the programmed shaper time of the HAL25 chip. This signal only needs to be buffered. It is not used inside the ALCAPONE

The CLK, HOLD and FastClear signals can be sent to both sides of a detector module hybrid at the same time. However, to make sure that the two sides are readout sequentially, the token is first sent to one side. A delayed (delay as long as one module readout) token is sent to the other module side. The delay can be programmed in steps of 128 CLK cycles, from 0 to 6 steps (maximum number of chips on a hybrid.) Once a hybrid is completely readout, it returns the token (TokenCheck). This is checked by the ALCAPONE. An internal delay is used to synchronize the hybrid return token with the internal token.

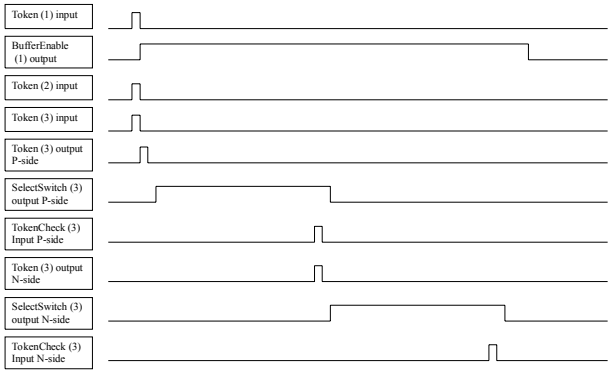


Figure 3 Timing diagram of the token readout

The token signal is sampled by the CLK at the rising edge, and the token output is released when the CLK goes low. If the returned token does not appear at the right moment in the ALCAPONE, an error will be generated. Errors are described later in chapter "Error Handling", page 8.
The readout signals in the EndCap are visualized in Figure 3 and Figure 4. First, the signals are received in the ALCAPONE (1) at GND level. Then they are sent to each detector side and there again buffered by (2). Then the signals reach the ALCAPONE (3) that is connected to the hybrids with the HAL25 chips. In these chips, the delay must be generated, such that each detector side of a module is readout sequentially. This chip also controls the analogue multiplexer in the ALABUF chip (SelectSwitch). The corresponding analogue channel is activated during readout.
The first ALCAPONE in the ECM will switch on the analogue buffer chip as soon as the token is received. The signal BufEnable, is active during the programmed CHIPCOUNT + the ReadoutTime time values.

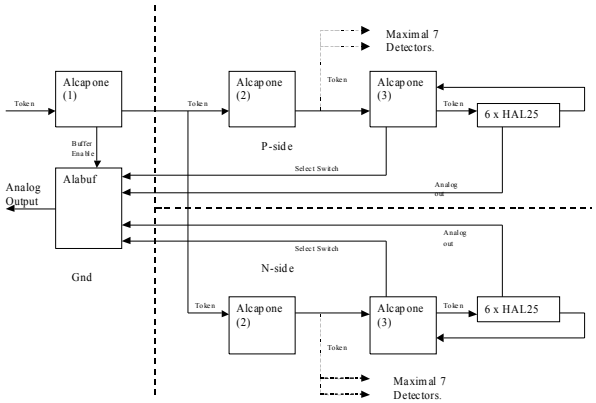


Figure 4 Token readout scheme.

The FastClear signal will RESET the delays, but nothing else. A readout cycle can be aborted, and after release of the signal, the chip is ready to start a new readout cycle.

2.3 Power regulator

A Power supply regulator in the chip is necessary to create latch-up protection for the electronics succeeding the ALCAPONE chips. This power "block" consists of two parts, the *shunt regulator* and the *power supply regulator*.

2.3.1 Shunt regulator

This circuit is used to generate the correct supply voltage for the power regulator circuit. It consists of a Bandgap reference with buffer and a shunt regulator circuit. This whole circuit can be supplied from a 3 to 6Volt power supply (via a 180Ω resistor) and it delivers always 2.5V for the power regulator circuit.

Specifications:	Value	Tolerance
VshuntRef	2.52V	30 mV
Max. Shunt current	XxxmA	1mA

Min. Shunt current	XxxmA	1mA

2.3.2 Power supply regulator

The regulator is able to regulate the power for 1 to 15 ALCAPONE chips, or for a HAL25 hybrid. This corresponds to ±150mA and ±1A. The circuit is controlled via JTAG and an external signal SuppOn. This signal determines if the regulator should switch on after the power is switched on, or not. In this always on mode, the shunt regulator must power the power supply circuit.
Again, a Bandgap reference circuit is used to generate a reference voltage for the regulator. To adjust the output voltage, an 8-bit DAC is implemented to modify the reference for the output voltage
The regulator is switched off when the output current exceeds a limit. This limit is determined by the value of the current sense resistor, R14 in Figure 5. When the voltage over this resistor exceeds 19mV (±0.1V), the power is switched off. It can be switched on again via JTAG, or in case, that SuppOn is "high", by switching off and on the external voltage.

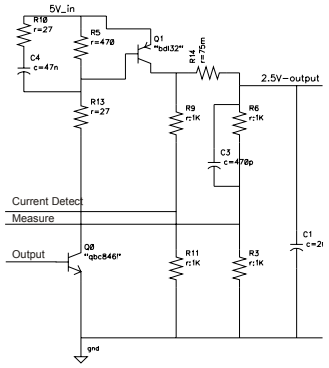


Figure 5 External Power supply components

During the power-up of the power supply of the ALCAPONE chip, the following sequence occurs:

1. Until the input power voltage reaches "Vin min.", the start-up circuit will keep the output off.
2. After this, the Bandgap reference becomes stable, the output is switched on to "Vout-min.", and the POnRESET is held active by the start-up circuit. During this time, the over-current protection is disabled and capacitive load can be charged.
3. The ALCAPONE is now switched on (Power DAC=0~2V), and after POnRESET is finished the default value for the power-DAC is loaded, and the output goes to about 2.5V.
4. Now the regulator circuit is in normal operating mode and sensing the output current. The power-DAC value can be modified via the JTAG port.

In ALCAPONE*1, every time a change is made to the DAC value, the over-current protection is disabled for about 30µs.* This is done to prevent the power to be switched off due to an over-current of charging load capacitors.

Specifications:	**Value**	**Tolerance**
Vin min	2.1V	200mV
Vin max.	2.7V	10mV
Vout min.	1.9V	100mV
Vout max.	2.9V	100mV
Vout default	2.52V	100mV
Vdropout min	300mV	50mV
Over current timer	34µs	10µs
Startup timer	320µs	50µs
Switch sense limit	19mV	0.5mV
Change timer	30µs	5us

2.4 Adc

For monitoring purposed is an 8-bit successive approximation ADC (Figure 6) implemented in the chip. The input multiplexer has 4 inputs. This is followed by a sample and hold circuit. This is a "switch" and a 2pF capacitor with a buffer. The voltage has the ALCAPONE "gnd" input as ground reference. The ADC logic is clocked from an oscillator that needs an external RC network (10k & 10nF for ~30kHz). Instead, a defined clock can be connected to the "OscIn" input.
The conversion time is the clock period multiplied by 20. From this clock, two non-overlapping signals are generated to operate the switches.
The SAR logic determines the correct DAC value that corresponds with the input voltage. The 'Hold' signal is to prevent the result register to be read and written at the same time, the read action is blocked.

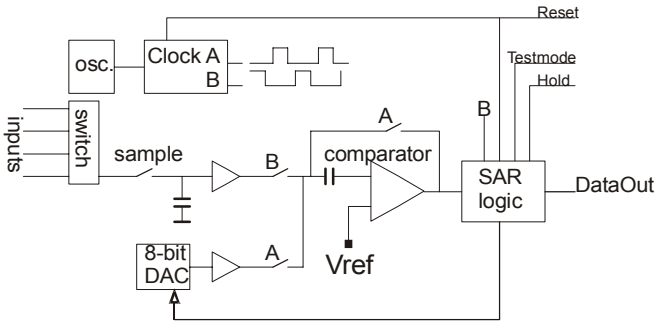


Figure 6 ADC block diagram

Specifications:	Value	Tolerance
Range min	0 V	+50mV
Range max	2 V	50mV
Linearity error	1 %	.5 %
Current out	9.96µA	.1µA

Input 3 is provided with a current source output of 10µA. This can be to connect a NTC of 100k to monitor the temperature.
In the ALCAPONE*1,* ADC *'TestMode' is added.*
In 'TestMode, the DAC value is counting from 255 to 0 continuously and the resulting voltage can be verified at one of the selected analog inputs (not 3). In normal operation, the ADC continuously digitizes the selected input, and the result can be read out via JTAG. The analogue range is from 0 to 2 Volts (0-255).

2.5 Error Handling

Some error situations can be monitored and flagged

- Supply switched off due to over current:
  PowerStatusLatch is '1' if the error has occurred. PowerStatus is '1' if the error is still there.
- Return token from hybrid is not received:
  TokenError is '1' if a token did not return at the expected moment.
- Parity of all control registers is changed (bit flip due to radiation).
  All bits in POWERCONTROL, DELAYCONTROL, CHIPCOUNT, POWERREF, and ERRORMASK are used in the parity check. If a bit flips during normal operation, (e.g. due to radiation) it is detected.
- External error from detector P- or N side received:
  If one of both inputs recognizes an error, the ErrP/Nside bit is '1'. The ErrN/P side bit represents that an error has been detected.

If one of these errors is recognized, it will be flagged. The flag must be RESET manually via the status register with bit ResetControl. All flags are now cleared.

2.6 JTAG logic

Via this logic, all ALCAPONE functions can be controlled. The logic consists of a TAP state machine with the mandatory IEEE 1049 JTAG registers and functions. Extra registers have been added for control functions of the chip. If "IEEE JTAG" is mentioned in the table header, the instruction behaves according to the IEEE 1049.1 standard.
The JTAG communication can occur via CMOS- or LVDS signals. The LVDS signals are used if the ALCAPONE receives the signals over a long distance and the CMOS signals inside the ALICE EndCap module and to the hybrid. Via the LVDS_CMOS input, the selection is made (see chapter Specials, 3.6)

2.6.1 Instruction register

The JTAG instruction register has four bits that are decoded to the following instructions:

1. Extest 0000
2. SAMPLE/PRELOAD 0001
3. IdCode 0010
4. INTEST 0011
5. ENDCAPSTATUS 0100
6. POWERCONTROL 0101
7. DELAYCONTROL 0110
8. CHIPCOUNT 0111
9. POWERREFERENCE 1000
10. ADC 1001
11. ADCINPUT 1010
12. ERRORMASK 1011
13. RESET 1100
14. Bypass 1111

The Instructions go together with data registers, although INTEST, EXTEST and SAMPLE/PRELOAD share the one Boundary-Scantest register.
The input and output cells, which have a BST register can be found in page 15, ALCAPONE Pin descriptions BYPASS and RESET have a register of 0 (zero) length.
Reading the instruction register will result in: [status1, status0, 0, 1]. The status bits are defined as '0'.
In the ALCAPONE*1, the Status1 bit is Power status, and Status0 is the Error sum.*

2.6.2 IdCode

This register holds a PRESET number this is *1000000*01, and can only be read.

IDCODE	0010	IEEE JTAG
Bits [1:0]	01	R
Bits [5:2]	Version Number [3:0], 0000, *0001*	R
Bits [9:6]	Chip ID [3:0], 0001	R

A RESET of the JTAG logic will set the IDCODE instruction in the instruction register. Therefore, after RESET, (or Power On) the IDCODE can be read out and the JTAG chain can be determined.
ALCAPONE*1: Version number = 0001*.

2.6.3 Bypass

The BYPASS Instruction is a mandatory JTAG instruction and has no real register. The instruction puts the chip in a transparent mode for JTAG communication.

BYPASS	1111	IEEE JTAG

2.6.4 Extest

This Instruction is used to test interconnections between chips. It puts all output cells in active mode and the EXTEST register content is placed in the BST cells to the output drivers. The situation of the input cells is sampled in to the EXTEST register and can be read out.

EXTEST	0000	IEEE JTAG
Bit [1:0]	01	R
Bit [2] ALCAPONE1	*LVDS_CMOS in*	*R*
Bit [2], *[3]*	Clk out	R/W
Bit [3], *[4]*	Hold out	R/W
Bit [4], *[5]*	FastClear out	R/W
Bit [5], *[6]*	Test out	R/W
Bit [6], *[7]*	Token out	R/W
Bit [7], *[8]*	TokenCh in	R/W
Bit [8], *[9]*	ErrNside in	R/W

Bit [9], *[10]*	ErrPside in	R/W
Bit [10], *[11]*	SelectSwitch out	R/W
Bit [11], *[12]*	BufEnable out	R/W
Bit [12], *[13]*	_POnRESET out	R
Bit [13], *[14]*	SuppOn in	R/W
Bit [14], *[15]*	_RESETAC in	R
Bit [15], *[16]*	Error CMOS out	R/W
Bit [16], *[17]*	Error LVDS out	R/W
Bit [17], *[18]*	Token in	R/W
Bit [18], *[19]*	Test in	R/W
Bit [19], *[20]*	FastClear in	R/W
Bit [20], *[21]*	Hold in	R/W
Bit [21], *[22]*	Clk in	R/W

The EXTEXT register bit _PonRESET is made read-only, this is because in some positions of the ALCAPONE0 on the ECM, the *_POn*RESET is connected to _RESETAC. An EXTEST write would cause an error in this situation

In ALCAPONE1, one Input pin is added, LVDS_CMOS.
This pin is the first pin in the list, so it becomes Bit [2]. All other Bits shift one position. This is in the INTEST, EXTEST and SAMPLE/PRELOAD register If it is '1' the LVDS JTAG inputs are used, else the CMOS.

2.6.5 INTEST

With this instruction, internal functions can be tested. In the ALCAPONE0, the direct connections between the input and output can be checked.
In addition, the token delay can be checked. By asserting a token, followed by enough TCK clock cycles according to the programmed delay, the TokenOut is latched internal. The latched token can be read out via the INTEST instruction and asserting a FastClr signal via the same register can clear the latched token. In this way, the various delay settings can be tested via JTAG. In addition, the activation of BufEnable and SelectSwitch can be checked this way.

INTEST	**0011**	**IEEE** JTAG
Bit [1:0]	01	R
Bit [2] ALCAPONE1	*LVDS_CMOS in*	*R*
Bit [2], *[3]*	Clk out	R
Bit [3], *[4]*	Hold out	R
Bit [4], *[5]*	FastClear out	R
Bit [5], *[6]*	Test out	R
Bit [6], *[7]*	Token out	R
Bit [7], *[8]*	TokenCh in	R/W
Bit [8], *[9]*	ErrNside in	R/W
Bit [9], *[10]*	ErrPside in	R/W
Bit [10], *[11]*	SelectSwitch out	R
Bit [11], *[12]*	BufEnable out	R
Bit [12], *[13]*	_POnRESET out	R
Bit [13], *[14]*	SuppOn in	R/W
Bit [14], *[15]*	_RESETAC in	R
Bit [15], *[16]*	Error CMOS out	R
Bit [16], *[17]*	Error LVDS out	R
Bit [17], *[18]*	Token in	R/W
Bit [18], *[19]*	Test in	R/W
Bit [19], *[20]*	FastClear in	R/W
Bit [20], *[21]*	Hold in	R/W
Bit [21], *[22]*	Clk in	R/W

No INTEST function can be performed with the _ResetAC pin. This would cause an error.

2.6.6 SAMPLE/PRELOAD

This register is used to sample the present input or output state of the I/O cells to which the BST registers are connected. The PRELOAD is used to set the registers before an INTEST instruction. Therefore, the content of this register is the same as the INTEST register.

2.6.7 ENDCAPSTATUS

The actual chip status can be checked.

ENDCAPSTATUS 0100	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [2]	PowerOn, 0	ResetLatches
Bit [3]	PowerStatus, 0	HALTestMode
Bit [4]	PowerStatusLatch, 0	X
Bit [5]	SuppOn, ext.[1]	X
Bit [6]	PowerMask, 1	X
Bit [7]	DelayOn, 0	X
Bit [8]	TokenError, 0	X
Bit [9]	TokenERRORMASK, 1	X
Bit [10]	HALTestMode, 0	X
Bit [18:11]	DAC [7:0], 95_{hex}	X
Bit [22:19]	ADC_Input [3:0], 0	X
Bit [25:23]	WaitTime [2:0], 6	X
Bit [28:26]	ReadoutTime [2:0], 6	X
Bit [29]	_ErrPside, 0	X
Bit [30]	ErrPsideLatched, 0	X
Bit [31]	P_Mask, 1	X
Bit [32]	_ErrNside, 0	X
Bit [33]	ErrNsideLatched, 0	X
Bit [34]	N_Mask, 1	X
Bit [35]	ParityError, 0	X
Bit [36]	ParityErrorLatched, 0	X
Bit [37]	ParityERRORMASK, 1	X

[1]:This bit is hardwired, so the initial value is determined by the external connection.

By writing a '1' to the ResetLatches bit, all the Latched error bits will be RESET. This occurs at the time of writing, so the bit does not need to be reset. The PowerStatus bits are the same as in the POWERCONTROL register.

The HALTestMode bit enables the user to read the analog output of the front-end (Transparent mode). It will activate BufEnable and SelectSwitch. In this way, one analogue detector channel can be monitored.

In ALCAPONE0, the DAC bits are inverted. This is solved in ALCAPONE1.

In ALCAPONE*1, the ENDCAPSTATUS register has 4 additional bits:*

ENDCAPSTATUS 0100	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [2]	PowerOn, 0	RESETLatches
Bit [3] *ALCAPONE1*	JTAGOn, 0	HALTestMode
Bit [4]	PowerStatus, 0	TestModeADC
Bit [5]	PowerStatusLatch, 0	X
Bit [6]	SuppOn, ext.	X
Bit [7] *ALCAPONE1*	LVDS_CMOS, ext[1]	X
Bit [8]	PowerMask, 1	X
Bit [9]	DelayOn, 0	X
Bit [10] *ALCAPONE1*	TokenFeedThrough, 0	X
Bit [11]	TokenError, 0	X

Bit [12]	TokenErrorMask, 0	X
Bit [13]	HALTestMode, 0	X
Bit [21:14]	DAC [7:0], 95_{hex}	X
Bit [22] *ALCAPONE1*	TestModeADC, 0	X
Bit [26:23]	Adc_Input [3:0], 0	X
Bit [29:27]	WaitTime [2:0], 6	X
Bit [32:30]	ReadoutTime [2:0], 6	X
Bit [33]	_ErrPside, 0	X
Bit [34]	ErrPsideLatched, 0	X
Bit [35]	P_Mask, 1	X
Bit [36]	_ErrNside, 0	X
Bit [37]	ErrNsideLatched, 0	X
Bit [38]	N_Mask, 1	X
Bit [39]	ParityError, 0	X
Bit [40]	ParityErrorLatched, 0	X
Bit [41]	ParityErrorMask, 1	X

[1]:This bit is hardwired, so the initial value is determined by the external connection.

2.6.8 POWERCONTROL

The power regulator can be controlled via this register. By default Power is Off, Reset is '0'.

POWERCONTROL 0101	**Control Read, default**	**Control Write**
Bit [1:0]	01	X
Bit [2]	StatusLatch, 0	X
Bit [3]	PowerStatus, 0	ResetPowerStatusLatch.
Bit [4]	PowerOn, 0	PowerOn
Bit [5] ALCAPONE1	*JTAG_ON, 0*	*JTAG_ON*
Bit [6] ALCAPONE1	*SuppOn, 0*	*X*

Once the power is on and ok, the PowerStatus bit will be '1'. If, as result of over current, the power is switched off, the PowerStatusLatch bit will be set. This means that the error is latched. Writing a '1' to the ResetPowerStatusLatch bit will reset it. Only the according bit will be reset.
If the Power is switched off, the JTAG TDOo-TDIo connection is made inside the ALCAPONE to bypass the un-powered hybrid.
When the power is on, the JTAG chain is automatically switched on to the devices behind the chip

In ALCAPONE1, two bits are added to the POWERCONTROL register.
When the power is on, the JTAG TDOo-TDIo connection can still be programmed via this register by the JTAGOn bit. The control bit is '0' after power-on, and should be made '1' to reach JTAG devices behind the chip. The bit is reset by TRSTB. This can help to reduce the JTAG chain when some parts do not need to be programmed.

2.6.9 DELAYCONTROL

The delay for the token signals can be switched on and off via this register. Default is '0', off.
The result can be read back. In case the delay is 'off', the TokenOut signal is still 2 Clock cycles delayed.
Delay "off" gives the same result as delay "on", and ReadoutTime=0 in CHIPCOUNT.

DELAYCONTROL 0110	**Control Read, default**	**Control Write**
Bit [1:0]	01	X
Bit [2]	DelayOn, 0	DelayOn
Bit [3] ALCAPONE1	*TokenFeedThrough, 0*	*TokenFeedThrough*

In ALCAPONE1, one bit is added in the DELAYCONTROL register.
It determines if the token is connected directly to the output or not (no delay). This must be selected in the chips in the EndCap that only buffer and distribute the control signals.

2.6.10 CHIPCOUNT

In here, the WaitTime and the ReadoutTime can be programmed. The WaitTime specifies the number of chips, which are readout before a token will be sent. The ReadoutTime specifies the number of chips to be readout. This setting is necessary for the return token (from the hybrids) to be checked.
Default values '6'.

CHIPCOUNT 0111	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [4:2]	WaitTime [2:0], 6	WaitTime [2:0]
Bit [7:5]	ReadoutTime [2:0], 6	ReadoutTime [2:0]

2.6.11 POWERREFERENCE

The power supply circuit reference voltage can be set using this register. Values from 0 to 255 can be used. The analogue result is 1.031V to 1.384V. This results in an output voltage of ~ 2.07V to 2.78V.
Default is 149 (~2.52V output).

POWERREF. 1000	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [9:2]	DAC [7:0], 95_{hex}	DAC [7:0]

2.6.12 ADC

Via this register the result of the 8-bit ADC can be read. First, one of the 4 inputs must be selected with the ADCINPUT register. In *ALCAPONE*0 the bits are swapped [0:7]=[7:0] and inverted.
In ALCAPONE*1, the ADC value is correct.*

ADC 1001	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [9:2]	ADC [7:0], xx	X

2.6.13 ADCINPUT

This register determines which of the 4 inputs is selected for the ADC. Default is '0'.
Input 3 has a current source of 9.96µA connected for NTC measurements.
In *ALCAPONE*0, if one selects an input, the result is that just that bit is NOT selected, but the other three are connected together, and connected to the ADC.
In ALCAPONE*1, the ADC input selection is correct.*

ADCINPUT 1010	Control Read, default	Control Write
Bit [1:0]	01	X
Bit [3:2]	ADCInput [1:0], 0	ADCINPUT [1:0]

2.6.14 ERRORMASK

A '1' in the mask means that a received error will be OR'ed with the others to the ERROR output, while a '0' will block the particular error.
By default, all errors are enabled (mask bits are '1').

ERRORMASK 1011	Control Read, default	ControlWrite
Bit [1:0]	01	X
Bit [2]	PowerStatusLatch, 1	PowerStatusLatch
Bit [3]	TokenErrorLatched, 1	TokenError
Bit [4]	ParityErrorLatched, 1	ParityErrorLatched
Bit [5]	_ErrPsideLatched, 1	ErrPsideLatched
Bit [6]	_ErrNsideLatched, 1	ErrNsideLatched

In ALCAPONE*1, all error status bits are active '1'. The mask bits are '1' when masked.*
The bits are inverted with respect to the *ALCAPONE*0, but it more obvious this way. The default values are therefore '0' in the *ALCAPONE*1.

2.6.15 RESET

By writing this instruction, a JTAG Reset signal is generated when a following UpdateDR occurs. This means that a write action of zero bits must be performed after the instruction is set.
This reset will reset all error latches, and load the default values to all registers.

RESET 1100	**Control Read Control Write**
No bits	

In ALCAPONE1, the JTAG chain remains closed when the RESET instruction is selected.
In alcapone0, the JTAG chain is interrupted after the selection of this instruction. The internal TDI-TDO connection is not there.

2.7 ALCAPONE reset functions

The chip has different reset input functions, as well as a Reset output.

- **_RESETAC input** (active low).
  This is the PowerOn reset input of the ALCAPONE, it will initialize the following:
  - The JTAG controller is set to Run_Test/Idle
  - The registers are loaded with the default values
  - The ADC logic is reset and will start if the oscillator runs
  - All input circuits that can be used with AC-coupling are set to the correct initial state.
- **TRSTB** JTAG reset **input** (active low).
  This signal will set the JTAG controller in the Test_Logic_Reset state. No register values are changed, only the controller goes to the defined state.
  In ALCAPONE1, it will reset the JTAGOn bit.
- **Reset via the** JTAG **register**.
  This will reset all JTAG registers to the default values. It goes without changing the JTAG controller state. This means that the communication is not interrupted.
- **_POnReset output** (active low)
  The _POnReset output is only valid when the power supply circuit is used. After power on, the output is low (active). Once the output voltage has reached the minimum level (~1.9V), but is stable, the signal becomes inactive (high). Now the value of the POWERREFERENCE register is connected to the DAC, and the output will "go" to the required voltage.
  In the case of self-powering (SuppOn is '1'), this reset output can be connected to the _ResetAC input to initialize the chip itself.

In ALCAPONE1, the ADC logic is reset by _ResetAC.
In *ALCAPONE0*, ADC was reset by TRSTB, so after the power was switched on the user had to assert a TRSTB to start the ADC.

3 ALCAPONE Pin descriptions

Note that the maximum voltage on each input may not exceed 2.7V. Regular Vdd is 2.5V.
The CMOS input/output signal levels are 0 to Vdd, the LVDS levels are ~1V to ~1.4V.
The CMOS switch level is ~ ½ Vdd. For LVDS, the switch level =~1.2V.

3.1 LVDS receivers & drivers pins for AC coupling

Signal	BST	Direction	Description
ClkN & ClkP[0]	Y	In	Readout clock in
ClkNo & ClkPo	Y	Out[1]	Readout clock out, direct from input to output
HoldN & HoldP[0]	Y	In	Sample and Hold for front-end
HoldNo & HoldPo	Y	Out[1]	Sample and Hold to front-end, direct from input to output
FastClN & FastClP[0]	Y	In	FastClear for front-end (active low), direct from input to output
FastClNo & FastClPo	Y	Out[1]	FastClear to front-end, direct from input to output
TestN & TestP[0]	Y	In	Test timing signal for front-end
TestNo & TestPo	Y	Out[1]	Test timing signal to front-end, direct from input to out-put
TokenN & TokenP[0]	Y	In	Token to start Readout of front-end
TokenNo & TokenPo	Y	Out[1]	Token to start Readout of front-end, delayed according to the side of the detector
ErrorN & ErrorP	Y	Out	EndCap Error signal to FEROM

0. *Only the signal receivers have been adapted for AC coupled signals*
1. *These outputs are **dis**abled if Power supply is **OFF**.*

3.2 JTAG signal pins

Signal	Dir.	Type	Description
TCKN & TCKP[2]	In	LVDS	Clock in from FEROM
TMSN & TMS[2]	In	LVDS	TestModeSelect in from FEROM
TDIN & TDIP[2]	In	LVDS	TestDataIn in from FEROM
TRSTBN & TRSTBP[2]	In	LVDS	TestResetTBar in from FEROM
TDON & TDOP[2]	Out	LVDS	TestDataOut to FEROM
TCK	In	CMOS	Internal EndCap input signal TCK (also for AC)
TMS	In	CMOS	Internal EndCap input signal TMS (also for AC)
TDI	In	CMOS	Internal EndCap input signal TDI (also for AC)
TRST	In	CMOS	Internal EndCap input signal TRST (also for AC)
TDO	Out	CMOS	Internal EndCap output signal TDO, 8mA SLR
TCKo	Out[1]	CMOS	Buffered internal EndCap signal TCK, 8mA
TMSo	Out[1]	CMOS	Buffered internal EndCap signal TMS, 8mA
TDIo	In	CMOS	Buffered internal EndCap signal TDI (also for AC)
TRSTBo	Out[1]	CMOS	Buffered internal EndCap signal TRSTB (active low), 8mA
TDOo	Out[1]	CMOS	Internal EndCap signal TDO, 8mA

2. *The LVDS receivers are the only Low Power versions in the ALCAPONE0. In ALCAPONE1 all LVDS receivers are the Low Power versions.*

3.3 Power supply pins

Signal	BST	Dir	Type	Description
ShuntRes	N	In	Power	Connection for 180Ω resistor for shunt-regulator power
SuppVdd (= vdda!)	N	Out	Power	Connection of Vdd out for Power Supply Circuit, 2.5V ± 200mV (Max.)
SuppOn[3]	Y	In	CMOS	Input to determine if power supply must be on after Pow-erOn ('H'= on, internal pull-down)

_POnRESET[3]	Y	Out	CMOS	PowerOn RESET out (Active Low during power-on ~250µs), 8mA
DriveOut	N	Out	Analogue	Drive of power transistor for power supply (max. 140µA)
CurrDet	N	In	Analogue	Current detection input of power supply circuit
Vmeas	N	In	Analogue	Measure Voltage input for power supply circuit
RefOut	N	Out	Analogue	Reference voltage out (1.25V) for ALABUF and HAL25 analogue output (max. 100uA)
Gnd! & vdd!	N		Power	Power for all circuits but the power supply circuit + it's DAC, and reference circuits.

3: SuppVdd powers the BST cells for these pins.

3.4 Miscellaneous pins

Signal	BST	Dir	Type	Description
_ResetAC	N	In	CMOS	Resets the AC coupled input circuits and is the PowerOn reset input for the logic ('L'=Reset)
BuffEn	Y	Out	CMOS	Enable signal for analogue buffer on SupplyCards, 20mA SRL
ErrPSide	Y	In	CMOS	Error input from the Pside (also for AC)
ErrNSide	Y	In	CMOS	Error input from the Pside (also for AC)
SelectSwitch	Y	Out	CMOS	Select signal for analogue multiplexer ('H'=Select), 8mA SRL
TokenChP & TokenChN	Y	In	LVDS	Token check input for end of readout
ErrorC	Y	Out	CMOS	Error signal out, EndCap internal error flag ('L'=error, wired OR function), 20mA open drain
Adc<0:2>	N	In	Analogue	AdcInput to monitor analogue values
Adc<3>	N	In	Analogue	AdcInput to 100k NTC (NTC connects to gnd!) Input is connected to 9.96A current source.
OscIn	N	In	CMOShyst.	Connect to RC load, input with hysteresis
OscOut	N	Out	CMOS	Add RC load (R=10k,C=1nF for ~30kHz)

3.5 Test Pads (internal pads in chip area)

Signal	Dir.	Value	Description
BandRef	Out	1.155 V	Voltage of BandGap reference
Vsupp	Out	0.9-1.3V	Reference for power supply circuit
DacBias	Out	1.6V	Reference for the DAC's and the NTC current
VrefOut	Out	1.25V	Reference for Power supply circuit
ADCdata<0:7>	Out	CMOS open drain	ADC data (1mA)

3.6 Specials

3.6.1 ALCAPONE0:

- "**SuppOn**" defines whether the supply circuit is always on after Power-On or not. This is only the case on the Interface Card. This signal also defines that some of the LVDS receivers and drivers will be enabled or not. See table below.

Signal name	In/Out	SuppOn "1"	SuppOn "0"
TCK_P/TCK_N	In	Enabled	Disabled
TDI_P/TDI_N	In	Enabled	Disabled
TMS_P/TMS_N	In	Enabled	Disabled
TRST_P/TRST_N	In	Enabled	Disabled
TDO_P/TDO_N	Out	Enabled	Disabled
TokenChP/TokenchN	In	Disabled	Enabled
ErrorP/ErrorN	Out	Enabled	Disabled

- "**ResetAC**" is used to set the AC coupled inputs into a defined state. This signal also is used as *Power-On*-Reset for the control logic inside the ALCAPONE. With this signal, all registers can be initialized.

3.6.2 ALCAPONE1:

The signals SuppOn and the LVDS/CMOS selection for the *JTAG* inputs are defined differently in the ALCAPONE1. This is because of the "second" chip in the EndCap module; the power supply circuit should switch on automatically, but for JTAG the CMOS signals must be used and **not** the LVDS signals.

In ALCAPONE1, the JTAG LVDS/CMOS input selection is made with the LVDS_CMOS input.

- "**SuppOn**" defines whether the supply circuit is always on after Power-On or not. This is only the case on the Interface Card. This signals also defines that some of the LVDS receivers and drivers will be enabled or not. See table below.

Signal name	In/Out	SuppOn "H"	SuppOn "L"
TokenChP/TokenchN	In	Disabled	Enabled
ErrorP/ErrorN	Out	Enabled	Disabled

- **The LVDS_CMOS input** defines whether the LVDS or the CMOS I/O's are used for the JTAG communication. LVDS_CMOS='H' means LVDS, and 'L' means CMOS.

Signal name	In/Out	LVDS_CMOS "H"	LVDS_CMOS "L"
TCK_P/TCK_N	In	Enabled	Disabled
TDI_P/TDI_N	In	Enabled	Disabled
TMS_P/TMS_N	In	Enabled	Disabled
TRST_P/TRST_N	In	Enabled	Disabled
TDO_P/TDO_N	Out	Enabled	Disabled

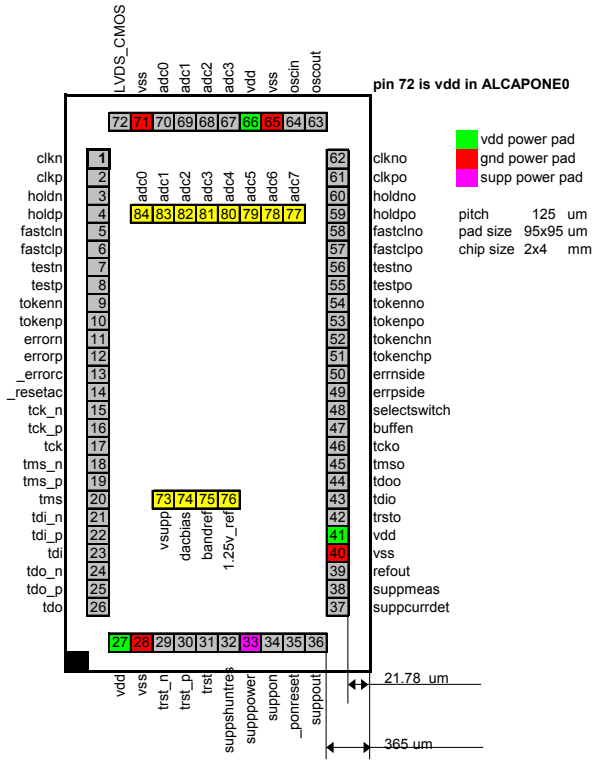


Figure 7 ALCAPONE1 pins

4 Connections by functional position in EndCap:

The ALCAPONE chip is used in 3 different functional positions in the EndCap:

1. Interface on GND level, buffer between EndCap and data-acquisition and -control.
2. AC coupling to P- or N-side, coupling from GND level to detector bias level to 14 hybrid controllers.
3. Buffer to detector hybrid, the actual controller and buffer for one of the 14 hybrids.

Depending on the position, the following chip connections are made:

1. -**SuppOn to Vdd:** This defines that the regulator is always on and cannot be controlled via JTAG. It is used to power the chip itself, and the 7 ALABUF chips inside the EndCap (2.5V).
   -**LVDS_CMOS='H':** JTAG signals use LVDS I/O's on GND level. CMOS inputs left open.
   -**The chip is powered by it self** from the control power at GND level.
2. **-SuppOn to Vdd:** The regulator is used to power itself and the ALCAPONE chips on the Supply Cards.
   -LVDS_CMOS='L': JTAG signals use CMOS I/O's on detector bias level (AC coupling), LVDS inputs are not enabled.
   -The chip is powered by itself from P- or N-side control power at detector bias level.
3. **-SuppOn not connected=('L')** (gnd): The supply circuit **must** be controlled via JTAG.
   -LVDS_CMOS='L': JTAG signals use CMOS I/O's on detector bias level but direct connected to the previously mentioned ALCAPONE. The LVDS inputs are switched off.
   -The chip is powered by the ALCAPONE in 2.

In all cases the _ResetAC is used to reset the AC coupled inputs, not connected AC compatible inputs are also set to a defined state.

5 Bugs & “features”:

1. RESET for the ADC is _POnReset internal from power supply circuit. This means that the power supply must be on and functional before the ADC can work. This is not the preferred behavior and it is changed to the Reset_AC input.
2. ADC range not correct. Reference of Bandgap cell is in reality lower that in simulation. By manually increasing the voltage at the test pad the range can be corrected. The bias circuit is changed to create a better ADC reference.

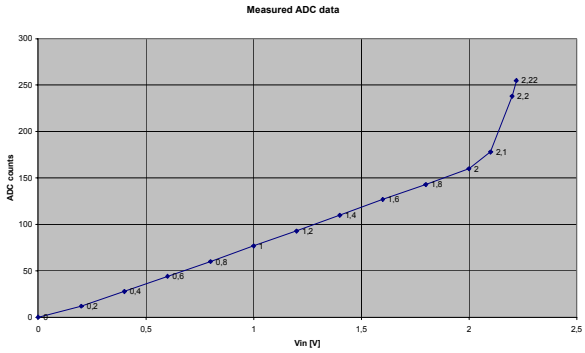


Figure 8 Adc input **range**

3. As result of the previous point, the POWERREFERENCE is also a bit out of range, although the default programmed required output voltage of the regulator is ok (~2.57V). The bias circuit is changed.
4. The LVDS P- and N outputs for the CLK, Token, FastClear, Hold and Test are inverted connected. Output pad cells are mirrored to solve this.
5. On some chip’s we see a bounce on _POnReset. This makes the logic to automatically switch off the power circuit. The bounce can be a result of the slow original signal from the supply circuit. This is solved by adding a buffer with hysteresis to the circuit to generate the _POnReset.
6. The power supply oscillates when connected to the ALCAPONE Vdd itself. A “large” capacitance is found between the ALCAPONE Vdd and the bias for the power supply reference bias. This is improved by adding a separate bias circuit for the ALCAPONE and the supply circuit.
7. The OR function in the LVDS/AC_CMOS inputs (JTAG) can block the correct input signal. Now a multiplexer is implemented and when in SuppOn mode, the LVDS inputs are selected and otherwise the AC_CMOS inputs are selected.
8. The AC_CMOS input did not work reliable. By adding an external resistor of 20Ω to 1kΩ, the circuit behaves correct (it creates hysteresis). Now a 400Ω resistor is integrated in the chip.
9. The SuppOn signal must be high on the Interface card ALCAPONE chips. The first one receives the JTAG signals via LVDS. However, the other two via CMOS signals using AC-coupling. In the latter case, SuppOn is high but the CMOS JTAG inputs must be used instead of the LVDS inputs. This requires an additional mode for the input selection. Solved with extra LVDS_CMOS input.
10. The Token signal must be synchronous with the falling edge of the ALCAPONE CLK signal. Now it is with the rising edge, and the signal is not sampled (rising edge) with the succeeding ALCAPONE chip.
11. The FastClr input signal is active low, assumed was active high. The input cell has changed and the output pins are switched. The internal FastClri signal is active high. This is the value read by the BST registers.
12. In case delay is “off”, TokenOut must be TokenIn without any delay. The delay was 1 clock cycle and this must be solved. A token feed-through switch (controlled via JTAG) will be added.
13. The errorLatched flags do not work. This is caused by the design software, which did not recognize wrong connections in the layout of the chip. Now this is known, we can manually find these errors and correct them. With the latest software version, the errors are detected.
14. When the RESET instruction was selected, the JTAG chain was interrupted. Since there is no data register for this instruction, it was not multiplexed internal. Solved in ALCAPONE1.

Measured values	**Nominal**	**Deviation**
Vshuntreg	2,53 V	20 mV
Vout	2,54 V	30 mV
Overcurrent Timer	34 us	3 us
Startup Timer	320 us	25 us
I max (R=76mOhm)	250 mA	35 mA

6 ALCAPONE Test description

Always *start with _ResetAC! This is the power on reset for the AC coupled input circuits, the ADC, and the logic in the chip.*

6.1 Supply & Shunt test:

1. De 'Shuntregulator'.

Controleer of de spanning op de aansluiting 'SuppShuntRes' 2.5V +/- 25mV is. Als deze met een serie-weerstand van 180 Ohm gesloten op een oplopende voedingsspanning van 3 tot 6 V. Deze voedingsspanning wordt in bedrijf ook gebruikt om de vermogenstransistor die door de supplyregulator wordt aangestuurd, te voeden. Deze voedingsspanning staat dan op 3V.

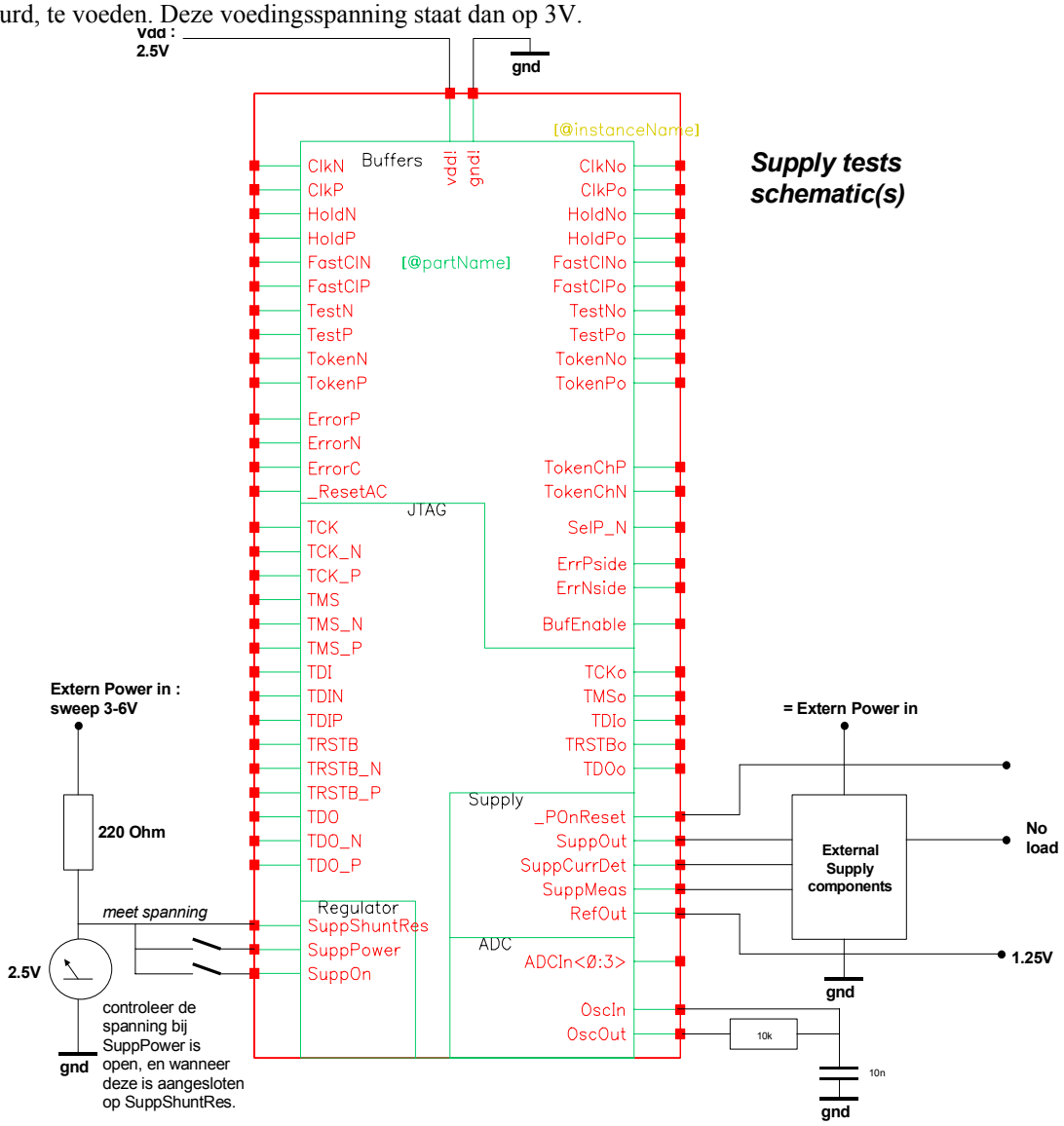


Figure 9 testschema voor 1. en 2.

2. De 1.25V referentiespanning. (RefOut).

Deze referentiespanning wordt gebruikt als 'common-mode' spanning voor de analoge HAL25 output op de hybrid. Dit circuit wordt gevoed door de VDD (2.5V). Controle of deze spanning 1.25V +/_-50mV is. Voor verdere tests is VDD niet meer noodzakelijk.

3. De 'Supplyregulator'.

A. De 'Supply regulator' heeft twee opstart modes: **remote on/off en auto-start**.
De remote on/off wordt intern door de' JTAG' controller gestuurd. In de auto-start mode moet de 'SuppOn' ingang "hoog" zijn. In de praktijk worden dan de 'SuppPower', de 'SuppShuntRes' en de 'SuppOn' doorverbonden.
Voor controle van het opstarten en de opstarttimer in de regulator is 2.5V voedingsspanning nodig op de 'SuppPower'.
Na het aanbieden van 2.5V op de 'SuppOn' zal de regulator opstarten. Ongeveer 300uSec. later zal 2.5 V op de 'POnRESET' staan. Controle of deze tijd tussen de 250uSec. en de 350uSec.

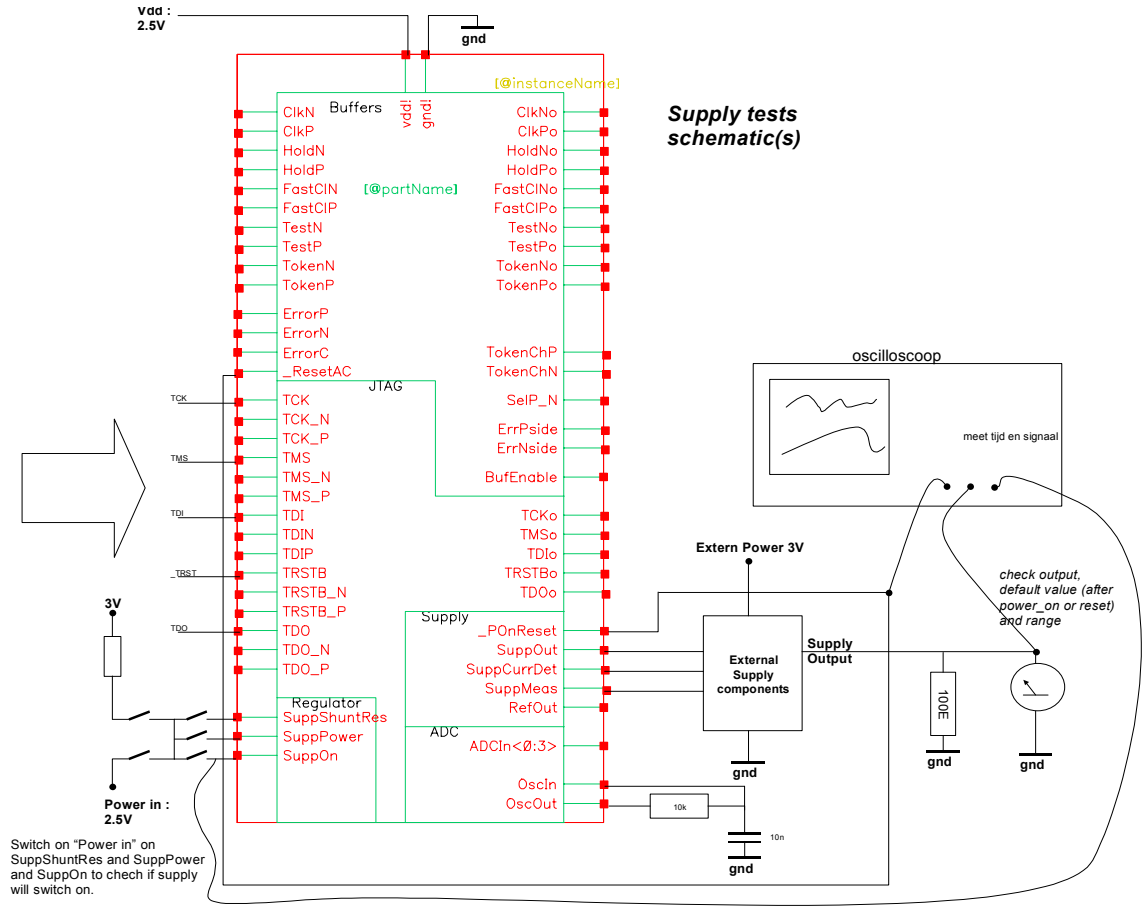


Figure 10 testschema voor 3A, C en D

B. Voor controle van de undervoltageprotector de 'SuppPower' en de 'SuppOn' met de voedings-spanning verbinden. Deze voedingsspanning in ± 0.2ms opregelen.
Controle of de regulator pas boven een aangeboden spanning van 2.1V +/- 50mV opstart. Controle of de regulator uitgaat als de aangeboden spanning lager is dan 2.1V +/-50mV.

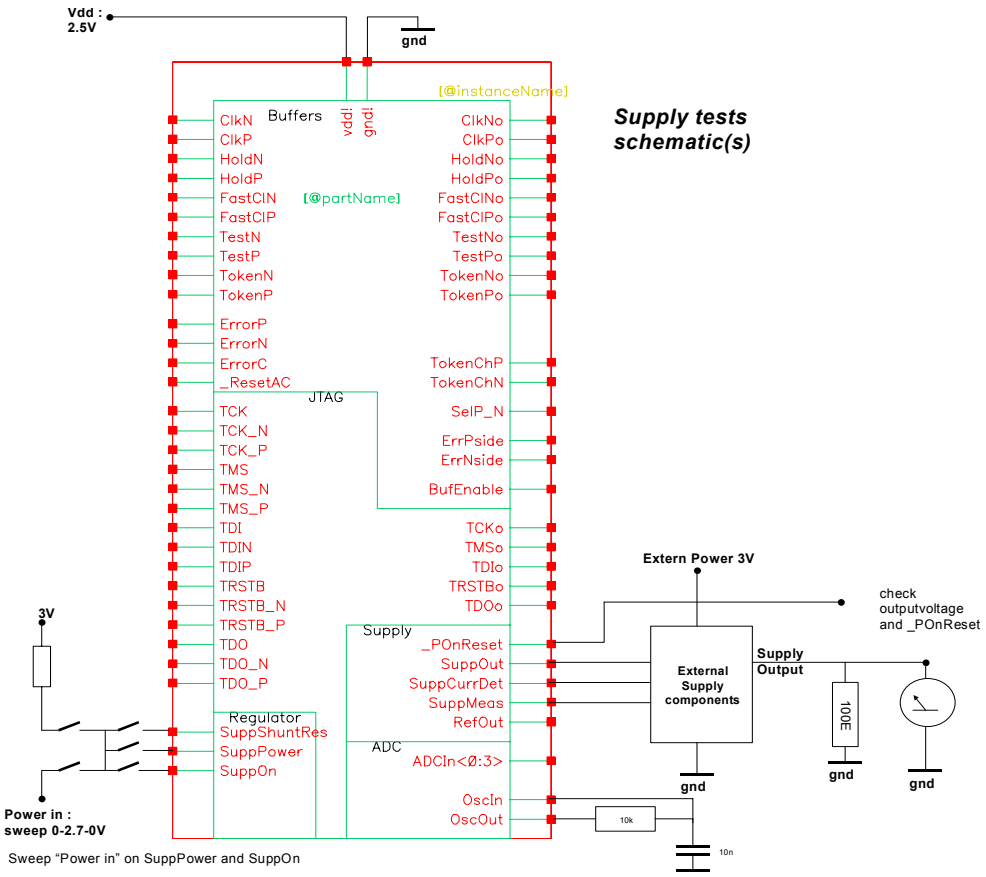


Figure 11 testschema voor 3 B.

C. Voor de controle of de regulator aan en uit kan worden gezet door de 'JTAG" controller is het nodig dat 'SuppOn' niet met 'SuppPower' is doorverbonden. Als SuppPower "laag" (interne pull down) is, is de regulator in de remote on/off mode. Controleer of de regulator met behulp van de 'JTAG" controller aan en uit te zetten is. Dit kan pas nadat de 'JTAG' logica een RESET van de regulator heeft gekregen. Deze RESET is '_POnRESET' en is dan doorverbonden met '_RESETAC'.

D. Voor controle van het bereik van de uitgangsspanning van de regulator is het nodig dat m.b.v. 'JTAG' de DAC voor de regulator wordt ingesteld. De voorinstelling is zodanig dat de uitgangsspanning bij opstarten ± 2.5V bedraagt. Dit kan pas nadat de 'JTAG' inputs een RESET van de regulator heeft gekregen. Deze RESET is de '_POnRESET' aan '_RESETAC'.
Controleer of de uitgangsspanning is in te stellen tussen 2V +/- 25mV en 2.8V +/- 25mV en ***alle*** DAC stappen (1 bit = ± 1,5 mV).

E. Voor controle van de maximale stroom kan de vorige meting gebruikt worden. Met een oplopende 'loadcurrent 'zal de regulator op een bepaald moment de uitgangsspanning afschakelen. De maximale stroom is ongeveer 330mA. Als de regulator door 'overcurrent' is afgeschakeld, blijft deze in afgeschakelde toestand ook al wordt de load losgekoppeld. Om de regulator weer te kunnen opstarten moet deze door de 'JTAG' controller uit en weer aan worden gezet of de voedingsspanning van de regulator (SuppPower) moet uit en weer aan worden gezet.
De maximale stroom is niet afhankelijk van de ingestelde uitgangsspanning.
Controle van die 330mA +/- 30mA. Tijdens deze meting kan de 'load regulation' worden gemeten door de uitgansspanning te meten als functie van de uitgansstroom.
Controleer of de uitgangsspanning niet meer dan 5mV zakt.
Controleer of het AC component niet meer dan 10mV bedraagt.

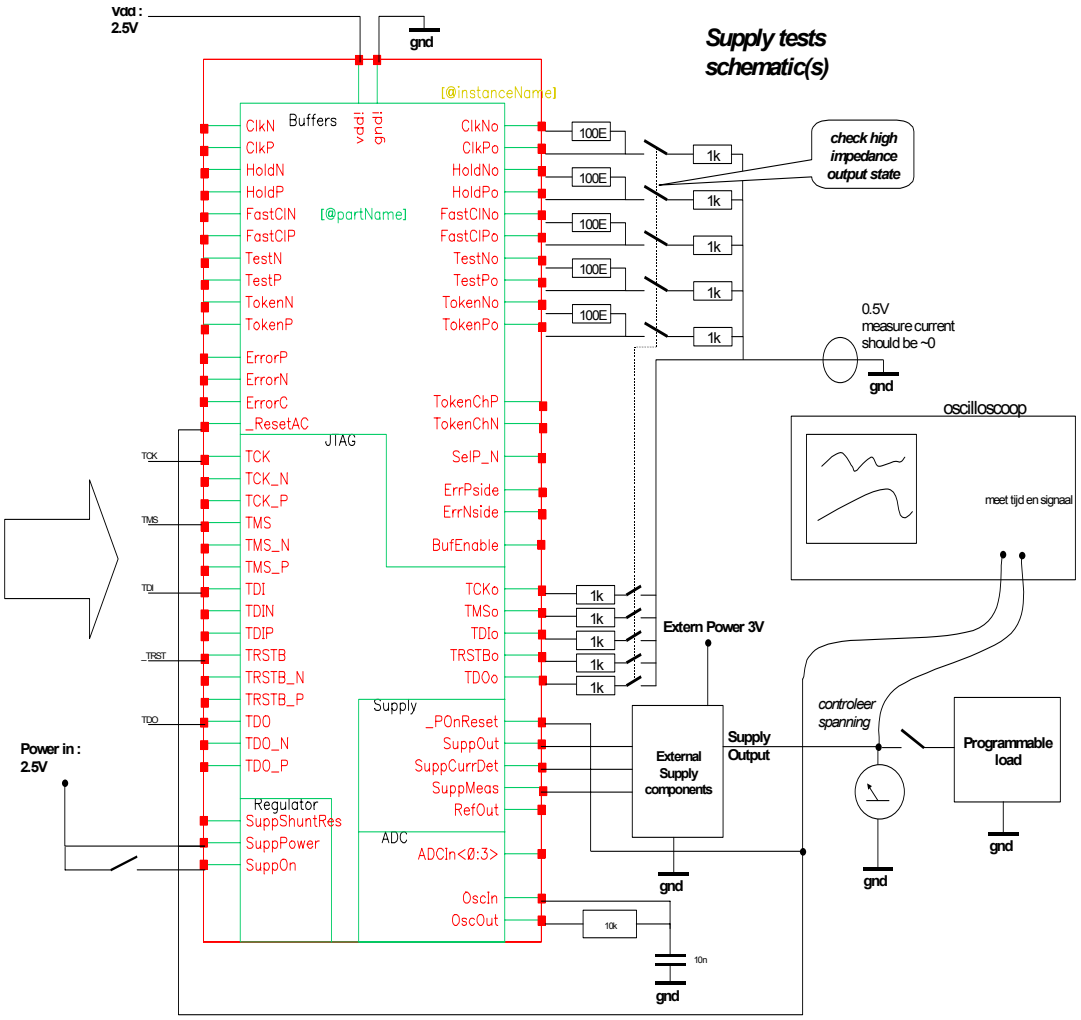


Figure 12 testschema voor E. en F. en 6.2 B.

F. Voor controle van de ‘over current timer’ kan ook de vorige meting gebruikt worden. Het is dan alleen noodzakelijk dat de maximale stroom overschreden wordt zolang de tijd van de ‘start-up timer’ verstreken is. De tijd tussen het verschijnen van de ‘_POnRESET’ en het zelfstandig afschakelen van de uitgangsspanning is de tijd die bepaald wordt door de overcurrent-timer. Deze is ongeveer 30µs.
Een andere manier om de ‘overcurrent-timer’ te testen is om na ongeveer 400uSec. een ‘loadcurrent’ af te nemen die hoger is dan de maximale stroom. (500mA). De regulator zal deze stroom ongeveer 30µs leveren en dan uitschakelen. Controleer of deze tijd tussen de 25µ en de 35µs ligt.

6.2 Receiver & Buffer test

A. Controleer de doorgaande buffers en drivers (LVDS en CMOS), en controleer de LVDS_CMOS selectie van de JTAG inputs m.b.v. de LVDS_CMOS input pin.

B. In de chip wordt het ‘POnRESET’ signaal van de regulator gebruikt als ‘disable’ signaal voor een aantal LVDS buffers en CMOS buffers. (Zie 3.1 en 3.2) De betreffende LVDS buffers zijn ‘ClkPo’ en ‘ClkNo’, ‘HoldPo’ en’ HoldNo’, ‘FastClPo’ en ‘FastClNo’, ‘TestPo’ en ‘TestNo, ‘TokenPo’ en ‘TokenNo’.
De betreffende CMOS buffers zijn ‘TCKo’,’ TMSo’,’TDOo’,’ TRSTBo’ en ‘_PonRESET’.
Controle of deze buffers in hoog-ohmige toestand zijn als de regulator “uit” staat en of deze buffers “actief” zijn als de regulator “aan” staat (zie Figure 12).

6.3 ADC test

A. **Oscilator test**: 10k Resistor and 10nF cap to gnd => Vl= 0.4V, Vh=1.9V, freq. = ~3.1kHz
ADC **clocked**: op Osc in: 10-100kHz check ADC output met 0.5 en 1.5V.

B. **ADC test**: Zet het ADC testmode bit (JTAG AlcaponeStatusRegister) en de DAC van de ADC zal nu continu aftellen (check ramp met scope). Deze spanning kan gemeten worden aan een input die m.b.v. het ADC input register is geselecteerd. Niet input 3 want daar zit een stroom output aan. De inputs 0,1 en 2 controleren. Met 100k aan input 3 de ADC uitlezen. Meet ook 2 spanningen voor iedere input (bv. 0.5 en 1.5V)

6.4 JTAG test

A. Controleer verbinding met JTAG. Lees alle bits, schrijf naar alles en controleer of dit goed gaat volgens de beschrijving van alle registers.

B. Controleer of the reset functies werken, zie 2.7.

C. Controleer of m.b.v. de Extest instructie de aangeboden signalen goed de chip bereiken. En doe hetzelfde met Extest of alles er goed uitkomt.

D. Doe m.b.v. INTEST een controle van de Token controle logica.

6.5 Readout test

Controleer de Token Out delays met alle mogelijke waarden. Controleer hierbij ook SelectSwitch en en BufEnable volgens Readout and Token (delays) op pag. 5

6.6 Test time calculation

	EndCaps	IntCard	SuppCard	sub. tot.	spare [%]	yield [%]		required	
	144	1	7		50	60			
Number of IC's									
ALABUF	7	0	1	1008	504	1008		**2520**	ALABUF2
ALCAPONE	31	3	4	4464	2232	4464		**11160**	ALCAPONE1
ALCAPONE's for LHC	500			500	250	500		1250	

				prod. Information:	eng. Run	prod. Run
nodig:	nr of ALABUF	2520	2500		1400	4344
	nr of ALCAPONE	12410	13000		520	12480

Tijd inclusief wafer handling.

ALABUF test

Test periode	4	weken		
Test duur	20	dagen van 8 uur (6 eff.)	120	uur
Test tijd per chip	**2**	**minuten en**	**39**	**seconden**

ALCAPONE test

Test periode	8	weken		
Test duur	40	dagen van 8 uur (6 eff.)	240	uur
Test tijd per chip	**1**	**minuten en**	**6**	**seconden**

		eng. run	prod. run	
file size per ALABUF	700 kB	957	2969,531	MB
file size per ALCAPONE	200 kB	104	2437,5	MB

7 References

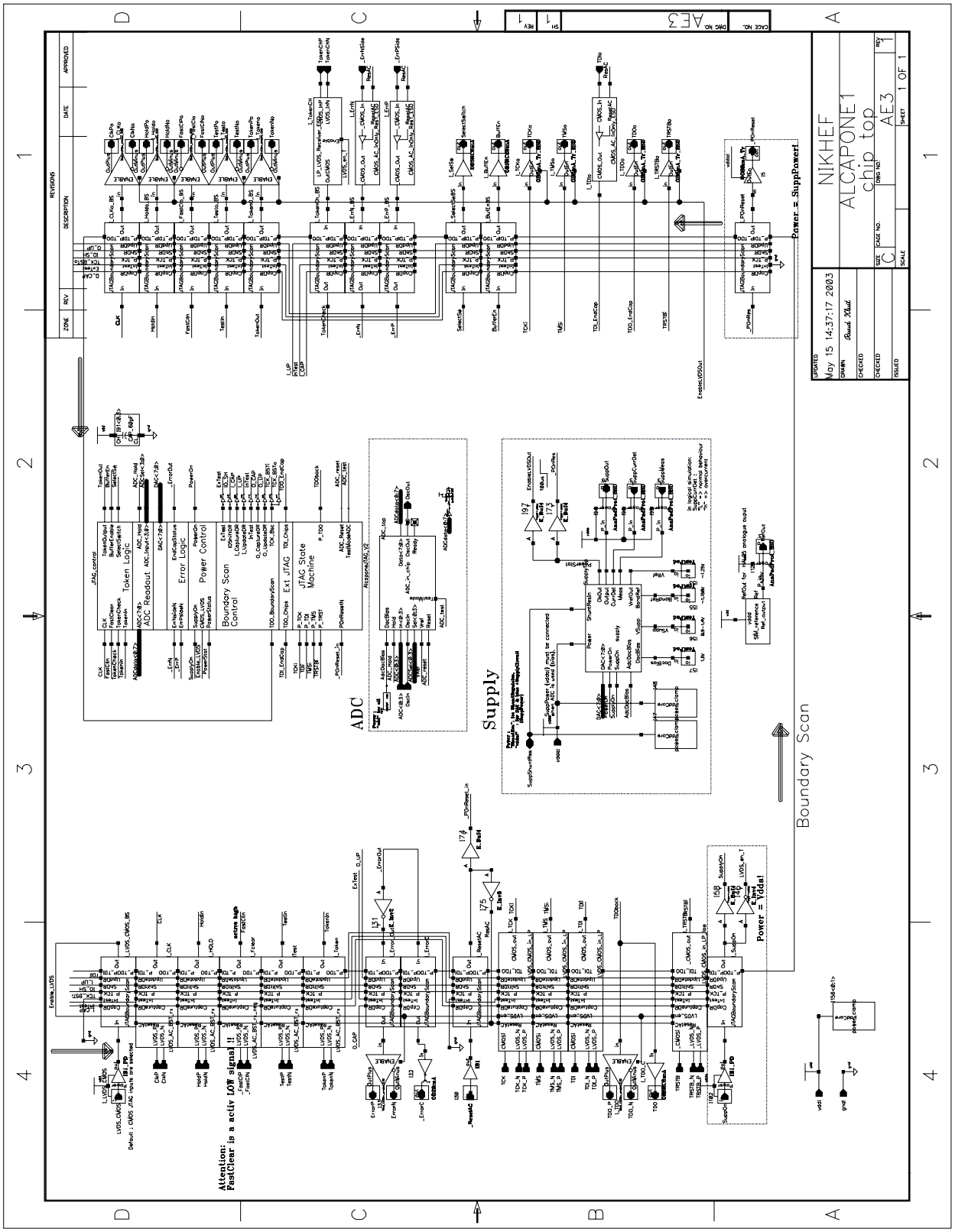
[1] HAL25 Hardened ALICE front-end chip in 0.25u CMOS technology. User manual.

[2] Design of ladder EndCap electronics for the ALICE ITS SSD.

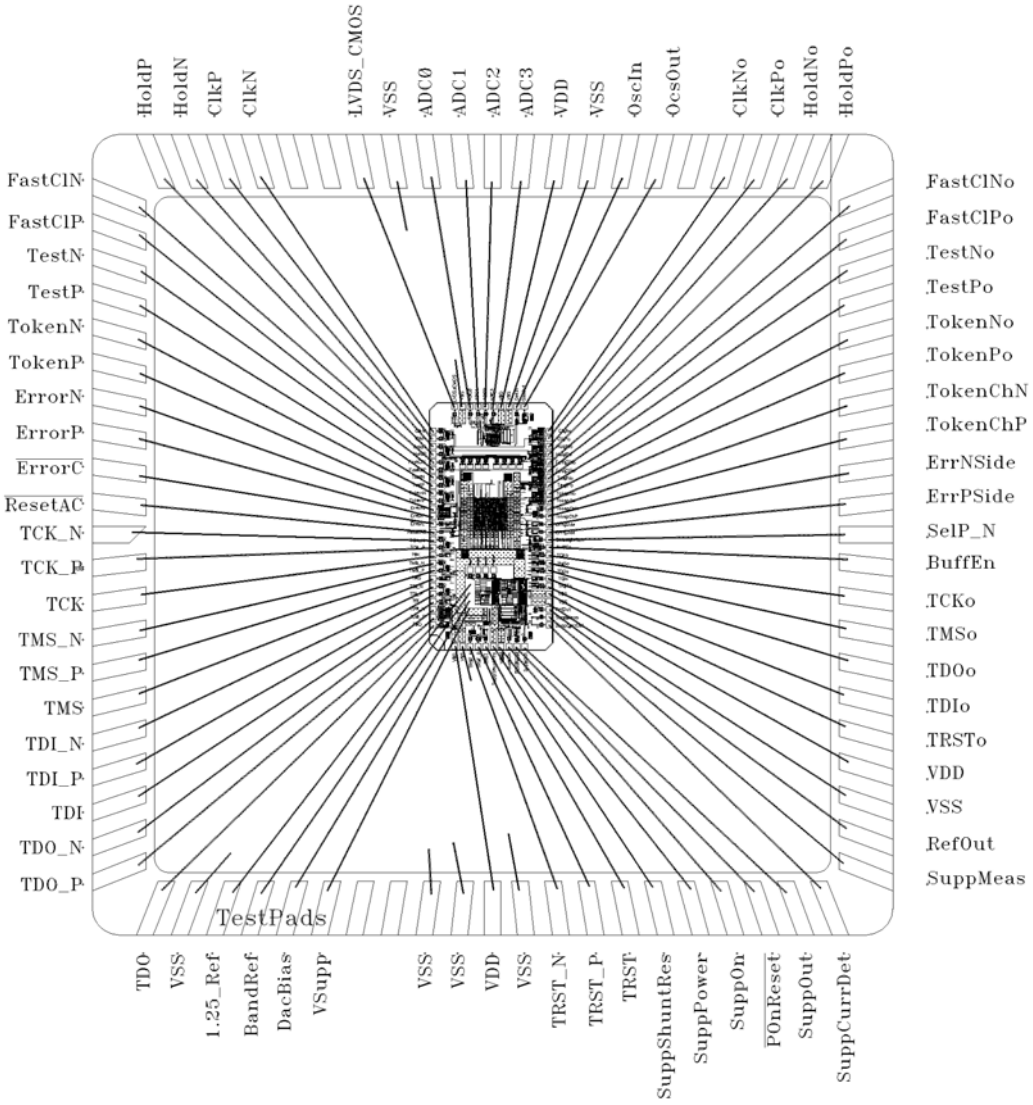
[3] Progress report on development of the Low Power LVDS Receiver in 0.25u CMOS technology for the ALICE Silicon Strip Detector (SSD). V. Gromov (vgromov@nikhef.nl), R. Kluit, ET NIKHEF, Amsterdam, 20 January 2003.

8 Appendix

Appendix 1 ALCAPONE**1 top schematic**

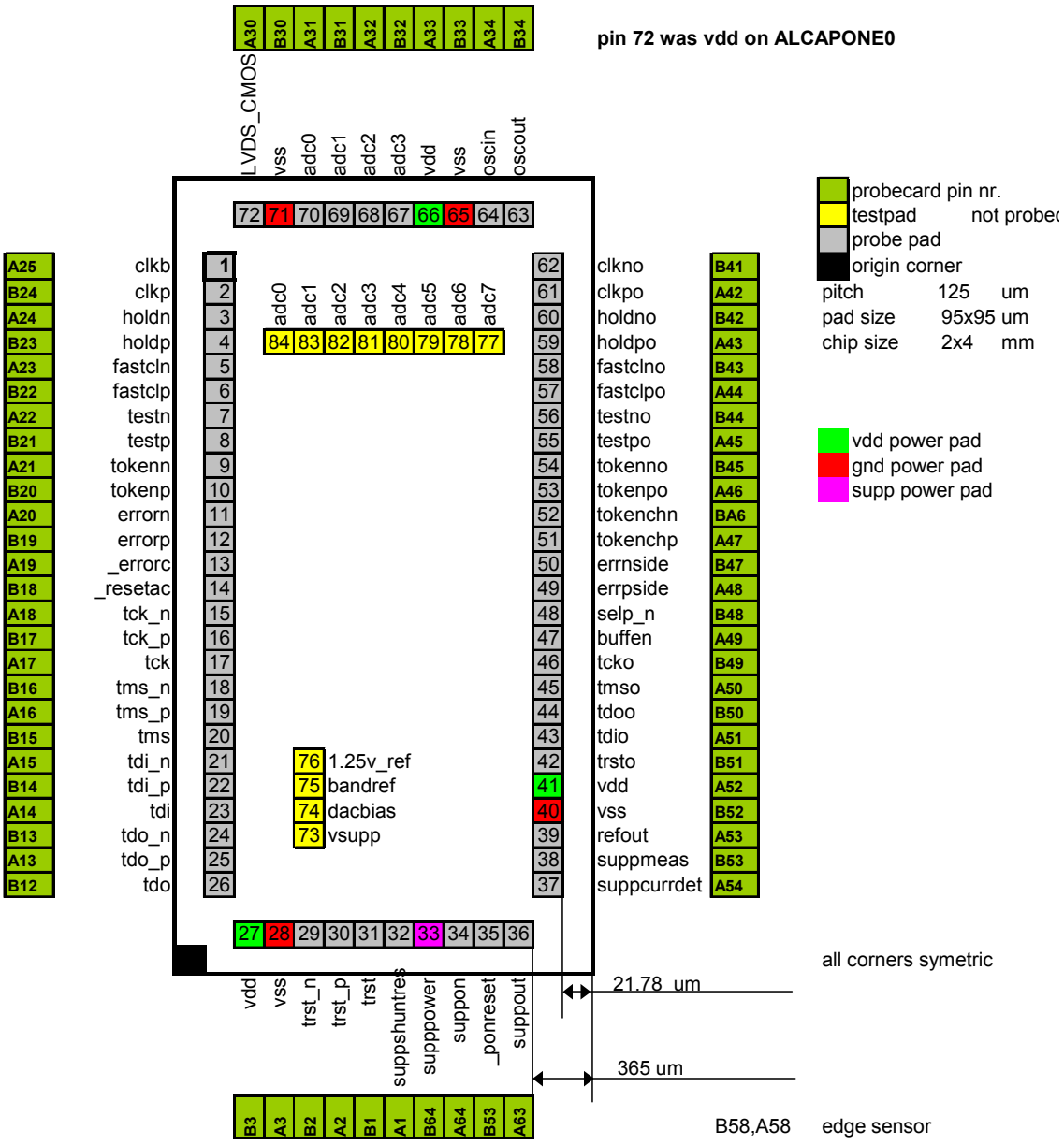


Appendix 2 ALCAPONE**0 bond diagram in PLCC84**



Appendix 3 ALCAPONE**0 Pads and probe numbers**

NIKHEF ALCAPONE1 pins



Appendix 4 ALCAPONE**0 layout**

Appendix 5 ALCAPONE**1 layout**