To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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April 1, 2003

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User's Manual

SH7750R E10A Emulation Memory Board (HS7750REJH01H)

User's Manual

Renesas Electronics
www.renesas.com

Rev.1.0 2002.11

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READ FIRST

• READ this user's manual before using this emulation memory board.

• KEEP the user's manual handy for future reference.

Do not attempt to use the emulation memory board until you fully understand its mechanism.

Emulation Memory Board:

Throughout this document, the term "emulation memory board" shall be defined as the following products produced only by Hitachi, Ltd. excluding all subsidiary products.

- Emulation memory board
- Power cables supplied together with this emulation memory board

The user system or a host computer is not included in this definition.

Purpose of the Emulation Memory Board:

This emulation memory board is an optional board for supporting the development of the systems using Hitachi microcomputer SH7750R. This emulation memory board must only be used for the above purpose.

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This emulation memory board is not authorized for use in MEDICAL, atomic energy, aeronautical or space technology applications without consent of the appropriate officer of a Hitachi sales company. Such use includes, but is not limited to, use in life support systems. Buyers of this emulation memory board must notify the relevant Hitachi sales offices before planning to use the product in such applications.

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Target User of the Emulation Memory Board:

This emulation memory board should only be used by those who have carefully read and thoroughly understood the information and restrictions contained in the user's manual. Do not attempt to use the emulation memory board until you fully understand its mechanism.

It is highly recommended that first-time users be instructed by users that are well versed in the operation of the emulation memory board.

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Figures:

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Limited Anticipation of Danger:

Hitachi cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this user's manual and on the emulation memory board are therefore not all inclusive. Therefore, you must use the emulation memory board safely at your own risk.

SAFETY PAGE

READ FIRST

• READ this user's manual before using this emulation memory board.

• KEEP the user's manual handy for future reference.

Do not attempt to use the emulation memory board until you fully understand its mechanism.

DEFINITION OF SIGNAL WORDS

This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

⚠ DANGER **DANGER** indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.

⚠ WARNING **WARNING** indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

⚠ CAUTION **CAUTION** indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.

CAUTION **CAUTION** used without the safety alert symbol indicates a potentially hazardous situation which, if not avoided, may result in property damage.

NOTE emphasizes essential information.

⚠ WARNING

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

1. **Do not repair or remodel the emulation memory board by yourself for electric shock prevention and quality assurance.**
2. **Always switch OFF the emulator product, the emulation memory board, and the user system before connecting or disconnecting any CABLES or JUMPERS.**
3. **Always switch OFF the emulation memory board and the user system before connecting or disconnecting the IC socket or the user interface connector.**
4. **When connecting the user interface connector to the IC socket on the user system, ensure that pin 1 on both sides are correctly aligned.**
5. **Supply power according to the power specifications and do not supply an incorrect power voltage. Use only the provided power cables.**

Warnings on Emulation Memory Board Usage

Be sure to read and understand the warnings below before using this emulation memory board. Note that these are the main warnings, not a complete list.

⚠ WARNING

Always switch OFF the emulator product, the emulation memory board, and the user system before connecting or disconnecting any CABLES, JUMPERS, or PARTS. Failure to do so will result in a FIRE HAZARD and will damage the emulator product, the emulation memory board, or the user system, or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

CAUTION

Position the emulator product, the emulation memory board, and the user system so that no cable is bent or twisted. A bent or twisted cable will impose stress on the user interface leading to connection or contact failure. Make sure that the emulation memory board is placed in a secure position so that it does not move during use nor impose stress on the user interface.

Preface

Thank you for purchasing the SH7750R E10A emulation memory board. The emulation memory board supports the development of systems using Hitachi microcomputer SH7750R.

Read this user's manual before using the emulation memory board, and keep the manual handy for future reference.

CAUTION

READ this user's manual before using the emulation memory board. Incorrect operation or connection will damage the emulation memory board and the user system. The USER PROGRAM will be LOST.

Related Manuals:

- SH7750 Series Hardware Manual
- SH7750R E10A Emulator User's Manual

Related Hardware: SH7750R E10A Emulators

- HS7750RKCM01H
- HS7750RKCI01H

Contents

Section 1 Overview

The SH7750R E10A emulation memory board (hereinafter referred to as the emulation memory board) has an SH7750R (hereinafter referred to as the MCU), an interface connector (H-UDI port connector) for the E10A emulator (hereinafter called the emulator), a user interface connector, and SRAM devices. User programs can be emulated by connecting this emulation memory board to the emulator.

1.1 Features

1. The emulation memory board has emulator connectors and a user interface socket (YQPACK208SD). When the user system has a user interface socket (NQPACK208SD) but has no H-UDI connector, the user system can be connected to the emulator through the emulation memory board and the user program can be emulated.
2. The emulation memory board has SRAM devices that can be used as a substitute for the flash memory or EPROM devices. User programs can be emulated by connecting the emulation memory board to the emulator and supplying external power to the emulation memory board, even when no user system is connected to the emulator.
3. The emulation memory board has switches for various settings. These switches can select
   (1) the source of the power supplied to the emulation memory board,
   (2) the source of the clock supplied to the MCU on the emulation memory board, and
   (3) the destination of the CS0 signal output from the MCU.
4. The emulation memory board has a DIP switch, which can set the MCU's MD terminal status.

1.2 Components

Figure 1.1 and table 1.1 show the components of the emulation memory board. Please make sure you have all of these components when unpacking.

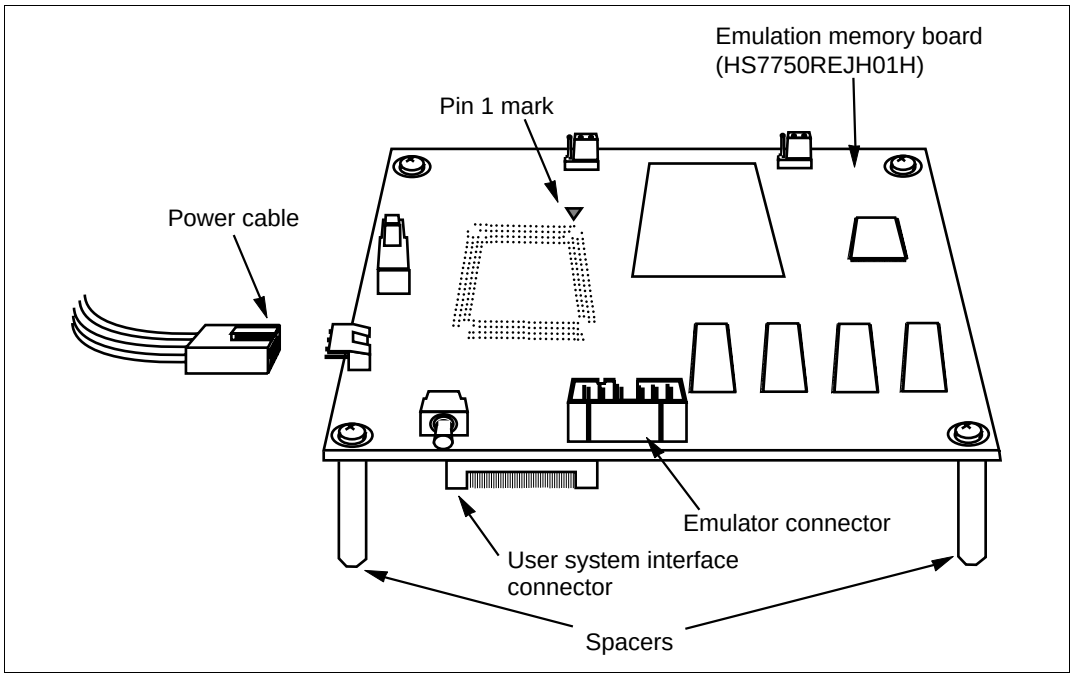


Figure 1.1 Emulation Memory Board Appearance

Table 1.1 Emulation Memory Board Components (HS7750REJH01H)

Item	Quantity	Notes
Emulation memory board	1	
Power cables (2 cables for 5 V and 2 cables for GND)	1 set	For an external power supply
Screws (M2 x 10 mm)	4	For fastening user interface socket
NQPACK208SD	1	User interface socket
Guide pins for NQPACK208SD	3	Provided for NQPACK208SD
Screwdriver	1	Provided for NQPACK208SD
Spacers (13 mm)	4	Fixed to the emulation memory board
SH7750R E10A Emulation Memory Board User's Manual	1	This manual

Section 2 Notes on Use

CAUTION

READ the following warnings before using the emulation memory board. Incorrect operation will damage the emulation memory board, the user system, and the emulator product. The USER PROGRAM will be LOST.

1. Cover the emulation memory board with a casing before using it. If using the emulation memory board without a casing, do not touch any component and prevent any short circuit.
2. Never place heavy objects on the emulation memory board.
3. Protect the emulation memory board from excessive impacts and stresses.
4. Do not supply power outside the specified voltage range.
5. When moving the emulation memory board, take care not to vibrate or damage it.
6. Supply power to the connected equipment only after connecting all cables. Cables must not be connected or removed while the power is on.
7. The emulation memory board may operate incorrectly due to static electricity. In this case, connect the GND patterns (the spacer-fixed sections at the four corners) on the emulation memory board to those of the user system through cables to discharge static electricity.
8. The emulation memory board can operate only when connected to the emulator; the emulation memory board cannot be used alone or only by connecting to the user system.

Section 3 Emulation Memory Board Functions

3.1 List of Functions

The functions of the emulation memory board are listed in table 3.1.

Table 3.1 Emulation Memory Board Functions

Function	Specifications
CPU clock	• Iϕ (CPU clock) = 240 MHz (max.) • Clock installed on the emulation memory board = 20 MHz (EXTAL input)
Substitution emulation memory	• Capacity: 4 Mbytes (8 blocks of 256 kwords x 16 bits) • •Independently used (disconnecting emulation memory board from the user system) 120 MHz (max.) = Bϕ (bus clock): Three wait cycles inserted by WCR2 •Connected (connecting emulation memory board to the user system) 66 MHz (max.) = Bϕ (bus clock): Two wait cycles inserted by WCR2 • Can be allocated to the CS0 area (Substitution memory area: H'00000000 to H'003FFFFF) • Data bus width can be selected from 16, 32, or 64 bits (8-bit width is not supported)
User interface	Supported package: 208-pin QFP
Crystal oscillator	Supported frequency for crystal oscillation: 16.7 MHz to 20 MHz
Switch settings	• SW3: Selects the power source • JP1: Selects the clock source • JP2: Selects the CS0 signal output destination
DIP switch settings	• SW2-1 to SW2-3: Selects the clock operating mode • SW2-4 and SW2-5: Selects the memory bus width • SW2-6: Selects the endian • SW2-7: Selects the memory type of area 0 • SW2-8: Selects the master or slave mode • SW2-9: Selects whether or not to use crystal oscillator
RESET switch	SW1: Issues a RESET signal
LEDs	• LED1: RESET and POWER • LED2: SHRDY and U-RUN • LED3: BREQ and NMI • LED4: STATUS1 and STATUS0

Table 3.1 Emulation Memory Board Functions (cont)

Function	Specifications
Power supply	• The emulation memory board can operate without connecting the user system by supplying +5 V through power connector J1 (IL-4P-S3FP2: manufactured by Japan Aviation Electronics Industry, Ltd.) The power connector pins work as follows: Pin 1: GND (black) Pin 2: 5 V (red) Pin 3: 5 V (red) Pin 4: GND (black) • When the emulation memory board is connected to the user system, supply +3.3 V from the VDDQ pin on the YQPACK208SD socket, respectively.

Notes: 1. For the substitution emulation memory, a 16-bit bus, a 32-bit bus, and a 64-bit bus are supported. Do not set the bus width to 8 bits when using the substitution emulation memory.

2. When allocating substitution emulation memory to an area, set WCR2 of the bus state controller to provide an appropriate cycle access state.

CAUTION

Restriction on Buffer Control Using the RD Signal:

RD signal output cannot be disabled from the emulator. Consequently, when the buffer control on the user system uses only the RD signal, data read from this emulation memory board and data output from the buffer may conflict. For this reason, when using the emulation memory board, be sure to control the data bus buffer of the user system with both the CS and RD (used in direction control) signals.

Section 4 Emulation Memory Board Operation

The emulation memory board has a RESET switch (SW1) for issuing a reset signal, a DIP switch (SW2) and jumper switches (JP1 and JP2) for various settings, a switch (SW3) for selecting the power source, a socket (SP1) for installing a crystal oscillator, and LEDs (LED1 to LED4) for signal monitoring. Figure 4.1 shows the switches, socket (SP1), and LEDs.

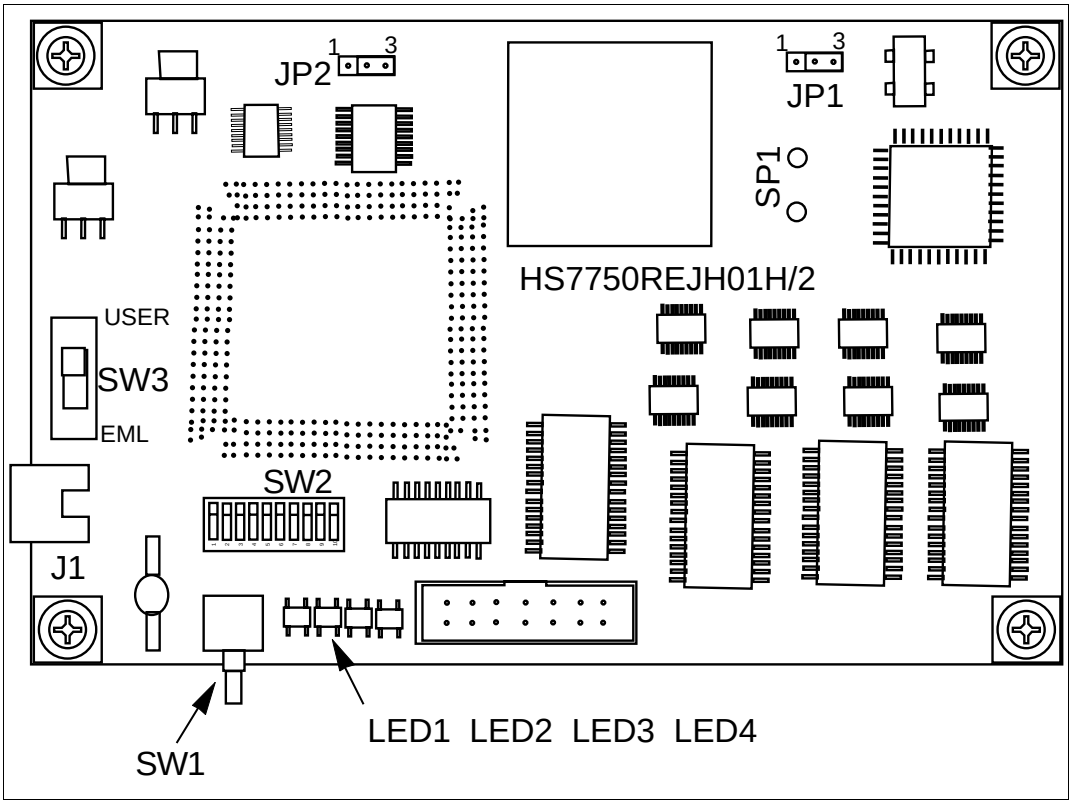


Figure 4.1 Switches, Socket, and LEDs

4.1 Switch Setting

4.1.1 Power Source Switch Setting

The SW3 selects whether the power for the emulation memory board is supplied from an external source or through the user interface.

⚠ WARNING

Always switch OFF the user system and the emulation memory board before power source switch (SW3) setting. Failure to do so will damage the user system and the emulation memory board. The USER PROGRAM will be LOST.

To supply power from an external source (sliding the switch to EML):

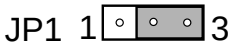
To supply power through the user interface (sliding the switch to USER):

4.1.2 Jumper Switch Setting

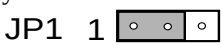
The emulation memory board has two jumper switches JP1 and JP2 for the following settings.

JP1 Function: The JP1 selects whether the clock for the MCU is supplied from the emulation memory board or from the user system. When installing a crystal oscillator into the socket (SP1) on the emulation memory board, open JP1. In this case, set the jumper connector on pin 3 as shown below so that the jumper connector will not be lost.

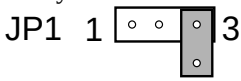
To supply the clock from the emulation memory board:



To supply the clock from the user system:



To install a crystal oscillator into the SP1 socket on the emulation memory board (JP1 is open):



Notes: 1. When closing 1-2 pins or 2-3 pins of JP1, turn switch 9 of SW2 ON (see table 4.6). When leaving JP1 open (installing a crystal oscillator), turn switch 9 of SW2 OFF.

2. The emulation memory board supports the external clock input through the EXTAL pin and the clock generated by the crystal oscillator connected to the EXTAL and XTAL pins. Therefore, be sure to supply the clock to the EXTAL pin when using the user system clock. If the clock is supplied to the XTAL, EXTAL2, or XTAL2 pin, the emulation memory board cannot operate.

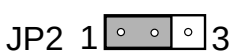
JP2 Function: The JP2 selects the CS0 signal output destination to specify whether the substitution memory on the emulation memory board or the memory of the user system is used.

CAUTION

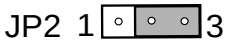
1. Restriction on Buffer Control Using the RD Signal:
RD signal output cannot be disabled from the emulator. Consequently, when the buffer control on the user system uses only the RD signal, data read from this emulation memory board and data output from the buffer may conflict. For this reason, when using the emulation memory board, be sure to control the data bus buffer of the user system with both the CS and RD (used in direction control) signals.

2. The substitution emulation memory is allocated to the 4 Mbytes from the start address of area 0. If the memory of the user system is allocated to area 0, that is, the same area as the substitution emulation memory, only the memory selected by the JP2 setting is used. When the substitution emulation memory is selected by JP2, the CS0 signal is not output to the user system.

To use the substitution memory on the emulation memory board:



To use the memory of the user system:



4.1.3 DIP Switch (SW2) Setting

The emulation memory board has one DIP switch for the following settings.

- Selecting the clock operating mode: Three switches
- Selecting the memory bus width: Two switches
- Selecting the endian: One switch
- Selecting the memory type of area 0: One switch
- Selecting the master or slave mode: One switch
- Selecting whether or not to install crystal oscillator: One switch

Tables 4.1 to 4.6 show the SW2 functions.

Note: For details on the mode control pins (MD0 to MD8), refer to the SH7750 Series Hardware Manual.

CAUTION
When a user system is connected to the emulation memory board, the DIP switch (SW2) settings are ignored, and the MD0 to MD8 signals input to the user system are used.

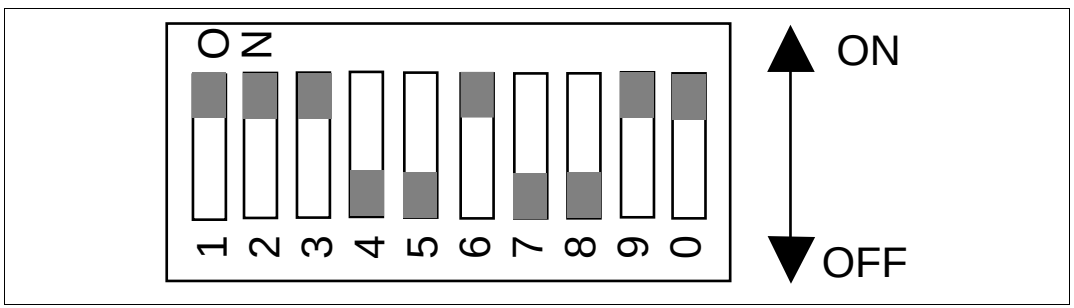


Figure 4.2 DIP Switch (SW2) Appearance and Settings at Shipment

Clock Operating Mode Setting: Select the clock operating mode as shown in table 4.1.

Table 4.1 Clock Operating Mode Setting (Switches 1 to 3 in SW2)

Switches in SW2 (Corresponding Mode Pins)				
1 (MD0)	**2 (MD1)**	**3 (MD2)**	**Clock Mode**	**Remarks**
ON	ON	ON	0	Initial setting at shipment
OFF	ON	ON	1	
ON	OFF	ON	2	
OFF	OFF	ON	3	
ON	ON	OFF	4	
OFF	ON	OFF	5	

Memory Bus Width Setting: Select the memory bus width for area 0 as shown in table 4.2.

Table 4.2 Memory Bus Width Setting (Switches 4 and 5 in SW2)

Switches in SW2 (Corresponding Mode Pins)			
4 (MD3)	**5 (MD4)**	**Memory Bus Width**	**Remarks**
OFF	ON	8 bits	Do not use this setting
ON	OFF	16 bits	
OFF	OFF	32 bits	Initial setting at shipment
ON	ON	64 bits	

Note: The substitution emulation memory does not support the 8-bit bus width.

Endian Setting: Select the endian as shown in table 4.3. Big endian is set when the switch is on, and little endian is set when the switch is off.

Table 4.3 Endian Setting (Switch 6 in SW2)

Switch in SW2 (Corresponding Mode Pin)		
6 (MD5)	**Endian**	**Remarks**
ON	Big endian	Initial setting at shipment
OFF	Little endian	

Memory Type Setting for Area 0: Select the memory type of area 0 as shown in table 4.4.

Table 4.4 Memory Type Setting for Area 0 (Switch 7 in SW2)

Switch in SW2 (Corresponding Pin) 7 (MD6)	Memory Type	Remarks
ON	MPX bus type	
OFF	Normal memory type	Initial setting at shipment

Note: When using the substitution emulation memory board, set this switch to OFF.

Master or Slave Mode Setting: Select the master or slave mode as shown in table 4.5.

Table 4.5 Master or Slave Mode Setting (Switch 8 in SW2)

Switch in SW2 (Corresponding Pin) 8 (MD7)	Master or Slave Mode	Remarks
ON	Slave mode	
OFF	Master mode	Initial setting at shipment

Crystal Oscillator Setting: Select whether or not to install a crystal oscillator as shown in table 4.6.

⚠ WARNING

Always switch OFF the user system and the emulation memory board before installing or uninstalling the crystal oscillator to/from the SP1 socket. Failure to do so will damage the user system, the emulation memory board, and the crystal oscillator. The USER PROGRAM will be LOST.

Table 4.6 Crystal Oscillator Setting (Switch 9 in SW2)

Switch in SW2 (Corresponding Pin) 9 (MD8)	Crystal Oscillator	Remarks
ON	Not installed	Initial setting at shipment
OFF	Installed	

Note: When setting this switch to ON, do not open JP1. When setting this switch to OFF, be sure to install a crystal oscillator into the SP1 socket on the emulation memory board.

SEL Switch:

Table 4.7 SEL Switch (Switch 0 in SW2)

Switch in SW2 (Corresponding Pin) 0 (-)	Function	Remarks
ON	Reserved	Initial setting at shipment
OFF	Reserved	

Note: Switch 0 in the SW2 is reserved. Use the initial setting at shipment and do not change it.

4.1.4 RESET Switch (SW1)

The emulation memory board has RESET switch for issuing a reset signal.

The /RESET signal to the MCU is obtained by ORing the reset signal from the RESET switch, the /RESET signal from the power-on reset circuit on the emulation memory board, and that from the user interface. The manual reset, on the other hand, is done using only the /MRESET signal from the user interface. Figure 4.3 shows the logic diagram for the reset circuit.

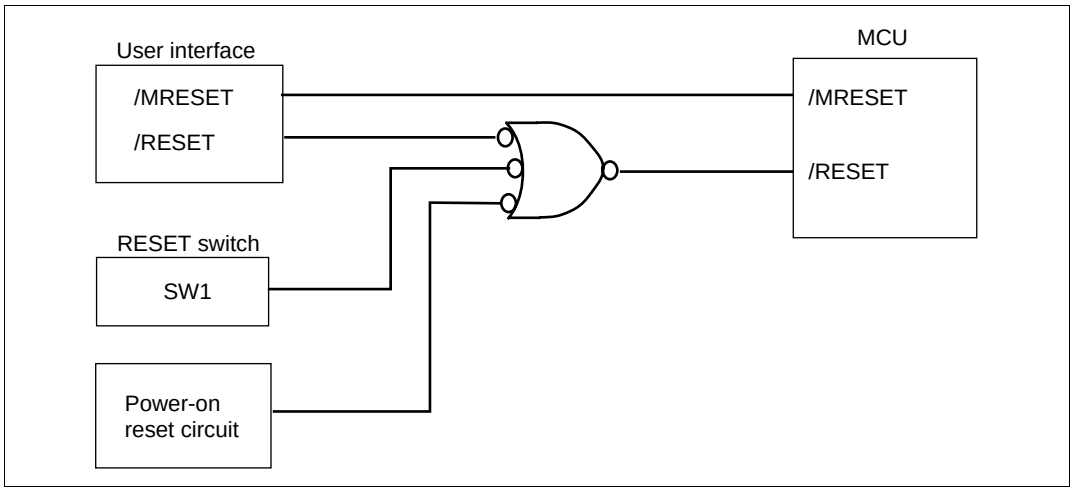


Figure 4.3 Reset Circuit Logic Diagram

4.2 Monitor LEDs

The emulation memory board has LEDs for monitoring the operating state. Table 4.8 shows the LEDs and the states to be monitored.

For details on STATUS1 and STATUS0 signals, refer to the SH7750 Series Hardware Manual.

Table 4.8 LEDs and States to Be Monitored

LED	Indication on the Board	LED Status	Remarks
LED1	RESET	Green LED lit when /RESET is asserted	
	POWER	Red LED lit when power is supplied	
LED2	SHRDY	Green LED lit when /RDY is asserted	
	U-RUN	Red LED lit when in USER RUN state	Signal: ASEBRKAK
LED3	BREQ	Green LED lit when /BREQ is asserted	
	NMI	Red LED lit when /NMI is asserted	
LED4	STATUS1	Green LED lit when STATUS1 is 0 (low)	
	STATUS0	Red LED lit when STATUS0 is 0 (low)	

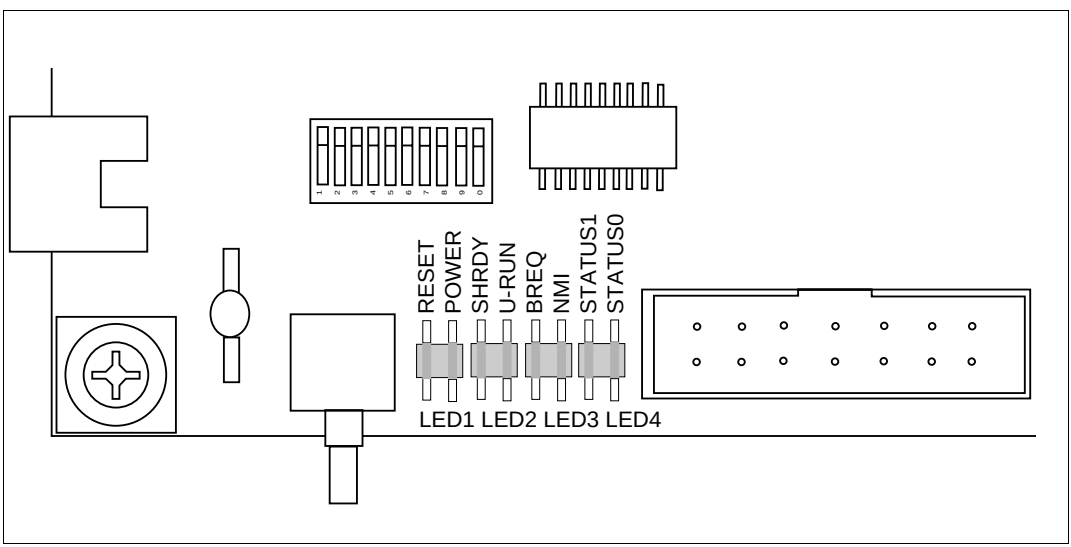


Figure 4.4 LED Location and Indication on the Board

Section 5 Connection Procedures

5.1 Connecting Emulation Memory Board to Emulator and User System

Be sure to switch off the emulator and user system before connecting the emulation memory board, emulator, and user system. Do not supply power to the power pin on the emulation memory board when using the user system.

⚠ WARNING

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

1. **Always switch OFF the emulator product, the emulation memory board, and the user system before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM.**
2. **DO NOT supply power to the emulation memory board from power connector (J1) when the emulation memory board is connected to the user system. When connected to the user system, the emulation memory board receives power from the VDDQ pin of the user interface socket (NQPACK208SD) and operates by the user system power.**

Connecting Emulation Memory Board to Emulator: Connect the emulator to the CN1 connector on the emulation memory board through an E10A emulator user system interface cable.

For details on the connection procedure, refer to the SH7750R E10A Emulator User's Manual.

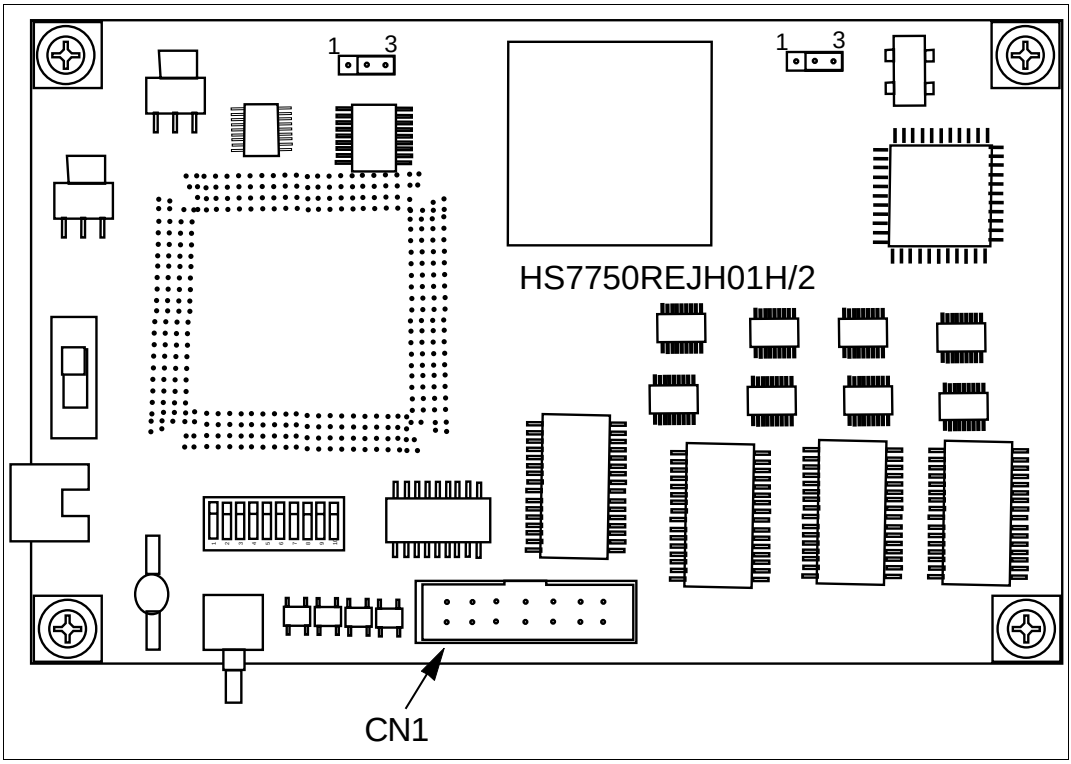


Figure 5.1 Connectors for Emulator

Connecting Emulation Memory Board to User System: Follow the instructions below.

⚠ WARNING

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

1. **Always switch OFF the emulator product, the emulation memory board, and the user system before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM.**
2. **Use the recommended user interface socket on the user system. Otherwise, excessive force will be applied to the emulation memory board and the user system when the emulation memory board is connected to or disconnected from the user system.**

CAUTION

1. **Use NQPACK208SD (manufactured by Tokyo Eletech Corporation) as the QFP208 socket on the user system.**
2. **To mount the MCU directly on the NQPACK208SD socket, a socket cover must be used. Separately purchase HQPACK208SD (manufactured by Tokyo Eletech Corporation).**

1. Confirm that the pins of the YQPACK socket on the emulation memory board are not bent.
2. Align pin 1 of the YQPACK socket on the emulation memory board with pin 1 of the NQPACK socket on the user system, and insert the connector into the socket.

CAUTION

The structures of the YQPACK and NQPACK sockets prevent the connector from being fully inserted in the wrong direction. If the connector cannot be inserted fully, pin 1 on the connector and that on the socket may not be aligned correctly. Forcibly connecting in the wrong direction will apply excessive force to the emulation memory board and the user system. Check the pin 1 locations on the connector and socket, and re-insert the YQPACK socket.

3. After inserting the YQPACK socket on the emulation memory board into the NQPACK socket of the user system, fix the emulation memory board in place with the supplied screws, as shown in figure 5.2.

CAUTION

1. **Use the supplied screwdriver.**
2. **The tightening torque must be 0.054 N•m or less. Stop tightening when the force required to turn the screw becomes significantly greater than that needed when first tightening.**
3. **If a screw is tightened too much, the screw head may break or an IC socket contact error may be caused by a crack in the IC socket solder.**
4. **If the emulator does not operate correctly, cracks might have occurred in the solder. Check conduction with a tester and re-solder the IC socket if necessary.**

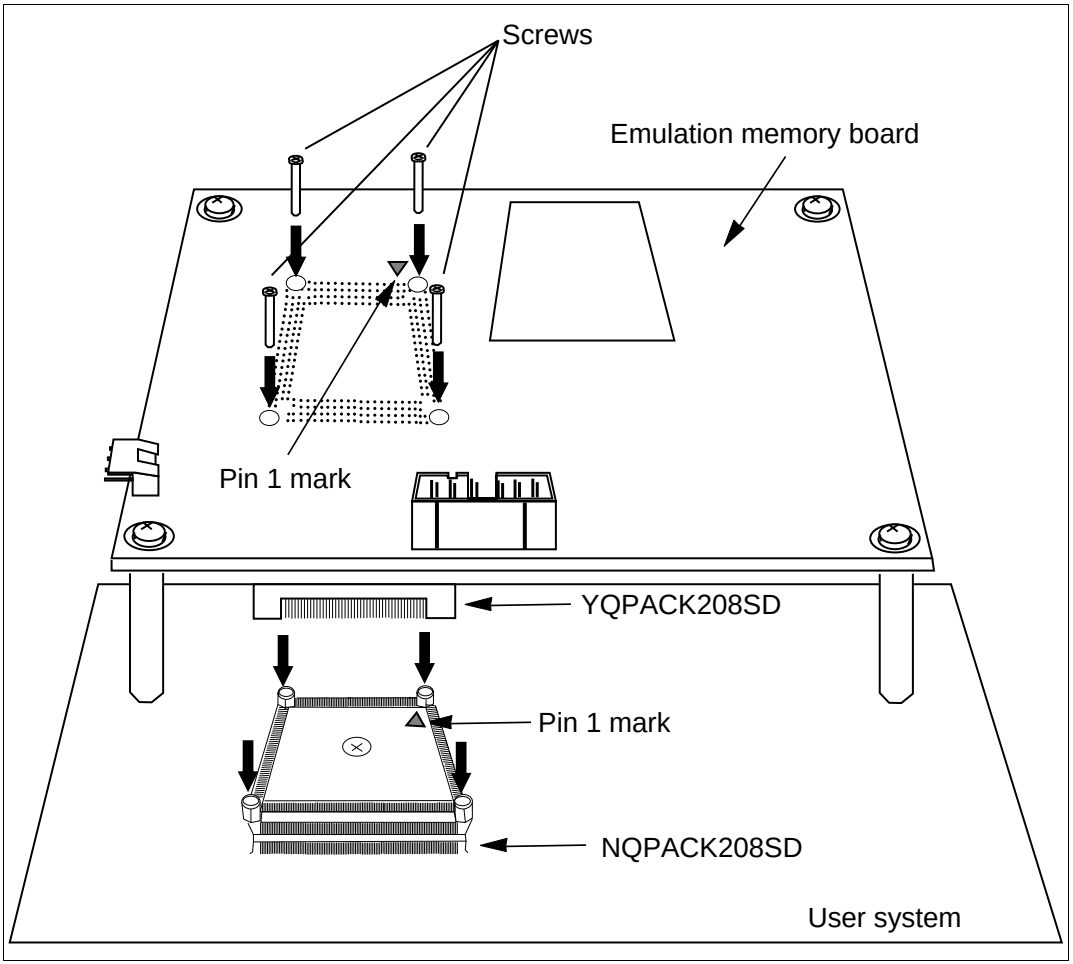


Figure 5.2 Connecting Emulation Memory Board to User System

Power Supply Specifications: When the user system is connected, the emulation memory board operates by the user system power. Supply the user system power according to the specifications and rising timing shown in table 5.1 and figure 5.3.

CAUTION

1. **Check that the SW3 switch is set to the power supply through the user interface, and supply 3.3-V power to the VDDQ pin. Do not supply power to the power connector (J1) on the emulation memory board.**
2. **When power is supplied through the user interface (YQPACK), only 3.3-V power should be supplied from the user system, and the emulation memory board generates 1.5-V power from the 3.3-V power. Therefore, the VDD pin (1.5 V) of the user interface (YQPACK) is not connected to the MCU on the emulation memory board.**

Table 5.1 Power Supply Specifications

Allowable Power Range	Current Consumption
+ 3.3 VDC ± 5%	2.15 A (max.)

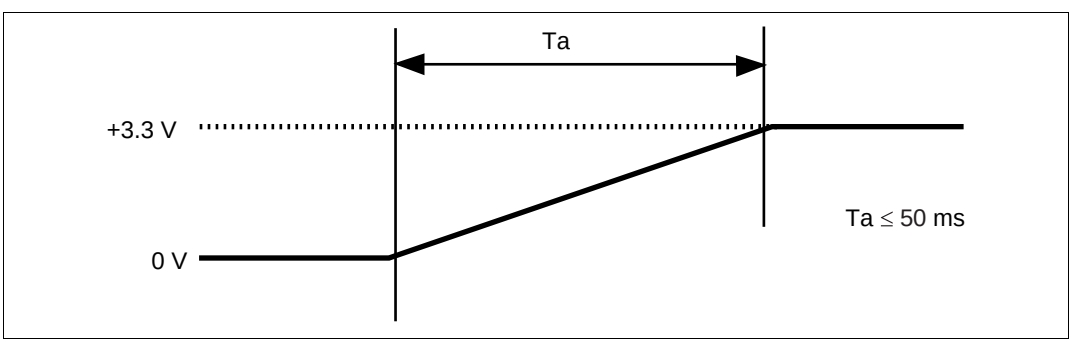


Figure 5.3 Characteristics of DC Rising Timing

5.2 Operating Emulation Memory Board Without Connecting User System

Be sure to switch off the emulator and emulation memory board before connecting them together and before connecting the power cables to the emulation memory board.

⚠ WARNING

Always switch OFF the emulator product and the emulation memory board before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or POWER CABLES. Failure to do so will result in a FIRE HAZARD and will damage the emulator product and the emulation memory board or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

Connecting to the Emulator: Connect the emulation memory board to the emulator by using the same procedure as that described in section 5.1, Connecting Emulation Memory Board to Emulator and User System.

Connecting the Power Cables: After making sure the alignment is correct, connect the provided power cables to the power connector (J1) on the emulation memory board to supply power, as shown in figure 5.4. (The power cable and connector structures will prevent the power cables from being connected in the wrong direction.)

Note that the red cables are for 5-V power and the black ones are for GND; connect them to the DC power source correctly. See figure 5.4.

⚠ WARNING

Be sure to connect the power cables to the DC power source correctly, that is, the red cables to the 5-V power and the black ones to GND. Failure to do so will result in a FIRE HAZARD and will damage the emulator product and the emulation memory board or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

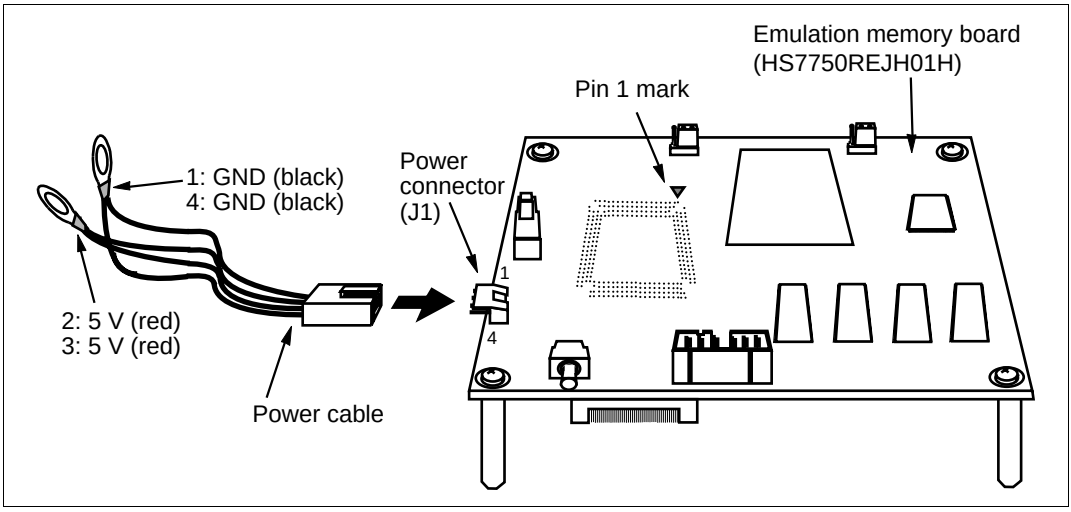


Figure 5.4 Connecting Power Cables to Power Connector

Power Supply Specifications: Table 5.2 shows the power supply specifications, and figure 5.5 shows the rising timing of the power.

Table 5.2 Power Supply Specifications

Allowable Power Range	Current Consumption
+ 5.0 VDC ± 5%	2.15 A (max.)

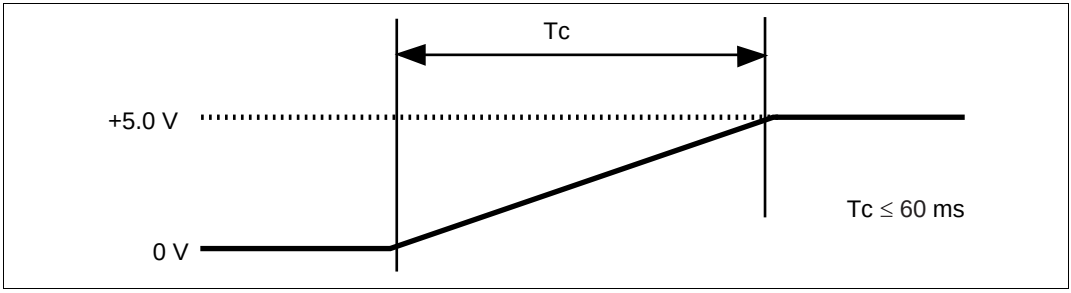


Figure 5.5 Characteristics of DC Rising Timing

5.3 Disconnecting Emulation Memory Board from User System

Be sure to switch off the emulator and user system before disconnection.

⚠ WARNING

Always switch OFF the emulator product, the emulation memory board, and the user system before disconnecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM. Failure to do so will result in a FIRE HAZARD and will damage the emulator product, the emulation memory board, and the user system or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

Disconnecting Emulation Memory Board from User System: Follow the instructions below.

1. Remove the screws that connect the YQPACK and NQPACK sockets.
2. After removing all screws, remove the emulation memory board from the user system, taking care not to bend any of the pins.

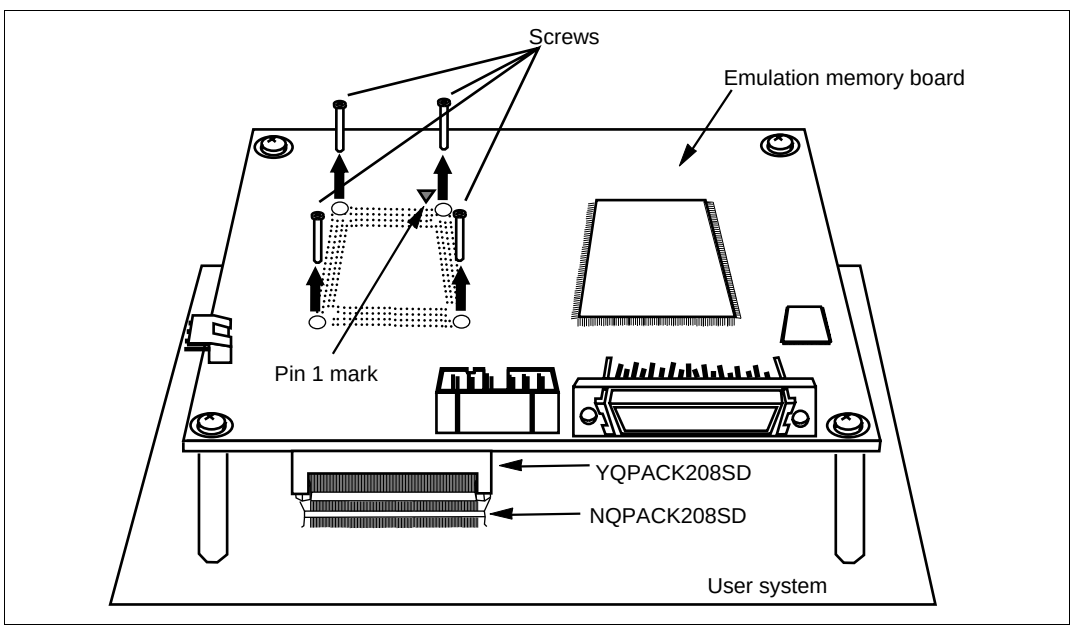


Figure 5.6 Disconnecting Emulation Memory Board

5.4 Recommended Dimensions for User System Mount Pad

Figure 5.7 shows the recommended dimensions for the mount pad (footprint) for the user system with an IC socket for a QFP208 package (NQPACK208SD: manufactured by Tokyo Eletech Corporation). Note that the dimensions in figure 5.7 are somewhat different from those of the actual chip's mount pad.

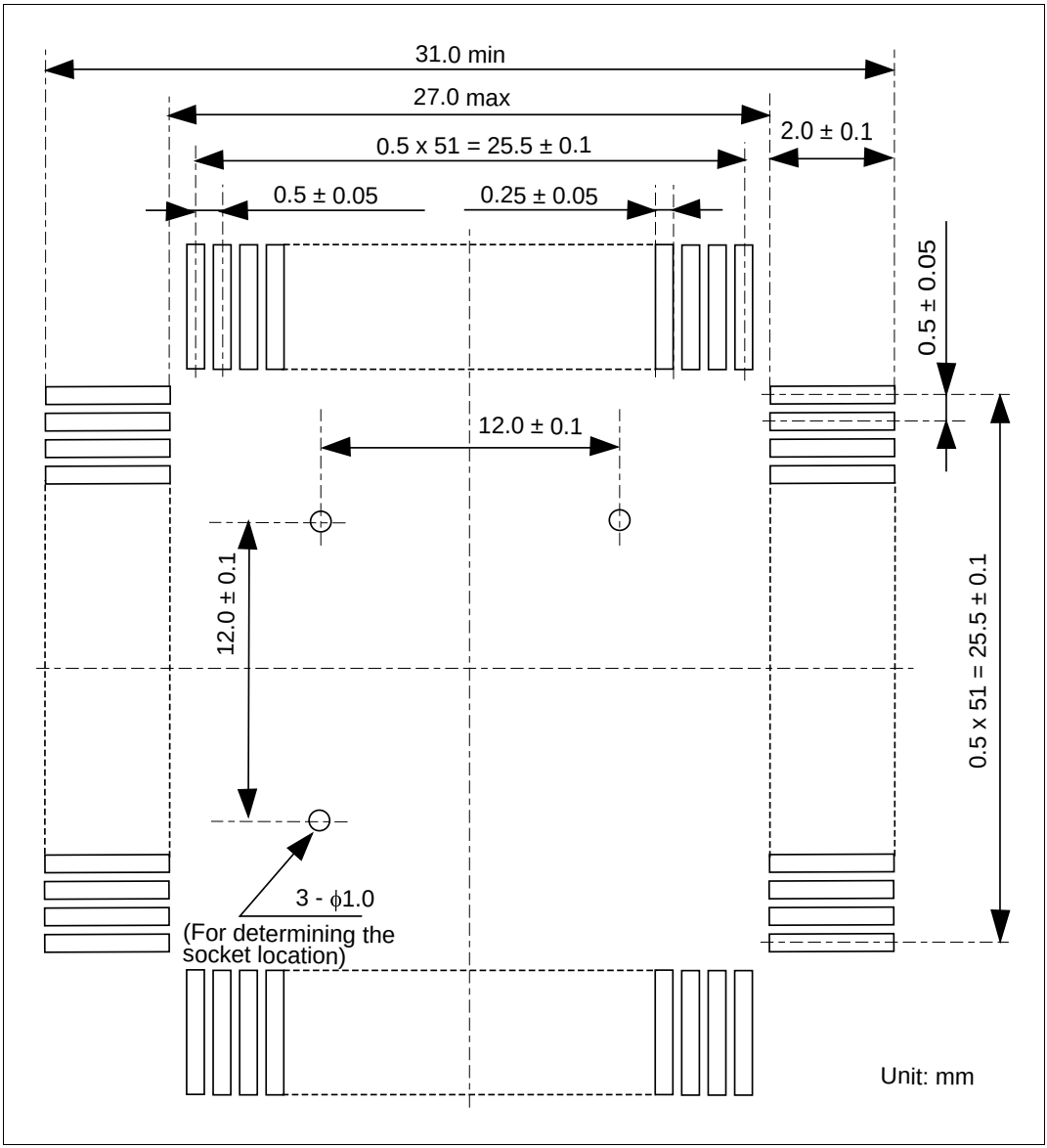


Figure 5.7 Recommended Dimensions for Mount Pad

Section 6 Limitations

6.1 Limitations on Connecting the User System

To use the emulation memory board together with the user system, do not mount any components in the mount-prohibited areas (figure 6.1) of the user system. If any component is mounted on any of these areas, remove the corresponding spacer from the emulation memory board. In this case, take special care not to give any stress to the user interface section (NQPACK).

The height of the mounted components must be 8.0 mm or shorter in the height-limited area (figure 6.1) of the user system. If any component in this area is higher than 8.0 mm, the emulation memory board cannot be connected to the user system.

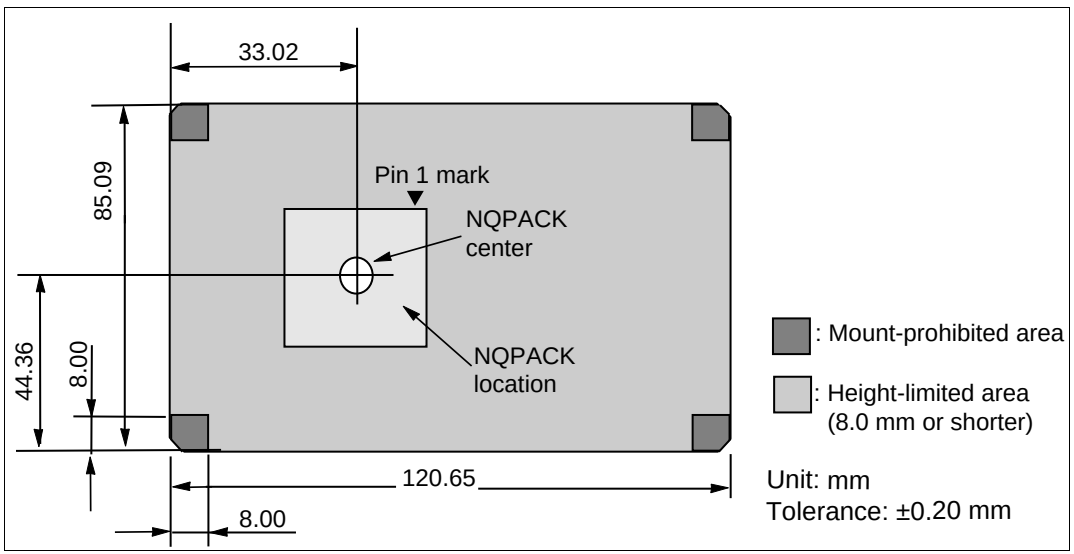


Figure 6.1 Mount-Prohibited and Height-Limited Areas of User System

Section 7 User Interface

7.1 Pin Assignment and Handling of User Interface Signals

The emulation memory board has a socket (YQPACK) for user interface. Table 7.1 shows the pin assignment of the user interface and signal handling on the emulation memory board.

Table 7.1 Pin Assignment and Handling of User Interface

No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
1	RDY	Pull-up	47 kΩ	31	VDDQ	3.3 V	
2	RESET	Pull-up	47 kΩ	32	VSSQ	GND	
3	CS0	Pull-up	47 kΩ	33	D15		
4	CS1			34	D0		
5	CS4			35	D14		
6	CS5			36	D1		
7	CS6			37	D13		
8	BS			38	D2		
9	VDDQ	3.3 V		39	VDD	NC	
10	VSSQ	GND		40	VSS	GND	
11	D47			41	D12		
12	D32			42	D3		
13	VDD	NC		43	VDDQ	3.3 V	
14	VSS	GND		44	VSSQ	GND	
15	D46			45	D11		
16	D33			46	D4		
17	D45			47	D10		
18	D34			48	D5		
19	D44			49	D9		
20	D35			50	D6		
21	VDDQ	3.3 V		51	BACK/BSREQ		
22	VSSQ	GND		52	BREQ/BSACK	Pull-up	47 kΩ
23	D43			53	D8		
24	D36			54	D7		
25	D42			55	CKE		
26	D37			56	VDDQ	3.3 V	
27	D41			57	VSSQ	GND	
28	D38			58	WE5/CAS5/DQM5		
29	D40			59	WE4/CAS4/DQM4		
30	D39			60	WE1/CAS1/DQM1		

Table 7.1 Pin Assignment and Handling of User Interface (cont)

No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
61	WE0/CAS0/DQM0			96	WE2/CAS2/DQM2/ICIORD		
62	A17			97	WE3/CAS3/DQM3/ICIOWR		
63	A16			98	WE6/CAS6/DQM6		
64	A15			99	VDDQ	3.3 V	
65	VDD	NC		100	VSSQ	GND	
66	VSS	GND		101	WE7/CAS7/DQM7/REG		
67	A14			102	D23		
68	A13			103	D24		
69	VDDQ	3.3 V		104	D22		
70	VSSQ	GND		105	RXD	Pull-up	47 kΩ
71	A12			106	DREQ0	Pull-up	47 kΩ
72	A11			107	DREQ1	Pull-up	47 kΩ
73	A10			108	D25		
74	A9			109	D21		
75	A8			110	D26		
76	A7			111	D20		
77	CKIO			112	D27		
78	VDDQ	3.3 V		113	VDDQ	3.3 V	
79	VSSQ	GND		114	VSSQ	GND	
80	A6			115	D19		
81	A5			116	D28		
82	A4			117	VDD	NC	
83	A3			118	VSS	GND	
84	A2			119	D18		
85	DRAK1			120	D29		
86	DRAK0			121	D17		
87	VDDQ	3.3 V		122	D30		
88	VSSQ	GND		123	D16		
89	CS3			124	D31		
90	CS2			125	VDDQ	3.3 V	
91	VDD	NC		126	VSSQ	GND	
92	VSS	GND		127	D55		
93	RAS			128	D56		
94	RD/CASS/FRAME			129	D54		
95	RD/WR			130	D57		

Table 7.1 Pin Assignment and Handling of User Interface (cont)

No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
131	D53			170	VSS	GND	
132	D58			171	A18		
133	D52			172	A19		
134	D59			173	A20		
135	VDDQ	3.3 V		174	A21		
136	VSSQ	GND		175	A22		
137	D51			176	A23		
138	D60			177	VDDQ	3.3 V	
139	D50			178	VSSQ	GND	
140	D61			179	A24		
141	D49			180	A25		
142	D62			181	MD3/CE2A	Pull-up	47 kΩ
143	VDD	NC		182	MD4/CE2B	Pull-up	47 kΩ
144	VSS	GND		183	MD5/RAS2	Pull-up	47 kΩ
145	D48			184	DACK0		
146	D63			185	DACK1		
147	VDDQ	3.3 V		186	A0		
148	VSSQ	GND		187	VDDQ	3.3 V	
149	MD0/SCK	Pull-up	47 kΩ	188	VSSQ	GND	
150	MD1/TXD2	Pull-up	47 kΩ	189	A1		
151	MD2/RXD2	Pull-up	47 kΩ	190	STATUS0		
152	IRL0	Pull-up	47 kΩ	191	STATUS1		
153	IRL1	Pull-up	47 kΩ	192	MD6/IOIS16	Pull-up	47 kΩ
154	IRL2	Pull-up	47 kΩ	193	ASEBRK/BRKACK	NC	
155	IRL3	Pull-up	47 kΩ	194	TDO	NC	
156	NMI	Pull-up	47 kΩ	195	VDD	NC	
157	XTAL2	NC		196	VSS	GND	
158	EXTAL2	NC		197	TMS	NC	
159	VSS-RTC	GND		198	TCK	NC	
160	VDD-RTC	3.3 V		199	TDI	NC	
161	CA	Pull-up	47 kΩ	200	TRST	NC	
162	VSS	GND		201	VDD-PLL2	3.3 V	
163	VDDQ	3.3 V		202	VSS-PLL2	U-GND	
164	CST2	Pull-up	47 kΩ	203	VDD-PLL1	3.3 V	
165	TCLK	Pull-up	47 kΩ	204	VSS-PLL1	GND	
166	MD8/RTS2	Pull-up	47 kΩ	205	VDD-CPG	3.3 V	
167	MD7/TXD	Pull-up	47 kΩ	206	VSS-CPG	GND	
168	SCK2/MRESET	Pull-up	47 kΩ	207	XTAL	NC	
169	VDD	NC		208	EXTAL	Pull-up	47 kΩ

CAUTION

When power is supplied through the user system interface (YQPACK), only 3.3-V power should be supplied from the user system, and the emulation memory board generates 1.5-V power from the 3.3-V power. Therefore, the VDD pin (1.5 V) of the user interface (YQPACK) is not connected to the MCU on the emulation memory board.

Handling:

Pull-up: The pin is pulled up to 3.3 V through a 47-kΩ resistor on the board.

3.3 V: 3.3 V is supplied from the user system (when sliding SW3 to USER).

U-GND: The pin is connected to user system GND (to check whether or not the user system is connected).

GND: The pin is connected to GND on the board.

NC: The MCU pin is not connected to the user interface.

Blank: The MCU pin is directly connected to the user interface.

7.2 Signal Line Handling on the Emulation Memory Board and User System

The emulation memory board is connected to the user system through the user interfaces (YQPACK and NQPACK). Figure 7.1 shows the signal line handling on the emulation memory board and the user system.

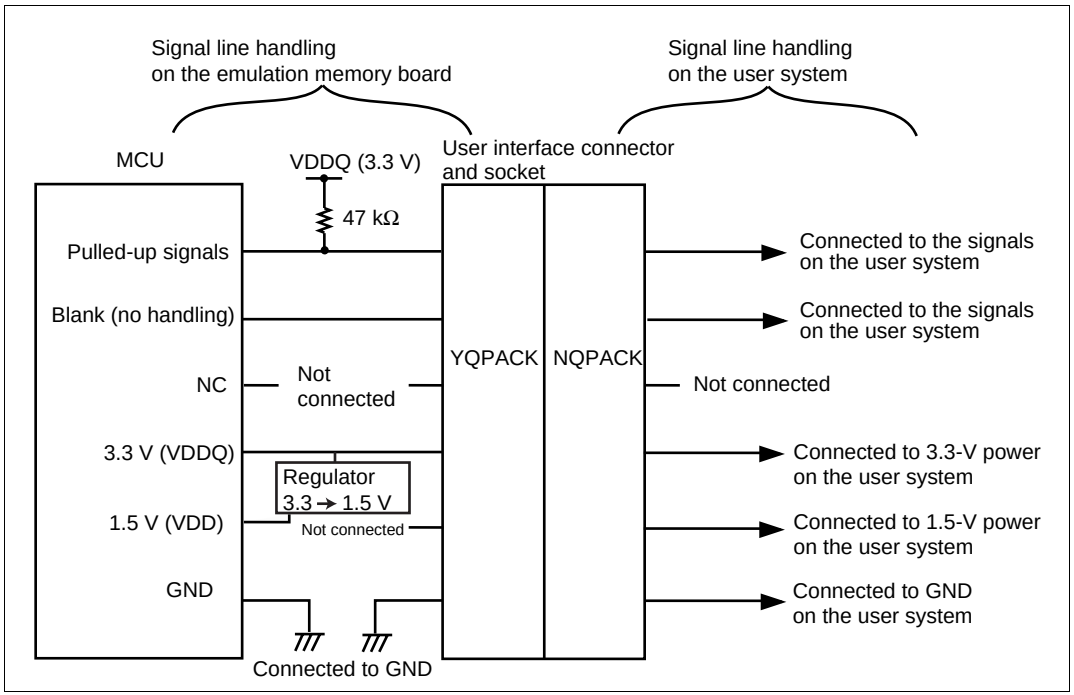


Figure 7.1 Signal Line Handling on the Emulation Memory Board and User System

Section 8 Emulation Memory Board Block Diagram

The emulation memory board has an MCU, a user interface, emulator connectors, and memory. Figure 8.1 shows the block diagram of the emulation memory board.

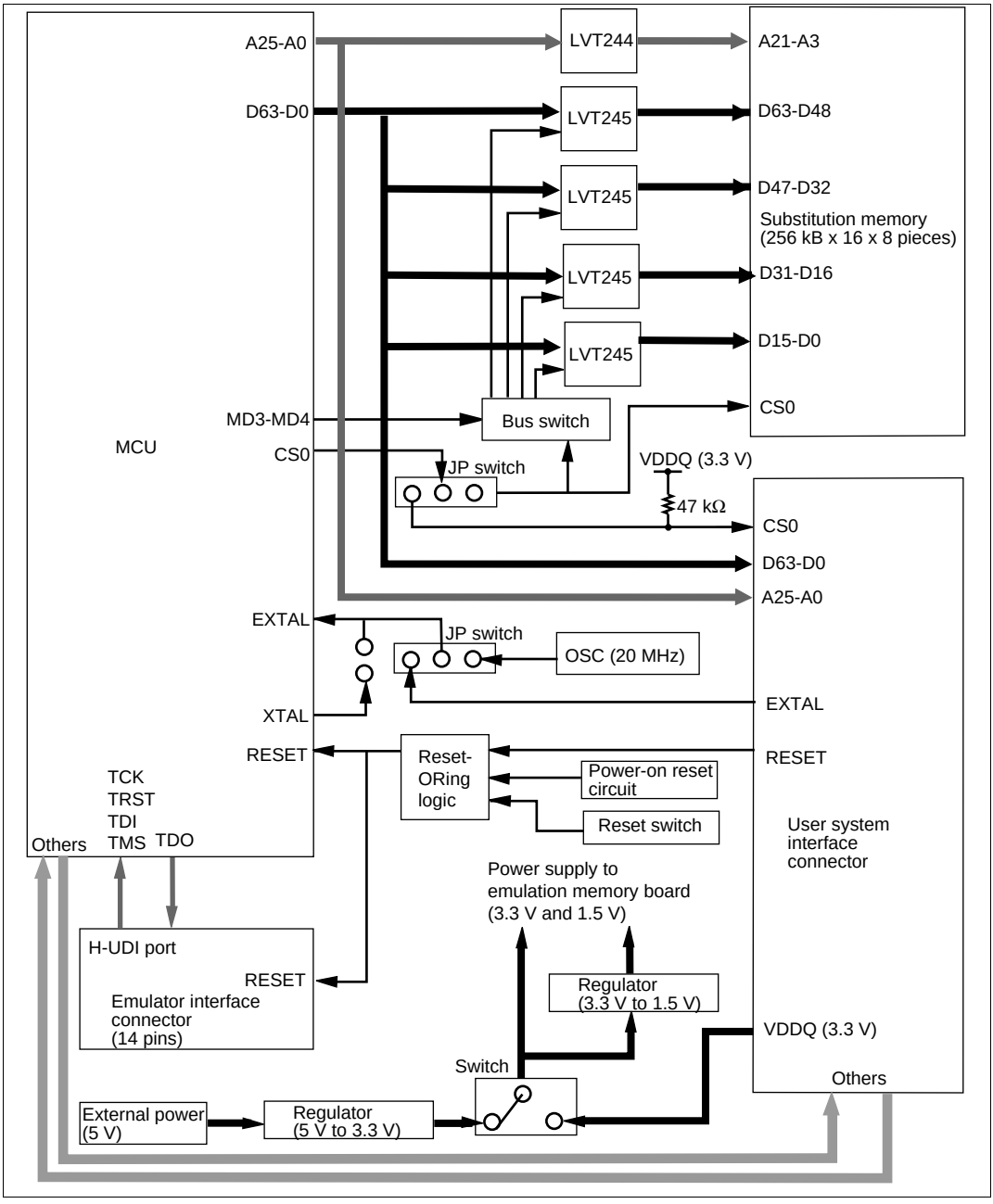


Figure 8.1 Emulation Memory Board Block Diagram

Section 9 Using the Emulator in a Case

Package the emulator and the emulation memory board in a case as shown below. The recommended material of the case to prevent EMI noise is iron plated with nickel or resin plated with nickel inside. The case must have enough size to hold the emulation memory board and the user system.

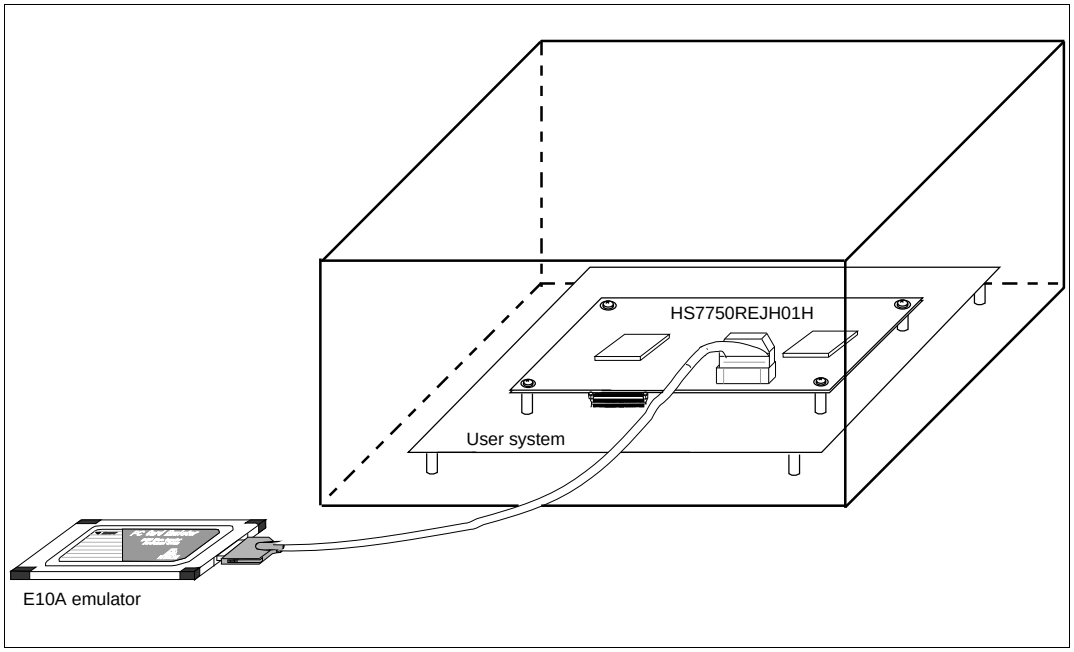


Figure 9.1 Configuration for Countermeasure against EMI Noise

Note: EMI stands for Electrical Magnetic Interference.