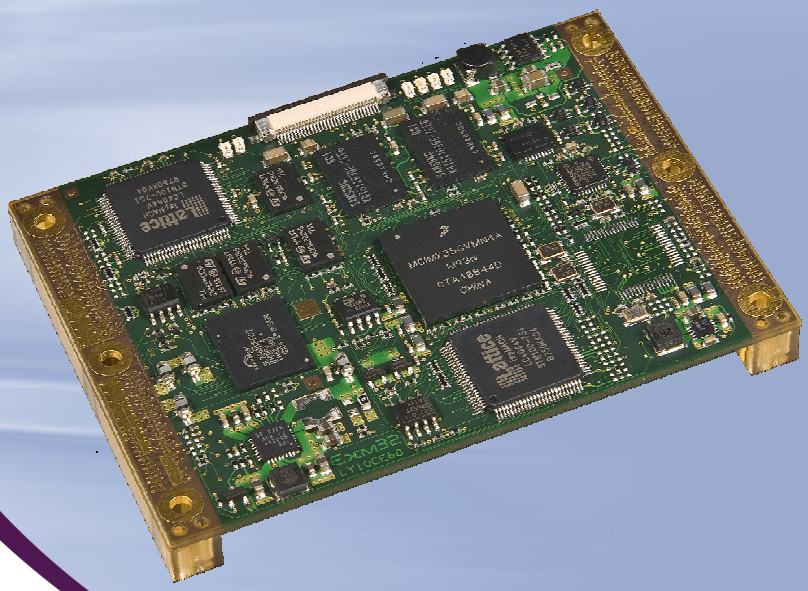
User's Manual



MSC EXM32-IMX35 CPU-Module

Rev. 1.1

Document change history

Date	Version	Document change description
2009-08-28	0.1	initial release Hardware Rev 2.0
2010-06-2	1.0	Hardware Rev 3.0 & Hardware Rev 4.0
2010-12-17	1.1	Various Updates & Corrections

Preface

Copyright Notice

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided “as is” and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Trademarks

All used product names, logos or trademarks are property of their respective owners.

Certification

MSC Vertriebs GmbH is certified according to DIN EN ISO 9001:2000 standards.

Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

Product Support

MSC engineers and technicians are committed to provide support to our customers whenever needed.
Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at www.msc-ge.com/support-boards for the latest documentation, drivers and software downloads.
If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com
Phone: +49 8165 906-200

Content

1 Blockdiagram

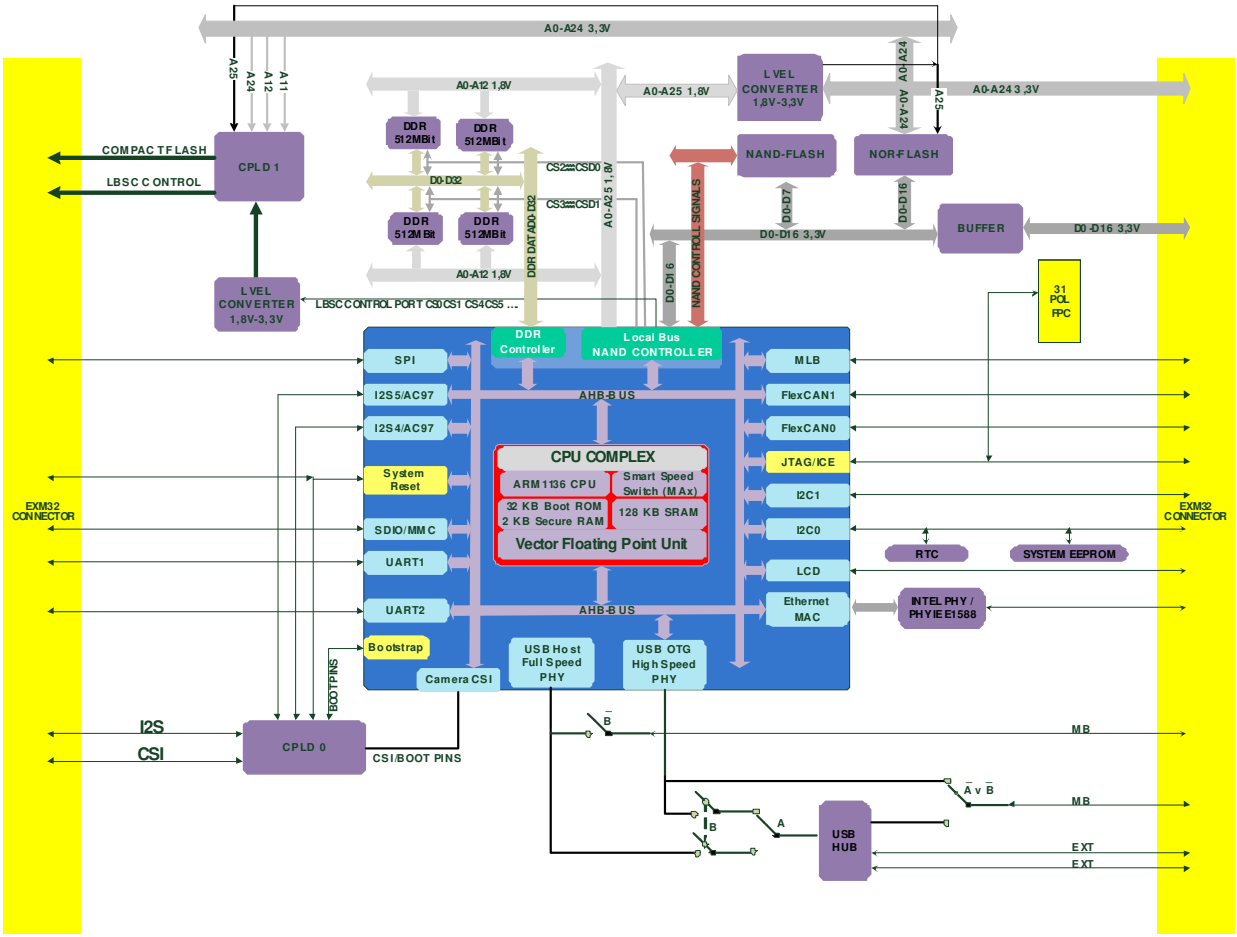


Figure 1 EXM-32 IMX35 CPU Module

The highly integrated IMX35 microprocessors possesses various interfaces except of CompactFlash. The Compact-Flash interface is implemented in a CPLD which adapts the CPU-timing to the Compact-Flash specification.
The DDR Memory Controller and the Local Bus share the lower address lines A0…A12 except of A10. The access decoding for the Local Bus is also implemented in the CPLD. The entire Local Bus is buffered in order to decouple the module from the baseboard and to facilitate baseboard designs, so further buffering, level-converting etc. is not needed on Motherboards.

1.1 Functional Blocks

The EXM32 IMX35 ARM 11 CPU Module includes the following functional blocks:

CPU

- IMX35 ARM11 CPU 532 MHz main clock and AHB Bus with maximum 133MHz clock, with Vector Floating Point Unit, 32 KB Boot ROM, 128 SRAM and 2 KB Secure Ram.

Peripherals

- Camera Interface (8 Bit)
- PCMCIA/CF Interface
- Ethernet 10/100Mbit/s Mac with external IEEE1588 PHY or standard PHY Cortina LXT971A Single Port
- Flex Can (2x) Controller
- I2C (2x)
- SPI
- MLB (3-wire Media Local Bus)
- AC97/I²S Sound Interface
- RTC
- SD/MMC (Secure Digital Memory Card /Multimedia Card)
- LCD
- USB (High Speed USB OTG and Full Speed USB Host)

Memory (onboard)

- Up to 256 Mbyte DDR2 Memory (32bit Data bus width @133MHz)
- Up to 128 Mbyte linear Flash (NOR Flash with 16 Bit bus width)
- Optional NAND Flash Memory up to 1GByte (8 bit Bus)

Local Bus

- 16-Bit CPU bus for SRAM or VLIO-type peripherals with Data acknowledge logic available on module connector (Buffer is 3.3V tolerant),

Connectors

- Two EXM32 Connectors carry all interfaces, the system CPU bus and the power supply.
- A Debug connector allows the connection of a JTAG based debug tool.

1.2 EXM32-i.MX35 available Signals

X1 - A (MB-CPU)			
Pin	Signal	Pin	Signal
1	IDE_IORDY	2	CF_SCKSEL
3	IDE_CS0#	4	CF_CE1#
5	IDE_CS1#	6	CF_CE2#
7	CF0_PWEN	8	CF_IORD# / IDE_DIOR#
9	CF1_PWEN	10	CF_IOWR# / IDE_DIOW#
11	CF_INPACK#	12	CF_POE#
13	CF0_RESET	14	CF_PWE#
15	CF1_RESET	16	CF_WAIT#
17	SPI_SS0#	18	CF_IOIS16#
19	SPI_SS1#	20	CF_PREG#
21	n.c.	22	CF0_RDY_IRQ#
23	SPI_SCK	24	CF1_RDY_IRQ#
25	SPI_MOSI	26	CF0_CD#
27	SPI_MISO	28	CF1_CD#
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND

X1 - A (CPU-EXT)			
Pin	Signal	Pin	Signal
1	IDE_IORDY	2	CF_SCKSEL
3	IDE_CS0#	4	CF_CE1#
5	IDE_CS1#	6	CF_CE2#
7	CF0_PWEN	8	CF_IORD# / IDE_DIOR#
9	CF1_PWEN	10	CF_IOWR# / IDE_DIOW#
11	CF_INPACK#	12	CF_POE#
13	CF0_RESET	14	CF_PWE#
15	CF1_RESET	16	CF_WAIT#
17	SPI_SS0#	18	CF_IOIS16#
19	SPI_SS1#	20	CF_PREG#
21	n.c.	22	CF0_RDY_IRQ#
23	SPI_SCK	24	CF1_RDY_IRQ#
25	SPI_MOSI	26	CF0_CD#
27	SPI_MISO	28	CF1_CD#
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND

X1 - B (MB-CPU)			
Pin	Signal	Pin	Signal
1	D00	2	D01
3	D02	4	D03
5	D04	6	D05
7	D06	8	D07
9	D08	10	D09
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	D16	18	D17
19	D18	20	D19
21	D20	22	D21
23	D22	24	D23
25	D24	26	D25
27	D26	28	D27
29	D28	30	D29
31	D30	32	D31
33	BE0#	34	BE1#
35	BE2#	36	BE3#
37	IRQ_EXT1#	38	n.c.
39	IRQ_EXT0#	40	CSA#
41	IRQ_MB2#	42	CSB#
43	IRQ_MB1#	44	BS#
45	IRQ_MB0#	46	OE#
47	GND	48	WE#
49	BUSCLK	50	R/W#
51	GND	52	RDY

X1 - B (CPU-EXT)			
Pin	Signal	Pin	Signal
1	D00	2	D01
3	D02	4	D03
5	D04	6	D05
7	D06	8	D07
9	D08	10	D09
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	D16	18	D17
19	D18	20	D19
21	D20	22	D21
23	D22	24	D23
25	D24	26	D25
27	D26	28	D27
29	D28	30	D29
31	D30	32	D31
33	BE0#	34	BE1#
35	BE2#	36	BE3#
37	IRQ_EXT1#	38	n.c.
39	IRQ_EXT0#	40	CSA#
41	IRQ_MB2#	42	CSB#
43	IRQ_MB1#	44	BS#
45	IRQ_MB0#	46	OE#
47	GND	48	WE#
49	BUSCLK	50	R/W#
51	GND	52	RDY

X1 - C (MB-CPU)			
Pin	Signal	Pin	Signal
1	VCC3V3	2	VCC3V3
3	VCC3V3	4	VCC3V3
5	VCC3V3	6	VCC3V3
7	VCC3V3	8	VCC3V3
9	VCC3V3	10	VCC3V3
11	VCC3V3	12	VCC3V3
13	VCC3V3	14	VCC3V3STB
15	VCC3V3	16	VCC3V3STB
17	VCC3V3	18	VCC3V3STB
19	VCC3V3	20	VCC3V3STB
21	VCC3V3	22	VCC3V3STB
23	VCC3V3	24	VCC3V3STB
25	VBAT	26	VCC5V0
27	VBAT_RET	28	VCC5V0
29	PWROFF/SUSPEND	30	VCC5V0
31	SLEEP#	32	VCC5V0
33	WAKEUP	34	VCC5V0
35	PWRFLT#	36	VCC5V0
37	MASTER_RST#	38	ETH_ACTLED#
39	PERIPH_RST#	40	ETH_LNKLED#
41	AUDIO_RST#	42	AC97_SDIN1
43	AC97_SYNC/ I2S0_LRCLK	44	AC97_SDIN0 / I2S0_SCLK
45	I2S1_LRCLK	46	I2S1_SCLK
47	GND	48	AC97_SDOUT / I2S0_SDIO
49	AC97_BCLK / I2S_MCLK	50	I2S1_SDIO
51	GND	52	PWRON#

X1 - C (CPU-EXT)			
Pin	Signal	Pin	Signal
1	VCC3V3	2	VCC3V3
3	VCC3V3	4	VCC3V3
5	VCC3V3	6	VCC3V3
7	VCC3V3	8	VCC3V3
9	VCC3V3	10	VCC3V3
11	VCC3V3	12	VCC3V3
13	VCC3V3	14	VCC3V3STB
15	VCC3V3	16	VCC3V3STB
17	VCC3V3	18	VCC3V3STB
19	VCC3V3	20	VCC3V3STB
21	VCC3V3	22	VCC3V3STB
23	VCC3V3	24	VCC3V3STB
25	VBAT	26	VCC5V0
27	n.c.	28	VCC5V0
29	PWROFF/SUSPEND	30	VCC5V0
31	SLEEP#	32	VCC5V0
33	WAKEUP	34	VCC5V0
35	PWRFLT#	36	VCC5V0
37	MASTER_RST#	38	n.c.
39	PERIPH_RST#	40	n.c.
41	AUDIO_RST#	42	AC97_SDIN1
43	AC97_SYNC/ I2S0_LRCLK	44	AC97_SDIN0 / I2S0_SCLK
45	I2S1_LRCLK	46	I2S1_SCLK
47	GND	48	AC97_SDOUT / I2S0_SDIO
49	AC97_BCLK / I2S_MCLK	50	I2S1_SDIO
51	GND	52	PWRON#

X1 - D (MB-CPU)			
Pin	Signal	Pin	Signal
1	A00	2	A01
3	A02	4	A03
5	A04	6	A05
7	A06	8	A07
9	A08	10	A09
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	A16	18	A17
19	A18	20	A19
21	A20	22	A21
23	A22	24	A23
25	A24	26	A25
27	DREQ0#	28	DREQ1#
29	DRAK0#	30	DRAK1#
31	DACK0#	32	DACK1#
33	n.c.	34	PCIE_PRSNT0#
35	PCIE_PERST#	36	PCIE_REFCLK0+
37	n.c.	38	PCIE_REFCLK0-
39	GND	40	GND
41	GND	42	PCIE_PET0+
43	GND	44	PCIE_PET0-
45	GND	46	GND
47	GND	48	PCIE_PER0+
49	GND	50	PCIE_PER0-
51	GND	52	GND

X1 - D (CPU-EXT)			
Pin	Signal	Pin	Signal
1	A00	2	A01
3	A02	4	A03
5	A04	6	A05
7	A06	8	A07
9	A08	10	A09
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	A16	18	A17
19	A18	20	A19
21	A20	22	A21
23	A22	24	A23
25	A24	26	A25
27	DREQ0#	28	DREQ1#
29	DRAK0#	30	DRAK1#
31	DACK0#	32	DACK1#
33	n.c.	34	PCIE_PRSNT1#
35	PCIE_PERST#	36	PCIE_REFCLK1+
37	n.c.	38	PCIE_REFCLK1-
39	GND	40	GND
41	GND	42	PCIE_PET1+
43	GND	44	PCIE_PET1-
45	GND	46	GND
47	GND	48	PCIE_PER1+
49	GND	50	PCIE_PER1-
51	GND	52	GND

X2 - A (MB-CPU)			
Pin	Signal	Pin	Signal
1	GND	2	HDMI_CEC
3	HDMI_TMDS_CLK+	4	MLB_MCLK
5	HDMI_TMDS_CLK-	6	MLB_MSI / n.u.
7	GND	8	MLB_MSO / MLB_MSIG
9	HDMI_TMDS_D2+	10	MLB_MDI / n.u.
11	HDMI_TMDS_D2-	12	MLB_MDO / MLB_MDAT
13	GND	14	JTAG_TDO
15	HDMI_TMDS_D1+	16	JTAG_TDI
17	HDMI_TMDS_D1-	18	JTAG_TCK
19	GND	20	JTAG_TMS
21	HDMI_TMDS_D0+	22	JTAG_TRST#
23	HDMI_TMDS_D0-	24	CAN0_EN
25	GND	26	CAN1_RX
27	SATA_TX+	28	CAN0_ERR#
29	SATA_TX-	30	CAN1_TX
31	GND	32	CAN0_STB#
33	SATA_RX+	34	CAN1_EN
35	SATA_RX-	36	CAN0_RX
37	GND	38	CAN1_ERR#
39	GND	40	CAN0_TX
41	USB_OTG_D+	42	CAN1_STB#
43	USB_OTG_D-	44	USB_OTG_ID
45	GND	46	USB_OTG_VBUS
47	USB_MB_D+	48	USB_OTG_PWEN
49	USB_MB_D-	50	USB_MB_PWEN
51	GND	52	USB_OC#

X2 - A (CPU-EXT)			
Pin	Signal	Pin	Signal
1	GND	2	n.c.
3	n.c.	4	MLB_MCLK
5	n.c.	6	MLB_MSI / n.u.
7	GND	8	MLB_MSO / MLB_MSIG
9	n.c.	10	MLB_MDI / n.u.
11	n.c.	12	MLB_MDO / MLB_MDAT
13	GND	14	JTAG_TDO
15	n.c.	16	JTAG_TDI
17	n.c.	18	JTAG_TCK
19	GND	20	JTAG_TMS
21	n.c.	22	JTAG_TRST#
23	n.c.	24	n.c.
25	GND	26	n.c.
27	n.c.	28	n.c.
29	n.c.	30	n.c.
31	GND	32	n.c.
33	n.c.	34	n.c.
35	n.c.	36	n.c.
37	GND	38	n.c.
39	GND	40	n.c.
41	USB0_EXT_D+	42	n.c.
43	USB0_EXT_D-	44	n.c.
45	GND	46	n.c.
47	USB1_EXT_D+	48	n.c.
49	USB1_EXT_D-	50	n.c.
51	GND	52	n.c.

X2 - B (MB-CPU)			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	DA0_SPDIF	4	DA1_SPDIF
5	GND	6	GND
7	DA0_MCLK	8	DA1_MCLK
9	GND	10	GND
11	DA0_SCLK	12	DA1_SCLK
13	DA0_LRCLK	14	DA1_LRCLK
15	DA0_SDIO0	16	DA1_SDIO0
17	DA0_SDIO1	18	DA1_SDIO1
19	n.c.	20	n.c.
21	DA_MUTE	22	BSCAN_EN#
23	GND	24	GND
25	DV_CLK	26	SDIO1_CLK
27	GND	28	GND
29	DV_AV#	30	SDIO1_WP
31	DV_HSYNC / DV_SYNC	32	SDIO1_CD#
33	DV_VSYNC / DV_DVALID	34	SDIO1_CMD
35	GND	36	GND
37	DV_D0	38	SDIO1_DAT0
39	DV_D1	40	SDIO1_DAT1 / IRQ#
41	DV_D2	42	SDIO1_DAT2 / RW
43	DV_D3	44	SDIO1_DAT3
45	DV_D4	46	SDIO1_DAT4
47	DV_D5	48	SDIO1_DAT5
49	DV_D6	50	SDIO1_DAT6
51	DV_D7	52	SDIO1_DAT7

X2 - B (CPU-EXT)			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	DA0_SPDIF	4	DA1_SPDIF
5	GND	6	GND
7	DA0_MCLK	8	DA1_MCLK
9	GND	10	GND
11	DA0_SCLK	12	DA1_SCLK
13	DA0_LRCLK	14	DA1_LRCLK
15	DA0_SDIO0	16	DA1_SDIO0
17	DA0_SDIO1	18	DA1_SDIO1
19	n.c.	20	n.c.
21	DA_MUTE	22	BSCAN_EN#
23	GND	24	GND
25	DV_CLK	26	SDIO1_CLK
27	GND	28	GND
29	DV_AV#	30	SDIO1_WP
31	DV_HSYNC / DV_SYNC	32	SDIO1_CD#
33	DV_VSYNC / DV_DVALID	34	SDIO1_CMD
35	GND	36	GND
37	DV_D0	38	SDIO1_DAT0
39	DV_D1	40	SDIO1_DAT1 / IRQ#
41	DV_D2	42	SDIO1_DAT2 / RW
43	DV_D3	44	SDIO1_DAT3
45	DV_D4	46	SDIO1_DAT4
47	DV_D5	48	SDIO1_DAT5
49	DV_D6	50	SDIO1_DAT6
51	DV_D7	52	SDIO1_DAT7

X2 - C (MB-CPU)			
Pin	Signal	Pin	Signal
1	LCD_D00 (B0)	2	I2C0_SDA
3	LCD_D01 (B1)	4	I2C0_SCL
5	LCD_D02 (B2)	6	I2C1_SDA
7	LCD_D03 (B3)	8	I2C1_SCL
9	LCD_D04 (B4)	10	ETH_CENTER
11	LCD_D05 (B5)	12	ETH_TXD1+
13	LCD_D06 (G0)	14	ETH_TXD1-
15	LCD_D07 (G1)	16	GND
17	LCD_D08 (G2)	18	ETH_TXD0+
19	LCD_D09 (G3)	20	ETH_TXD0-
21	LCD_D10 (G4)	22	GND
23	LCD_D11 (G5)	24	ETH_RXD0+
25	LCD_D12 (R0)	26	ETH_RXD0-
27	LCD_D13 (R1)	28	GND
29	LCD_D14 (R2)	30	ETH_RXD1+
31	LCD_D15 (R3)	32	ETH_RXD1-
33	LCD_D16 (R4)	34	GND
35	LCD_D17 (R5)	36	VGA_R
37	LCD_VDON	38	GND
39	LCD_M_DE	40	VGA_G
41	LCD_VCON	42	GND
43	LCD_HSYNC	44	VGA_B
45	LCD_VSYNC	46	GND
47	LCD_DON	48	VGA_HSYNC
49	LCD_SHFCLK	50	VGA_VSYNC
51	LCD_BLON	52	GND

X2 - C (CPU-EXT)			
Pin	Signal	Pin	Signal
1	LCD_D00 (B0)	2	I2C0_SDA
3	LCD_D01 (B1)	4	I2C0_SCL
5	LCD_D02 (B2)	6	I2C1_SDA
7	LCD_D03 (B3)	8	I2C1_SCL
9	LCD_D04 (B4)	10	n.c.
11	LCD_D05 (B5)	12	n.c.
13	LCD_D06 (G0)	14	n.c.
15	LCD_D07 (G1)	16	GND
17	LCD_D08 (G2)	18	n.c.
19	LCD_D09 (G3)	20	n.c.
21	LCD_D10 (G4)	22	GND
23	LCD_D11 (G5)	24	n.c.
25	LCD_D12 (R0)	26	n.c.
27	LCD_D13 (R1)	28	GND
29	LCD_D14 (R2)	30	n.c.
31	LCD_D15 (R3)	32	n.c.
33	LCD_D16 (R4)	34	GND
35	LCD_D17 (R5)	36	n.c.
37	LCD_VDON	38	GND
39	LCD_M_DE	40	n.c.
41	LCD_VCON	42	GND
43	LCD_HSYNC	44	n.c.
45	LCD_VSYNC	46	GND
47	LCD_DON	48	n.c.
49	LCD_SHFCLK	50	n.c.
51	LCD_BLON	52	GND

X2 - D (MB-CPU)			
Pin	Signal	Pin	Signal
1	Multi Mode Pin	2	Multi Mode Pin
3	Multi Mode Pin	4	Multi Mode Pin
5	Multi Mode Pin	6	Multi Mode Pin
7	Multi Mode Pin	8	Multi Mode Pin
9	Multi Mode Pin	10	Multi Mode Pin
11	Multi Mode Pin	12	Multi Mode Pin
13	Multi Mode Pin	14	Multi Mode Pin
15	Multi Mode Pin	16	Multi Mode Pin
17	Multi Mode Pin	18	SDIO0_WP
19	Multi Mode Pin	20	SDIO0_CLK
21	Multi Mode Pin	22	SDIO0_CD#
23	Multi Mode Pin	24	SDIO0_CMD
25	Multi Mode Pin	26	SDIO0_DAT0
27	Multi Mode Pin	28	SDIO0_DAT1 / IRQ#
29	Multi Mode Pin	30	SDIO0_DAT2 /RW
31	Multi Mode Pin	32	SDIO0_DAT3
33	LCD2_EN	34	MODULE_ID0 (MB)
35	MODULE_DETECT	36	MODULE_ID1 (MB)
37	COM0_TXD	38	FR_TXD
39	COM0_RXD	40	FR_RXD
41	COM0_RTS#	42	FR_TXEN#
43	COM0_CTS#	44	FR_RXEN#
45	COM1_TXD	46	FR_BGE
47	COM1_RXD	48	FR_EN
49	COM1_RTS#	50	FR_STB#
51	COM1_CTS#	52	FR_ERR#

X2 - D (CPU-EXT)			
Pin	Signal	Pin	Signal
1	Multi Mode Pin	2	Multi Mode Pin
3	Multi Mode Pin	4	Multi Mode Pin
5	Multi Mode Pin	6	Multi Mode Pin
7	Multi Mode Pin	8	Multi Mode Pin
9	Multi Mode Pin	10	Multi Mode Pin
11	Multi Mode Pin	12	Multi Mode Pin
13	Multi Mode Pin	14	Multi Mode Pin
15	Multi Mode Pin	16	Multi Mode Pin
17	Multi Mode Pin	18	SDIO0_WP
19	Multi Mode Pin	20	SDIO0_CLK
21	Multi Mode Pin	22	SDIO0_CD#
23	Multi Mode Pin	24	SDIO0_CMD
25	Multi Mode Pin	26	SDIO0_DAT0
27	Multi Mode Pin	28	SDIO0_DAT1 / IRQ#
29	Multi Mode Pin	30	SDIO0_DAT2 /RW
31	Multi Mode Pin	32	SDIO0_DAT3
33	LCD2_EN	34	MODULE_ID0 (EXT)
35	MODULE_DETECT	36	MODULE_ID1 (EXT)
37	COM0_TXD	38	n.c.
39	COM0_RXD	40	n.c.
41	COM0_RTS#	42	n.c.
43	COM0_CTS#	44	n.c.
45	COM1_TXD	46	n.c.
47	COM1_RXD	48	n.c.
49	COM1_RTS#	50	n.c.
51	COM1_CTS#	52	n.c.

2 Hardware Description

2.1 Functional Blocks

2.1.1 CPU

Freescale 532 MHz IMX35 Processor with 133 MHz AHB Clock and 66.5 MHz external Local Bus Clock (X1B_CLKOUT).

2.1.2 Clocks

The processor clocks are generated from two crystals – a 24MHz crystal for the core frequency and a 24,576 MHz crystal for the audio subsystem.

2.1.3 I²C ID-EEPROM

The IDEEPROM is used to store module specific parameters. For a parameter overview and a memory map of the IDEEPROM please refer to appendix A. The Catalyst Supervisor CAT1026 device is used on the board to provides 2048 byte of serial electrical erasable and programmable read only memory. Data transfer between CPU and the IDEEPROM is handled via I²C Bus. The I²C Bus is routed to I²C Channel 1 of the IMX35 I²C interface. The address offset 1010000 is used to access the device.

IDEEPROM device address:	1010000x (0xA0)

Table 1 ID-EEPROM Address

2.1.4 Real Time Clock

On the EXM32-IMX35 CPU Module a discrete I2C RTC device is used so a Lithium coin cell is sufficient to buffer the device over >5 years. The Seiko Epson RTC8564NB real time clock module offers many functions such as calendar clock, alarm, timer and frequency output (1 Hz, 32 Hz, 1024 Hz and 32.768 kHz). I²C Bus Channel 1 (on IMX35) is used to access the RTC at address offset 1010001.

RTC device address:	1010001x (0xA2)

Table 2 RTC Address

For a detailed description of the real time clock device please refer to the Seiko Epson RTC8564NB Application Manual.

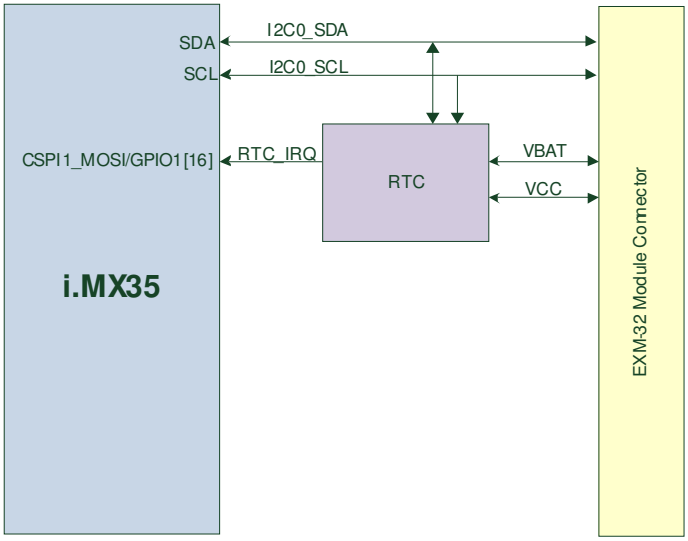


Figure 1 IMX35 and Real Time Clock

2.1.5 SPI-Interface

The EXM32-IMX35 CPU Module features one SPI interface. The interface supports up to two devices via slave select logic. SPI 2 interface of the IMX35 microprocessor is used to provide the interface.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
SRXD5	ALT2	CSPI2	MISO	22K- UP	X1A_SPI_MISO
ATA_DIOW	ALT4	CSPI2	MOSI		X1A_SPI_MOSI
ATA_DATA3	ALT4	CSPI2	SCLK		X1A_SPI_SCK
ATA_DIOR	ALT4	CSPI2	SS1	22K-UP	X1A_SPI_SS1#
ATA_CS1	ALT4	CSPI2	SS0	22K-UP	X1A_SPI_SS0

Table 3 SPI IMX35 I/O multiplexing (pin-out)

2.1.6 I²Cinterface

The EXM32-IMX35 CPU Module supports two I²C Busses. I2C1 and I2C3 interfaces of the IMX35 are used for EXM32 I2C0/1. The IMX35 I2C interface supports transfer rates of 100 Kbits/s and 400 Kbits/s.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
I2C1_CLK	ALT0	I2C1	SCL	22K-UP	X2C_I2C0_SCL
I2C1_DAT	ALT0	I2C1	SDA	22K-UP	X2C_I2C0_SDA
SD2_CLK	ALT1	I2C3	SDA	22K- UP	X2C_I2C1_SDA
SD2_CMD	ALT1	I2C3	SCL	22K- UP	X2C_I2C1_SCL

Table 4 I2C IMX35 I/O multiplexing (pin-out)

2.1.7 MMC/SD/SDIO

Multi Media Card (MMC)/
Secure Digital Memory Card (SD)/
Secure Digital Input/Output Card (SDIO)

The EXM32-IMX35 CPU Module supports an SD/SDIO/MMC I/O Card interface using the IMX35. eSDHC controller. The interface supports both write protection and card detection using IMX35 GPIOs.

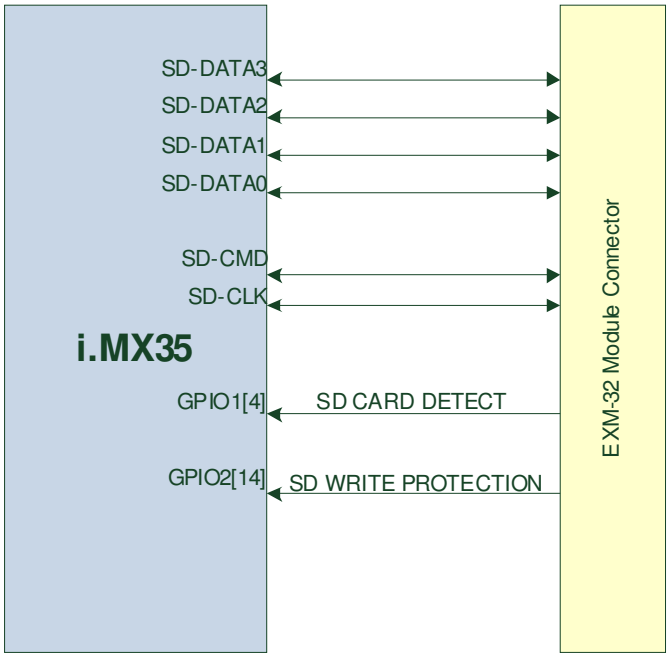


Figure 2 IMX35 SD interface

A falling edge interrupt indicates a card insertion. GPIO2[14] senses the Card Write-Protection switch.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
SD1_CMD	ALT0	ESDHC1	CMD	-	X2D_SDIO_CMD
SD1_CLK	ALT0	ESDHC1	CLK	-	X2D_SDIO_CLK
SD1_DATA0	ALT0	ESDHC1	DAT0	-	X2D_SDIO_DAT0
SD1_DATA1	ALT0	ESDHC1	DAT1	-	X2D_SDIO_DAT1
SD1_DATA2	ALT0	ESDHC1	DAT2	-	X2D_SDIO_DAT2
SD1_DATA3	ALT0	ESDHC1	DAT3	-	X2D_SDIO_DAT3
ATA_DATA14	ALT5	GPIO2	GPIO2[27]	22K-UP	X2D_SDIO_CD
STXFS4	ALT5	GPIO2	GPIO2[31]	22K-UP	X2D_SDIO_WP

Table 5 SD/MMC Card IMX35 I/O multiplexing (pin-out)

2.1.8 Linear (NOR) Flash

Up to 128MByte NOR-Flash can be populated on the module in one device connected to CS0#. Therefore the NOR-Flash can be used as boot-device

Hardware write protection for Linear Flash Memory is not supported.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function NOR-FLASH
D0-D15	ALT0	EMI	EMI_D[n]	-	DQ[0]-DQ[15]
A0-A25	ALT0	EMI	EMI_A[n]	-	A[0]-A[25]
CS0	ALT0	EMI	EMI_CS0	-	CE
RW	ALT0	EMI	EMI_RW	-	WE
OE	ALT0	EMI	EMI_OE	-	OE
TX0	ALT3	EMI	DTACK_B	-	CPLD/RDY

Table 6 Linear Flash IMX35 I/O multiplexing (pin-out)

For a detailed description of the memory space mapping please refer to chapter 3 off chip Memory.

2.1.9 NAND Flash

The EXM32-IMX35 CPU module can be populated with an 8 Bit NAND Flash. For detailed information please refer the IMX35 Processor Reference Manuel.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function NAND-FLASH
D0-D8	ALT0	EMI	EMI_D[n]	-	IO0]-IO[15]
NF_CE0	ALT0	EMI	NANDF_CE0	-	CE
NFALE	ALT0	EMI	NANDF_ALE	-	ALE
NFCLE	ALT0	EMI	NANDF_CLE	-	CLE
NFRE_B	ALT0	EMI	NANDF_RE	-	RE
NFWE_B	ALT0	EMI	NANDF_WE	-	WE
NFRB	ALT0	EMI	NANDF_RB	-	RB
NFWP_B	ALT0	EMI	NANDF_WP	-	WP

Table 7 NAND-FLASH IMX35 I/O multiplexing (pin-out)

2.1.10 Ethernet

There are two options available for the PHY used with the integrated Fast Ethernet Controller (FEC) MAC of the IMX35 microprocessor: Either a standard PHY (SMSC LAN8710i) or an IEEE1588 compatible Real-time PHY (National DP83640) can be populated.

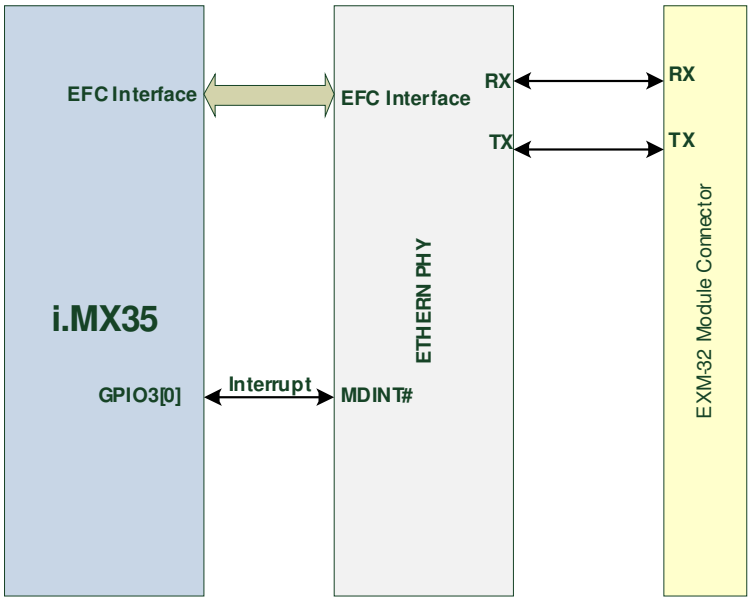


Figure 3 IMX35 Ethernet interface (PHY) SMSC LAN 8710i

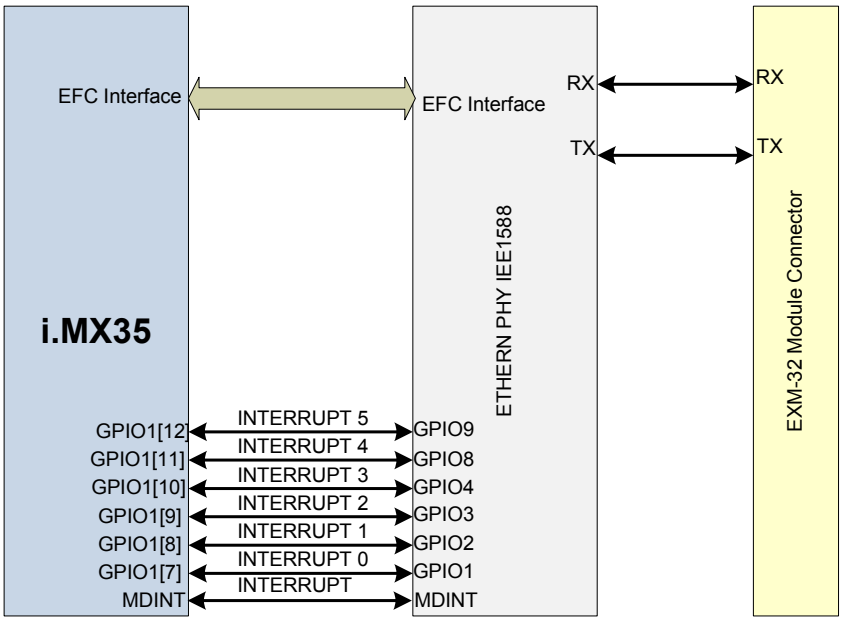


Figure 4 IMX35 Real Time Ethernet interface

Figure 4 and figure 5 show simplified wiring schemes of the MAC/PHY interface. MDINT is standard interrupt and interrupt 0-5 are Real-time IEEE1588 interrupts/GPIOs.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function ETH-PHY
FEC_TX_CLK	ALT0	FEC	TX_CLK	-	PHY_TX_CLK
FEC_RX_CLK	ALT0	FEC	RX_CLK	-	PHY_RX_CLK
FEC_RX_DV	ALT0	FEC	RX_DV	-	PHY_RX_DV
FEC_COL	ALT0	FEC	COL	-	PHY_COL
FEC_RDATA0	ALT0	FEC	RDATA[0]	-	PHY_RD[0]
FEC_TDATA0	ALT0	FEC	TDATA[0]	-	PHY_TD[0]
FEC_TX_EN	ALT0	FEC	TX_EN	-	PHY_TX_EN
FEC_MDC	ALT0	FEC	MDC		PHY_MDC
FEC_MDIO	ALT0	FEC	MDIO	-	PHY_MDIO
FEC_TX_ERR	ALT0	FEC	TX_ERR	-	PHY_TX_ERR
FEC_RX_ERR	ALT0	FEC	RX_ERR	-	PHY_RX_ERR
FEC_CRS	ALT0	FEC	CRS		PHY_CRS
FEC_RDATA1	ALT0	FEC	RDATA[1]	-	PHY_RD[1]
FEC_TDATA1	ALT0	FEC	TDATA[1]	-	PHY_TD[1]
FEC_RDATA2	ALT0	FEC	RDATA[2]	-	PHY_RD[2]
FEC_TDATA2	ALT0	FEC	TDATA[2]	-	PHY_TD[2]
FEC_RDATA3	ALT0	FEC	RDATA[3]	-	PHY_RD[3]
FEC_TDATA3	ALT0	FEC	TDATA[3]	-	PHY_TD[3]

Table 8 Ethernet IMX35 I/O multiplexing (pin-out)

2.1.11 CAN Bus

The EXM-IMX35 CPU Module has got two independent CAN interfaces. CAN<1:0>_EN (Transceiver Enable), CAN<1:0>_STB# (Transceiver Standby) and CAN<1:0>_ERR# (Bus Error Flag) are controlled via GPIO. Tx and Rx are dedicated pins of the IMX35 microprocessor.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
RTS2	ALT2	CAN2	RXCAN	100K-UP	X2A_CAN1_RX
CTS2	ALT2	CAN2	TXCAN	-	X2A_CAN1_TX
ATA_DATA6	ALT1	CAN1	TXCAN	-	X2A_CAN0_TX
ATA_DATA7	ALT1	CAN1	RXCAN	100K-UP	X2A_CAN0_RX
ATA_DATA1	ALT5	GPIO2	GPIO2[14]	-	X2A_CAN1_EN
ATA_DATA2	ALT5	GPIO2	GPIO2[15]	-	X2A_CAN0_EN
ATA_IORDY	ALT5	GPIO2	GPIO2[12]	100K-UP	X2A_CAN1_ERR#
ATA_DATA12	ALT5	GPIO2	GPIO2[25]	100K-UP	X2A_CAN0_ERR#
ATA_DATA0	ALT5	GPIO2	GPIO2[13]	-	X2A_CAN1_STB#
ATA_DATA0	ALT5	GPIO2	GPIO2[26]	-	X2A_CAN0_STB#

Table 9 IMX35 CAN I/O multiplexing (pin-out)

2.1.12 Audio Codec Interface (AC'97/I²S/LJ/RJ)

The EXM-IMX35 CPU Module features a combined AC'97 / I²S(slave) audio codec interface.
The signals are routed through the CPLD in order to adapt the audio signal to the module pin-out as required for the respective interface mode.
The audio multiplexer in the CPLD is controlled by a GPIO (IMX_I2S/AC97#_MODE).

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
STXD4	ALT0	AUDMUX	AUD4_TXD	-	CPLD0
SRXD4	ALT0	AUDMUX	AUD4_RXD	-	CPLD0
SCK4	ALT0	AUDMUX	AUD4_TXC	-	CPLD0
STXFS4	ALT0	AUDMUX	AUD4_TXFS	-	CPLD0
SD2_DATA0	ALT5	GPIO2	GPIO2[2]	-	I2S/AC97_MODE
ATA_INTRQ	ALT5	GPIO2	GPIO2[29]	100K-DN	X1C_AUDIO_RST#

Table 10 IMX35 I2S/AC9 interface to CPLD I/O multiplexing (pin-out)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Direction IMX35	Function EXM-32
STXD4	ALT0	AUDMUX	AUD4_TXD	Output	X1C_I2S_SDOUT
SRXD4	ALT0	AUDMUX	AUD4_RXD	Input	X1C_I2S_SDIN
SCK4	ALT0	AUDMUX	AUD4_TXC	Input	X1C_I2S_SCLK
STXFS4	ALT0	AUDMUX	AUD4_TXFS	Input	X1C_I2S_LRCLK

Table 11 IMX35 I2S interface I/O multiplexing (pin-out)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Direction IMX35	Function EXM-32
STXD4	ALT0	AUDMUX	AUD4_TXD	Output	X1C_AC_SDOUT
SRXD4	ALT0	AUDMUX	AUD4_RXD	Input	X1C_AC_SDIN
SCK4	ALT0	AUDMUX	AUD4_TXC	Input	X1C_AC_BCLK
STXFS4	ALT0	AUDMUX	AUD4_TXFS	Output	X1C_AC_SYNC

Table 12 IMX35 AC97 interface I/O multiplexing (pin-out)

2.1.13 UART Interfaces (COM0, COM1)

UART1 and UART3 of the IMX35 are used to implement EXM32 COM0 & COM1.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
RXD1	ALT0	UART1	RXD_MUX	22K-UP	X2D_COM0_RXD
TXD1	ALT0	UART1	TXD_MUX	-	X2D_COM0_TXD
RTS1	ALT0	UART1	RTS	22K-UP	X2D_COM0_CTS
CTS1	ALT0	UART1	CTS	-	X2D_COM0_RTS
ATA_DATA10	ALT1	UART3	RXD_MUX	22K-UP	X2D_COM1_RXD
ATA_DATA11	ALT1	UART3	TXD_MUX	-	X2D_COM1_TXD
ATA_DATA8	ALT1	UART3	RTS	22K-UP	X2D_COM1_CTS
ATA_DATA9	ALT1	UART3	CTS	-	X2D_COM1_RTS

Table 13 IMX35 UART I/O multiplexing (pin-out)

2.1.14 Media Local Bus (MLB)

The 3-wire MLB interface of the IMX35 microprocessors is routed to the respective EXM32 connector pins. For detailed MLB capability please refer to the IMX35 Reference Manual chapter 36.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
MLB_CLK	ALT0	MLB	RXD_MUX	22K-UP	X2A_MLB_MCLK
MLB_DAT	ALT0	MLB	TXD_MUX	-	X2A_MLB_MDAT
MLB_SIG	ALT0	MLB	RTS	-	X2A_MLB_MSIG

Table 14 IMX35 MLB I/O multiplexing (pin-out)

2.1.15 USB

The IMX35 microprocessor has got two independent USB interfaces, one of which is a High-Speed USB-OTG Port, while the other interface is just a Full-Speed USB Host.

There are three assembly options in the IMX35 CPU module:

USB Hub is populated:

- 3x full speed USB host and 1x High Speed On–The-Go.
- Four High speed USB ports, HOST only.

USB Hub is not populated

- 1x Full speed USB host and 1x High speed On-The-Go, in this case USB is only available on motherboards.

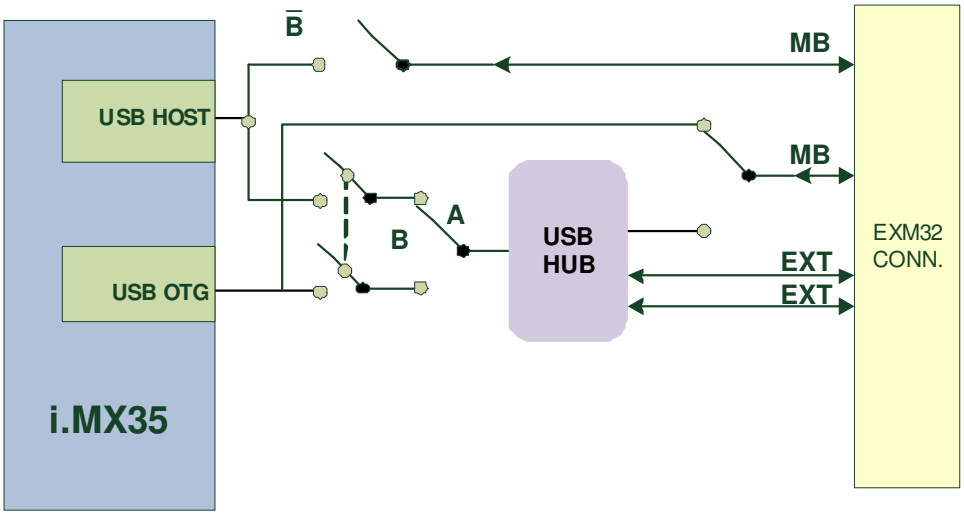


Figure 5 IMX35 USB interface

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
USBPHY1_VBUS	ALT0	USBPHY_UTMI	USBPHY1_VBUS	-	X2A_USB_OTG_VBUS
USBPHY1_DP	ALT0	USBPHY_UTMI	USBPHY1_DP	-	X2A_USB_OTG_D+
USBPHY1_DM	ALT0	USBPHY_UTMI	USBPHY1_DM	-	X2A_USB_OTG_D-
USBPHY1_UID	ALT0	USBPHY_UTMI	USBPHY1_UID	-	X2A_USB_OTG_ID
USBOTG_PWR	ALT0	USBPHY_UTMI	USBOTG_PWR	100K-DN	X2A_USB_OTG_PWEN
I2C2_CLK	ALT2	USB_TOP	USBH2_PWR	100K-DN	X2A_USB_MB_PWEN
USBPHY2_DM	ALT0	USBPHY_UTMI	USBXCVR		X2A_USB_MB_D-
USBPHY2_DP	ALT0	USBPHY_UTMI	USBXCVR		X2A_USB_MB_D+
USBOTG_OC	ALT0	USBPHY_UTMI	USBOTG_OC	22K-UP	X2A_USB_OC
I2C2_DAT	ALT2	USB_TOP	USBH2_OC	22K-UP	X2A_USB_OC

Table 15 IMX35 Full Speed USB/High Speed (no HUB) OTG I/O multiplexing (pin-out)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
USBPHY1_VBUS	ALT0	USBPHY_UTMI	USBPHY1_VBUS	-	X2A_USB_OTG_VBUS
USBPHY1_DP	ALT0	USBPHY_UTMI	USBPHY1_DP	-	X2A_USB_OTG_D+
USBPHY1_DM	ALT0	USBPHY_UTMI	USBPHY1_DM	-	X2A_USB_OTG_D-
USBPHY1_UID	ALT0	USBPHY_UTMI	USBPHY1_UID	-	X2A_USB_OTG_ID
USBOTG_PWR	ALT0	USBPHY_UTMI	USBOTG_PWR	100K-DN	X2A_USB_OTG_PWEN
USBPHY2_DM	ALT0	USBPHY_UTMI	USBXCVR	-	X2A_USB_MB_D-
USBPHY2_DP	ALT0	USBPHY_UTMI	USBXCVR	-	X2A_USB_MB_D+
USBOTG_OC	ALT0	USBPHY_UTMI	USBOTG_OC	22K-UP	X2A_USB_OC
I2C2_DAT	ALT02	USB_TOP	USBH2_OC	22K-UP	X2A_USB_OC

Table 16 IMX35 Full Speed USB/High Speed OTG (with HUB) I/O multiplexing (pin-out)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function USB-HUB
USBPHY1_DP	ALT0	USBPHY_UTMI	USBPHY1_DP	-	USBUP_D+
USBPHY1_DM	ALT0	USBPHY_UTMI	USBPHY1_DM	-	USBUP_D-
USBOTG_OC	ALT0	USBPHY_UTMI	USBOTG_OC	22K-UP	X2A_USB_OC
I2C2_DAT	ALT02	USB_TOP	USBH2_OC	22K-UP	X2A_USB_OC

Table 17 IMX35 High Speed USB interface (with HUB)

USBOTG_OC and I2C2_DAT must always be configured as input USBOTG_PWR (Pull-Down) and I2C2_CLK (Pull-Up) as output.

2.1.16 Compact Flash

The CF-interface implemented on the EXM32 IMX35 module supports only PC Card Memory Mode and PC Card I/O Mode, while True IDE Mode is not supported. The various operational modes are implemented by address decoding. For detailed information please refer to the Compact Flash Specification.

Slot	Chip select	Base address
Slot 1	CS4	0xB4000000
Slot 2	CS4	0xB4000000

Table 18 Compact Flash address space

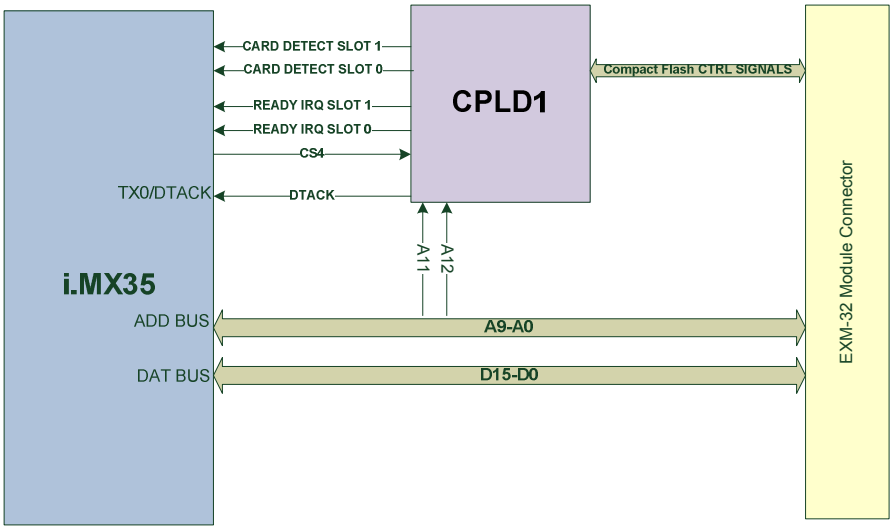


Figure 6 IMX35 Compact Flash interface

Only address bits A0-A9 are used for the Compact Flash interface in DTACK mode. Card Detect and READY or IRQ signals connected to GPIOs.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
CS4	ALT0	EMI	EMI_CS4	-	-
TX0	ALT3	EMI	EMI_DTAC	22K-UP	X1A_CF_WAIT#
TX1	ALT5	GPIO1	GPIO1[14]	22K-UP	X1A_CF1_CD#
TX2_RX3	ALT5	GPIO1	GPIO1[13]	22K-UP	X1A_CF0_CD#
ATA_DA0	ALT5	GPIO3	GPIO3[0]	22K-UP	X1A_CF0_RDY_IRQ#
TXD2	ALT5	GPIO3	GPIO3[11]	22K-UP	X1A_CF1_RDY_IRQ#

Table 19 IMX35 Compact Flash I/O multiplexing (pin-out)

Slot	Operation Mode	Chip select	Base Address
Slot 1	PC Card Memory Mode	CS4	0xB4000800
Slot 1	PC Card I/O Mode	CS4	0xB4000800
Slot 2	PC Card Memory Mode	CS4	0xB4002800
Slot 2	PC Card I/O Mode	CS4	0xB4002800

Table 20 Compact Flash operation modes

Address **bus A11 is used to decode Memory Mode or I/O Mode cycles.**

Slot	PC Card Memory Mode	Chip select	Base Address
Slot 1	Common Memory Mode	CS4	0xB4000000
Slot 1	Attribute Mode	CS4	0xB4001000
Slot 2	Common Memory Mode	CS4	0xB4002000
Slot 2	Attribute Mode	CS4	0xB4003000

Table 21 Compact Flash PC Card Memory Mode sub operations

For reliable operation of the CF-Interface the memory controller must be configured as follows:

	Description
CSA	TBD
OEA	TBD
LBA	TBD
DCT	TBD
EDC	TBD

Table 22 IMX35 CS4 and CS5 Compact Flash Timings

CS5 not available

2.1.17 Graphics Controller

The LCD-controller signals are routed directly to the EXM connector.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
LD0	ALT0	IPU	IPU_D[n]	-	X2D_LCD_B0
LD1	ALT0	IPU	IPU_D[n]	-	X2D_LCD_B1
LD2	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B2
LD3	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B3
LD4	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B4
LD5	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B5
LD6	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B6
LD7	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B7
LD8	ALT0	IPU	IPU_D[n]	-	X2D_LCD_G0
LD9	ALT0	IPU	IPU_D[n]	-	X2D_LCD_G1
LD10	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G2
LD11	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G3
LD12	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G4
LD13	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G5
LD14	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G6
LD15	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G7
LD16	ALT0	IPU	IPU_D[n]	-	X2D_LCD_R0
LD17	ALT0	IPU	IPU_D[n]	-	X2D_LCD_R1
LD18	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R2
LD19	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R3
LD20	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R4
LD21	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R5
LD22	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R6
LD23	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R7
D3_HSYNC	ALT0	IPU	DISPB_D3_HSYNC	-	X2C_LCD_HSYNC
D3_FPSHIFT	ALT0	IPU	IDISPB_D3_CLK	-	X2C_LCD_SHFCLK
D3_DRDY	ALT0	IPU	DISPB_D3_DRDY	-	X2C_LCD_M_DE
D3_VSYNC	ALT0	IPU	DISPB_D3_VSYNC	-	X2C_LCD_R5

Table 23 IMX35 24 Bit LCD interface I/O multiplexing (pin-out)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
LD0	ALT0	GPIO2	GPIO2[0]	-	X2C_GP_OUT2
LD1	ALT0	GPIO2	GPIO2[1]	-	X2C_GP_OUT3
LD2	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B0
LD3	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B1
LD4	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B2
LD5	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B3
LD6	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B4
LD7	ALT0	IPU	IPU_D[n]	-	X2C_LCD_B5
LD8	ALT0	GPIO2	GPIO2[8]	-	X2C_GP_OUT4
LD9	ALT0	GPIO2	GPIO2[9]	-	X2C_GP_OUT5
LD10	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G0
LD11	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G1
LD12	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G2
LD13	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G3
LD14	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G4
LD15	ALT0	IPU	IPU_D[n]	-	X2C_LCD_G5
LD16	ALT0	GPIO2	GPIO2[16]	-	X2C_GP_OUT6
LD17	ALT0	GPIO2	GPIO2[17]	-	X2C_GP_OUT7
LD18	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R0
LD19	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R1
LD20	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R2
LD21	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R3
LD22	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R4
LD23	ALT0	IPU	IPU_D[n]	-	X2C_LCD_R5
D3_HSYNC	ALT0	IPU	DISPB_D3_HSYNC	-	X2C_LCD_HSYNC
D3_FPSHIFT	ALT0	IPU	IDISPB_D3_CLK	-	X2C_LCD_SHFCLK
D3_DRDY	ALT0	IPU	DISPB_D3_DRDY	-	X2C_LCD_M_DE
D3_VSYNC	ALT0	IPU	DISPB_D3_VSYNC		X2C_LCD_R5

Table 24 IMX35 18 Bit LCD interface I/O multiplexing (pin-out)

The IPU interface must generally be configured for 24-bit mode. In 18 bit mode the two least significant bits of each colour component must be configured as GPIO (GP-OUT).

2.1.18 IPU-CSI (CAMERA SENSOR INTERFACE)

A subset of the camera interface of the IMX35 CPU is available on the EXM32 camera interface for 8-Bit BT.656 video sources. The CSI is routed through a CPLD, since the signals also serve as strap-option pins during Reset. For detailed boot options of the microprocessor please refer the IMX35 Reference Manual.

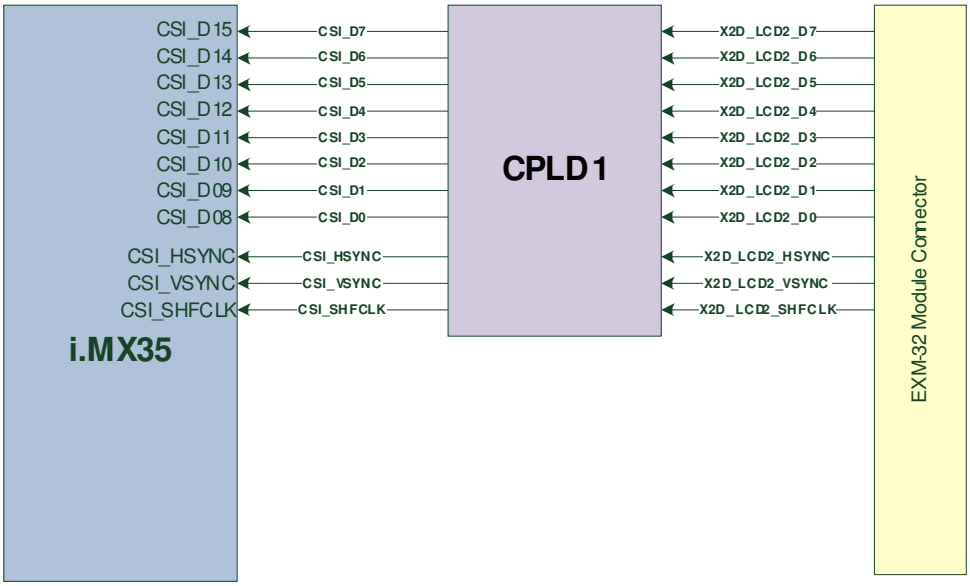


Figure 7 IMX35 Camera Sensor interface

The IMX35 CPU can boot from NOR-Flash, NAND-Flash, SD-Card or NOR-Flash populated on motherboards. The various boot modes are selected by the EXM32 signals Module_ID0/1.

Boot medium	Baseboard Module ID	Chip select
NOR-FLASH	00	CS0
NAND-FLASH	00	CSN
SD-CARD	10 or 01	-
NOR-FLASH(TEST mode)	11	CSA

Table 25 IMX35 Boots Modes

For detailed EXM32 pin multiplexing please refer the EXM32 specification.

2.1.19 GPIO

The IMX35 microprocessor provides 3 Banks of GPIO with interrupt capability; all system interrupts are located on GPIO Bank 1.

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	GPIO	Interrupt capability	Function EXM-32
STXD5	ALT5	GPIO1	GPIO1[0]	22K-UP	IN	Yes	X1B_IRQ_MB0#
CONTRAST	ALT5	GPIO1	GPIO1[1]	22K-UN	IN	Yes	X1B_IRQ_MB1#
SCK5	ALT5	GPIO1	GPIO1[2]	22K-UP	IN	Yes	X1B_IRQ_MB2#
D3_REV	ALT5	GPIO1	GPIO1[3]	----------	OUT	NO	IMX_CNFG_RDY
STXFS5	ALT5	GPIO1	GPIO1[3]	22K-UP	IN	Yes	X2D_SDIO_CD#
D3_CLS	ALT5	GPIO1	GPIO1[4]	22K-UP	IN	Yes	X1B_IRQ_EXT0#
D3_SPL	ALT5	GPIO1	GPIO1[5]	22K-UP	IN	Yes	X1B_IRQ_EXT1#
HCKR	ALT5	GPIO1	GPIO1[6]	100K-DN	IN	Yes	IMX_WAKEUP
SCKT	ALT5	GPIO1	GPIO1[7]	----------	IN	Yes	IMX_IEE_INT0
FST	ALT5	GPIO1	GPIO1[8]	----------	IN	Yes	IMX_IEE_INT1
HCKT	ALT5	GPIO1	GPIO1[9]	----------	IN	Yes	IMX_IEE_INT2
TX5_RX0	ALT5	GPIO1	GPIO1[10]	----------	IN	Yes	IMX_IEE_INT3
TX4_RX1	ALT5	GPIO1	GPIO1[11]	----------	IN	Yes	IMX_IEE_INT4
TX3_RX2	ALT5	GPIO1	GPIO1[12]	----------	IN	Yes	IMX_IEE_INT5
TX2_RX3	ALT5	GPIO1	GPIO1[13]	22K-UP	IN	Yes	IMX_CF_CD1#
TX1	ALT5	GPIO1	GPIO1[14]	22K-UP	IN	Yes	IMX_CF_CD2#
CSPI1_MOSI	ALT5	GPIO1	GPIO1[16]	22K-UP	IN	Yes	RTC_IRQ#
CSPI1_MISO	ALT5	GPIO1	GPIO1[17]	22K-UP	IN	Yes	IMX_ETH_MDINT#
CSPI1_SS0#	ALT5	GPIO1	GPIO1[18]	----------	OUT	NO	IMX_FUSE_WRITE
CSPI1_SS1#	ALT5	GPIO1	GPIO1[19]	----------	OUT	NO	IMX_CPLD0_GPIO0
CSI_MCLK	ALT5	GPIO1	GPIO1[28]	----------	IN	TBD	IMX_CPLD0_GPIO1

Table 26 IMX35 GPIO Bank 1 I/O multiplexing

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	IGPIO	Interrupt capability	Function
DD2_DATA0	ALT5	GPIO2	GPIO2[2]	----------	OUT	NO	IMX_AUDIO_RST#
SD2_DATA1	ALT5	GPIO2	GPIO2[3]	----------	OUT	NO	X1D_DRAK0#
SD2_DATA2	ALT5	GPIO2	GPIO2[4]	----------	OUT	NO	X1D_DRAK1#
SD2_DATA3	ALT5	GPIO2	GPIO2[5]	----------	OUT	NO	X2C_LCD_BLON
ATA_CS0	ALT5	GPIO2	GPIO2[6]	----------	OUT	NO	X2C_LCD_VCON
ATA_DMACK	ALT5	GPIO2	GPIO2[10]	----------	OUT	NO	X2C_LCD_VDON
ATA_RESET#	ALT5	GPIO2	GPIO2[11]	----------	OUT	NO	X2C_LCD_DON
ATA_IORDY	ALT5	GPIO2	GPIO2[12]	----------	IN	NO	X2A_CAN1_ERR#
ATA_DATA0	ALT5	GPIO2	GPIO2[13]	----------	OUT	NO	X2A_CAN1_STB#
ATA_DATA1	ALT5	GPIO2	GPIO2[14]	----------	OUT	NO	X2A_CAN1_EN
ATA_DATA2	ALT5	GPIO2	GPIO2[15]	----------	OUT	NO	X2A_CAN0_EN
ATA_DATA5	ALT5	GPIO2	GPIO2[18]	----------	OUT	NO	IMX_RESET_OUT#
ATA_DATA12	ALT5	GPIO2	GPIO2[25]	----------	IN	NO	X2A_CAN0_ERR#
ATA_DATA13	ALT5	GPIO2	GPIO2[26]	----------	OUT	NO	X2A_CAN0_STB#
ATA_DATA14	ALT5	GPIO2	GPIO2[27]	----------	OUT	NO	X2D_SDIO_WP
ATA_DATA15	ALT5	GPIO2	GPIO2[28]	----------	OUT	NO	X2D_LCD2_EN
ATA_INTRQ	ALT5	GPIO2	GPIO2[29]	----------	OUT	NO	IMX_I2S / AC97#_MODE
ATA_BUFF_EN	ALT5	GPIO2	GPIO2[30]	----------	OUT	NO	X2D_GP_OUT0
ATA_DMARQ	ALT5	GPIO2	GPIO2[31]	----------	OUT	NO	X2D_GP_OUT1
LD0	ALT5	GPIO2	GPIO2[0]	----------	OUT	NO	X2D_GP_OUT2
LD1	ALT5	GPIO2	GPIO2[1]	----------	OUT	NO	X2D_GP_OUT3
LD8	ALT5	GPIO2	GPIO2[8]	----------	OUT	NO	X2D_GP_OUT4
LD9	ALT5	GPIO2	GPIO2[9]	----------	OUT	NO	X2D_GP_OUT5
LD16	ALT5	GPIO2	GPIO2[16]	----------	OUT	NO	X2D_GP_OUT6
LD17	ALT5	GPIO2	GPIO2[17]	----------	OUT	NO	X2D_GP_OUT7

Table 27 IMX35 GPIO Bank 2 I/O multiplexing

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	IGPIO	Interrupt capability	Function
GPIO3[0]		GPIO3	GPIO3[]	----------	IN	NO	GPIO_DDR_ASMBLY_OPT
ATA_DA0		GPIO3	GPIO3[]	----------	IN	NO	IMX_CPLD1_GPIO0
ATA_DA1		GPIO3	GPIO3[]	----------	OUT	NO	IMX_SUSPEND
ATA_DA2		GPIO3	GPIO3[]	----------	OUT	NO	IMX_USER_LED0#
CSPI1_SCLK		GPIO3	GPIO3[]	----------	OUT	NO	X1D_DACK0#
CSPI1_SPI_RDY		GPIO3	GPIO3[]	----------	OUT	NO	X1D_DACK1#
ATA_DA0 RXD2		GPIO3	GPIO3[]	----------	OUT	NO	IMX_USER_LED1#
TXD2		GPIO3	GPIO3[]	----------	IN	NO	IMX_CPLD1_GPIO1

Table 28 IMX35 GPIO Bank 3 I/O multiplexing

2.1.20 DDR2 SDRAM

During initialisation the software can detect the amount of DRAM populated on the module by reading GPIO3[0] (H=256MByte/L=128MByte). It is not possible to detect memory by reading/writing invalid memory.
After reading GPIO3[0] the pin-multiplexing must be changed as follows:

1. Set GPIO3[0] as input
2. Read GPIO3[0]
3. Route GPIO3[0] to pin ATA_DA0
4. Set respective daisy chain bit

The EXM32-IMX35 CPU Module can be populated with up to 256 Mbyte / 133MHz DDR2 SDRAM memory, organized in 2 banks of 2 x16-devices (512MBit), each. For the 128-MByte configuration only bank 0 is populated.
For detailed description of the memory space mapping and for detailed setup and initialization of the IMX35 SDRAM Controller please refer to chapter 3 (3.3.7/3.3.8) "Off chip Memory Map".

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function DDR Memory
SD0	ALT0	EMI	DRAM[0]	-	SD0
SD1	ALT0	EMI	DRAM[1]	-	SD1
SD2	ALT0	EMI	DRAM[2]	-	SD2
SD3	ALT0	EMI	DRAM[3]	-	SD3
SD4	ALT0	EMI	DRAM[4]	-	SD4
SD5	ALT0	EMI	DRAM[5]	-	SD5
SD6	ALT0	EMI	DRAM[6]	-	SD6
SD7	ALT0	EMI	DRAM[7]	-	SD7
SD8	ALT0	EMI	DRAM[8]	-	SD8
SD9	ALT0	EMI	DRAM[9]	-	SD9
SD10	ALT0	EMI	DRAM[10]	-	SD10
SD11	ALT0	EMI	DRAM[11]	-	SD11
SD12	ALT0	EMI	DRAM[12]	-	SD12
SD13	ALT0	EMI	DRAM[13]	-	SD13
SD14	ALT0	EMI	DRAM[14]		SD14
SD15	ALT0	EMI	DRAM[15]	-	SD15
SD16	ALT0	EMI	DRAM[16]	-	SD16
SD17	ALT0	EMI	DRAM[17]	-	SD17
SD18	ALT0	EMI	DRAM[18]	-	SD18
SD19	ALT0	EMI	DRAM[19]	-	SD19
SD20	ALT0	EMI	DRAM[20]	-	SD20
SD21	ALT0	EMI	DRAM[21]	-	SD21
SD22	ALT0	EMI	DRAM[22]	-	SD22
SD23	ALT0	EMI	DRAM[23]	-	SD23
SD24	ALT0	EMI	DRAM[24]	-	SD24
SD24	ALT0	EMI	DRAM[25]	-	SD24
SD26	ALT0	EMI	DRAM[26]	-	SD26
SD27	ALT0	EMI	DRAM[27]	-	SD27
SD28	ALT0	EMI	DRAM[28]	-	SD28

SD29	ALT0	EMI	DRAM[29]	-	SD29
SD30	ALT0	EMI	DRAM[30]	-	SD30
SD31	ALT0	EMI	DRAM[31]	-	SD31
SDBA1	ALT0	EMI	EMI_SDBA1	-	SDBA1
SABA0	ALT0	EMI	EMI_SDBA0	-	SABA0
DQM0	ALT0	EMI	DRAM_DQM0	-	DQM0
DQM1	ALT0	EMI	DRAM_DQM1	-	DQM1
DQM2	ALT0	EMI	DRAM_DQM2	-	DQM2
DQM3	ALT0	EMI	DRAM_DQM3	-	DQM3
RAS	ALT0	EMI	DRAM_RAS	-	RAS
CAS	ALT0	EMI	DRAM_CAS	-	CAS
SDWE	ALT0	EMI	DRAM_SDWE	-	SDWE
SDCKE0	ALT0	EMI	DRAM_SDCKE0	-	SDCKE0
SDCKE1	ALT0	EMI	DRAM_SDCKE1	-	SDCKE1
SDCLK	ALT0	EMI	DRAM_SCLK	-	SDCLK
SDQS0	ALT0	EMI	DRAM_SDQS[0]	-	SDQS0
SDQS1	ALT0	EMI	DRAM_SDQS[1]	-	SDQS1
SDQS2	ALT0	EMI	DRAM_SDQS[2]	-	SDQS2
SDQS3	ALT0	EMI	DRAM_SDQS[3]	-	SDQS3
A0	ALT0	EMI	EMI_DA_H[0]	-	A0
A1	ALT0	EMI	EMI_DA_H[1]	-	A1
A2	ALT0	EMI	EMI_DA_H[2]	-	A2
A3	ALT0	EMI	EMI_DA_H[3]	-	A3
A4	ALT0	EMI	EMI_DA_H[4]	-	A4
A5	ALT0	EMI	EMI_DA_H[5]	-	A5
A6	ALT0	EMI	EMI_DA_H[6]	-	A6
A7	ALT0	EMI	EMI_DA_H[7]	-	A7
A8	ALT0	EMI	EMI_DA_H[8]	-	A8
A9	ALT0	EMI	EMI_DA_H[9]	-	A9
MA10	ALT0	EMI	EMI_DA_H[10]	-	MA10
MA11	ALT0	EMI	EMI_DA_H[11]	-	MA11
MA12	ALT0	EMI	EMI_DA_H[12]	-	MA12
SDCLK#	ALT0	EMI	DRAM_SDCLK#	-	SDCLK#

Table 29 IMX35 Memory interface

	Address Space	**Memory Select**
Bank 0	0x80000000-0x8FFFFFFF	CS0 (CS2)
Bank 1	0x90000000-0x9FFFFFFF	CS1 (CS3)

Table 30 IMX35 Memory Space

The following register settings (defaults) are needed to select the appropriate power-rail for the SDRAM memory.

Address	Source	Power Supply in V	Value
0x43FAC794	CAS, RAS, SDCKE0, SDCKE1	1.8	0x00001000
0x43FAC798	SDQS0, SDQS1, SDQS2, SDQS3	1.8	0x00001000
0x43FAC79C	SDBA0. SDBA 1	1.8	0x00001000
0x43FAC7A0	SD0-SD31	1.8	0x00001000
0x43FAC7A4	A0-A25, DQM0 – DQM3, MA10	1.8	0x00001000

Table 31 IMX35 Memory interface power supply register

WARNING: Setting this registers to 0x00000800 (Power Supply 3.3V) may damage the memory.

3 Programming Guide

3.1 Peripheral Memory Map

For a description of the Peripheral Memory Space please refer to the IMX35 Hardware Manual.

3.2 Off-chip Memory Map

AREA	OFF-CHIP ADDRESSES A25-A0			SIZE	BUS WIDTH	INTERFACE
0	0xA0000000	to	0xA7FFFFFF	128 MB	16-bit	CS0 (Flash)
1	0xA8000000	to	0xAFFFFFFF	128 MB	16-bit	CS1 (Flash)
2	0xB0000000	to	0xB1FFFFFF	32 MB	16-bit	CS2 (SRAM)
3	0xB2000000	to	0xB3FFFFFF	32 MB	16-bit 16-bit	CS3 (Spare)
4	0xB4000000	to	0xB5FFFFFF	32 MB	16-bit 16-bit	CS4 (Spare)
5	0xB6000000	to	0xB7FFFFFF	32 MB	16-bit	CS5 (spare)

Table 32 IMX35 external memory space

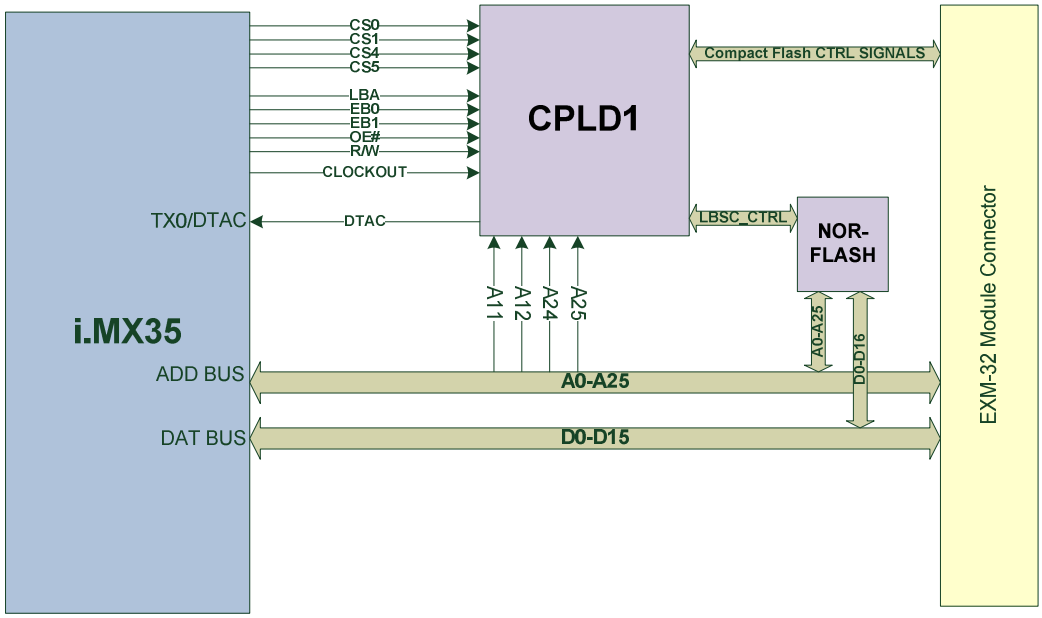


Figure 8 IMX35 external Local Bus architecture

The TX0 pin of the IMX35 must be configured as Data Acknowledge (DTACK) input. Data Acknowledge is used for CS1, CS4 and CS5. The CLKO pin must be configured to output the Local Bus clock signal (= AHB-Clock/2)

Pad Name IMX35	Mode IMX35	Instance IMX35	Port	Pad settings IMX35	Function EXM-32
D0	ALT0	EMI	EMI_D[0]	-	X1B_D0
D1	ALT0	EMI	EMI_D[1]	-	X1B_D1
D2	ALT0	EMI	EMI_D[2]	-	X1B_D2
D3	ALT0	EMI	EMI_D[3]	-	X1B_D3
D4	ALT0	EMI	EMI_D[4]	-	X1B_D4
D5	ALT0	EMI	EMI_D[5]	-	X1B_D5
D6	ALT0	EMI	EMI_D[6]	-	X1B_D6
D7	ALT0	EMI	EMI_D[7]	-	X1B_D7
D8	ALT0	EMI	EMI_D[8]	-	X1B_D8
D9	ALT0	EMI	EMI_D[9]	-	X1B_D9
D10	ALT0	EMI	EMI_D[10]	-	X1B_D10
D11	ALT0	EMI	EMI_D[11]	-	X1B_D11
D12	ALT0	EMI	EMI_D[12]	-	X1B_D12
D13	ALT0	EMI	EMI_D[13]	-	X1B_D13
D14	ALT0	EMI	EMI_D[14]	-	X1B_D14
D15	ALT0	EMI	EMI_D[15]	-	X1B_D15
A0	ALT0	EMI	EMI_DA_L[0]	-	X1D_A1
A1	ALT0	EMI	EMI_DA_L[1]	-	X1D_A2
A2	ALT0	EMI	EMI_DA_L[2]	-	X1D_A3
A3	ALT0	EMI	EMI_DA_L[3]	-	X1D_A4
A4	ALT0	EMI	EMI_DA_L[4]	-	X1D_A5
A5	ALT0	EMI	EMI_DA_L[5]	-	X1D_A6
A6	ALT0	EMI	EMI_DA_L[6]	-	X1D_A7
A7	ALT0	EMI	EMI_DA_L[7]	-	X1D_A8
A8	ALT0	EMI	EMI_DA_L[8]	-	X1D_A9
A9	ALT0	EMI	EMI_DA_L[9]	-	X1D_A10
A10	ALT0	EMI	EMI_DA_L[10]	-	X1D_A11
A11	ALT0	EMI	EMI_DA_L[11]	-	X1D_A12
A12	ALT0	EMI	EMI_DA_L[12]	-	X1D_A13
A13	ALT0	EMI	EMI_DA_L[13]	-	X1D_A14
A14	ALT0	EMI	EMI_DA_L[14]	-	X1D_A15
A15	ALT0	EMI	EMI_DA_L[15]	-	X1D_A16
A16	ALT0	EMI	EMI_DA_L[16]	-	X1D_A17
A17	ALT0	EMI	EMI_DA_L[17]	-	X1D_A18
A18	ALT0	EMI	EMI_DA_L[18]	-	X1D_A19
A19	ALT0	EMI	EMI_DA_L[19]	-	X1D_A20
A20	ALT0	EMI	EMI_DA_L[20]	-	X1D_A21
A21	ALT0	EMI	EMI_DA_L[21]	-	X1D_A22
A22	ALT0	EMI	EMI_DA_L[22]	-	X1D_A23
A23	ALT0	EMI	EMI_DA_L[23]	-	X1D_A24
A24	ALT0	EMI	EMI_DA_L[24]	-	X1D_A25
A25	ALT0	EMI	EMI_DA_L[25]	-	-
CLKO	ALT0	CCM	CLKO	-	X1B_BUSCLK

EB0	ALT0	EMI	EMI_EB0	-	X1B_BE0
EB1	ALT0	EMI	EMI_EB1	-	X1B_BE1
OE	ALT0	EMI	EMI_OE	-	X1B_OE#
CS0	ALT0	EMI	EMI_CS0	-	NOR_FLASH_CS0#
CS1	ALT0	EMI	EMI_CS1	-	X1B_CSA
CS2	ALT0	EMI	EMI_CS2	-	DDR_CS0
CS3	ALT0	EMI	EMI_CS3	-	DDR_CS1
CS4	ALT0	EMI	EMI_CS4	-	-
CS5	ALT0	EMI	EMI_CS5	-	-
LBA	ALT0	EMI	EMI_LBA	-	-
RW	ALT0	EMI	EMI_RW	-	X1B_R/W#
TX0	ALT3	EMI	EMI_DTAC	-	X1B_RDY/X1A_CF_WAIT#
COMPARE	ALT7	SDMA	EXTDMA_2		X1D_DREQ0#
GPIO1_1	ALT7	SDMA	EXTDMA_1		X1D_DREQ1#

Table 33 IMX35 Local Bus I/O multiplexing

3.3 Local Bus External Timing Definition

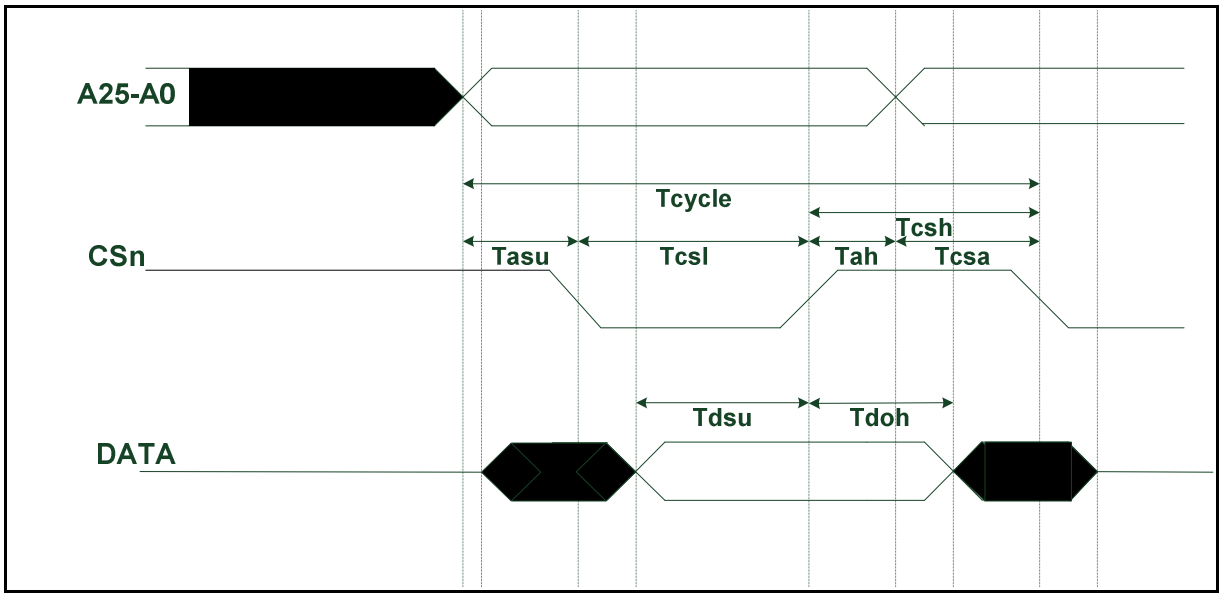


Figure 9 External Bus Timing definitions

Definition	Description	Time in ns
Tcycle	Read or Write Cycle	150
Tcsl	Chip select Assertion Time	106
Tcsh	Chip select Deassertion Time	44
Tcsdv	Chip select Valid	--
Tasu	Address Setup Time	22
Tah	Address Hold Time	8
Tdoh	Data Hold Time	34

Table 34 Bus Timing Definitions

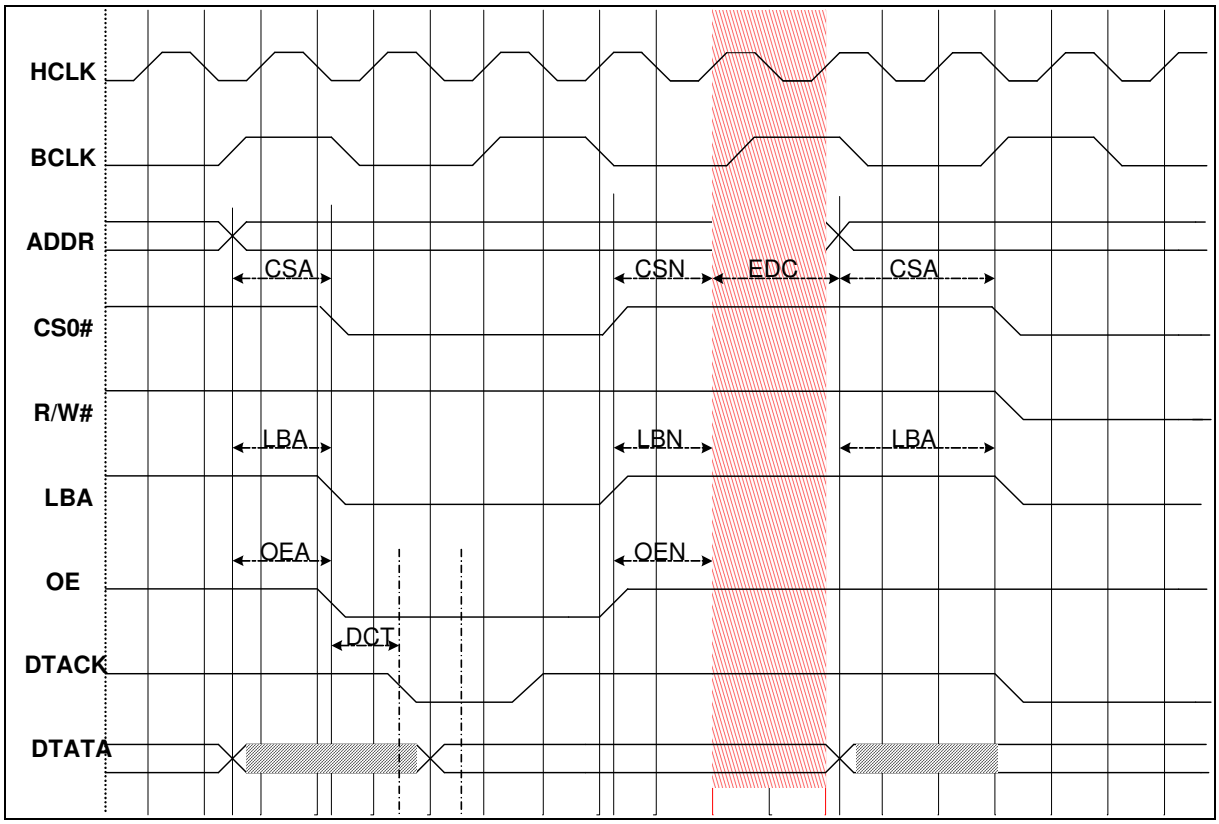


Figure 10 IMX35 Internal Bus Timing

Figure 10 shows the bus timing of the IMX35 CPU on the module. The bus timing parameters must be configured for each CS# signal. BCLK is alyways half of AHB Clock (HCLK).

	Time in ns
CSA /CSN	24/24
OEA/OEN	46/22
LBA	---
DCT	46
EDC	15
Data Setup	34

Table 35 IMX35 WEIM Timing Configuration Register Bits

3.3.1 Area 0 (Nor-Flash)

Area 0 (CS0#) addresses up to 128MByte NOR-Flash. The CS0# address space is mapped to 0xA0000000 to 0xA7FFFFFF.

	Description
CSA	---
OEA	---
LBA	---
DCT	---
EDC	---

Table 36 Chip Select 0 Timings

WEIM control registers for Area 0 default values please refer Datasheet.

3.3.2 Area 1

Area 1 (CS1#) is reserved for EXM32 (Motherboards) Local Bus chip select (X1B_CSA#) , mapped to 0xA800 0000 - 0xAFFF FFFF.

	Description
CSA	6
OEA	C
LBA	0
DCT	0
EDC	2

Table 37 Chip Select 1 Timings

WEIM control registers for Area 1

0xB8002010 → 0x3F02
0xB8002014 → 0xCACA6561
0xB8002018 → 0xCACA1000

3.3.3 Area 2

CS2#

CS0# for DDR Memory.

3.3.4 Area 3

CS3#

CS1# for DDR Memory.

3.3.5 Area 4

CS4# Compact Flash Slot 0 (0xB4000000 to 0xB5FFFFFF)

	Description
CSA	5
OEA	F
LBA	2
DCT	3
EDC	0

Table 38 Chip Select 4 Compact Flash Timings

WEIM control registers for Area 4

0xB8002040 → 0x3F00
0xB8002044 → 0xFA005551
0xB8002048 → 0x22FA0A30

3.3.6 Area 5

This Area is no longer available

CS5# Compact Flash Slot (0xB6000000 to 0xB7FFFFFF)

	Description
CSA	---
OEA	---
LBA	---
DCT	---
EDC	---

Table 39 Chip Select 5 Compact Flash Timings

3.3.7 Area 0 DDR Memory Bank 0

DDR-Memory CS0# (0x80000000 - 0x8FFFFFFF).
The following memory bus timings are needed for reliable system operation.

ESDCFG0 **Address 0xB8001004**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W										tXP		tWTR	tRp		tMRD	
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	tWR	tRAS			tRRD		tCAS			tRCD			tRC			
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	1	1	1	1	1	1	0	0	0	0	1	1	0	1	0	0

Table 40 IMX35 Bank 2 SDRAM Timing Register

3.3.8 Area 1 DDR Memory Bank 1

DDR-Memory CS1# (0x90000000 - 0x9FFFFFFF).

The following memory bus timings are needed for reliable system operation.

ESDCFG1 **Address 0xB800100C**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W										tXP		tWTR	tRp		tMRD	
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	tWR	tRAS			tRRD		tCAS			tRCD			tRC			
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	1	1	1	1	1	1	0	0	0	0	1	1	0	1	0	0

Table 41 IMX35 Bank 1 SDRAM Timing Register

4 Pin I/O Multiplexing

4.1.1 IMX35 Pin-Out

The base address for I/O multiplexing and daisy chain is 0x43FAC000.

Pad Name	Mode	Instance	Port	Function
CAPTURE	ALT4	CCM	CLK32K	
COMPARE	ALT7	SDMA	EXTDMA_2	
WDOG_RST	ALT0	WDOG	WDOG_B	
GPIO1_0	ALT1	CCM	PMIC_RDY	
GPIO1_1	ALT7	SDMA	EXTDMA_1	
GPIO2_0	ALT0	GPIO2	GPIO[0]	
GPIO3_0	ALT0	GPIO3	GPIO[0]	
CLKO	ALT0	CCM	CLKO	
VSTBY	ALT0	CCM	VSTBY	
CS1	ALT0	EMI	EIM_CS1	
CS2	No Muxing	EMI	EIM_CS2	
CS3	No Muxing	EMI	EIM_CS3	
CS4	ALT0	EMI	EIM_CS4	
CS5	ALT0	EMI	EIM_CS5	
NF_CE0	ALT0	EMI	NANDF_CE0	
NFWE_B	ALT0	EMI	NANDF_WE_B	
NFRE_B	ALT0	EMI	NANDF_RE_B	
NFALE	ALT0	EMI	NANDF_ALE	
NFCLE	ALT0	EMI	NANDF_CLE	
NFWP_B	ALT0	EMI	NANDF_WP_B	
NFRB	ALT0	EMI	NANDF_RB	
CSI_D8	ALT0	IPU	CSI_D[8]	
CSI_D9	ALT0	IPU	CSI_D[9]	
CSI_D10	ALT0	IPU	CSI_D[10]	
CSI_D11	ALT0	IPU	CSI_D[11]	
CSI_D12	ALT0	IPU	CSI_D[12]	
CSI_D13	ALT0	IPU	CSI_D[13]	
CSI_D14	ALT0	IPU	CSI_D[14]	
CSI_D15	ALT0	IPU	CSI_D[15]	
CSI_MCLK	ALT5	GPIO1	GPIO[28]	
CSI_VSYNC	ALT0	IPU	CSI_VSYNC	
CSI_HSYNC	ALT0	IPU	CSI_HSYNC	
CSI_PIXCLK	ALT0	IPU	CSI_PIXCLK	
I2C1_CLK	ALT0	I2C1	SCL	
I2C1_DAT	ALT0	I2C1	SDA	
I2C2_CLK	ALT2	USB_TOP	USB2_PWR	
I2C2_DAT	ALT2	USB_TOP	USBH2_OC	
STXD4	ALT0	AUDMUX	AUD4_TXD	
SRXD4	ALT0	AUDMUX	AUD4_RXD	
SCK4	ALT0	AUDMUX	AUD4_TXC	
STXFS4	ALT0	AUDMUX	AUD4_TXFS	

STXD5	ALT5	GPIO1	GPIO[0]	
SRXD5	ALT2	CSPI2	MISO	
SCK5	ALT5	GPIO1	GPIO[2]	
STXFS5	ALT5	GPIO1	GPIO[3]	
SCKR	ALT0	ESAI	SCKR	N.C.
FSR	ALT0	ESAI	FSR	N.C.
HCKR	ALT5	GPIO1	GPIO[6]	
SCKT	ALT5	GPIO1	GPIO[7]	
FST	ALT5	GPIO1	GPIO[8]	
HCKT	ALT5	GPIO1	GPIO[9]	
TX5_RX0	ALT5	GPIO1	GPIO[10]	
TX4_RX1	ALT5	GPIO1	GPIO[11]	
TX3_RX2	ALT5	GPIO1	GPIO[12]	
TX2_RX3	ALT5	GPIO1	GPIO[13]	
TX1	ALT5	GPIO1	GPIO[14]	
TX0	ALT5	GPIO1	GPIO[15]	
CSPI1_MOSI	ALT5	GPIO1	GPIO[17]	
CSPI1_MISO	ALT5	GPIO1	GPIO[17]	
CSPI1_SS0	ALT5	GPIO1	GPIO[18]	
CSPI1_SS1	ALT5	GPIO1	GPIO[17]	
CSPI1_SCLK	ALT5	GPIO3	GPIO[4]	
CSPI1_SPI_RDY	ALT5	GPIO3	GPIO[5]	
RXD1	ALT0	UART1	RXD_MUX	
TXD1	ALT0	UART1	TXD_MUX	
RTS1	ALT0	UART1	RTS	
CTS1	ALT0	UART1	CTS	
RXD2	ALT5	GPIO3	GPIO[10]	
TXD2	ALT5	GPIO3	GPIO[11]	
RTS2	ALT2	CAN2	RXCAN	
CTS2	ALT2	CAN2	TXCAN	
USBPHY1_VBUS	ALT0	USBPHY_UTMI	USBPHY1_VBUS	
USBPHY1_DP	ALT0	USBPHY_UTMI	USBPHY1_DP	
USBPHY1_DM	ALT0	USBPHY_UTMI	USBPHY1_DM	
USBPHY1_UID	ALT0	USBPHY_UTMI	USBPHY1_UID	
USBPHY2_DM	ALT0	USBXCVR	USBPHY2_DM	
USBPHY2_DP	ALT0	USBXCVR	USBPHY2_DP	
USBOTG_PWR	ALT0	USB_TOP	USBOTG_PWR	
USBOTG_OC	ALT0	USB_TOP	USBOTG_OC	
LD0	ALT5	GPIO2	GPIO[0]	
LD1	ALT5	GPIO2	GPIO[1]	
LD2	ALT0	IPU	DISPB_DAT[2]	
LD3	ALT0	IPU	DISPB_DAT[3]	
LD4	ALT0	IPU	DISPB_DAT[4]	
LD5	ALT0	IPU	DISPB_DAT[5]	
LD6	ALT0	IPU	DISPB_DAT[6]	
LD7	ALT0	IPU	DISPB_DAT[7]	
LD8	ALT5	GPIO2	GPIO[8]	
LD9	ALT5	GPIO2	GPIO[9]	
LD10	ALT0	IPU	DISPB_DAT[10]	

LD11	ALT0	IPU	DISPB_DAT[11]	
LD12	ALT0	IPU	DISPB_DAT[12]	
LD13	ALT0	IPU	DISPB_DAT[13]	
LD14	ALT0	IPU	DISPB_DAT[14]	
LD15	ALT0	IPU	DISPB_DAT[15]	
LD16	ALT5	GPIO2	GPIO[16]	
LD17	ALT5	GPIO2	GPIO[17]	
LD18	ALT0	IPU	DISPB_DAT[18]	
LD19	ALT0	IPU	DISPB_DAT[19]	
LD20	ALT0	IPU	DISPB_DAT[20]	
LD21	ALT0	IPU	DISPB_DAT[21]	
LD22	ALT0	IPU	DISPB_DAT[22]	
LD23	ALT0	IPU	DISPB_DAT[23]	
D3_HSYNC	ALT0	IPU	DISPB_D3_HSYNC	
D3_FPSHIFT	ALT0	IPU	DISPB_D3_CLK	
D3_DRDY	ALT0	IPU	DISPB_D3_DRDY	
CONTRAST	ALT5	GPIO1	GPIO[1]	
D3_VSYNC	ALT0	IPU	DISPB_D3_VSYNC	
D3_REV	ALT5	GPIO1	GPIO[3]	
D3_CLS	ALT5	GPIO1	GPIO[4]	
D3_SPL	ALT5	GPIO1	GPIO[5]	
SD1_CMD	ALT0	ESDHC1	CMD	
SD1_CLK	ALT0	ESDHC1	CLK	
SD1_DATA0	ALT0	ESDHC1	DAT0	
SD1_DATA1	ALT0	ESDHC1	DAT1	
SD1_DATA2	ALT0	ESDHC1	DAT2	
SD1_DATA3	ALT0	ESDHC1	DAT3	
SD2_CMD	ALT1	I2C3	SCL	
SD2_CLK	ALT1	I2C3	SDA	
SD2_DATA0	ALT5	GPIO2	GPIO[2]	
SD2_DATA1	ALT5	GPIO2	GPIO[3]	
SD2_DATA2	ALT5	GPIO2	GPIO[4]	
SD2_DATA3	ALT5	GPIO2	GPIO[5]	
ATA_CS0	ALT5	GPIO2	GPIO[6]	
ATA_CS1	ALT4	CSPI2	SS0	
ATA_DIOR	ALT4	CSPI2	SS1	
ATA_DIOW	ALT4	CSPI2	MOSI	
ATA_DMACK	ALT5	GPIO2	GPIO[10]	
ATA_RESET_B	ALT5	GPIO2	GPIO[11]	
ATA_IORDY	ALT5	GPIO2	GPIO[12]	
ATA_DATA0	ALT5	GPIO2	GPIO[13]	
ATA_DATA1	ALT5	GPIO2	GPIO[14]	
ATA_DATA2	ALT5	GPIO2	GPIO[15]	
ATA_DATA3	ALT5	GPIO2	GPIO[16]	
ATA_DATA4	ALT5	GPIO2	GPIO[17]	
ATA_DATA5	ALT5	GPIO2	GPIO[18]	
ATA_DATA6	ALT1	CAN1	TXCAN	
ATA_DATA7	ALT1	CAN1	RXCAN	
ATA_DATA8	ALT1	UART3	RTS	

ATA_DATA9	ALT1	UART3	CTS	
ATA_DATA10	ALT1	UART3	RXD_MUX	
ATA_DATA11	ALT1	UART3	TXD_MUX	
ATA_DATA12	ALT5	GPIO2	GPIO[25]	
ATA_DATA13	ALT5	GPIO2	GPIO[26]	
ATA_DATA14	ALT5	GPIO2	GPIO[27]	
ATA_DATA15	ALT5	GPIO2	GPIO[28]	
ATA_INTRQ	ALT5	GPIO2	GPIO[29]	
ATA_BUFF_EN	ALT5	GPIO2	GPIO[30]	
ATA_DMARQ	ALT5	GPIO2	GPIO[31]	
ATA_DA0	ALT5	GPIO3	GPIO[0]	
ATA_DA1	ALT5	GPIO3	GPIO[1]	
ATA_DA2	ALT5	GPIO3	GPIO[2]	
TTM_PAD	ALT0	THERMAL	TTM_PAD	N.C.
MLB_CLK	ALT0	MLB	MLB_CLK	
MLB_DAT	ALT0	MLB	MLB_DAT	
MLB_SIG	ALT0	MLB	MLB_SIG	
FEC_TX_CLK	ALT0	FEC	TX_CLK	
FEC_RX_CLK	ALT0	FEC	RX_CLK	
FEC_RX_DV	ALT0	FEC	RX_DV	
FEC_COL	ALT0	FEC	COL	
FEC_RDATA0	ALT0	FEC	RDATA[0]	
FEC_TDATA0	ALT0	FEC	TDATA[0]	
FEC_TX_EN	ALT0	FEC	TX_EN	
FEC_MDC	ALT0	FEC	MDC	
FEC_MDIO	ALT0	FEC	MDIO	
FEC_TX_ERR	ALT0	FEC	TX_ERR	
FEC_RX_ERR	ALT0	FEC	RX_ERR	
FEC_CRS	ALT0	FEC	CRS	
FEC_RDATA1	ALT0	FEC	RDATA[1]	
FEC_TDATA1	ALT0	FEC	TDATA[1]	
FEC_RDATA2	ALT0	FEC	RDATA[2]	
FEC_TDATA2	ALT0	FEC	TDATA[2]	
FEC_RDATA3	ALT0	FEC	RDATA[3]	
FEC_TDATA3	ALT0	FEC	TDATA[3]	
EXT_ARMCLK	ALT0	CCM	EXT_ARMCLK	
TEST_MODE	ALT0	FEC	TEST_MODE	

Table 42 IMX35 I/O multiplexing (pin-out)

4.1.2 Daisy Chain Bit

Address	Function	Value	PIN	
0x07C8	CAN1_RX	0x10	ATA_DATA7	
0x07CC	CAN2_RX	0x01	RTS2	
0x07D0	CCM_32K	0x00	CAPTURE	
0x07D4	PMIC_RDY	0x00	GPIO1_0	
0x07E0	CSPI2_CLK	0x10	ATA_DATA3	
0x07E8	CSPI2_MISO	0x00	SRXD5	
0x07EC	CSPI2_MOSI	0x10	ATA_DIOW	
0x07F0	CSPI2_SS0	0x01	ATA_CS1	
0x07F4	CSPI2_SS1	0x01	ATA_DIOR	
0x0800	EMI_DTAC_B	0x01	TX0	
0x082C	GPIO1_0	0x01	STXD5	
0x0830	GPIO1_10	0x00	TX5_RX0	
0x0834	GPIO1_11	0x00	TX4_RX1	
0x0838	GPIO1_1	0x10	CONTRAST	
0x083C	GPIO1_20	0x01	CSI_D8	
0x0840	GPIO1_21	0x01	CSI_D9	
0x0844	GPIO1_22	0x01	CSI_D810	
0x0848	GPIO1_2	0x00	SCK5	
0x084C	GPIO1_3	0x01	D3_REV	
0x0850	GPIO1_4	0x10	D3_CLS	
0x0854	GPIO1_5	0x10	D3_SPL	
0x0858	GPIO1_6	0x01	HCKR	
0x085C	GPIO1_7	0x01	HCKT	
0x0860	GPIO1_8	0x01	FST	
0x0864	GPIO1_9	0x00	HCKT	
0x0868	GPIO2_0	0x01	LD0	
0x086C	GPIO2_10	0x10	ATA_DMACK	
0x0870	GPIO2_11	0x10	ATA_RESET	
0x0874	GPIO2_12	0x01	ATA_IORDY	
0x0878	GPIO2_13	0x01	ATA_DATA0	
0x087C	GPIO2_14	0x01	ATA_DATA1	
0x0880	GPIO2_15	0x01	ATA_DATA2	
0x0884	GPIO2_16	0x01	LD16	
0x0888	GPIO2_17	0x00	LD17	
0x088C	GPIO2_18	0x01	ATA_DATA5	
0x0890	GPIO2_19	0x01	ATA_DATA6	
0x0890	GPIO2_1	0x00	LD1	
0x0898	GPIO2_20	0x01	ATA_DATA7	
0x08A0	GPIO2_21	0x01	ATA_DATA8	
0x08A1	GPIO2_22	0x01	ATA_DATA9	
0x08A2	GPIO2_23	0x01	ATA_DATA10	
0x08AC	GPIO2_25	0x01	ATA_DATA12	
0x08B0	GPIO2_26	0x01	ATA_DATA13	
0x08B4	GPIO2_27	0x01	ATA_DATA14	

0x08B8	GPIO2_28	0x01	ATA_DATA15	
0x08BC	GPIO2_29	0x01	ATA_INTRQ	
0x08C0	GPIO2_2	0x01	SD2_ATA0	
0x08C4	GPIO2_30	0x01	ATA_BUFF_EN	
0x08C8	GPIO2_31	0x01	ATA_DMARQ	
0x08CC	GPIO2_3	0x01	SD2_DATA1	
0x08D0	GPIO2_4	0x01	SD2_DATA4	
0x08D4	GPIO2_5	0x01	SD2_DATA3	
0x08D8	GPIO2_6	0x00	ATA_CS0	
0x08E0	GPIO2_8	0x00	LD8	
0x08E4	GPIO2_9	0x00	LD9	
0x08E8	GPIO3_0	0x00	GPIO3_0	
0x08EC	GPIO3_10	0x00	RXD2	
0x08F0	GPIO3_11	0x00	TXD2	
0x0904	GPIO3_4	0x00	CSPI1_SCLK	
0x0908	GPIO3_5	0x00	CSPI1_SPI_RDY	
0x091C	I2C3_SCL	0x10	SD2_CMD	
0x0920	I2C3_SDA	0x10	SD2_CLK	
0x099C	UART3_RTS	0x01	ATA_DATA8	
0x09A0	UART3_RXD	0x10	ATA_DATA10	
0x09F4	USBH2_OC	0x00	I2C_DATA	

Table 43 Daisy Chain Register

End of Document