AT91SAM9G20 Microcontroller Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding the Atmel® ARM® Thumb®-based AT91SAM9G20 microcontroller.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM9G20. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM9G20 microcontroller on Atmel's Web site.

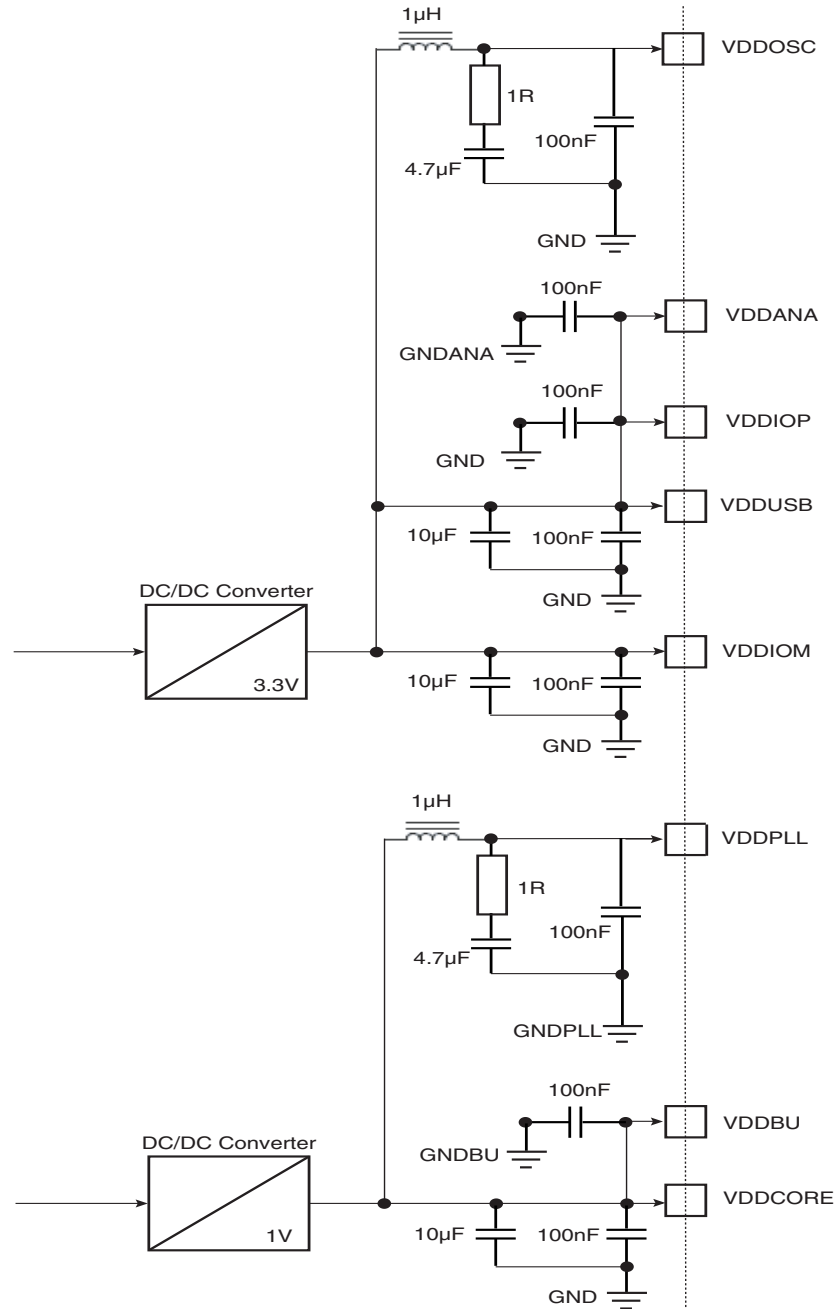Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM9G20 Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	AT91SAM9G20-EK Evaluation Board User Guide
Using SDRAM on AT91SAM9 Microcontrollers	Using SDRAM on AT91SAM9 Microcontrollers
NAND Flash Support in AT91SAM9 Microcontrollers	NAND Flash Support in AT91SAM9 Microcontrollers

3. Schematic Check List

CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the Electrical Characteristics section in the datasheet to guarantee reliable operation of the device.
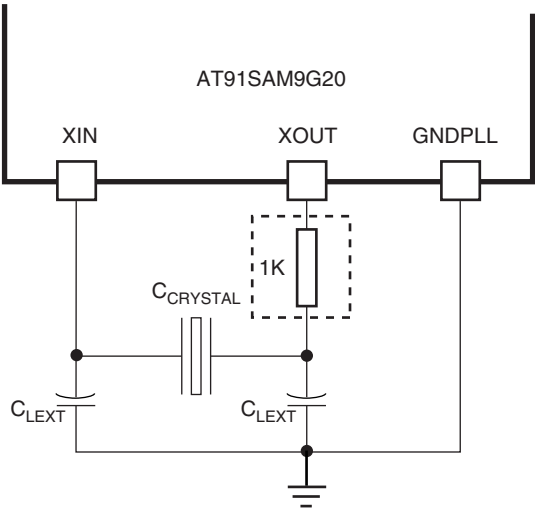
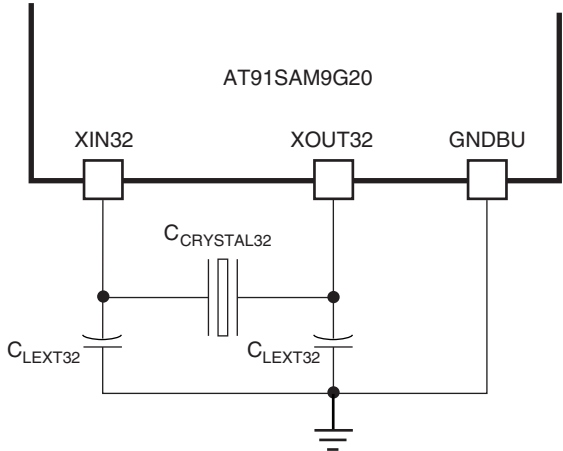**1V and 3.3V Dual Power Supply with 3.3V Powered Memories Schematic Example**

1V and 3.3V Dual Power Supply Schematic Example:[1]
3.3V external memories (VDDIOM) - ADC (VDDANA) is used

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	0.9V to 1.1V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	0.9V to 1.1V Decoupling/filtering RLC circuit[1]	Powers the PLL cells. The VDDOSC power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDOSC power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 10mV.
	VDDBU	0.9V to 1.1V Decoupling capacitor (100 nF)[1][2]	Powers the Backup I/O lines (Slow Clock Oscillator and a part of the System Controller).
	VDDOSC	1.65V to 3.6V Decoupling/Filtering RLC circuit[1]	Powers the oscillator. The VDDOSC power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDOSC power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 30mV.
	VDDIOM[3]	1.65V to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers External Bus Interface I/O lines. Dual voltage range supported. The voltage ranges are selected by programming the VDDIOMSEL bit in the EBI_CSA register. At power-up, the selected voltage is 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDUSB[3]	3V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers USB transceivers. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP[3]	1.65V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers all peripherals. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDANA	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2] Application dependent	Powers the Analog to Digital Converter (ADC) and some PIOC I/O lines.
	GND	Ground	GND pins are common to VDDCORE, VDDIOM, VDDIOP and VDDUSB pins. GND pins should be connected as shortly as possible to the system ground plane.

Application Note

☑	Signal Name	Recommended Pin Connection	Description
	GNDBU	Backup Ground	GNDBU pin is provided for VDDBU pin. GNDBU pin should be connected as shortly as possible to the system ground plane.
	GNDPLL	PLL and Main Oscillator Ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.
	GNDANA	Analog Ground	GNDANA pin is provided for VDDANA pin. GNDANA pin should be connected as shortly as possible to the system ground plane.

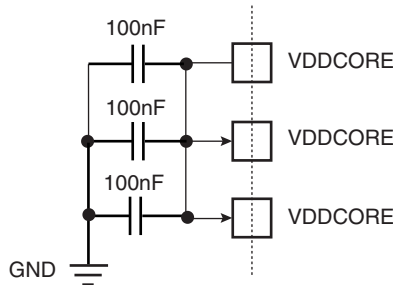| ☑	Signal Name	Recommended Pin Connection	Description
	Clock, Oscillator and PLL		
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependent) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Crystal Load Capacitance to check ($C_{CRYSTAL}$). AT91SAM9G20 XIN XOUT GNDPLL 1K $C_{CRYSTAL}$ C_{LEXT} C_{LEXT} Example: for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 17.5 pF, external capacitors are required: C_{LEXT} = 12 pF. Refer to the electrical specifications of the AT91SAM9G20 datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected	3.3V Square wave signal External Clock Source up to 50 MHz Duty Cycle: 40 to 60% Refer to the electrical specifications of the AT91SAM9G20 datasheet.

☑	Signal Name	Recommended Pin Connection	Description
	XIN32 XOUT32 Slow Clock Oscillator	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Crystal Load Capacitance to check ($C_{CRYSTAL32}$). Example: for an 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32}$= 12.5 pF, external capacitors are required: C_{LEXT32} = 17pF. Refer to the electrical specifications of the AT91SAM9G20 datasheet.
	OSCSEL	Application dependent. Please refer to the I/O line considerations and errata section of the AT91SAM9G20 datasheet.	Slow Clock Oscillator Selection. Must be tied to V_{VDDBU} to select the external 32,768 Hz crystal. Must be tied to GNDBU to select the on-chip RC oscillator.

☑	Signal Name	Recommended Pin Connection	Description
	ICE and JTAG[4]		
	TCK	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDO	Floating	Output driven at up to V_{VDDIOP}
	RTCK	Floating	Output driven at up to V_{VDDIOP}
	NTRST	Can be left unconnected. **It is strongly recommended to tie this pin to V_{DDIOP0} in harsh[5] environments.**	Internal pull-up resistor to V_{VDDIOP} (100 kOhm).
	JTAGSEL	**In harsh environments,[5] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).**	Internal pull-down resistor to GNDBU (15 kOhm). Must be tied to V_{VDDBU} to enter JTAG Boundary Scan.
	Reset/Test		
	NRST	Application dependent. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIOP} (100 kOhm) is available for User Reset and External Reset control.
	TST	**In harsh environments,[5] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).**	Internal pull-down resistor to GNDBU (15 kOhm).
	BMS	Application dependent.	Must be tied to V_{VDDIOP} to boot on Embedded ROM. Must be tied to GND to boot on external memory (EBI Chip Select 0).
	Shutdown/Wakeup Logic		
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies. An external pull-up to VDDBU is needed and its value is to be higher than 1 MOhm. The resistor value is calculated according to the regulator enable implementation and the SHDN level.	The SHDN pin is a tri state output. No internal pull-up resistor. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).
	WKUP	0V to V_{VDDBU}	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).

☑	Signal Name	Recommended Pin Connection	Description
	PIO		
	PAx PBx PCx	Application dependent	All PIOs are pulled-up inputs at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals: PC4 (A23), PC5 (A24) and PC10 (A25). To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
	ADC		
	ADVREF	2.8V to V_{VDDANA} Decoupling/Filtering capacitors. Application dependent	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used: connect ADVREF to GNDANA.
	EBI		
	D0-D15 (D16-D31)	Application dependent	Data Bus (D0 to D31) Data Bus lines D0 to D15 are pulled-up inputs to V_{VDDIOM} at reset. Note: Data Bus lines D16 to D31 are multiplexed with the PIOC controller. Their I/O line reset state is input with pull-up enabled too.
	A0-A22 (A23-A25)	Application dependent	Address Bus (A0 to A25) All Address Lines are driven to '0' at reset. Note: A23 (PC4), A24 (PC5) and A25 (PC10) are enabled by default at reset through the PIO controllers.
	SMC - SDRAM Controller - CompactFlash Support - NAND Flash Support		
	See "External Bus Interface (EBI) Hardware Interface" on page 12.		

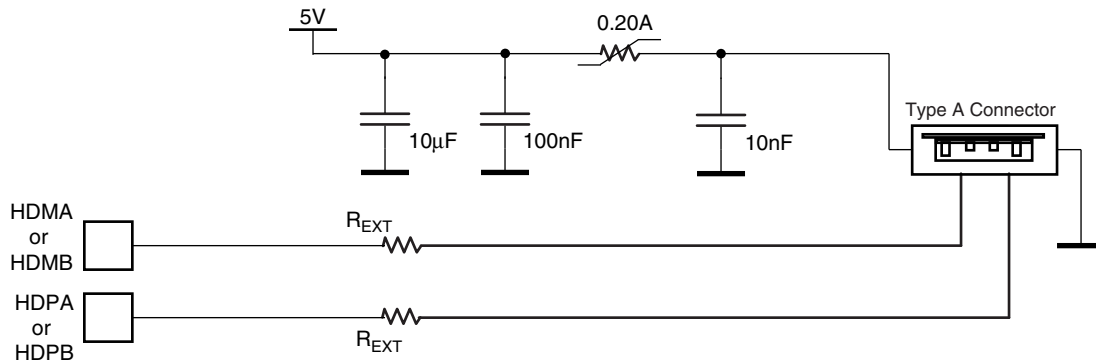| ☑	Signal Name	Recommended Pin Connection	Description
	USB Host (UHP)		
	HDPA HDPB	Application dependent[6]	Internal pull-down resistors. Refer to the electrical specifications of the AT91SAM9G20 datasheet.
	HDMA HDMB	Application dependent[6]	Internal pull-down resistors. Refer to the electrical specifications of the AT91SAM9G20 datasheet.
	USB Device (UDP)		
	DDP	Application dependent[7]	Integrated programmable pull-up resistor (UDP_TXVC) Integrated pull-down resistor to prevent over consumption when the host is disconnected. To reduce power consumption, if USB Device is not used, DDP must be left unconnected.
	DDM	Application dependent[7]	Integrated pull-down resistor to prevent over consumption when the host is disconnected. To reduce power consumption, if USB Device is not used, DDM must be left unconnected.

Notes: 1. These values are given only as a typical example.

2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.

3. The power supplies VDDIOM and VDDIOP and VDDUSB power the device differently when interfacing with memories or with peripherals.

4. It is recommended to establish accessibility to a JTAG connector for debug in any case.

5. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
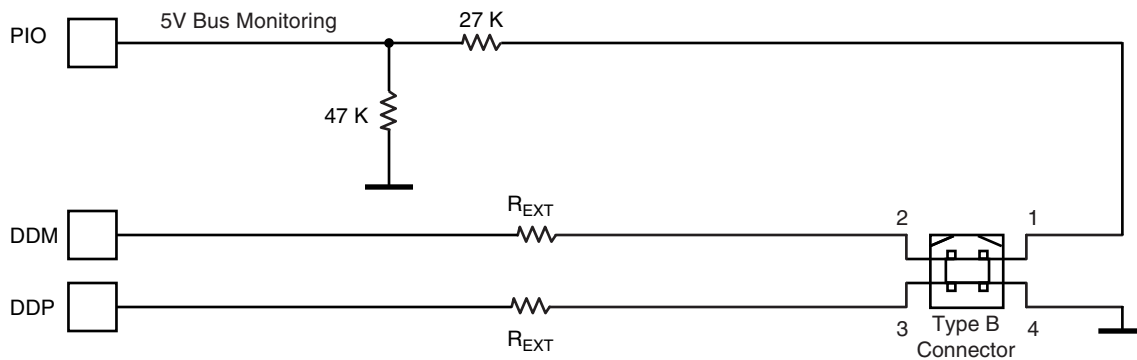
Application Note

6. Example of USB Host connection:
A termination serial resistor (R_{EXT}) must be connected to HDPA/HDPB and HDMA/HDMB. A recommended resistor value is defined in the electrical specifications of the AT91SAM9G20 datasheet.

7. Example of USB Device connection:
As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up.
Internal pull-downs on DDP and DDM are embedded to prevent over consumption when the host is disconnected.
A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM9G20 datasheet.

4. External Bus Interface (EBI) Hardware Interface

Table 4-1 and Table 4-2 detail the connections to be applied between the EBI pins and the external devices for each Memory Controller:

Table 4-1. EBI Pins and External Static Devices Connections

Signals: EBI_	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	SMC					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB[3]	BE0[5]
A1/NWR2/NBS2	A1	A0	A0	WE[2]	NLB[4]	BE2[5]
A2 - A22	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4/CFCS0	CS	CS	CS	CS	CS	CS
NCS5/CFCS1	CS	CS	CS	CS	CS	CS
NRD/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE[1]	WE	WE[2]	WE	WE
NWR1/NBS1	–	WE[1]	NUB	WE[2]	NUB[3]	BE1[5]
NWR3/NBS3	–	–	–	WE[2]	NUB[4]	BE3[5]

Notes: 1. NWR1 enables upper byte writes. NWR0 enables lower byte writes.

2. NWRx enables corresponding byte x writes. (x = 0, 1, 2 or 3)

3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.

4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.

5. BEx: Byte x Enable (x = 0,1,2 or 3)

Table 4-2. EBI Pins and External Device Connections

Signals: EBI_	Pins of the Interfaced Device			
	SDRAM[3]	CompactFlash (EBI only)	CompactFlash True IDE Mode (EBI only)	NAND Flash[4]
Controller	**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0-I/O7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8-I/O15[5]
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21	–	–	–	ALE
A22	–	REG	REG	CLE
A23 - A24	–	–	–	–
A25	–	CFRNW[1]	CFRNW[1]	–
NCS0	–	–	–	–
NCS1/SDCS	CS	–	–	–
NCS2	–	–	–	–
NCS3/NANDCS	–	–	–	CE[6]
NCS4/CFCS0	–	CFCS0[1]	CFCS0[1]	–
NCS5/CFCS1	–	CFCS1[1]	CFCS1[1]	–
NANDOE	–	–	–	RE
NANDWE	–	–	–	WE
NRD/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFCE1	–	CE1	CS0	–
CFCE2	–	CE2	CS1	–
SDCK	CLK	–	–	–

Table 4-2. EBI Pins and External Device Connections (Continued)

Signals: EBI_	Pins of the Interfaced Device			
	SDRAM[3]	CompactFlash (EBI only)	CompactFlash True IDE Mode (EBI only)	NAND Flash[4]
Controller	SDRAMC	SMC		
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx[2]	–	CD1 or CD2	CD1 or CD2	–
Pxx[2]	–	–	–	CE[6]
Pxx[2]	–	–	–	RDY

Notes: 1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.

2. Any PIO line.

3. For SDRAM connection examples, See Using SDRAM on AT91SAM9 Microcontrollers application note.

4. For NAND Flash connection examples, See NAND Flash Support in AT91SAM9 Microcontrollers application note.

5. I/O8 - I/O15 bits used only for 16-bit NAND Flash.

6. CE connection depends on the NAND Flash.
   For standard NAND Flash devices, it must be connected to any free PIO line.
   For "CE don't care" NAND Flash devices, it can be connected either to NCS3/NANDCS or to any free PIO line.

5. AT91SAM Boot Program Hardware Constraints

See the AT91SAM Boot Program section of the AT91SAM9G20 datasheet for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals and Input Frequencies

5.1.1 On-chip RC Selected (OSCSEL = 0)

If the Internal RC Oscillator is used (OSCSEL = 0) and the Main Oscillator is active:

Table 5-1. Supported Crystals (MHz)

	3.0	8.0	18.432	Other Crystal
Boot on DBGU	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	No

Note: Any other crystal can be used but it prevents using the USB for SAM-BA Boot.

If the Internal RC Oscillator is used (OSCSEL = 0) and the Main Oscillator is bypassed:

Table 5-2. Supported Input Frequencies (MHz)

	3.0	8.0	20.0	50.0	Other Frequency
Boot on DBGU	Yes	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	Yes	No

Note: Any other input frequency can be used but it prevents using the USB for SAM-BA Boot.

For the current AT91SAM9G20 revisions (A and B), booting from the Internal RC Oscillator (OSCSEL = 0) prevents from using SAM-BA Boot through the USB device interface. More details in the errata section of the product datasheet.

5.1.2 External 32,768 Hz Crystal Selected (OSCSEL = 1)

If an external 32,768 Hz Oscillator is used (OSCSEL = 1) and the Main Oscillator is active:

Table 5-3. Supported Crystals (MHz)

3.0	3.6864	3.84	4	4.9152
5.24288	6.0	6.144	6.4	6.5536
7.3728	8.0	9.8304	10.0	11.05920
12.0	12.288	14.31818	14.7456	16.0
16.367667	17.734470	18.432	20.0	-

Note: Booting either on USB or on DBGU is possible with any of these crystals.

If an external 32,768 Hz Oscillator is used (OSCSEL = 1) and the Main Oscillator is bypassed:

Table 5-4. Supported Input Frequencies (MHz)

3.0	3.6864	3.84	4	4.9152
5.24288	6.0	6.144	6.4	6.5536
7.3728	8.0	9.8304	10.0	11.05920
12.0	12.288	14.31818	14.7456	16.0
16.367667	17.734470	18.432	20.0	24.0
24.576	25.0	28.224	32.0	33.0
40.0	48.0	50.0	-	-

Note: Booting either on USB or on DBGU is possible with any of these input frequencies.

5.2   SAM-BA® Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-5. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PB14
DBGU	DTXD	PB15

5.3   DataFlash® Boot

The DataFlash Boot program searches for a valid application in the SPI DataFlash memory.

The DataFlash must be connected to NPCS0 or NPCS1 of the SPI0.

Table 5-6. Pins Driven during DataFlash Boot Program Execution

Peripheral	Pin	PIO Line
SPI0	MOSI	PA1
SPI0	MISO	PA0
SPI0	SPCK	PA2
SPI0	NPCS0	PA3
SPI0	NPCS1	PC11

5.4   NAND Flash Boot

The NAND Flash Boot program searches for a valid application in the NAND Flash memory.

Table 5-7. Pins Driven during NAND Flash Boot Program Execution

Peripheral	Pin	PIO Line
PIOC	PIOC14 (for NAND Chip Select)	PC14
PIOC	PIOC13 (for NAND Ready Busy)	PC13
Address Bus	NAND CLE	A22
Address Bus	NAND ALE	A21

16   Application Note

5.5   EEPROM Boot

The EEPROM Boot program searches for a valid application in the EEPROM memory connected to the TWI.

Table 5-8.   Pins driven during EEPROM Boot Program Execution

Peripheral	Pin	PIO Line
TWI	TWCK	PA24
TWI	TWD	PA23

5.6   SD Card Boot

The SD Card Boot program searches for a valid application in the SD Card memory.

Table 5-9.   Pins Driven during SD Card Boot Program Execution

Peripheral	Pin	PIO Line
MCI1	MCCK	PA8
MCI1	MCCDA	PA7
MCI1	MCDA0	PA6
MCI1	MCDA1	PA9
MCI1	MCDA2	PA10
MCI1	MCDA3	PA11

SD Card Boot support depends on component version. Refer to the AT91SAM9G20 datasheet.

Revision History

Doc. Rev	Comments	Change Request Ref.
6431B	Remove PLLRCA pin from Section 3. "Schematic Check List"	rfo
	1V to 3.3V change in Section 3. "Schematic Check List"	5942
	Add Section 5.5 "EEPROM Boot" and Section 5.6 "SD Card Boot" on page 17	6144
	Edit SHDN in Section 3. "Schematic Check List"	6028
	Edit the hyperlink to AT91SAM9G20 product in Section 2. "Associated Documentation" on page 2	5912
	Add 2 sentences at the end of Section 5.1.1 "On-chip RC Selected (OSCSEL = 0)" on page 15	6143
	Add a Caution paragraph on top of Section 3. "Schematic Check List"	6124
6431A	First Issue	

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