User Manual: S-band Transmitter (STX)

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Document Control

Rev.	Date	Section	Description of Change	Reason for Change
1.0	26 July 2012	All	First Release	
1.1	14 September 2012	Hardware and data interfacing	Additional information	
1.2	28 January 2013	Data interfacing	Additional information	Buffer size increased in software version 1.2
1.3	28 March 2013	Data interfacing and test procedures	Additional information	Software version 1.3
1.4	16 September 2013	All	Additional information	Hardware update
1.5	27 November 2013	All	Additional information	Hardware update
1.6	28 February 2014	All	Additional information	Software update

Revision Control

Product	Part Number	Revisions Covered	Notes
S-band Transmitter	CPUT-STX-01	1.7	

Related Documents

No.	Document Name	Document Reference
CPUT-ICD-STX-01	STX Interface Control Document	
CPUT-TR-STX-xx	STX Test Results Document	

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Nomenclature

Abbreviations

ADC	Analogue-to-Digital Converter
BCD	Binary-Coded Decimal
CSK	CubeSat Kit
FIFO	First In First Out
FPGA	Field Programmable Gate Array
MC	Major Component
OBC	On Board Computer
PA	Power Amplifier
SPI	Serial Peripheral Interface
STX	S-band Transmitter
TBD	To Be Determined

1 Introduction

This document describes the operation, handling and storage of the first generation of the S-band Transmitter (STX). The STX is an integrated RF data transmitter module supporting a maximum transmission bit rate of 2 Mbps (1 Mbps user data + 1 Mbps encoding). An overview of the STX is shown in Figure 1.
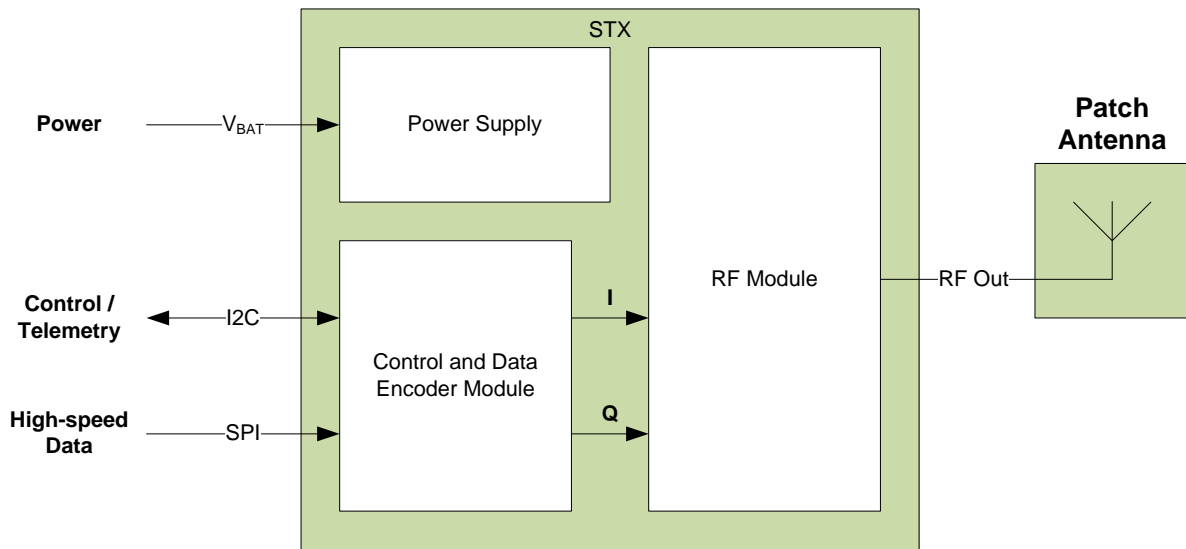
Figure 1: System block diagram

2 Overview

The STX is a compact S-band Transmitter designed for CubeSat nanosatellite missions. It is compatible with the CubeSat nanosatellite standard, with a CubeSat Kit PC/104 form factor. The STX implements QPSK or OQPSK modulation with Intelsat IESS-308 based encoding which ensures compatibility with low cost commercial ground segment receivers.

The STX frequency of operation is selectable from 2.4–2.45 GHz (amateur band).The frequency of operation is user selectable within the band. The carrier frequency is adjustable in 500 kHz steps. Output power is adjustable in 3 dB steps from 21 dBm to 30 dBm. The STX is configured via an I^2C data bus and high speed payload data is sent via SPI. Data transmission rates of up to 2 Mbps are supported with $1/2$, $1/4$ and $1/8$ rate modes. The STX is powered from the battery bus, yet may be powered down externally via an enable line from the PC/104 header.

2.1　Encoding and modulation overview

- QPSK and OQPSK modulation schemes.

- Open Network Encoding scheme based on IntelSAT IESS-308 specifications.

- V.35 IntelSAT scrambler.

- Differential encoding.

- Half-rate convolutional encoding (K=7).

- Pulse shaping filter (0.35 roll-off factor).

- 2 Mbps data rate with full, $1/2$, $1/4$, and $1/8$ data rate modes.

    - 1 Mbps maximum user data as half-rate convolutional encoding is implemented.

3   Absolute maximum ratings

Table 1: Absolute maximum ratings

Parameter	Notes	Value	Unit
Supply voltage	Battery bus	14	V
STX_EN	STX enable	–0.3 to 5	V
Operating temperature		–25 to +61	°C
Storage temperature		–40 to +85	°C

4   Electrical characteristics

Table 2: Electrical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Power					
Input voltage	Battery bus	6	7.2	12	V
Input current	Vbatt = 7.2 V				
	$1/8$ W RF power	–	0.31	–	A
	$1/4$ W RF power	–	0.42	–	A
	$1/2$ W RF power	–	0.55	–	A
	1 W RF power	–	0.83	–	A
Idle power	PA off	–	0.6	0.7	W
RF characteristics					
Frequency range	Amateur band	2400	–	2450	MHz
Output power	3 dBm increments	21	–	30	dBm
Output return loss		–	7	–	dB
Frequency stability		–	±2.5	–	ppm
Channel spacing		–	500	–	kHz
I^{2}C					
Transmission speed		50	400	500	kbps
Node address		–	0x26	–	hex
Address scheme		–	7	–	bit
SPI					
Transmission speed		–	4	8	Mbps

5   Mechanical characteristics

5.1   Specifications

Table 3: Mechanical specifications

Parameter	Notes	Min	Typ	Max	Unit
Physical		L	W	H	
Dimensions		96	90.2	17	mm
Weight		90	95	100	g
Input ports					
Header connector		–	PC/104	–	–
Output ports					
RF connector		–	SMA	–	–

5.2   Materials

Table 4: List of materials

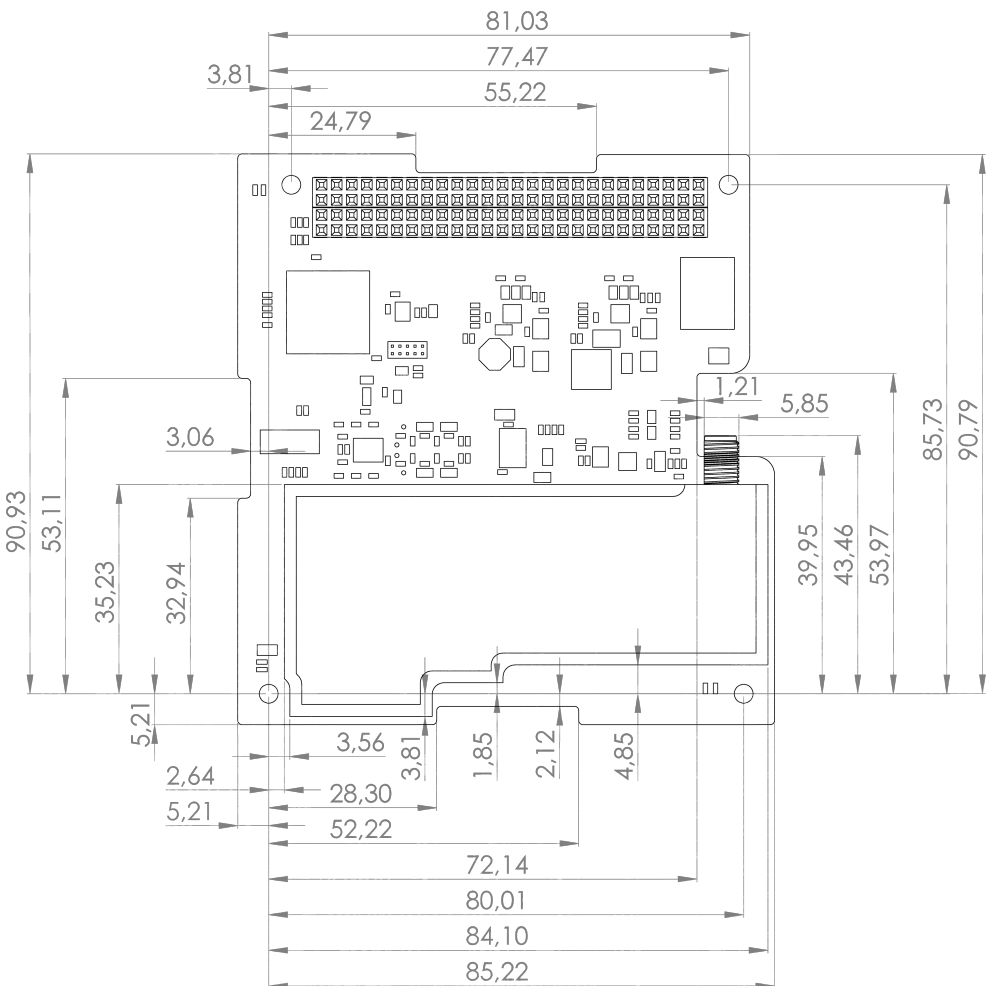| Materials	Manufacturer	%TML	%CVCM	%WVR	Application	Note
Scotch-Weld 2216 Epoxy B/A	3M	0.97	0.02	0.32	Adhesive Fixing	
PCB Material	FR4	0.62	0	0.1	PCB Board	NASA Worst Case
Solder Resist	CARAPACE EMP110	0.95	0.02	0.31	Solder Mask	
Solder	Sn63					

5.3   Mechanical configuration
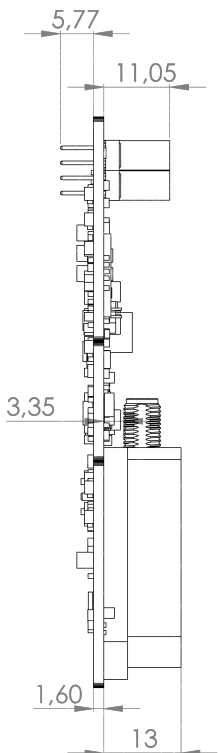
Figure 2: Mechanical diagram (shown in mm) [ESQ-126-13-G-D header shown]

6   Handling and storage

Specific guidelines must be adhered to when handling, transporting and storing the transmitter. Failure to follow these guidelines may result in damage to the unit or degradation in performance.

Although the unit has been tested at full RF output power across the temperature range, it is advisable to fit an appropriate heat strap between the power amplifier and the chassis metal. The heat strap may be attached to the bottom side of the unit where mounting holes have been provided around the power amplifier. A heat strap may be cut from 1 mm thick copper or brass plate and fastened to the unit with M1.6 screws, washers and nuts.

6.1   Power amplifier protection

Caution must be taken to ensure that an appropriate 50 Ω RF load (at least 2 W rating) is presented to the RF output of the STX while the power amplifier is enabled. Failure to do so could result in permanent damage to the power amplifier unit.

6.2   Antenna impedance

Physically touching an antenna or bringing reflective obstacles in close proximity to an antenna can affect the antenna's impedance and reflection coefficient at the frequencies at which it was designed, thereby causing excessive RF power to be reflected which may cause permanent damage to the transmitter. Care should be taken to keep the area around the antenna free of room reflections.

6.3   ESD protection

The STX incorporates static sensitive devices and care should be taken when handling the module. Under no circumstances should the transceiver be handled without appropriate electrostatic protection. The STX should only be handled in a static dissipative environment.

6.4   General handling

The transmitter has been designed to withstand satellite flight conditions but care must still be taken when handling the hardware.

- Do not drop the hardware.

- All work must be done in a clean room environment.

- Keep all metal objects away from the module to prevent accidental short circuiting.

- Gloves should be worn when handling flight hardware.

- Anti-static procedures should be followed at all times.

6.5 Storage and shipping

The STX is shipped in anti-static packaging enclosed in a hard protective case. When storing the STX it should be placed in an anti-static package and preferably stored in the hard protective case.

7 System operation

The operation of the STX as well as the initialisation process is described in this section.

7.1 Method of operation

- The STX will be configured through commands sent via I^{2}C. The commands set parameters such as output power, carrier frequency, and transmission data rate. Telemetry such as buffer underruns and overruns as well as data read from the ADC channels are made available. A detailed description of all I^{2}C commands is provided in Section 9.2.

- After configuration, the STX may be placed into data mode where real-time data from the SPI bus is encoded, modulated and transmitted.

7.2 Telemetry data
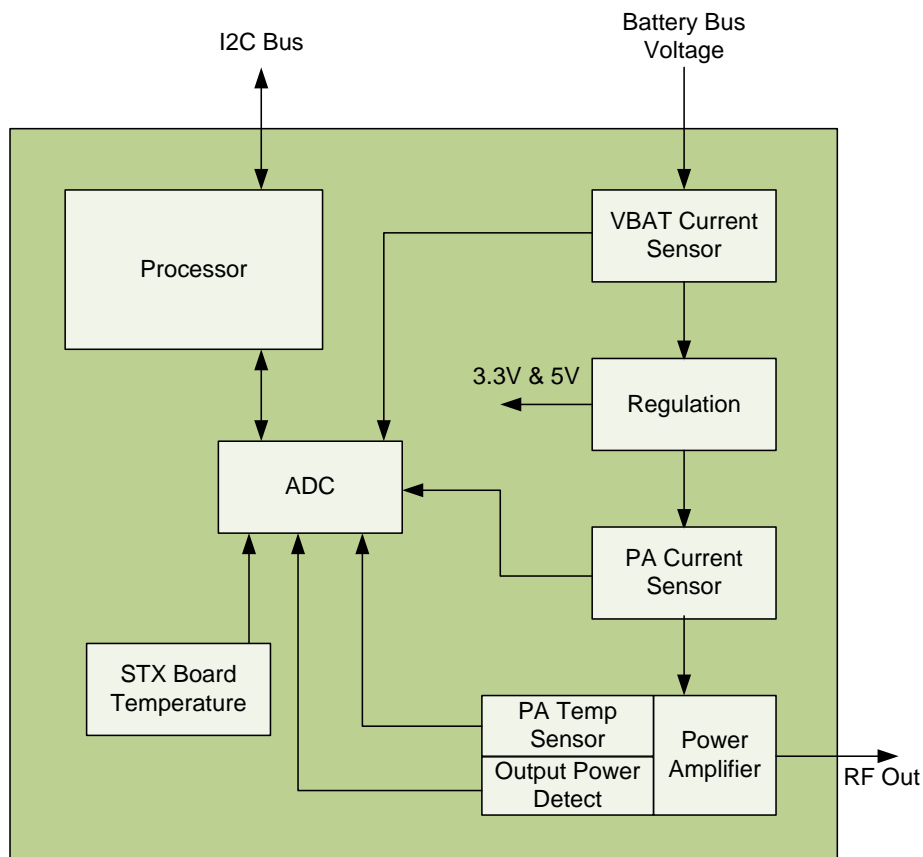
Figure 3: Telemetry data from STX

The following telemetry data may be read from the STX via I^{2}C:

- Current drawn from the battery bus.

- Current drawn by the driver amplifier and power amplifier.

- Battery bus voltage level.

- Power amplifier voltage level.

- RF output power level.

- Power amplifier temperature.

- STX top side board temperature.

- STX bottom side board temperature.

The various analogue sensors used to measure these parameters are connected to an ADC. The ADC values are read by the onboard processor, and are made available via I^{2}C.

A detailed list of the I^{2}C registers is provided in Section 9.2.

8 Hardware interfacing

8.1 CSK header connections
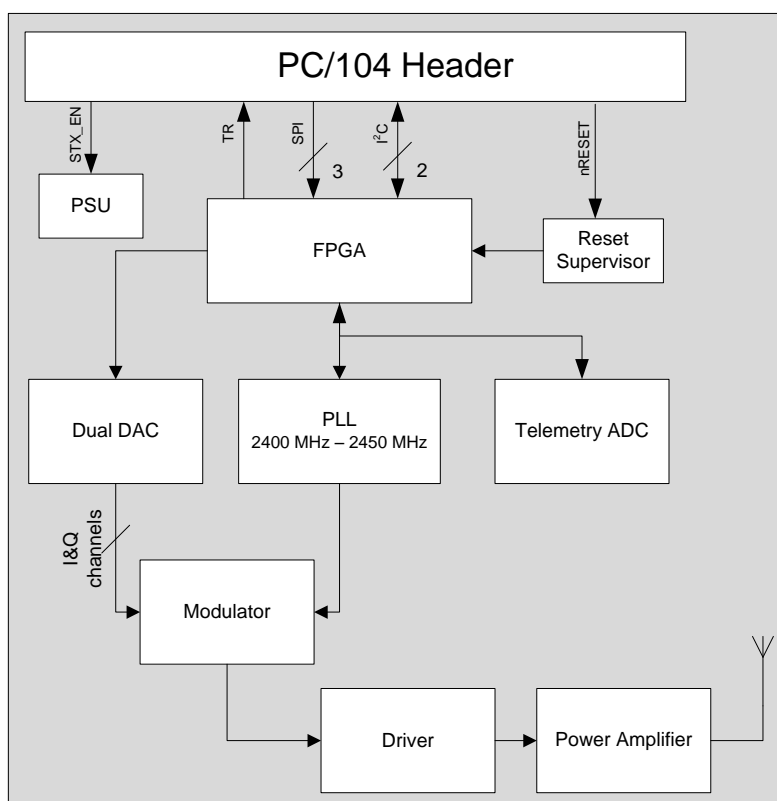
Figure 4: Block diagram of the CSK header connections and system layout

Figure 5: PC/104 header pinouts

Table 5: PC/104 header pinout definitions

Pin #	Pin name	I/O type	Description	Optional
H1-41	SDA	Bidirectional	I^{2}C serial data	Yes*
H1-43	SCL	Input	I^{2}C serial clock	Yes*
H1-23	SDA_ALT	Bidirectional	Alternate I^{2}C data	Yes*
H1-21	SCL_ALT	Input	Alternate I^{2}C clock	Yes*
H1-13	TR	Output	Transmitter ready for data	Yes
H1-09	COMM_SCLK	Input	SPI clock	Yes
H1-11	COMM_MOSI	Input	SPI data	Yes
H1-12	COMM_CS	Input	SPI chip select	Yes
H1-15	nFPGA_RESET	Input	FPGA reset (active low)	Yes
H1-10	STX_EN	Input	STX enable (active high)	Yes
H2-45	VBATT_BUS	Power	Battery bus supply	No
H2-46	VBATT_BUS	Power	Battery bus supply	No
H2-29	GND	Power	Power ground	No
H2-30	GND	Power	Power ground	No
H2-32	GND	Power	Power ground	No

*Either the I^{2}C or alternative I^{2}C option must be chosen, not both.

8.2 RF connector

An SMA connector is used to connect the RF output of the STX to an antenna. Please ensure that the correct connector is used and that it is correctly tightened and torqued. When not transmitting into an antenna, ensure that an appropriate 50 Ω RF load is connected to prevent damaging the transmitter. Refer to the mechanical dimensions of the STX shown in Figure 2 for the connector placement.

8.3 STX enable

The STX enable line allows the board to be powered down when not in use. This is a hard line connected to the PC/104 header and its functionality needs to be configured at manufacture. The STX may be configured to always be enabled if so desired, negating the use of the enable line. The enable line includes a pull-up. Pull below 1.2 V to disable the STX. Float to enable or apply LVCMOS logic 1.8 V - 3.3 V to enable the board.

9 Data interfacing

9.1 Modes of operation

The STX has three basic modes of operation:

- Configuration mode.

- Synchronisation mode.

- Data mode.

9.1.1 Configuration mode

At power-up, the S-band transmitter is in configuration mode. The I^{2}C interface should be used to send telecommands to the STX to set it up prior to the transmission of data (data rate, transmit frequency, transmit power, etc).

9.1.2 Synchronisation mode

After configuration, a telecommand may be sent to put the STX into Synchronisation Mode. In this mode, when the PA is activated, synchronisation bytes will be sent from the transmitter (no real data is read from the SPI input data FIFO). This allows the ground station receiver to achieve lock (synchronisation) before actual payload data is transmitted over the link. In this mode, the data buffer will accept data via the SPI interface only until the internal FIFO is full (indicated via the transmit ready line going low). The synchronisation word is a CCSDS 32bit Attached Sync Marker (ASM) for non-turbo-coded data: 0x1ACFFC1D.

9.1.3 Data mode

In data mode, data from the SPI input FIFO is transmitted. The transmitter should only be placed into Data Mode when the SPI FIFO contains data (indicated by the transmit ready line low) - this will avoid an initial buffer underrun condition. Each SPI bus transaction transfers one (or more) byte(s) of data (a maximum of 4096 bytes may be transferred per SPI transaction). The buffer is 4096 bytes deep. The source of the SPI data (On-Board Computer or Mass Storage) should monitor the Transmit Ready (TR) line, and send data as quickly as possible if the TR line is high, to ensure that a buffer underrun does not occur (FIFO empty condition). The TR line is active (high) when there are less than 513 bytes in the buffer. It is recommended

that the SPI data source sends data to the STX at twice the required transmission rate. If a buffer underrun occurs, *dummy data* (0x55) will be transmitted.

9.1.4   Test data mode

Test data mode will continuously encode and send a test counter of data. The counter begins at 0x00 and continues until 0xFF, before beginning again. In this mode, the data buffer will accept data via the SPI interface only until the internal FIFO is full.

9.1.5   Recommended procedure for transmitting data

A recommended procedure for transmitting user data with the STX is as follows:

- Ensure that a 50 Ω load is connected at all times.

- Configure STX registers (Power level, data rate...).

- Place STX into sync mode with PA on.

- Fill buffer with 4096 bytes of user data.

- Allow enough time for sync to occur with ground station.

- Place STX into data mode.

- Monitor transmit ready line; transfer additional data to the buffer as required.

- Place STX into sync mode with PA off.

- Request telemetry relating to overruns, underruns and the buffer count as a source of transmit verification.

- Place STX into config mode.

Notes:

In order to free up the OBC for the maximum amount of time when the STX is in data mode and operating the SPI transfer at 4 MHz, 4096 bytes of user data may be placed into the buffer when the transmit ready flag indicates that there are 512 bytes or less in the buffer. The amount of time that it takes for the SPI to transfer the data into the buffer is enough time for the FIFO to lower the amount of data bytes in the buffer and therefore balance the amount of data coming into the buffer and the amount going out of it.

On entering data mode from sync, test data or config mode, a filler byte (0x55) is first transmitted, indicating a change in the mode, which is then followed by the user data.

Data interfacing
I²C registers

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When the buffer is filled with 4096 bytes of data, it typically takes 33 ms to transmit all the data from the buffer, at full data rate.

If the STX is in data mode with the PA off, the buffer will still send data out and operate as per usual, yet the data will not actually be transmitted to the ground station as the PA is not active.

The STX has a 15 minute failsafe timeout which disables the PA if it is left on accidentally. The timer operates independently from the other control logic and as such the I^2C config register will indicate that the PA is on. The PA would need to be disabled first before trying to use it again once a timeout has occurred.

9.2 I^2C registers

The STX is controlled by the following 8-bit registers, which are accessed via the I^2C interface. The STX's I^2C address is **0x26** (38_{10}). All command registers (0x00 to 0x04) will default to 0x00 upon reset, unless otherwise specified at manufacture.

Writing to I^2C
The first byte of a transaction is always the pointer (address of register) and the second byte is the value to write to the register.

Reading from I^2C
A write transaction is performed first to set the pointer (register address). Thereafter a read transaction is performed. Further read transactions will auto increment the pointer.

Table 6: I²C register map.

	Address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	r/w	Register group
(9.2.1)	00 h	PA	–	–	–	–	–	MODE1	MODE0	r/w	Control
(9.2.2)	01 h	–	–	–	–	nFILTER	O/QPSK	DR1	DR0	r/w	Encoder
(9.2.3)	02 h	–	–	–	–	–	LED2	LED1	LED0	r/w	Debug
(9.2.4)	03 h	–	–	–	–	–	–	PWR1	PWR0	r/w	PA power level
(9.2.5)	04 h	–	D6	D5	D4	D3	D2	D1	D0	r/w	Synth offset
(9.2.6)	05 h	–	–	–	–	–	–	–	nRST	w	Reset
(9.2.7)	11 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Firmware version
(9.2.8)	12 h	–	–	–	–	–	–	PWRGD	TXL	r	Status
(9.2.9)	13 h	–	–	–	–	–	–	–	TR	r	Transmit ready
(9.2.10)	14 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Buffer underruns (UB)
	15 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Buffer underruns (LB)
(9.2.11)	16 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Buffer overruns (UB)
	17 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Buffer overruns (LB)
(9.2.12)	18 h	–	–	–	D12	D11	D10	D9	D8	r	Buffer count (UB)
	19 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Buffer count (LB)
(9.2.13)	1A h	–	–	–	–	D11	D10	D9	D8	r	RF output power (UB)
	1B h	D7	D6	D5	D4	D3	D2	D1	D0	r	RF output power (LB)
(9.2.14)	1C h	–	–	–	–	D11	D10	D9	D8	r	PA temperature (UB)
	1D h	D7	D6	D5	D4	D3	D2	D1	D0	r	PA temperature (LB)
(9.2.15)	1E h	T11	T10	T9	T8	T7	T6	T5	T4	r	Board temperature top (UB)
	1F h	T3	T2	T1	T0	–	–	–	–	r	Board temperature top (LB)

	Address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	r/w	Register group
(9.2.16)	20 h	T11	T10	T9	T8	T7	T6	T5	T4	r	Board temperature bottom (UB)
	21 h	T3	T2	T1	T0	–	–	–	–	r	Board temperature bottom (LB)
(9.2.17)	22 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Battery current (UB)
	23 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Battery current (LB)
(9.2.18)	24 h	–	–	–	D12	D11	D10	D9	D8	r	Battery voltage (UB)
	25 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Battery voltage (LB)
(9.2.19)	26 h	D15	D14	D13	D12	D11	D10	D9	D8	r	PA current (UB)
	27 h	D7	D6	D5	D4	D3	D2	D1	D0	r	PA current (LB)
(9.2.20)	28 h	–	–	–	D12	D11	D10	D9	D8	r	PA voltage (UB)
	29 h	D7	D6	D5	D4	D3	D2	D1	D0	r	PA voltage (LB)

9.2.1 Register 0x00: Control register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA	–	–	–	–	–	MODE1	MODE0

MODE[1:0] Operating mode for the STX

Mode1	Mode0	
0	0	Configuration
0	1	Synchronisation (Send sync word)
1	0	Data (Transmit real data from FIFO)
1	1	Test data (Transmit test counter)

PA

0	Power amplifer disabled
1	Power amplifier enabled

Note: If the PA enable bit is set while in Configuration mode, the PA will remain disabled until the STX is changed to either Synchronisation, Data or Test data mode.

9.2.2 Register 0x01: Encoder register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	nFILTER	O/QPSK	DR1	DR0

DR[1:0] Data rate of the encoder

DR1	DR0	
0	0	Full data rate
0	1	½ data rate
1	0	¼ data rate
1	1	⅛ data rate

QPSK or OQPSK modulation

O/QPSK

0	QPSK
1	OQPSK

Pulse shaping filter, active low (roll-off = 0.35)

nFILTER

0	Filter enabled
1	Filter disabled

9.2.3   Register 0x02: Debug register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	LED2	LED1	LED0

Writing to the debug register will activate the LEDs. The debug LEDs are active high. LEDs are not populated on flight boards unless otherwise specified.

9.2.4   Register 0x03: PA power level register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	PWR1	PWR0

PWR[1:0] Power level of the power amplifier

PWR1	PWR0	
0	0	21 dBm
0	1	24 dBm
1	0	27 dBm
1	1	30 dBm

9.2.5   Register 0x04: Synth offset register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	D6	D5	D4	D3	D2	D1	D0

A programmable frequency synthesizer is used to generate the STX carrier frequency. The default frequency of 2400 MHz may be adjusted in steps of 500 kHz, to a maximum of 2450 MHz. When a value is written to the Synth offset register, the synthesizer is reprogrammed to the new frequency which will be equal to the default frequency of 2400 MHz plus the value in the Synth offset register (in 500 kHz increments).

E.g. if Synth offset register = 0x01 = 1, then f = 2400.5 MHz.

E.g. if Synth offset register = 0x64 = 100, then f = 2450 MHz.

9.2.6 Register 0x05: Reset register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	nRST

Writing a '0' to this register will cause a soft reset of the FPGA logic, placing it into a known good state. This will reset all registers to their default values.

9.2.7 Register 0x11: Firmware version register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

This register is a BCD encoded value. Bits 7:4 represent the Major number, whilst bits 3:0 represent the Minor number. A firmware version of 1.5 has a Major number equal to 1, and a Minor number equal to 5, 0x15 in hex.

9.2.8 Register 0x12: Status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	PWRGD	TXL

This register contains the frequency lock detect signal for the transmitter (TXL). A value of '1' indicates that a lock was achieved.

The power good (PWRGD) signal will be '1' indicating that the PA power supply is operating correctly whilst the PA is activated.

9.2.9 Register 0x13: Transmit ready register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	TR

The transmit ready (TR) signal register provides an indication as to when data can be written to the STX's buffer. This is identical to the TR hard signal made available to the PC/104 header if requested at manufacture, although as a pollable register. The TR signal has its bit set if data in the transmit buffer drops below a threshold value of 513 bytes of the 4096 byte buffer.

9.2.10   Register 0x14 & 0x15: Buffer underruns register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x14	D15	D14	D13	D12	D11	D10	D9	D8
0x15	D7	D6	D5	D4	D3	D2	D1	D0

The transmit buffer underrun register increments by one each time a "filler" byte (0x55) is transmitted while in data mode.

9.2.11   Register 0x16 & 0x17: Buffer overruns register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x16	D15	D14	D13	D12	D11	D10	D9	D8
0x17	D7	D6	D5	D4	D3	D2	D1	D0

The transmit buffer overrun register increments by one each time a byte is written to the transmit buffer when there are no free slots available. Any data added to the transmit buffer while it is full will be dropped. If this type of error is occuring then care must be taken as to when new data is added to the transmit buffer.

9.2.12   Register 0x18 & 0x19: Buffer count register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	–	–	–	D12	D11	D10	D9	D8
0x19	D7	D6	D5	D4	D3	D2	D1	D0

This register provides an indication of how many bytes of the buffer are currently in use. This value will lower as the transmitter sends out data, and increase as the SPI data source sends data to the STX. It is limited to a count of 4096.

9.2.13   Register 0x1A & 0x1B: RF output power register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1A	–	–	–	–	D11	D10	D9	D8
0x1B	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent RF power output reading. Refer to the test results document for an explanation of the V_{DET} value.

$$V_{DET} = \frac{value\ (dec)\ \times 3}{4096} \times \frac{28}{18}\ [V]$$

Temperature (°C)	Digital output (Binary)	Hex
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
−0.25	1111 1111 1100	FFC
−25	1110 0111 0000	E70

Table 7: Temperature sensor data format.

9.2.14 Register 0x1C & 0x1D: PA temperature

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1C	–	–	–	–	D11	D10	D9	D8
0x1D	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading from the PA's temperature sensor. The temperature sensor is only enabled when the PA is being used.

$$Temperature = \left(\left(\frac{value\ (dec) \times 3}{4096} \right) - 0.5 \right) \times 100\ [°C]$$

9.2.15 Register 0x1E & 0x1F: Board temperature sensor (top)

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E	T11	T10	T9	T8	T7	T6	T5	T4
0x1F	T3	T2	T1	T0	–	–	–	–

This register contains the most recent reading from the temperature sensor located on the top of the board. T11 is a signed bit. Negative values are returned in two's complement. The data format of the temperature sensor is illustrated in Table 7.

$$Temperature = [T11 : T0] \times 0.0625\ [°C]$$

9.2.16 Register 0x20 & 0x21: Board temperature sensor (bottom)

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	T11	T10	T9	T8	T7	T6	T5	T4
0x21	T3	T2	T1	T0	–	–	–	–

This register contains the most recent reading from the temperature sensor located on the bottom of the board. T11 is a signed bit. Negative values are returned in two's complement. The data format of the temperature sensor is illustrated in Table 7.

$$Temperature = [T11 : T0] \times 0.0625\ [°C]$$

9.2.17   Register 0x22 & 0x23: Battery current register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x22	D15	D14	D13	D12	D11	D10	D9	D8
0x23	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading from the battery bus current sensor. It returns a two's complement signed value with D15 being the signed bit.

$$Current = value\ (dec) \times 40 \times 10^{-6}\ [\text{A}]$$

9.2.18   Register 0x24 & 0x25: Battery voltage register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24	–	–	–	D12	D11	D10	D9	D8
0x25	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent battery voltage reading.

$$Voltage = value\ (dec) \times 4 \times 10^{-3}\ [\text{V}]$$

9.2.19   Register 0x26 & 0x27: PA current register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x26	D15	D14	D13	D12	D11	D10	D9	D8
0x27	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading from the power amplifier current sensor. It returns a signed value with D15 being the signed bit. Negative values are returned in two's complement.

$$Current = value\ (dec) \times 40 \times 10^{-6}\ [\text{A}]$$

9.2.20   Register 0x26 & 0x27: PA voltage register

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x28	–	–	–	D12	D11	D10	D9	D8
0x29	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent power amplifier voltage reading. It should have a nominal value of 5 Volts when the PA is in use.

$$Voltage = value\ (dec) \times 4 \times 10^{-3}\ [\text{V}]$$

9.3   SPI Interface

The SPI interface is the High speed data interface to the STX. Once the STX has been correctly configured data can be clocked in via SPI. The user must ensure that buffer underruns and overruns do not occur by monitoring the Transmit Ready line (H1.13).

The SPI mode setting for the interface is:

Mode 0

CPOL = 0 (polarity)

CPHA = 0 (phase)

This means that the serial data (MOSI) will be sampled on the rising edge of SCLK.

9.3.1   Transmit Ready

The data buffer size of the STX is 4096 bytes. The Transmit Ready (TR) line will be a logic HIGH while data can be safely written to the data buffer. The TR line will become a logic LOW when the buffer is filled with more than 512 bytes. No more than 4096 bytes of data should be written to the data buffer via SPI at any one time, this is to ensure that overruns do not occur. It is recommended that the OBC sending data to the STX monitors the TR line, when the TR line is HIGH it then sends user data, while TR is LOW, it waits. The state of TR is also available via I^{2}C, when reading the Transmit Ready register (0x13). The availability of free slots in the buffer may be monitored by viewing the buffer count register (0x18 & 0x19).

10 Test procedures

This section describes the process of testing the STX. When testing with the power amplifier on, be sure to connect the RF output port to an appropriate 50 Ω load. Use an attenuator if required.

10.1 Transmit full buffer with buffer emptied

- Write a value of 0x00 to register 0x00. This will reset the buffer and the overruns, underruns and buffer count registers.

- Write a value of 0x02 to register 0x03. This will configure the PA to have a 27 dBm power output. Only necessary if the PA is used in the test.

- Confirm that the buffer is empty by checking the buffer count register.

- Write a value of 0x01 to register 0x00. This will put the STX into sync mode, with the PA off.

- Transfer 4096 bytes of user data via SPI to the STX.

- Confirm buffer has been filled, with no overruns, by checking the overrun and buffer count telemetry registers.

- Write a value of 0x81 to register 0x00. This will turn the PA on, while still in sync mode. 0x01 may be sent if the PA is not used in the test.

- Wait for five seconds to allow for a sync lock occur with the ground station receiver. If the PA is used in the test.

- Write a value of 0x82 to register 0x00. This will put the STX into data mode with the PA on. 0x02 may be written if the PA is not to be used.

- Wait for 33 ms (at full data rate).

- Write a value of 0x01 to register 0x00. This will put the STX into sync mode, with the PA off.

- Retrieve overrun, underrun and buffer count telemetry data. A small amount of underruns and a buffer count of zero indicates that all the data was sent.

- Write a value of 0x00 to register 0x00. This will reset the buffer and the overruns, underruns and buffer count registers.

10.2   Continuous transmit of user data with buffer not emptied

- Write a value of 0x00 to register 0x00. This will reset the buffer and the overruns, underruns and buffer count registers.

- Write a value of 0x02 to register 0x03. This will configure the PA to have a 27 dBm power output. Only necessary if the PA is used in the test.

- Confirm that the buffer is empty by checking the buffer count register.

- Write a value of 0x01 to register 0x00. This will put the STX into sync mode, with the PA off.

- Transfer 4096 bytes of user data via SPI to the STX.

- Confirm buffer has been filled, with no overruns, by checking the overrun and buffer count telemetry registers.

- Write a value of 0x81 to register 0x00. This will turn the PA on, while still in sync mode. 0x01 may be sent if the PA is not used in the test.

- Loop: Monitor receive ready flag, if flag is high then immediately transmit user data via SPI to the buffer, otherwise do not transmit data via SPI. Loop as many times as desired.

- Monitor transmit ready flag, when the flag goes from low to high, indicating less than 513 bytes in the buffer, promptly stop sending SPI data to the STX and write a value of 0x01 to register 0x00. This will put the STX into Sync mode, with the PA off.

- Retrieve overrun, underrun and buffer count telemetry data. The buffer count register should indicate a value less than 513 bytes, if the data transfers were successful during the test, then the overrun and underrun registers should be zero indicating that the data transfer timing is correct.

- Write a value of 0x00 to register 0x00. This will reset the buffer and the overruns, underruns and buffer count registers, and place the STX into Configuration mode.

11   Special note regarding transmit power

Each STX's RF frequency is 2400 MHz at startup (default transmit frequency). Four power steps are selectable: $1/8$, $1/4$, $1/2$ and 1 W. The transmit power levels have been optimised for 2400 MHz operation and as such, the transmit power increases significantly as the transmit frequency is increased towards 2450 MHz. If the power is set to $1/2$ W at 2400 MHz, the STX will output approximately 1 W at 2450 MHz. The 1 W setting may overdrive the power amplifier at the higher frequencies in the range, which may or may not damage it.

While this might not be an issue if the STX is to be used at a single frequency (which is usually the case), the transmit power levels must be recalibrated if it is to be used at a frequency higher than approximately 2405 MHz. The calibration should be performed at manufacture, yet the client will not be charged if this occurs at a later date, it would however be best to make such a change at our premises. The adjustment requires the replacement of a single resistor. If no such adjustment is made, the STX will continue to perform as expected, yet attention must be paid to the power level settings at particular frequencies.

If the user has specified a particular startup frequency, then the STX would be optimized accordingly for that selection at manufacture.