



LDI Demonstration Kit User Manual

(LVDS Display Interface)

P/N LDI3V8BT-112

Rev 4.1

Interface Products

Information contained in this document is subject to change

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Introduction

National Semiconductor's Interface Products Group LDI demo kit contains a Transmitter (Tx) demo board and a Receiver (Rx) demo board along with an interface cable. This kit will demonstrate the chipsets interfacing from a graphics controller using Low Voltage Differential Signaling (LVDS) to a Liquid Crystal Display (LCD) flat panel.

The Transmitter board accepts 3V LVTLL/CMOS RGB signals from a graphics controller along with the clock and control signals. The LVDS Transmitter converts the LVTLL/CMOS parallel lines into serialized LVDS pairs. The serial data streams toggle at 3.5 times the clock speed.

The Receiver board accepts the LVDS serialized data (and clock) and converts them back into parallel LVTLL/CMOS RGB signals for the Panel Timing Controller.

The user needs to provide the proper RGB inputs to the Transmitter and also to provide a proper interface from the Receiver output to the panel timing controller. In some cases, a cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used.

Warnings:

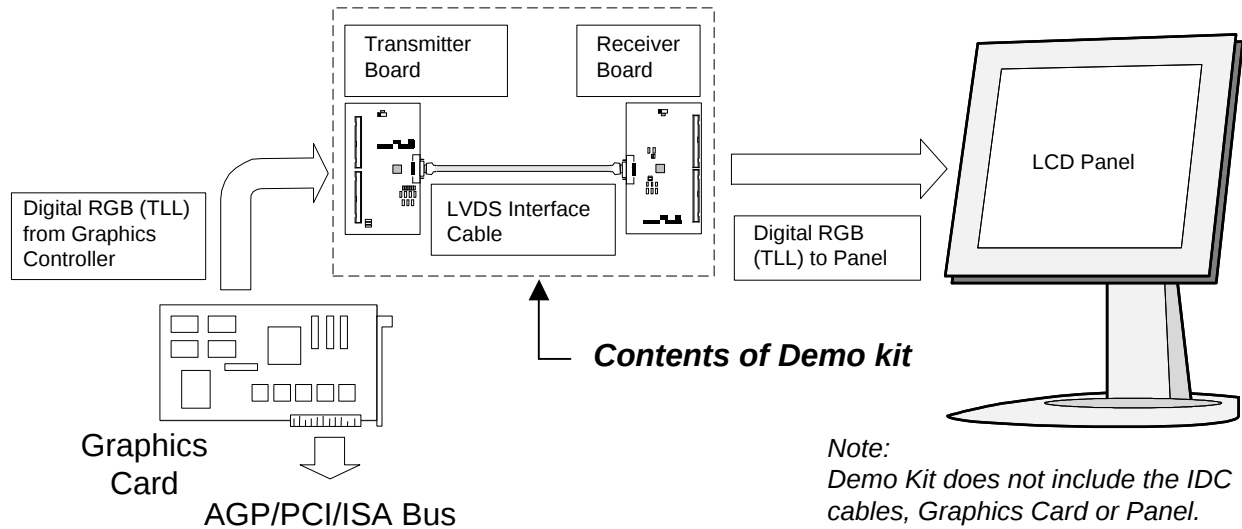
The maximum voltage that should ever be applied to the LDI Transmitter or Receiver Vcc is 4V. The Transmitter and Receiver power supply pins (Vccs) are **NOT** 5V tolerant. The Transmitter can however accept a 3.3V or 5V LVTLL/CMOS level on the inputs (TxIN). The Transmitter inputs are 5V tolerant. The maximum voltage that can be applied to any input pin is 5.0V.

Contents of Demo Kit

- 1) One Transmitter board with IDC connectors on Tx input
DS90C387MTD - 48 bit Transmitter
- 2) One Receiver board with IDC connectors on Rx output
DS90CF388MTD - 48 bit Receiver
- 3) One 2-meter 3M MDR LVDS Cable interface to connect TxOUT to RxIN. Note: The MDR footprint has been set to accept a D26-1 pinout.
- 4) AN1127: LVDS Display Interface TFT Data Mapping
- 5) Demonstration Kit Documentation
- 6) DS90C387/DS90CF388 Datasheet

*Note: The demo board trace layout is designed for minimum skew between channels. It is not absolutely required in most applications but be aware that the skew margins will be reduced if your board layout is not optimized.

Applications



LDI Application

The diagram above illustrates the use of the Chipset (Tx/Rx) in a Host to LCD Panel Interface.

Chipsets support up to 24-bit single pixel or 24-bit dual pixel AM-TFT LCD Panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), SXGA (1280X1024), or UXGA (1600X1200).

Because of the non-periodic nature of STN-DD SHFCLK, the Chipset may not work with all D-STN panels. The PLL CLK input of the Transmitter requires a free running periodic SHFCLK. Most Graphics Controller can provide a separate pin with a free running clock. In this case the STN-DD SHFCLK can be sent as Data while the free running clock can be used as SHFCLK for the PLL ref CLK. For example, C&T's 65550's WEC(Pin102) can be programmed to provide a free running clock using the BMP (Bios Modification Program). Please refer to STN Application using (AN-1056) for more information.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

Note: Refer to AN-1127 for suggested mapping schemes.

Features and Explanations

Transmitter

Pre-emphasis (PRE - pin 14/JP1):

1. This feature enables you to overcome cable capacitance through the LVDS interface. This function provides additional instantaneous current during switching transitions. NOTE: This function does NOT affect Rx output drive.
2. This function works in “Old Mode” or “New Mode”.
3. It affects Tx A0-A7 and CLKs LVDS outputs only.
4. To disable this function, pin 14 must be tied LOW. LVDS output drive will then be at its standard value of 3.5mA.
5. The input will be pulled low (0.7V) if no jumper is used. To adjust the level of pre-emphasis, place a jumper on JP1 to Vcc. R48 will now be connected. R48 is a 2K potentiometer. Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. Too much pre-emphasis can create an overshoot condition at the rising edge and an undershoot condition on the falling edge. Icc will increase but allows you to drive longer cables. Too little pre-emphasis will not allow you to drive longer cables. Monitor any one of the LVDS lines (A0-A7) or CLK1 for a visual confirmation of its effect. It is recommended that you monitor the LVDS signals with a differential probe. If a differential probe is not used, a single ended probe can be used for a quick check.

PLL range select (PLLSEL - pin 15/JP5):

1. Auto-range is selected by tying pin 15 HIGH.
2. Low-range is selected by tying pin 15 LOW.
3. This function works in “Old Mode” or “New Mode”.

Dual/Single Operation (DUAL - pin 23/JP7):

1. This feature provides three different modes of operation. The modes of operation are:
 - 1) Dual 112MHz TxIN, Dual 112MHz TxOUT (pin 23 = HIGH; jumper JP7 to Vcc)
 - 2) Single 170MHz TxIN, Dual 85MHz TxOUT (pin 23 = Vcc/2; no jumper on JP7)
 - 3) Single 112MHz TxIN, Single 112MHz TxOUT (pin 23 = LOW; jumper JP7 to GND)
2. This function works in “Old Mode” or “New Mode” .
3. In Single to Single mode, TxOUT0 through TxOUT3 and associated Tx inputs are active. TxOUT4 through TxOUT7 and associated inputs are disabled to promote power savings on the part.

DC Balance (BAL - pin 24/JP4):

1. This feature prevents charging of a cable in one state e.g. all “1s” or all “0s” for an extended period of time. The benefit to this is to “open” up the LVDS “eye-pattern” (Reducing the Inter-Symbol Interference).

2. This function works in "New Mode" ONLY.
3. It affects Tx A0-A7 and LVDS CLK outputs only.
4. To disable this function, pin 24 is tied LOW. To enable this function pin 24 is tied HIGH.
5. BAL (pin 6 of the Rx/JP6 on Rx board) must also be tied HIGH to enable this function.
6. In this mode, the part is NOT backward compatible with existing FPD-Link technology. This feature must be turned off to be backward compatible with current FPD-Link chipsets.

NOTE: Refer to the "Application Notes" on back of the data sheet for complete description of each feature.

Receiver

PLL range select (PLLSEL - pin 5/JP5):

1. Auto-range is selected by tying pin 5 HIGH.
2. Low-range is selected by tying pin 5 LOW.

DESKEW option (pin 4/JP4):

1. This function works in "New Mode" ONLY.
2. In order for the "DESKEW" feature to be operational (DESKEW=HIGH), a minimum of four clock cycles is required during blanking time.
3. To set "DESKEW" feature OFF, set jumper JP4 LOW.

DC Balance (BAL - pin 6/JP6):

1. This feature prevents charging of a cable in one state e.g. all "1s" or all "0s" for an extended period of time. The benefit to this is to "open" up the LVDS "eye-pattern".
2. This function works in "New Mode" ONLY.
3. To disable this function, pin 6 is tied LOW. To enable this function pin 6 is tied HIGH.
4. BAL (pin 24 of the Tx/JP4 on Tx board) must also be tied HIGH to enable this function.
5. In this mode, the chipset is NOT backward compatible with existing FPD-Link technology. This feature must be turned off to be backward compatible with current FPD-Link chipsets.

NOTE: Refer to the "Application Notes" section on the back of the datasheet for complete description of each feature.

How to hook up the demo boards (overview)

The Tx demo board TxIN has been laid out to accept data from the Video Graphics card through two 50 pin IDC connectors. The TxOUT/RxIN interface uses the 3M MDR connector and 3M MDR cable with a D26-1 pin out. This combination provides minimal skew between LVDS channels. The receiver board RxOUT is laid out generically and must be mapped correctly to the panel being used.

- 1) Connect one end of the D26-1 MDR cable to the transmitter board and the other end to the receiver board. This is a standard pinout cable, longer lengths are available for purchase from 3M - see <http://www.mmm.com>
- 2) Jumpers have been configured from the factory (Refer to Tx and Rx "Jumper Default Settings" on pages 11 and 17) to run in normal mode with Deskew function OFF and with pre-emphasis ON. Jumpers are also provided on both boards so make sure that they are positioned correctly. See "Jumper Setting Examples" on page 22 and page 25 for different application configurations.
- 3) From the Graphics card, connect the appropriate IDC cable to the transmitter board and connect two 50-pin IDC cables from the receiver boards to the panel (**Note:** Refer to AN-1127 for suggested mapping schemes.) Note that pin 1 on the connector should be connected to pin 1 of the cable.
- 4) Power for the Tx and Rx boards are supplied externally through Test Pad (TP) TP1. Grounds for both boards are connected through TP2.
- 5) Turn on the PC first then power up the panel.

Warning:

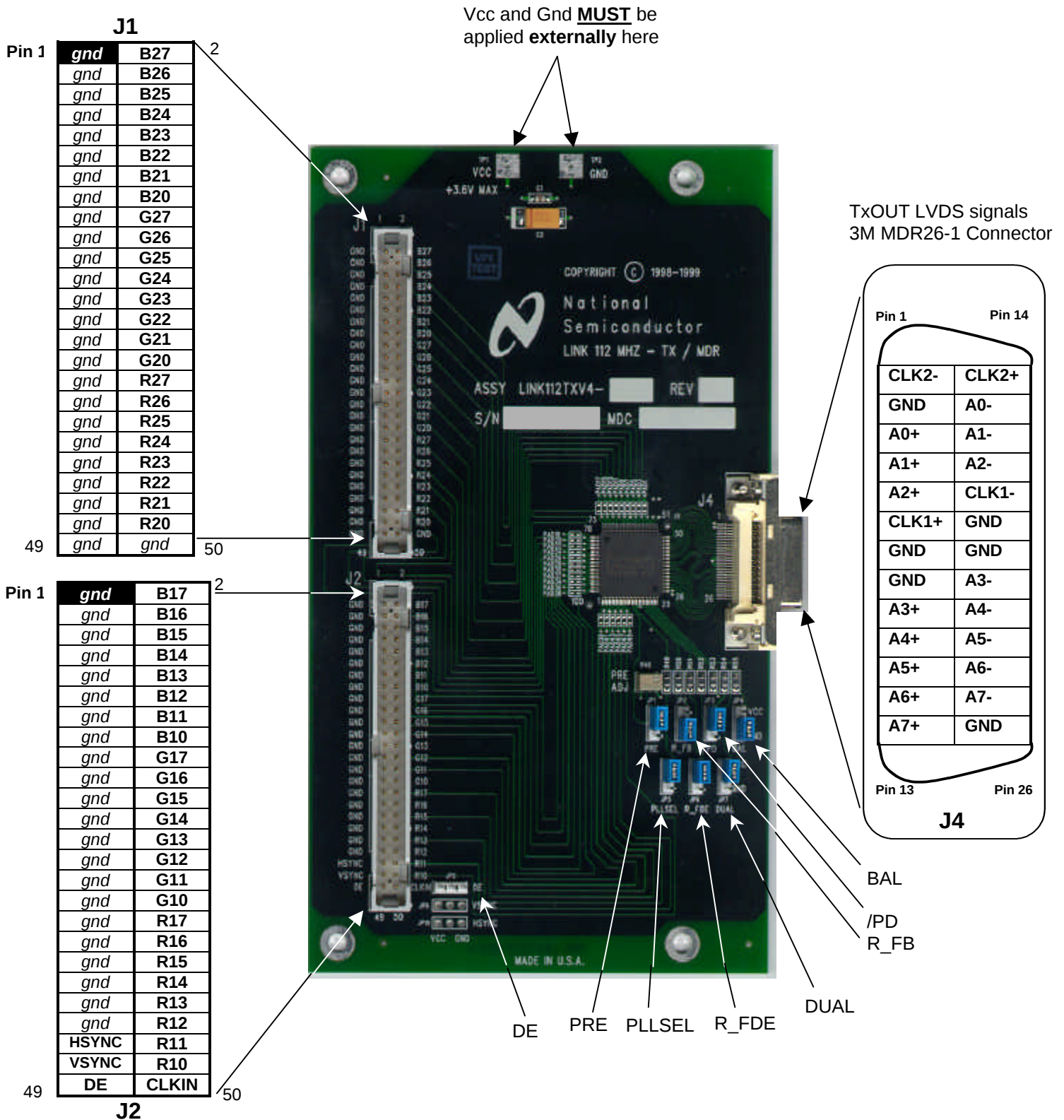
Clock 2 is brought over to the Rx board through the USB pair, which are not matched in length with Clock 1, or LVDS data lines. Also the differential impedance of the USB pair is rated at 90 ohms.

Power Connections

The Transmitter and Receiver boards can only be powered by supplying power externally through TP1 (Vcc) and TP2 (GND). The **maximum voltage** that should ever be applied to the LDI Transmitter or Receiver **Vcc is 4V**. For the transmitter and the receiver to be operational, /PD must be tied to Vcc which is labeled as "JP3" and "JP1", respectively.

Note: J4 on the Tx and J1 on the Rx provide the interface for LVDS signals.

Transmitter Board



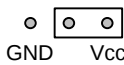
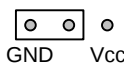
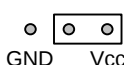
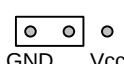
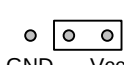
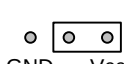
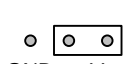
Tx Board Jumper Definition

<u>Jumper</u>	<u>Purpose</u>	<u>Settings</u>
PRE (JP1)	PRE-emphasis	  = NONE   = ON GND Vcc GND Vcc (NONE: NO pre-emphasis; ON: pre-emphasis is adjusted through R48) When NO jumper is used, pre-emphasis is at 0.7V value.
R_FB (JP2)	Rising or Falling data strobe	  = Rising   = Falling GND Vcc GND Vcc
/PD (JP3)	PowerDown	  = OFF   = ON GND Vcc GND Vcc (OFF: Tx powers down; ON: Tx is operational)
BAL (JP4)	DC BALance	  = OFF   = ON GND Vcc GND Vcc (Old Mode DC Balance OFF; New Mode DC Balance ON)
PLLSEL (JP5)	PLL SElect (auto-range)	  = LOW   = HIGH GND Vcc GND Vcc (LOW: auto-range OFF; HIGH: auto-range ON)
R_FDE (JP6)	Rising or Falling Data Enable¹	  = Rising   = Falling GND Vcc GND Vcc
DUAL (JP7)	DUAL/single mode	  = Single   = Dual GND Vcc GND Vcc (When NO jumper is used, it is in Single to Dual Mode.)

¹ In Old Mode, the R_FDE pin is ignored by both the Tx and Rx when operating in Single (DUAL=LOW) or DUAL (DUAL=HIGH) mode. When the transmitter is operating in Single-to-Dual Mode (DUAL=1/2 Vcc), the R_FDE pin must be set HIGH if active data when DE signal is HIGH.
In New Mode, R_FDE pins of both Tx and Rx boards MUST set to HIGH if DE signal is High during active data. R_FDE pins must set to LOW when DE signal is LOW during active data.

Tx Board Jumper Default Settings

The default setting for the Tx board is set to Old Mode, Dual-pixel mode and with pre-emphasis¹.

<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
PRE	PRE -Emphasis ¹		JP1
R_FB	R ising or F alling data strobe		JP2
/PD	P ower D own		JP3
BAL	DC B ALance (Old Mode)		JP4
PLLSEL	PLL SE lect (auto-range)		JP5
R_FDE	R ising or F alling D ata E nable		JP6
DUAL	D UAL/single mode		JP7

¹ An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.

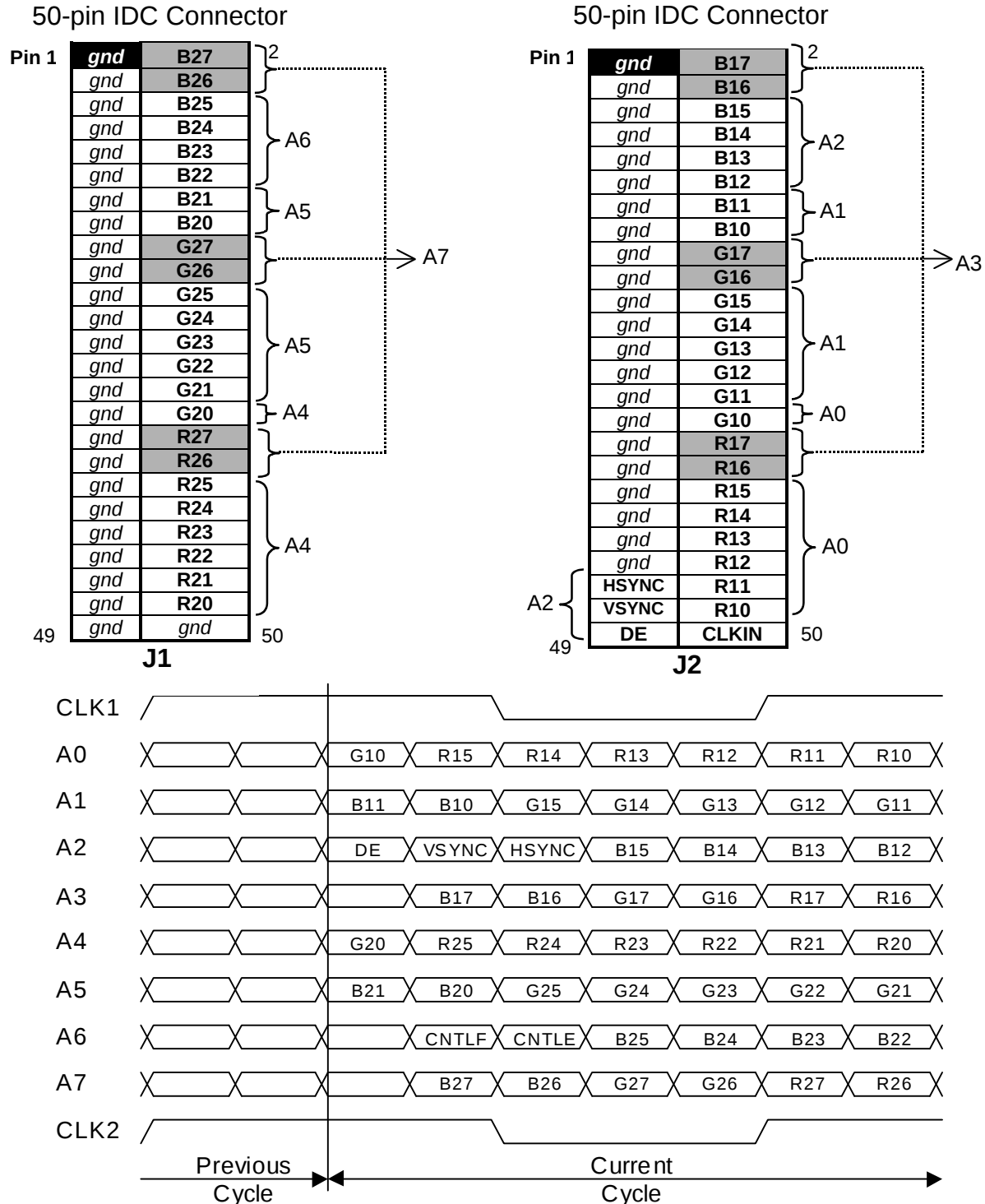
See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

LVDS Mapping by IDC Connector

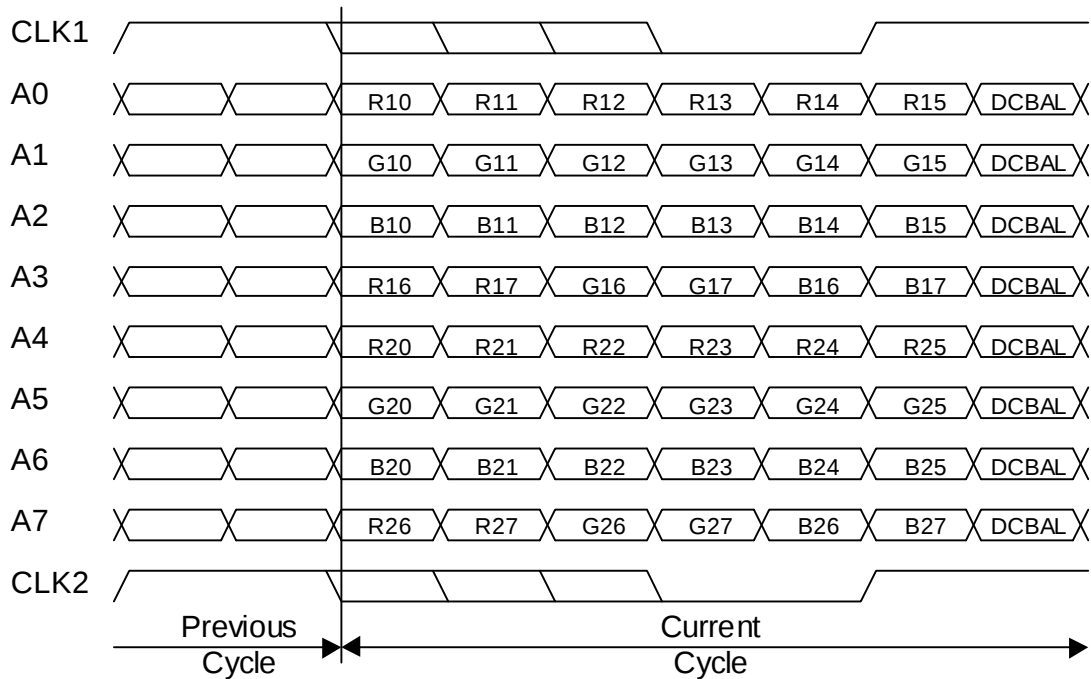
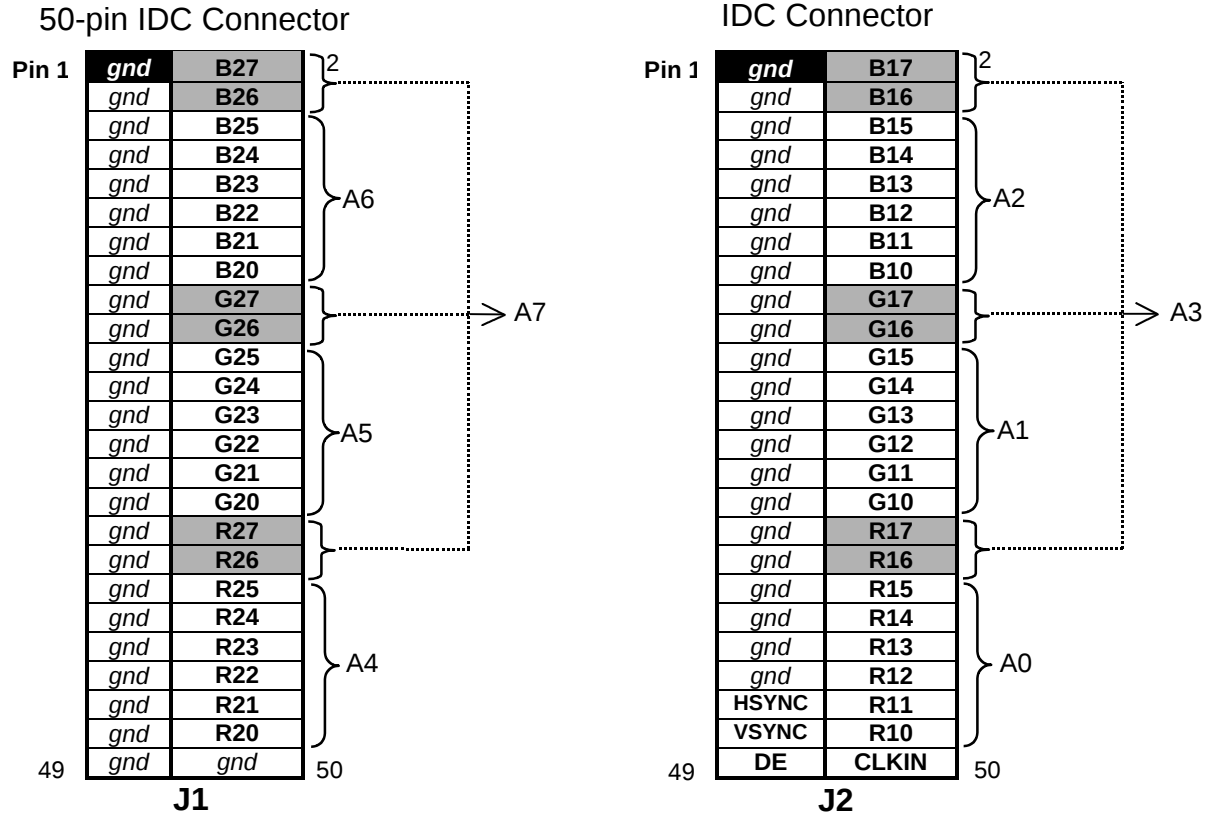
The following two figures show how the Tx inputs are mapped to the IDC connector (It is also printed on the demo boards.) and to each of the eight LVDS channels.

Note: Refer to AN-1127 for suggested mapping schemes.

Mapping for Old Mode (Transmitter Board)



Mapping for New Mode (Transmitter Board)



Tx Optional: Parallel Termination for TxIN

On the Tx demo board, there are 50 inputs that have an 0402 pad on one side and the other side tied to ground. These pads are unpopulated from the factory but are provided if the user needs to adjust the input termination to match the impedance of the input signal. PAD1 TO PAD48 and PAD50 to PAD52 are associated with the Tx data input lines. PAD49 is associated with CLKIN.

Mapping for Transmitter Inputs for the Optional Parallel Termination Resistors:

Tx Pin Names	Tx Pin Number	Parallel Termination Resistor
R10	10	PAD48
R11	9	PAD47
R12	8	PAD46
R13	7	PAD45
R14	6	PAD44
R15	5	PAD43
R16	4	PAD42
R17	3	PAD41
G10	2	PAD40
G11	1	PAD39
G12	100	PAD38
G13	99	PAD37
G14	96	PAD36
G15	95	PAD35
G16	94	PAD34
G17	93	PAD33
B10	92	PAD32
B11	91	PAD31
B12	90	PAD30
B13	89	PAD29
B14	88	PAD28
B15	87	PAD27
B16	86	PAD26
B17	85	PAD25
R20	84	PAD24
R21	81	PAD23

Tx Pin Names	Tx Pin Number	Parallel Termination Resistor
R22	80	PAD22
R23	79	PAD21
R24	78	PAD20
R25	77	PAD19
R26	76	PAD18
R27	75	PAD17
G20	74	PAD16
G21	73	PAD15
G22	72	PAD14
G23	71	PAD13
G24	70	PAD12
G25	69	PAD11
G26	66	PAD10
G27	65	PAD9
B20	64	PAD8
B21	63	PAD7
B22	62	PAD6
B23	61	PAD5
B24	60	PAD4
B25	59	PAD3
B26	58	PAD2
B27	57	PAD1
DE	56	PAD50
VSYNC	55	PAD51
HSYNC	54	PAD52
CLKIN	11	PAD49

BOM (Bill of Materials)

Bill of Materials LDI_112_MHz_Tx_Bom

Type	Pattern	Value	Designators
3M_MDR_D26-1 Qty = 1			J4
3_PIN_HEADER Qty = 10	.1" spacing		JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10
25X2_IDC_CONN Qty = 2			J1 J2
PAD Qty = 52	0402 (See previous page)	Optional	PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8 PAD9 PAD10 PAD11 PAD12 PAD13 PAD14 PAD15 PAD16 PAD17 PAD18 PAD19 PAD20 PAD21 PAD22 PAD23 PAD24 PAD25 PAD26 PAD27 PAD28 PAD29 PAD30 PAD31 PAD32 PAD33 PAD34 PAD35 PAD36 PAD37 PAD38 PAD39 PAD40 PAD41 PAD42 PAD43 PAD44 PAD45 PAD46 PAD47 PAD48 PAD49 PAD50 PAD51 PAD52
CAP Qty = 2	CC0805	.001uF	C4 C10
CAP Qty = 4	CC0805	.01uF	C5 C6 C8 C11
CAP Qty = 5	CC0805	.1uF	C1 C3 C7 C9 C12
DS90C387 Qty = 1			U1
POT Qty = 1		10Kohm	R48
RES Qty = 7		10ohm	R49 R50 R51 R52 R53 R54 R55
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10uF	C2 C13 C14 C15

Receiver Board

Vcc and Gnd **MUST** be applied **externally** here

R_FDE

PowerDown (bar) Jumper

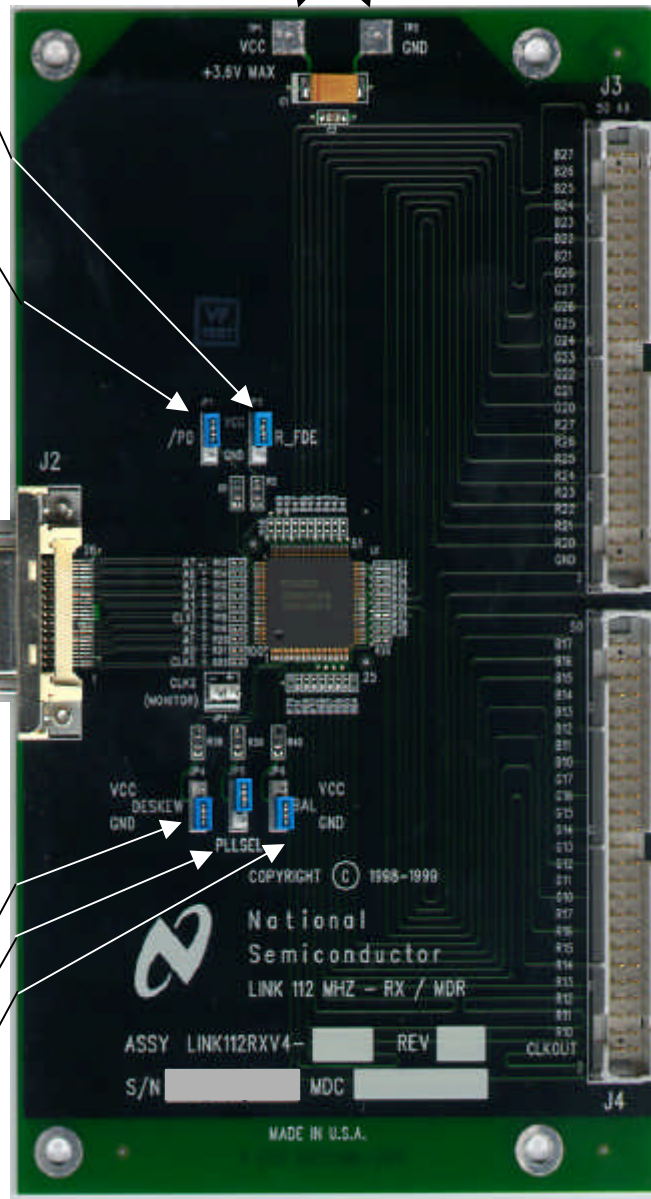
RxIN LVDS signals
3M MDR26-1 connector

Pin 26	Pin 13
GND	A7+
A7-	A6+
A6-	A5+
A5-	A4+
A4-	A3+
A3-	GND
GND	GND
GND	CLK1+
CLK1-	A2+
A2-	A1+
A1-	A0+
A0-	GND
CLK2+	CLK2-
Pin 14	Pin 1

DESKEW

PLLSEL

BAL



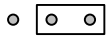
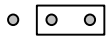
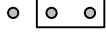
J3

50	B27	gnd	49
	B26	gnd	
	B25	gnd	
	B24	gnd	
	B23	gnd	
	B22	gnd	
	B21	gnd	
	B20	gnd	
	G27	gnd	
	G26	gnd	
	G25	gnd	
	G24	gnd	
	G23	gnd	
	G22	gnd	
	G21	gnd	
	G20	gnd	
	B27	gnd	
	B26	gnd	
	B25	gnd	
	B24	gnd	
	B23	gnd	
	B22	gnd	
	B21	gnd	
	B20	gnd	
	gnd	gnd	Pin 1

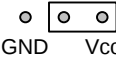
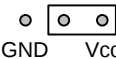
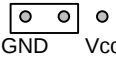
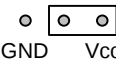
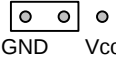
50	B17	gnd	49
	B16	gnd	
	B15	gnd	
	B14	gnd	
	B13	gnd	
	B12	gnd	
	B11	gnd	
	B10	gnd	
	G17	gnd	
	G16	gnd	
	G15	gnd	
	G14	gnd	
	G13	gnd	
	G12	gnd	
	G11	gnd	
	G10	gnd	
	R17	gnd	
	R16	gnd	
	R15	gnd	
	R14	CNTLE/NC	
	R13	CNTLF/NC	
	R12	STOPCLK	
	R11	HSYNC	
	R10	VSYN	
2	CLKOUT	DE	Pin 1

J4

Rx Board Jumper Definition

<u>Jumper</u>	<u>Purpose</u>	<u>Settings</u>
/PD (JP1)	PowerDown	 = OFF  = ON GND Vcc GND Vcc (OFF Tx powers down; ON Tx is operational)
R_FDE (JP2)	Rising or Falling Data Enable	 = Falling  = Rising GND Vcc GND Vcc
DESKEW (JP4)	DESKEW	 = OFF  = ON GND Vcc GND Vcc
PLLSEL (JP5)	PLL SElect (auto range)	 = OFF  = ON GND Vcc GND Vcc
BAL (JP6)	DC BALance	 = OFF  = ON GND Vcc GND Vcc (Old Mode DC Balance OFF; New Mode DC Balance ON)

Rx Board Jumper Default Settings

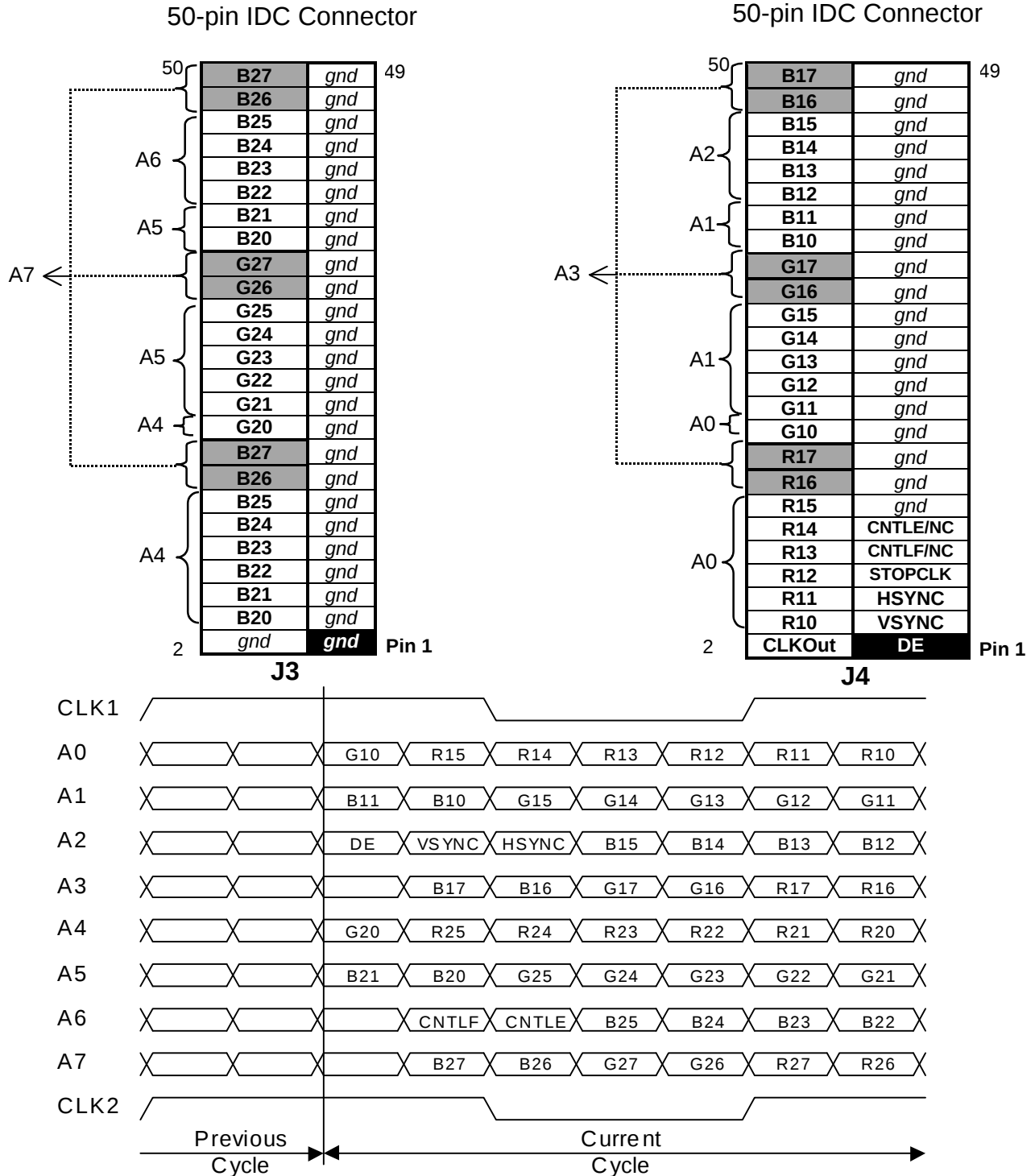
<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
/PD	PowerDown – ON (Part is enabled)	 GND Vcc	JP1
R_FDE	Rising or Falling Data Enable	 GND Vcc	JP2
DESKEW	DESKEW	 GND Vcc	JP4
PLLSEL	PLL SElect (auto-range)	 GND Vcc	JP5
BAL	DC BALance	 GND Vcc	JP6

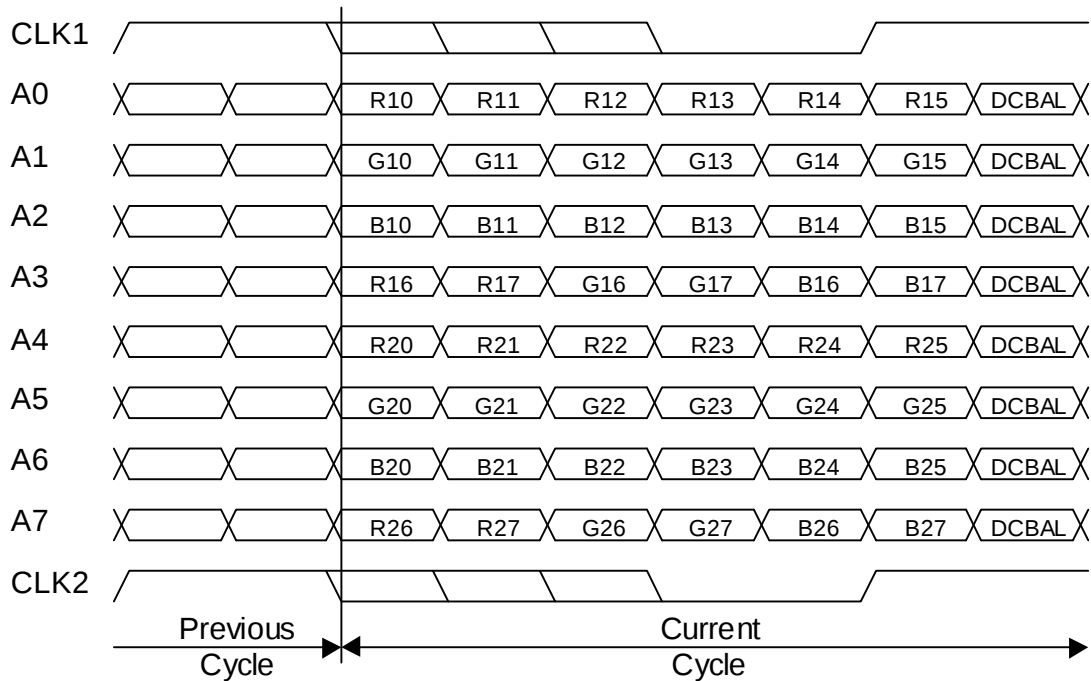
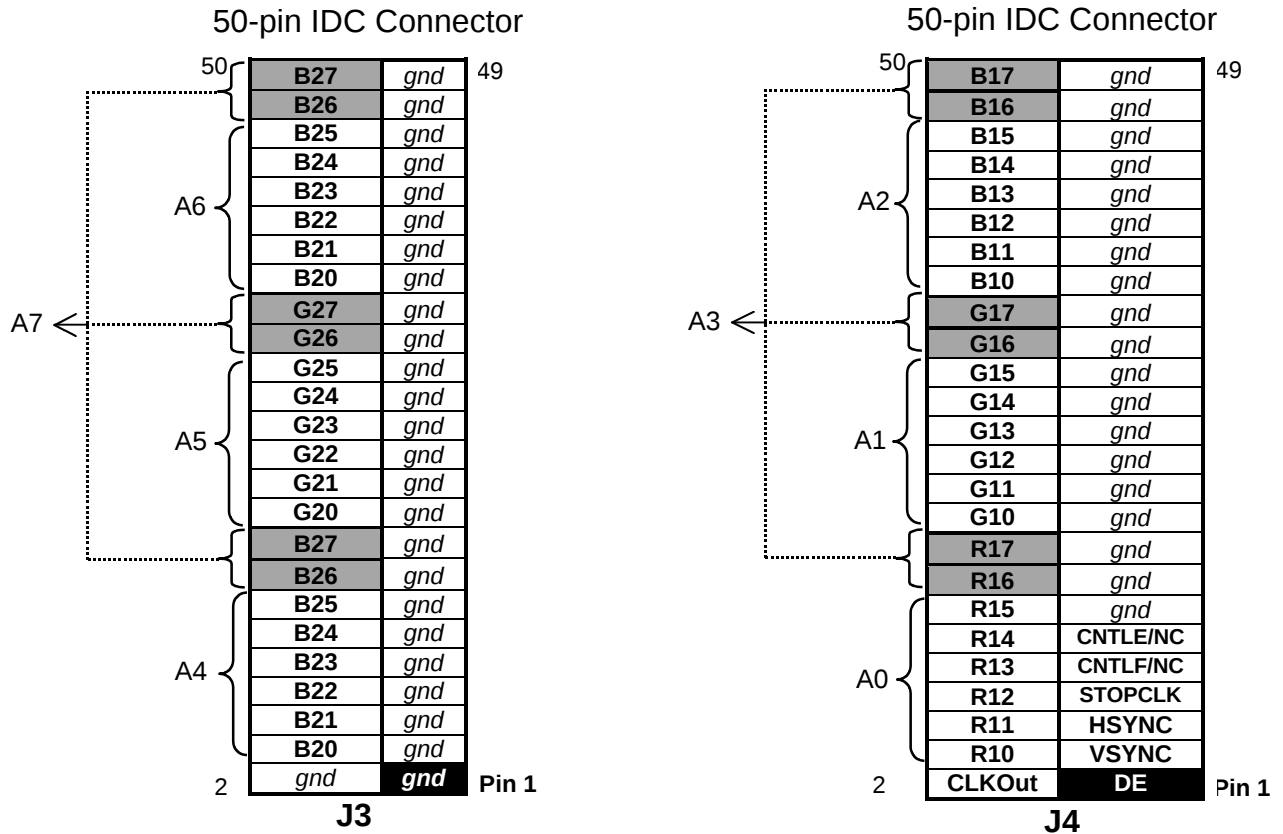
LVDS Mapping by IDC Connector

The following two figures show how the Rx outputs are mapped to the IDC connector and to each of the eight LVDS channels.

Note: Refer to AN-1127 for suggested mapping schemes.

Mapping for Old Mode (Receiver Board)



Mapping for New Mode (Receiver Board)

Rx Optional: Series Termination for RxOut

On the Rx demo board there are 49 outputs that have an 0402 pad in series (but shorted). These pads are unpopulated from the factory but are provided if the user needs to adjust the output series termination to match the impedance of an input line the user must cut the short out before mounting a series resistor. R6-R12, R24-R37, R41-R70 are associated with the DATA input lines. R23 is associated with CLKOUT.

Rx Pin Names	Rx Pin Number	Parallel Termination Resistor
R10	8	R70
R11	9	R31
R12	10	R69
R13	11	R32
R14	12	R68
R15	14	R33
R16	15	R67
R17	17	R34
G10	18	R66
G11	19	R35
G12	20	R65
G13	21	R36
G14	22	R64
G15	24	R37
G16	26	R30
G17	27	R63
B10	28	R29
B11	29	R62
B12	30	R28
B13	31	R61
B14	32	R27
B15	34	R60
B16	36	R26
B17	37	R59
R20	38	R58
R21	39	R25
R22	40	R57
R23	41	R24

Rx Pin Names	Rx Pin Number	Parallel Termination Resistor
R24	43	R56
R25	46	R55
R26	47	R54
R27	48	R53
G20	49	R52
G21	50	R51
G22	51	R41
G23	52	R12
G24	53	R42
G25	55	R11
G26	57	R43
G27	58	R10
B20	59	R44
B21	60	R9
B22	61	R45
B23	62	R8
B24	64	R46
B25	65	R7
B26	67	R47
B27	68	R6
DE	69	R48
VSYNC	70	R5
HSYNC	71	R49
STOPCLK	73	R4
CNTLF/NC	74	R50
CNTLE/NC	75	R3
CLKOUT	42	R23

BOM (Bill of Materials)

Bill of Materials		LDI_112_MHz_Rx_Bom	
Type	Pattern	Value	Designators
2_PIN_HEADER Qty = 1	.1" spacing		JP3
3M_MDR_D26--1 Qty = 1			J2
3_PIN_HEADER Qty = 5	.1" spacing		JP1 JP2 JP4 JP5 JP6
25X2_IDC_R Qty = 2			J3 J4
PAD Qty = 6	0402	Shorted	PAD1 PAD2 PAD3 PAD4 PAD5 PAD6
CAP Qty = 2	CC0805	.001uF	C4 C10
Qty = 4	CC0805	.01uF	C5 C6 C8 C11
Qty = 5	CC0805	.1uF	C2 C3 C7 C9 C12
DS90CF388 Qty = 1			U1
R0402 Qty = 55	Optional (See previous page)		R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70
RES Qty = 10		100ohm	R13 R14 R15 R16 R17 R18 R19 R20 R21 R22
Qty = 5		10ohm	R1 R2 R38 R39 R40
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10uF	C1 C13 C14 C15

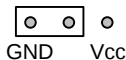
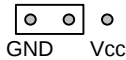
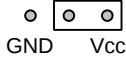
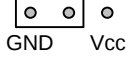
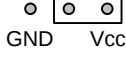
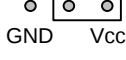
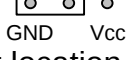
Jumper Setting Examples 1 (Old Mode)

The LDI chipset supports up to 24-bit single pixel and 24-bit dual pixel formats. The following examples show how to set the jumpers for a specific pixel format in Old Mode.
WARNING

18-bit or 24-bit Single Pixel (Old Mode)

The jumper settings below are for Old Mode, Single to Single pixel application.

For Tx board: (For Rx board jumper settings in this application, see Rx Board Jumper Default Settings on page 17)

<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
PRE	PRE -Emphasis ¹		JP1
R_FB	R ising or F alling data strobe		JP2
/PD	P ower D own		JP3
BAL	DC B ALance		JP4
PLLSEL	PLL SE lect (auto-range)		JP5
R_FDE	R ising or F alling D ata E nable ²		JP6
DUAL	DUAL /single mode		JP7

¹ An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.

See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

² In Old Mode, R_FDE can be set HIGH or LOW.

Note:

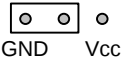
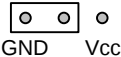
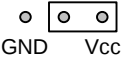
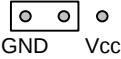
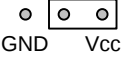
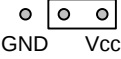
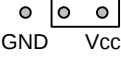
- A) In the single pixel mode, only TxOUT0 through TxOUT3 (LVDS channels A0-A3) and their associated inputs are active. TxOUT4 through TxOUT7 and their associated inputs and CLK2 are disabled for power savings.
- B) "Old Mode" is backward compatible to existing FPD-Link technology.

18-bit or 24-bit Dual Pixel (Old Mode)

(Default Setting from the factory)

The jumper settings below are for Old Mode, Dual to Dual pixel application.

For Tx board: (For Rx board jumper settings in this application, see Rx Board Jumper Default Settings on page 17)

<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
PRE	PRE -Emphasis ¹	 GND Vcc	JP1
R_FB	R ising or F alling data strobe	 GND Vcc	JP2
/PD	P ower D own	 GND Vcc	JP3
BAL	DC B ALance	 GND Vcc	JP4
PLLSEL	PLL SE lect (auto-range)	 GND Vcc	JP5
R_FDE	R ising or F alling D ata E nable ²	 GND Vcc	JP6
DUAL	D UAL/single mode	 GND Vcc	JP7

¹ An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.

See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

² In Old Mode, R_FDE can be set HIGH or LOW.

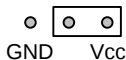
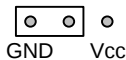
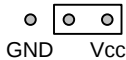
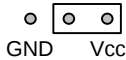
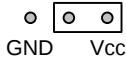
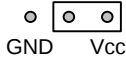
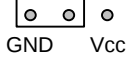
Jumper Setting Example 2 (New Mode)

The LDI chipset supports up to 24-bit single pixel and 24-bit dual pixel formats. The following examples show how to set the jumper for a specific pixel format in New Mode.

18-bit or 24-bit Single Pixel (New Mode)

The jumper settings below are for New Mode, Single to Single pixel application.

For Tx board: (The Rx board jumper settings in this application is the same as the Rx Board Jumper Default Settings on page 17 except the BAL pin(JP6), which must be set to Vcc.)

<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
PRE	PRE -Emphasis ¹		JP1
R_FB	R ising or F alling data strobe		JP2
/PD	PowerDown		JP3
BAL	DC BAL ance (New Mode)		JP4
PLLSEL	PLL SE lect (auto-range)		JP5
R_FDE	R ising or F alling Data Enable ²		JP6
DUAL	DUAL /single mode		JP7

¹ An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.

See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

² In Balanced Mode (New Mode), R_FDE pin (pin 21) MUST be set to HIGH if DE signal (pin 56) is HIGH during active data. R_FDE pin must set to LOW when DE signal is LOW during active data.

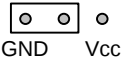
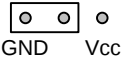
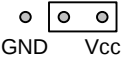
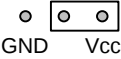
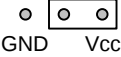
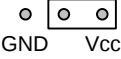
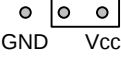
Note:

- A) In the single pixel mode, only TxOUT0 through TxOUT3 (LVDS channels A0-A3) and their associated inputs are active. TxOUT4 through TxOUT7 and their associated inputs and CLK2 are disabled for power savings.

18-bit or 24-bit Dual Pixel (New Mode)

The jumper settings below are for New Mode, Dual to Dual pixel application.

For Tx Board: (The Rx board jumper settings in this application is the same as the Rx Board Jumper Default Settings on page 17 except the BAL pin(JP6), which must be set to Vcc.)

<u>Jumper Name</u>	<u>Purpose</u>	<u>Settings</u>	<u>Jumper Number</u>
PRE	PRE -Emphasis ¹	 GND Vcc	JP1
R_FB	R ising or F alling data strobe	 GND Vcc	JP2
/PD	P ower D own	 GND Vcc	JP3
BAL	DC B ALance	 GND Vcc	JP4
PLLSEL	PLL SE lect (auto-range)	 GND Vcc	JP5
R_FDE	R ising or F alling D ata E nable ²	 GND Vcc	JP6
DUAL	D UAL/single mode	 GND Vcc	JP7

¹ An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.

See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

² In Balanced Mode (New Mode), R_FDE pin (pin 21) MUST set to HIGH if DE signal (pin 56) is HIGH during active data. R_FDE pin must set to LOW when DE signal is LOW during active data.

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to common problems. If the problem persists, contact the hotline number listed under Additional Information section of this document.

Check the following:

1. Power and Ground are connected to both Tx AND Rx boards.
2. Supply voltage (typical 3.3V) and current (It's around 200mA with clock and one data bit at 66MHz.) are correct.
3. Input clock and input data (It's best to start with one data bit.) to the Tx board.
4. Jumpers are set correctly or to default settings.
5. The 2 meter cable is connecting the Tx and Rx boards.
6. Make sure all of the connections are good.
7. Start with a low clock frequency (40 or 66 MHz) and work from there.

Trouble shooting chart:

Problem...	Solution...
There is only the output clock. There is no output data.	Make sure the data scramble/mapping is correct. Make sure there is data input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the 2 meter cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure the devices are enabled (/PD=ON) for operation.
The devices are pulling more than 1A of current.	Check for shorts on the demo boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards.

Additional Information

For more information on FPD-Link Transmitters/Receivers, refer to the National Semiconductor URL: <http://www.national.com/appinfo/lvds>

Application Notes

- AN-971 An Overview of LVDS technology
- AN-1032 An Introduction to FPD-Link
- AN-1127 LVDS Display Interface TFT Data Mapping for Interoperability with FPD-Link
- AN-1163 TFT Data Mapping for Dual Pixel LDI Application - Alternate A - Color Map
- AN-1085 FPD-Link PCB and Interconnect Design-In Guidelines
- AN-977 LVDS Signal Quality: Jitter measurement using Eye pattern
- AN-1056 STN Application using FPD-Link
- AN-1059 High Speed Transmission with LVDS Devices

Open LVDS Display Interface (OpenLDI) Specification:
<http://www.national.com/appinfo/fpd/0,2132,228,00.html>

SID'99 LDI Paper:
http://www.national.com/appinfo/fpd/files/LDI_SID.pdf

Information also available on the Internet:
<http://www.national.com/apnotes/Analog-FlatPanelDisplay.html>
<http://www.national.com/appinfo/fpd/>

Interface Hotline:

The Interface Hotline number is: (408) 721-8500

3M 26-Mini D Ribbon cable and connector

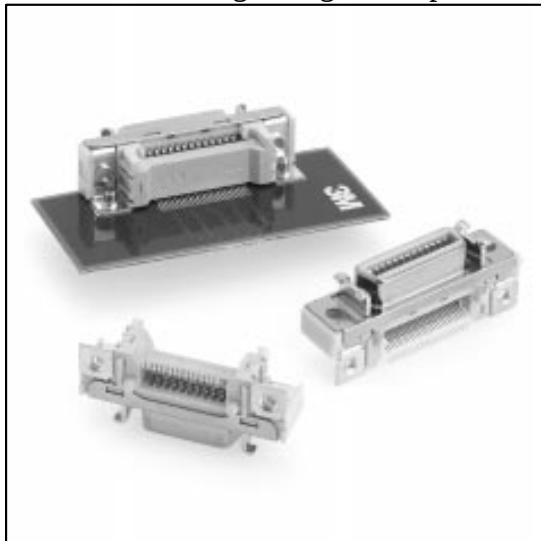
The next few pages provide a full description of the cable and connector. For product request please contact 3M.

3M Cable and Connector Data is available at: <http://www.mmm.com/Interconnects>

.050" Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded

102XX-1210VE Series



- Surface mount right angle shielded I/O receptacle
- MDR digital LCD interface — 20 and 26 position
- Ultra-low signal skew design for high data rate transmission
- Ribbon type contact — industry preferred
- Reliable repetitive plugging/unplugging
- Latch design for easy use
- Positions: 14, 20, 26, 40 and 50

Date Modified: August 2, 1999

TS-0755-06
Sheet 1 of 3

8

Physical

Insulation

Material: Glass Reinforced Polyester (PCT)
 Flammability: UL 94V-0
 Color: Beige

Contact

Material: Copper Alloy (C521)
 Plating
 Underplate: 80 μ " [2.0 μ m] Nickel — QQ-N-290, Class 2
 Wiping Area: 20 μ " [0.50 μ m] Min Gold — MIL-G-45204, Type II, Grade C

Shroud and Latch Hook

Material: Steel
 Plating: Nickel

Screw Lock

Material: Copper Alloy (C521)
 Plating: Tin

Marking: 3M Logo and Part Number

Electrical

Current Rating: 1 A
Insulation Resistance: $> 5 \times 10^8 \Omega$ at 500 VDC
Withstanding Voltage: 500 Vrms for 1 Minute

3M Interconnect Solutions Division

6801 River Place Blvd.
 Austin, TX 78726-9000

For technical, sales or ordering information call
800-225-5373

National Semiconductor Corporation
 Interface Products

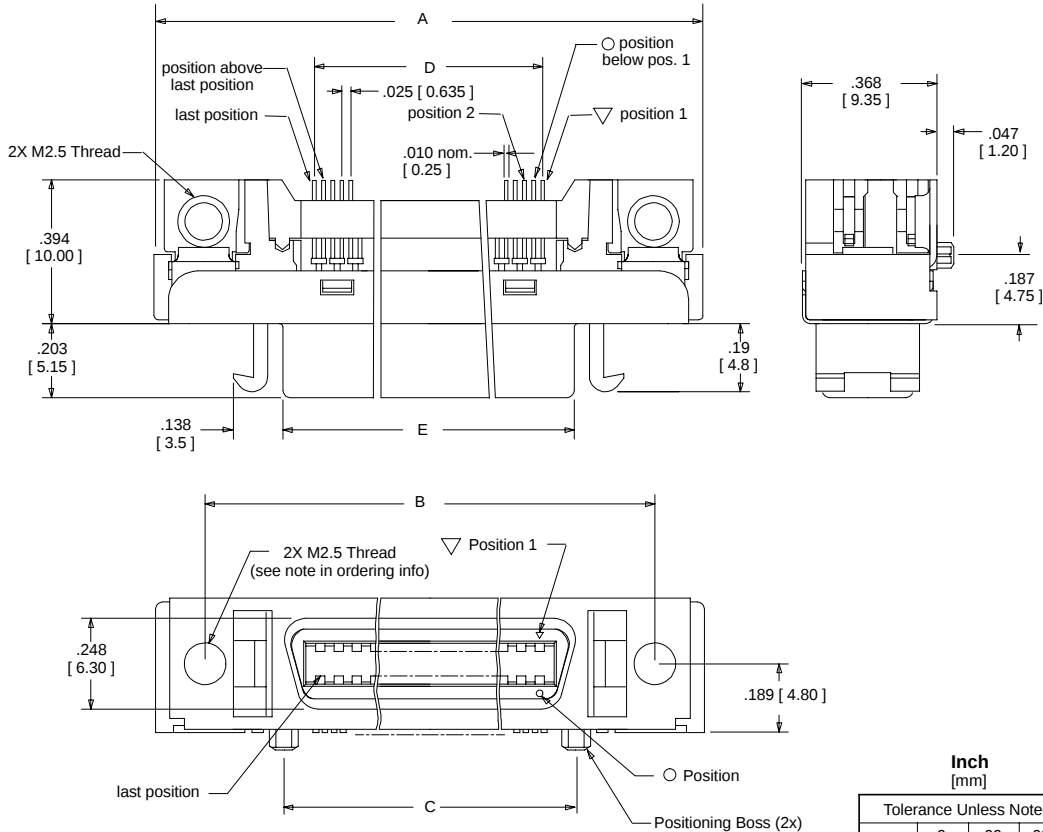
LIT# LDI3V8BT-112-UM
 Date 04/04/01
 Page 29 of 34

.050" Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded

102XX-1210VE Series

Contact Quantity	3M Part Number	Dimensions				
		A±.008	B±.006	C±.006	D±.006	E±.006
14	10214-1210 VE	1.16 [29.5]	.93 [23.64]	.47 [12.70]	.33 [8.26]	.50 [12.6]
20	10220-1210 VE	1.32 [33.4]	1.081 [27.45]	.650 [16.51]	.475 [12.07]	.646 [16.4]
26	10226-1210 VE	1.50 [38.2]	1.231 [31.26]	.800 [20.32]	.625 [15.88]	.795 [20.2]
40	10240-1210 VE	1.85 [47.1]	1.581 [40.15]	1.150 [29.21]	.975 [24.77]	1.150 [29.2]
50	10250-1210 VE	2.06 [52.4]	1.831 [46.50]	1.400 [35.56]	1.225 [31.12]	1.40 [35.5]



Ordering Information

102XX-1210VE

Contact Quantity
(See Table)

Note: Use (M2.5x8mm) screws to mount to panel with max. thickness of 2.0 mm.

TS-0755-06
Sheet 2 of 3

3M Interconnect Solutions Division

6801 River Place Blvd.
Austin, TX 78726-9000

For technical, sales or ordering information call
800-225-5373

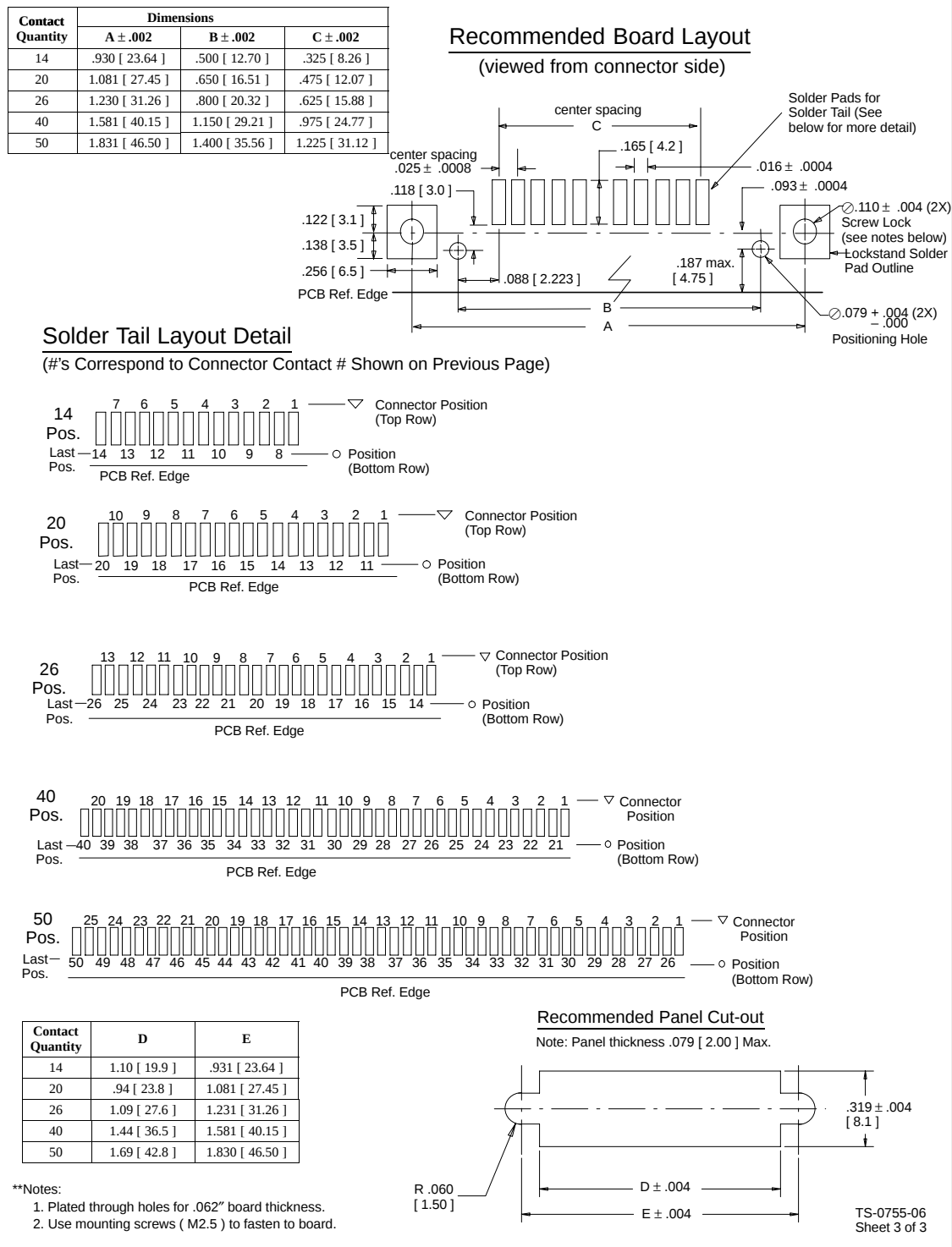
National Semiconductor Corporation
Interface Products

LIT# LDI3V8BT-112-UM
Date 04/04/01
Page 30 of 34

.050" Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded

102XX-1210VE Series



3M Interconnect Solutions Division

6801 River Place Blvd.
Austin, TX 78726-9000

For technical, sales or ordering information call
800-225-5373

National Semiconductor Corporation
Interface Products

LIT# LDI3V8BT-112-UM
Date 04/04/01
Page 31 of 34

.050" Mini D Ribbon (MDR) Cable Assembly

High Speed Digital Data Transmission System — 26 Position

14526-EZHB-XXX-0QC



- 10 shielded pairs plus 4 individual wires
- The solution for high speed datacom and telecom applications
- Each differential pair is shielded with foil; entire cable bundle is shielded with foil and braid
- Rugged MDR ribbon type contact
- Quick release latches

Date Modified: February 23, 2000

TS-0891-05
Sheet 1 of 3

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Physical

Connector Contact Plating

Wiping Area: 30μ" [0.76μm] Min. Gold

Shell

Color: Parchment/Beige

Material: Acrylonitrile Butadiene Styrene (ABS)

Cable

Color: Parchment/Beige

Jacket Material: Polyvinyl Chloride (PVC)

Flammability: AWM VW-1

Electrical

Voltage Rating: 30 V**Current Rating:** 1 A**Insulation Resistance:** $> 1 \times 10^8 \Omega$ at @100 Vdc**Withstanding Voltage:** 350 Vrms for 1 minute

Individually Shielded Twisted Pairs

Characteristic Impedance: $100 \pm 10 \Omega$ (USB 90Ω)**Conductor Size:** 28 AWG Stranded**Propagation Velocity:** 1.25 ns/ft [4.1 ns/m]

Environmental

Temperature Rating: -20°C to +75°C

UL File No.: E86982

3M Interconnect Solutions Division

6801 River Place Blvd.
Austin, TX 78726-9000For technical, sales or ordering information call
800-225-5373National Semiconductor Corporation
Interface ProductsLIT# LDI3V8BT-112-UM
Date 04/04/01
Page 32 of 34

3M - Preliminary LDI CableRev A
3/3/99**Assembly Specification**

Cable: v24.0

Connector: Plug type 10126-6000

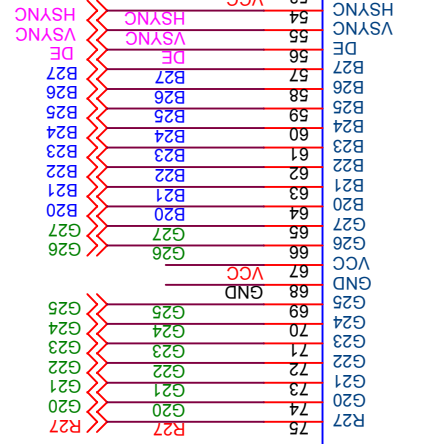
D26-1 wiring diagram for cable assembly and board layout**MDR 26 position right angle surface mount receptacle 10226-1210 VE**

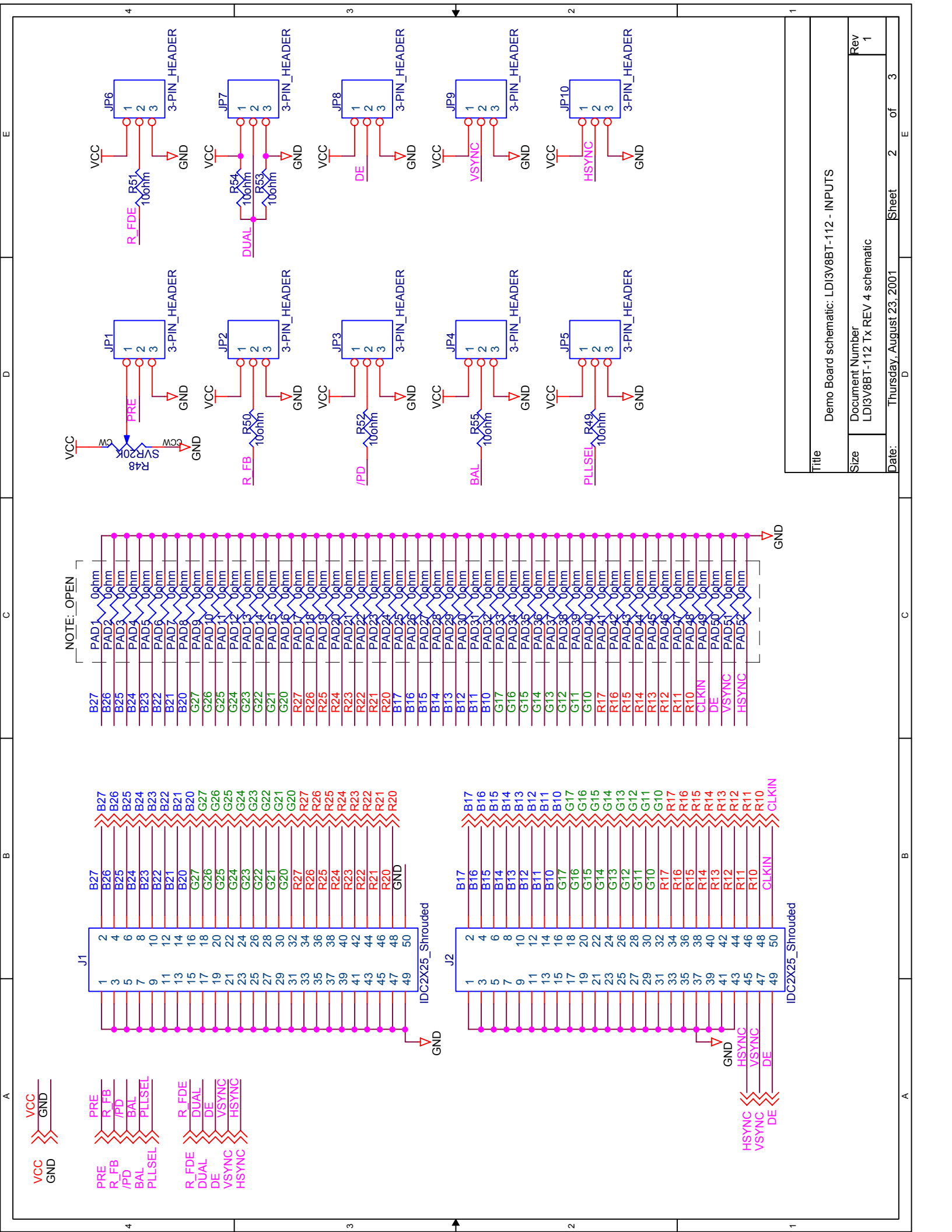
Note: "pad" column represents actual position of solder pad on board layout.

"pin #" column specifies corresponding receptacle contact #.

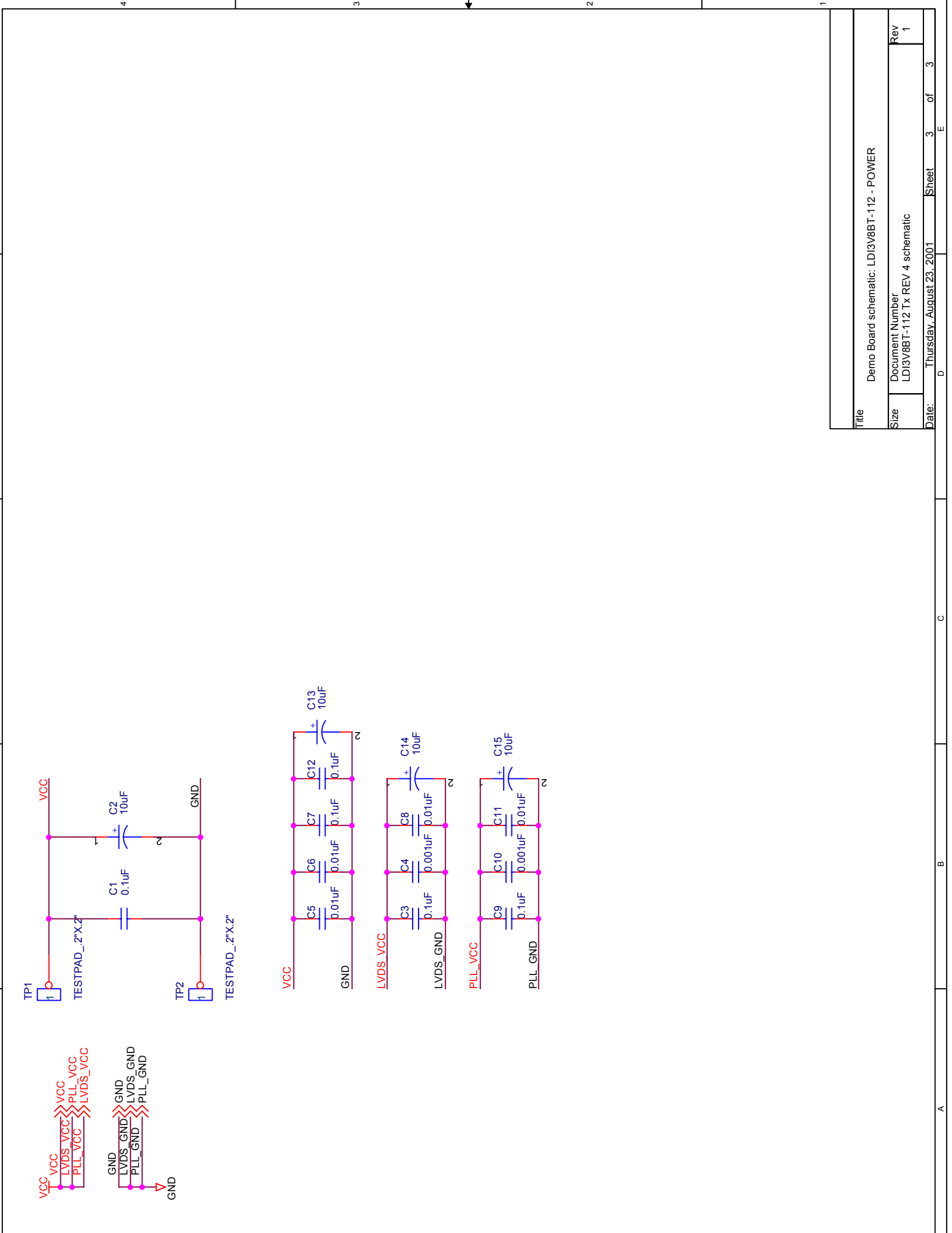
**** Note: Temporary pinout for LDI testing purposes only.****Transmitter-387
pin #**Transmitter receptacle**
pad pin # signal type**Cable Assembly****Receiver receptacle**
signal type pin # padReceiver-388
pin #

		1	Extra 1			LVDS gnd	26		
		14	Extra 2			A7P	13		79
		2	Extra 3			A7M	25		80
50		15	A0M			A6P	12		82
49		3	A0P			A6M	24		83
47		16	A1M			A5P	11		84
46		4	A1P			A5M	23		85
45		17	A2M			A4P	10		86
44		5	A2P			A4M	22		87
42		18	CLK1M			A3P	9		89
41		6	CLK1P			A3M	21		90
		19	Control 1			Control 4	8		
		7	Control 2			Control 3	20		
		20	Control 3			Control 2	7		
		8	Control 4			Control 1	19		
39		21	A3M			CLK1P	6		91
38		9	A3P			CLK1M	18		92
37		22	A4M			A2P	5		94
36		10	A4P			A2M	17		95
34		23	A5M			A1P	4		96
33		11	A5P			A1M	16		97
32		24	A6M			A0P	3		98
31		12	A6P			A0M	15		99
29		25	A7M			Extra 3	2		
28		13	A7P			Extra 2	14		
		26	LVDS gnd			Extra 1	1		





Title			Demo Board schematic: LD13V8BT-112 - INPUTS		
Size	Document Number		LD13V8BT-112 Tx Rev 4 schematic		
	Rev		1		
Date:		Thursday, August 23, 2001	Sheet	2	of 3

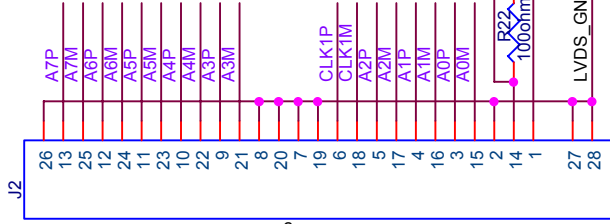
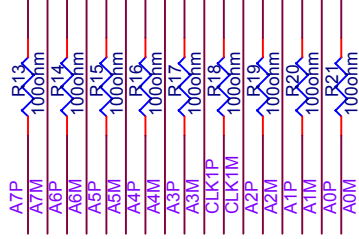


Title			Demo Board schematic: LD13V8BT-112 - POWER		
Size	Document Number		LD13V8BT-112 Tx REV 4 schematic		
	Rev		1		
Date:		Thursday, August 23, 2001	Sheet	3	of 3

VCC
LVDS_VCC
PLL_VCC

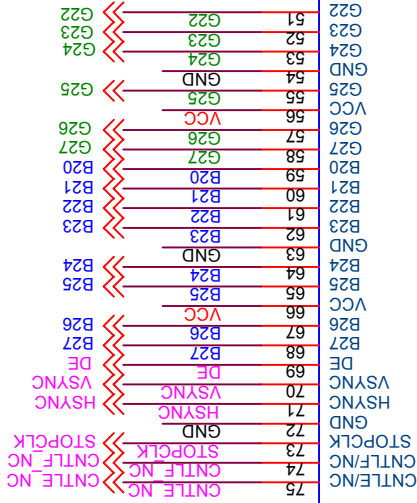
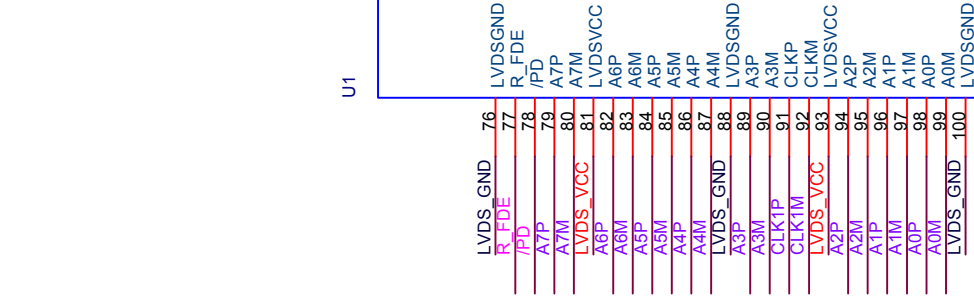
GND
LVDS_GND
PLL_GND

NOTE: MOUNT TERMINATION
RESISTORS NEXT TO DEVICE

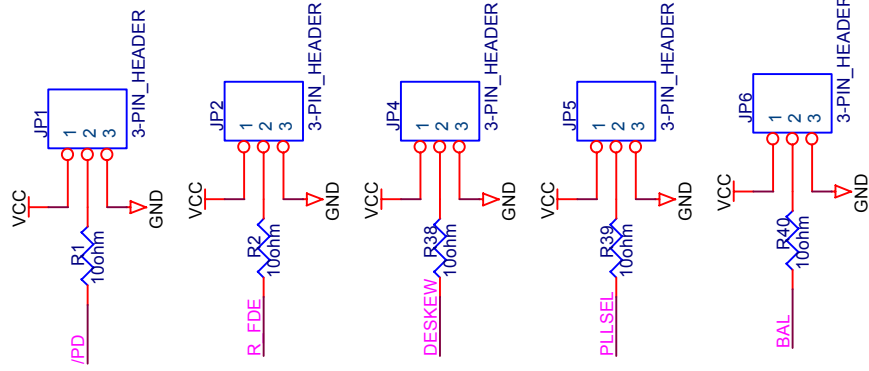
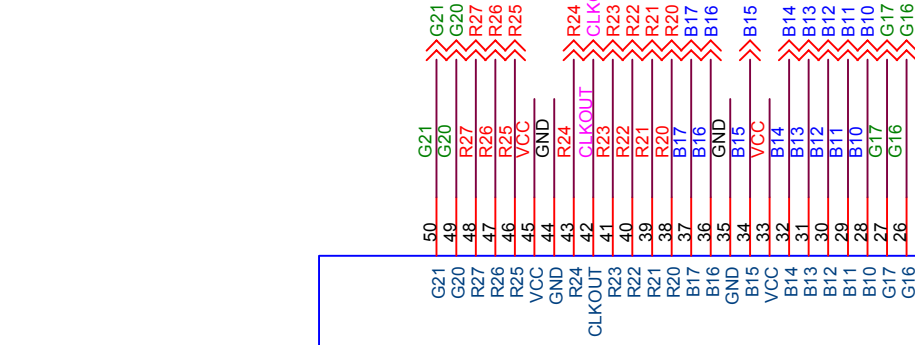
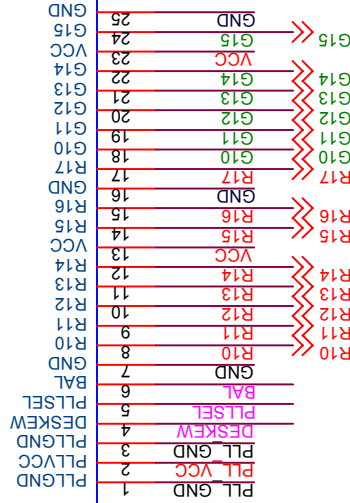


26 position

NOTE: Pins 27 and 28 ties the Screw Lock to ground



DS90CF388



Thursday, September 06, 2001 Sheet

