# ispDesignExpert Tutorial

*Version 8.0*

*Technical Support Line:* 1-800-LATTICE or (408) 732-0555
DE-TUT Rev 8.0.1

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December 1999

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# Table of Contents

# Part I: Introduction to ispDesignExpert

# Tutorial 1 ispDesignExpert ispLSI Design Basics

This tutorial provides an overview of the features and operation of ispDesignExpert for ispLSI designs, focusing on the Project Navigator to complete a programmable device design.

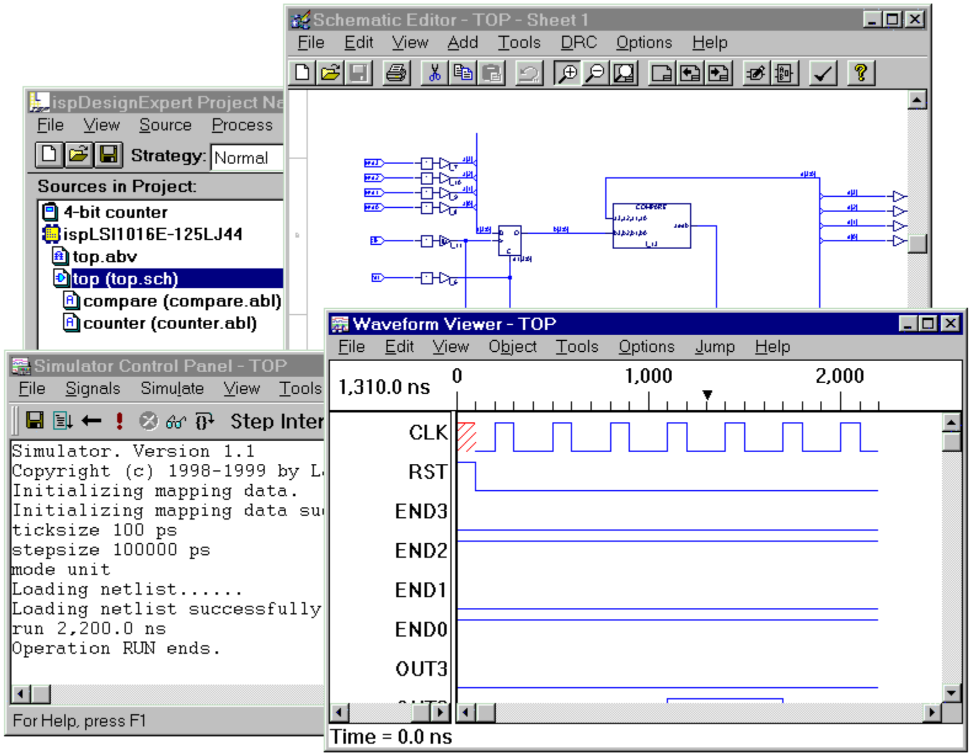
Follow the steps in this tutorial to implement a design using a mixture of schematics and ABEL-HDL.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of the steps and tools necessary to complete an ispLSI design using ispDesignExpert.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.



```
Simulator. Version 1.1
Copyright (c) 1998-1999 by L
Initializing mapping data.
Initializing mapping data su
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully
run 2,200.0 ns
Operation RUN ends.
```

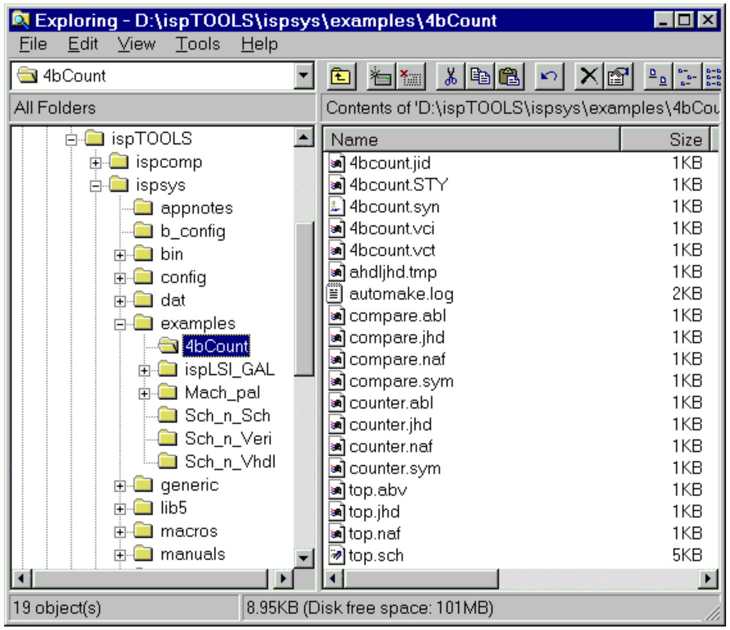
# Task 1 *Create a Project Directory*

ispDesignExpert employs the concept of a project. Source files, such as behavioral and schematic logic descriptions, device type, and design documentation, intermediate data files, and output files, of a project can be stored in one directory.

However, it is recommended that each project has its own directory for storing source files.

*To create a project directory:*

1. Start Windows Explorer, or similar tool.
2. Go to the `\ispTOOLS\ispsys\examples\ispLSI_GAL` directory.
3. In Explorer, create the directory `4bCount`.



Exploring - D:\ispTOOLS\ispsys\examples\4bCount

Contents of 'D:\ispTOOLS\ispsys\examples\4bCou

| Name | Size |
|---|---|
| 4bcount.jid | 1KB |
| 4bcount.STY | 1KB |
| 4bcount.syn | 1KB |
| 4bcount.vci | 1KB |
| 4bcount.vct | 1KB |
| ahdljhd.tmp | 1KB |
| automake.log | 2KB |
| compare.abl | 1KB |
| compare.jhd | 1KB |
| compare.naf | 1KB |
| compare.sym | 1KB |
| counter.abl | 1KB |
| counter.jhd | 1KB |
| counter.naf | 1KB |
| counter.sym | 1KB |
| top.abv | 1KB |
| top.jhd | 1KB |
| top.naf | 1KB |
| top.sch | 5KB |

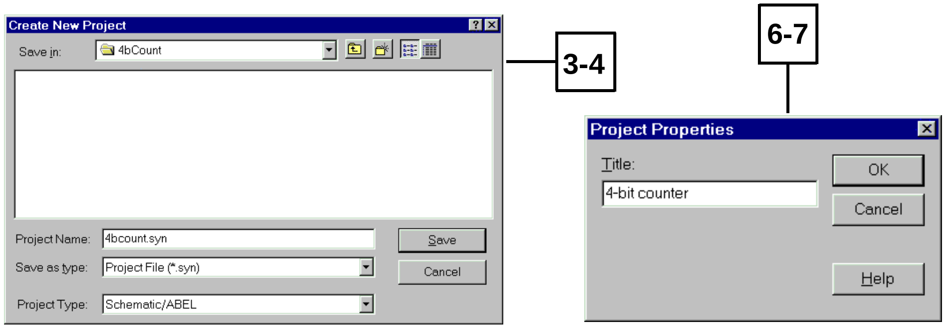
19 object(s) 8.95KB (Disk free space: 101MB)

# Task 2 *Create a New Project*

Now you need to select the project type and name the project file (`.syn`) that the Project Navigator will use later to reload the project.

*To create a new project*:

1. Start ispDesignExpert if it is not already running.
2. Choose **File** ⇒ **New Project** to open the Create New Project dialog box.
3. In this dialog box, change the directory to `\ispTOOLS\ispsys\examples\ispLSI_GAL\4bCount`.
4. Select Schematic/ABEL from the Project Type field. The default project name is `Untitled.syn`. Type `4bcount` as the project name for this tutorial project.
5. Click **Save**. The untitled project appears in the Sources window of the Project Navigator.
6. In the Sources window, double-click the title of the project (Untitled) to open the Project Properties dialog box.
7. Type in `4-bit counter` as your project title.
8. Click **OK**. The new project title appears in the Sources window.



Create New Project

Save in: 4bCount

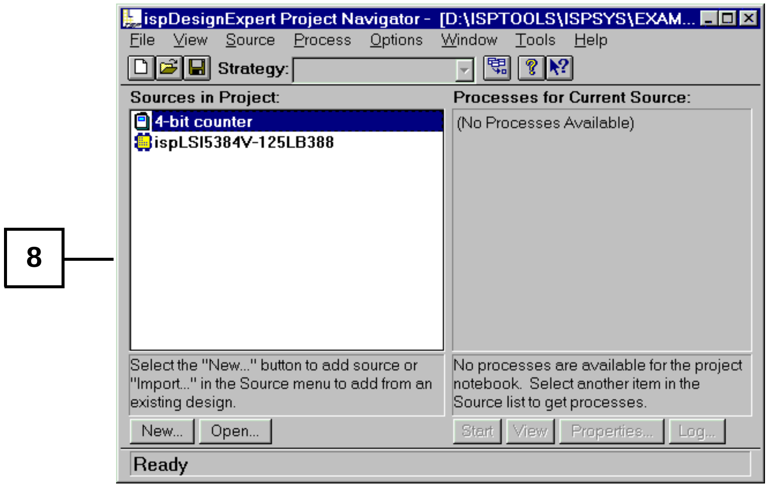
Project Name: 4bcount.syn

Save as type: Project File (*.syn)

Project Type: Schematic/ABEL

Project Properties

Title: 4-bit counter



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAM...

Sources in Project:

4-bit counter
ispLSI5384V-125LB388

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

# Task 3 *Select a Device*

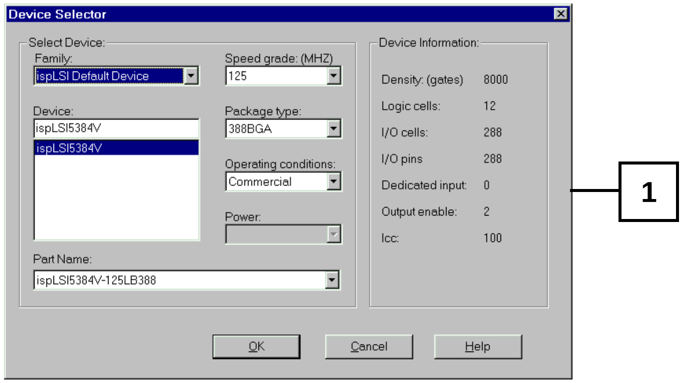
Below the Project Notebook is the device icon that identifies the target device for the project. The Project Navigator lets you target a design to a specific Lattice device at any time during the design process.

*To view the list of available devices and to change the target device*:

1. In the Sources window, double-click the **Device** icon to open the Device Selector dialog. The dialog box shows the default device.
2. In the Device Selector dialog box, select the ispLSI 1K device family.
3. Select the ispLSI1016E-125LJ44 device.
4. Accept the default settings and then click **OK**.
5. The Confirm Change dialog box appears. Click **Yes** to confirm that you wish to change device families.

   Notice that the process options changed after selecting the ispLSI device.

   When you change the target device, ispDesignExpert design environment reconfigures to facilitate designing with the selected device family.

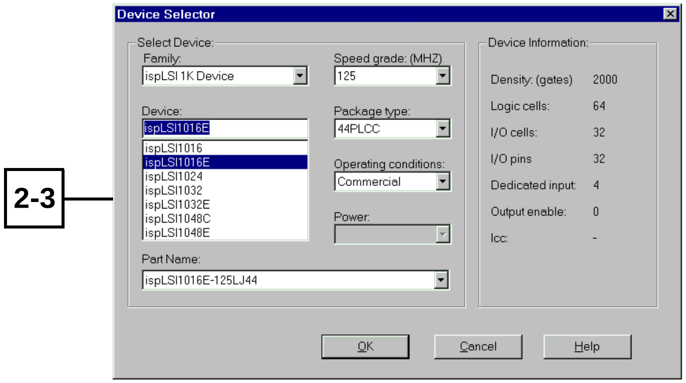


Device Selector

Select Device:
Family: ispLSI Default Device
Speed grade: (MHZ) 125
Device: ispLSI5384V
ispLSI5384V
Package type: 388BGA
Operating conditions: Commercial
Power:
Part Name: ispLSI5384V-125LB388

Device Information:

| | |
|---|---|
| Density: (gates) | 8000 |
| Logic cells: | 12 |
| I/O cells: | 288 |
| I/O pins | 288 |
| Dedicated input: | 0 |
| Output enable: | 2 |
| Icc: | 100 |

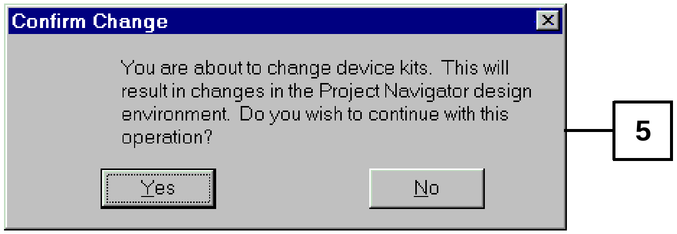


Device Selector

Select Device:
Family: ispLSI 1K Device
Speed grade: (MHZ) 125
Device: ispLSI1016E
ispLSI1016
ispLSI1016E
ispLSI1024
ispLSI1032
ispLSI1032E
ispLSI1048C
ispLSI1048E
Package type: 44PLCC
Operating conditions: Commercial
Power:
Part Name: ispLSI1016E-125LJ44

Device Information:

| | |
|---|---|
| Density: (gates) | 2000 |
| Logic cells: | 64 |
| I/O cells: | 32 |
| I/O pins | 32 |
| Dedicated input: | 4 |
| Output enable: | 0 |
| Icc: | - |



Confirm Change

You are about to change device kits. This will result in changes in the Project Navigator design environment. Do you wish to continue with this operation?

# Task 4 *Create and Import a Design Documentation File*

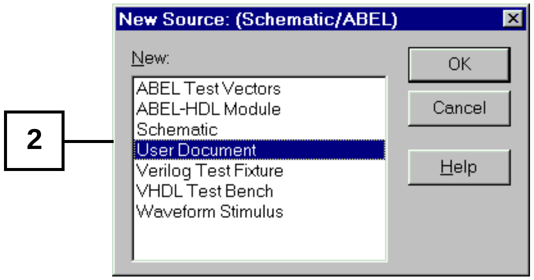
The Project Notebook works much like an engineering notebook. You can give it any name to describe your project. In addition, you can include files created by Windows applications other than ispDesignExpert. For instance, you might want to include a project schedule, a specification document, or a timing diagram.

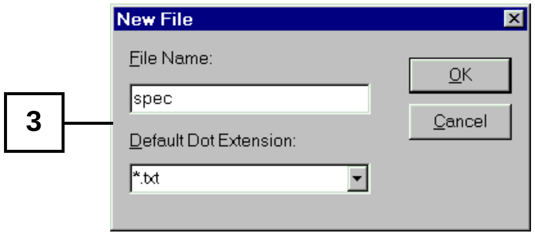
*To create a text document and import it into the Project Notebook*:

1. Choose **Source** ⇒ **New**.
2. In the New Source dialog, select User Document, and then click **OK**.
3. In the New File dialog, type `spec` in the File Name field. Then click **OK**.
4. In the Text Editor, type `This is a sample text document`.
5. Choose **File** ⇒ **Save**.

   ispDesignExpert automatically adds the file to the Sources window, under the Project Notebook.
6. Choose **File** ⇒ **Exit** to close the Text Editor.

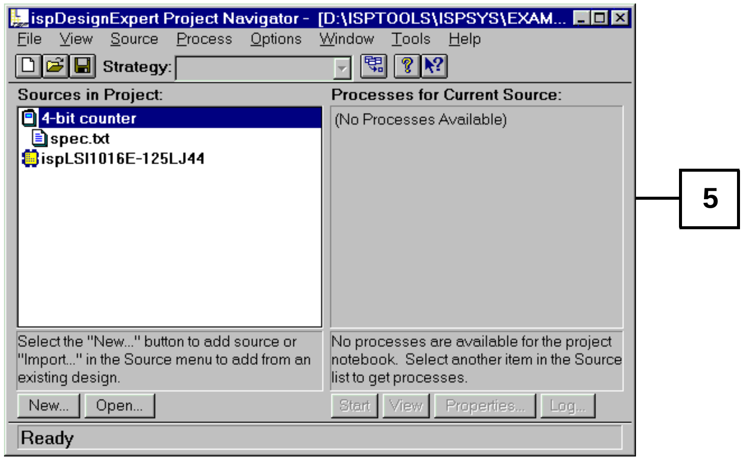
***Note:** You can add logic source files (for example, schematics and ABEL-HDL files) in the same way, although they appear in a different place in the Sources window. The Project Notebook area is for non-design source files.*





File Name: spec

Default Dot Extension: *.txt



Sources in Project:

4-bit counter
spec.txt
ispLSI1016E-125LJ44

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

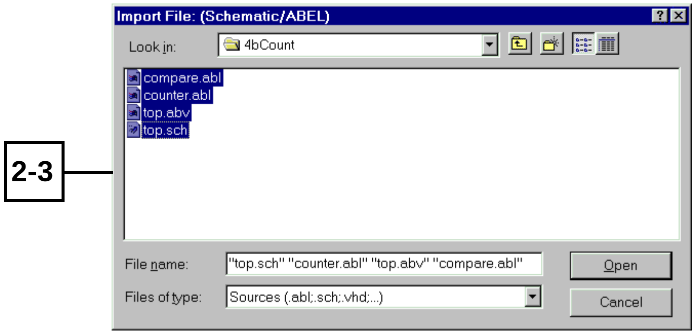
# Task 5 *Import Existing Source Files*

To save time in this tutorial, you will import existing source files. Although, in a practical sense, you will probably have existing sources that you will want to import into a design in addition to creating new ones.

*To import existing source files:*

1. Select **Source** ⇒ **Import** from the Project Navigator.
2. The Import File dialog box appears. You can double check your project type (Schematic/ ABEL) from the title bar of this dialog box.
3. Browse to change the directory to `ispTools/ ispsys\examples\MACH_PAL\ tutorial\Tutor4\4bCount`.
4. Select all the source files and click **Open**.
5. The Project Navigator should now look like the image shown to the right.

   A project contains all the source files for the design, such as schematic logic descriptions, ABEL-HDL file, test vector, device type, and design documentation.



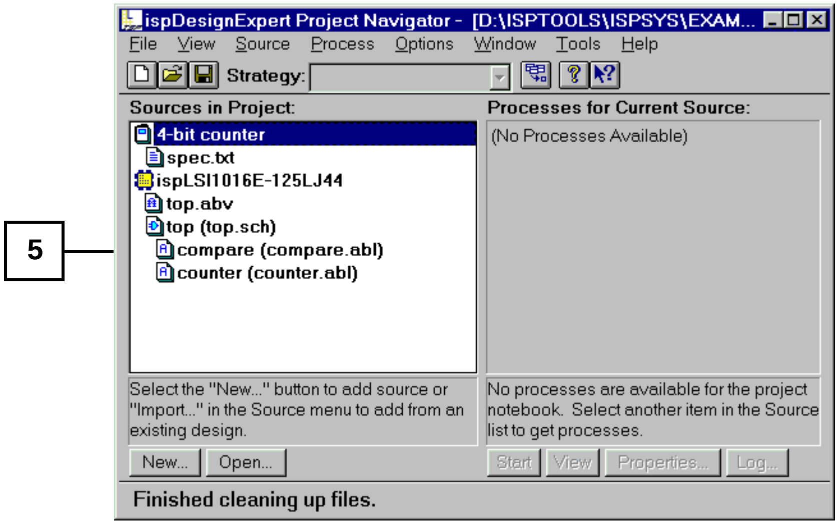
Import File: (Schematic/ABEL)

Look in: 4bCount

compare.abl
counter.abl
top.abv
top.sch

File name: "top.sch" "counter.abl" "top.abv" "compare.abl"

Files of type: Sources (.abl;.sch;.vhd;...)



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAM...

Strategy:

Sources in Project:

4-bit counter
spec.txt
ispLSI1016E-125LJ44
top.abv
top (top.sch)
compare (compare.abl)
counter (counter.abl)

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Finished cleaning up files.

# Task 6 *About the Project Navigator Interface*

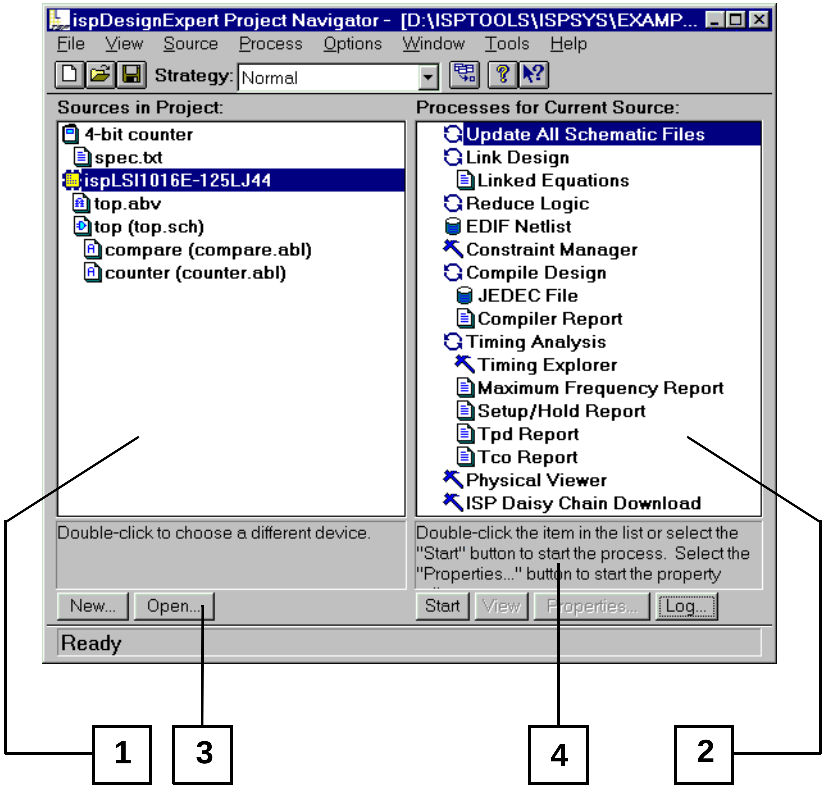
The Project Navigator has two primary interface elements: the Sources window and the Processes window.

The Sources window (**1**) shows all the design files associated with a project, listed in their logical, hierarchical order. Each source in the list is identified with an icon.

The Processes window (**2**) shows all the processing tasks that apply to a selected source in the Sources window. Typical programmable device processing tasks include netlisting, compiling, logic reduction, logic synthesis, fitting, and simulation model building.

Buttons at the bottom of the Project Navigator (**3**) provide quick command access to key functions.

There are also two message areas (**4**) located above and below these buttons.



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMP...

Strategy: Normal

Sources in Project:

- 4-bit counter
  - spec.txt
- ispLSI1016E-125LJ44
  - top.abv
  - top (top.sch)
    - compare (compare.abl)
    - counter (counter.abl)

Processes for Current Source:

- Update All Schematic Files
- Link Design
  - Linked Equations
- Reduce Logic
- EDIF Netlist
- Constraint Manager
- Compile Design
  - JEDEC File
  - Compiler Report
- Timing Analysis
  - Timing Explorer
  - Maximum Frequency Report
  - Setup/Hold Report
  - Tpd Report
  - Tco Report
- Physical Viewer
- ISP Daisy Chain Download

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property

Ready

# Task 7 *Examine the Process Flows*

The Project Navigator is context sensitive — that is, it automatically adjusts the processes for you depending on what you want to do.

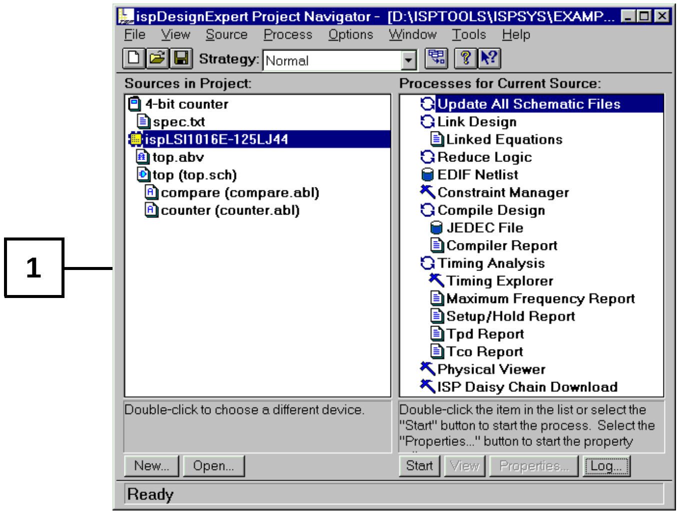
First, processes for a given file change depending on the target device. This is called the project-level flow. For instance, a design targeted for an ispLSI device is processed differently than a design targeted for a MACH or PAL device.

Second, the process flow changes depending on what type of source file is highlighted in the Sources window. This is called the source-level flow. For example, if you select a schematic source (`.sch`), several processes appear in the Processes window. But, if you select an ABEL test vector file (`.abv`), only the processes necessary for that source (functional simulation and timing simulation) are shown.

*Examine the process flows*:

1. To see the process-level flow, select the Device icon in the Sources window. The processes for the project appear in the Processes window.
2. To see a source-level flow, select a source. The processes for the selected source appear in the Processes window.

   Continue to select different sources and notice that the processes change in the Processes window.

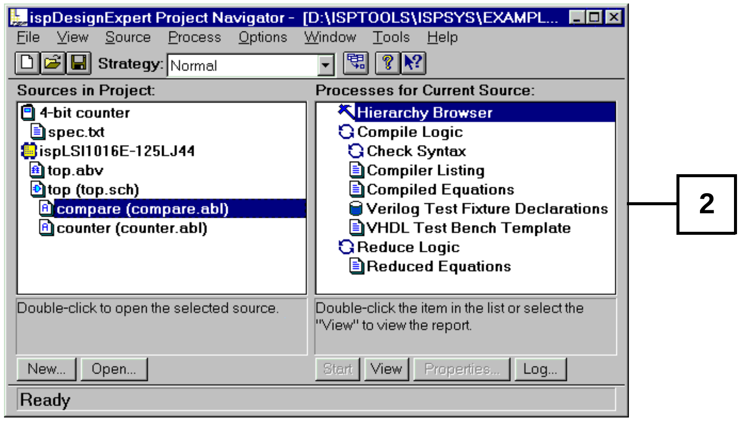

1
ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMP...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Processes for Current Source:
New... Open...
Start View Properties... Log...
Ready

4-bit counter
spec.txt
ispLSI1016E-125LJ44
top.abv
top (top.sch)
compare (compare.abl)
counter (counter.abl)

Update All Schematic Files
Link Design
Linked Equations
Reduce Logic
EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Timing Explorer
Maximum Frequency Report
Setup/Hold Report
Tpd Report
Tco Report
Physical Viewer
ISP Daisy Chain Download

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property


2
ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Processes for Current Source:
New... Open...
Start View Properties... Log...
Ready

4-bit counter
spec.txt
ispLSI1016E-125LJ44
top.abv
top (top.sch)
compare (compare.abl)
counter (counter.abl)

Hierarchy Browser
Compile Logic
Check Syntax
Compiler Listing
Compiled Equations
Verilog Test Fixture Declarations
VHDL Test Bench Template
Reduce Logic
Reduced Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

# Task 8 *Edit a Project Source*

You can edit project source files by double clicking the desired source in the Sources window. ispDesignExpert opens the appropriate editor with the selected source for editing.

In this task you will see how to open the Schematic Editor from a schematic source.

*To edit a schematic source file*:

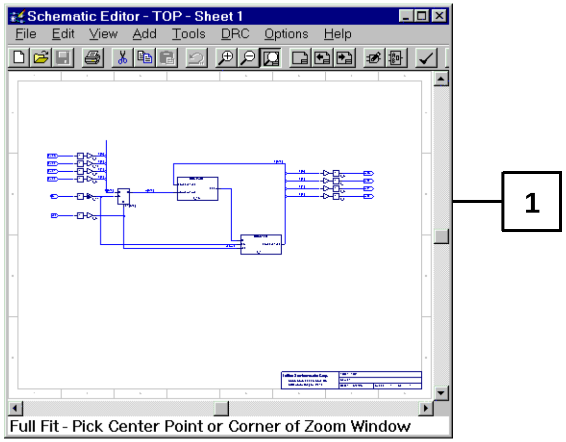
1. Double-click the top-level schematic `top` (`top.sch`) in the Sources window. The Schematic Editor opens with `top.sch`.

   When you double-click any source, ispDesignExpert automatically opens the application associated with that source file.

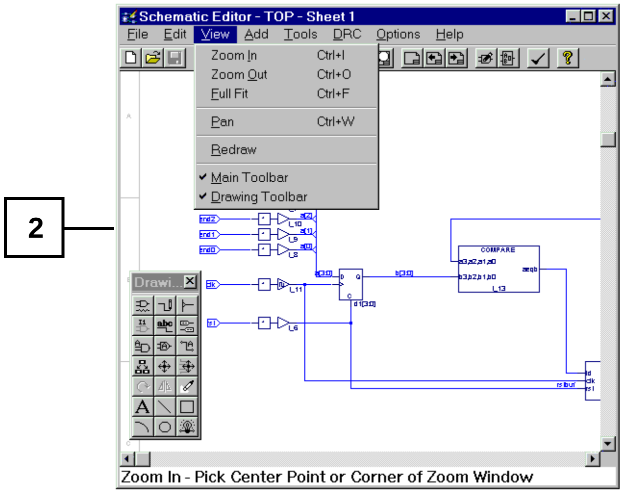
2. In the **View** menu, make sure that there is a check mark beside the **Main Toolbar** and **Drawing Toolbar** commands. (Click the command to toggle the check mark.) You can then edit the schematic.

3. Choose **File** ⇒ **Exit** to exit the Schematic Editor.

***Note:*** *You can also open an ispDesignExpert application from the Project Navigator* ***Window*** *menu.*


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
1

Full Fit - Pick Center Point or Corner of Zoom Window



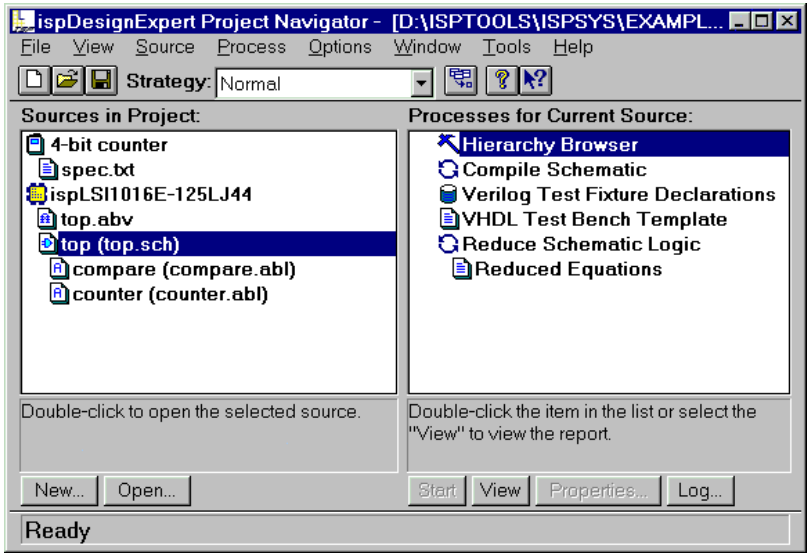
Zoom In - Pick Center Point or Corner of Zoom Window

# Task 9 *View the Design Hierarchy*

You can view the hierarchy of top-level and lower-level sources using the Hierarchy Browser. You select the top-level source in the Project Navigator and double-click the Hierarchy Browser process. The Hierarchy Browser will be opened together with the Hierarchy Navigator (if the source is a schematic) or with the HDL Viewer/Text Editor (if it is an HDL file). All the instances will be listed in the Hierarchy Browser.

With the Hierarchy Browser, you can traverse the design hierarchy by clicking on the displayed hierarchy tree and access a number of powerful database features, such as pushing into blocks to see the source they refer to, accessing connectivity information, and querying nets. If a relevant module of the selected instance is defined in a schematic source file, it will be opened in the Hierarchy Navigator. If a relevant module of the selected instance is defined in an HDL source file, it will be opened in the HDL Viewer/Text Editor.

***Note:*** *The Hierarchy Browser and Hierarchy Navigator are meant for viewing a design, not editing a design. For editing source files, use the Schematic Editor or Text Editor.*



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPL...

File View Source Process Options Window Tools Help
Strategy: Normal
New... Open...
Start View Properties... Log...

Sources in Project:

- 4-bit counter
  - spec.txt
- ispLSI1016E-125LJ44
  - top.abv
  - top (top.sch)
    - compare (compare.abl)
    - counter (counter.abl)

Processes for Current Source:

- Hierarchy Browser
- Compile Schematic
- Verilog Test Fixture Declarations
- VHDL Test Bench Template
- Reduce Schematic Logic
  - Reduced Equations

Double-click to open the selected source.

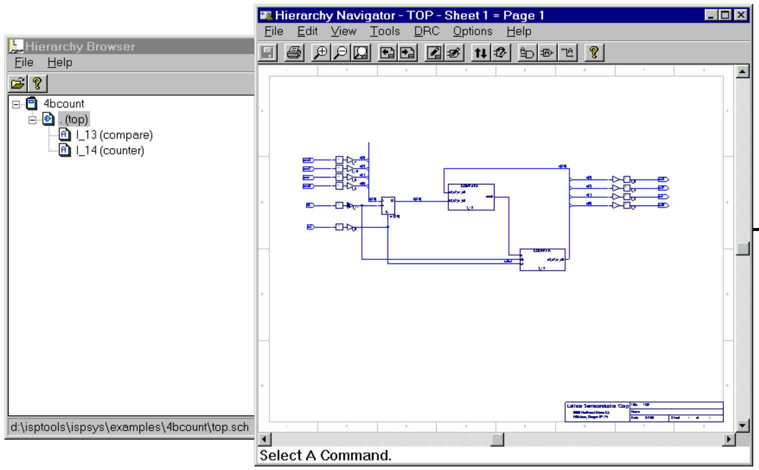
Double-click the item in the list or select the "View" to view the report.

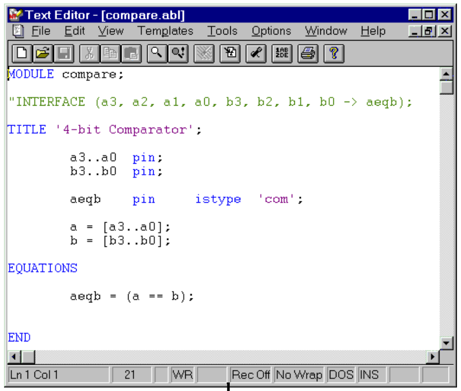
Ready

# View the Design Hierarchy (continued)

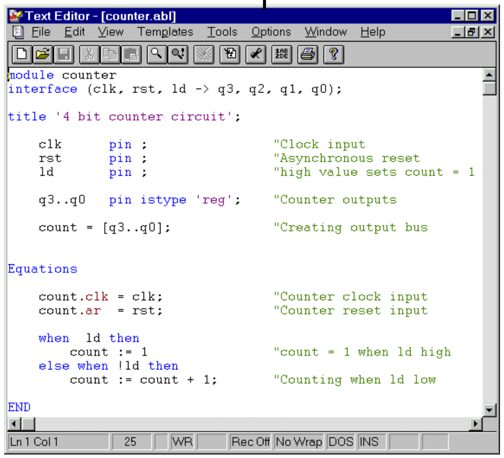
*To view the design hierarchy using the Hierarchy Browser and Hierarchy Navigator*:

1. Select the top-level schematic `top` in the Sources window and double-click the Hierarchy Browser process in the Processes window. The Hierarchy Browser opens with the hierarchy tree of the project and `top.sch` is opened in the Hierarchy Navigator.
2. The Hierarchy Browser lists all the sub-level sources in a tree format. You can expand the sources to the lowest-level instances.
3. Click the **Push/Pop** icon from the toolbar of the Hierarchy Navigator. The cursor changes to cross hairs. The **Push/Pop** command lets you "Push" down into a lower, more-detailed, level in the hierarchy or "Pop" up to a higher, less-detailed, level in the hierarchy.
4. Click inside the COMPARE block (upper-middle) to push down into the block. The Text Editor displays the contents for this block, which is an ABEL-HDL file.
5. Now click inside the COUNTER block. The Text Editor displays the ABEL-HDL source for this block. There is no more hierarchy in this schematic.
6. Choose **File** ⇒ **Exit** to close the Text Editor.
7. Choose **File** ⇒ **Exit** to close the Hierarchy Navigator.
8. Choose **File** ⇒ **Exit** to close the Hierarchy Browser.


Hierarchy Browser
File Help
4bcount
. (top)
I_13 (compare)
I_14 (counter)
d:\isptools\ispsys\examples\4bcount\top.sch
Hierarchy Navigator - TOP - Sheet 1 = Page 1
File Edit View Tools DRC Options Help
Select A Command.
1-2


Text Editor - [compare.abl]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
21
WR
Rec Off
No Wrap
DOS
INS
4

```
MODULE compare;

"INTERFACE (a3, a2, a1, a0, b3, b2, b1, b0 -> aeqb);

TITLE '4-bit Comparator';

        a3..a0  pin;
        b3..b0  pin;

        aeqb    pin     istype  'com';

        a = [a3..a0];
        b = [b3..b0];

EQUATIONS

        aeqb = (a == b);


END
```


5
Text Editor - [counter.abl]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
25
WR
Rec Off
No Wrap
DOS
INS

```
module counter
interface (clk, rst, ld -> q3, q2, q1, q0);

title '4 bit counter circuit';

    clk      pin ;                    "Clock input
    rst      pin ;                    "Asynchronous reset
    ld       pin ;                    "high value sets count = 1

    q3..q0   pin istype 'reg';        "Counter outputs

    count = [q3..q0];                 "Creating output bus


Equations

    count.clk = clk;                  "Counter clock input
    count.ar  = rst;                  "Counter reset input

    when  ld then
        count := 1                    "count = 1 when ld high
    else when !ld then
        count := count + 1;           "Counting when ld low

END
```

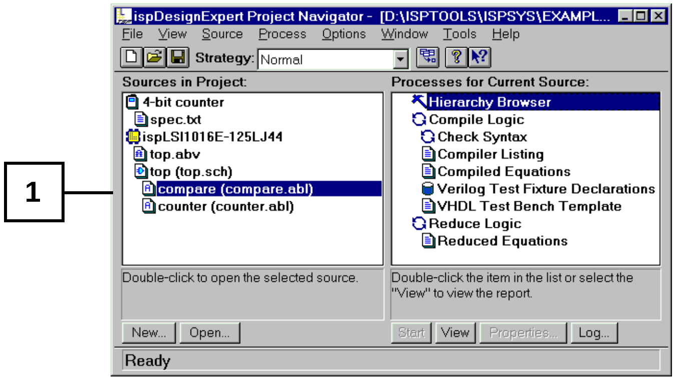
# Task 10 *Process a Module*

ispDesignExpert allows you to think less about the tools and steps involved in getting to a result and more about the desired result. For example, if you want to view a report, you do not have to figure out which processes should be run to generate the report. ispDesignExpert determines what steps are involved and runs them automatically. Because you intuitively know what results you want, ispDesignExpert's results-oriented processing greatly simplifies learning new architectures because it minimizes the impact of having to learn new tools and procedures.

*To process a module*:

1. In the Project Navigator Sources window, select the ABEL-HDL source `compare`. Notice that there is one process for this ABEL-HDL file (Compile Logic) that generates one report file (Compiled Equations).

   While you can run each process separately, it's faster and easier to tell ispDesignExpert what end result you want, and let ispDesignExpert determine which steps should be run in what order.

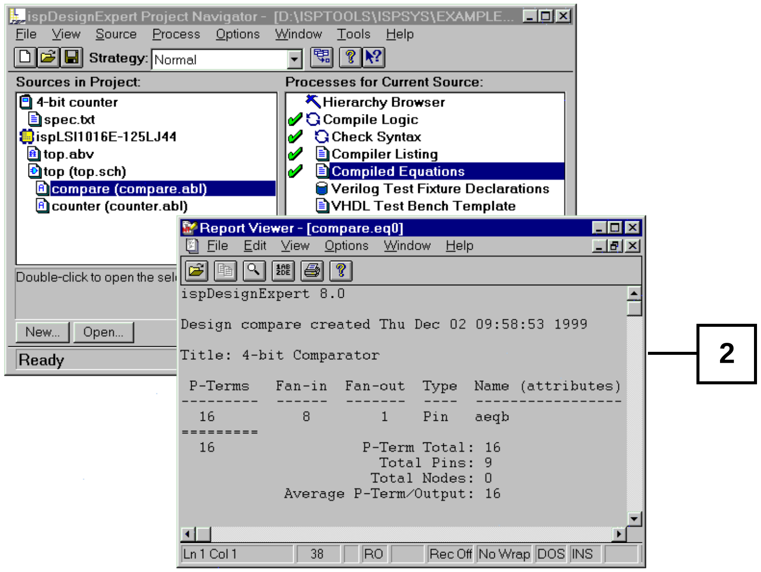


Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

2. In the Processes window, double-click the Compile Logic process. ispDesignExpert compiles the ABEL-HDL source. You can view the results in the Report Viewer by clicking **Log** button at the bottom of the Project Navigator or choosing **Process** ⇒ **Log**.

   The Processes window displays the status of each process as it runs.


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLE...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
4-bit counter
spec.txt
ispLSI1016E-125LJ44
top.abv
top (top.sch)
compare (compare.abl)
counter (counter.abl)
Processes for Current Source:
Hierarchy Browser
✓ Compile Logic
✓ Check Syntax
✓ Compiler Listing
✓ Compiled Equations
Verilog Test Fixture Declarations
VHDL Test Bench Template
New... Open...
Ready
Report Viewer - [compare.eq0]
File Edit View Options Window Help
Ln 1 Col 1 38 RO Rec Off No Wrap DOS INS
2

Double-click to open the sel

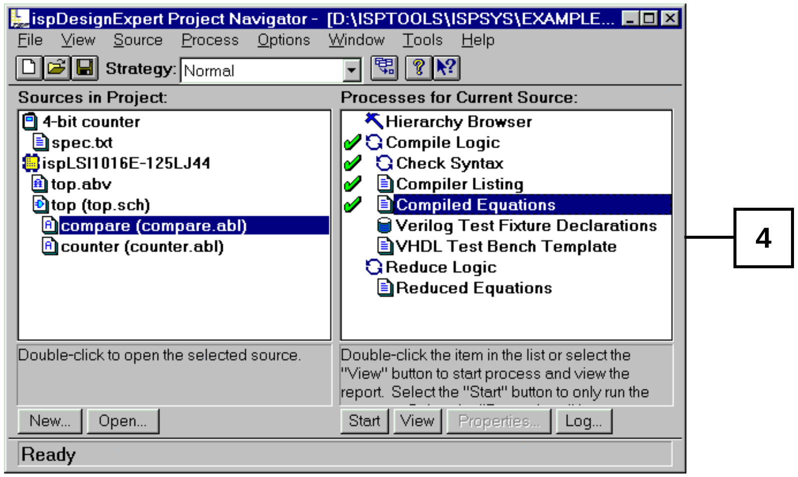
```
ispDesignExpert 8.0

Design compare created Thu Dec 02 09:58:53 1999

Title: 4-bit Comparator

 P-Terms   Fan-in  Fan-out  Type  Name (attributes)
---------  ------  -------  ----  -----------------
  16         8        1     Pin   aeqb
=========
  16                   P-Term Total: 16
                        Total Pins: 9
                       Total Nodes: 0
              Average P-Term/Output: 16
```

# Process a Module (continued)

3. Close the Report Viewer.
4. Look at the Processes window. Note that a green check mark has been added to the Compile Logic process that has been successfully completed.

***Note****: Yellow exclamation marks beside the process indicate that warnings were generated. Red Xs indicate that errors were encountered. The warning or error is described in the auto-make log file displayed in the Report Viewer. Green check marks indicate the process completed successfully.*

***Note****: The Processes window is constantly updated. If you edit a source file, the green check marks disappear for processes that were previously run.*



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLE...

Strategy: Normal

Sources in Project:

- 4-bit counter
- spec.txt
- ispLSI1016E-125LJ44
- top.abv
- top (top.sch)
- compare (compare.abl)
- counter (counter.abl)

Processes for Current Source:

- Hierarchy Browser
- ✓ Compile Logic
- ✓ Check Syntax
- ✓ Compiler Listing
- ✓ Compiled Equations
- Verilog Test Fixture Declarations
- VHDL Test Bench Template
- Reduce Logic
- Reduced Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" button to start process and view the report.  Select the "Start" button to only run the

Ready

# Task 11 *Run Functional Simulation*

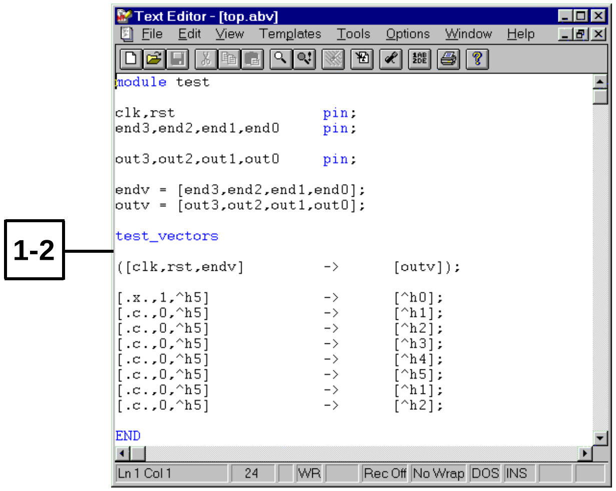
Functional simulation uses design test stimuli to simulate design logic or equations, independent of any device. The more comprehensive and detailed your test stimuli are, the more useful your simulation results will be.

The Lattice Logic Simulator accepts both graphic waveform stimulus and ABEL-HDL test vectors as the test stimulus. The Lattice Logic simulator applies the inputs from the test stimulus to the simulated circuit and compares the simulated output with the output specified in the test vectors. If there is any difference, the difference will be listed in the Simulator Control Panel or the Simulator Log.

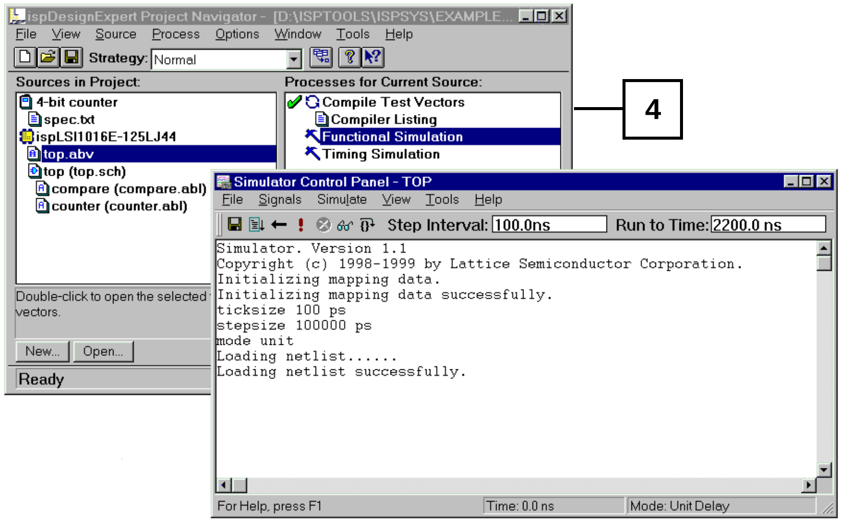
Functional simulation tests your design without using device-specific information. Therefore, functional simulation can be conducted before you select a device.

*To behaviorally simulate your design*:

1. In the Sources window, double-click `top.abv` to open the test vector file in the Text Editor.
2. Scroll the window and view the Test Vector section.
3. Close the file and exit the Text Editor.
4. In the Processes window, double-click the Functional Simulation process or click the **View** button at the bottom of the Project Navigator to launch the Simulator Control Panel.



```
module test

clk,rst                  pin;
end3,end2,end1,end0      pin;

out3,out2,out1,out0      pin;

endv = [end3,end2,end1,end0];
outv = [out3,out2,out1,out0];

test_vectors

([clk,rst,endv]          ->       [outv]);

[.x.,1,^h5]              ->       [^h0];
[.c.,0,^h5]              ->       [^h1];
[.c.,0,^h5]              ->       [^h2];
[.c.,0,^h5]              ->       [^h3];
[.c.,0,^h5]              ->       [^h4];
[.c.,0,^h5]              ->       [^h5];
[.c.,0,^h5]              ->       [^h1];
[.c.,0,^h5]              ->       [^h2];

END
```



```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
```

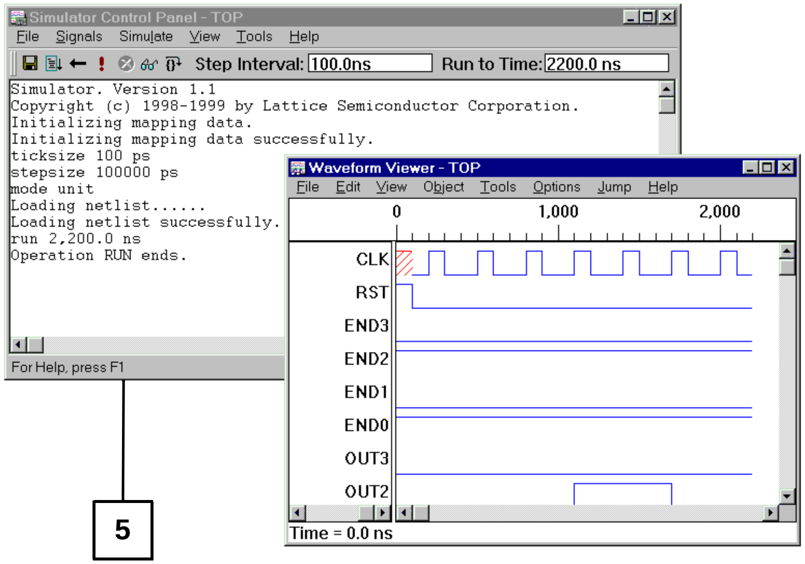
# Run Functional Simulation (continued)

The ispDesignExpert process dialog box appears momentarily. When this process is completed, the Simulator Control Panel is launched.

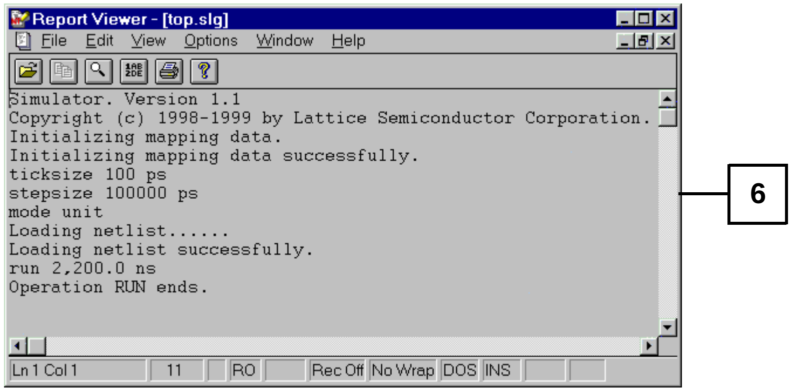
5. In the Simulator Control Panel, click the **Run** icon from the toolbar or choose the **Simulate** ⇒ **Run** menu item to start the simulation.

***Note**: Keep the **View** ⇒ **Show Waveforms** menu item checked in the Simulation Control Panel so that the Waveform Viewer will automatically be opened with the waveforms of the simulated signals.*

6. When the run ends, you can compare the functional simulation results with the expected values specified in the test vectors. If there is any difference between the simulation results and the specified values such as the stimulation time, signal name, expected values, or actual value, messages will be printed in the Simulator Control Panel window. Or, you can view the messages in the LOG file by choosing **View** ⇒ **Simulator Log**.
7. Choose **File** ⇒ **Exit** to exit the Report Viewer.
8. Choose **File** ⇒ **Exit** to exit the Waveform Viewer.
9. Choose **File** ⇒ **Exit** to exit the Simulator Control Panel.



```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 2,200.0 ns
Operation RUN ends.
```



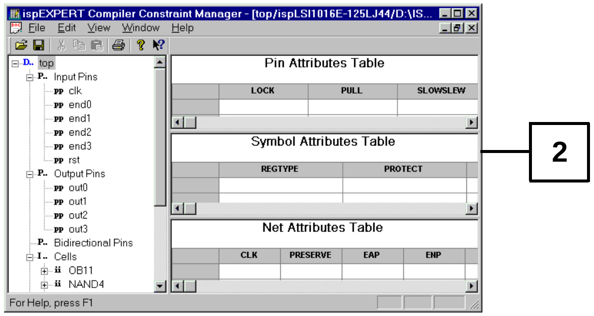
```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 2,200.0 ns
Operation RUN ends.
```

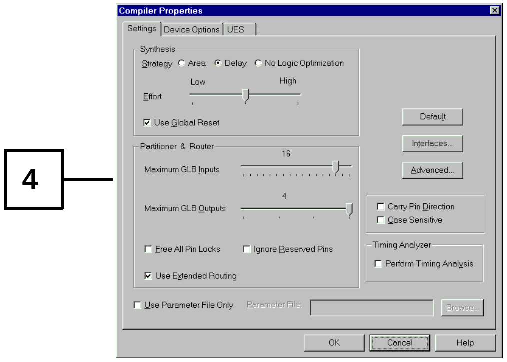
# Task 12 *Compile your Design*

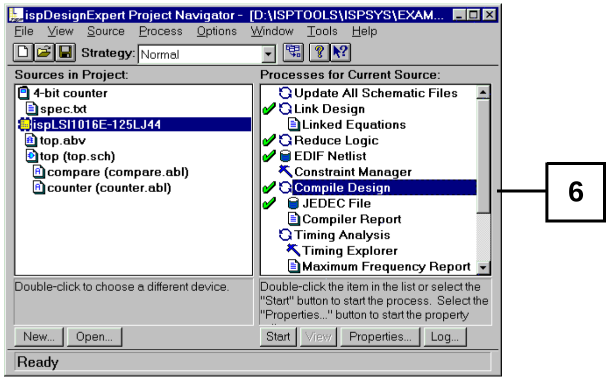
Now you can fit your design to the target device using the Compile Design process. For ispLSI designs, you can set options that control the compiler processes of your design, including global design control properties and a User Electronic Signature in the Compiler Properties dialog box.

*To compile your design:*

1. In the Sources window, select ispLSI1016E-125LJ44 as the target device.
2. Before running the Compiler, double-click Constraint Manager in the Processes window to open the Constraint Manager window. Notice that there are no constraints assigned.
3. Choose **File** ⇒ **Exit ispEXPERT Compiler Constraint Manager** to exit the Constraint Manager.
4. In the Processes window, select the Compile Design process. Click the **Properties** button at the bottom of the Project Navigator. The Compiler Properties dialog box appears. In this tutorial project, we do not need to set any options. Click **OK** to exit the Compiler Properties dialog box.
5. Double-click the Compile Design process from the Project Navigator. The ispDesignExpert Process dialog box opens to show the progress.
6. When the Compiler is finished running, ispDesignExpert updates the Processes window with green check marks.

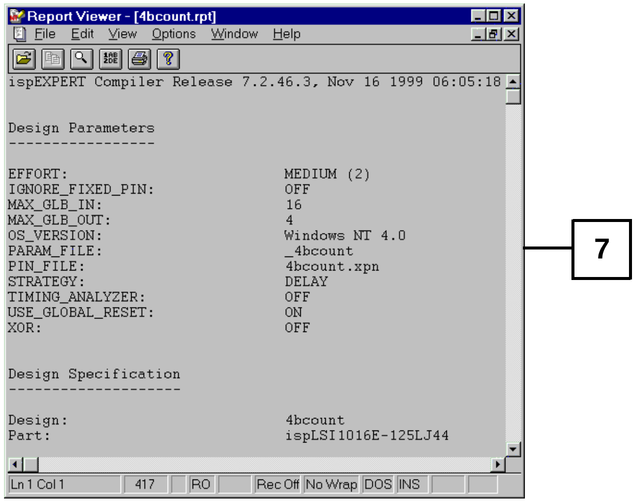






# Compile Your Design (continued)

7. When the process is finished, double click the Compiler Report process in the Processes window or click the **View** button at the bottom of the Project Navigator to display the Compiler Report (`.rpt`) in the Report Viewer. If there is any syntax error in the compilation procedure, the software displays errors in the report and an error indication (red X) appears beside the Compile Design process in the Processes window.
8. Close the Report Viewer.



```
ispEXPERT Compiler Release 7.2.46.3, Nov 16 1999 06:05:18


Design Parameters
-----------------

EFFORT:                         MEDIUM (2)
IGNORE_FIXED_PIN:               OFF
MAX_GLB_IN:                     16
MAX_GLB_OUT:                    4
OS_VERSION:                     Windows NT 4.0
PARAM_FILE:                     _4bcount
PIN_FILE:                       4bcount.xpn
STRATEGY:                       DELAY
TIMING_ANALYZER:                OFF
USE_GLOBAL_RESET:               ON
XOR:                            OFF


Design Specification
--------------------

Design:                         4bcount
Part:                           ispLSI1016E-125LJ44
```

# Task 13 *About Auto-Make*

The ispDesignExpert Automake feature knows which processing steps are up-to-date and which must be rerun when you double-click on a process or resulting file.

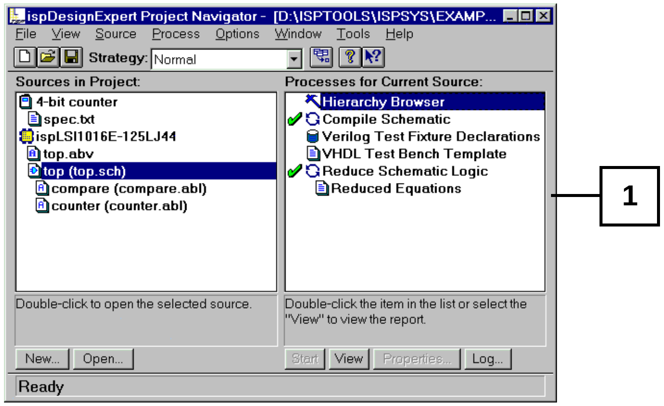
***Note:** Choose **Options** ⇒ **Environment** to open the Environment Options dialog box and make sure that the Auto-Make feature is selected.*

*To see a demonstration of Auto-Make*:

1. Select the schematic `top.sch` in the Sources window. Notice in the Processes window that there is a green check mark to the left of the Compile Schematic process. This indicates that the process has already run successfully.
2. Double-click the Compile Schematic process. The message bar at the bottom of the Project Navigator displays:

   `Process “Compile Schematic” is up to date.`

   The Auto-Make feature tells ispDesignExpert that it does not have to run this process again because the file is up to date.


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMP...
File View Source Process Options Window Tools Help
New... Open... Start View Properties... Log...
1

Strategy: Normal

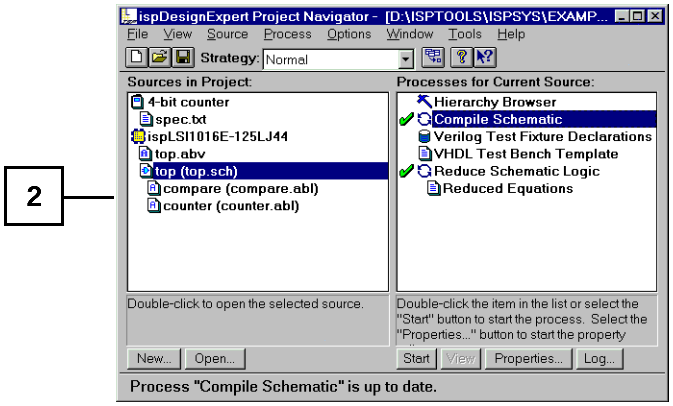
Sources in Project:
- 4-bit counter
- spec.txt
- ispLSI1016E-125LJ44
- top.abv
- top (top.sch)
- compare (compare.abl)
- counter (counter.abl)

Processes for Current Source:
- Hierarchy Browser
- ✓ Compile Schematic
- Verilog Test Fixture Declarations
- VHDL Test Bench Template
- ✓ Reduce Schematic Logic
- Reduced Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

Ready


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMP...
File View Source Process Options Window Tools Help
New... Open... Start View Properties... Log...
2

Strategy: Normal

Sources in Project:
- 4-bit counter
- spec.txt
- ispLSI1016E-125LJ44
- top.abv
- top (top.sch)
- compare (compare.abl)
- counter (counter.abl)

Processes for Current Source:
- Hierarchy Browser
- ✓ Compile Schematic
- Verilog Test Fixture Declarations
- VHDL Test Bench Template
- ✓ Reduce Schematic Logic
- Reduced Equations

Double-click to open the selected source.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property

Process "Compile Schematic" is up to date.

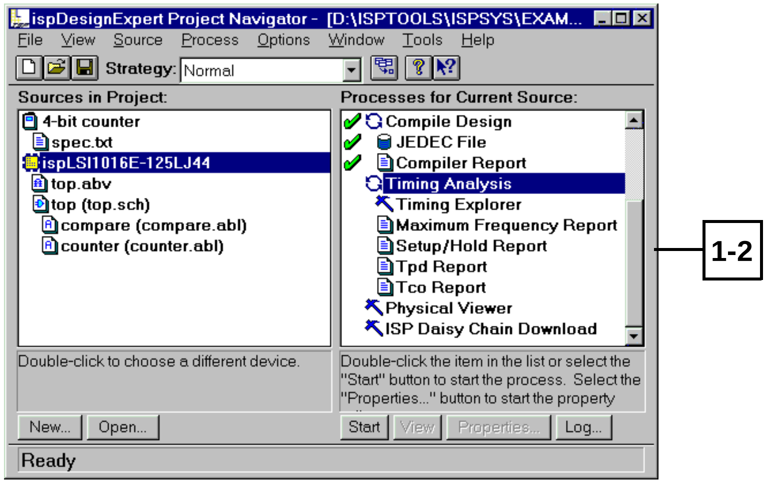
# Task 14 *Run Timing Analysis and View Timing Reports*

The Timing Analyzer allows you to evaluate the performance of the ispLSI design after successful compilation. The analyzer traces all the signal paths and their delays, determines critical (timing) paths, and evaluates the maximum frequency of the design and setup/hold requirements.

After running Timing Analysis, you can view the timing reports in ispEXPERT Timing Explorer. The Timing Explorer provides an interactive method for viewing and querying timing information for the design. Information is calculated in response to your query. Only the data you requested displays.

*To run timing analysis and view timing reports*:

1. In the Project Navigator, select the target device (ispLSI1016E-125LJ-44).
2. In the Processes window, double-click the Timing Analysis process.
3. When this process is completed, double-click the Timing Explorer process or select **Tools** ⇒ **Timing Explorer** from the Project Navigator.



Strategy: Normal

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property

Ready

# Run Timing Analysis and View Timing Reports (continued)

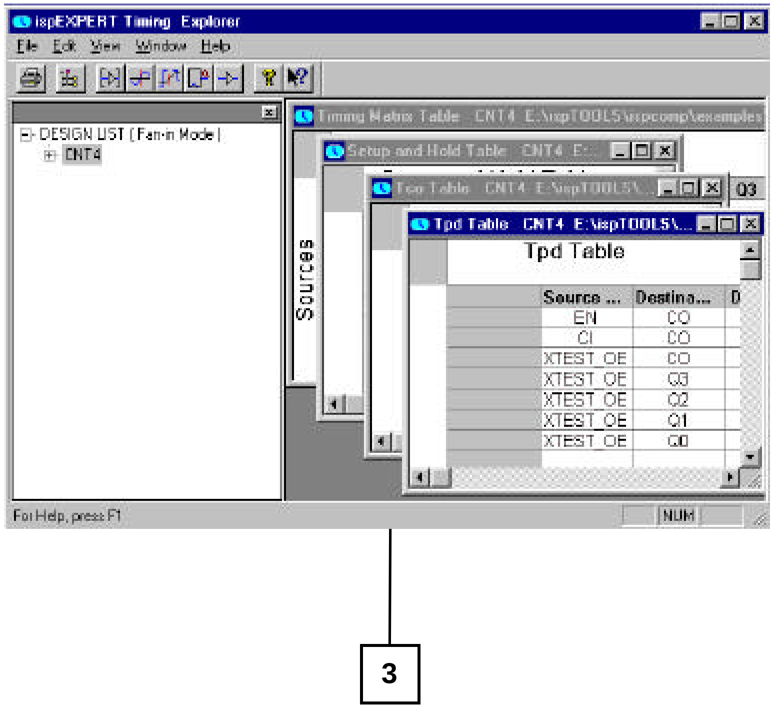
4. The ispEXPERT Timing Explorer appears.

   The Timing Explorer consists of Signal Navigator and several tables. The Signal Navigator lists design signals in a tree format and groups them into four categories—Inputs, Outputs, Bidirectional, and Registers. You can traverse the design in fan-in or fan-out mode (click the right mouse button to select the mode). You can expand the signal tree until the selected signal is a boundary signal or starts a loop.

   Available graphical tables include a Timing Matrix table, Clock Frequency table, Setup and Hold table, Tco table, and Tpd table. You can either tile or cascade these tables for easier access. Once the tables have been created, you can move between tables or redisplay a closed table using the **View** menu or the **Timing Matrix Table**, **Frequency Table**, **Setup and Hold Table**, **Tco Path Table**, and **Tpd Table** icons from the toolbar of the Timing Viewer.

***Note:*** *You can also view the Frequency table, Setup and Hold table, Tco Path table, or Tpd table in text format by choosing the Maximum Frequency Report, Setup/Hold Report, Tpd Report, or the Tco Report process from the Project Navigator. The relevant report will be opened in the Report Viewer.*

5. Choose **File** ⇒ **Exit ispEXPERT Timing Explorer** to exit the Timing Explorer.


ispEXPERT Timing Explorer
File Edit View Window Help
DESIGN LIST (Fan-in Mode)
CNT4
Timing Matrix Table CNT4 E:\ispTOOLS\ispcomp\examples
Setup and Hold Table CNT4 E:...
Tco Table CNT4 E:\ispTOOLS\...
Tpd Table CNT4 E:\ispTOOLS\...
Sources
Q3
For Help, press F1
NUM
3

Tpd Table

| Source ... | Destina... | D |
|---|---|---|
| EN | CO | |
| CI | CO | |
| XTEST_OE | CO | |
| XTEST_OE | Q3 | |
| XTEST_OE | Q2 | |
| XTEST_OE | Q1 | |
| XTEST_OE | Q0 | |

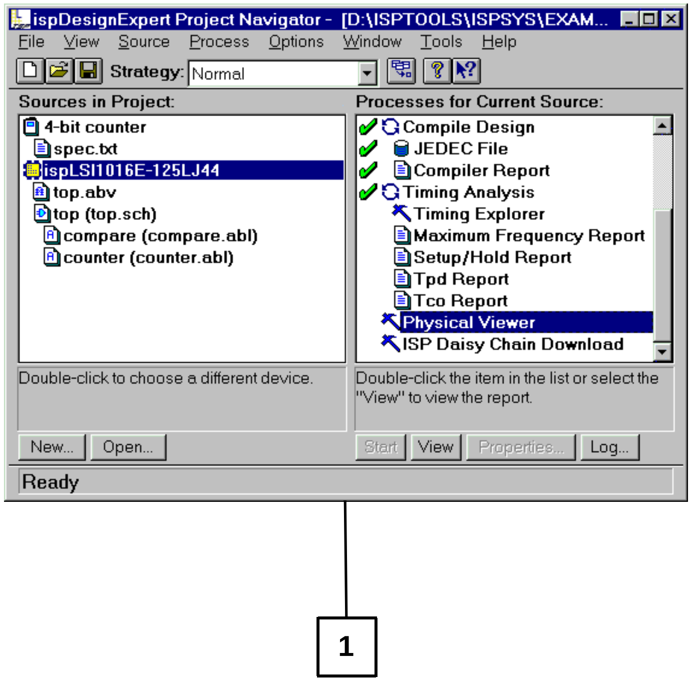
# Task 15 *Run Physical Viewer*

The Physical Viewer is a tool for graphically viewing the implementation details for a compiler project. It shows how the design logic is implemented in the device using the GLB, IOC, and Dedicated/Control Input logic resources. It also shows how data is propagated between the logic resources by displaying point-to-point routing information at the GLB level.

You can control what information is displayed and how it is displayed by selecting view modes and by selecting GLB, GLB output pin, IOC, or Dedicated/ Control Input pin for which you wish to see information.

*To run the Physical Viewer:*

1. In the Project Navigator, with the target device selected, double-click the Physical Viewer process or select **Tools** ⇒ **Physical Viewer**.



Strategy: Normal

- 4-bit counter
- spec.txt
- ispLSI1016E-125LJ44
- top.abv
- top (top.sch)
- compare (compare.abl)
- counter (counter.abl)

- ✓ Compile Design
- ✓ JEDEC File
- ✓ Compiler Report
- ✓ Timing Analysis
- Timing Explorer
- Maximum Frequency Report
- Setup/Hold Report
- Tpd Report
- Tco Report
- Physical Viewer
- ISP Daisy Chain Download

Double-click to choose a different device.

Double-click the item in the list or select the "View" to view the report.

Ready

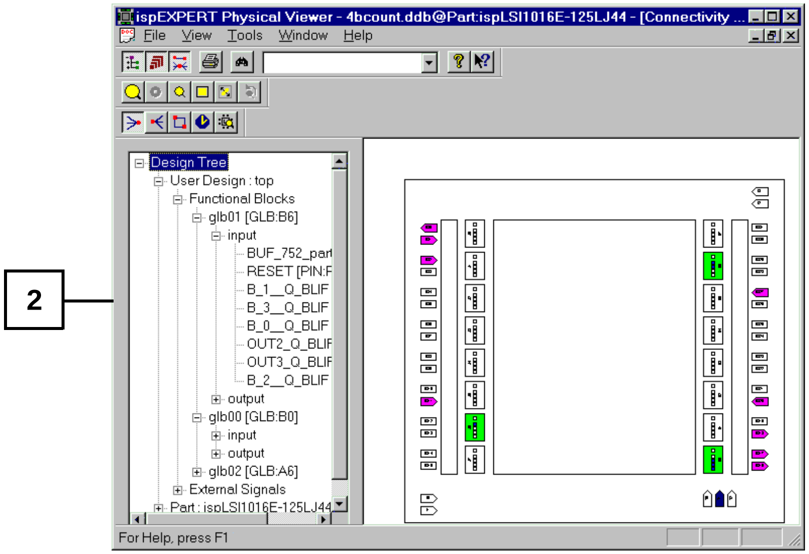
# Run Physical Viewer (continued)

2. When the Physical Viewer displays, the Design Navigator window is on the left side of the screen and the Connectivity window on the right side of the screen. The design implementation reflects the current compiled project.

   You can expand the design tree in the Design Navigator window to get information on the design and device logic resource usage.

   In the Connectivity window, the block diagram is displayed to show how the design logic is implemented in the device and how data is propagated across GLBs, IOCs, and Dedicated/ Control Inputs. You can select the GLBs, IOCs, and Dedicated/Control Inputs pin and the mode of display to control the information in the Connectivity window.

3. Close the Physical Viewer by selecting **File ⇒ ispEXPERT Physical Viewer**.



# Task 16 *Perform Timing Simulation*

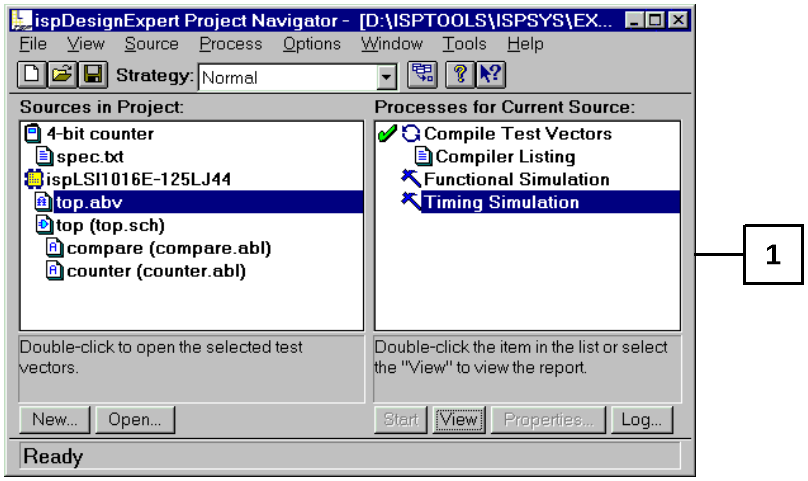
Timing simulation confirms that your design is compatible with the timing and propagation delays that exist in a specific device.

*To perform timing simulation:*

1. Select the test vector (`top.abv`) from the Sources window of the Project Navigator. Double click the associated Timing Simulation process or click the **Start** button at the bottom of the Project Navigator to launch the Simulator Control Panel.
2. When the Simulator Control Panel window opens, click the **Run** icon from the toolbar or choose **Simulate** ⇒ **Run** to start the simulation.
3. When the simulation ends, you can view the simulation results in the Waveform Viewer.

***Note**: Keep the **View** ⇒ **Show Waveforms** menu item checked so that the Waveform Viewer will automatically open with the waveforms of the simulated signals.*

4. Choose **File** ⇒ **Exit** to close the Waveform Viewer.
5. Choose **File** ⇒ **Exit** to close the Simulator Control Panel.


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EX...
File View Source Process Options Window Tools Help
Sources in Project:
Processes for Current Source:
New... Open...
Start View Properties... Log...
1

Strategy: Normal

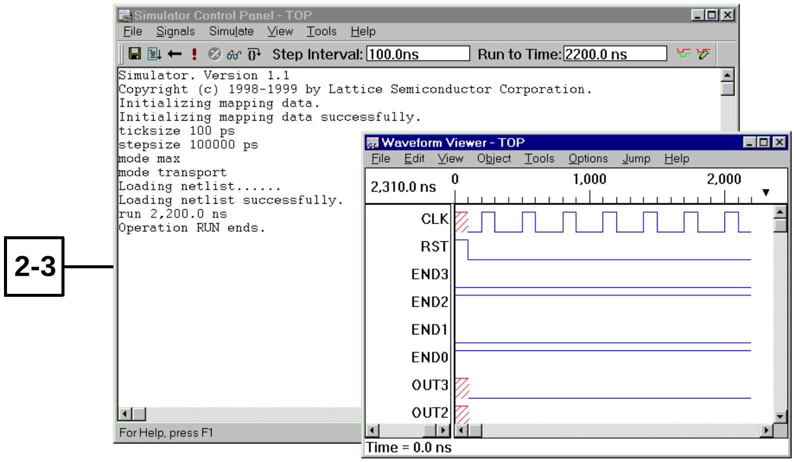
Sources in Project:
4-bit counter
spec.txt
ispLSI1016E-125LJ44
top.abv
top (top.sch)
compare (compare.abl)
counter (counter.abl)

Processes for Current Source:
Compile Test Vectors
Compiler Listing
Functional Simulation
Timing Simulation

Double-click to open the selected test vectors.

Double-click the item in the list or select the "View" to view the report.

Ready


Simulator Control Panel - TOP
File Signals Simulate View Tools Help
Waveform Viewer - TOP
File Edit View Object Tools Options Jump Help
0
1,000
2,000
CLK
RST
END3
END2
END1
END0
OUT3
OUT2
2-3

Step Interval: 100.0ns Run to Time: 2200.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode max
mode transport
Loading netlist......
Loading netlist successfully.
run 2,200.0 ns
Operation RUN ends.
```

For Help, press F1

2,310.0 ns

Time = 0.0 ns

# Congratulations!

You have completed the ispLSI Basics tutorial. In this tutorial you have learned:

- how to create a project directory.
- how to create a new project.
- how to select a device.
- how to create and import a design document file.
- how to import source files into a project.
- the introduction about the Project Navigator interface.
- how to examine the process flows.
- how to edit a project source.
- how to view the design hierarchy.
- how to process a module.
- how to run functional simulation.
- how to compile the design.
- the Auto-Make feature.
- how to run timing analysis and view timing reports.
- how to run Physical Viewer.
- how to perform timing simulation.

# Tutorial 2 ispDesignExpert MACH Design Basics

This tutorial provides an overview of the features and operation of ispDesignExpert for MACH designs, focusing on the Project Navigator to complete a programmable device design.

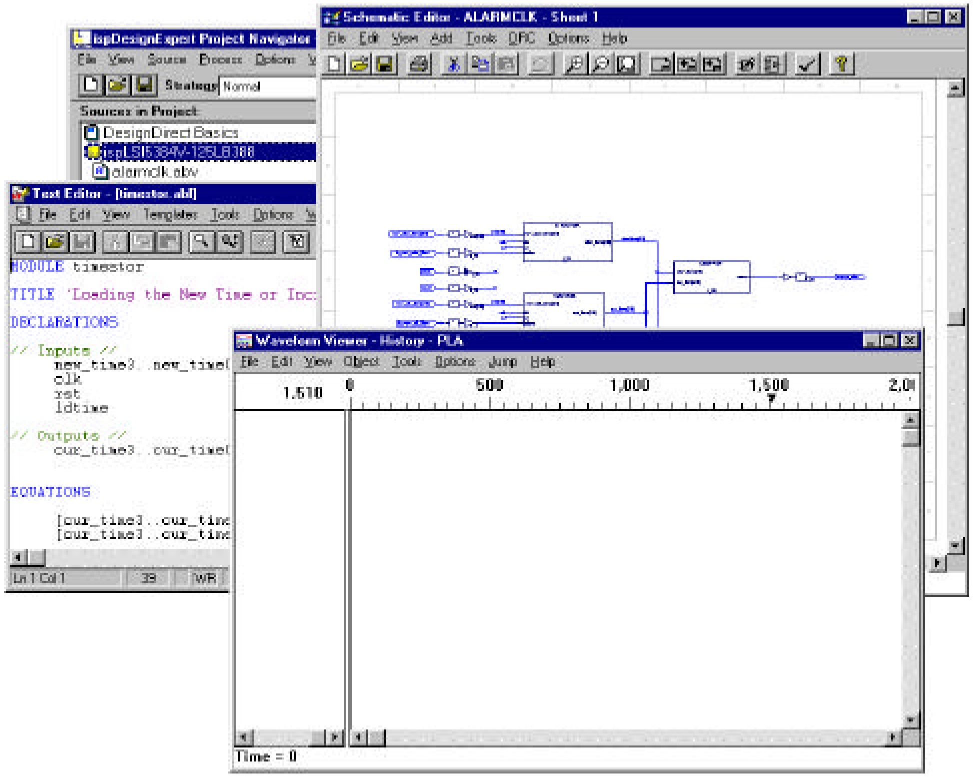
Follow the steps in this tutorial to implement a design called ddbasics using a mixture of schematics and ABEL-HDL.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of the steps and tools necessary to complete a Lattice programmable MACH design using ispDesignExpert.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.


ispDesignExpert Project Navigator
File View Source Process Options
Strategy Normal
Sources in Project
DesignDirect Basics
ispLSI5384V-125LB388
alarmclk.abv
Schematic Editor - ALARMCLK - Sheet 1
File Edit View Add Tools DRC Options Help
Text Editor - [timestor.abl]
File Edit View Templates Tools Options
Ln 1 Col 1
39
WR
Waveform Viewer - History - PLA
File Edit View Object Tools Options Jump Help
1,510
0
500
1,000
1,500
2,00
Time = 0

```
MODULE timestor

TITLE 'Loading the New Time or Inc

DECLARATIONS

// Inputs //
      new_time3..new_time(
      clk
      rst
      ldtime

// Outputs //
      cur_time3..cur_time(


EQUATIONS

      [cur_time3..cur_time
      [cur_time3..cur_time
```

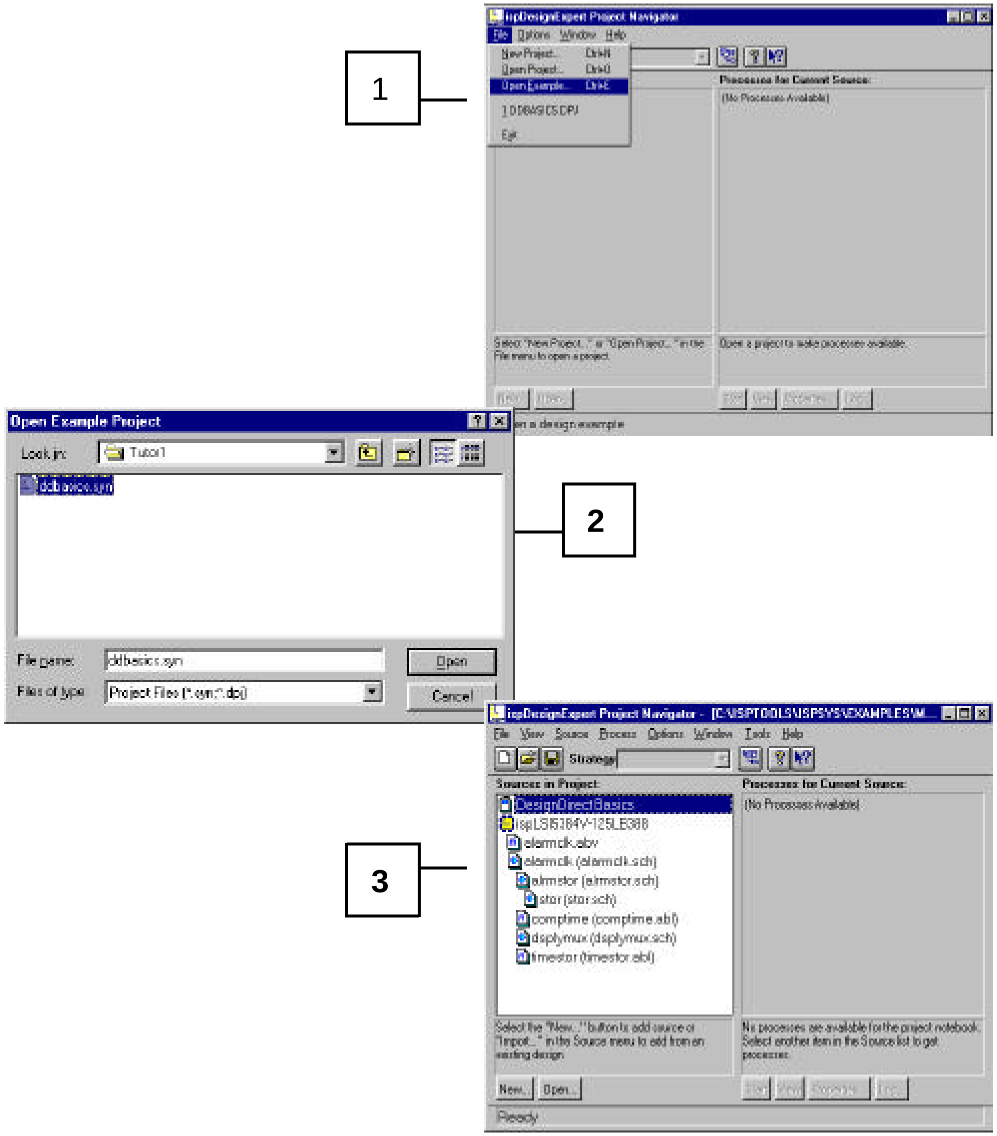
# Task 1 *Open a Project*

After starting the Project Navigator, you are ready to open the tutorial project file.

*To open a project*:

1. Choose **File** ⇒ **Open Example** to open the Open Project dialog.
2. In the dialog, change directories to `Mach_pal\tutorial\tutor1`**.**
3. Select the `ddbasics.syn` file and then click **Open**.

   The ispDesignExpert Basics project opens in the Project Navigator. A project contains all the source files for the design, such as behavioral and schematic logic descriptions, test fixtures, test benches, test vectors, waveforms, device type, and design documentation.



Select "New Project..." or "Open Project..." in the File menu to open a project.

Open a project to make processes available.

Open a design example

File name: ddbasics.syn

Files of type: Project Files (*.syn;*.dpj)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

# Task 2 *About the Project Navigator Interface*

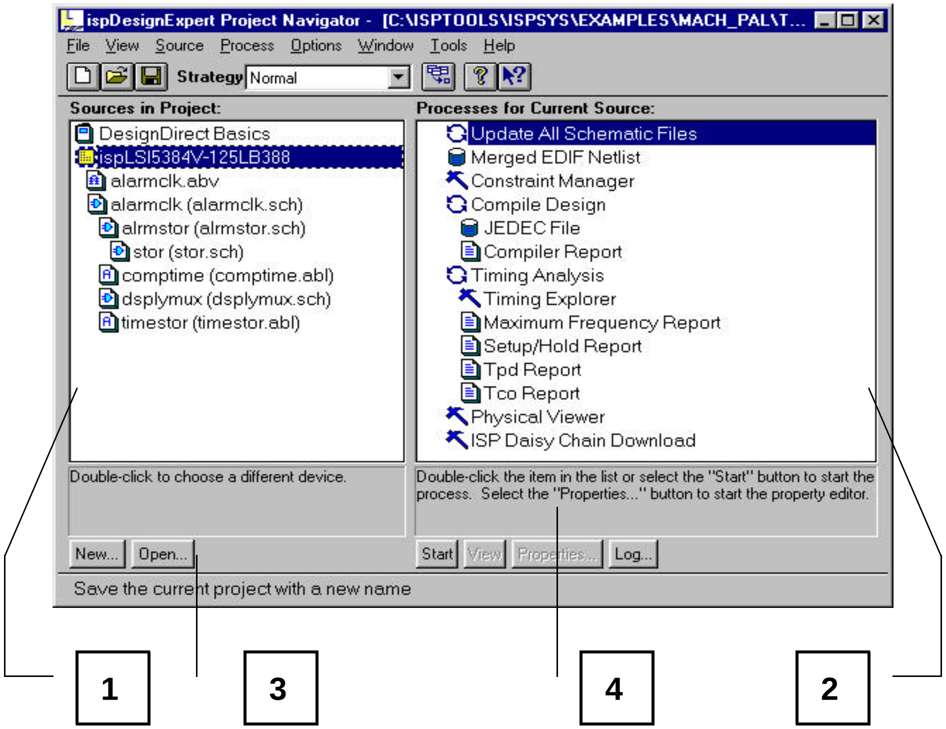
The Project Navigator has two primary interface elements: the *Sources* window and the *Processes* window.

The Sources window (**1**) shows all the design files associated with a project, listed in their logical, hierarchical order. Each source in the list is identified with an icon.

The Processes window (**2**) shows all the processing tasks that apply to a selected source in the Sources window. Typical programmable device processing task includes netlisting, compiling, logic reduction, logic synthesis, fitting, and simulation model building.

Buttons at the bottom of the Project Navigator (**3**) provide quick command access to key functions.

Also, there are two message areas (**4**) located above and below these buttons.



Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Save the current project with a new name

# Task 3 *Examine the Process Flows*

The Project Navigator is context sensitive—that is, it automatically adjusts the processes for you depending on what you want to do.

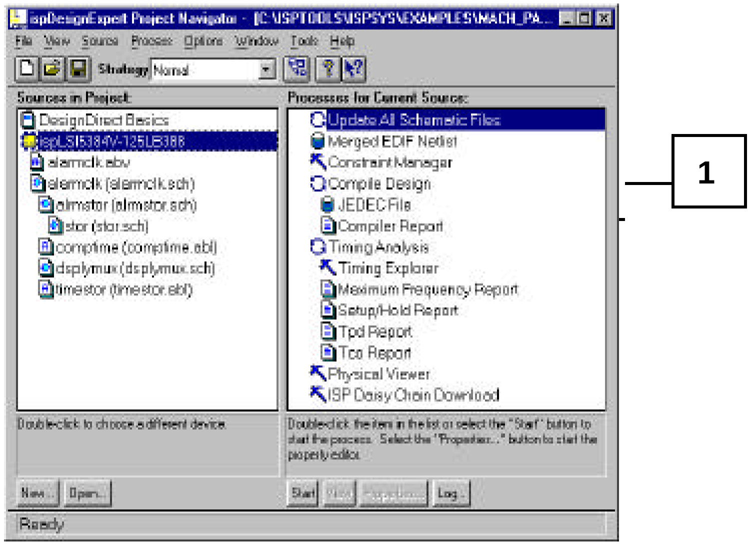
First, processing for a given file changes depending on the target device. This is called the *project-level* flow. For instance, a design targeted for a CPLD device is processed differently than a design targeted for a PAL device.

Second, the process flow changes depending on what kind of source file is highlighted in the Sources window. This is called the *source-level* flow. For example, if you select a schematic source (.sch), several processes appear in the Processes window. But if you select an ABEL test vector file (.abv), only the processes necessary for that source (functional simulation) are shown.

*Examine the process flows*:

1. To see the process-level flow, select the Device icon in the Sources window. The processes for the project appear in the Processes window.
2. To see a source-level flow, select a source. The processes for the selected source appear in the Processes window.

   Continue to select different sources and notice the processes change in the Processes window.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Process Options Window Tools Help
Strategy Normal
New... Open...
Start View Properties... Log...
1

Sources in Project:

- DesignDirect Basics
- ispLSI5384V-125LB388
- alarmclk.abv
- alarmclk (alarmclk.sch)
- almstor (almstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

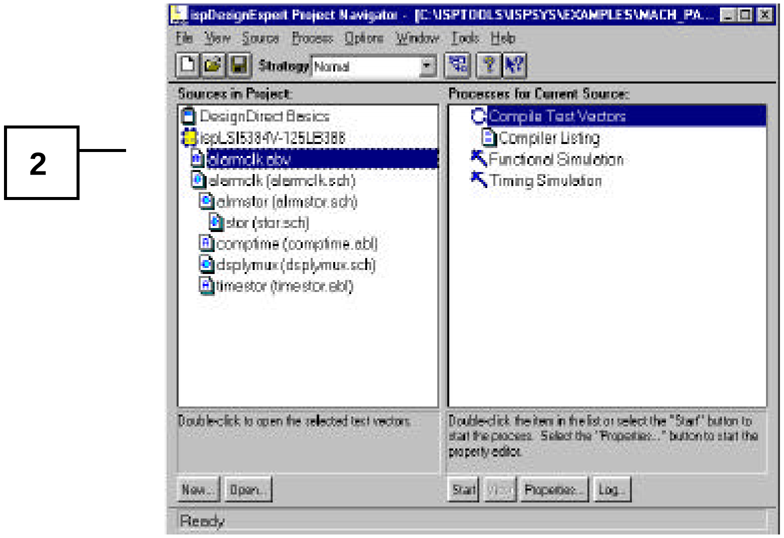
Processes for Current Source:

- Update All Schematic Files
- Merged EDIF Netlist
- Constraint Manager
- Compile Design
- JEDEC File
- Compiler Report
- Timing Analysis
- Timing Explorer
- Maximum Frequency Report
- Setup/Hold Report
- Tpd Report
- Tco Report
- Physical Viewer
- ISP Daisy Chain Download

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Process Options Window Tools Help
Strategy Normal
New... Open...
Start View Properties... Log...
2

Sources in Project:

- DesignDirect Basics
- ispLSI5384V-125LB388
- alarmclk.abv
- alarmclk (alarmclk.sch)
- almstor (almstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

Processes for Current Source:

- Compile Test Vectors
- Compiler Listing
- Functional Simulation
- Timing Simulation

Double-click to open the selected test vectors.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

# Task 4 *Select a Device*

Below the Project Notebook is the device icon that identifies the target device for the project. The Project Navigator lets you target a design to a specific Lattice device at any time during the design process.

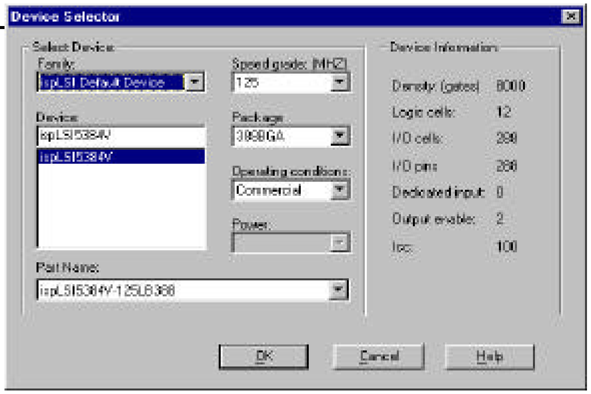
*To view the list of available devices and to change the target device*:

1. In the Sources window, double-click the **Device** to open the Device Selector dialog. The dialog shows the available device families and the devices in the selected family.
2. In the Device Selector dialog, select the **MACH 4** device family.
3. Select the **M4-32/32** device.
4. Accept the default settings and then click **OK**.
5. Click **Yes** to confirm that you wish to change device families.

   Notice that the process options changed after selecting the MACH device.

   When you change device families, the ispDesignExpert design environment reconfigures to facilitate designing with the selected device.

1



Device Selector

Select Device:

Family: ispLSI Default Device

Speed grade: (MHZ) 125

Device: ispLSI5384V

ispLSI5384V

Package 388BGA

Operating conditions: Commercial

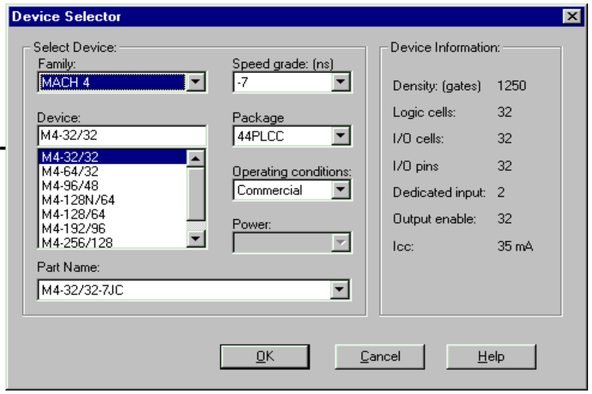
Power:

Part Name: ispLSI5384V-125LB388

Device Information:

Density: (gates) 8000
Logic cells: 12
I/O cells: 288
I/O pins: 288
Dedicated input: 0
Output enable: 2
Icc: 100

3



Device Selector

Select Device:

Family: MACH 4

Speed grade: (ns) -7

Device: M4-32/32

M4-32/32
M4-64/32
M4-96/48
M4-128N/64
M4-128/64
M4-192/96
M4-256/128

Package 44PLCC

Operating conditions: Commercial

Power:

Part Name: M4-32/32-7JC

Device Information:

Density: (gates) 1250
Logic cells: 32
I/O cells: 32
I/O pins: 32
Dedicated input: 2
Output enable: 32
Icc: 35 mA

# Task 5 *Create and Import a Design Documentation File*

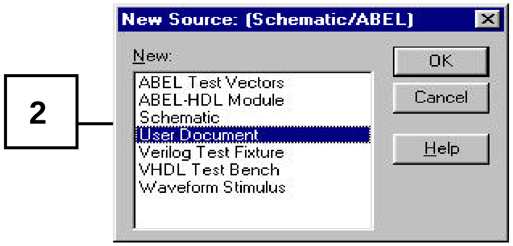
The Project Notebook works much like an engineering notebook. You can give it any name to describe your project. In addition, you can include files created by Windows applications other than ispDesignExpert. For instance, you might want to include a project schedule, a specification document, or a timing diagram.

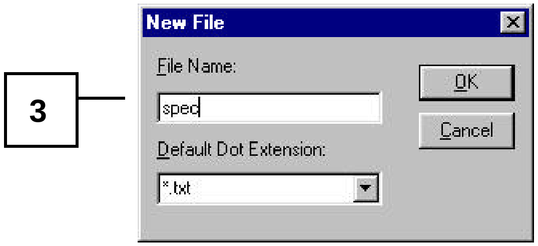
*To create a text document and import it into the Project Notebook*:

1. Choose **Source** ⇒ **New**.
2. In the New Source dialog, select **User Document**, and then click **OK**.
3. In the New File dialog, type **`spec`** in the File Name field. Then click **OK**.
4. In the Text Editor, type **`This is a sample text document`**.
5. Choose **File** ⇒ **Save**.

   ispDesignExpert automatically adds the file to the Sources window, under the Project Notebook, as part of the **ispDesignExpert Basics** project.
6. Choose **File** ⇒ **Exit**.

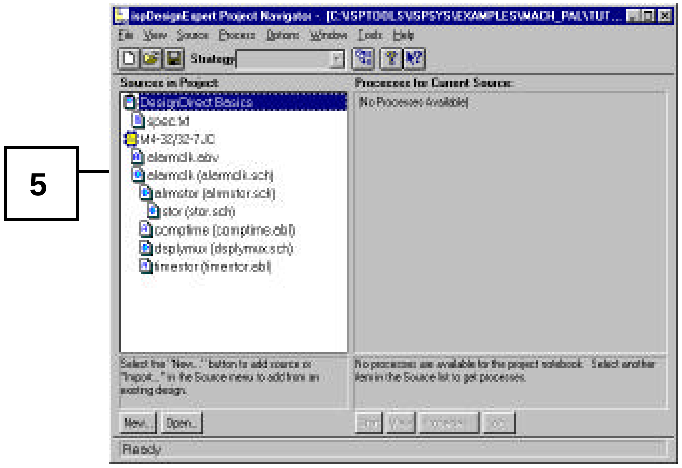
***Note:*** *You can add logic source files (for example, schematics and ABEL-HDL files) in the same way, although they appear in a different place in the Sources window. The Project Notebook area is for non-design source files.*





File Name: spec

Default Dot Extension: *.txt


5
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...
File
View
Source
Process
Options
Window
Tools
Help
Strategy
Sources in Project
Processes for Current Source:
New...
Open...

DesignDirect Basics
spec.txt
M4-32/32-7JC
alarmclk.abv
alarmclk (alarmclk.sch)
almstor (almstor.sch)
stor (stor.sch)
comptime (comptime.abl)
displymux (displymux.sch)
timestor (timestor.abl)

[No Processes Available]

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

# Task 6 *Edit a Project Source*

You can edit project source files by double clicking the desired source in the Sources window. ispDesignExpert opens the appropriate editor with that source ready for editing.

In this step you will see how to open the Schematic Editor from a schematic source.

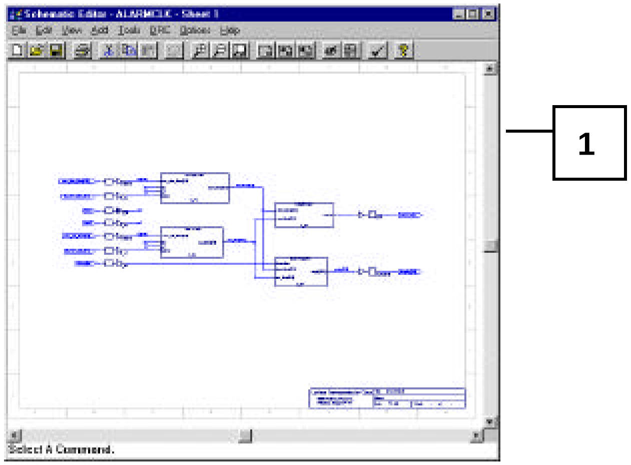
*To edit a schematic source file*:

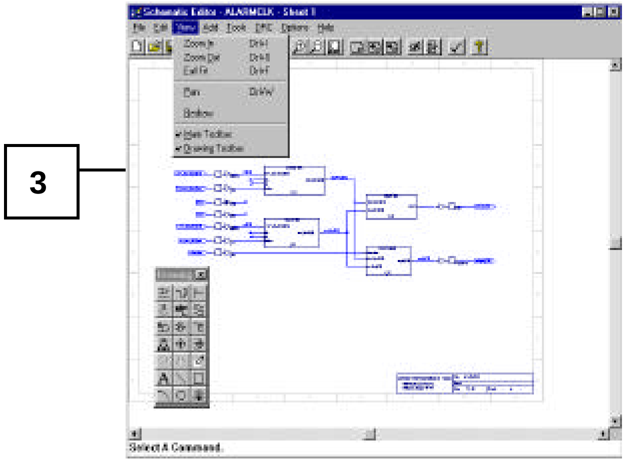
1. Double-click the top-level schematic **alarmclk** (`alarmclk.sch`) in the Sources window. The Schematic Editor opens on the schematic.

   When you double-click any source, ispDesignExpert automatically opens the application associated with that source file.

2. On the **View** menu, make sure that there is a check mark beside the **Main Toolbar** and **Drawing Toolbar** commands. (Click the command to toggle the check mark.)
3. Choose **File** ⇒ **Exit** to exit the Schematic Editor.

***Note:*** *You can also open a ispDesignExpert application from the Project Navigator Window menu.*


Schematic Editor - ALARMCLK - Sheet 1
File Edit View Add Tools DRC Options Help
Select A Command.
1



# Task 7 *View the Design Hierarchy*

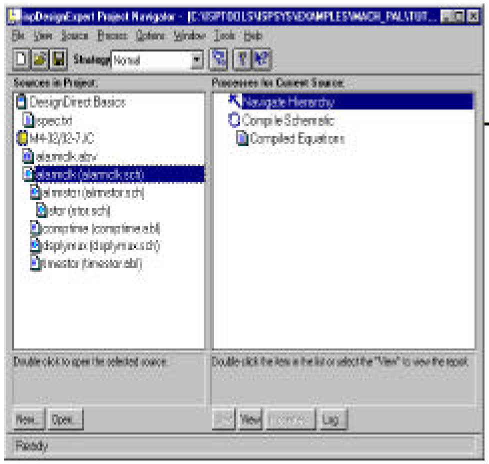
You can view the hierarchy of a top-level schematic and lower-level sources using the Hierarchy Navigator. With the Hierarchy Navigator you can traverse a design and access a number of powerful database features, such as pushing into blocks to see the source they refer to, accessing connectivity information, and querying nets.

***Note:*** *The Hierarchy Navigator is for viewing a design, not editing. For editing source files, use the Schematic Editor or Text Editor.*

*To view the design hierarchy using the Hierarchy Navigator*:

1. Select the top-level schematic **alarmclk** in the Sources window and double-click **Navigate Hierarchy** in the Processes window. The schematic opens in the Hierarchy Navigator.
2. Click **Push/Pop** (⇅) on the toolbar. The cursor changes to cross hairs.

   The **Push/Pop** command lets you "Push" down into a lower, more-detailed, level in the hierarchy or "Pop" up to a higher, less-detailed, level in the hierarchy.
3. Click *inside* the **ALRMSTOR** block symbol (upper-left) to push down into the block. The Hierarchy Navigator displays the contents for this block, which is another schematic. (You may need to use the **Zoom** command.)



1

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...

Strategy: Normal

Sources in Project:

- DesignDirect Basics
- spec.txt
- M4-32/32-7JC
- alarmclk.abv
- alarmclk (alarmclk.sch)
- alrmstor (alrmstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- displymx (displymx.sch)
- timestor (timestor.abl)

Processes for Current Source:

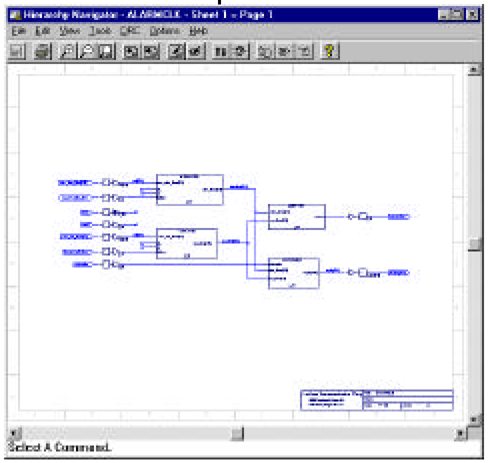
- Navigate Hierarchy
- Compile Schematic
- Compiled Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

Ready

File View Source Process Options Window Tools Help
New... Open...
View Log

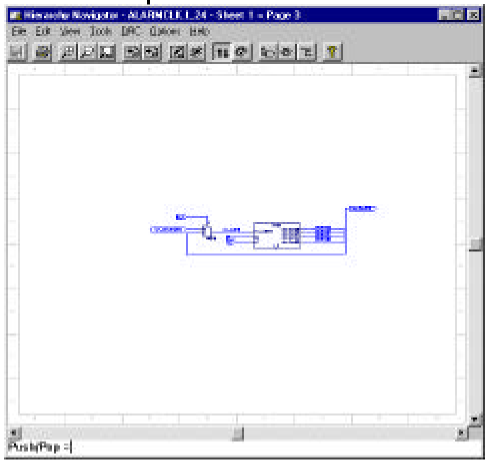


2

Hierarchy Navigator - ALARMCLK - Sheet 1 - Page 1

Select A Command.

File Edit View Tools DRC Options Help



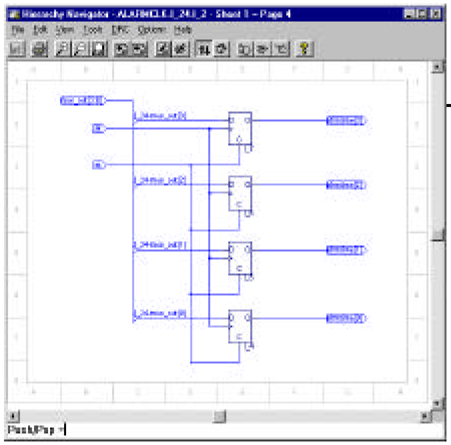
3

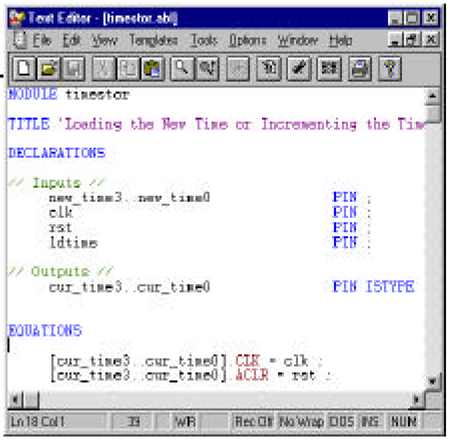
Hierarchy Navigator - ALARMCLK_L24 - Sheet 1 - Page 3

Push/Pop -|

# View the Design Hierarchy (continued)

4. Now click *inside* the **STOR** block symbol to see another level of the hierarchy. Try to click on another symbol. Nothing happens; there is no more hierarchy in this schematic.
5. Next "pop" back up to the top level of the design by clicking *outside* any symbol, in the white space. The Hierarchy Navigator "pops" you up to the second level. Repeat this step again to return to the top level schematic.
6. Now, push into an ABEL-HDL block. Click *inside* the **TIMESTOR** block symbol (lower-left). ispDesignExpert opens the Text Editor and displays the ABEL-HDL source for this block.
7. Choose **File** ⇒ **Exit** to close the Text Editor.
8. Choose **File** ⇒ **Exit** to close the Hierarchy Navigator.


Hierarchy Navigator - ALARMCLK.I_24.I_2 - Sheet 1 -- Page 4
File Edit View Tools DRC Options Help
Push/Pop
4


Text Editor - [timestor.abl]
File Edit View Templates Tools Options Window Help
6

```
MODULE timestor

TITLE 'Loading the New Time or Incrementing the Tim

DECLARATIONS

// Inputs //
     new_time3..new_time0                          PIN ;
     clk                                           PIN ;
     rst                                           PIN ;
     ldtime                                        PIN ;

// Outputs //
     cur_time3..cur_time0                          PIN ISTYPE


EQUATIONS

     [cur_time3..cur_time0].CLK = clk ;
     [cur_time3..cur_time0].ACLR = rst ;
```

Ln 18 Col 1
33
WR
Rec Off
No Wrap
DOS
INS
NUM

# Task 8 *Process a Module*

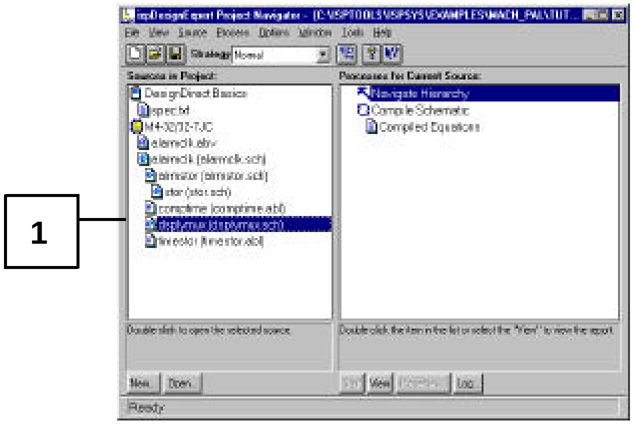
ispDesignExpert allows you to think *less* about the tools and steps involved in getting to a result and *more* about the desired result. For example, if you want to view a report, you don't want to have to figure out which processes should be run to generate the report. ispDesignExpert determines what steps are involved and runs them automatically if required. Because you *intuitively* know what results you want, ispDesignExpert's results-oriented processing greatly simplifies learning new architectures because it minimizes the impact of having to learn new tools and procedures.

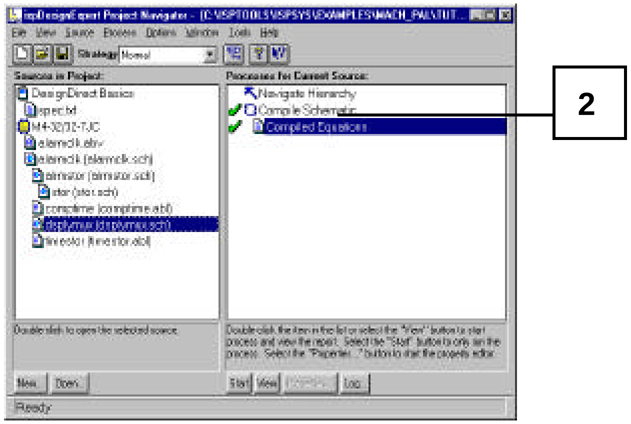
*To process the counter module*:

1. In the Project Navigator Sources window, select the schematic **dsplymux**. Notice that there is one process for this schematic (Compile Schematic) that generates one report file (Compiled Equations).

   While you can run each process separately, it’s faster and easier to tell ispDesignExpert what end result you want, and let ispDesignExpert determine which steps should be run in what order.
2. In the Processes window, double-click **Compiled Equations**. ispDesignExpert compiles the schematic into ABEL-HDL equations and displays the results in the Report Viewer.

   The Processes window displays the status of each process as it runs.
3. Close the Report Viewer.





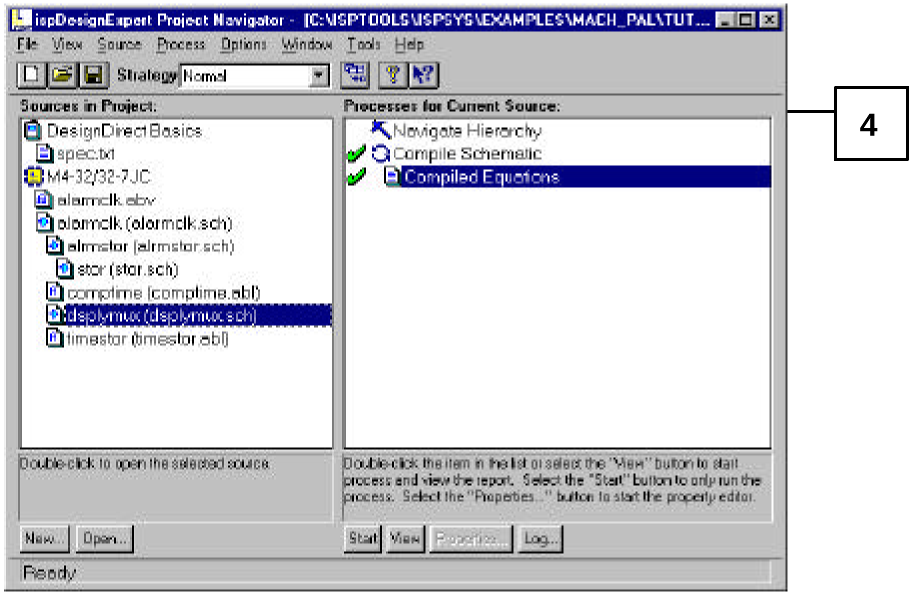
# Process a Module (continued)

4. Look at the Processes window. Note the processing-status icon that has appeared to the left of the processes, including the prerequisite processes that ispDesignExpert ran automatically.

   ispDesignExpert tells you the current status of any process using icons next to the process name. Status icons and their meanings are listed below.

| Icon | Meaning |
|---|---|
| ✓ | The process completed successfully and is up-to-date. |
| ⚠ | The process completed successfully, but warnings or messages were generated; these can be read in the Report Viewer. |
| ✗ | The process did not complete, because errors occurred. Errors must be corrected to go forward. |

The Processes window is constantly updated. If you edit a source file, the green check marks disappear for processes that were previously run.



Double-click to open the selected source.

Double-click the item in the list or select the "View" button to start process and view the report. Select the "Start" button to only run the process. Select the "Properties..." button to start the property editor.

# Task 9 *Run Equation Simulation*

Equation simulation uses design test vectors to simulate the design logic or equations, independent of any device. The more comprehensive and detailed your test vectors are, the more useful your simulation results will be.

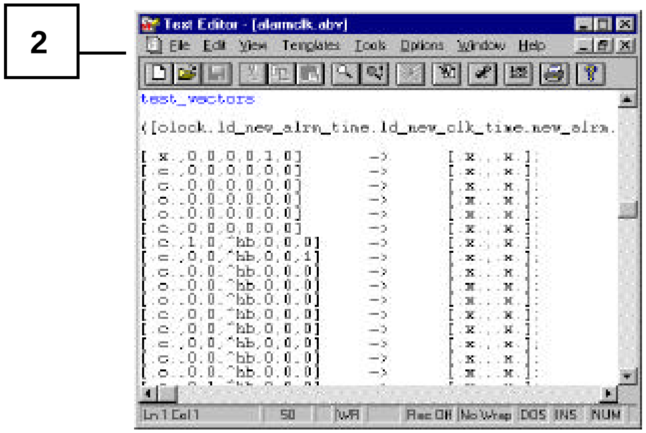
The simulator applies the inputs from the test vectors to the simulated circuit and compares the simulated output with the output specified in the test vectors. If there is any difference, an error is indicated.

Equation simulation tests your design without using device-specific information. Therefore, Equation simulation can be conducted before you select a device. Equation Simulation, however, only tests the equations in your design as specified by test stimulus (ABEL-HDL test vectors).

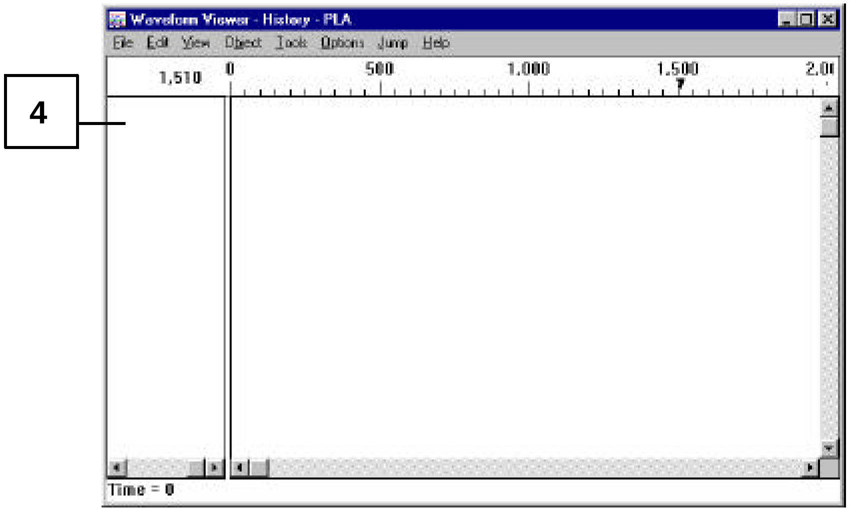
*To behaviorally simulate your design*:

1. In the Sources window, double-click `alarmclk.abv` to open the test vector file in the Text Editor.
2. Scroll the window and view the Test Vector file.
3. Close the file and exit the Text Editor.
4. In the Processes window, double-click **Equation Simulation Waveform** to open the Waveform Viewer. The viewer will be empty until you add waveforms to it.

   You can use the Waveform Viewer to view the output of a logic simulation. The state of any net on a schematic can be viewed as a time line trace, similar to what you would observe when using a logic analyzer. Traces may display individual signals or buses.
5. Choose **File** ⇒ **Exit** to exit the Waveform Viewer.


2
Text Editor - [alarmclk.abv]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
50
WR
Rec Off
No Wrap
DOS
INS
NUM

```
test_vectors

([clock,ld_new_alrm_time,ld_new_clk_time,new_alrm.

[.x.,0,0,0,0,1,0]        ->        [.x.,.x.];
[.c.,0,0,0,0,0,0]        ->        [.x.,.x.];
[.c.,0,0,0,0,0,0]        ->        [.x.,.x.];
[.c.,0,0,0,0,0,0]        ->        [.x.,.x.];
[.c.,0,0,0,0,0,0]        ->        [.x.,.x.];
[.c.,0,0,0,0,0,0]        ->        [.x.,.x.];
[.c.,1,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,1]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
[.c.,0,0,^hb,0,0,0]      ->        [.x.,.x.];
```

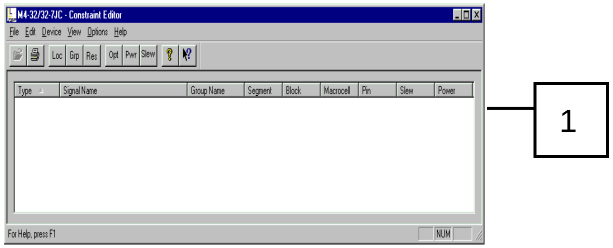

4
Waveform Viewer - History - PLA
File Edit View Object Tools Options Jump Help
1,510
0
500
1,000
1,500
2,00
Time = 0

# Task 10 *Fit the Design*

After you have targeted a specific device, you can "fit" your design. The Fitter is a program that maps designs into a targeted device. This process may include assigning pins and nodes, logic synthesis, and complex device routing.

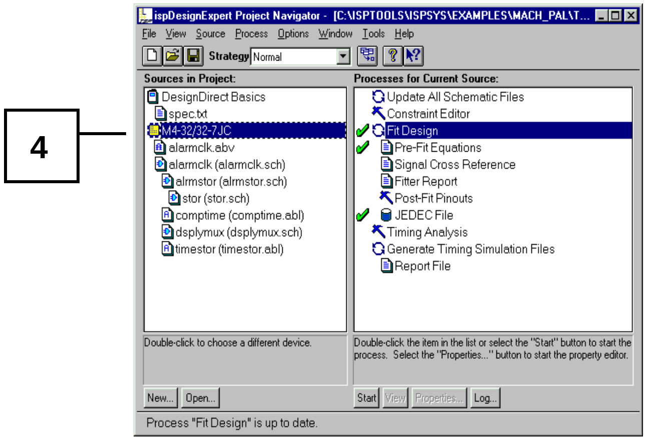
To fit your design:

1. In the Sources window, select the target device (**M4-32/32**) if it is not already selected.
2. Before running the Fitter, double-click **Constraint Editor** in the Processes window to open the dialog. Notice that there are no constraints assigned.
3. Choose **File** ⇒ **Exit** to exit the Constraint Editor.
4. In the Processes window, double-click **Fit Design**. The ispDesignExpert Process dialog opens to show the progress.
5. When the Fitter is finished running, ispDesignExpert updates the Processes window with check marks.
6. In the Processes window, double-click **Post-Fit Pinouts**. This dialog shows you the location assignments made by the Fitter.
7. Choose **File** ⇒ **Exit** to exit the Post-Fit Pinouts dialog.


M4-32/32-7JC - Constraint Editor
File Edit Device View Options Help
Loc Grp Res Opt Pwr Slew
NUM
1

| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|

For Help, press F1


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\T...
File View Source Process Options Window Tools Help
Strategy Normal
New... Open...
Start View Properties... Log...
4

Sources in Project:

- DesignDirect Basics
- spec.txt
- M4-32/32-7JC
- alarmclk.abv
- alarmclk (alarmclk.sch)
- alrmstor (alrmstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

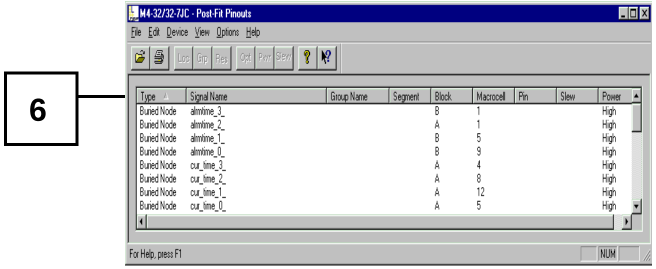
Processes for Current Source:

- Update All Schematic Files
- Constraint Editor
- ✓ Fit Design
- ✓ Pre-Fit Equations
- Signal Cross Reference
- Fitter Report
- Post-Fit Pinouts
- ✓ JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
- Report File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Process "Fit Design" is up to date.


M4-32/32-7JC - Post-Fit Pinouts
File Edit Device View Options Help
Loc Grp Res Opt Pwr Slew
NUM
6

| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|
| Buried Node | alrmtime_3_ | | | B | 1 | | | High |
| Buried Node | alrmtime_2_ | | | A | 1 | | | High |
| Buried Node | alrmtime_1_ | | | B | 5 | | | High |
| Buried Node | alrmtime_0_ | | | B | 9 | | | High |
| Buried Node | cur_time_3_ | | | A | 4 | | | High |
| Buried Node | cur_time_2_ | | | A | 8 | | | High |
| Buried Node | cur_time_1_ | | | A | 12 | | | High |
| Buried Node | cur_time_0_ | | | A | 5 | | | High |

For Help, press F1

# Task 11 *About Auto-Make*

The ispDesignExpert Auto-Make feature knows which processing steps are up-to-date and which must be rerun when you double-click on a process or resulting file.

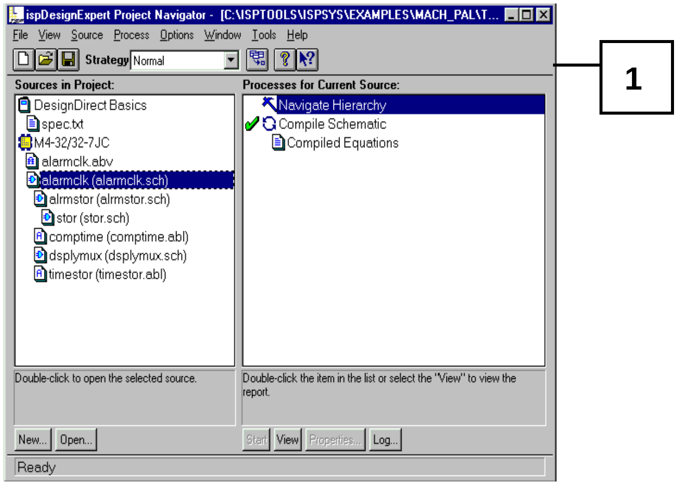
***Note:** Choose **Options** ⇒ **Environment** to open the Environment Options dialog and make sure that the Auto-Make feature is selected.*

*To see a demonstration of Auto-Make*:

1. Select the schematic `alarmclk.sch` in the Sources window. Notice in the Processes window that there is a green check mark to the left of **Compile Schematic**. This indicates that the process has already run successfully.
2. Double-click **Compile Schematic**. The message bar at the bottom of the Project Navigator displays:

   Process “Compile Schematic” is up to date.

   The Auto-Make feature tells ispDesignExpert that it does not have to run this process again because the file is up to date.


1
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\T...
File View Source Process Options Window Tools Help
Strategy Normal
New... Open... Start View Properties... Log...

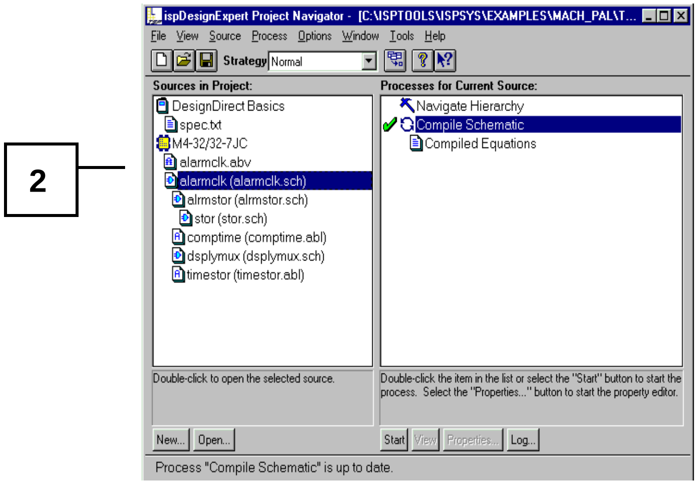
Sources in Project:
- DesignDirect Basics
- spec.txt
- M4-32/32-7JC
- alarmclk.abv
- alarmclk (alarmclk.sch)
- alrmstor (alrmstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

Processes for Current Source:
- Navigate Hierarchy
- ✓ Compile Schematic
- Compiled Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

Ready


2
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\T...
File View Source Process Options Window Tools Help
Strategy Normal
New... Open... Start View Properties... Log...

Sources in Project:
- DesignDirect Basics
- spec.txt
- M4-32/32-7JC
- alarmclk.abv
- alarmclk (alarmclk.sch)
- alrmstor (alrmstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

Processes for Current Source:
- Navigate Hierarchy
- ✓ Compile Schematic
- Compiled Equations

Double-click to open the selected source.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Process "Compile Schematic" is up to date.

# Task 12 *Run Timing Analysis*

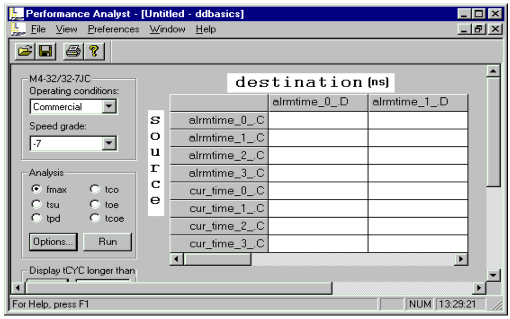
The Performance Analyst is a static timing analysis tool that enables you to quickly determine the performance of your design after it has been optimized and implemented by the Fitter.

Worst case signal delays are reported in a graphical spreadsheet format that you can filter to verify the speed of critical paths and identify performance bottlenecks.

*To run timing analysis*:

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Timing Analysis** to open the Performance Analyst.

   Under Analysis, there are six types of analysis you can perform using the Performance Analyst. Notice the Source and Destination report format on the right.
3. Under Analysis, select **tco** and notice the change in the Source and Destination format.
4. Under Analysis, click **Run** and see the timing report to the right.
5. You can double-click any number in the report to see how the Performance Analyst generated these numbers.
6. Choose **File** ⇒ **Exit** to exit the Performance Analyst.


Performance Analyst - [Untitled - ddbasics]
File View Preferences Window Help
Options...
Run

2

M4-32/32-7JC
Operating conditions: Commercial
Speed grade: -7

Analysis: ● fmax ○ tsu ○ tpd ○ tco ○ toe ○ tcoe

Display tCYC longer than

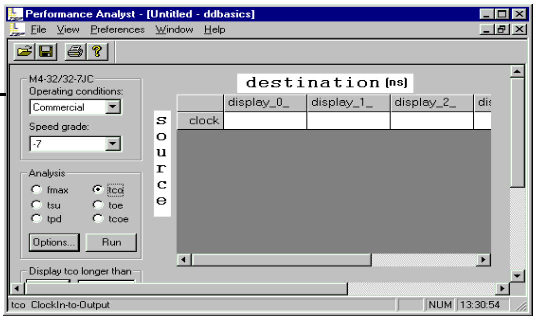
destination (ns)

source

| | alrmtime_0_.D | alrmtime_1_.D |
|---|---|---|
| alrmtime_0_.C | | |
| alrmtime_1_.C | | |
| alrmtime_2_.C | | |
| alrmtime_3_.C | | |
| cur_time_0_.C | | |
| cur_time_1_.C | | |
| cur_time_2_.C | | |
| cur_time_3_.C | | |

For Help, press F1 NUM 13:29:21

3


Performance Analyst - [Untitled - ddbasics]
File View Preferences Window Help
Options...
Run

M4-32/32-7JC
Operating conditions: Commercial
Speed grade: -7

Analysis: ○ fmax ○ tsu ○ tpd ● tco ○ toe ○ tcoe

Display tco longer than

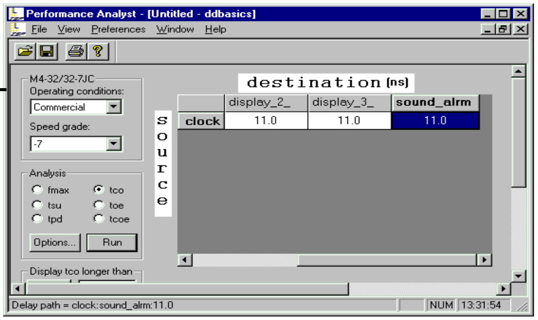
destination (ns)

source

| | display_0_ | display_1_ | display_2_ | dis |
|---|---|---|---|---|
| clock | | | | |

tco ClockIn-to-Output NUM 13:30:54

4


Performance Analyst - [Untitled - ddbasics]
File View Preferences Window Help
Options...
Run

M4-32/32-7JC
Operating conditions: Commercial
Speed grade: -7

Analysis: ○ fmax ○ tsu ○ tpd ● tco ○ toe ○ tcoe

Display tco longer than

destination (ns)

source

| | display_2_ | display_3_ | sound_alrm |
|---|---|---|---|
| clock | 11.0 | 11.0 | 11.0 |

Delay path = clock:sound_alrm:11.0 NUM 13:31:54

# Task 13 *Backannotate Pin Location Assignments*

You can backannotate assignments from the Fitter output using the Backannotation tab on the Constraints Options dialog. This feature lets you retain the assignments made by the Fitter so they can be used in the future.

You can only backannotate project assignments after the “Fit Design” process has been successfully completed.

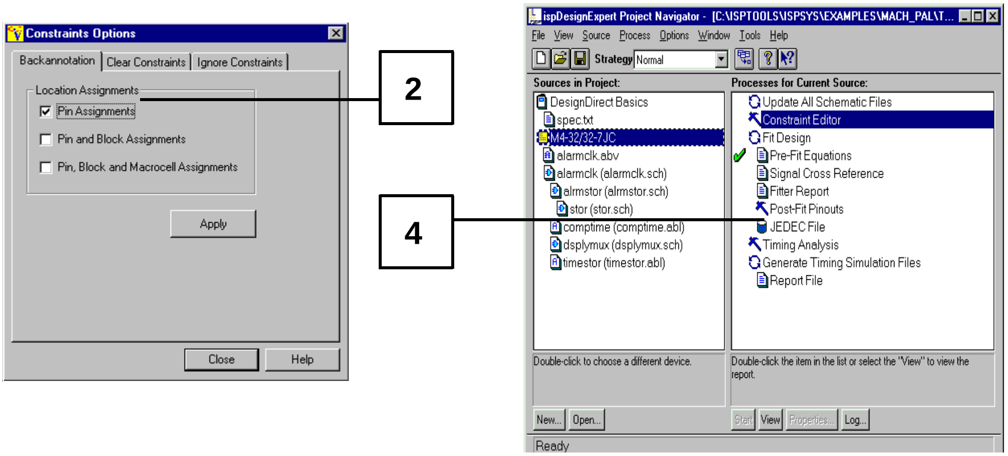
T*o backannotate pin location assignments*:

1. In the Project Navigator, choose **Tools** ⇒ **Backannotate Project Assignments** to open the Constraints Options dialog.
2. On the Backannotation tab, select **Pin Assignments**, and then click **Apply**.
3. A warning message appears asking if you want to continue. Click **Yes**.
4. Click **Close** to close the dialog.

   Notice that several process had their green check marks removed. This indicates that the previous fitter results are no longer valid because you have assigned pin location constraints.
5. Double-click **Constraint Editor**. Notice that there are now pin location constraints assigned.

***Note****: If you wanted to edit certain constraints, you would use this editor (for example,* ***Edit*** ⇒ ***Location Assignment****).*

6. Double-click **Fit Design** to fit the design with these new constraints.



☑ Pin Assignments

☐ Pin and Block Assignments

☐ Pin, Block and Macrocell Assignments

Strategy Normal

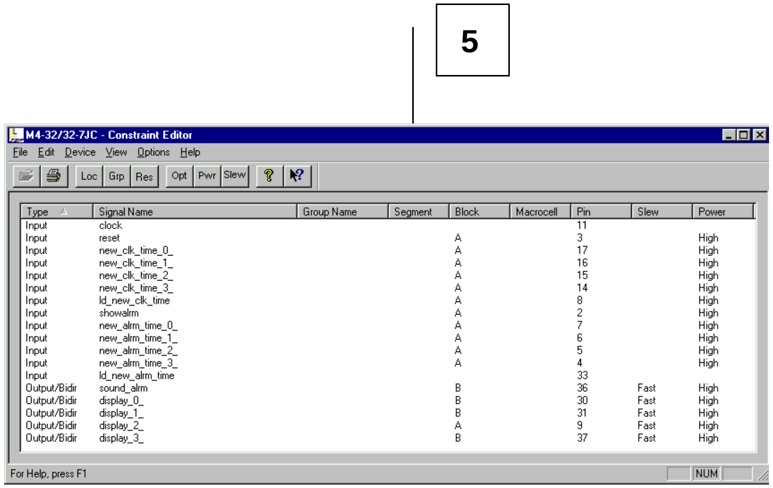
Sources in Project:
- DesignDirect Basics
- spec.txt
- M4-32/32-7JC
- alarmclk.abv
- alarmclk (alarmclk.sch)
- alrmstor (alrmstor.sch)
- stor (stor.sch)
- comptime (comptime.abl)
- dsplymux (dsplymux.sch)
- timestor (timestor.abl)

Processes for Current Source:
- Update All Schematic Files
- Constraint Editor
- Fit Design
- ✓ Pre-Fit Equations
- Signal Cross Reference
- Fitter Report
- Post-Fit Pinouts
- JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
- Report File

Double-click to choose a different device.

Double-click the item in the list or select the "View" to view the report.

Ready



| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|
| Input | clock | | | | | 11 | | |
| Input | reset | | | A | | 3 | | High |
| Input | new_clk_time_0_ | | | A | | 17 | | High |
| Input | new_clk_time_1_ | | | A | | 16 | | High |
| Input | new_clk_time_2_ | | | A | | 15 | | High |
| Input | new_clk_time_3_ | | | A | | 14 | | High |
| Input | ld_new_clk_time | | | A | | 8 | | High |
| Input | showalrm | | | A | | 2 | | High |
| Input | new_alrm_time_0_ | | | A | | 7 | | High |
| Input | new_alrm_time_1_ | | | A | | 6 | | High |
| Input | new_alrm_time_2_ | | | A | | 5 | | High |
| Input | new_alrm_time_3_ | | | A | | 4 | | High |
| Input | ld_new_alrm_time | | | | | 33 | | |
| Output/Bidir | sound_alrm | | | B | | 36 | Fast | High |
| Output/Bidir | display_0_ | | | B | | 30 | Fast | High |
| Output/Bidir | display_1_ | | | B | | 31 | Fast | High |
| Output/Bidir | display_2_ | | | A | | 9 | Fast | High |
| Output/Bidir | display_3_ | | | B | | 37 | Fast | High |

For Help, press F1

# *Congratulations!*

You have completed the ispDesignExpert Basics tutorial. In this tutorial you have learned:

- how to open a ispDesignExpert project.
- the different elements of the Project Navigator user interface.
- that there are *project-* and *source-level* process flows, and how to switch between them using the Project Navigator interface.
- how to create and import source file into a project.
- how to edit sources by double clicking the source file in the Project Navigator.
- how to use the Hierarchy Navigator to view a design.
- how to process a design.
- how to run Equation Simulation and open the Waveform Viewer to analyze the results.
- how to select a target device and choose operating options.
- how to use the Location Assignments dialog to assign pins, and then save the information to the constraints file.
- how to place and route a design using the Fitter.
- how the Auto-Make feature eliminates unnecessary processing of already-completed steps.
- how to run static timing analysis on a design, and evaluate the results graphically.
- how to backannotate pin location assignments.

# Part II: Design Entry with ispDesignExpert

# Tutorial 3 Schematic and ABEL-HDL Design Entry

This tutorial leads you through the design of a counter circuit targeted to a CPLD device (in this tutorial, a MACH device). The design consists of a top-level schematic and two lower-level ABEL-HDL modules. A top-down, bottom-up design methodology is used.

## Prerequisites

Before attempting this tutorial, you should complete Tutorial 1, *ispLSI Design Basics* or Tutorial 2, *MACH Design Basics*.

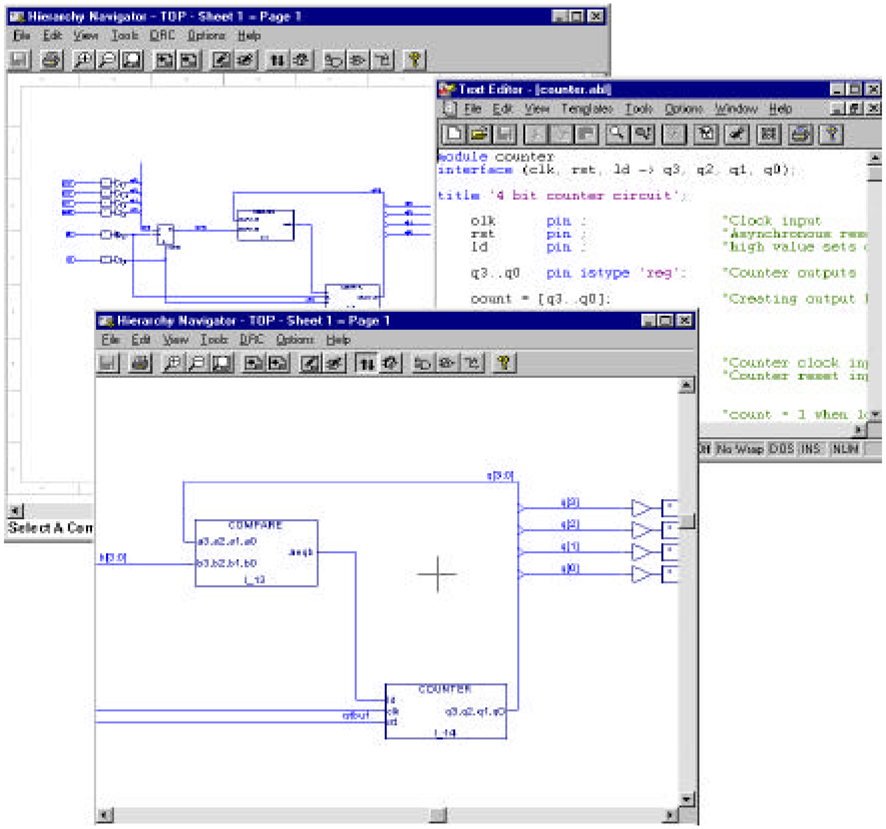
## Learning Objectives

When you are finished with the tutorial, you should be able to:

- Add various schematic elements to create a top-level schematic source
- Check the schematic for errors
- Use the Text Editor to create a new ABEL-HDL source
- Import an ABEL-HDL source into the project
- Use the Hierarchy Browser to navigate through the design and try "debug" methods

## Time to Complete This Tutorial

On average, it should take you approximately 90 minutes to complete this tutorial.



```
module counter
interface (clk, rst, ld -> q3, q2, q1, q0);

title '4 bit counter circuit';

    clk        pin ;                          "Clock input
    rst        pin ;                          "Asynchronous res
    ld         pin ;                          "high value sets 

    q3..q0     pin istype 'reg';              "Counter outputs

    count = [q3..q0];                         "Creating output 


                                              "Counter clock in
                                              "Counter reset in


                                              "count = 1 when l
```

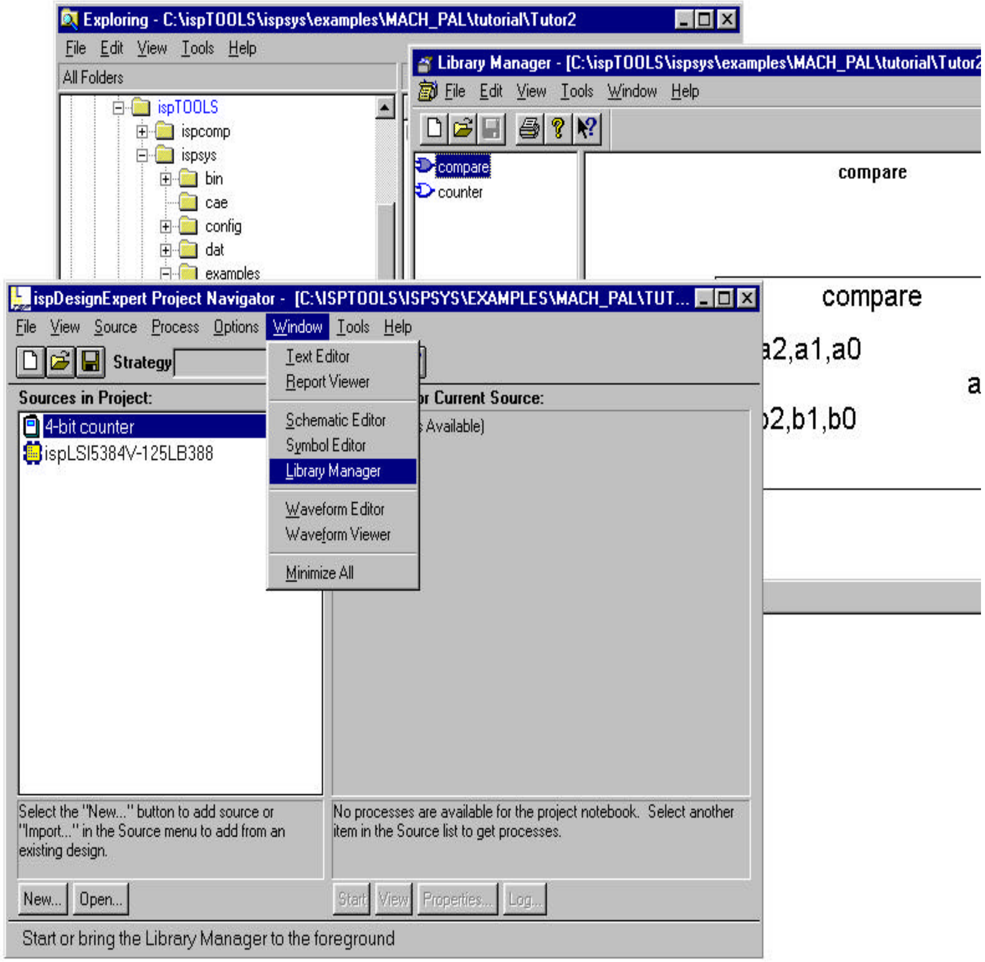
Hierarchy Navigator - TOP - Sheet 1 - Page 1
File Edit View Tools DRC Options Help
Text Editor - [counter.abl]
File Edit View Templates Tools Options Window Help
Select A Con
No Wrap DOS INS NLIN
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb
I_13
COUNTER
ld
clk
rst
q3,q2,q1,q0
I_14
q[3:0]
q[3]
q[2]
q[1]
q[0]
b[3:0]
ldout

# Lesson 1 – Setting Up the Project

In Lesson 1 you will get ready to start the tutorial project.

Tasks covered in this lesson are:

- **Task 1**: Create a Project Directory
- **Task 2**: Create a New Project
- **Task 3**: Copy Schematic Symbols to the Project Directory



Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

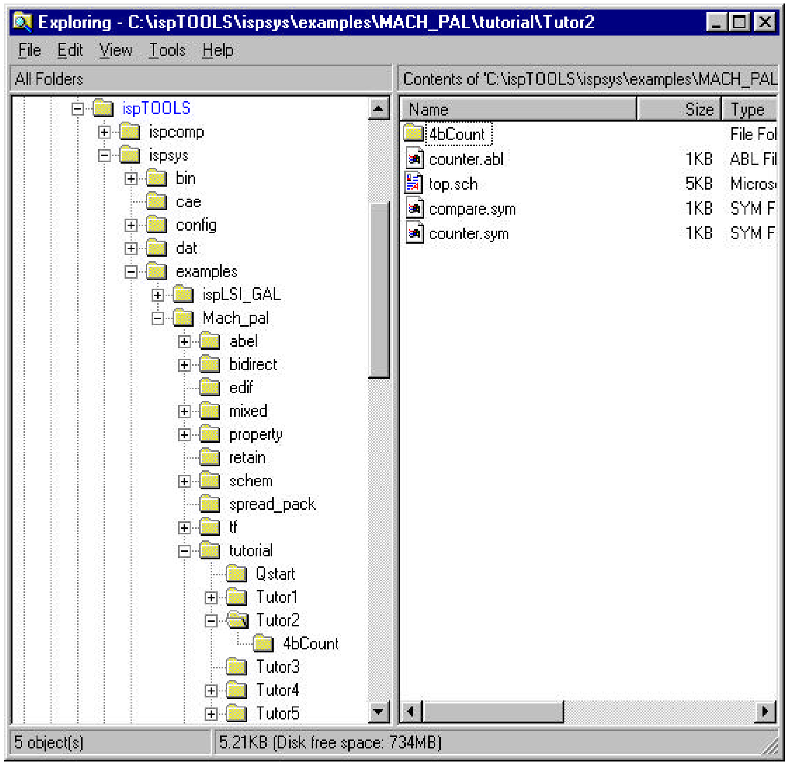
Start or bring the Library Manager to the foreground

# Task 1 *Create a Project Directory*

Before you start this tutorial, you need to create a project directory for all of your tutorial design files.

*To create a project directory*:

1. Start Windows Explorer, or similar tool.
2. Go to the `\ispTOOLS\ispsys\examples\MACH_pal\tutorial\Tutor2` directory.
3. In Explorer, create the directory **4bCount**.



| Name | Size | Type |
|---|---|---|
| 4bCount | | File Fol |
| counter.abl | 1KB | ABL Fil |
| top.sch | 5KB | Micros |
| compare.sym | 1KB | SYM F |
| counter.sym | 1KB | SYM F |

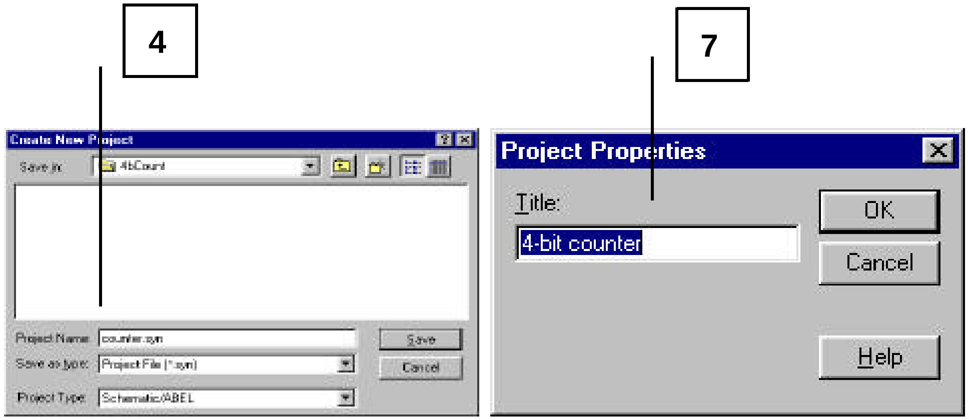
# Task 2 *Create a New Project*

ispDesignExpert employs the concept of a project. A project is a design. Each project has its own directory in which all source files, intermediate data files, and resulting files are stored.

The first step to start a project is to create a project directory. Then, you need to name the project (.syn) file, which the Project Navigator uses later to reload the project.

*To create a new project*:

1. Start ispDesignExpert if it is not already running.
2. In the Project Navigator, choose **File** ⇒ **New Project** to open the Create New Project dialog.
3. Go to the new **4bCount** directory.
4. The default project name is `Untitled.syn`. The project name can be up to 8 characters long, spaces are not allowed. For this tutorial, name the project file **`counter.syn`**.
5. Click **Save**. The untitled generic project appears in the Sources window of the Project Navigator.
6. In the Sources window, double-click the title of the project (Untitled) to open the Project Properties dialog.
7. Type the name **`4-bit counter`** for the title of your project.
8. Click **OK**. The new project title appears in the Sources window.
9. in the Sources window, double-click the device to open the Device Selector dialog. Select the **MACH 4** device family. Accept the default settings and click **OK**.



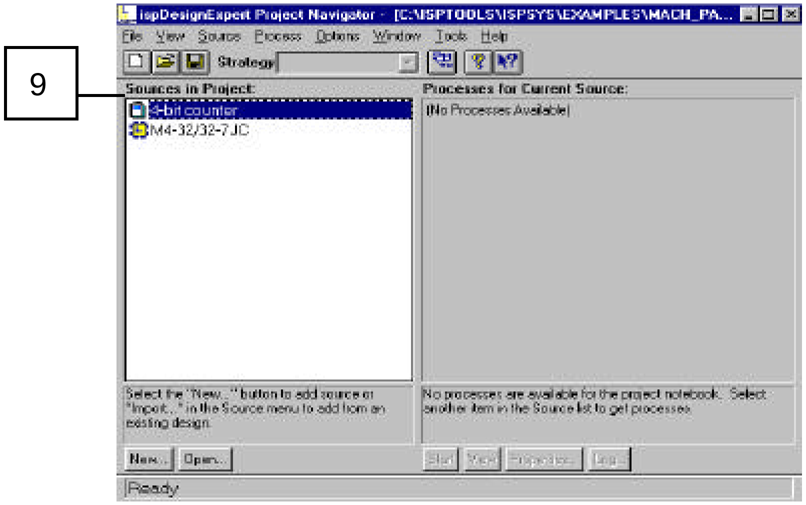
Save in: 4bCount

Project Name: counter.syn

Save as type: Project File (*.syn)

Project Type: Schematic/ABEL

Title: 4-bit counter



ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

Sources in Project:

4-bit counter

M4-32/32-7JC

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

# Task 3 *Copy Schematic Symbols to the Project Directory*

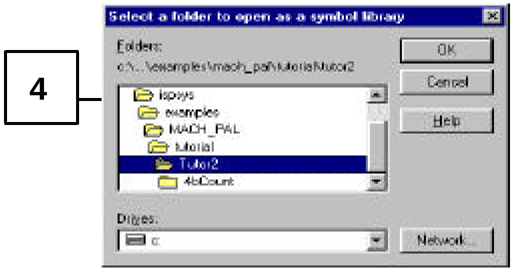
A schematic is composed of symbols, wires, I/O markers, graphics, and text. Symbols are graphic representations of components. The term “symbol” usually refers to an electrical symbol, such as a gate or a sub-circuit. You can draw graphic-only symbols (such as title blocks) with the Symbol Editor, but these have no electrical meaning.

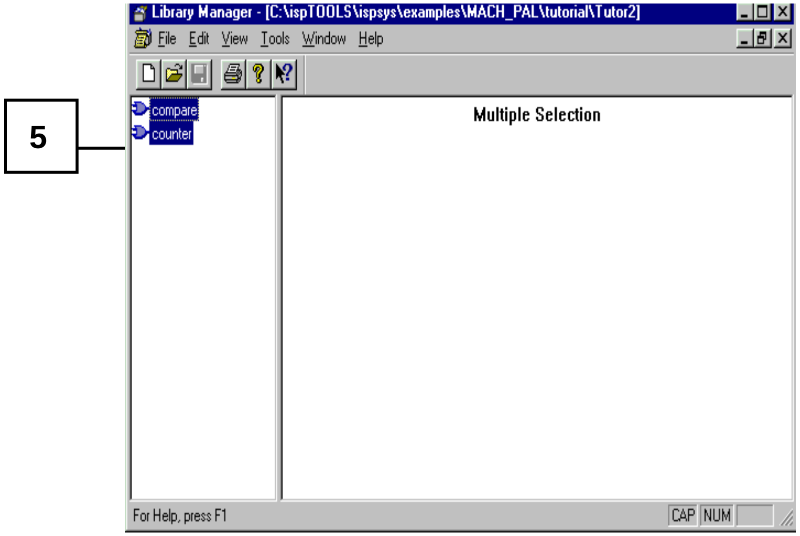
Symbols are the most basic elements of a schematic. Symbols represent primitive design elements, whether those elements are individual transistors, complete gates, or a complex IC. A symbol can also be the hierarchical representation of a sub-circuit (a “Block” symbol).

In this Step you will copy two symbol files to your project directory so you can use these pre-made symbols in your design.

*To copy schematic symbols to the project directory*:

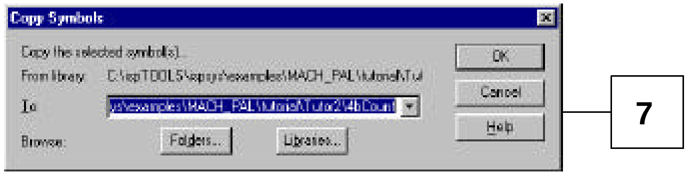
1. In the Project Navigator, choose **Window** ⇒ **Library Manager**.
2. In the Library Manager, choose **File** ⇒ **Open Folder** to open the dialog.
3. Go to the `\ispTOOLS\ispsys\examples\Mach_pal\tutorial\Tutor2` directory.
4. Click **OK** to open the library in the Library Manager.
5. Select the two symbols (**compare** and **counter**).
6. In the Library Manager, choose **Edit** ⇒ **Copy Symbol** to open the Copy Symbols dialog.


4
Select a folder to open as a symbol library
Folders:
c:\...\examples\mach_pal\tutorial\tutor2
ispsys
examples
MACH_PAL
tutorial
Tutor2
4bCount
Drives:
c:
OK
Cancel
Help
Network...


5
Library Manager - [C:\ispTOOLS\ispsys\examples\MACH_PAL\tutorial\Tutor2]
File Edit View Tools Window Help
compare
counter
Multiple Selection
For Help, press F1
CAP NUM

# Copy Schematic Symbols to the Project Directory (continued)

7. Click **Folders**, go to the **4bCount** folder, and then click **OK**.
8. Click **OK** to close the dialog.
9. Exit the Library Manager.



Copy the selected symbol(s)...

From library: C:\ispTOOLS\ispsys\examples\MACH_PAL\tutorial\Tut

To: ys\examples\MACH_PAL\tutorial\Tutor2\4bCount

Browse:

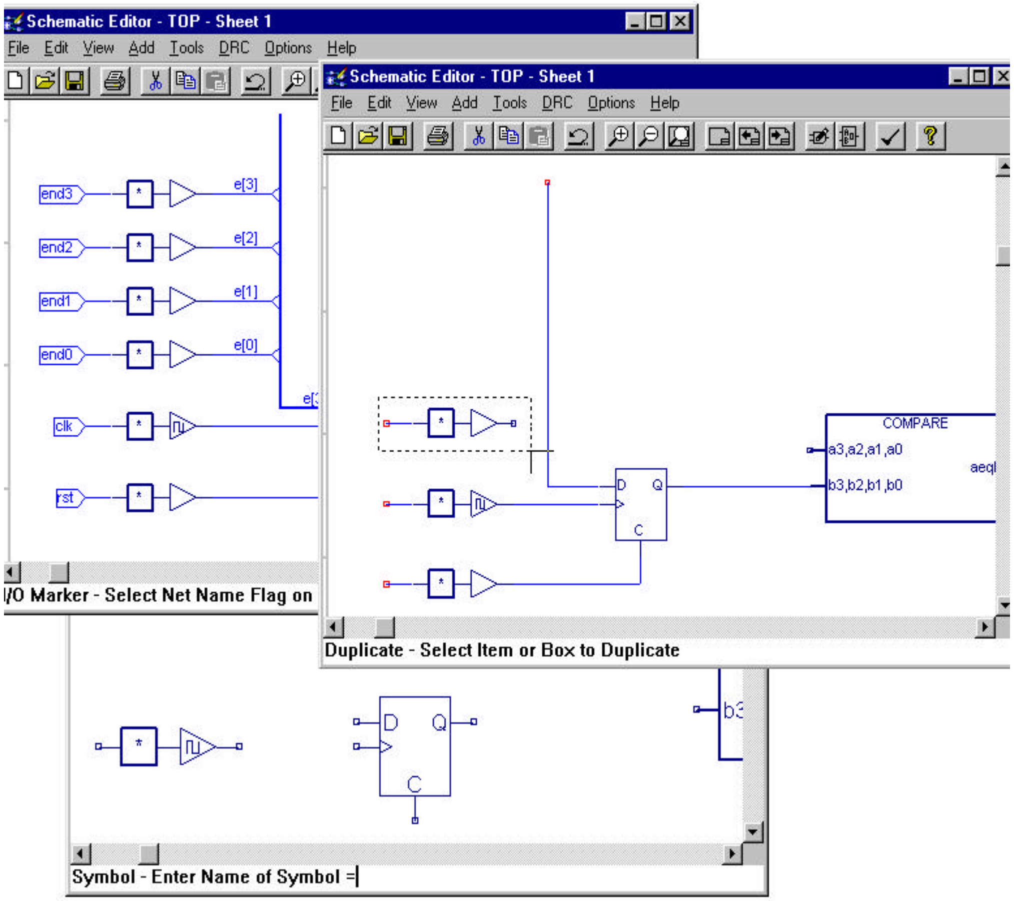
# *Lesson 2 – Creating a Top-Level Schematic Source*

In Lesson 2, you will begin creating a top-level schematic source for the project.

Steps covered in this lesson are:

- **Task 4**: Add a New Schematic to the Project
- **Task 5**: Resize the Schematic Sheet
- **Task 6**: Place Two Block Symbols from the Local Symbol Library
- **Task 7**: Place a Symbol from the REGS Generic Symbol Library
- **Task 8**: Place Three Symbols from the IOPAD Generic Symbol Library
- **Task 9**: Add Wires to Connect the Symbols
- **Task 10**: Add Wires to Connect the Symbols (con't)
- **Task 11**: Duplicate the Input Pad and Wire Stub
- **Task 12**: Name the Buses
- **Task 13**: Add Bus Taps with Signal Names
- **Task 14**: Add Input Net Names
- **Task 15**: Add Data Input Net Names
- **Task 16**: Create Iterated Instances of the Flip-Flop
- **Task 17**: Add Input Markers

When you are finished with this lesson, the schematic should look like the one on the right.


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
end3
end2
end1
end0
e[3]
e[2]
e[1]
e[0]
e[
clk
rst
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
D
Q
C
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeql
D
Q
C
b3

I/O Marker - Select Net Name Flag on

Duplicate - Select Item or Box to Duplicate

Symbol - Enter Name of Symbol =

# Task 4 *Add a New Schematic to the Project*

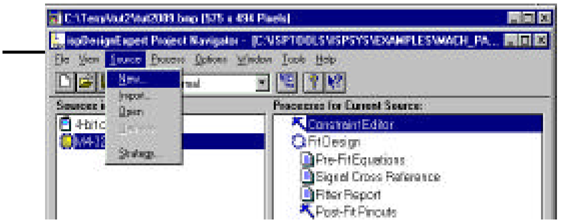
Designing top-down, we'll first create the top-level source for the project. It can be any type of source. Because this design is ABEL-HDL-based, you can use either an ABEL-HDL or schematic source at the top level. For this tutorial we'll use a schematic.

*To add a new schematic source to the project*:

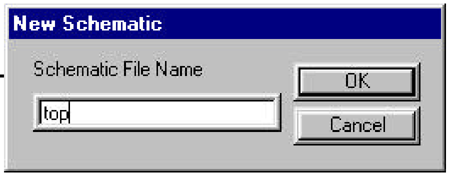
1. In the Project Navigator, choose **Source** ⇒ **New** to open the New Source dialog.
2. Select **Schematic**, and then click **OK**. The Schematic Editor opens and prompts you to enter a file name for the schematic.
3. Type the name **top**, and then click **OK**.

   The Schematic Editor names the current schematic sheet as *top*, and the software imports the schematic into the Project Navigator as a new source file.

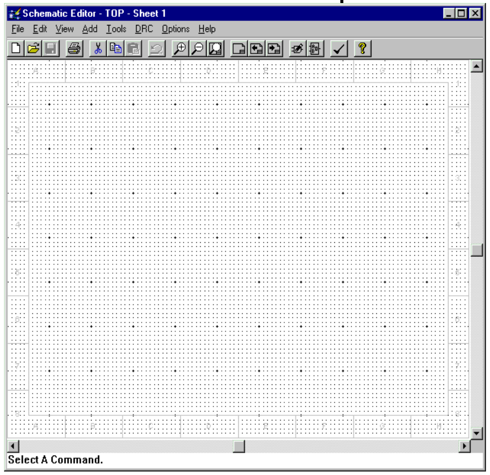
1

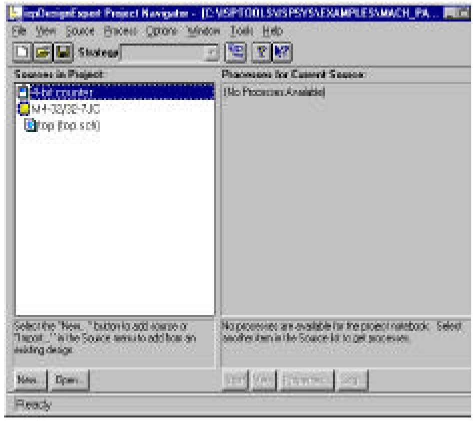

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Process Options Window Tools Help
New...
Import...
Open
Strategy...
Sources i
4-bit c
M4-32
Processes for Current Source:
Constraint Editor
Fit Design
Pre-Fit Equations
Signal Cross Reference
Fitter Report
Post-Fit Pinouts

3



Schematic File Name: top


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
Select A Command.

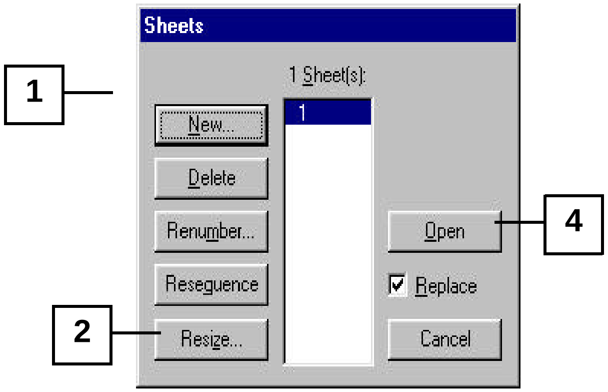

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
4-bit counter
M4-32/32-7JC
top (top.sch)
Processes for Current Source:
(No Processes Available)
New...
Open...
Ready

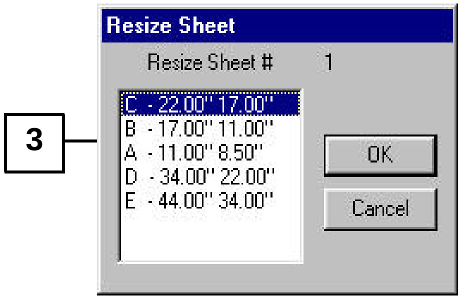
# Task 5 *Resize the Schematic Sheet*

You can resize a schematic sheet using the **Resize** command. The **Resize** command takes effect immediately and is applied to the sheet selected in the Sheets dialog, not the active sheet or the sheet currently being worked on.

*To resize the schematic sheet*:

1. Choose **File** ⇒ **Sheets** to open the Sheets dialog. Because there is only one sheet in the schematic, you cannot select another sheet.
2. Click **Resize** to open the Resize Sheets dialog. The current size of the selected sheet is highlighted. Other available sheet size choices are listed.
3. Select **B**, and then click **OK** to close the Resize Sheet dialog.
4. Click **Open**. The software resizes the sheet in the Schematic Editor.





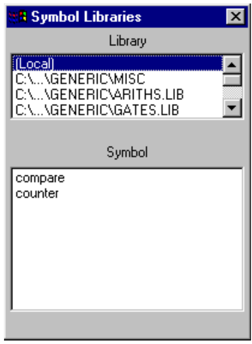
# Task 6 *Place Two Block Symbols from the Local Symbol Library*

The first step in this top-down design is to create block symbols to represent lower-level modules in the design. Later, you will design the I/O ports of the lower-level ABEL-HDL sources to match the names of the pins on the corresponding block symbols.

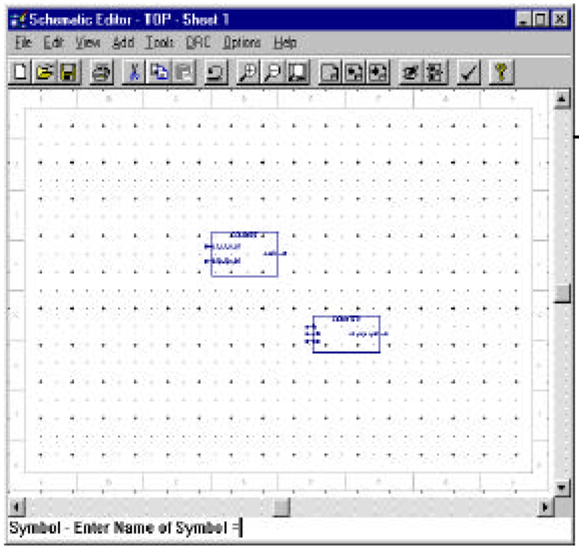
To place the block symbols in the schematic:

1. Choose **Add** ⇒ **Symbol** to open the Symbol Libraries dialog.
2. Under Library, select **Local**. This is the library in the project folder you created and copied two block symbols into at the beginning of this tutorial in Task 3.
3. Under Symbol, select **compare**. The symbol is attached to the cursor.
4. Move the cursor to the upper middle of the schematic and click to place the symbol.
5. Right-click to remove the symbol from the cursor.
6. Select the **counter** symbol.
7. Move the cursor to the middle of the schematic and click to place the symbol.
8. Again, right-click to remove the symbol from the cursor.
9. Leave the dialog open. You will continue to use it in the next step.

***Note****: It is not critical that your schematic look “exactly” like the example. Yours may look different depending on several unimportant factors that do not affect the proper use of this tutorial.*



1


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help

Symbol - Enter Name of Symbol =

3-8

# Task 7 *Place a Symbol from the REGS Generic Symbol Library*

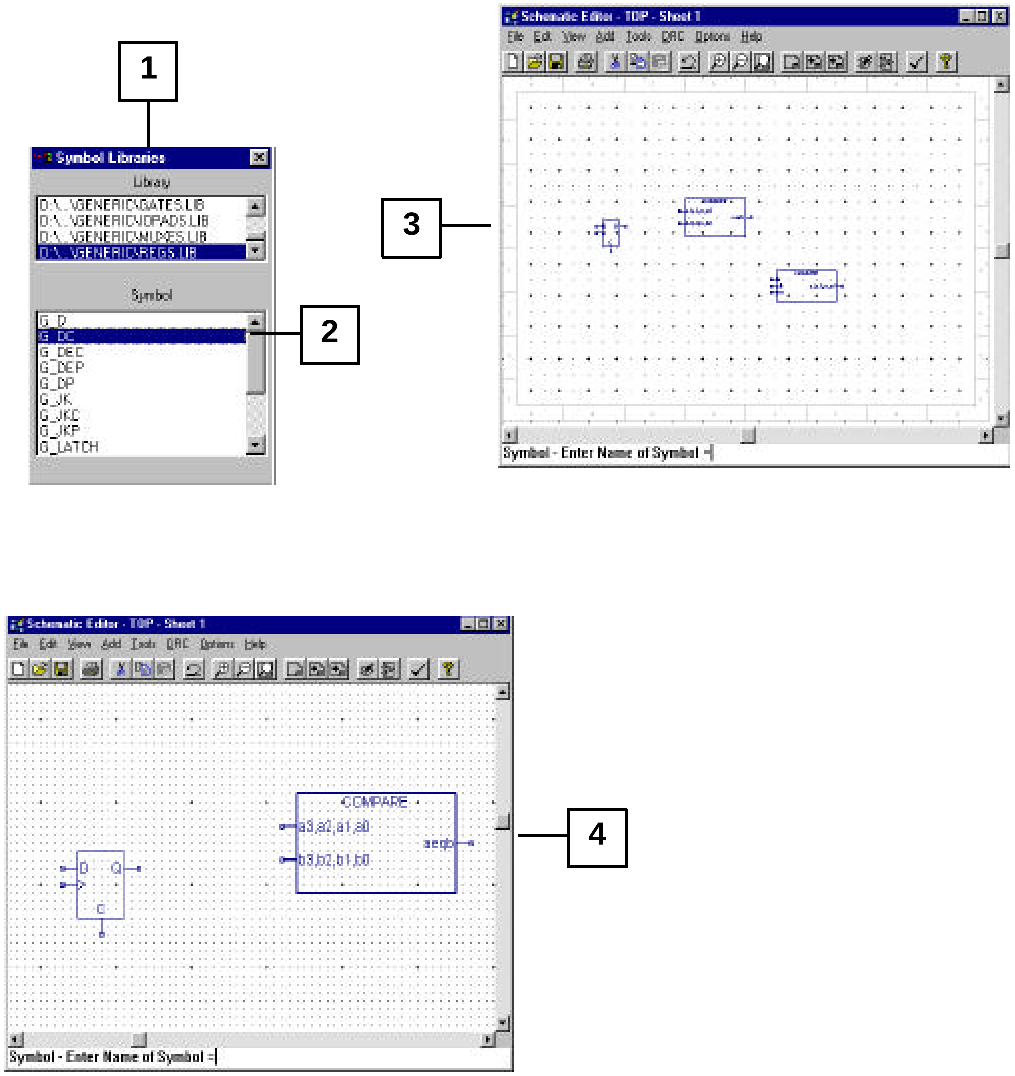
The target device selected for the project determines which symbol libraries are available.

If you use symbols from the Generic Symbol Library, you can migrate designs to different devices without having to redraw the schematic.

To place a symbol from the REGS generic symbol library:

***Note**: You can use the Drawing Toolbar to add symbols and other schematic drawing functions. To display the Drawing Toolbar, choose **View** ⇒ **Drawing Toolbar**.*

1. In the Symbol Libraries dialog, under Library, select GENERIC\REGS.LIB.
2. Under Symbol, select **G_DC**.
3. Place the symbol so the **G_DC** symbol's output is aligned with the **b** input pin on the Compare block symbol. (Ignore the title block in the schematic.)
4. Choose **View** ⇒ **Zoom In** and drag an area to zoom in to a view similar to the one on the right.


1
Symbol Libraries
Library
D:\...\GENERIC\GATES.LIB
D:\...\GENERIC\IOPADS.LIB
D:\...\GENERIC\MUXES.LIB
D:\...\GENERIC\REGS.LIB
Symbol
G_D
G_DC
G_DEC
G_DEP
G_DP
G_JK
G_JKC
G_JKP
G_LATCH
2
3
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
Symbol - Enter Name of Symbol =
4
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb
D
Q
C
Symbol - Enter Name of Symbol =

# Task 8 *Place Symbols from the IOPAD Generic Symbol Library*

In this step you will continue adding symbols to the schematic. However, you will use the IOPADS generic symbol library.

***Tip**: You can turn grid display off by choosing **Options ⇒ Preferences**.*

*Add a clock buffer symbol*:

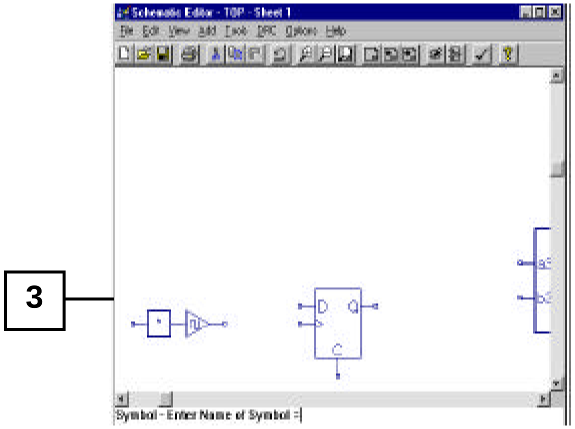
1. In the Symbol Libraries dialog, under Library, select GENERIC\IOPADS.LIB.
2. Under Symbol, select **g_clkbuf**.
3. Place the symbol so that the output is aligned with the **clk** input pin on the **g_dc** symbol.

***Note**: The spacing of symbols in the schematic is very important. If symbols are placed too close together, you will not be able to add wires, bus taps, etc. between the symbols. In the following step, make sure the horizontal distance between the **g_clkbuf** symbol and **g_dc** symbol is equal to **at least the width of the g_clkbuf symbol** (see the picture to the right).*

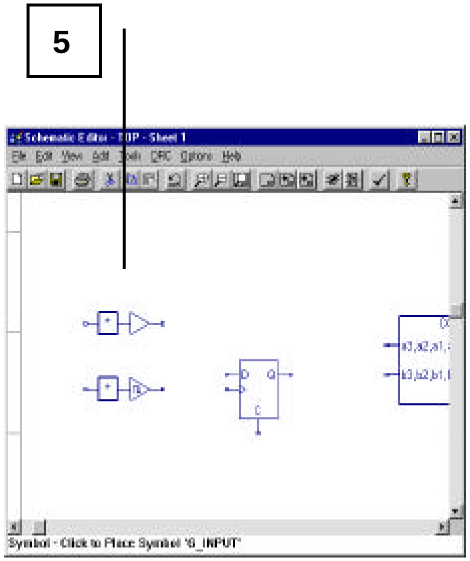
*Add two input buffer symbols*:

4. Under Symbol, select **g_input**
5. Click once to place an instance. (Try to align symbols vertically as shown in the picture.)
6. Click once again to place an instance.

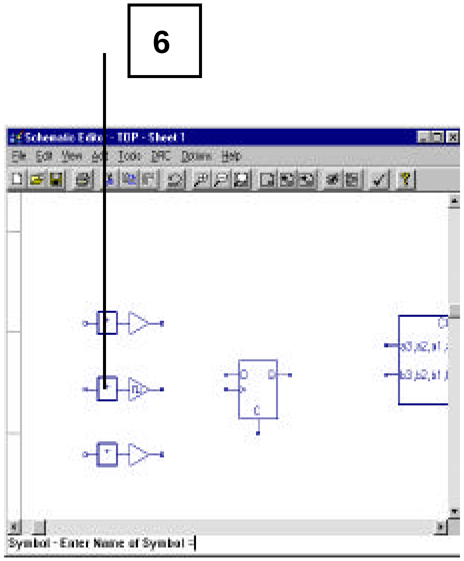
***Note**: The **Add Symbol** command will be canceled when you select the next command in the next section.*


3
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
D Q
C

Symbol - Enter Name of Symbol :|


5
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
D Q
C

Symbol - Click to Place Symbol 'G_INPUT'


6
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
D Q
C

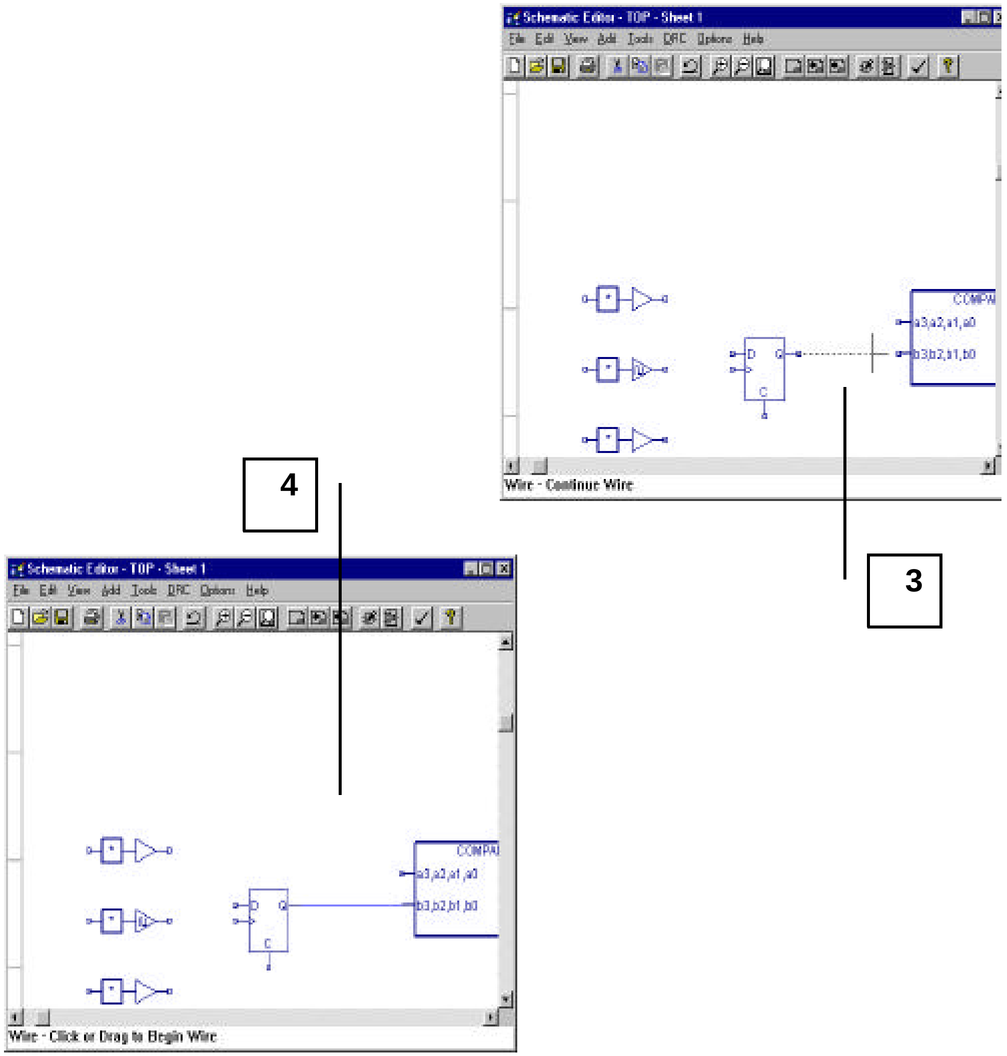
Symbol - Enter Name of Symbol :|

# Task 9 *Add Wires to Connect the Symbols*

The next step is adding wires and buses to interconnect the symbols. You draw wires and buses the same way; the Schematic Editor knows if a wire is a bus or a single net by the wire’s name. In this task, you will draw all of the wires. Later, you will add names to the wires.

*Connect the flip-flop output to the Compare symbol*:

1. Choose **Add** ⇒ **Wire**.
2. Click the **Q** output of the flip-flop
3. Drag the wire across to the **b** input of **Compare**.
4. Click on the **b** pin to end the wire segment.


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPA
a3,a2,a1,a0
b3,b2,b1,b0
D
Q
C
4
3

Wire - Continue Wire

Wire - Click or Drag to Begin Wire

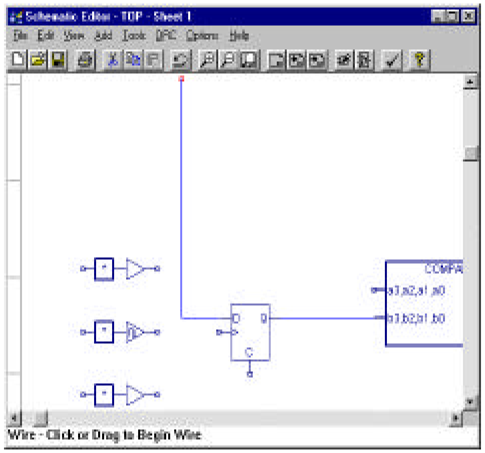
# Task 10 *Add Wires to Connect the Symbols*

In the continuation of this step, you will add three wires to the flip-flop. Also, you will add wire stubs to the buffers

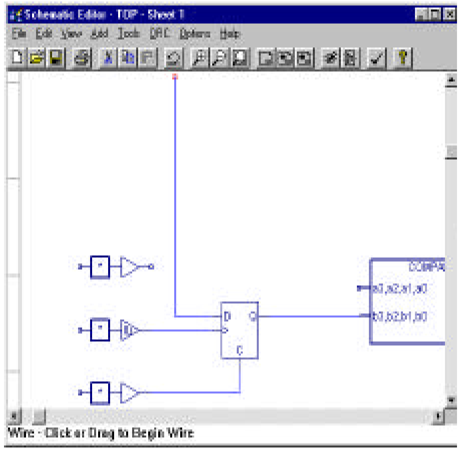
The length of the horizontal and vertical segments of the D input wire (Step 5) is important. The wire segments must be long enough so that you will have room to add a bus name to the horizontal wire segment and add bus taps between the vertical wire segment and input buffers.

*Add a wire from D input*:

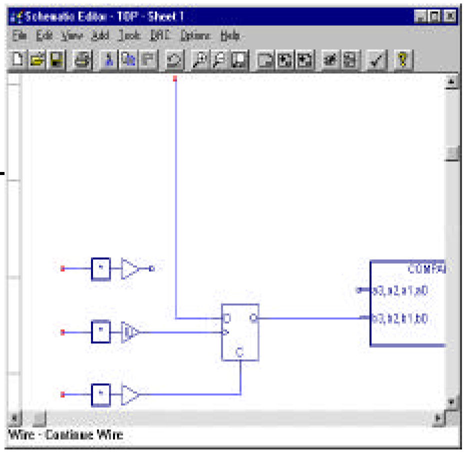
1. Click the **D input**. Move the cursor to the left to create a horizontal segment with a length equal to about half the horizontal distance between the input buffer and flip-flop. Click once to end the segment.
2. Move the cursor up until the vertical height of the wire is about equal to 3 times the height of the flip-flop.
3. Double-click to end the wire.
4. Add a wire from the **C input** to the **input buffer**.
5. Add wire from the **clock input** to the **clock buffer**.
6. Add wire stubs (short wires) to the **input buffers** and the **clock buffer**. (Double-click to end a wire in space, or use the right mouse button to cancel the command.)


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPA
a3,a2,a1,a0
b3,b2,b1,b0
D
Q
C
1-3

Wire - Click or Drag to Begin Wire


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPA
a3,a2,a1,a0
b3,b2,b1,b0
D
Q
C
4-5

Wire - Click or Drag to Begin Wire


6
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPA
a3,a2,a1,a0
b3,b2,b1,b0
D
Q
C

Wire - Continue Wire

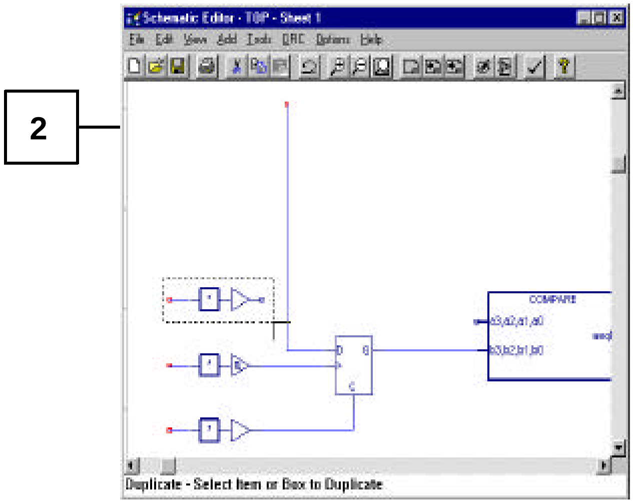
# Task 11 *Duplicate the Input Pad and Wire Stub*

This step shows you how to use the **Duplicate** command to quickly add the rest of the input pads.

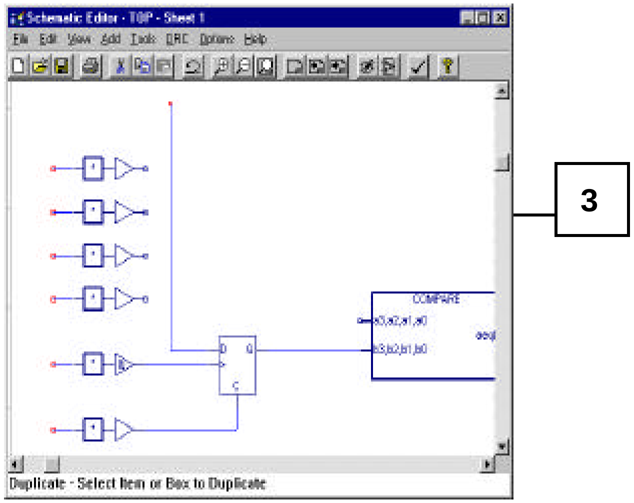
The **Duplicate** command lets you copy one or more elements, then place them at different locations within the same symbol or schematic. You can place the duplicated item as many times as you want until you select another command. **Duplicate** differs from the **Copy / Paste** command sequence only in that it does not change the contents of the clipboard.

*To duplicate the input buffer*:

1. Choose **Edit** ⇒ **Duplicate**.
2. Hold down the mouse button and **drag a region** around the input buffer and wire stub.
3. Click to place the duplicated buffer and wires until there are 4, as shown in the drawing on the right.
4. Right-click to cancel the command.


2
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb
D
Q
C

Duplicate - Select Item or Box to Duplicate


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb
D
Q
C
3

Duplicate - Select Item or Box to Duplicate

# Task 12 *Name the Buses*

Any single- or multi-wire connection between pins is called a network, or net. A bus is a combination of two or more signals into a single wire. Buses are a convenient way to group related signals. This grouping can produce a less cluttered, functionally clearer drawing and clarify the connection between the main circuit and a Block symbol.

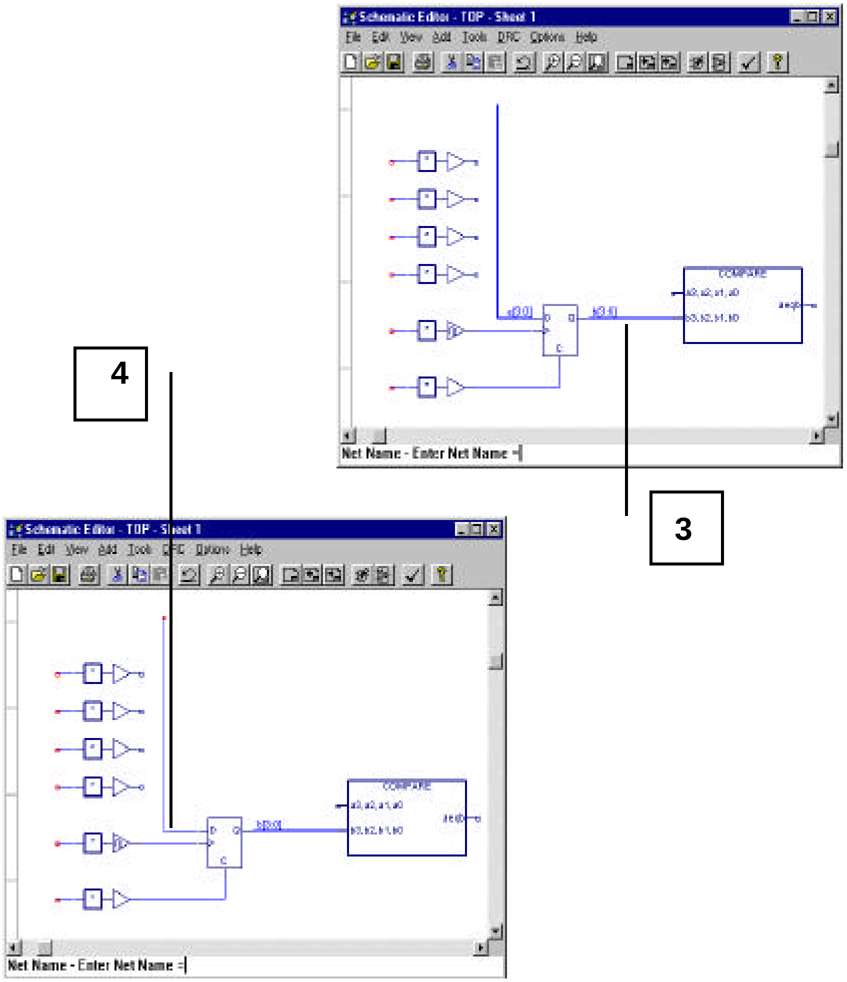
There are two types of buses: *ordered* and *unordered*. An ordered bus has a compound name consisting of the names of the signals that comprise the bus. Any signals can be combined into an ordered bus, whether or not they are related.

A net becomes an ordered bus when it is given a *compound name*. You form a compound name by adding a sequence of numbers to the name. The sequence is specified as a starting number, an ending number, and an optional increment (default = 1). The numbers are positive integers, and are delimited by commas ( **,** ), dashes ( – ), or colons ( **:** ). The sequence is enclosed in brackets **[ ]**, parentheses **( )**, or curly braces **{ }.**

*To name the buses*:

1. Choose **Add** ⇒ **Net Name**.
2. In the status area at the bottom of the Schematic Editor, type the name of the bus: **b[3:0]**, and then press **Enter**. The name attaches to the cursor.
3. Click the wire between the flip-flop and the compare symbol to place the name on the wire. Also, when a wire is named as a bus, its shape thickens to indicate it is a bus.
4. Now name another bus. In the status area, type the name: **e[3:0]**, and then press **Enter**.
5. Click the horizontal segment of the wire connected to the flip-flop input.

***Note****: Names should be placed on wires, not pins.*


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
e[3:0]
b[3:0]
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb
4
3
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
b[3:0]
COMPARE
a3,a2,a1,a0
b3,b2,b1,b0
aeqb

Net Name - Enter Net Name =

Net Name - Enter Net Name =

# Task 13 *Add Bus Taps with Signal Names*

Signals enter and exit a bus at points called bus taps. A bus tap can be added to any existing bus, net, or wire. If a net or wire is not already a bus, adding the tap automatically promotes it to a bus.

You can add bus taps only on vertical or horizontal sections of a bus. Tap connections are shown with two diagonal lines, rather than a solder dot.

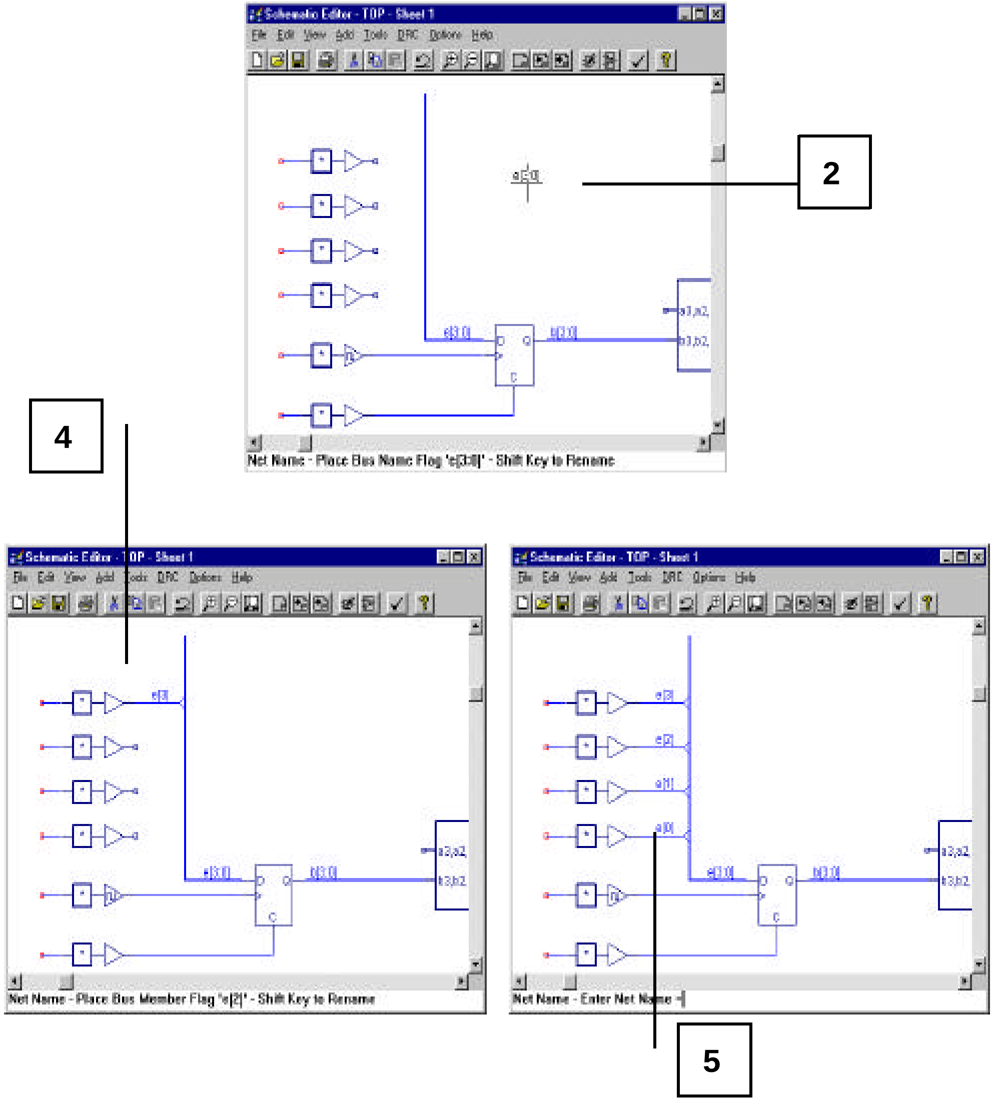
There are several ways to add bus taps. The following procedure shows you how to create a tap, the connecting wire, and the net name in one simple step using the **Net Name** command.

*To add bus taps with signal names*:

1. Choose **Add** ⇒ **Net Name**.
2. Click the bus labeled **e[3:0]**. The cursor picks up the name of the bus.
3. Right-click once to split the bus name into its individual signal names.

   The signal name **e[3]** is attached to the cursor.
4. In one action, click the pin of the top input pad, drag a wire to the bus, and then release the mouse button.

   The software adds a bus tap, wire, and signal label. Notice that the signal name decrements.
5. Add the remaining taps (in descending order) just by clicking on the pins of the buffers.


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
2
4
5
e[3:0]
b[3:0]
a3,a2,
b3,b2,
e[3]
e[2]
e[1]
e[0]
D
Q
C

Net Name - Place Bus Name Flag 'e[3:0]' - Shift Key to Rename

Net Name - Place Bus Member Flag 'e[2]' - Shift Key to Rename

Net Name - Enter Net Name -

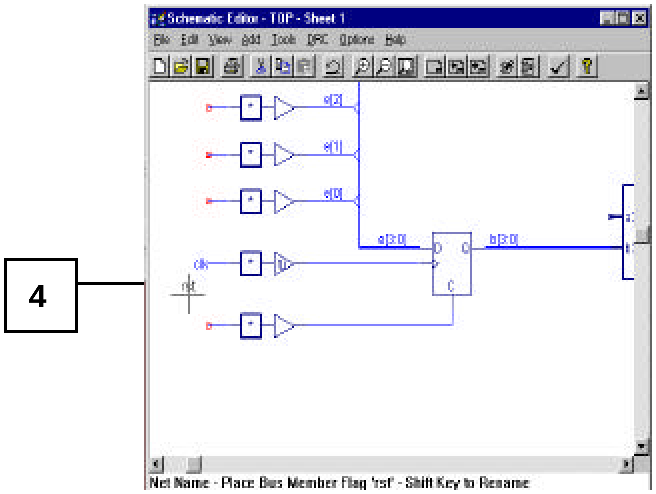
# Task 14 *Add Input Net Names*

Every net has a name, either assigned by you or by the Schematic Editor. You can override any name assigned by the Schematic Editor by assigning one of your own using the **Add** ⇒ **Net Name** command.

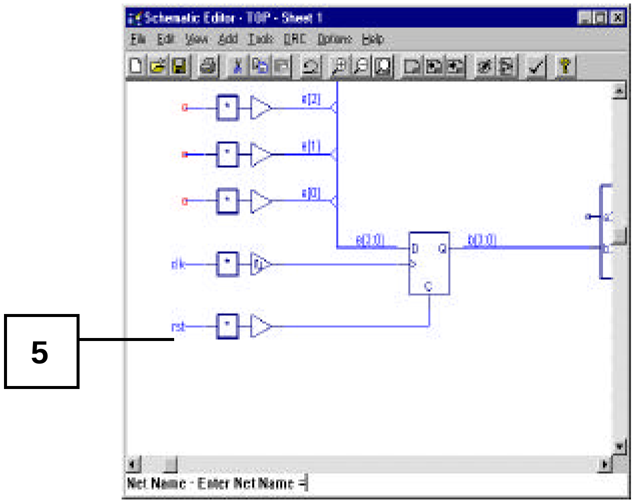
You can name nets one at a time. A faster way is to create a compound name (in this example, a group of unique names), and then sequentially attach individual names of a compound name to different nets.

*To add a compound net name*:

1. Choose **Add** ⇒ **Net Name**.
2. In the status area, type: **clk, rst**, and then press **Enter**. (Don’t forget the comma separating the names.)
3. Notice that both names are attached to the cursor. Right-click once to separate the names. Now only **clk** is showing.
4. Click the end of the input wire for clock buffer. The software adds the first name ( **clk**) to the wire. Also notice that the next name in the list (**rst**) appears on the cursor.
5. Click the end of the rst input buffer to add the final name (**rst**) to the wire.


4
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
a[2]
a[1]
a[0]
a[3:0]
b[3:0]
clk
rst
D
Q
C

Net Name - Place Bus Member Flag 'rst' - Shift Key to Rename


5
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
a[2]
a[1]
a[0]
a[3:0]
b[3:0]
clk
rst
D
Q
C

Net Name - Enter Net Name =

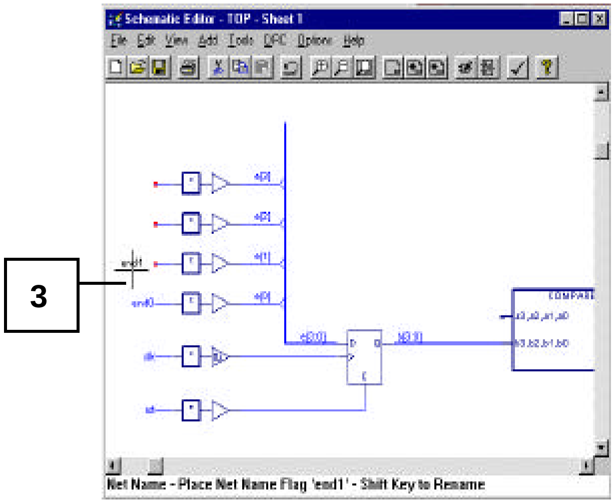
# Task 15 *Add Data Input Net Names*

Another net naming feature makes it easy to deal with buses by automatically incrementing the net name as you place it. In this step, you will add net names to the end segments, and the Schematic Editor will automatically increment the name.

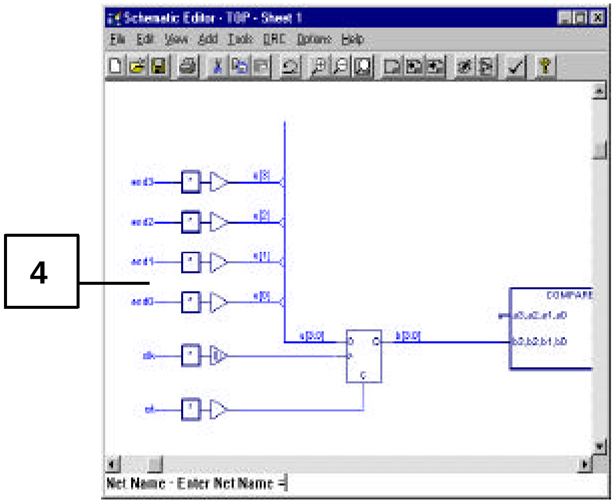
*To add sequential net names*:

1. Choose **Add** ⇒ **Net Name**.
2. In the status area, type: **end0+**, and then press **Enter**. The name is attached to the cursor.

   This tells the Schematic Editor to name the signal **end**, to start numbering at **0**, and to increment (**+**) the numbers as the names are placed.
3. Click on the bottom data input wire stub. The Schematic Editor places the name **end0** and automatically increments the net name.
4. Click on the next wire stub. Repeat until all data input wire stubs have net names.
5. Right-click when **end4** appears on the cursor to cancel the command.


3
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
end1
end0
COMPARE

Net Name - Place Net Name Flag 'end1' - Shift Key to Rename


4
Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
end3
end2
end1
end0
COMPARE

Net Name - Enter Net Name =

# Task 16 *Create Iterated Instances of the Flip-Flop*

A powerful feature in the schematic is its capability of using an iterated instance. Iterated instances allow a single symbol to represent multiple instances connected in parallel.

You can convert a single instance into an iterated instance by giving it a compound instance name of the form:

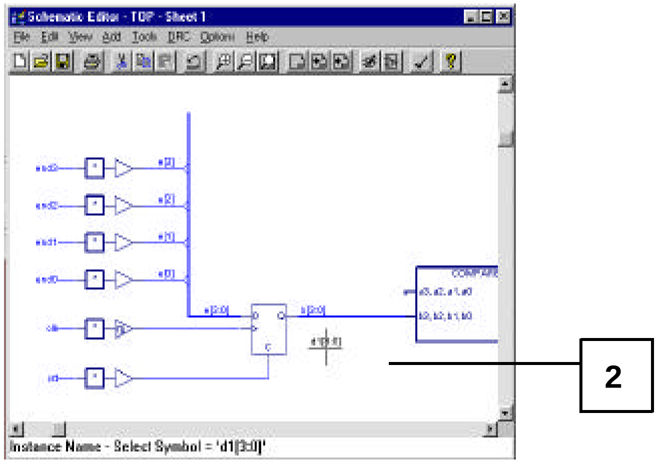
```
INV[3-10]
```

In this case, eight instances of the symbol you've named INV are created, but the symbol appears only once in the schematic.

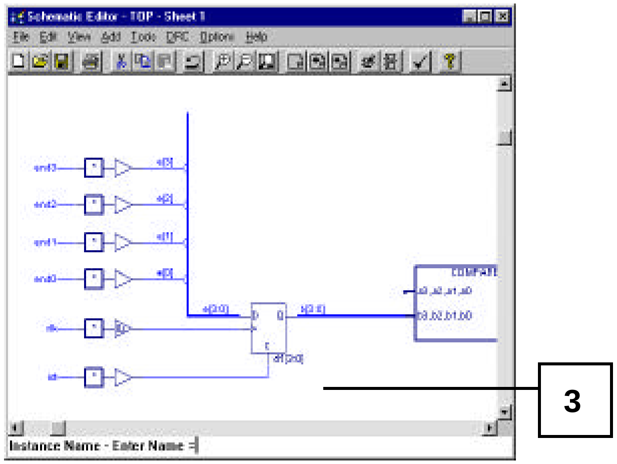
*To create iterated instances of the flip-flop*:

1. Choose **Add** ⇒ **Instance Name**.
2. In the status area, type: **d1[3:0]**, and then press **Enter**. The name is attached to the cursor.
3. Click once on the flip-flop. The Schematic Editor places the label on the symbol.

   The flip-flop is now really four flip-flops, with signal e[3] feeding d[3], e[2] feeding d[2], etc. The common signals are connected in parallel to the common pins (such as clk and rst).


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPARE
2

Instance Name - Select Symbol = 'd1[3:0]'


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
COMPARE
d1[3:0]
3

Instance Name - Enter Name =

# Task 17 *Add Input Markers*

An I/O marker is a special indicator that identifies a net name as a device input, output, or bidirectional signal. This establishes net polarity (direction of signal flow) and indicates that the net is externally accessible.

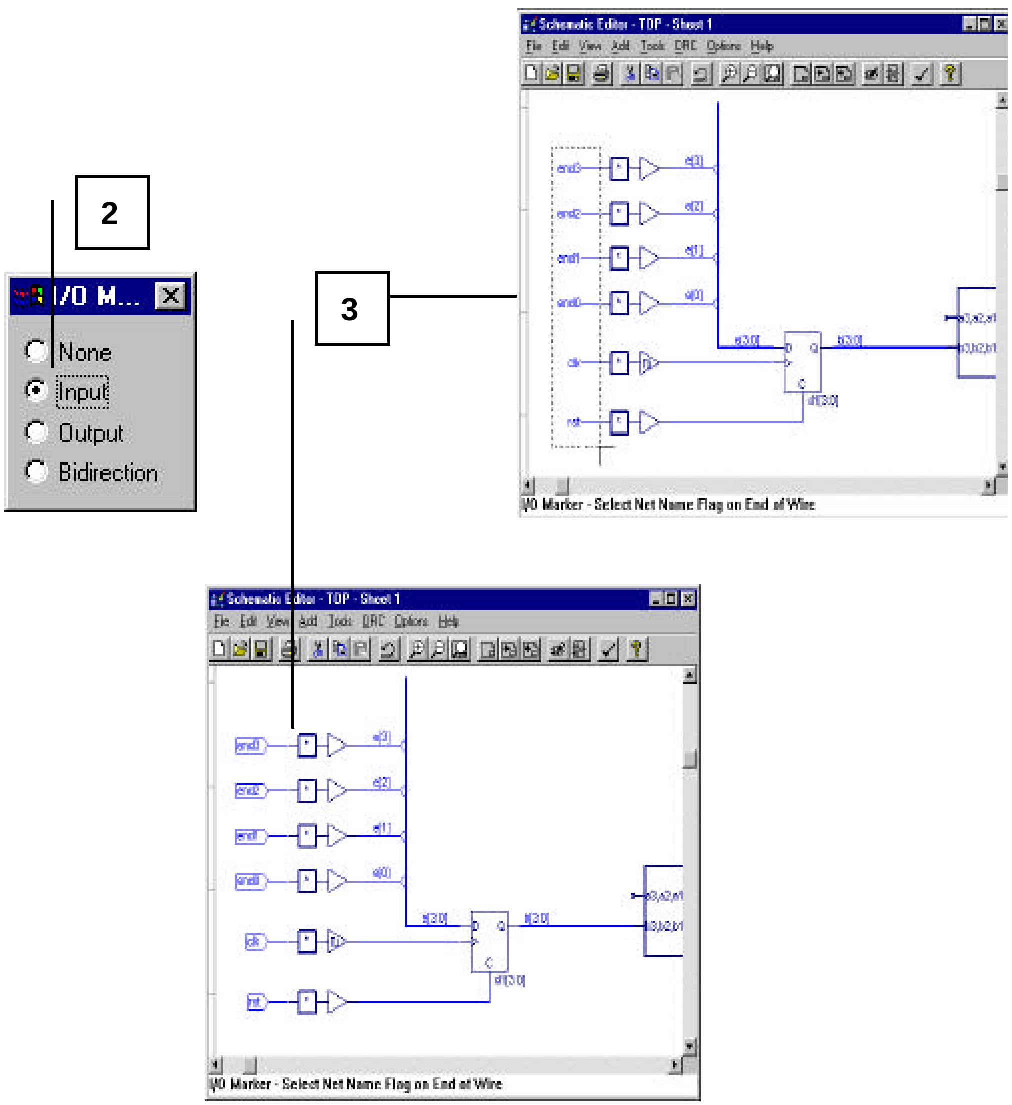
The **Schematic Editor Consistency Check** command uses I/O markers to flag any discrepancies in the polarity of marked signals and the symbol pins. Discrepancies in polarity are also flagged each time you run the Hierarchy Navigator.

*To add input markers*:

1. Choose **Add** ⇒ **I/O Marker** to open the dialog.
2. Select **Input**.

   You can add a marker by clicking at the point where the I/O marker touches the end of a horizontal or vertical wire segment or bus. However, if you have a group of nets that you want to add markers to, there is a faster way.
3. Select all of the input wires at once by dragging a region around them. The Schematic Editor adds markers to all the nets at once.
4. Close the I/O Marker dialog.

***Note**: To remove an I/O marker, select **None**.*



I/O M...

○ None
● Input
○ Output
○ Bidirection

Schematic Editor - TOP - Sheet 1

I/O Marker - Select Net Name Flag on End of Wire

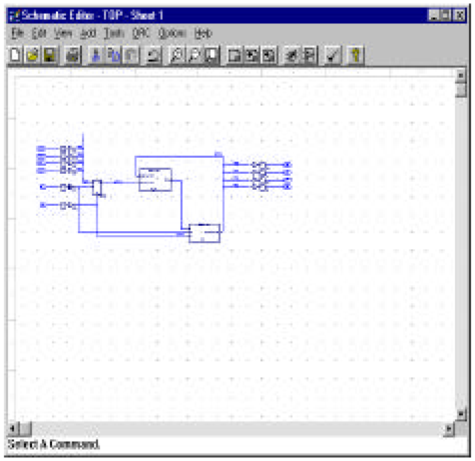
# Lesson 3 – Finishing Up the Schematic

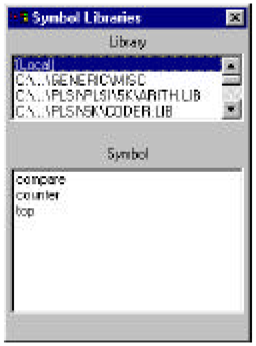
To save time, we have completed the schematic for you.

In this lesson you will remove the schematic source you were building and import a completed source. You will learn how to automatically create a symbol for the currently loaded schematic. Also, you are shown how to check your schematic for design rule violations.

Steps covered in this lesson are:

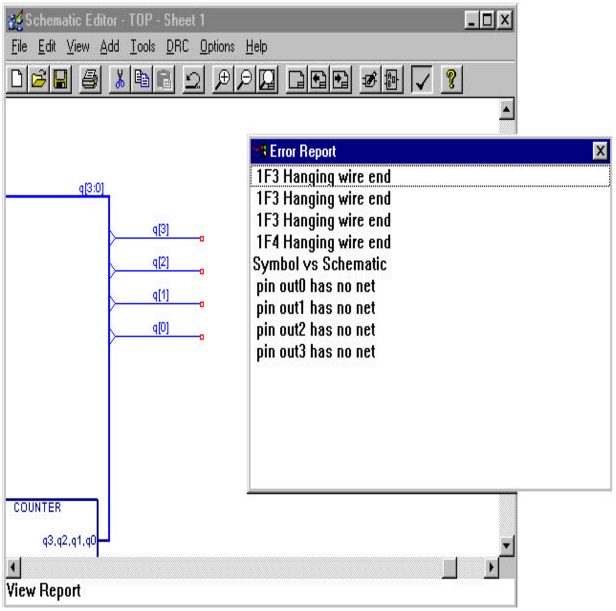
- **Task 18**: Import the completed schematic
- **Task 19**: Create a Matching Symbol
- **Task 20**: Check the Schematic for Consistency Errors


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
Select A Command.



[Local]
C:\...\GENERIC\MISC
C:\...\PLSI\PLSI\5K\ARITH.LIB
C:\...\PLSI\5K\CODER.LIB

compare
counter
top


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
Error Report
q[3:0]
q[3]
q[2]
q[1]
q[0]
COUNTER
q3,q2,q1,q0
View Report

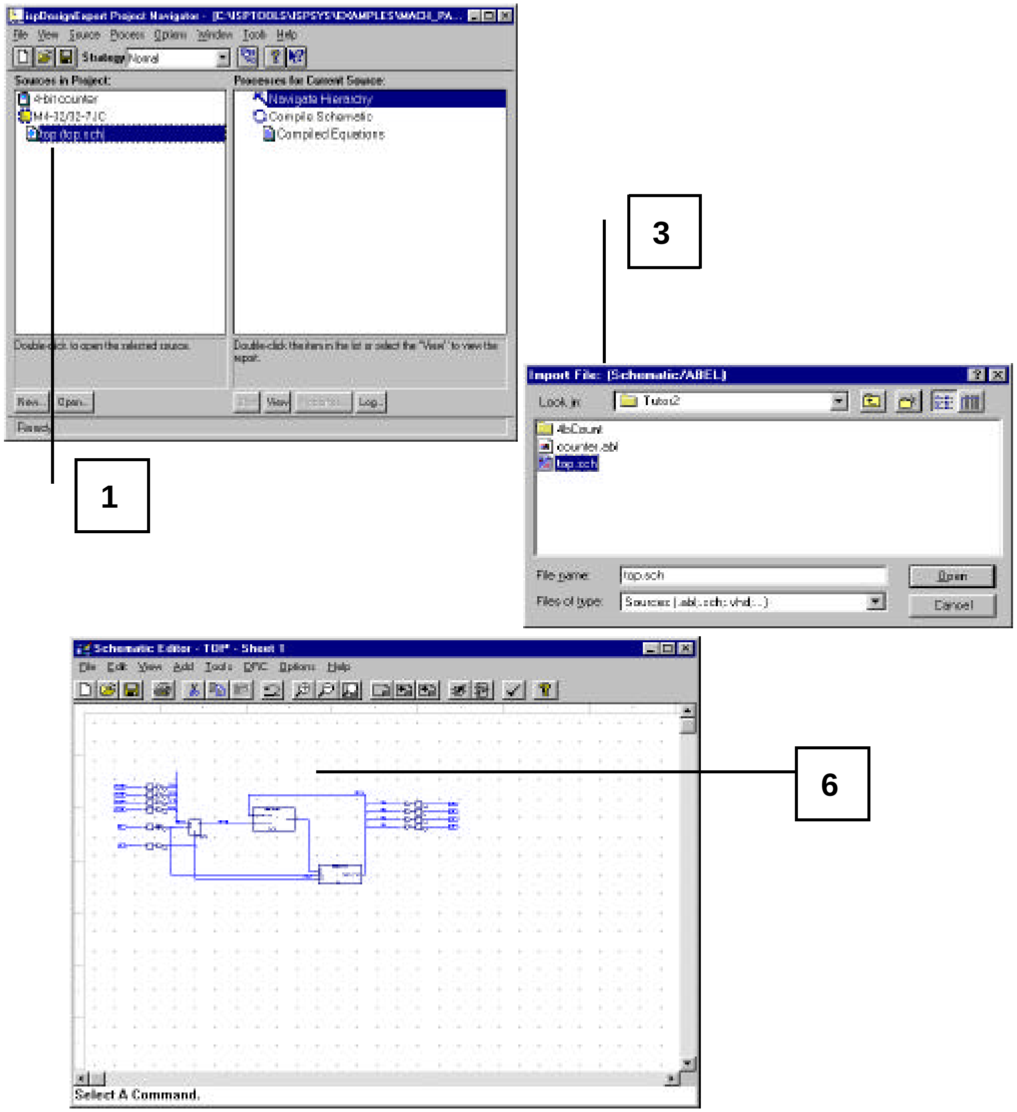
1F3 Hanging wire end
1F3 Hanging wire end
1F3 Hanging wire end
1F4 Hanging wire end
Symbol vs Schematic
pin out0 has no net
pin out1 has no net
pin out2 has no net
pin out3 has no net

# Task 18 *Import the Completed Schematic*

In this step, you will remove the schematic source you have been working on and import the completed schematic of the same name.

*To import the completed schematic*:

1. In the Sources window, select the **top** schematic source.
2. Choose **Source** ⇒ **Remove** to delete the source from the project.
3. Choose **Source** ⇒ **Import** to open the Import Source dialog. Go to the **TUTOR2** directory and select `top.sch`. Then click **OK**.
4. Click **Yes** to confirm file replacement.
5. The completed schematic is now a top-level source in the project.
6. Double-click the **top** source to open the schematic in the editor.



ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

File View Source Process Options Window Tools Help

Strategy: Normal

Sources in Project:
- 4-bit counter
- M4-32/32-7JC
- top (top.sch)

Processes for Current Source:
- Navigate Hierarchy
- Compile Schematic
- Compiled Equations

Double-click to open the selected source.

Double-click the item in the list or select the "View" to view the report.

New... Open... View Log...

Ready

Import File: (Schematic/ABEL)

Look in: Tutor2

- 4bCount
- counter.abl
- top.sch

File name: top.sch

Files of type: Sources (.abl;.sch;.vhd;...)

Open Cancel

Schematic Editor - TOP* - Sheet 1

File Edit View Add Tools DRC Options Help

Select A Command.

# Task 19 *Create a Matching Symbol*

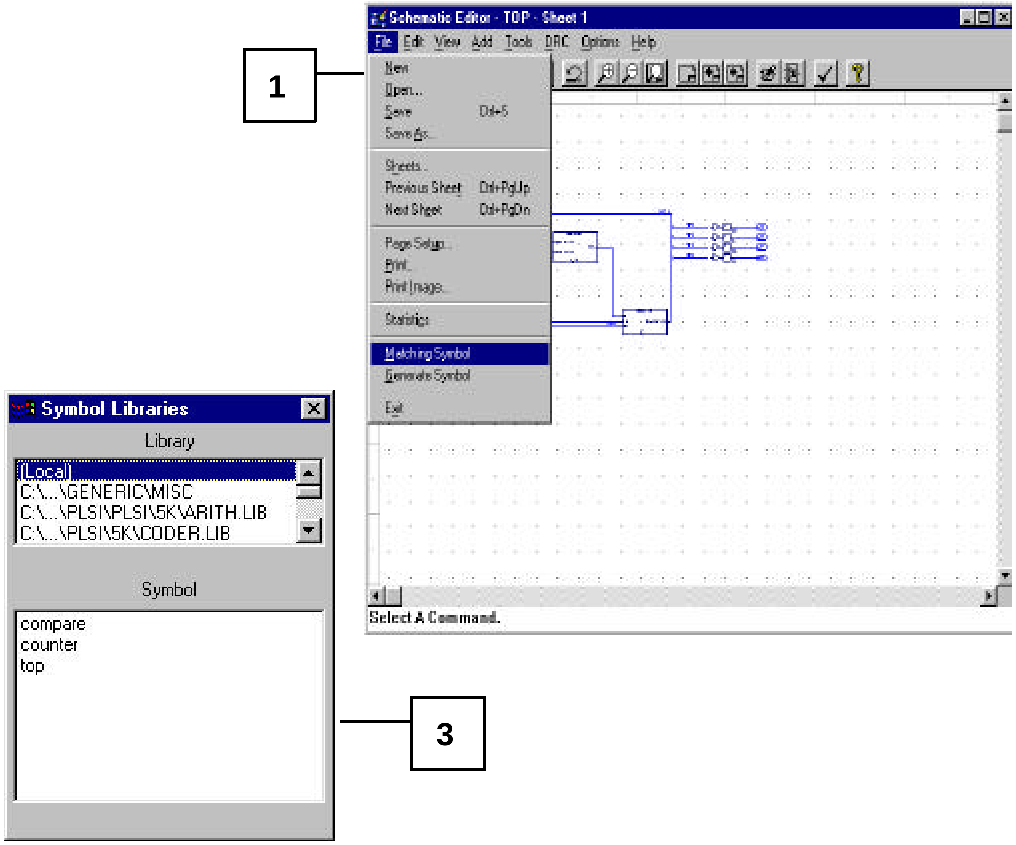
You can use the **Matching Symbol** command to create a symbol file (*.sym) for the schematic currently loaded, with the same base name. The input and output pins on the symbol have the same signal names and polarities as the I/O markers in the schematic.

The Schematic Editor creates the symbol in the same directory as the schematic. You can use the **Add Symbol** command to insert the symbol into any other schematic.

In this step, you will create a symbol for the *Top* schematic. The symbol will be saved in the Local symbol library in the project directory.

*To create a matching symbol for the* Top *schematic*:

1. Choose **File** ⇒ **Matching Symbol**. The Schematic Editor automatically creates a symbol.
2. Choose **Add** ⇒ **Symbol** to open the Symbol Libraries dialog.
3. Under Library, scroll to the top and select **(Local)**. Notice the symbol named **top**.



# Task 20 *Check the Schematic for Consistency Errors*

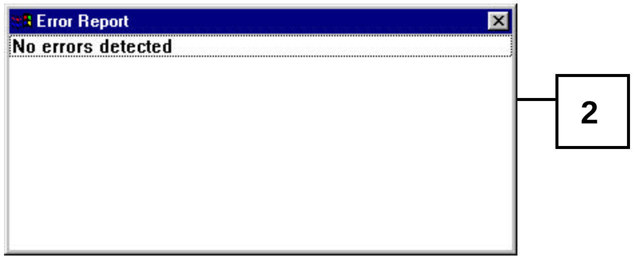
The Schematic Editor continually checks for errors, such as closed loops and shorted nets, while you're drawing your schematic. You can also check your schematic for other errors such as unconnected wires or pins or an unnamed signal tapped from a bus. Errors found are shown in a "hot" list box. Clicking an error causes the cursor to jump to the offending location.

*To check for consistency errors*:

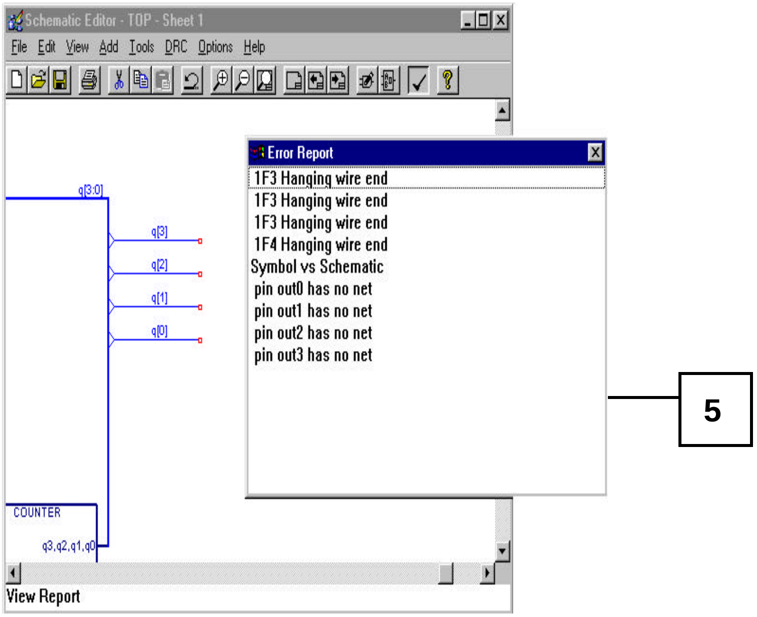
1. Choose **File** ⇒ **Save** to save the schematic.
2. Choose **DRC** ⇒ **Consistency Check** to open the Error Report.

   There should be no errors in the report.
3. Choose **Edit** ⇒ **Delete** and delete the circuitry on the right side of the schematic.
4. Choose **DRC** ⇒ **Consistency Check** again.
5. In the Error Report, select an error. Notice that the schematic view shifts to the location of the selected error.
6. Choose **File** ⇒ **Exit** to exit the schematic. When asked if you wish to save your changes, click **No**.

Congratulations! You have just created and checked a top-level schematic. Now let's create an ABEL-HDL source and add it to the project.



No errors detected



1F3 Hanging wire end
1F3 Hanging wire end
1F3 Hanging wire end
1F4 Hanging wire end
Symbol vs Schematic
pin out0 has no net
pin out1 has no net
pin out2 has no net
pin out3 has no net

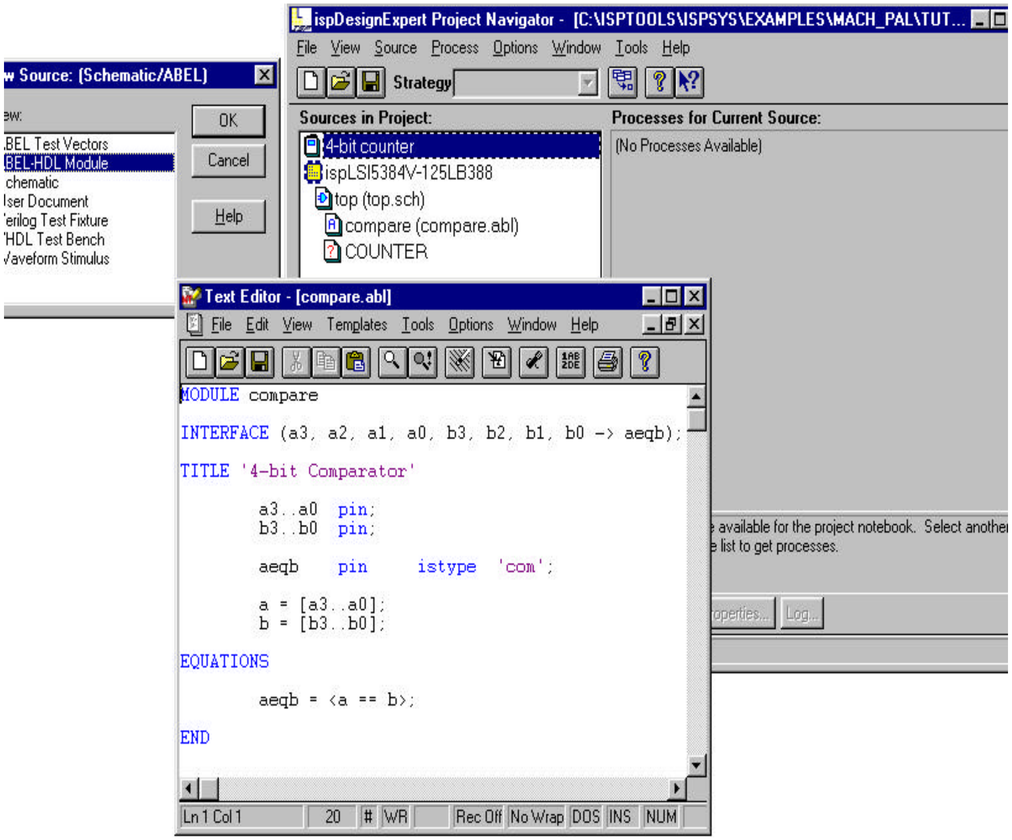
# Lesson 4 – Adding ABEL-HDL Sources to the Project

The Project Navigator now lists the schematic, *Top*, and the two block symbols referenced in the schematic, Counter and Compare. These sources have the undefined icon next to them because they do not exist yet. Remember that this is a top-down design example.

This lesson leads you through the steps necessary to add two lower-level ABEL-HDL modules to the project. One you will create from scratch. The other you will import.

Steps covered in this lesson are:

- **Task 21**: Create a New ABEL-HDL Source File Template
- **Task 22**: Enter the ABEL-HDL Source Description
- **Task 23**: Import an Existing ABEL-HDL Source File


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
4-bit counter
ispLSI5384V-125LB388
top (top.sch)
compare (compare.abl)
COUNTER
Processes for Current Source:
(No Processes Available)
available for the project notebook. Select another list to get processes.
operties... Log...
w Source: (Schematic/ABEL)
ew:
BEL Test Vectors
BEL-HDL Module
chematic
lser Document
'erilog Test Fixture
HDL Test Bench
Vaveform Stimulus
OK
Cancel
Help
Text Editor - [compare.abl]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
20
#
WR
Rec Off
No Wrap
DOS
INS
NUM

```
MODULE compare

INTERFACE (a3, a2, a1, a0, b3, b2, b1, b0 -> aeqb);

TITLE '4-bit Comparator'

        a3..a0  pin;
        b3..b0  pin;

        aeqb    pin     istype  'com';

        a = [a3..a0];
        b = [b3..b0];

EQUATIONS

        aeqb = (a == b);

END
```

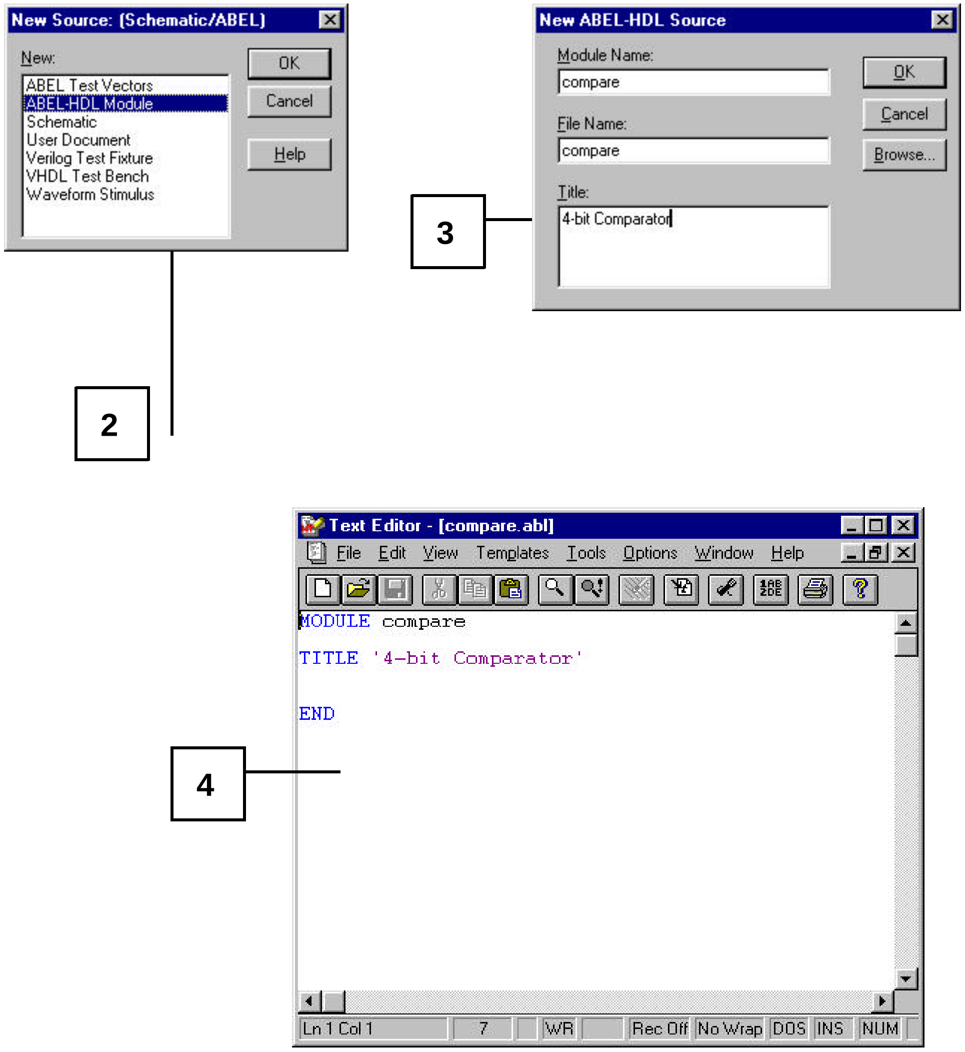
# Task 21 *Create a New ABEL-HDL Source File Template*

There are two steps to create a new ABEL-HDL source file. First you have to create the template. Then you enter the source description. In this step, you will create a template for the compare ABEL-HDL module.

*To create an ABEL-HDL template*:

1. In the Project Navigator Sources window, double-click **compare** to open the New Source dialog.
2. Select **ABEL-HDL Module** and then click **OK**.

   The Text Editor opens, as well as the **New ABEL-HDL Source** dialog, prompting you for additional information about the module.
3. In the dialog, type the information shown at the right. The text is case sensitive. Make sure to enter the text as shown to the right. Note that the Module Name matches the corresponding block symbol name. It is not necessary that the module name and file name be the same but it makes things simpler.
4. Click on **OK** to close the dialog. The ispDesignExpert Text Editor appears with an ABEL-HDL template.



Module Name: compare

File Name: compare

Title: 4-bit Comparator

```
MODULE compare

TITLE '4-bit Comparator'

END
```

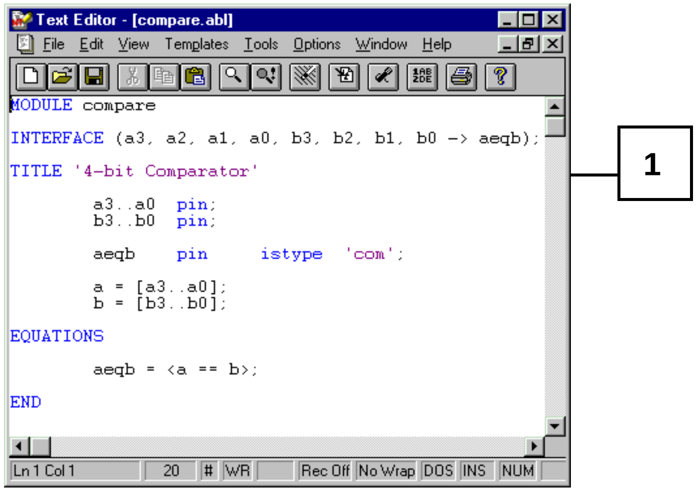
# Task 22 *Enter the ABEL-HDL Source Description*

In this step, you will complete the ABEL-HDL module by entering its description.

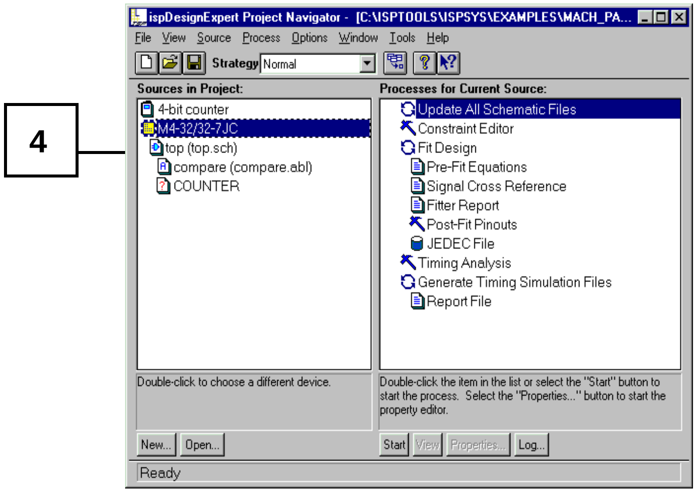
*To describe an ABEL-HDL module*:

1. In the Text Editor, type the text description as shown in the picture on the right.

   Notice that the ABEL-HDL pin declarations must match the name and the case of the I/O pins on the corresponding block symbol.
2. When you are through, choose **File** ⇒ **Save As** to save the file. Save the file with the same name.
3. Close the Text Editor.
4. In the Project Navigator Sources window, notice that the icon next to the compare has changed, and that the file name (compare.abl) appears next to the name. This indicates that this is now a *defined* module.


Text Editor - [compare.abl]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1 20 # WR Rec Off No Wrap DOS INS NUM
1

```
MODULE compare

INTERFACE (a3, a2, a1, a0, b3, b2, b1, b0 -> aeqb);

TITLE '4-bit Comparator'

        a3..a0  pin;
        b3..b0  pin;

        aeqb    pin     istype  'com';

        a = [a3..a0];
        b = [b3..b0];

EQUATIONS

        aeqb = (a == b);

END
```



Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

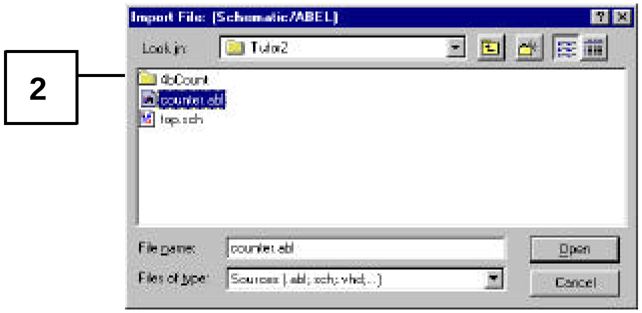
# Task 23 *Import an Existing ABEL-HDL Source File*

To save time in this tutorial, you will import the remaining ABEL-HDL source file. Although, in a practical sense, you will probably have existing ABEL-HDL files that you will want to import into a design in addition to creating new ones.

To import an existing ABEL-HDL source:

1. In the Project Navigator, choose **Source** ⇒ **Import** to open the Import File dialog.
2. Go to the `\ispTOOLS\ispsys\examples\MACH_pal\tutorial\Tutor2 directory` and select `counter.abl`.
3. Click **OK**. When prompted to replace the file, click **Yes**.
4. The Project Navigator should now look like the image shown to the right.

You'll take a look at the "insides" of this module in the following lesson.



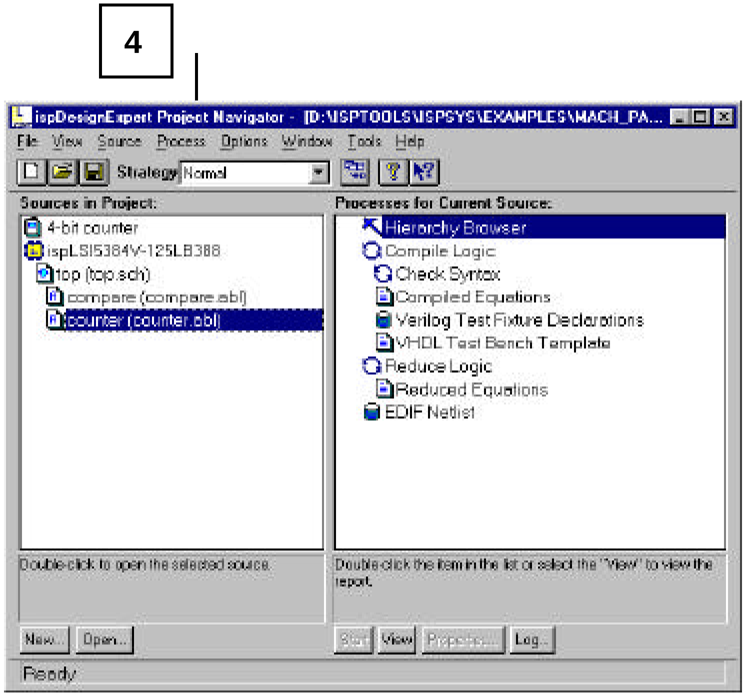
Import File: (Schematic/ABEL)

Look in: Tutor2

4bCount
counter.abl
top.sch

File name: counter.abl

Files of type: Sources (.abl; sch; vhd;...)



ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

Strategy: Normal

Sources in Project:

4-bit counter
ispLSI5384V-125LB388
top (top.sch)
compare (compare.abl)
counter (counter.abl)

Processes for Current Source:

Hierarchy Browser
Compile Logic
Check Syntax
Compiled Equations
Verilog Test Fixture Declarations
VHDL Test Bench Template
Reduce Logic
Reduced Equations
EDIF Netlist

Double-click to open the selected source.

Double-click the item in the list or select the 'View' to view the report.

Ready

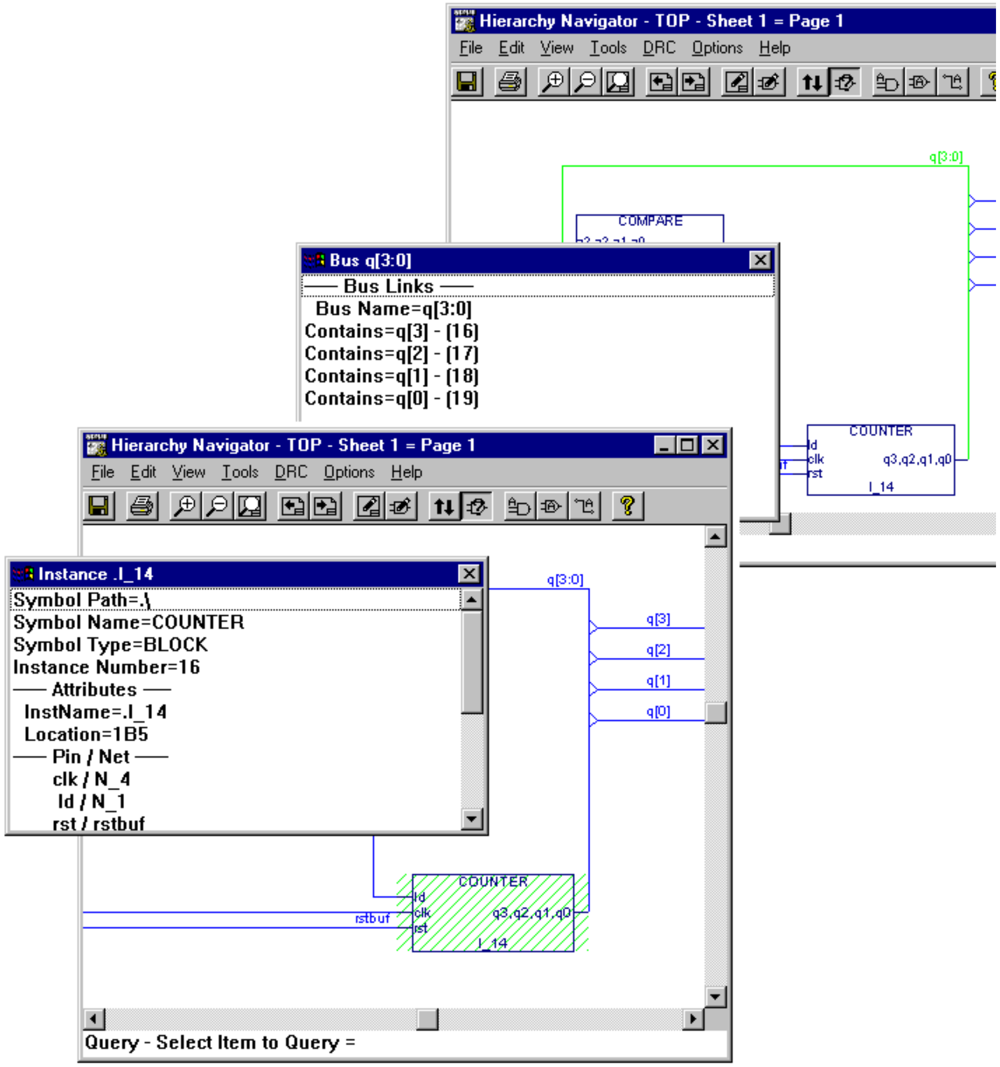
# Lesson 5 – Navigating the Design

The Hierarchy Navigator program allows you to navigate through a schematic design consisting of a top-level schematic and lower-level schematics and HDL modules. The Hierarchy Navigator loads a full hierarchical design all at once so that you can view it in its complete form, rather than as individual sources. Every schematic sheet and behavioral file at all levels of hierarchy is included.

Lesson 5 shows you how to use the Hierarchy Navigator to perform several useful functions.

Steps covered in this lesson are:

- **Task 24**: Open the Hierarchy Navigator
- **Task 25**: Push into the Counter Block Symbol
- **Task 26**: Access Connectivity Information for the Counter Block
- **Task 27**: Query a Net


Hierarchy Navigator - TOP - Sheet 1 = Page 1
File Edit View Tools DRC Options Help
q[3:0]
COMPARE
COUNTER
ld
clk
rst
q3,q2,q1,q0
I_14
q[3]
q[2]
q[1]
q[0]
rstbuf

Bus q[3:0]

—— Bus Links ——
Bus Name=q[3:0]
Contains=q[3] - [16]
Contains=q[2] - [17]
Contains=q[1] - [18]
Contains=q[0] - [19]

Instance .I_14

Symbol Path=.\
Symbol Name=COUNTER
Symbol Type=BLOCK
Instance Number=16
—— Attributes ——
InstName=.I_14
Location=1B5
—— Pin / Net ——
clk / N_4
ld / N_1
rst / rstbuf

Query - Select Item to Query =

# Task 24 *Open the Hierarchy Browser*

The Hierarchy Navigator performs several important functions.

- It verifies the correctness and consistency of a design's wiring. Verification occurs at each level in the design, and across all the levels, from top to bottom.
- It provides the environment in which you can analyze and optimize the circuit's performance.
- It prepares the design data for later steps in the design process, for example creating netlists.

You open the Hierarchy Navigator from the Project Navigator.

*To open the Hierarchy Browser*:

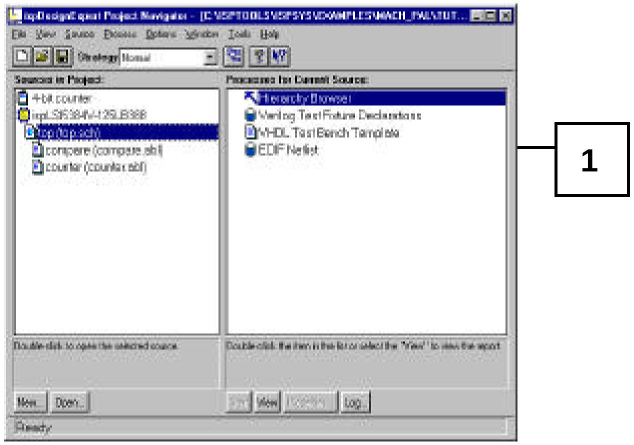
1. In the Sources window, select the **top** schematic source (`top.sch`).

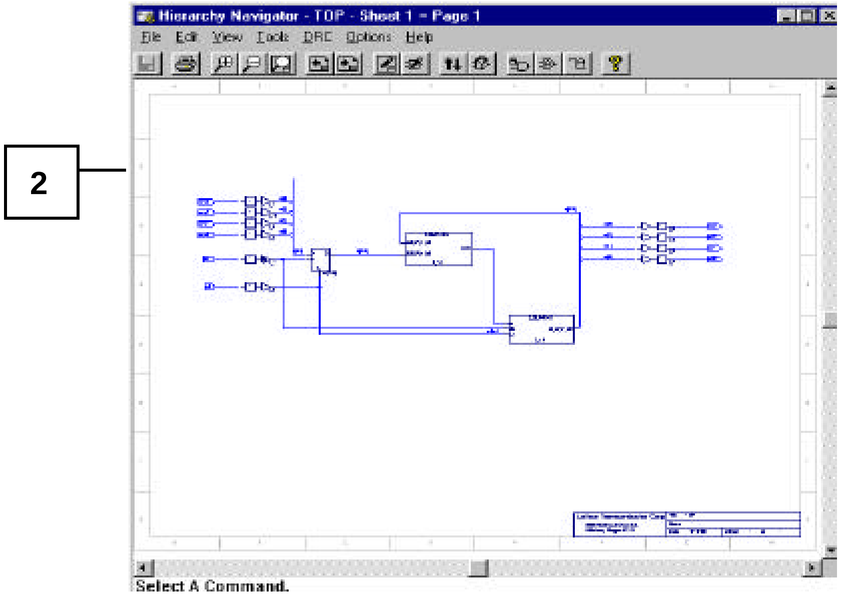
   Notice the Hierarchy Navigator icon at the top of the Processes window is automatically selected. Also notice that the Hierarchy Navigator icon is visible *only* when a schematic source is selected.

2. Double-click the Hierarchy Navigator icon in the Processes window.

   The Hierarchy Navigator opens with sheet 1 of the selected schematic source loaded.

***Note**: Remember, this is not the Schematic Editor. You cannot edit the schematic or one of its symbols in the Hierarchy* Navigator*. However, you can open editors from the Hierarchy* Navigator *to make changes in a specific schematic element.*


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
4-bit counter
ispLSI5384V-125LB388
top (top.sch)
compare (compare.abl)
counter (counter.abl)
Processes for Current Source:
Hierarchy Browser
Verilog Test Fixture Declarations
VHDL TestBench Template
EDIF Netlist
Double-click to open the selected source.
Double-click the item in the list or select the "View" to view the report
New... Open...
View Log...
Ready
1


2
Hierarchy Navigator - TOP - Sheet 1 - Page 1
File Edit View Tools DRC Options Help
Select A Command.

# Task 25 *Push into the Counter Block Symbol*

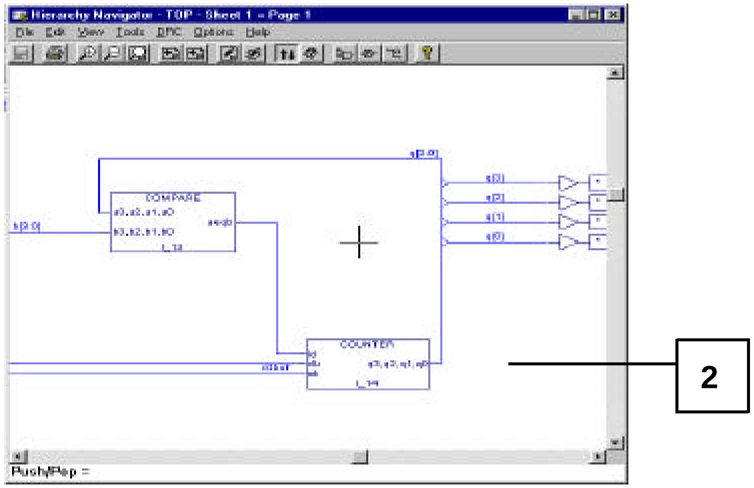
You can use the **Push/Pop** command on the View menu to move down and up (respectively) through the various hierarchical levels of a design. This command works on both schematics and ABEL-HDL modules.

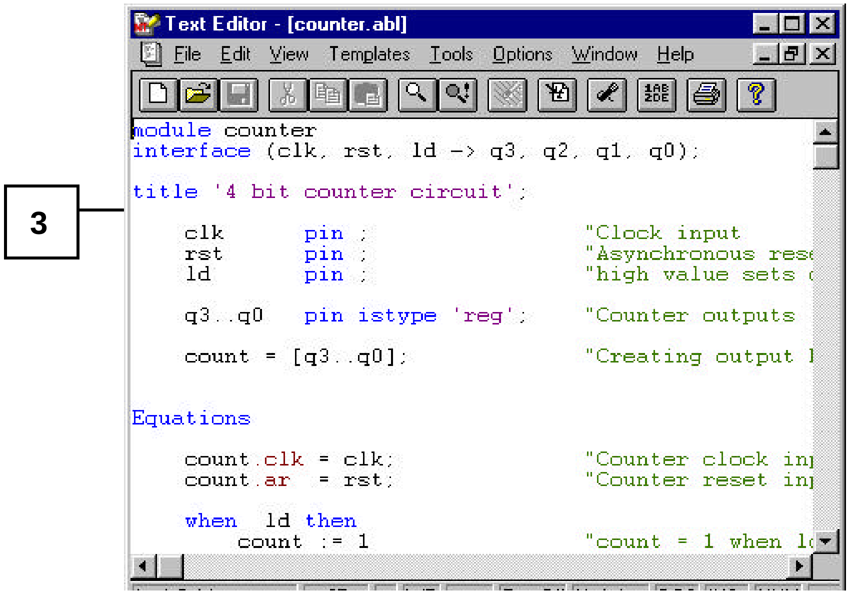
You may want to use the **Zoom In** command to view the **counter** module before starting this step.

To push into the Counter block symbol:

1. Choose **View** ⇒ **Push/Pop**. The cursor changes to a cross hair.
2. To move down a level, into the counter module, click *inside* the **counter** schematic symbol.

   The Text Editor opens with the ABEL-HDL description of the module.
3. View the contents of the **counter** module. When you are finished, close the **Text Editor**.


Hierarchy Navigator - TOP - Sheet 1 - Page 1
File Edit View Tools DRC Options Help
COMPARE
COUNTER
Push/Pop =
2


Text Editor - [counter.abl]
File Edit View Templates Tools Options Window Help
3

```
module counter
interface (clk, rst, ld -> q3, q2, q1, q0);

title '4 bit counter circuit';

    clk       pin ;                    "Clock input
    rst       pin ;                    "Asynchronous rese
    ld        pin ;                    "high value sets c

    q3..q0    pin istype 'reg';        "Counter outputs

    count = [q3..q0];                  "Creating output l


Equations

    count.clk = clk;                   "Counter clock in
    count.ar  = rst;                   "Counter reset in

    when  ld then
        count := 1                     "count = 1 when lc
```

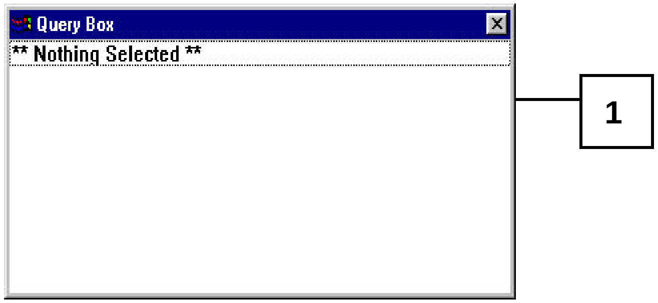
# Task 26 *Access Connectivity Information for the Counter Block*

You can use the **Query** command to display additional information about circuit elements. The information appears in a text box that pops up when the first element is selected, and is updated when another element is selected.

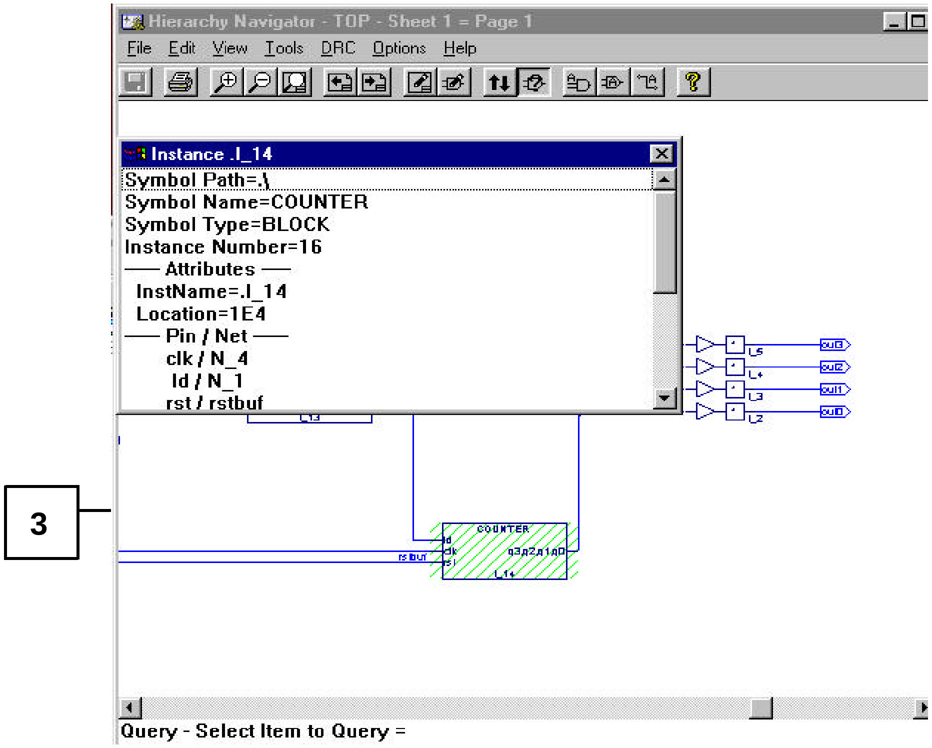
In this step, you will use the **Query** command to query the Counter ABEL-HDL module for information.

*To query the Counter block symbol*:

1. Choose **DRC** ⇒ **Query**. The Query text box opens with the message: Nothing Selected.
2. Move the text box so that you can see the counter block.
3. Click the **counter** block. The Query text box updates to show various information about the counter block.
4. Look at the **Pin/Net** section. The Hierarchy Browser knows which nets are connected to which pins, and displays instance names, reference designators, or symbol names that have been assigned to that symbol.



** Nothing Selected **


Hierarchy Navigator - TOP - Sheet 1 = Page 1
File Edit View Tools DRC Options Help
Instance .I_14
COUNTER
3

```
Symbol Path=.\
Symbol Name=COUNTER
Symbol Type=BLOCK
Instance Number=16
—— Attributes ——
 InstName=.I_14
 Location=1E4
—— Pin / Net ——
    clk / N_4
     ld / N_1
    rst / rstbuf
```

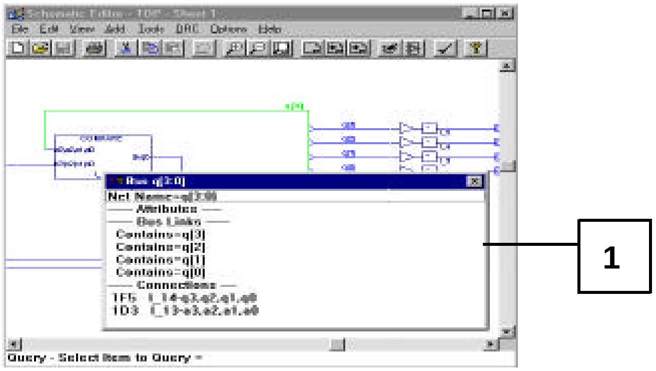
Query - Select Item to Query =

# Task 27 *Query a Net*

Although design problems are usually observed at the top level, the source of those problems is often at a lower level. Tracing signals from the primary outputs down through the hierarchy can greatly aid debugging. For instance, to determine if a net needs more buffers, the **Query** command lets you quickly determine what components are attached to the net and what will be affected by changes to the net.

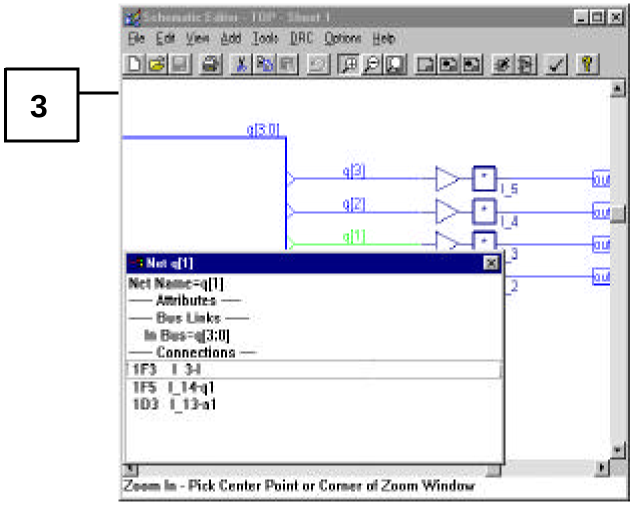
*To query a net*:

1. With the **Query** command still active, click the bus labeled **q[3:0]** in the schematic. A list of its content signals appears in the Query text box.
2. Observe that the signals displayed in the hot report window are links (pointers) to the individual nets.
3. In the Query Text box, click **q[1]**. The report updates showing new information for the net. (You will not see information about the Bus and Net at the same time. When one window opens, the other window closes.)
4. In the Query Text box, click one of the connections to a net. The cursor automatically moves to the component where the connecting pin is located. The cursor automatically moves to any page in the hierarchy, no matter which level, if necessary to display the selected pin.
5. Close the Query Text box and the Hierarchy Navigator. If prompted, **Data has been modified, yes/no?** click **no**. Close the Hierarchy Navigator.


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
q[0]
Bus q[3:0]
1

Net Name=q[3:0]
— Attributes —
— Bus Links —
Contains=q[3]
Contains=q[2]
Contains=q[1]
Contains=q[0]
— Connections —
1F5 I_14-q3,q2,q1,q0
1D3 I_13-a3,a2,a1,a0

Query - Select Item to Query -


Schematic Editor - TOP - Sheet 1
File Edit View Add Tools DRC Options Help
q[3:0]
q[3]
q[2]
q[1]
I_5
I_4
I_3
I_2
Net q[1]
3

Net Name=q[1]
— Attributes —
— Bus Links —
In Bus=q[3:0]
— Connections —
1F3 I_3-I
1F5 I_14-q1
1D3 I_13-a1

Zoom In - Pick Center Point or Corner of Zoom Window

# Congratulations

You have finished…

- add various schematic elements to create a top-level schematic source.
- check the schematic for errors.
- use the Text Editor to create a new ABEL-HDL source.
- import an ABEL-HDL source into the project.
- use the Hierarchy Navigator to navigate through the design and try “debug” methods.

Now you are ready to implement the design. You can continue working with this design in Tutorial 4, *Implementing a Design.*

# *Tutorial 4 HDL Design Entry with Synplicity Synplify*

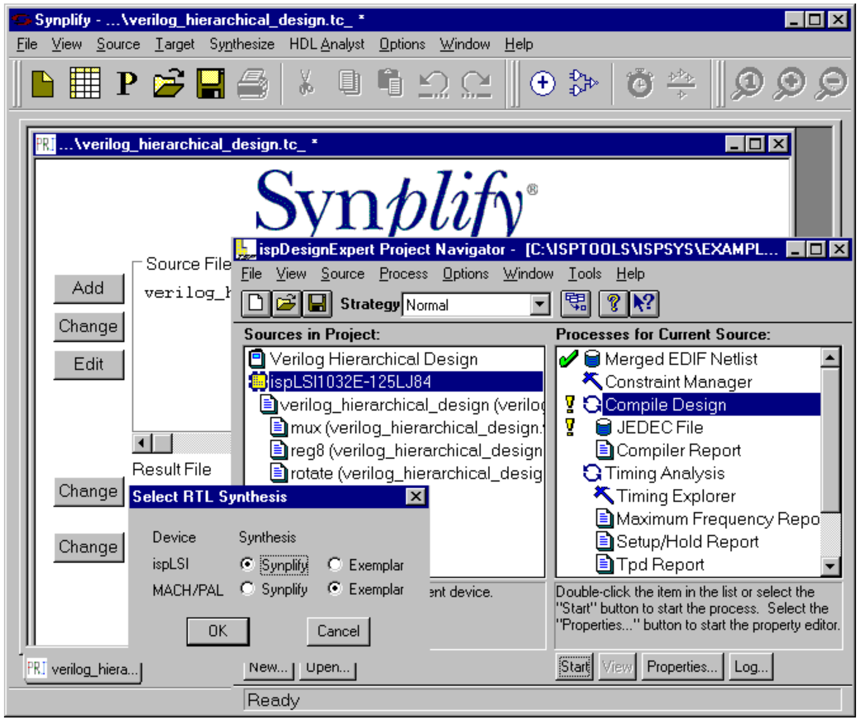
This tutorial shows you how to use Synplify to synthesize a Verilog HDL design for a Lattice CPLD device. In this tutorial, you will implement the design in an ispLSI device.

## Learning Objectives

When you are finished with this tutorial, you should understand the steps necessary to generate an EDIF file from Synplify for a Lattice CPLD device. You will also learn how to target a device, fit the design, and generate a JEDEC file.

## Time to Complete This Tutorial

The time to complete this tutorial is about 20 minutes.


Synplify - ...\verilog_hierarchical_design.tc_ *
File View Source Target Synthesize HDL Analyst Options Window Help
...\verilog_hierarchical_design.tc_ *
Synplify
Add
Change
Edit
Source File
verilog_h
Result File
Change
Change
verilog_hiera...
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
New... Open...
Start View Properties... Log...

Strategy: Normal

Sources in Project:
- Verilog Hierarchical Design
- ispLSI1032E-125LJ84
- verilog_hierarchical_design (verilog
- mux (verilog_hierarchical_design.
- reg8 (verilog_hierarchical_design
- rotate (verilog_hierarchical_desig

Processes for Current Source:
- ✓ Merged EDIF Netlist
- Constraint Manager
- Compile Design
- JEDEC File
- Compiler Report
- Timing Analysis
- Timing Explorer
- Maximum Frequency Repo
- Setup/Hold Report
- Tpd Report

ent device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

**Select RTL Synthesis**

| Device | Synthesis | |
|---|---|---|
| ispLSI | ● Synplify | ○ Exemplar |
| MACH/PAL | ○ Synplify | ● Exemplar |

OK Cancel

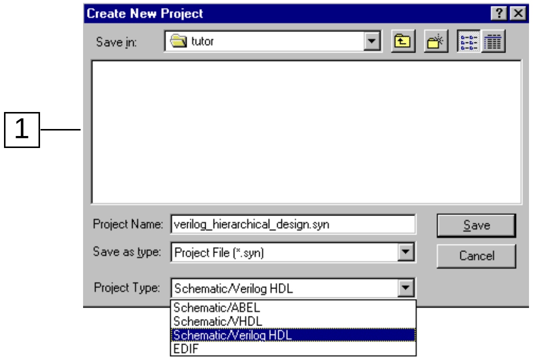
# Task 1 *Create a New Project in ispDesignExpert*

After starting the Project Navigator, you are ready to create a new project, whose type is Verilog HDL. The design flow for Verilog HDL is similar to VHDL designs, so you can follow this tutorial to process a VHDL design by substituting VHDL for Verilog HDL. Create a directory to save your tutorial designs.

*To create a new project*:

1. In the Project Navigator, choose **File** ⇒ **New Project** to open the Create New Project dialog.
2. Navigate to the `ispTools\ispsys\examples\ispLSI_GAL \verilog` directory.
3. Create a new folder called `tutor`.
4. Go into the new folder and type the name `verilog_hierarchical_design.syn` for the Project Name, choose Schematic/Verilog HDL in the Project Type list box, and then click **Save** to close the dialog.

   The untitled project with ispLSI default device (ispLSI5384V-125LB388) appears in the Sources window.
5. In the Sources window, double-click the project book icon to open the Project Properties dialog. Type `Verilog Hierarchical Design` for the project title. Click **OK** to save the change.
6. Double-click the device icon to open the Device Selector dialog and change the device to `ispLSI1032E-125LJ84`.
7. Click **Yes** to confirm that you wish to change the device kits. The ispDesignExpert design environment reconfigures to facilitate with the selected device.



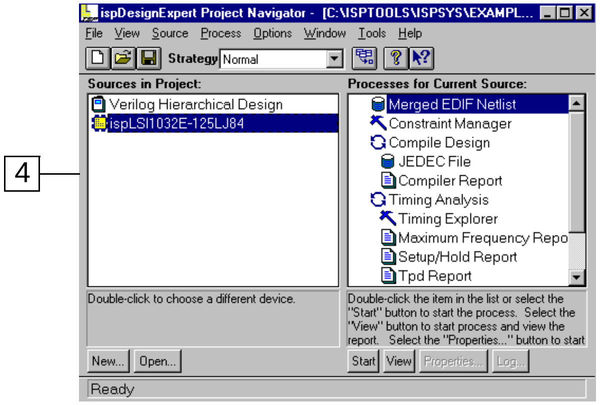
Save in: tutor

Project Name: verilog_hierarchical_design.syn

Save as type: Project File (*.syn)

Project Type: Schematic/Verilog HDL

Schematic/ABEL
Schematic/VHDL
Schematic/Verilog HDL
EDIF


4
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy
New...
Open...
Start
View
Properties...
Log...

Strategy: Normal

Sources in Project:

Verilog Hierarchical Design
ispLSI1032E-125LJ84

Processes for Current Source:

Merged EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Timing Explorer
Maximum Frequency Repo
Setup/Hold Report
Tpd Report

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "View" button to start process and view the report. Select the "Properties..." button to start

Ready

# Task 2 *Create or Import Design Sources*

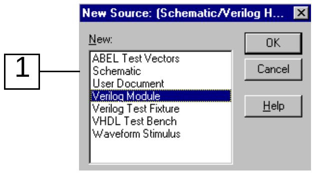
You need to add sources to complete your Verilog HDL design. You can either create or import a Verilog HDL module.

*To create a Verilog HDL module:*

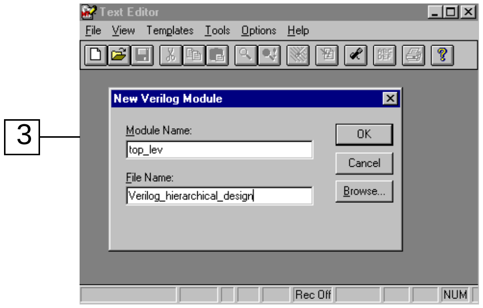
1. In the Project Navigator, select **Source** ⇒ **New** to open the New Source dialog.
2. Highlight Verilog Module in the New field, click **OK** to close the dialog. Then the Text Editor window appears, along with the New Verilog Module dialog.
3. Type `top_lev` in the Module Name field and `verilog_hierarchical_design` in the File Name field.
4. Click **OK**. The `verilog_hierarchical_design.v` file appears on the Text Editor title bar. The Verilog module template is displayed in the Editor window.
5. Type the design syntax in the Verilog module template.
6. Select **File** ⇒ **Save** from the Editor to save the `.v` file.

   Notice the Verilog modules defined in the `.v` file are displayed in the Sources window.

***Tip**: You can use **Source** ⇒ **Import** from the Project Navigator to include the design sources directly.*

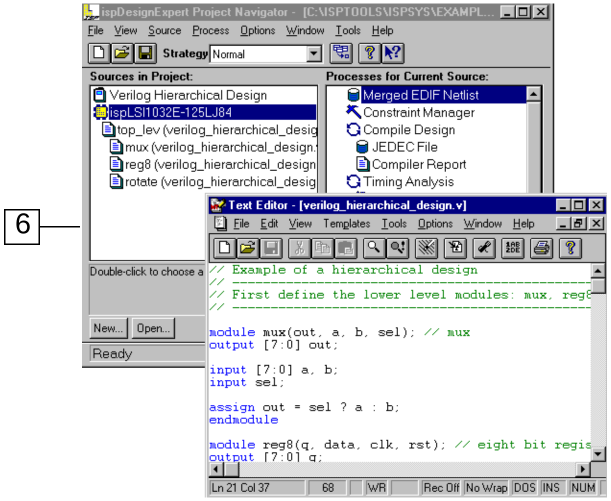


New:
ABEL Test Vectors
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Test Bench
Waveform Stimulus



Module Name: top_lev

File Name: Verilog_hierarchical_design


6
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy
Normal
Sources in Project:
Processes for Current Source:
Merged EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Double-click to choose a
New...
Open...
Ready
Text Editor - [verilog_hierarchical_design.v]
File Edit View Templates Tools Options Window Help
Ln 21 Col 37
68
WR
Rec Off
No Wrap
DOS
INS
NUM

Verilog Hierarchical Design
ispLSI1032E-125LJ84
top_lev (verilog_hierarchical_desig
mux (verilog_hierarchical_design.
reg8 (verilog_hierarchical_design
rotate (verilog_hierarchical_desig

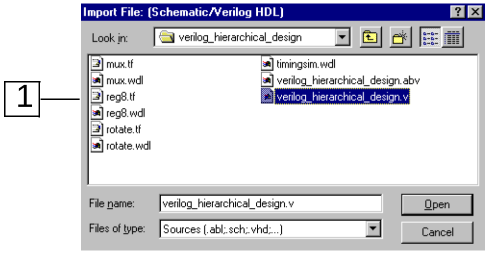
```
// Example of a hierarchical design
// -------------------------------------------------------
// First define the lower level modules: mux, reg8
// -------------------------------------------------------

module mux(out, a, b, sel); // mux
output [7:0] out;

input [7:0] a, b;
input sel;

assign out = sel ? a : b;
endmodule

module reg8(q, data, clk, rst); // eight bit regis
output [7:0] q;
```

# Create or Import Design Sources (continued)

*To import a Verilog HDL module:*

1. In the Project Navigator, select **Source** ⇒ **Import** to open the Import File dialog box.
2. Navigate to the `ispTools\ispsys\examples\verilog\verilog_hierarchical_design` directory and choose Sources (`.abl`;`.sch`;`.vhd`;...) in the Files of type field.
3. Select `verilog_hierarchical_design.v` file in the file list area, then click **Open**.

   The top-level Verilog module along with three submodules are imported into the Sources window as shown on the right.



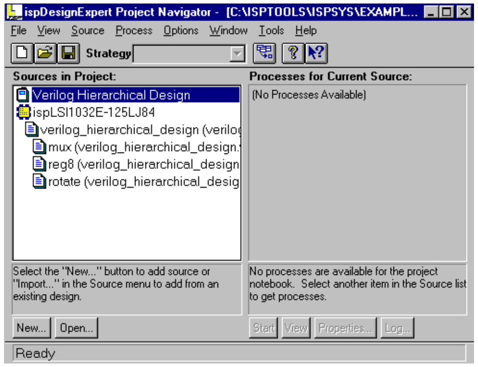
Import File: (Schematic/Verilog HDL)

Look in: verilog_hierarchical_design

mux.tf
mux.wdl
reg8.tf
reg8.wdl
rotate.tf
rotate.wdl
timingsim.wdl
verilog_hierarchical_design.abv
verilog_hierarchical_design.v

File name: verilog_hierarchical_design.v

Files of type: Sources (.abl;.sch;.vhd;...)



ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...

Sources in Project:

Verilog Hierarchical Design
ispLSI1032E-125LJ84
verilog_hierarchical_design (verilog
mux (verilog_hierarchical_design.
reg8 (verilog_hierarchical_design
rotate (verilog_hierarchical_desig

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

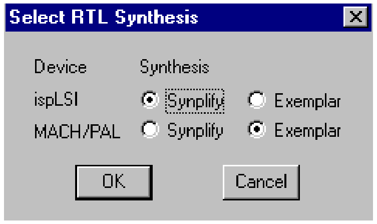
Ready

# Task 3 *Select RTL Synthesis Tool*

The ispDesignExpert provides two synthesis tools: Exemplar (default for MACH devices) and Synplify (default for ispLSI devices), for your HDL designs. You can use RTL synthesis tool to select one of them to run synthesis.

*To select an RTL synthesis tool:*

1. Select **Options** ⇒ **Select RTL Synthesis** from the Project Navigator. The Select RTL Synthesis dialog is displayed.
2. Make sure Synplify is checked for ispLSI device (you've selected an ispLSI device in a previous step), click **OK** to accept the selected synthesis tool.



Select RTL Synthesis

| Device | Synthesis | |
|---|---|---|
| ispLSI | ● Synplify | ○ Exemplar |
| MACH/PAL | ○ Synplify | ● Exemplar |

# Task 4 *Fit the Design*

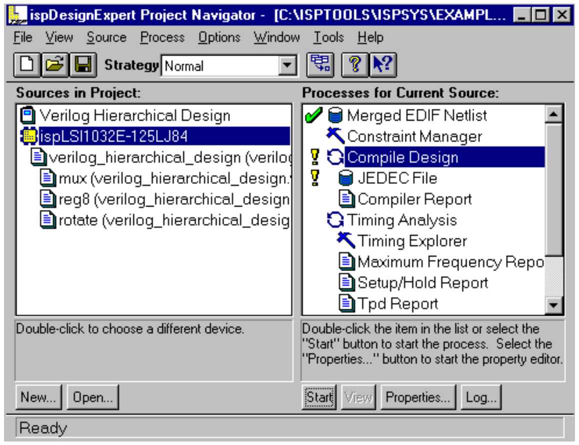
Now you can fit the design into the target device. Synplify runs automatically to synthesize the Verilog HDL source and generates an EDIF file. The ispEXPERT Compiler merges the EDIF netlist and generates a JEDEC file.

*To fit the design with the target device*:

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Compile Design**, or select the process and click **Start** to start the compilation.

   This opens the ispEXPERT Compiler Graphic User Interface and the design is automatically being compiled in the Compiler window.

   After compilation, check marks are added to the left of the associated processes.



Sources in Project:

- Verilog Hierarchical Design
- ispLSI1032E-125LJ84
- verilog_hierarchical_design (verilog
- mux (verilog_hierarchical_design.
- reg8 (verilog_hierarchical_design
- rotate (verilog_hierarchical_desig

Processes for Current Source:

- ✓ Merged EDIF Netlist
- Constraint Manager
- Compile Design
- JEDEC File
- Compiler Report
- Timing Analysis
- Timing Explorer
- Maximum Frequency Repo
- Setup/Hold Report
- Tpd Report

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

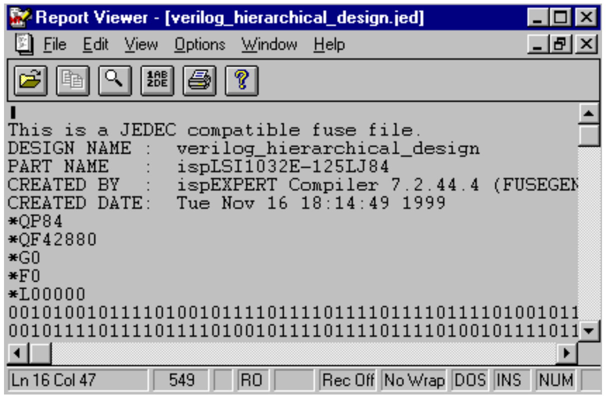
# Task 5 *View JEDEC File*

After compiling the design, a JEDEC file is generated.

*To view the JEDEC file:*

1. In the Sources window, select the target device.
2. In the Processes window, select JEDEC File and click the **View** button to open the file.

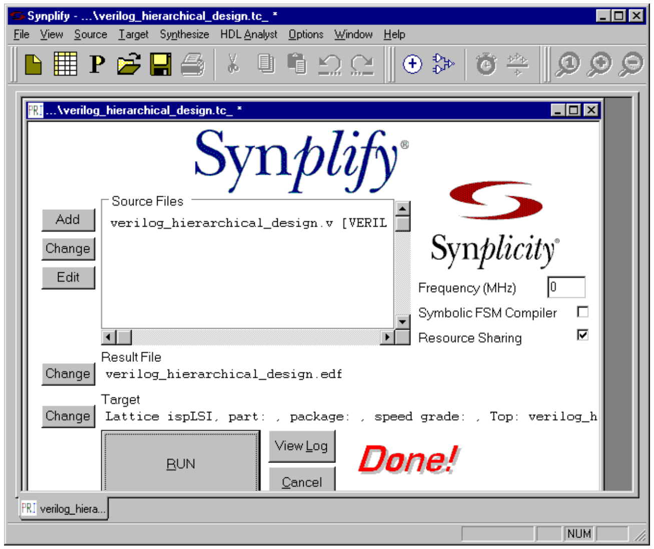
   The JEDEC file is displayed in the Report Viewer window. Scroll down in the Viewer window to view the file in detail.


Report Viewer - [verilog_hierarchical_design.jed]
File Edit View Options Window Help
Ln 16 Col 47
549
RO
Rec Off
No Wrap
DOS
INS
NUM

```
This is a JEDEC compatible fuse file.
DESIGN NAME :  verilog_hierarchical_design
PART NAME   :  ispLSI1032E-125LJ84
CREATED BY  :  ispEXPERT Compiler 7.2.44.4 (FUSEGEN
CREATED DATE:  Tue Nov 16 18:14:49 1999
*QP84
*QF42880
*G0
*F0
*L00000
001010010111101001011110111101111011110111101001011
001011110111101111010010111101111011110100101111011
```

# Task 6 *Run the Stand-alone Synplify*

Synplify can be invoked in its stand-alone mode by selecting **Tools ⇒ Synplicity Synplify Synthesis** from the Project Navigator. The stand-alone Synplify lets you generate an EDIF file and then import the EDIF file into your project as a design source. Then, you can fit the design without running Synplify again.



Source Files
verilog_hierarchical_design.v [VERIL

Frequency (MHz) 0
Symbolic FSM Compiler □
Resource Sharing ☑

Result File
verilog_hierarchical_design.edf

Target
Lattice ispLSI, part: , package: , speed grade: , Top: verilog_h

*To start Synplify in stand-alone mode:*

1. From the Project Navigator, choose **Tools ⇒ Synplicity Synplify Synthesis** to open the Synplify synthesis tool.
2. In the Unsaved Project window, click **Add** to open the Add Source Files dialog.
3. Select a `.v` file, then click **Add** to add the target file to the Source Files field.

   You can change or edit the selected source file using the **Change** or **Edit** button beside the Source Files field.
4. Click the large **Run** button to start compiling and mapping the source file.

   After successful synthesis, Synplify displays “Done!”. A `.edf` file with the same base name appears as Result File. Double-click the file name to view the Synplify output file. You can also click **View Log** to view Synplify log file.

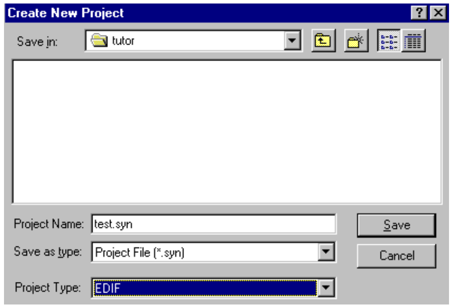
# Run the Stand-alone Synplify (continued)

*To import the EDIF file into your project:*

1. In the Project Navigator, select **File** ⇒ **New Project** to open the Create New Project dialog. Choose EDIF in the Project Type field to create an EDIF project.
2. In the Project Navigator, select **Source** ⇒ **Import** to open the Import File dialog.
3. Select the generated `.edf` file and click **Open**. The EDIF Reader Settings dialog appears.
4. Choose Synplicity for the Vendor. Check the desired radio buttons in the VCC GND Representation field and Bus Reconstruction field, then click **OK** to close the dialog.
5. The software adds the selected EDIF file to the Sources window as a design source.

*To fit the design with the target device:*

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Compile Design**, or select the process and click **Start** to run compilation.
3. Click **Log** to open the Report Viewer and view the process status report.

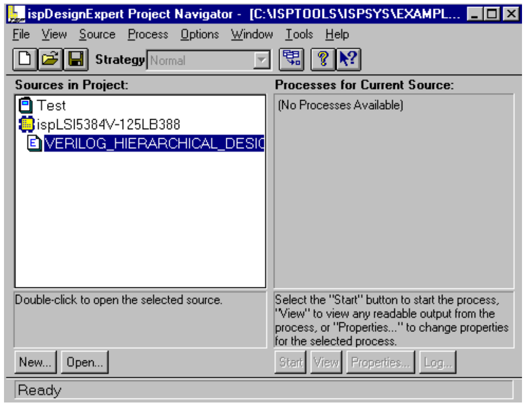


Save in: tutor

Project Name: test.syn

Save as type: Project File (*.syn)

Project Type: EDIF



Strategy: Normal

Test

ispLSI5384V-125LB388

VERILOG_HIERARCHICAL_DESIG

(No Processes Available)

Double-click to open the selected source.

Select the "Start" button to start the process, "View" to view any readable output from the process, or "Properties..." to change properties for the selected process.

Ready

# Congratulations!

You have completed the HDL Design Entry with Synplicity Synplify tutorial. In this tutorial you have learned how to:

- create a new project in ispDesignExpert.
- create or import a Verilog HDL source in the Sources window.
- select an RTL synthesis tool.
- fit the design.
- view the JEDEC file.
- run the stand-alone Synplify to generate a .edf file, import it as the design source and fit the design.

# Tutorial 5 HDL Design Entry with LeonardoSpectrum

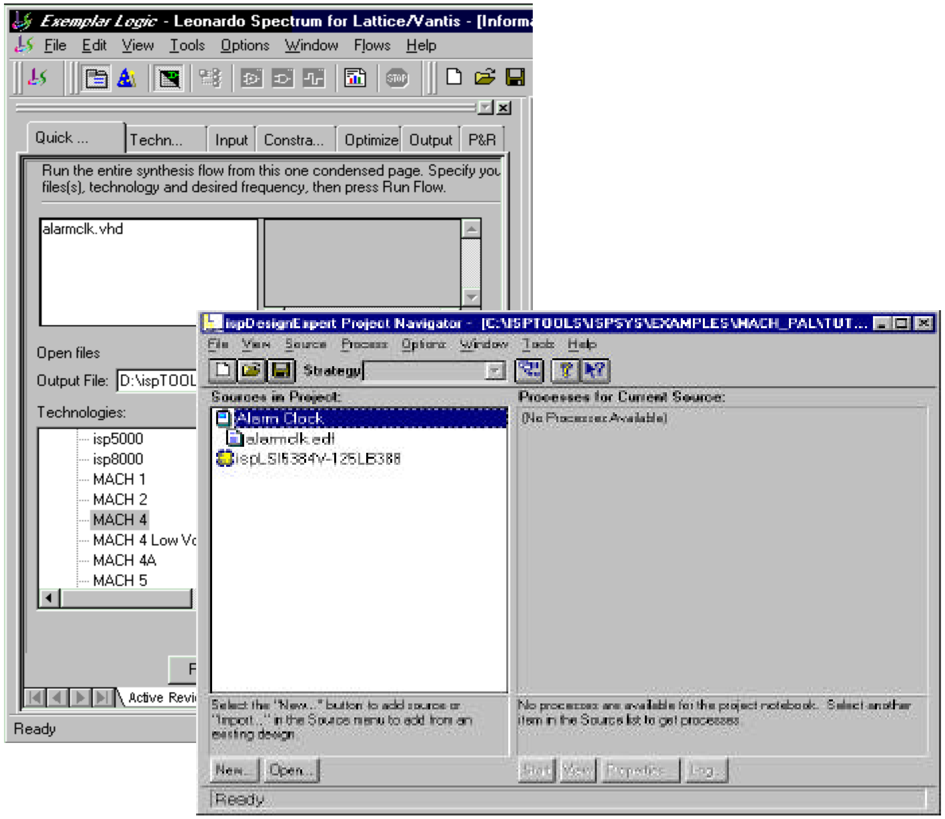
This tutorial shows you how to use LeonardoSpectrum to synthesize a VHDL design and generate an EDIF file for a Lattice CPLD device. For this tutorial, you implement it in a MACH4 device.

## Learning Objectives

When you are finished with this tutorial, you should understand the steps and tools necessary to generate an EDIF file from the LeonardoSpectrum synthesis tool and import it into ispDesignExpert. You will also learn how to target a Lattice CPLD device, fit the design, and generate a JEDEC file.

## Time to Complete This Tutorial

The time to complete this tutorial is about 20 minutes.



Run the entire synthesis flow from this one condensed page. Specify you files(s), technology and desired frequency, then press Run Flow.

Output File: D:\ispTOOL

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

# Task 1 *Create a new project in ispDesignExpert*

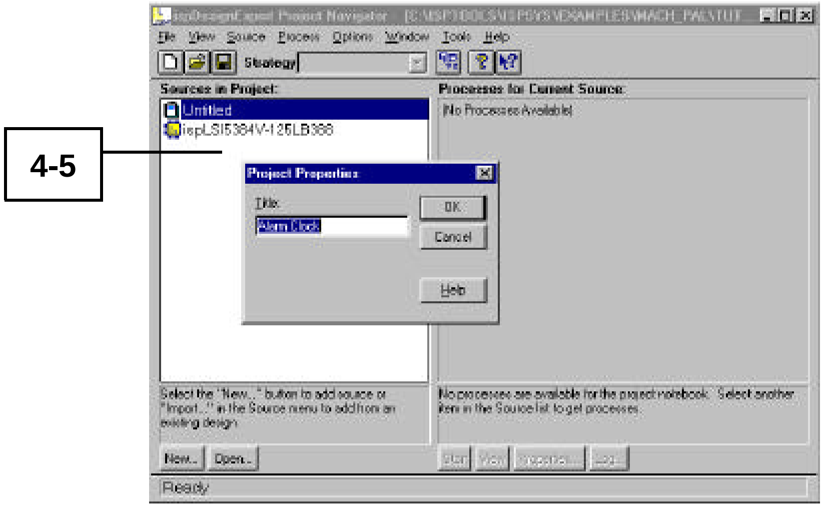
After starting the Project Navigator, you are ready to create a new project.

*To create a project*:

1. Choose **File** ⇒ **New Project** to open the Create New Project dialog.
2. In the dialog, change directories to `ispTOOLS\ispsys\examples\Mach_pal\tutorial\Tutor3`.
3. Name the file `alarmclk.syn` file and then click **Save**. The untitled generic project appears in the Sources window of the Project Navigator
4. In the Project Type, select **EDIF**.

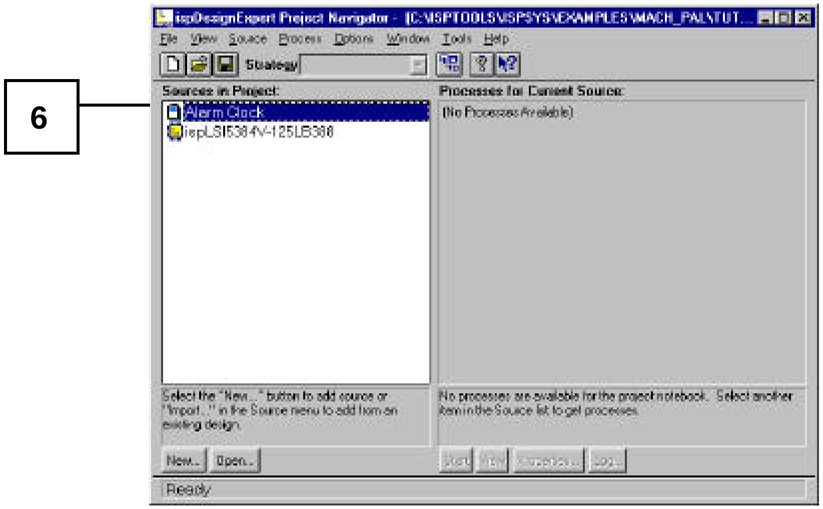
***Important:*** *Select the proper project type. You will not be able to change this later in your project.*

5. In the Sources window, double-click the title of the project (**Untitled**) to open the Project Properties dialog.
6. Type the name **`Alarm Clock`** for the title of your project.
7. Click **OK**. The new project title appears in the Sources window.


4-5
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
Untitled
ispLSI5384V-125LB388
Processes for Current Source:
(No Processes Available)
Project Properties
Title:
Alarm Clock
OK
Cancel
Help
New... Open...
Start View Properties... Log...
Ready

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.


6
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\TUT...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
Alarm Clock
ispLSI5384V-125LB388
Processes for Current Source:
(No Processes Available)
New... Open...
Start View Properties... Log...
Ready

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

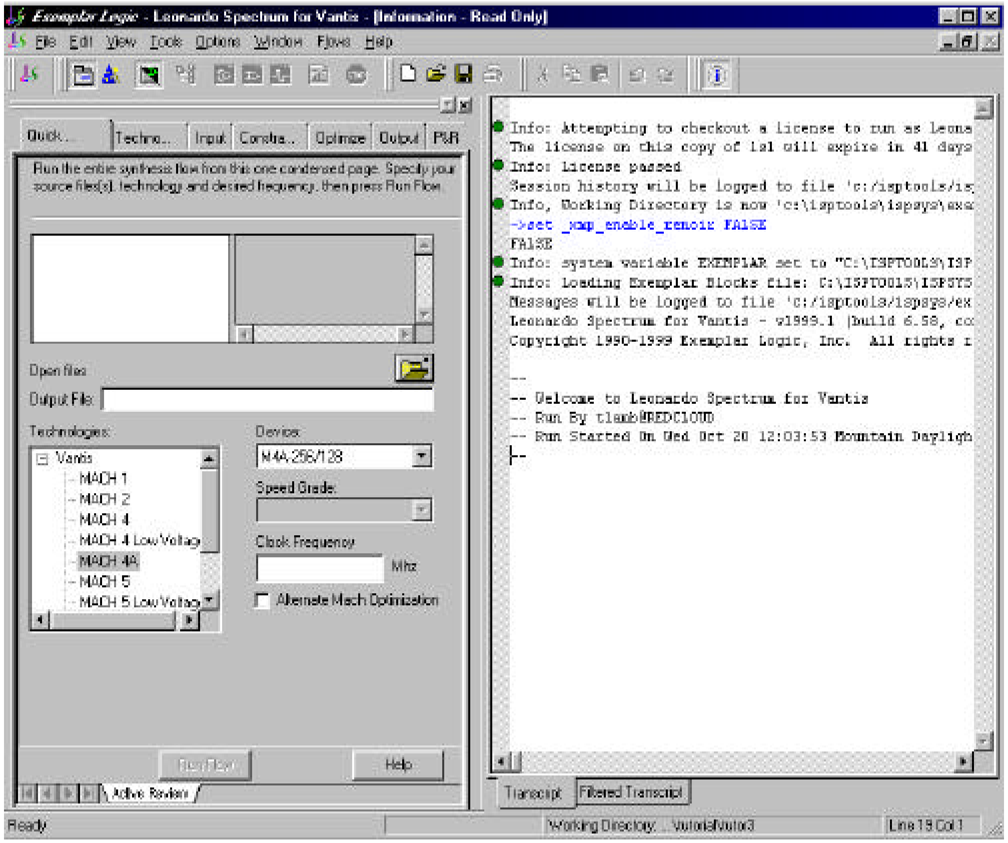
No processes are available for the project notebook. Select another item in the Source list to get processes.

# Task 2 *Start LeonardoSpectrum from ispDesignExpert*

When you start LeonardoSpectrum for the first time, the main window is maximized and displays the Tip of the Day, FlowTabs, and an information window.

*To start LeonardoSpectrum*:

1. On the ispDesignExpert menu, choose **Tools ⇒ LeonardoSpectrum Synthesis** to open the LeonardoSpectrum synthesis tool.
2. There are three ways to synthesize your design: Synthesis Wizard, Quick Setup, and FlowTabs. For this tutorial you will use the Quick Setup method.
   a. Click **OK** to close the Tip of the Day.
   b. Click **Cancel** to close the Device Settings dialog.
3. Make sure the **Quick Setup** tab is selected. Your screen should look similar to the one on the right.



Exemplar Logic - Leonardo Spectrum for Vantis - [Information - Read Only]

Run the entire synthesis flow from this one condensed page. Specify your source file(s), technology and desired frequency, then press Run Flow.

Technologies: Vantis — MACH 1, MACH 2, MACH 4, MACH 4 Low Voltag, MACH 4A, MACH 5, MACH 5 Low Voltag

Device: M4A-256/128

Speed Grade:

Clock Frequency: Mhz

□ Alternate Mach Optimization

```
Info: Attempting to checkout a license to run as leona
The license on this copy of lsl will expire in 41 days
Info: License passed
Session history will be logged to file 'c:/isptools/is
Info, Working Directory is now 'c:\isptools\ispsys\exe
->set _xmp_enable_renoir FALSE
FALSE
Info: system variable EXEMPLAR set to "C:\ISPTOOLS\ISP
Info: Loading Exemplar Blocks file: C:\ISPTOOLS\ISPSYS
Messages will be logged to file 'c:/isptools/ispsys/ex
Leonardo Spectrum for Vantis - v1999.1 |build 6.58, co
Copyright 1990-1999 Exemplar Logic, Inc.  All rights r

--
-- Welcome to Leonardo Spectrum for Vantis
-- Run By tlamb@REDCLOUD
-- Run Started On Wed Oct 20 12:03:53 Mountain Dayligh
|--
```

Ready | Working Directory: ...\tutorial\tutor3 | Line 19 Col 1

# Task 3 *Use Quick Setup to Synthesize the Design*

Everything that can be specified in the synthesis wizard can be specified on the Quick Setup tab. Once specified, you can click **Run Flow** to run the entire synthesis flow, including synthesis, global constraints, optimization, and writing netlist. Additionally, Quick Setup automatically sets up all options, defaults, and settings in the FlowTabs to assist you when walking through the more advanced tabs.

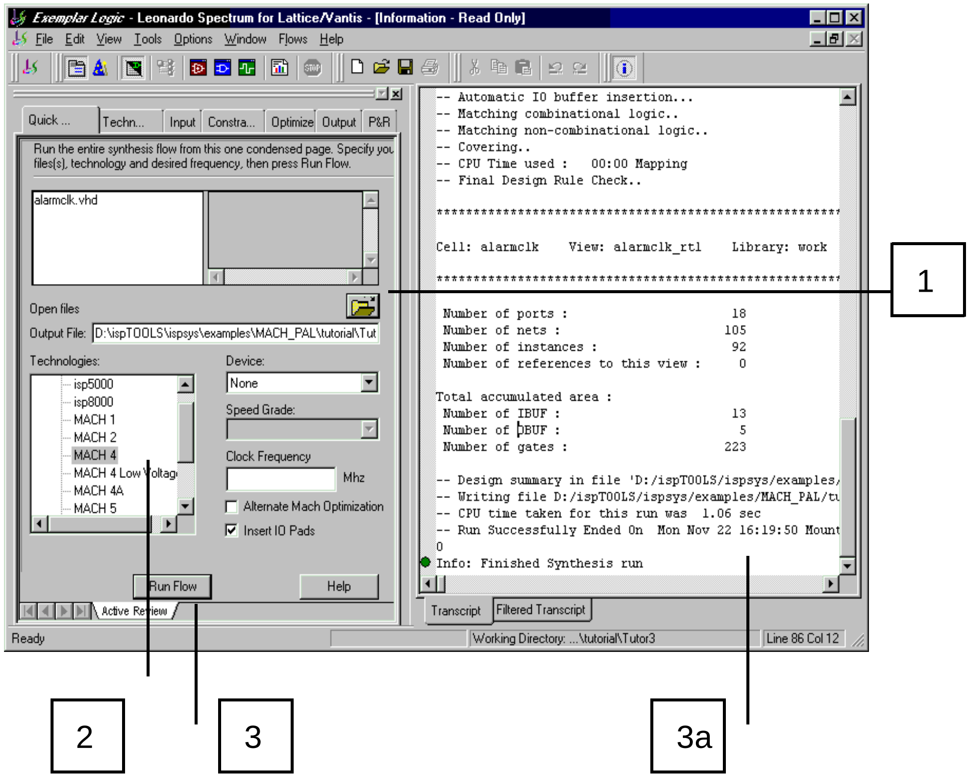
*To set up the synthesis run*:

1. Click the **Open File** icon and select the VHDL input file.

   Go to the ..`\examples\Tutorial\Tutor3` directory and select `alarmclk.vhd`. Notice that the software automatically points the output file to the project directory.
2. Under Technologies, select the **MACH 4** device family. You do not need to select a specific device; you will do this in ispDesignExpert.
3. Click **Run Flow**. LeonardoSpectrum runs the entire flow using all options set on all dialogs and tabs, including options which are not shown on this tab, and creates an EDIF file.

***Note**: The **Run Flow** button is not active until you have selected your Input File(s) and target technology. Notice in the Information window on the right (**3a**) that it says the run successfully ended when the synthesis process is complete.*

***Note**: Click the **Stop** icon to cancel the run.*



Run the entire synthesis flow from this one condensed page. Specify you files(s), technology and desired frequency, then press Run Flow.

alarmclk.vhd

Output File: D:\ispTOOLS\ispsys\examples\MACH_PAL\tutorial\Tut

Technologies: isp5000, isp8000, MACH 1, MACH 2, MACH 4, MACH 4 Low Voltage, MACH 4A, MACH 5

Device: None

Speed Grade:

Clock Frequency Mhz

☐ Alternate Mach Optimization

☑ Insert IO Pads

```
-- Automatic IO buffer insertion...
-- Matching combinational logic..
-- Matching non-combinational logic..
-- Covering..
-- CPU Time used :   00:00 Mapping
-- Final Design Rule Check..

*******************************************************

Cell: alarmclk    View: alarmclk_rtl    Library: work

*******************************************************

 Number of ports :                            18
 Number of nets :                            105
 Number of instances :                        92
 Number of references to this view :          0

Total accumulated area :
 Number of IBUF :                             13
 Number of OBUF :                              5
 Number of gates :                           223

-- Design summary in file 'D:/ispTOOLS/ispsys/examples/
-- Writing file D:/ispTOOLS/ispsys/examples/MACH_PAL/tu
-- CPU time taken for this run was  1.06 sec
-- Run Successfully Ended On  Mon Nov 22 16:19:50 Mount
0
Info: Finished Synthesis run
```

Working Directory: ...\tutorial\Tutor3

Line 86 Col 12

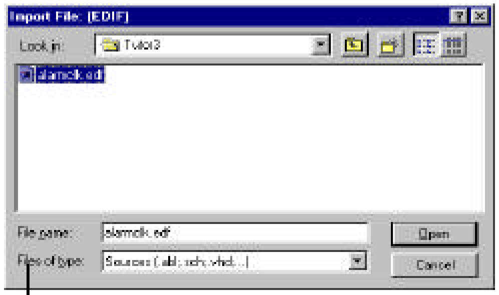
# Task 4 *Import the EDIF file into ispDesignExpert*

You can import EDIF 2.0.0 netlists from third-party synthesis tools such as Exemplar LeonardoSpectrum.

*To import an EDIF netlist into your project*:

1. In the Project Navigator, choose **Source** ⇒ **Import** to open the Import File dialog.
2. Select `alarmclk.edf`.
3. Select **OK** to open the Import EDIF dialog
4. Select **Exemplar** for the Vendor and click **OK**. The software adds the selected EDIF file (alarmclk.edf) to the project sources.

***Note**: After you import an EDIF file into the ispDesignExpert project, it is always linked in the Project Navigator. Therefore, if you make changes and recompile your VHDL file to create a new EDIF file, you just have to choose **View** ⇒ **Update** in the Project Navigator to update the process.*


Import File: [EDIF]

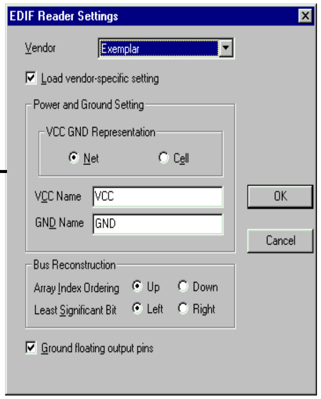
Look in: Tutor3

alarmclk.edf

File name: alarmclk.edf

Files of type: Sources (.abl; .sch; .vhd; ...)

1-2


EDIF Reader Settings

Vendor: Exemplar

☑ Load vendor-specific setting

Power and Ground Setting

VCC GND Representation: ● Net ○ Cell

VCC Name: VCC

GND Name: GND

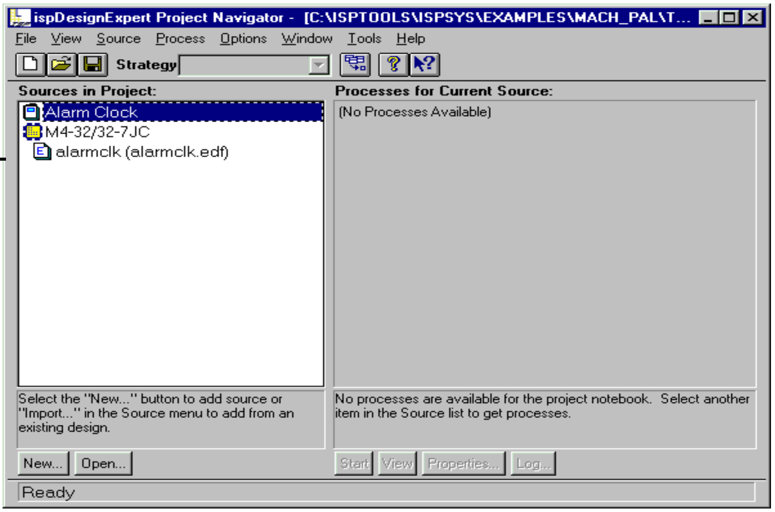
Bus Reconstruction

Array Index Ordering: ● Up ○ Down

Least Significant Bit: ● Left ○ Right

☑ Ground floating output pins

3


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PAL\T...

Sources in Project:

Alarm Clock
M4-32/32-7JC
alarmclk (alarmclk.edf)

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

4

# Task 5 *Target a Device and Fit the Design*

The Project Navigator lets you target a design to a specific Lattice device at any time during the design process.

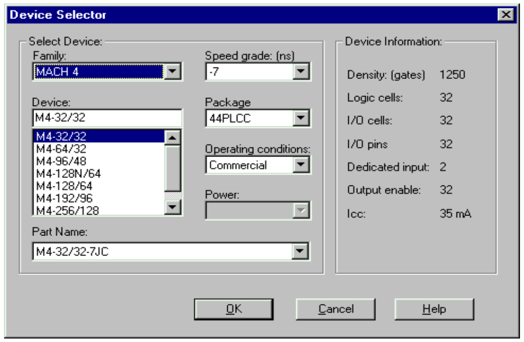
*To target a device and run the Fitter*:

1. In the Sources window, double-click **default device** to open the Device Selector dialog. The dialog shows the available device families and the devices in the selected family.
2. In the Device Selector dialog under Family, select the **MACH 4** device family.
3. Select the **M4-32/32** device.
4. Accept the default settings and then click **OK**.
5. Click **Yes** to confirm that you wish to change device families.

***Note**: When you change device kits, the ispDesignExpert design environment reconfigures to facilitate designing with the selected device family.*

6. The ispDesignExpert software shows the selected device in the Sources window.
7. With the target device selected in the Sources window, double-click **Fit Design** in the Processes window to run the Fitter. ispDesignExpert fits the design in the specified device and generates a JEDEC file.

If you want to see how to simulate this design using Model*Sim*, see Tutorial 12.



Select Device:

Family: MACH 4

Speed grade: (ns) -7

Device: M4-32/32

M4-32/32
M4-64/32
M4-96/48
M4-128N/64
M4-128/64
M4-192/96
M4-256/128

Package 44PLCC

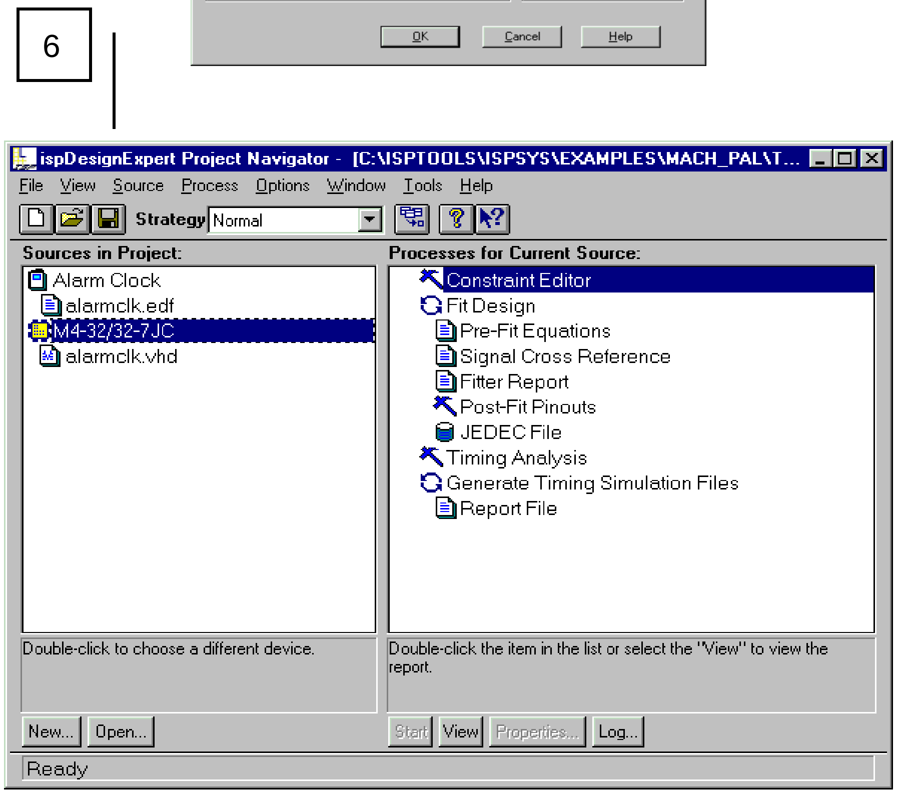
Operating conditions: Commercial

Power:

Part Name: M4-32/32-7JC

Device Information:

| | |
|---|---|
| Density: (gates) | 1250 |
| Logic cells: | 32 |
| I/O cells: | 32 |
| I/O pins | 32 |
| Dedicated input: | 2 |
| Output enable: | 32 |
| Icc: | 35 mA |



Sources in Project:

Alarm Clock
alarmclk.edf
M4-32/32-7JC
alarmclk.vhd

Processes for Current Source:

Constraint Editor
Fit Design
Pre-Fit Equations
Signal Cross Reference
Fitter Report
Post-Fit Pinouts
JEDEC File
Timing Analysis
Generate Timing Simulation Files
Report File

Double-click to choose a different device.

Double-click the item in the list or select the "View" to view the report.

Ready

# Congratulations!

You have completed the HDL Design Entry with LeonardoSpectrum tutorial. In this tutorial you have learned how to:

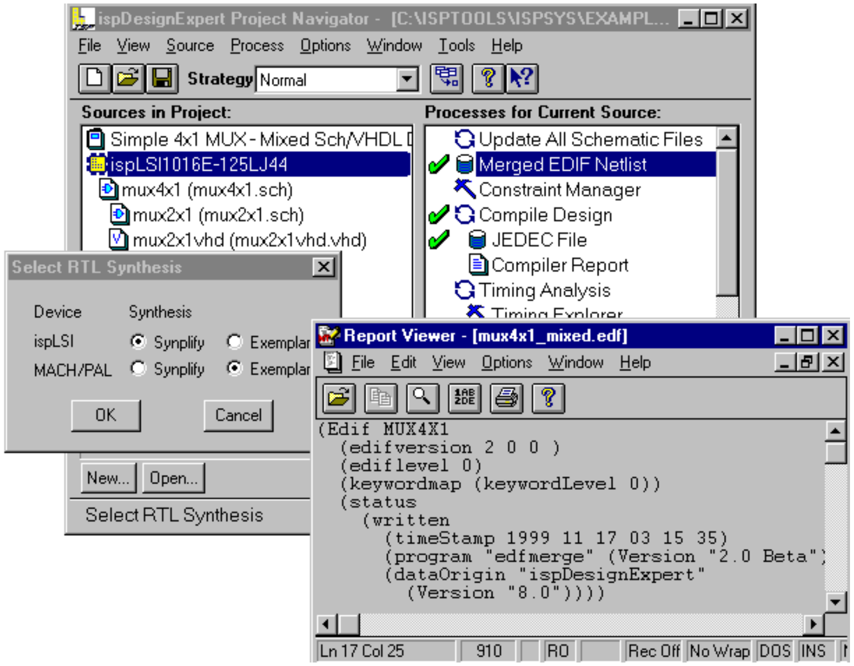
- create a new project in ispDesignExpert.
- start LeonardoSpectrum from ispDesignExpert.
- use the Quick Setup tab in LeorardoSprectum to set up and run synthesis, creating an EDIF files.
- import the EDIF file into ispDesignExpert.
- target a device for the design.
- run the Fitter and automatically generate a JEDEC file.

# Tutorial 6 Mixed Design Entry and Implementation

ispDesignExpert features the following mixed design entries:

- mixed schematic and ABEL-HDL design
- mixed schematic and VHDL design
- mixed schematic and Verilog HDL design

This tutorial shows how to implement a mixed design of schematic and VHDL using third-party synthesis tools.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
Simple 4x1 MUX - Mixed Sch/VHDL D
ispLSI1016E-125LJ44
mux4x1 (mux4x1.sch)
mux2x1 (mux2x1.sch)
mux2x1vhd (mux2x1vhd.vhd)
Processes for Current Source:
Update All Schematic Files
Merged EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Timing Explorer
New... Open...
Select RTL Synthesis
Select RTL Synthesis
OK
Cancel
Report Viewer - [mux4x1_mixed.edf]
File Edit View Options Window Help
Ln 17 Col 25 910 RO Rec Off No Wrap DOS INS

| Device | Synthesis | |
|---|---|---|
| ispLSI | ● Synplify | ○ Exemplar |
| MACH/PAL | ○ Synplify | ● Exemplar |

```
(Edif MUX4X1
  (edifversion 2 0 0 )
  (ediflevel 0)
  (keywordmap (keywordLevel 0))
  (status
    (written
      (timeStamp 1999 11 17 03 15 35)
      (program "edfmerge" (Version "2.0 Beta")
      (dataOrigin "ispDesignExpert"
        (Version "8.0"))))
```

## Learning Objectives

When you are finished with this tutorial, you should understand the steps and tools necessary to implement a mixed design in ispDesignExpert.

## Time to Complete This Tutorial

The time to complete this tutorial is about 20 minutes.

# Task 1 *Create a New Project in ispDesignExpert*

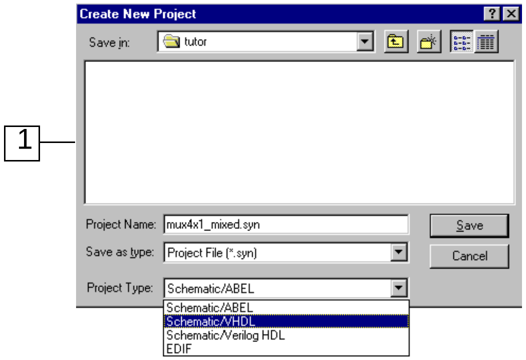
After starting the Project Navigator, you are ready to create a new project with mixed schematic and VHDL design modules. Create a directory `tutor` to save your tutorial example.

*To create a new project*:

1. Choose **File** ⇒ **New Project** to open the Create New Project dialog.
2. In the dialog, navigate to the `ispTools\ispsys\examples\ispLSI_GAL` directory.
3. Create a new directory called `mixed`.
4. Go into the new folder and type the name `mux4x1_mixed.syn` for the Project Name, choose Schematic/VHDL in the Project Type list box, and then click **Save**.

   The untitled project with ispLSI default device (ispLSI5384V-125LB388) appears in the Sources window of the Project Navigator.
5. Double-click the project book to open the Project Properties dialog. Type `Simple 4x1 MUX - Mixed Sch/VHDL Design` for the project title. Click **OK** to accept the change.
6. Double-click the device icon to open the Device Selector dialog. Select `ispLSI1016E-125LJ44` and click **OK** to accept the device.
7. Click **Yes** in the Confirm Change dialog to confirm the changes to device kits.

The Project Navigator Processes window reconfigures to facilitate with the selected device.



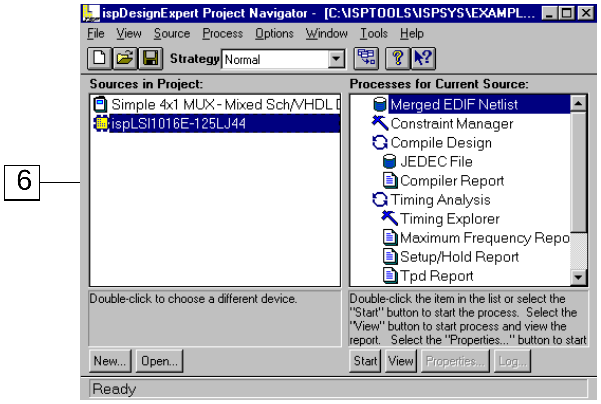
Save in: tutor

Project Name: mux4x1_mixed.syn

Save as type: Project File (*.syn)

Project Type: Schematic/ABEL

Schematic/ABEL
Schematic/VHDL
Schematic/Verilog HDL
EDIF


6
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
New...
Open...
Start
View
Properties...
Log...

Strategy Normal

Sources in Project:
Simple 4x1 MUX - Mixed Sch/VHDL D
ispLSI1016E-125LJ44

Processes for Current Source:
Merged EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Timing Explorer
Maximum Frequency Repo
Setup/Hold Report
Tpd Report

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "View" button to start process and view the report. Select the "Properties..." button to start

Ready

# Task 2 *Create or Import Mixed Design Entries*

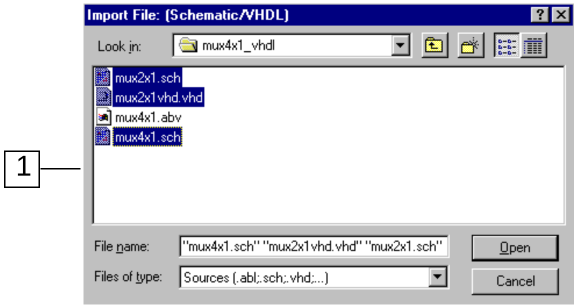
Now you need to add schematic and VHDL sources to the project.

You can create a design source by selecting **Source** ⇒ **New** from the Project Navigator. In the New Source dialog, select the desired source type you want to create for the top module in this mixed design. See the *ispDesignExpert User Manual* for detailed information on mixed design entries.

*In this task you are going to import mixed designs:*

1. Select **Source** ⇒ **Import** from the Project Navigator to open the Import File dialog.
2. Navigate to the directory of `ispTOOLS\ispsys\examples\ ispLSI_GAL\vhdl\mux4x1_vhdl`. Choose Sources (`.abl;.sch;.vhd;...`) in the Files of type list box. Select `mux4x1.sch`, `mux2x1.sch`, and `mux2x1vhd.vhd` in the file display area, then click **Open**. In the pop-up Import Source Type dialog, choose VHDL Module in the Type of Source field for `mux2x1vhd.vhd` file. Click **OK** to close the dialog.

   The top design module `mux4x1.sch` with two submodules `mux2x1.sch` and `mux2x1vhd.vhd` are imported into the Sources window as shown on the right.

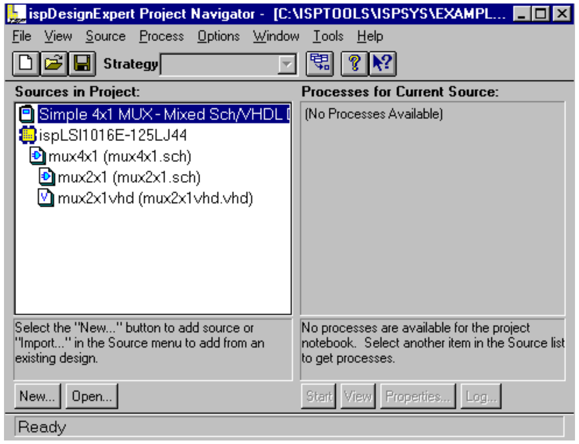


Look in: mux4x1_vhdl

mux2x1.sch
mux2x1vhd.vhd
mux4x1.abv
mux4x1.sch

File name: "mux4x1.sch" "mux2x1vhd.vhd" "mux2x1.sch"

Files of type: Sources (.abl;.sch;.vhd;...)


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
Processes for Current Source:
New...
Open...
Start
View
Properties...
Log...

Simple 4x1 MUX - Mixed Sch/VHDL
ispLSI1016E-125LJ44
mux4x1 (mux4x1.sch)
mux2x1 (mux2x1.sch)
mux2x1vhd (mux2x1vhd.vhd)

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

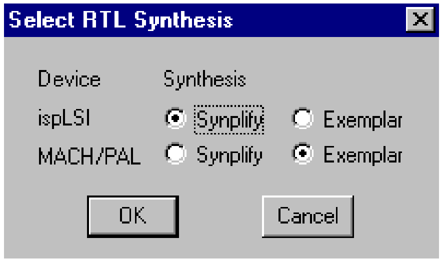
Ready

# Task 3 *Select RTL Synthesis Tool*

ispDesignExpert provides two synthesis tools for your designs with VHDL or Verilog HDL entries. Synplicity Synplify is the default for ispLSI devices, while MACH devices have Exemplar LeonardoSpectrum as the default. It is easy to use RTL synthesis tool to assign Synplify or Exemplar to run synthesis for different flows.

*To select an RTL synthesis tool:*

1. Select **Options** ⇒ **Select RTL Synthesis** from the Project Navigator. The Select RTL Synthesis dialog is displayed.
2. The current device is ispLSI. Check Synplify (or Exemplar as you like). Click **OK** to accept the synthesis tool.



Select RTL Synthesis

| Device | Synthesis | |
|---|---|---|
| ispLSI | ● Synplify | ○ Exemplar |
| MACH/PAL | ○ Synplify | ● Exemplar |

# Task 4 *Merge EDIF Files*

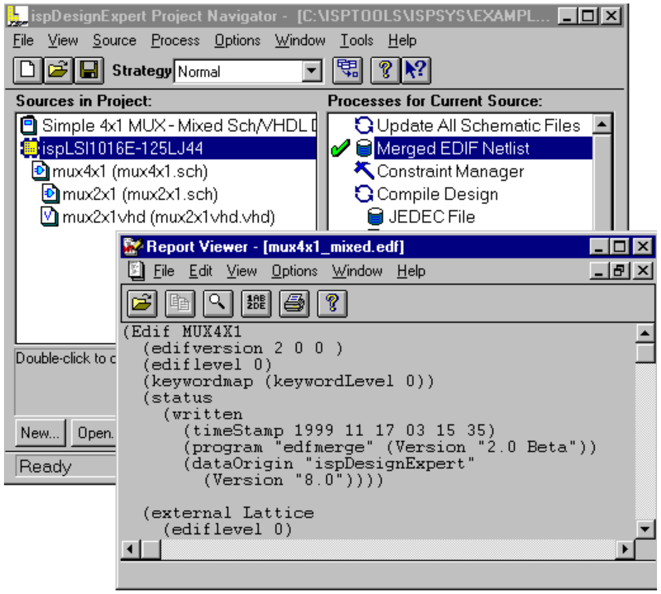
Before you compile the mixed design, you need to merge the EDIF generated from the schematics in the design and the EDIF generated by the selected synthesis tool after VHDL/Verilog HDL synthesis.

*To merge EDIF files:*

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Merged EDIF Netlist**, or select the process and click **Start** to run the process.

   The schematics are processed by the system, and the selected synthesis tool runs for the `.vhd` file synthesis.

   After successful processing, a merged `mux4x1_mixed.edf` is produced. Click **View** to open the Report Viewer and view the merged `.edf` file in detail.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Double-click to c
New...
Open.
Ready
Report Viewer - [mux4x1_mixed.edf]
File Edit View Options Window Help

Strategy Normal

Sources in Project:

- Simple 4x1 MUX - Mixed Sch/VHDL [
- ispLSI1016E-125LJ44
  - mux4x1 (mux4x1.sch)
    - mux2x1 (mux2x1.sch)
    - mux2x1vhd (mux2x1vhd.vhd)

Processes for Current Source:

- Update All Schematic Files
- ✓ Merged EDIF Netlist
- Constraint Manager
- Compile Design
  - JEDEC File

```
(Edif MUX4X1
  (edifversion 2 0 0 )
  (ediflevel 0)
  (keywordmap (keywordLevel 0))
  (status
    (written
      (timeStamp 1999 11 17 03 15 35)
      (program "edfmerge" (Version "2.0 Beta"))
      (dataOrigin "ispDesignExpert"
        (Version "8.0"))))

  (external Lattice
    (ediflevel 0)
```

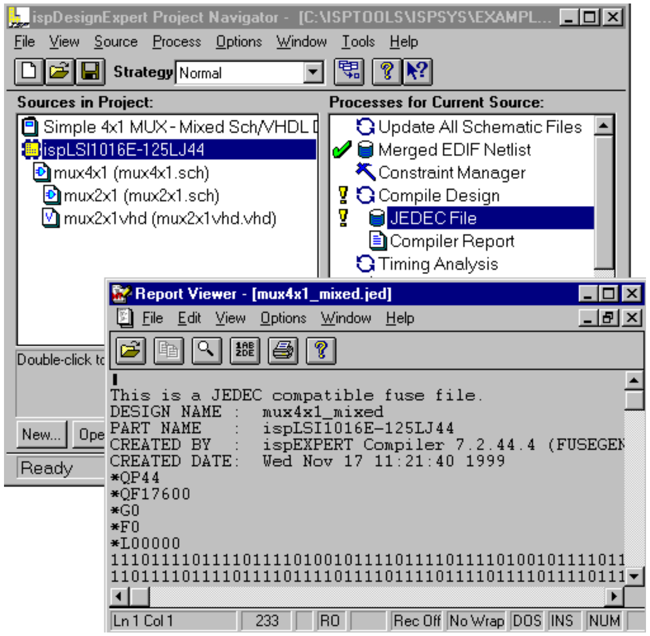
# Task 5 *Fit the Design*

In this task, you will implement the design into the target device with the EDIF netlist generated in the previous step.

*To fit the design into the target device*:

1. In the Sources window, select the device.
2. Double-click Compile Design in the Processes window or select the process and click the **Start** button to run the compilation.

   This starts the ispEXPERT Compiler and the design is automatically compiled and fitted into the target device. A JEDEC file is generated after successful compilation. You can click **View** to open the Report Viewer and view the `.jed` file in detail.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
Simple 4x1 MUX - Mixed Sch/VHDL D
ispLSI1016E-125LJ44
mux4x1 (mux4x1.sch)
mux2x1 (mux2x1.sch)
mux2x1vhd (mux2x1vhd.vhd)
Processes for Current Source:
Update All Schematic Files
Merged EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis
Double-click to
New...
Ope
Ready
Report Viewer - [mux4x1_mixed.jed]
File Edit View Options Window Help
Ln 1 Col 1
233
RO
Rec Off
No Wrap
DOS
INS
NUM

```
This is a JEDEC compatible fuse file.
DESIGN NAME :  mux4x1_mixed
PART NAME   :  ispLSI1016E-125LJ44
CREATED BY  :  ispEXPERT Compiler 7.2.44.4 (FUSEGEN
CREATED DATE:  Wed Nov 17 11:21:40 1999
*QP44
*QF17600
*G0
*F0
*L00000
111011110111101111010010111101111011110100101111011
110111101111011110111101111011110111101111011110111
```

# Congratulations!

You have completed the Mixed Design Entry and Implementation tutorial. In this tutorial you have learned how to:

- create a new project of mixed schematics and VHDL design in ispDesignExpert.
- create or import design entries.
- select an RTL synthesis tool for the target device.
- merge an EDIF netlist.
- fit the design for the target device.

# Part III: Design Implementation and Verification with ispDesignExpert

# *ispLSI Design Implementation and Verification*

This tutorial provides an overview of the features and operation of ispDesignExpert, focusing on the tasks and tools needed to implement and verify an ispLSI design.

## Prerequisites

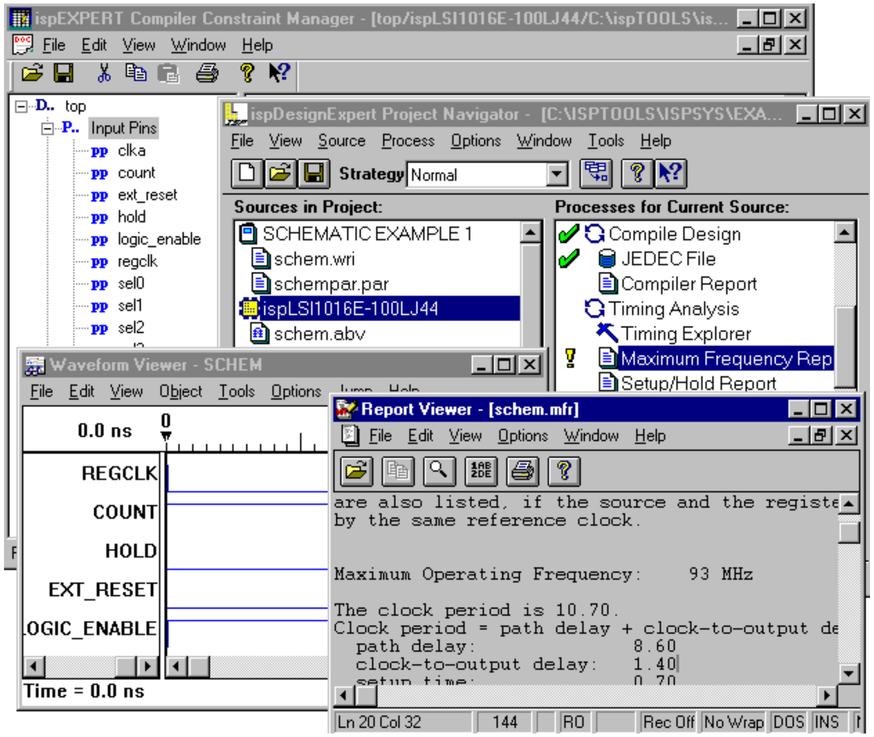
Before attempting this tutorial, you should complete the Schematic or ABEL-HDL tutorial.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of the steps and tools necessary to implement and verify an ispLSI design using ispDesignExpert.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.



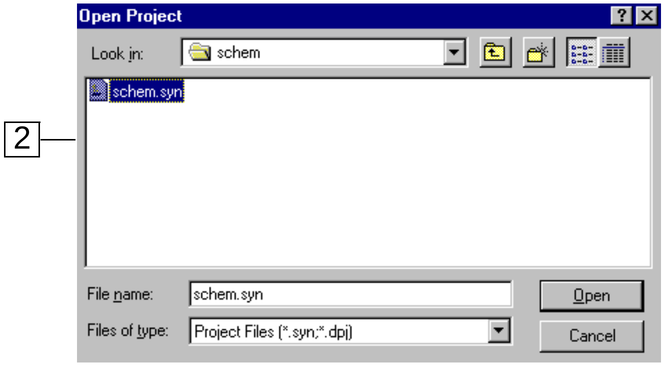
```
are also listed, if the source and the registe
by the same reference clock.


Maximum Operating Frequency:    93 MHz

The clock period is 10.70.
Clock period = path delay + clock-to-output de
  path delay:                 8.60
  clock-to-output delay:      1.40
  setup time:                 0.70
```

# Task 1 *Open the Project*

*To open the tutorial project*.

1. In the Project Navigator, choose **File** ⇒ **Open Example** to open the dialog.
2. Select the file `ispLSI_GAL\abel\schem\schem.syn` and click **Open** to open the project in the Project Navigator.

   The `SCHEMATIC EXAMPLE 1` appears in the Sources window of the Project Navigator.

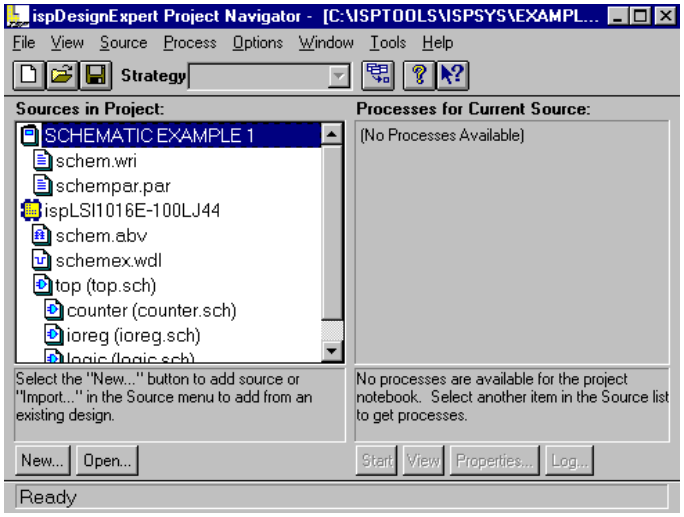


Look in: schem

schem.syn

File name: schem.syn

Files of type: Project Files (*.syn;*.dpj)



Sources in Project:

- SCHEMATIC EXAMPLE 1
- schem.wri
- schempar.par
- ispLSI1016E-100LJ44
- schem.abv
- schemex.wdl
- top (top.sch)
- counter (counter.sch)
- ioreg (ioreg.sch)
- logic (logic.sch)

Processes for Current Source:

(No Processes Available)

Select the "New..." button to add source or "Import..." in the Source menu to add from an existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Ready

# Task 2 *Select a Device*

The Project Navigator lets you target a design to a specific device at any time during the design process.

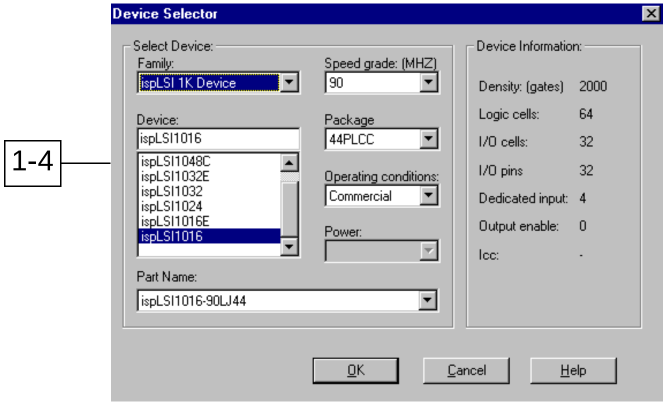
*To select a device:*

1. Double-click the device icon in the Sources window. The Device Selector dialog box opens.
2. Select `ispLSI 1K` Device family.
3. Click on `ispLSI1016` device.
4. Select `ispLSI1016-90LJ44` for the part name.

   The Device Information field lists the detailed information for the selected device.
5. Click **OK** to accept the settings.
6. Click **Yes** to confirm that you wish to change device families (if prompted).

***Note****: ispLSI default device is ispLSI5384V-125LB388.*

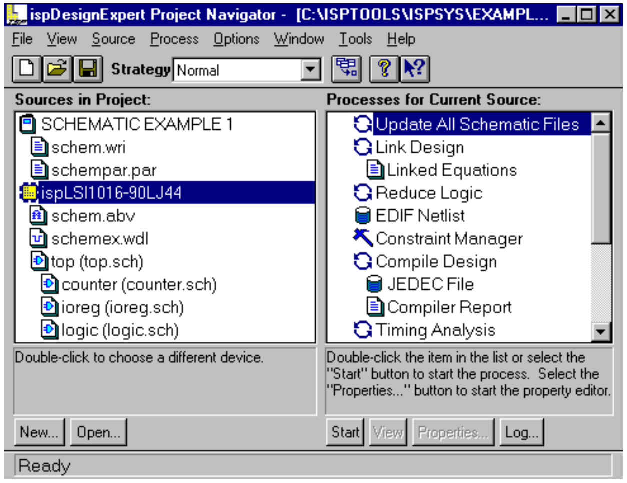
When you change device, the ispDesignExpert design environment reconfigures to facilitate designing with the selected device.



Select Device:
Family: ispLSI 1K Device
Speed grade: (MHZ) 90
Device: ispLSI1016
ispLSI1048C
ispLSI1032E
ispLSI1032
ispLSI1024
ispLSI1016E
ispLSI1016
Package 44PLCC
Operating conditions: Commercial
Power:
Part Name: ispLSI1016-90LJ44

Device Information:

| | |
|---|---|
| Density: (gates) | 2000 |
| Logic cells: | 64 |
| I/O cells: | 32 |
| I/O pins | 32 |
| Dedicated input: | 4 |
| Output enable: | 0 |
| Icc: | - |


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Strategy Normal
New...
Open...
Start
View
Properties...
Log...

Sources in Project:
SCHEMATIC EXAMPLE 1
schem.wri
schempar.par
ispLSI1016-90LJ44
schem.abv
schemex.wdl
top (top.sch)
counter (counter.sch)
ioreg (ioreg.sch)
logic (logic.sch)

Processes for Current Source:
Update All Schematic Files
Link Design
Linked Equations
Reduce Logic
EDIF Netlist
Constraint Manager
Compile Design
JEDEC File
Compiler Report
Timing Analysis

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

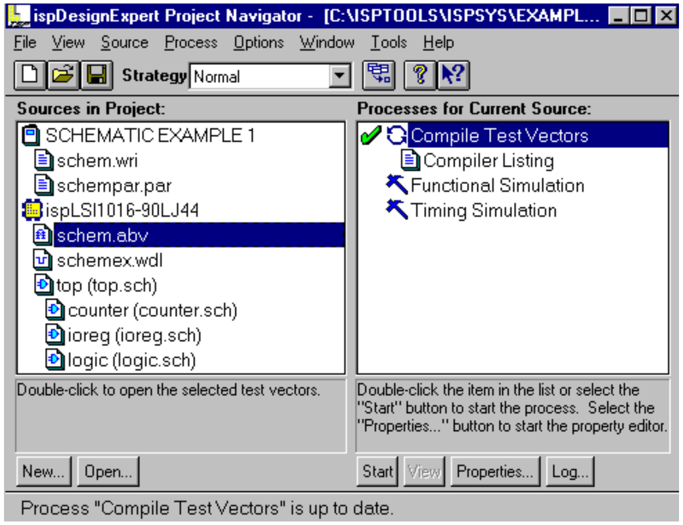
# Task 3 *Compile Test Vectors*

When you compile test vectors, the design is automatically formatted as netlists and at the same time the stimulus is compiled to serve as input to the Lattice Logic Simulator.

*To compile test vectors*:

1. In the Sources window, select the `.abv` source.
2. In the Processes window, double-click **Compile Test Vectors**.

   After successful compilation, a green check mark is added to the selected process.



ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...

Sources in Project:

- SCHEMATIC EXAMPLE 1
- schem.wri
- schempar.par
- ispLSI1016-90LJ44
- schem.abv
- schemex.wdl
- top (top.sch)
- counter (counter.sch)
- ioreg (ioreg.sch)
- logic (logic.sch)

Processes for Current Source:

- ✓ Compile Test Vectors
- Compiler Listing
- Functional Simulation
- Timing Simulation

Double-click to open the selected test vectors.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Process "Compile Test Vectors" is up to date.

# Task 4 *Functional Simulation*

Two types of stimulus files that can be accepted by the Lattice Logic Simulator are:

- graphic waveform file (`.wdl`)
- test vector file (`.abv`)

Functional simulation is called pre-route simulation because it occurs before the design has been fitted and routed. Functional simulation helps you find logical or coding errors early in the design cycle.

*To run functional simulation and view the results*:

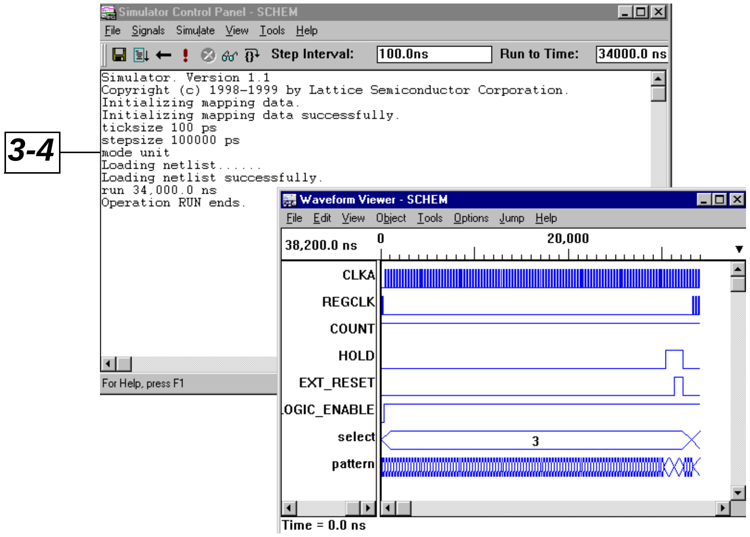
1. In the Sources window, select `.abv.`
2. In the Processes window, double-click **Functional Simulation**.

   The Simulator Control Panel (Simcp) is invoked and netlist is loaded successfully.
3. Click the Run icon or select **Simulate** ⇒ **Run** to start the simulation.

***Tip**: If **View** ⇒ **Show Waveforms** in the Simcp is checked, the Waveform Viewer will be opened during the simulation to show waveforms of the simulation results.*

4. Select **Tools** ⇒ **Waveform Viewer** to open the Waveform Viewer. Waveforms of the simulation results are displayed in the Waveform Viewer window.

   You can refer to the ***Design Verification Tools User Manual*** for information on selecting waveforms to show in the Waveform Viewer.



3-4

Simulator Control Panel - SCHEM

Step Interval: 100.0ns Run to Time: 34000.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 34,000.0 ns
Operation RUN ends.
```

For Help, press F1

Waveform Viewer - SCHEM

Time = 0.0 ns

File Signals Simulate View Tools Help
File Edit View Object Tools Options Jump Help
38,200.0 ns
0
20,000
CLKA
REGCLK
COUNT
HOLD
EXT_RESET
OGIC_ENABLE
select
3
pattern

# Task 5 *Assign Design Constraints*

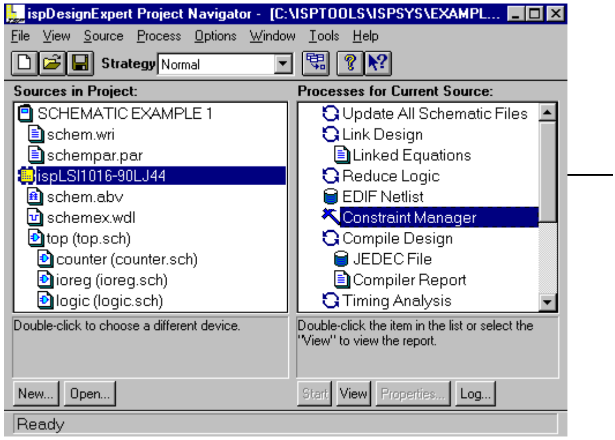
The Constraint Manager lets you set pin, symbol, and net attributes for the signals and pins in your design. You can also read in an existing Property File or save the attributes as a Property File.

*To assign constraints to the design*:

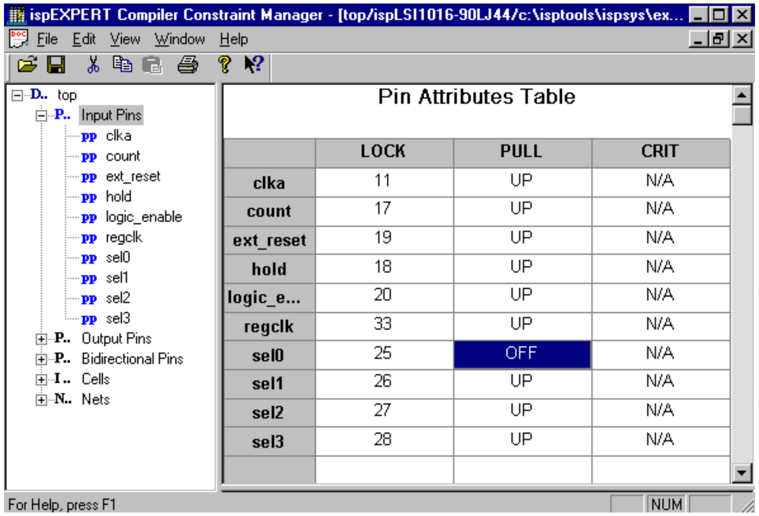
1. In the Sources window, select the target device.
2. In the Processes window, double-click **Constraint Manager**.

   The ispEXPERT Compiler is enabled in the background before the Constraint Manager opens.
3. In the Constraint Manager window, click the plus sign (**+**) in the Design Browser on the left to expand the list to see the signal or pin names.
4. Double-click on Input Pins to add all the pins in this category to the Pin Attributes Table.
5. Click the right mouse button on a cell to display a list of attribute values that can be used for that attribute. In this way, change the PULL attribute value of sel0 from UP to OFF.
6. Select **File** ⇒ **Save Property**, and then exit the Constraint Manager window. The new value is saved and reflected in your project.

For more information on using the Constraint Manager to assign attributes for the signals and pins in your design, refer to the *ispEXPERT Compiler User Manual*.



1



Pin Attributes Table

| | LOCK | PULL | CRIT |
|---|---|---|---|
| clka | 11 | UP | N/A |
| count | 17 | UP | N/A |
| ext_reset | 19 | UP | N/A |
| hold | 18 | UP | N/A |
| logic_e... | 20 | UP | N/A |
| regclk | 33 | UP | N/A |
| sel0 | 25 | OFF | N/A |
| sel1 | 26 | UP | N/A |
| sel2 | 27 | UP | N/A |
| sel3 | 28 | UP | N/A |

# Task 6 *Set Compiler Properties*

You can set the properties for the ispEXPERT Compiler using the Compiler Properties dialog. The dialog lets you set settings and device options to control how the Compiler processes your design.

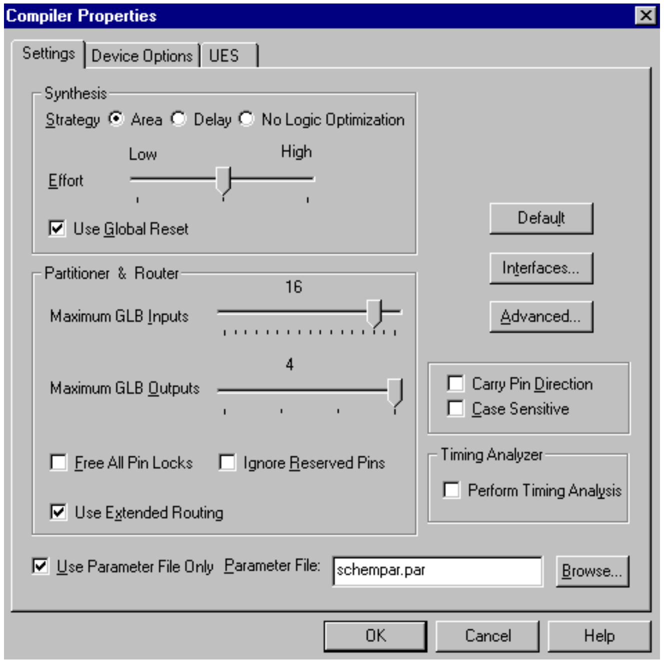
*To set the Compiler properties*:

1. In the Sources window, select the target device.
2. In the Processes window, select **Compile Design**.
3. Click the **Properties** button under the Processes window. The Compiler Properties dialog is displayed, three tabs are available for you to change the Compiler options.

***Tip****: You can also open the Compiler Properties dialog by selecting* ***Tools*** *⇒* ***Compiler Properties*** *from the Project Navigator.*

4. On the Settings tab, check the Area radio button in the Synthesis Strategy field.
5. Click **OK** to accept the setting.

You can refer to the *ispDesignExpert User Manual* for more information on how to set the Compiler properties.



Compiler Properties

Settings | Device Options | UES

Synthesis
Strategy ● Area ○ Delay ○ No Logic Optimization
Effort Low — High
☑ Use Global Reset

Partitioner & Router
Maximum GLB Inputs 16
Maximum GLB Outputs 4
☐ Free All Pin Locks ☐ Ignore Reserved Pins
☑ Use Extended Routing

☐ Carry Pin Direction
☐ Case Sensitive

Timing Analyzer
☐ Perform Timing Analysis

☑ Use Parameter File Only Parameter File: schempar.par

# Task 7 *Fit the Design*

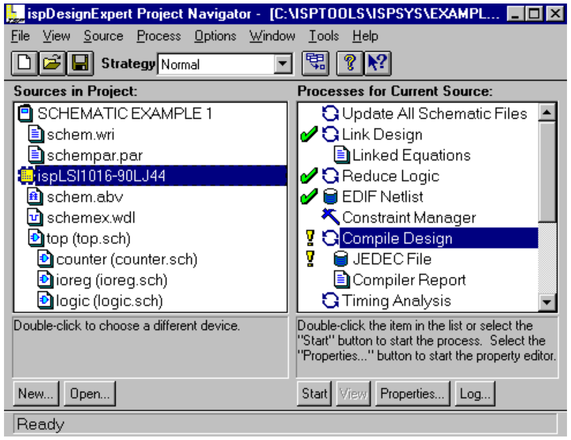
In this step, you need to fit the design into a Lattice Semiconductor ispLSI part.

*To run the ispEXPERT Compiler*:

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Compile Design** or click the **Start** button to start processing the design.

   For more information about the ispEXPERT Compiler, refer to the *ispEXPERT Compiler User Manual*.)

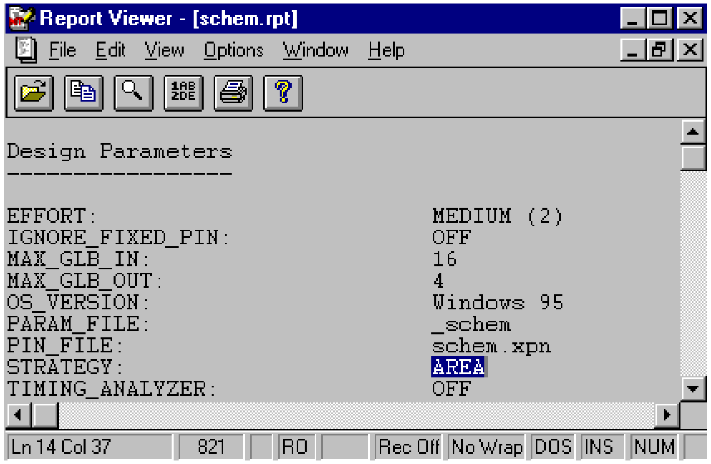
   Check marks are added to the processes associated with the design fitting to show the current status of the process.
3. After fitting the design into the ispLSI part, double-click Compiler Report in the Processes window to open the Report Viewer and view the report (`schem.rpt`).



Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready


Report Viewer - [schem.rpt]
File Edit View Options Window Help

```
Design Parameters
-----------------

EFFORT:                          MEDIUM (2)
IGNORE_FIXED_PIN:                OFF
MAX_GLB_IN:                      16
MAX_GLB_OUT:                     4
OS_VERSION:                      Windows 95
PARAM_FILE:                      _schem
PIN_FILE:                        schem.xpn
STRATEGY:                        AREA
TIMING_ANALYZER:                 OFF
```

Ln 14 Col 37 | 821 | RO | Rec Off | No Wrap | DOS | INS | NUM

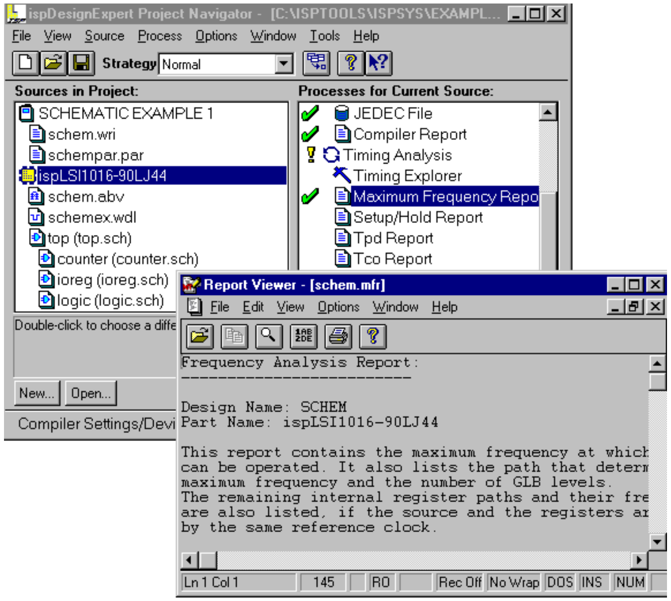
# Task 8 *Timing Analysis*

The ispDesignExpert software has a built-in Timing Analyzer (ispTA) that provides accurate pin-to-pin timing information for an ispLSI design after it has been processed by the ispEXPERT Compiler.

*To run Timing Analysis and view the timing reports:*

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Timing Analysis** or click the **Start** button to run the timing analysis.
3. Double-click **Maximum Frequency Report** under the Timing Analysis process.

   The report (schem.mfr) is displayed in the Report Viewer window.

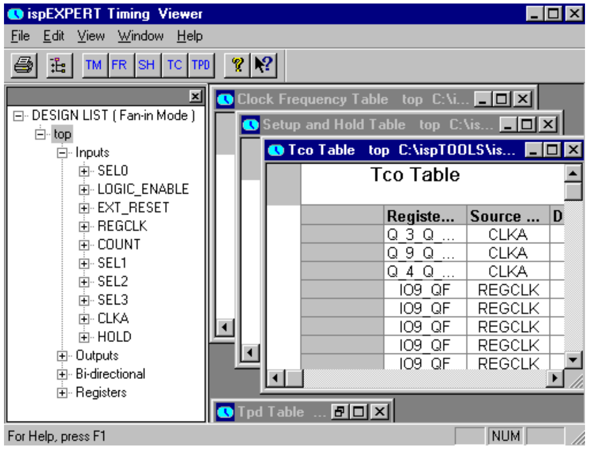


```
Frequency Analysis Report:
--------------------------

Design Name: SCHEM
Part Name: ispLSI1016-90LJ44

This report contains the maximum frequency at which
can be operated. It also lists the path that determ
maximum frequency and the number of GLB levels.
The remaining internal register paths and their fre
are also listed, if the source and the registers ar
by the same reference clock.
```

You can open the Timing Explorer to query the timing information after you compile the design.

*To run the Timing Explorer in the following two ways:*

- Double-click **Timing Explorer** in the Processes window
- Select **Tools** ⇒ **Timing Explorer** from the Project Navigator



Tco Table

| | Registe... | Source ... | D |
|---|---|---|---|
| | Q_3_Q_... | CLKA | |
| | Q_9_Q_... | CLKA | |
| | Q_4_Q_... | CLKA | |
| | IO9_QF | REGCLK | |
| | IO9_QF | REGCLK | |
| | IO9_QF | REGCLK | |
| | IO9_QF | REGCLK | |
| | IO9_QF | REGCLK | |

***Note**: The ispEXPERT Compiler GUI is enabled when you invoke the Timing Explorer. If you close the Compiler window, the Timing Explorer will be closed, too. For more information on using the Timing Explorer to query timing information, refer to the ispEXPERT Compiler User Manual.*

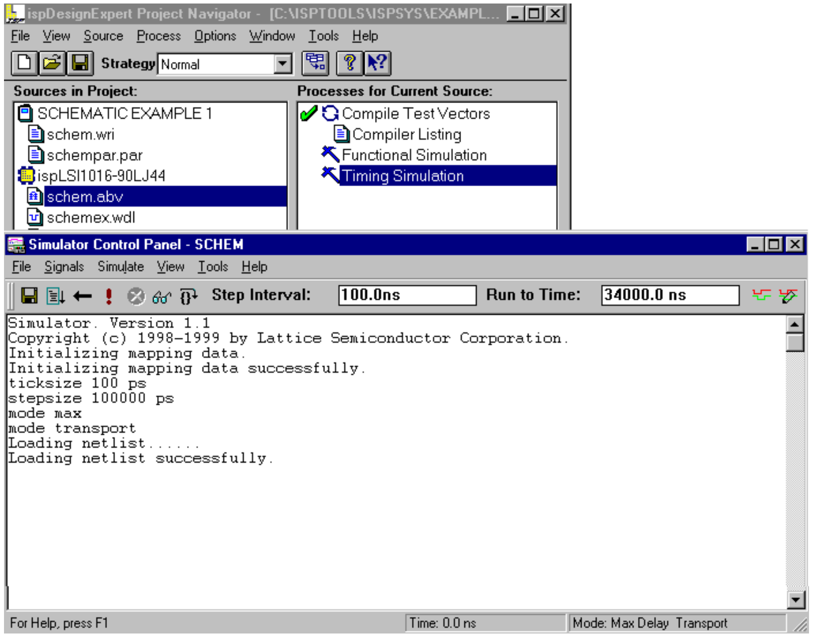
# Task 9 *Timing Simulation*

*To run timing simulation:*

1. In the Sources window, click the `.abv` file.
2. In the Processes window, double-click Timing Simulation.

   The Simulator Control Panel is displayed and the netlists are loaded in the Simcp window.
3. Click the Run icon or select **Simulate** ⇒ **Run** to start the simulation.

As the timing simulation steps are similar to functional simulation, you can refer to Task4, “Functional Simulation for information how to view the simulation results.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPL...
File View Source Process Options Window Tools Help
Sources in Project:
SCHEMATIC EXAMPLE 1
schem.wri
schempar.par
ispLSI1016-90LJ44
schem.abv
schemex.wdl
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Functional Simulation
Timing Simulation
Simulator Control Panel - SCHEM
File Signals Simulate View Tools Help
For Help, press F1

Strategy: Normal

Step Interval: 100.0ns

Run to Time: 34000.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode max
mode transport
Loading netlist......
Loading netlist successfully.
```

Time: 0.0 ns

Mode: Max Delay Transport

# Task 10 *Reset the Compiler Properties and Reanalyze the Timing*

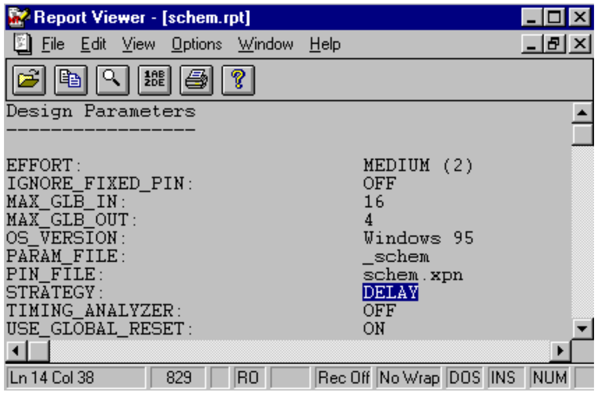
In a previous task you learned how to set the Compiler properties using the Compiler Properties dialog.

Now you will change the Compiler setting, and re-run the timing analysis process and see the differences in the reports generated by the Compiler.

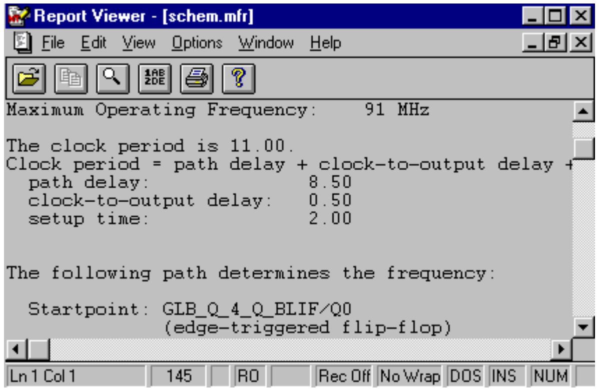
*To change the Compiler properties and re-run timing analysis*:

1. In the Project Navigator, choose **Tools** ⇒ **Compiler Properties** to open the dialog.
2. On the Settings tab, check the **Delay** radio button in the Synthesis Strategy field.
3. Click **OK** to close the dialog.
4. In the Sources window, select the target device. Then in the Processes window, double-click **Timing Analysis**. Notice this runs the Compiler again.
5. After successful compilation, double-click **Compiler Report** in the Processes window to view the report. You can see the change to the Compiler property reflected in this report.
6. In the Processes window, double-click **Maximum Frequency Report** to display it in the Report Viewer.

   Compare the report with the one before you changed the Compiler properties.


Report Viewer - [schem.rpt]
File Edit View Options Window Help
Ln 14 Col 38
829
RO
Rec Off
No Wrap
DOS
INS
NUM

```
Design Parameters
-----------------

EFFORT:                         MEDIUM (2)
IGNORE_FIXED_PIN:               OFF
MAX_GLB_IN:                     16
MAX_GLB_OUT:                    4
OS_VERSION:                     Windows 95
PARAM_FILE:                     _schem
PIN_FILE:                       schem.xpn
STRATEGY:                       DELAY
TIMING_ANALYZER:                OFF
USE_GLOBAL_RESET:               ON
```


Report Viewer - [schem.mfr]
File Edit View Options Window Help
Ln 1 Col 1
145
RO
Rec Off
No Wrap
DOS
INS
NUM

```
Maximum Operating Frequency:    91 MHz

The clock period is 11.00.
Clock period = path delay + clock-to-output delay +
  path delay:               8.50
  clock-to-output delay:    0.50
  setup time:               2.00


The following path determines the frequency:

  Startpoint: GLB_Q_4_Q_BLIF/Q0
              (edge-triggered flip-flop)
```

# Congratulations!

You have completed the Design Implementation and Verification for ispLSI Devices tutorial. In this tutorial you have learned how to:

- choose a device family and select a specific device.
- compile the test vector.
- run simulation and view the results using the Waveform Viewer.
- use the Constraint Manager to specify pin and node assignments for the Compiler.
- set properties for the Compiler using the Compiler Properties dialog.
- run the ispEXPERT Compiler and open the Compiler report.
- analyze the timing results.
- change the Compiler properties and re-analyze the timing results.

# Tutorial 8 MACH Design Implementation and Verification

This tutorial provides an overview of the features and operation of ispDesignExpert, focusing on the tasks and tools needed to implement and verify a MACH device design.

## Prerequisites

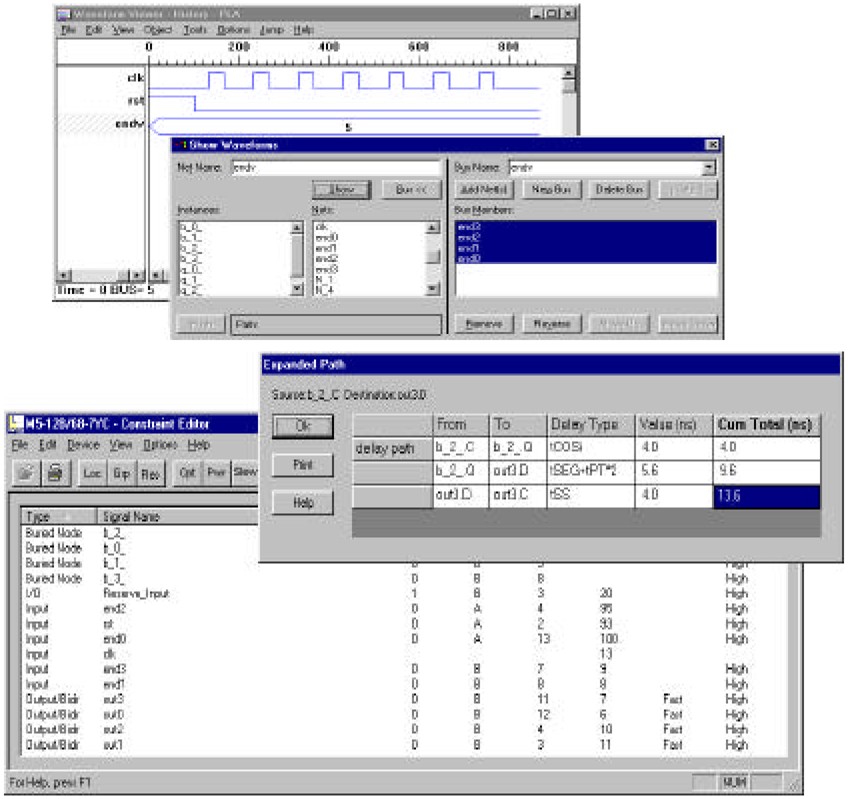
Before attempting this tutorial, you should complete the Schematic or ABEL-HDL Design Entry tutorial.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of the steps and tools necessary to implement and verify a Lattice programmable MACH design using ispDesignExpert.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.



Expanded Path

Source: b_2_C Destination: out3.D

| | From | To | Delay Type | Value (ns) | Cum Total (ns) |
|---|---|---|---|---|---|
| delay path | b_2_C | b_2_Q | tCOSi | 4.0 | 4.0 |
| | b_2_Q | out3.D | tSEG+tPT*2 | 5.6 | 9.6 |
| | out3.D | out3.C | tSS | 4.0 | 13.6 |

| Type | Signal Name | | | | | | |
|---|---|---|---|---|---|---|---|
| Buried Node | b_2_ | | | | | | |
| Buried Node | b_0_ | | | | | | |
| Buried Node | b_1_ | [illegible] | [illegible] | [illegible] | | | [illegible] |
| Buried Node | b_3_ | 0 | B | 8 | | | High |
| I/O | Reserve_Input | 1 | B | 3 | 20 | | High |
| Input | end2 | 0 | A | 4 | 95 | | High |
| Input | rst | 0 | A | 2 | 93 | | High |
| Input | end0 | 0 | A | 13 | 100 | | High |
| Input | clk | | | | 13 | | |
| Input | end3 | 0 | B | 7 | 9 | | High |
| Input | end1 | 0 | B | 8 | 8 | | High |
| Output/Bidir | out3 | 0 | B | 11 | 7 | Fast | High |
| Output/Bidir | out0 | 0 | B | 12 | 6 | Fast | High |
| Output/Bidir | out2 | 0 | B | 4 | 10 | Fast | High |
| Output/Bidir | out1 | 0 | B | 3 | 11 | Fast | High |

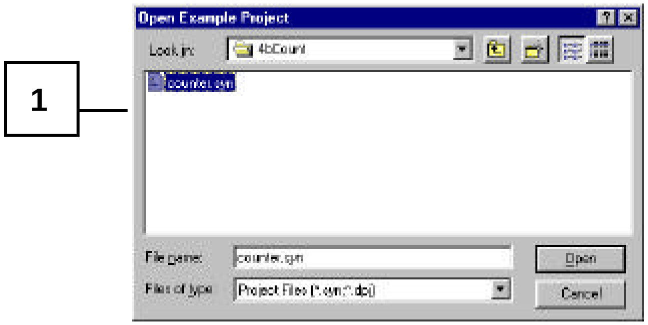
# Task 1 *Open the Project*

To continue with the design example, open the project for this tutorial.

*To open the tutorial project*:

1. In the Project Manager, choose **File** ⇒ **Open Example** to open the dialog.
2. Open the file `\Tutorial\Tutor4\4bCount\counter.dpj`.

   The 4-bit counter project opens in the Project Manager.



1

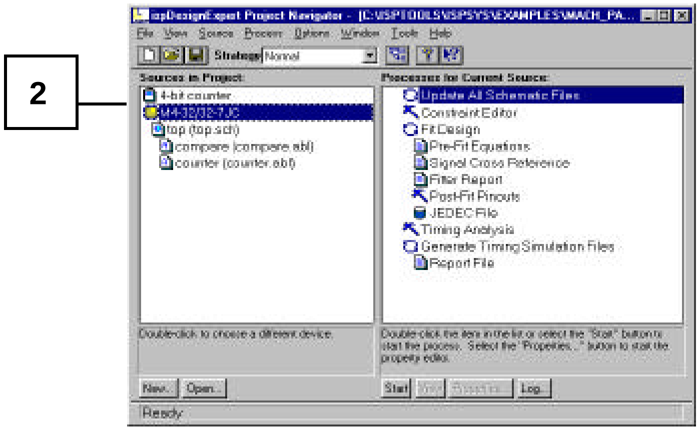
Open Example Project

Look in: 4bCount

counter.syn

File name: counter.syn

Files of type: Project Files (*.syn;*.dpj)



2

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

Strategy: Normal

Sources in Project:

- 4-bit counter
- M4-32/32-7JC
  - top (top.sch)
    - compare (compare.abl)
    - counter (counter.abl)

Processes for Current Source:

- Update All Schematic Files
- Constraint Editor
- Fit Design
  - Pre-Fit Equations
  - Signal Cross Reference
  - Fitter Report
  - Post-Fit Pinouts
  - JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
  - Report File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

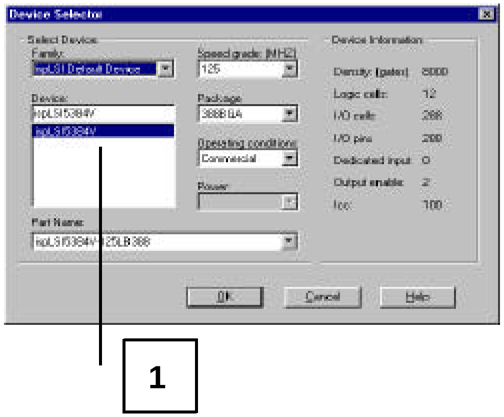
# Task 2 *Select a Device*

The Project Manager lets you target a design to a specific Lattice device at any time during the design process.

*To select a device:*

1. In the Sources window, double-click the device to open the Device Selector dialog. The dialog show the available device families and the devices in the selected family.
2. In the Device Selector dialog, select the **MACH 5** device family.
3. Select the **M5-128/68** device.
4. Accept the default settings and the click **OK**.
5. Click **Yes** to confirm that you wish to change device kits.

   When you change device families, the ispDesignExpert design environment reconfigures to facilitate designing with the selected device family.



Device Selector

Select Device

Family: ispLSI Default Device

Speed grade (MHz): 125

Device: ispLSI5384V

ispLSI5384V

Package: 388BGA

Operating conditions: Commercial

Power:

Part Name: ispLSI5384V-125LB388

Device Information

Density (gates): 8000

Logic cells: 12

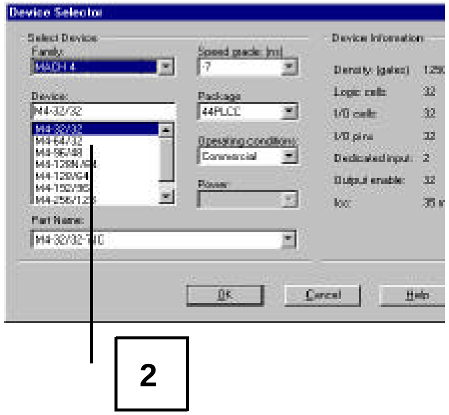
I/O cells: 288

I/O pins: 288

Dedicated input: 0

Output enable: 2

Icc: 100



Device Selector

Select Device

Family: MACH 4

Speed grade (ns): -7

Device: M4-32/32

M4-32/32
M4-64/32
M4-96/48
M4-128N/64
M4-128/64
M4-192/96
M4-256/128

Package: 44PLCC

Operating conditions: Commercial

Power:

Part Name: M4-32/32-7JC

Device Information

Density (gates): 1250

Logic cells: 32

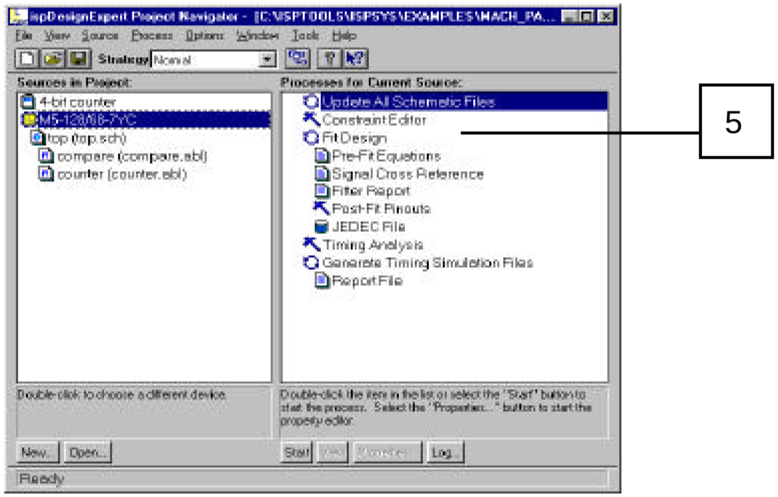
I/O cells: 32

I/O pins: 32

Dedicated input: 2

Output enable: 32

Icc: 35



ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

Strategy: Normal

Sources in Project:

- 4-bit counter
- M5-128/68-7YC
  - top (top.sch)
    - compare (compare.abl)
    - counter (counter.abl)

Processes for Current Source:

- Update All Schematic Files
- Constraint Editor
- Fit Design
  - Pre-Fit Equations
  - Signal Cross Reference
  - Fitter Report
  - Post-Fit Pinouts
  - JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
  - Report File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

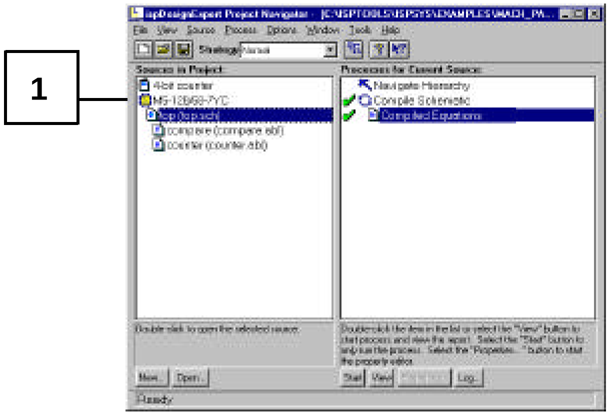
Ready

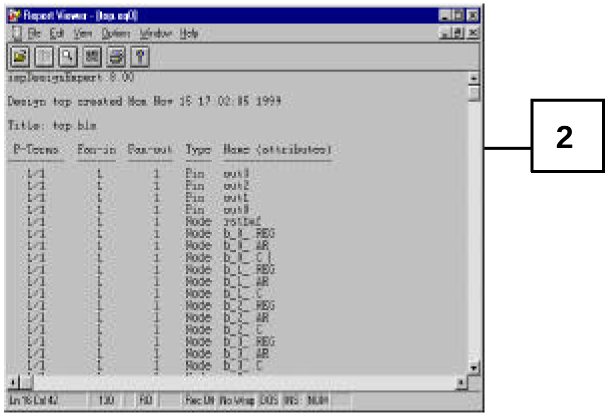
# Task 3 *Compile a Source File*

When you compile a design, you are changing your design entry format into Boolean equations, which serve as input to simulation and device implementation programs. The Project Manager processes each ABEL-HDL module or schematic file to obtain an intermediate file that can later be linked together before fitting the design into a Lattice device.

*To compile a source and automatically view the report*:

1. In the Sources window, select the `top.sch` source.
2. In the Processes window, double-click **Compiled Equations**. The ispDesignExpert software compiles the source file and automatically displays the resulting file in the Report Viewer. If an ABEL-HDL file contains syntax errors, the software displays the errors in a view window and an error indication appears in the Processes window.
3. Close the Report Viewer.




2
Report Viewer - [top.eq0]
File Edit View Options Window Help
Ln 16 Col 42 | 130 | RO | Rec Off No Wrap DOS INS NUM

```
ispDesignExpert 8.00

Design top created Mon Nov 15 17:02:05 1999

Title: top.bls

 P-Terms   Fan-in  Fan-out  Type  Name (attributes)
---------  ------  -------  ----  -----------------
   1/1        1       1     Pin   out3
   1/1        1       1     Pin   out2
   1/1        1       1     Pin   out1
   1/1        1       1     Pin   out0
   1/1        1       1     Node  rstbuf
   1/1        1       1     Node  b_0_.REG
   1/1        1       1     Node  b_0_.AR
   1/1        1       1     Node  b_0_.C
   1/1        1       1     Node  b_1_.REG
   1/1        1       1     Node  b_1_.AR
   1/1        1       1     Node  b_1_.C
   1/1        1       1     Node  b_2_.REG
   1/1        1       1     Node  b_2_.AR
   1/1        1       1     Node  b_2_.C
   1/1        1       1     Node  b_3_.REG
   1/1        1       1     Node  b_3_.AR
   1/1        1       1     Node  b_3_.C
```

# Task 4 *Simulate the Equations and View the Results*

Equation simulation uses design test vectors, that you supply, to simulate the design logic or equations independent of any device.

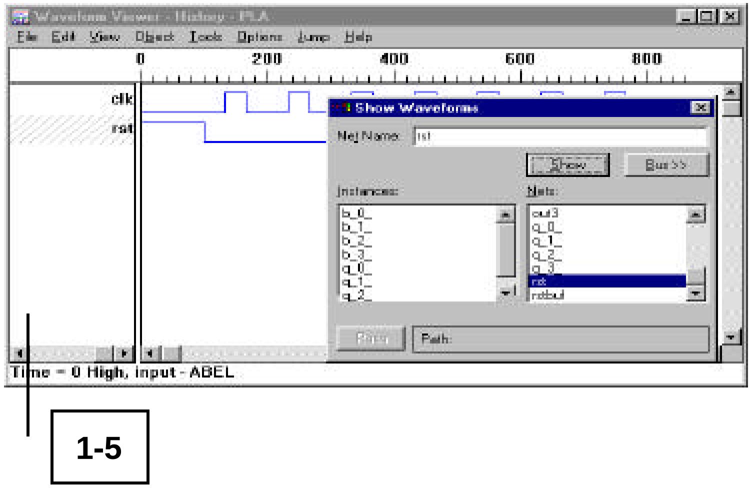
There are two ways to specify test vectors. The most common method is to put test vectors into the ABEL-HDL source file. The other way to specify test vectors is to create a "real" test vector file (`*filename*.abv`).

The advantages to placing test vectors in the ABV file instead of in the ABEL-HDL source is an improvement in processing time. By placing test vectors in the ABV file you will be able to change the test vectors and re-simulate without having to re-compile the logic. This can make a significant difference in large hierarchical designs.

In this next step, you will import an ABV source file into the project. Then you will run equation simulation and view the results using the Waveform Viewer.

*To simulate equations and view the results*:

1. Choose **Source** ⇒ **Import**, select `top.abv`, and then click **Open** to load the file into the project.
2. In the Sources window, select `top.abv` and then double-click **Equation Simulation Waveform** in the Processes window. The software runs equation simulation and opens the Waveform Viewer.
3. Choose **Edit** ⇒ **Show** to open the Show Waveforms dialog.

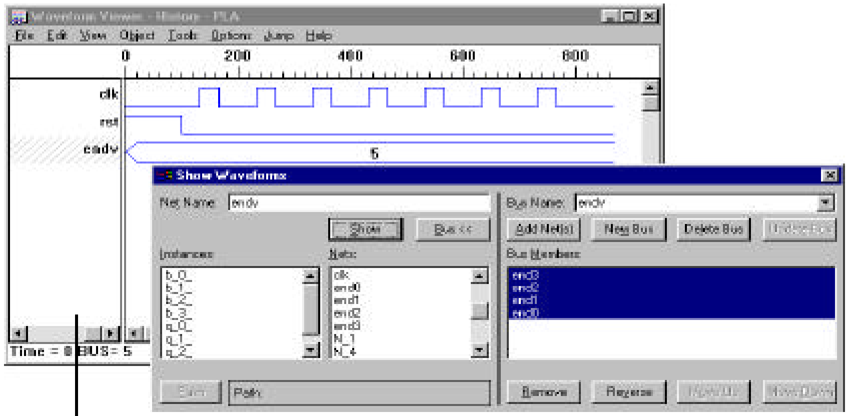


Net Name: rst

Time = 0 High, input - ABEL

# *Simulate the Equations and View the Results (continued)*

4. Under Nets, scroll down and select **clk**. Then click **Show**. The software adds the waveform to the viewer.
5. Scroll down more and select **rst**. Then click **Show**.
6. Now you will create a bus. Click **Bus** to expand the dialog.
7. In the Bus Name field, type endv.
8. Under Nets, select end0 to end3. Then click **Add Nets**.
9. Click **Reverse** to reverse the order.
10. Click **Save Bus**. Then click **Show** to add the bus to the viewer.
11. Exit the Waveform Viewer. When prompted to save the file, click **No**.



Net Name: endv

Bus Name: endv

Bus Members: end3, end2, end1, end0

Time = 0 BUS= 5

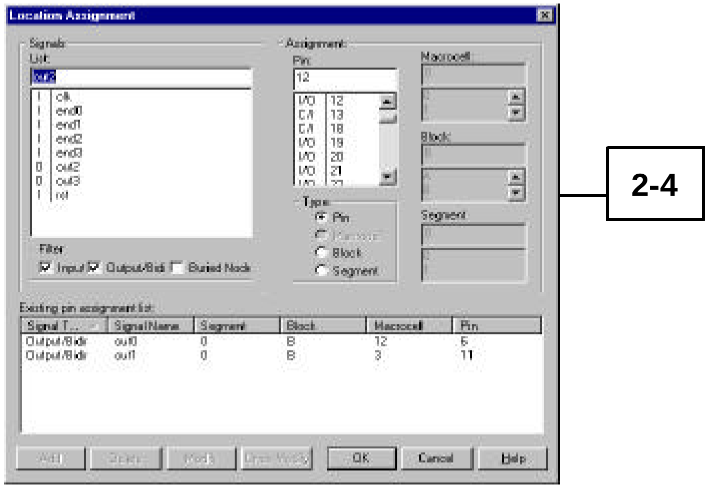
6-10

# Task 5 *Assign Some Constraints*

The Constraint Editor lets you specify pin and node assignments, group assignments, pin reservations, power level settings, output slew-rates and JEDEC file options. The editor reads the constraint file and displays the constraint settings in the main window. You can modify the constraint file using the function dialogs available from the toolbar

*To assign constraints to the design*:

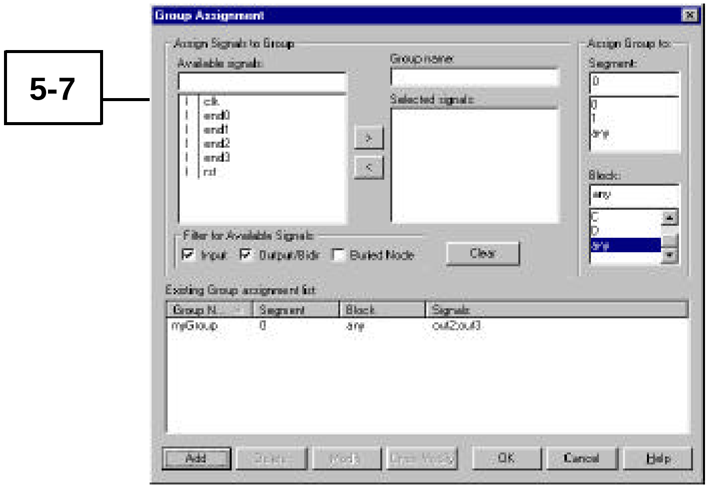
1. In the Sources window, select the target device. In the Processes window, double-click **Constraint Editor** to open it.
2. In this step, you will specify two pin assignments. On the toobar, click **Loc** to open the Location Assignment dialog.
3. Under Filter, select **Output/Bid**i. In the Signals List, select out0. Under Asignment select pin 6. Then click **Add**. The software adds the pin assignment to the assignment list.
4. Now, using the same procedure, assign out1 to pin 11, and then add it to the assignment list. Click **OK** to close the dialog.
5. Next, you will create a group and assign it to any block . On the toolbar, click the **Grp** button to open the Group Assignment dialog.
6. Under Filter, select **Output/Bidir**. In the Available Signals list, select out2 and out3. Then click the **right-arrow** button to add them to the Selected Signals list.



Existing pin assignment list:

| Signal T... | SignalName | Segment | Block | Macrocell | Pin |
|---|---|---|---|---|---|
| Output/Bidir | out0 | 0 | B | 12 | 6 |
| Output/Bidir | out1 | 0 | B | 3 | 11 |

2-4



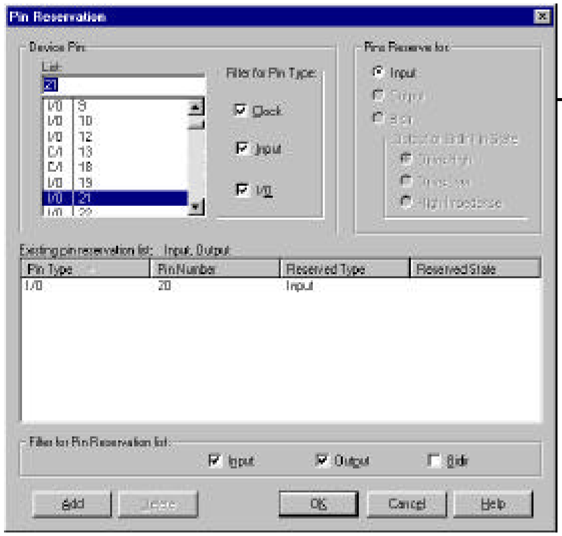
Existing Group assignment list:

| Group N... | Segment | Block | Signals |
|---|---|---|---|
| myGroup | 0 | any | out2,out3 |

5-7

# Assign Some Constraints (continued)

7. In the Group Name field, type myGroup. Under Assign Group To, select block Any, if it is not already selected. Then click **Add** to add the group to the assignment list. Click **OK** to close the dialog.
8. Finally, you will specify Pin Reservation constraints, which are “soft constraints.” That is, if the design fails to fit, the pin reservation constraints are ignored by the Fitter. On the toolbar, click the **Res** button to open the Pin Reservation dialog.
9. Select pin 20, select Output, and then click **Add**. Click **OK** to close the dialog.
10. Look at the assignments in the Constraint Editor, and then exit the editor.



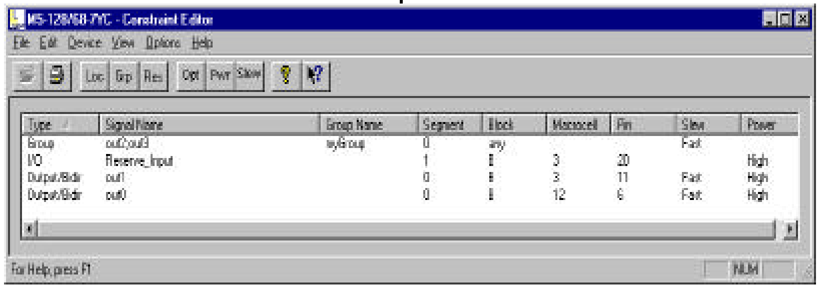
| | |
|---|---|
| I/O | 9 |
| I/O | 10 |
| I/O | 12 |
| C/I | 13 |
| C/I | 18 |
| I/O | 19 |
| I/O | 21 |
| I/O | 22 |

Existing pin reservation list: Input, Output

| Pin Type | Pin Number | Reserved Type | Reserved State |
|---|---|---|---|
| I/O | 20 | Input | |

8-9

10


M5-128/68-7YC - Constraint Editor
File Edit Device View Options Help
Loc Grp Res Opt Pwr Slew
For Help, press F1
NUM

| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|
| Group | out2,out3 | myGroup | 0 | any | | | Fast | |
| I/O | Reserve_Input | | 1 | B | 3 | 20 | | High |
| Output/Bidir | out1 | | 0 | B | 3 | 11 | Fast | High |
| Output/Bidir | out0 | | 0 | B | 12 | 6 | Fast | High |

# Task 6 *Set Fitter Optimization Options*

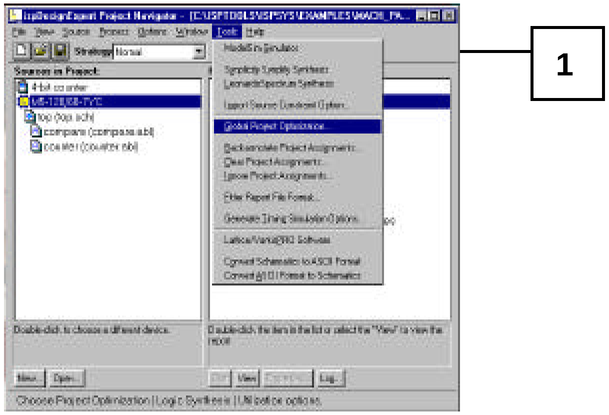
You set the optimization options for the Fitter using the Global Optimization dialog. The default Fitter options are set up to achieve the highest possible performance in the smallest possible device, for most designs. You can choose to maximize design flexibility by spreading out logic or exercise tighter control over the fitting process by packing the logic to achieve your design goals.

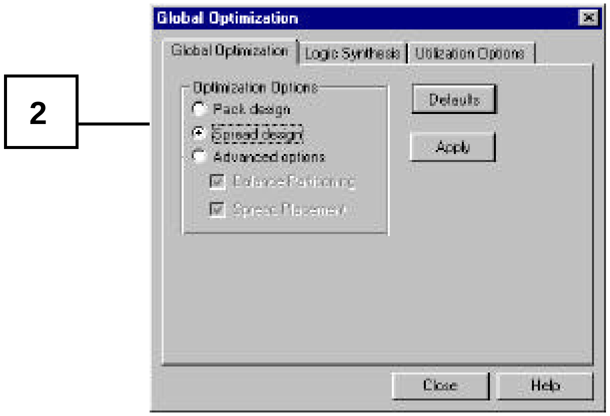
*To set the Fitter optimization options*:

1. In the Project Manager, choose **Tools** ⇒ **Global Project Optimization** to open the dialog.
2. On the Global Optimization tab, select **Spread Design**.

   The Spread Design option spreads the design throughout the device, allowing the design to be partitioned and placed in a spread out method. This placement method enhances the upgrade capability of the design by spreading the resources throughout the device. However, the disadvantage is that more resources may be used because the design is partitioned evenly through all the blocks.

   Later, you will choose Pack Design and see the difference in performance results.
3. Click **Apply**, and then click **Close** to close the dialog.


1
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Project Options Window Tools Help
Strategy Normal
Sources in Project:
4-bit counter
M5-128/68-7YC
top (top.sch)
compare (compare.abl)
counter (counter.abl)
ModelSim Simulator
Synplicity Synplify Synthesis
LeonardoSpectrum Synthesis
Import Source Constraint Option...
Global Project Optimization...
Backannotate Project Assignments...
Clear Project Assignments...
Ignore Project Assignments...
Fitter Report File Format...
Generate Timing Simulation Options...
Lattice/Vantis/ISO Software
Convert Schematic to ASCII Format
Convert ASCII Format to Schematic
Double-click to choose a different device.
Double-click the item in the list or select the "View" to view the report
New... Open...
View Log...
Choose Project Optimization | Logic Synthesis | Utilization options.



# Task 7 *Fit the Design*

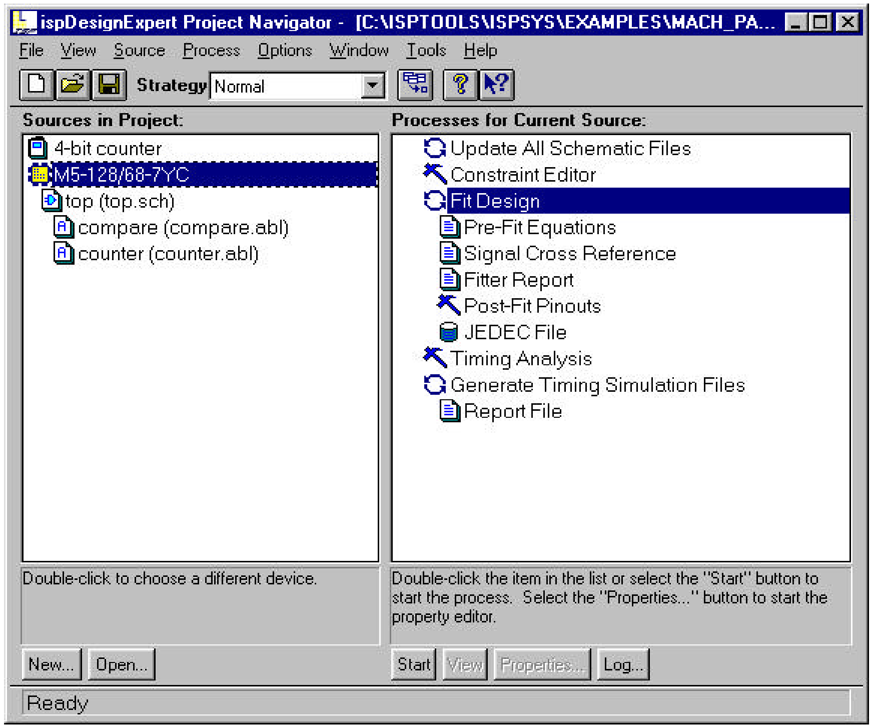
ispDesignExpert has a single user interface with all options preset to deliver the highest possible push-button performance. At the end of a successful fitter run, ispDesignExpert generates a JEDEC file, as well as a fitter report, so that you can see how ispDesignExpert has utilized and routed the part.

There are four phases to the fitting process. These are:

**Initialization** – When you start a new project, ispDesignExpert automatically copies a default constraint file from the ispDesignExpert directory into your project directory.

**Optimization** – Each clock signal is evaluated and classified as a global clock or a non-global clock. The Fitter attempts to place all global clock signals at global clock pins (check the log file for the status of all clock signals after optimization). The Fitter assigns all other clock signals to I/O pins and implements them as Product Term clocks, if the architecture supports Product Term clocks. Input pins and nodes that are defined but not referenced (not used by another equation) are discarded from the design during optimization (warning messages are generated).

**Partitioning** – After optimization, ispDesignExpert partitions the design into individual blocks of the specified MACH device. Partitioning is achieved by assigning logic to specific PAL blocks, based on several considerations.



Strategy: Normal

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

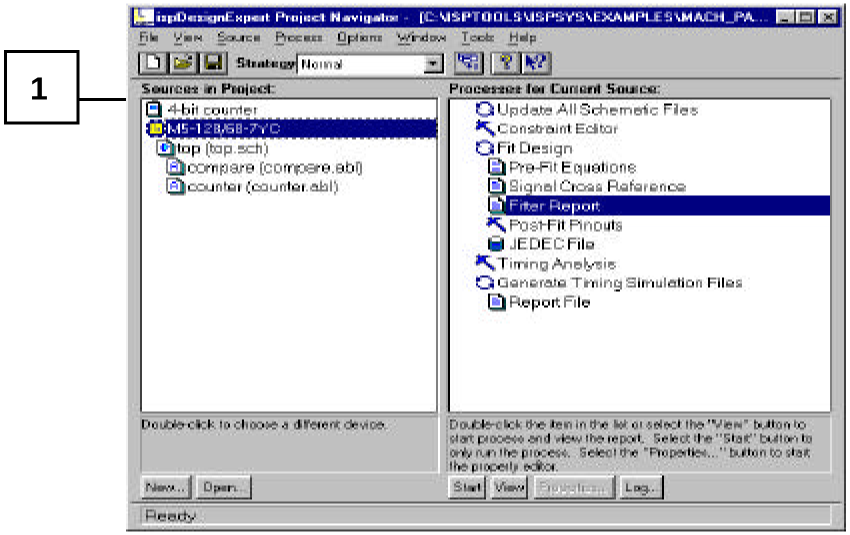
# Fit the Design (continued)

The Partitioner considers commonality of signals, macrocell requirements, Set/Reset requirements, product-term requirements, and other factors to determine which partition is most likely to succeed in fitting the design. Only partitions that are likely to succeed (according to the Partitioner's rules) are attempted.

**Placement and Routing** – In the placement phase of the fitting process, individual equations are assigned to physical resources. In the routing phase, the Fitter attempts to route input, output, and feedback signals to and from the physical resources assigned in the placement phase.

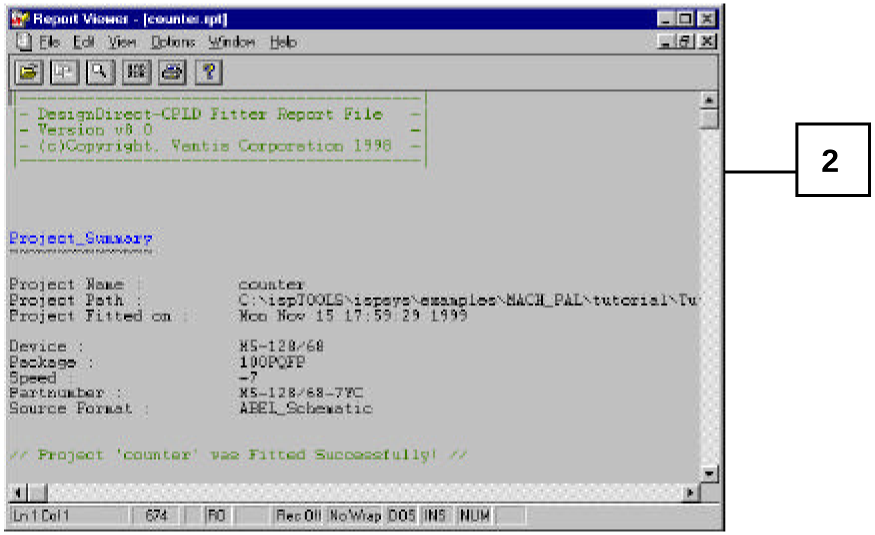
*To run the Fitter and view the Fitter report*:

1. In the Sources window, select the target device.
2. In the Processes window, double-click **Fitter Report**. This starts the Fitter and automatically opens the Fitter report in the Report Viewer.
3. Browse the Fitter report and then close the Report Viewer.



Double-click to choose a different device.

Double-click the item in the list or select the "View" button to start process and view the report. Select the "Start" button to only run the process. Select the "Properties..." button to start the property editor.


Report Viewer - [counter.rpt]
File Edit View Options Window Help
2
Ln 1 Col 1 674 RO Rec Off No Wrap DOS INS NUM

```
------------------------------------------------
- DesignDirect-CPLD Fitter Report File         -
- Version v8.0                                 -
- (c)Copyright, Vantis Corporation 1998        -
------------------------------------------------



Project_Summary
~~~~~~~~~~~~~~~

Project Name :          counter
Project Path :          C:\ispTOOLS\ispsys\examples\MACH_PAL\tutorial\Tu
Project Fitted on :     Mon Nov 15 17:59:29 1999

Device :                M5-128/68
Package :               100PQFP
Speed :                 -7
Partnumber :            M5-128/68-7YC
Source Format :         ABEL_Schematic


// Project 'counter' was Fitted Successfully! //
```

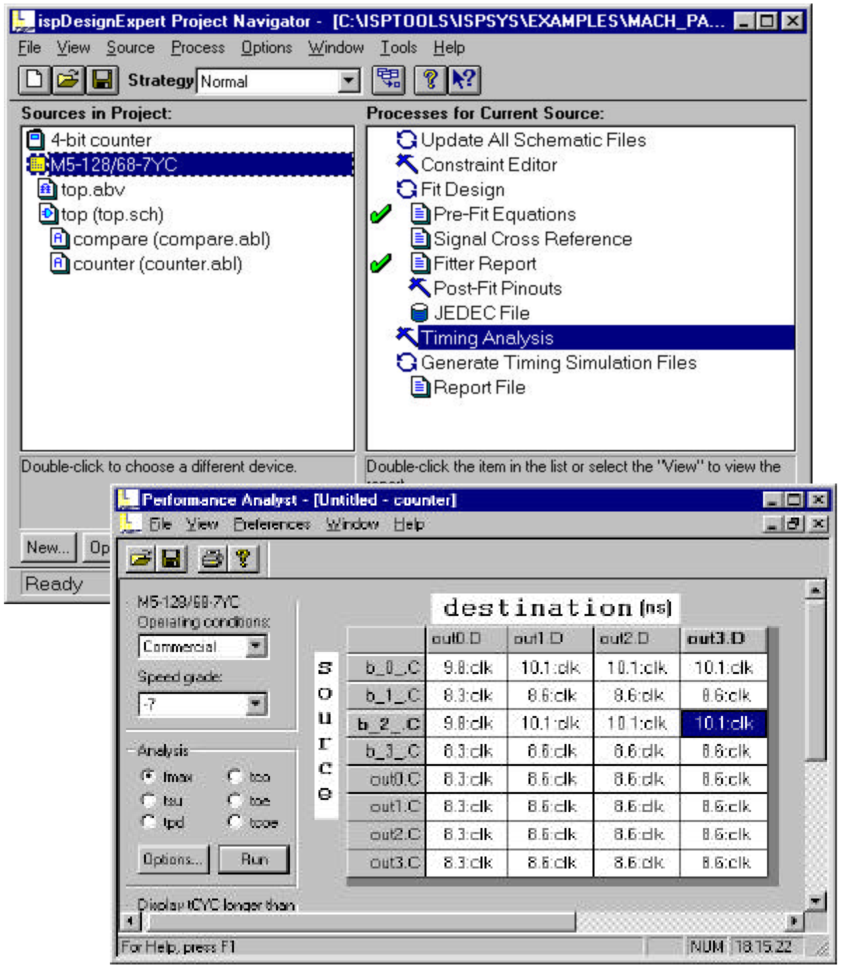
# Task 8 *Analyze the Timing Results*

The Performance Analyst analyzes the performance of your design after it had been optimized and implemented by the Fitter.

The Timing Analyzer traces each logical path in the design and calculates the path delays using the timing model and worst case values supplied in the device data sheet.

The Performance Analyst performs six distinct analysis types: fMAX, tSU, tPD, tCO, tOE and tCOE. Timing filters, source and destination filters and path filters can be used to independently fine-tune each analysis.

The timing analysis results are displayed in a graphical spreadsheet with sources displayed on one axis and destinations displayed on the other. The worst case delay value is displayed in the spreadsheet cell if there is a path between the source and destination. Path details are obtained by placing the cursor on the cell and double-clicking the left-hand mouse button, allowing the user to easily identify performance bottlenecks.


File View Source Process Options Window Tools Help
File View Preferences Window Help
New... Op
Options... Run

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...

Strategy: Normal

Sources in Project:

- 4-bit counter
- M5-128/68-7YC
- top.abv
- top (top.sch)
- compare (compare.abl)
- counter (counter.abl)

Double-click to choose a different device.

Processes for Current Source:

- Update All Schematic Files
- Constraint Editor
- Fit Design
- ✓ Pre-Fit Equations
- Signal Cross Reference
- ✓ Fitter Report
- Post-Fit Pinouts
- JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
- Report File

Double-click the item in the list or select the "View" to view the

Ready

Performance Analyst - [Untitled - counter]

M5-128/68-7YC

Operating conditions: Commercial

Speed grade: -7

Analysis: ● fmax ○ tco ○ tsu ○ toe ○ tpd ○ tcoe

Display tCYC longer than

destination (ns)

| source | out0.D | out1.D | out2.D | out3.D |
|---|---|---|---|---|
| b_0_C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| b_1_C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |
| b_2_C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| b_3_C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |
| out0.C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |
| out1.C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |
| out2.C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |
| out3.C | 8.3:clk | 8.6:clk | 8.6:clk | 8.6:clk |

For Help, press F1 NUM 18:15:22

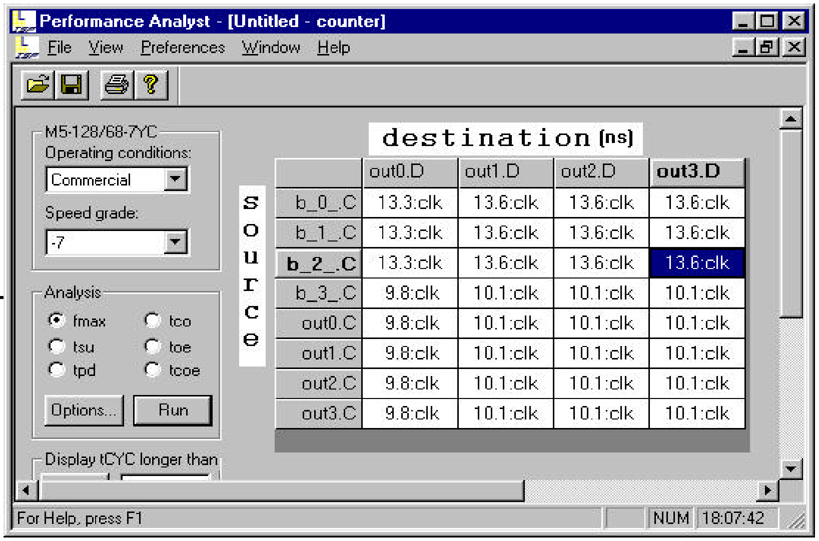
# Analyze the Timing Results (continued)

*To run the Performance Analyst and view the results*:

1. In the Sources window, select the target device. Then in the Processes window, double-click **Timing Analysis**.
2. Select **fmax** and then click **Run**. The overall timing results appear in the spreadsheet.

***Note****: Your numbers may differ from those shown in this example.*

3. Double-click inside the highlighted cell to open the Extended Path dialog and analyze the timing results of an individual path.
4. Notice the timing results. The longest delay was 13.6 ns.
5. (*Optional*) Print both output reports. You will use this in the next task to comapre timing results.
6. Close both spreadsheet dialogs without saving.



1-2

Performance Analyst - [Untitled - counter]
File View Preferences Window Help
Options...
Run
For Help, press F1
NUM
18:07:42

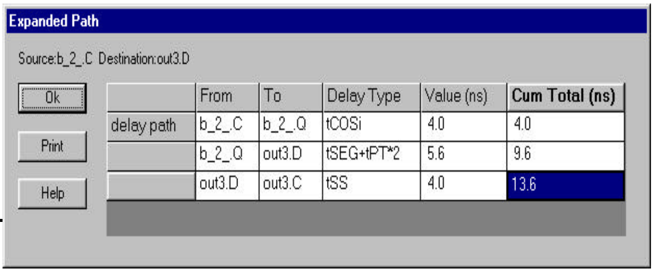
M5-128/68-7YC
Operating conditions: Commercial
Speed grade: -7

Analysis
● fmax ○ tco
○ tsu ○ toe
○ tpd ○ tcoe

Display tCYC longer than

destination (ns)

| source | out0.D | out1.D | out2.D | out3.D |
|---|---|---|---|---|
| b_0_.C | 13.3:clk | 13.6:clk | 13.6:clk | 13.6:clk |
| b_1_.C | 13.3:clk | 13.6:clk | 13.6:clk | 13.6:clk |
| b_2_.C | 13.3:clk | 13.6:clk | 13.6:clk | 13.6:clk |
| b_3_.C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| out0.C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| out1.C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| out2.C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |
| out3.C | 9.8:clk | 10.1:clk | 10.1:clk | 10.1:clk |



3

Source:b_2_.C Destination:out3.D

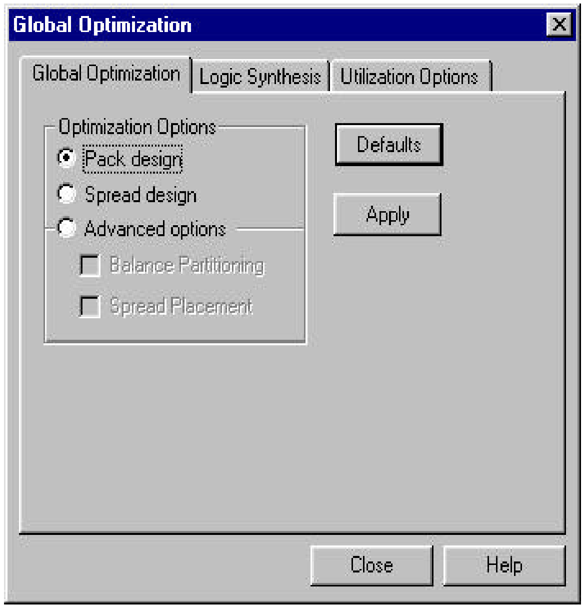
| | From | To | Delay Type | Value (ns) | Cum Total (ns) |
|---|---|---|---|---|---|
| delay path | b_2_.C | b_2_.Q | tCOSi | 4.0 | 4.0 |
| | b_2_.Q | out3.D | tSEG+tPT*2 | 5.6 | 9.6 |
| | out3.D | out3.C | tSS | 4.0 | 13.6 |

# Task 9 *Change the Fitter Options and Reanalyze the Timing*

In a previous task you learned how to set Fitter optimization options using the Global Optimization dialog. If you recall, the default Fitter option is Spread Design. This option allows you to achieve the highest possible performance, while leaving room for any additional functionality that you may want to add in the future.

Now you will choose another option, Pack Design. This option lets you pack as much logic into the device as possible. Pack Design allows you to achieve the highest possible performance in the smallest possible device, for most designs. Each block may be completely filled, leaving less room for any design changes or logic additions.

After you change the Fitter optimization option, you will re-run timing analysis and see the performance differences with the new setting.



● Pack design
○ Spread design
○ Advanced options
□ Balance Partitioning
□ Spread Placement

# Change the Fitter Options (continued)

*To change the Fitter optimization options and re-run timing analysis*:

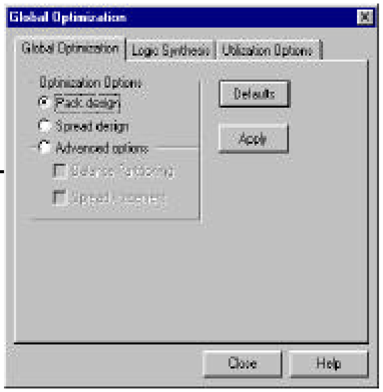
1. In the Project Manager, choose **Tools** ⇒ **Global Project Optimization** to open the dialog.
2. On the Global Optimization tab, select **Pack Design** and then click **Apply**. Click **Close** to close the dialog.

***Note****: You must click* ***Apply*** *to register the changes in the dialog.*

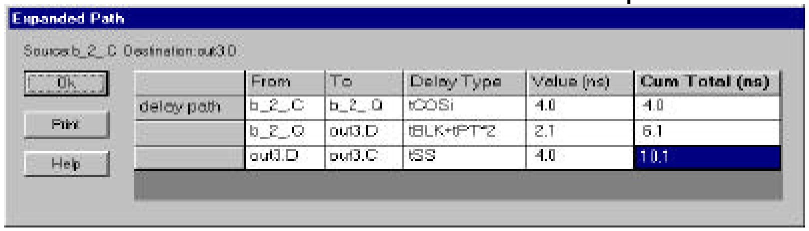
3. In the Sources window, select the target device. Then in the Processes window, double-click **Timing Analysis** to open the Peformance Analyst. Notice this runs the Fitter again.
4. Select **fmax** and click **Run**. The overall timing results appear in the spreadsheet. Notice the the performance has improved. Now the longest delay is 10.1 ns.

***Note****: Your numbers may differ from those in this example. What is important to notice is the “relative” improvement in performance compared to the previous run.*

5. Double-click inside the highlighted cell to open the Extended Path dialog and analyze the timing results of an individual path. Again, notice that the cumulative total has improved.
6. Close both spreadsheet dialogs without saving.



Optimization Options
● Pack design
○ Spread design
○ Advanced options
☐ Balance Partitioning
☐ Spread placement



Source:b_2_C Destination:out3.D

| | From | To | Delay Type | Value (ns) | Cum Total (ns) |
|---|---|---|---|---|---|
| delay path | b_2_C | b_2_Q | tCOSi | 4.0 | 4.0 |
| | b_2_Q | out3.D | tBLK+tPT*2 | 2.1 | 6.1 |
| | out3.D | out3.C | tSS | 4.0 | 10.1 |

# Task 10 *Backannotate Project Assignments*

You can backannotate assignments from the Fitter output to the project constraint file using the Backannotation tab on the Constraints Options dialog. This feature lets you retain the assignments made by the Fitter so they can be used in the future.

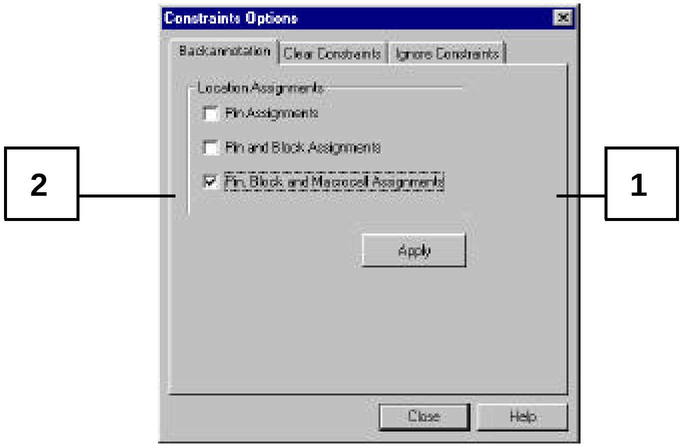
You can only backannotate project assignments after the "Fit Design" process has been successfully completed. An error message appears if ispDesignExpert detects that this process did not complete successfully.

*To backannotate assignments*:

1. In the Project Manager, choose **Tools** ⇒ **Backannotate Project Assignments** to open the Constraints Options dialog.
2. Select **Pin, Block, and Macrocell Assignments**, and then click **Apply**.
3. Click **Yes** to continue, and then click **Close**. Notice that the green check mark next to Timing Analysis is removed, indicating that timing constraints have changed and that the design should be processed again.
4. Now open the Constraint Editor and view the file contents. In the Sources window, select the device. In the Processes window, double-click **Constraint Editor** to open it.

   The picture on the right [**4**] shows the smaller file containing the constraints set earlier in Task 5. The larger file on top contains the constraints that have been backannotated.

   Notice that there are many more constraints now than there previously were. Also notice that the constraints you specified in Task 5 are still retained. For example, signal out0 is assigned to pin 6.


Constraints Options

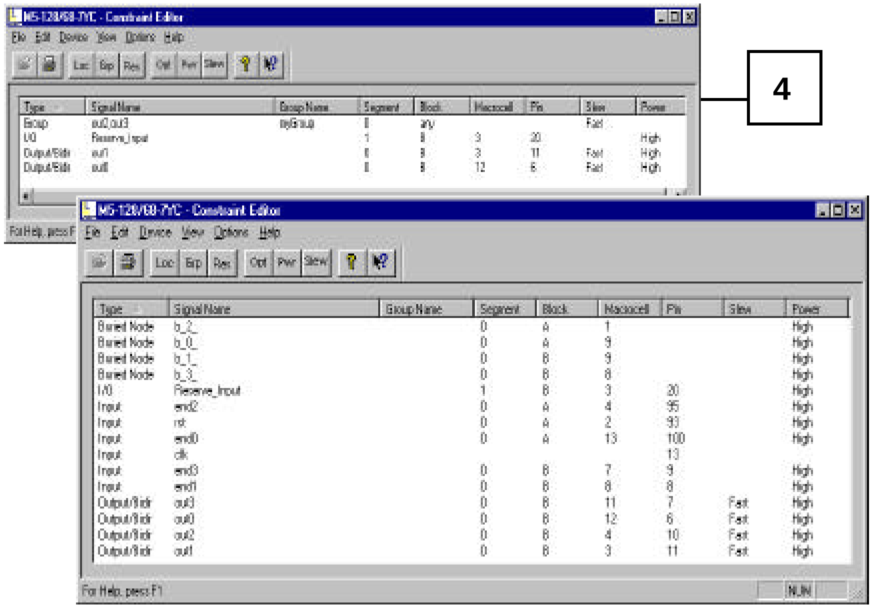
Backannotation | Clear Constraints | Ignore Constraints

Location Assignments

☐ Pin Assignments

☐ Pin and Block Assignments

☑ Pin, Block and Macrocell Assignments


M5-128/68-7YC - Constraint Editor

| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|
| Group | out2,out3 | myGroup | 0 | any |  |  | Fast |  |
| I/O | Reserve_input |  | 1 | B | 3 | 20 |  | High |
| Output/Bidir | out1 |  | 0 | B | 3 | 11 | Fast | High |
| Output/Bidir | out0 |  | 0 | B | 12 | 6 | Fast | High |

M5-128/68-7YC - Constraint Editor

| Type | Signal Name | Group Name | Segment | Block | Macrocell | Pin | Slew | Power |
|---|---|---|---|---|---|---|---|---|
| Buried Node | b_2_ |  | 0 | A | 1 |  |  | High |
| Buried Node | b_0_ |  | 0 | A | 9 |  |  | High |
| Buried Node | b_1_ |  | 0 | B | 9 |  |  | High |
| Buried Node | b_3_ |  | 0 | B | 8 |  |  | High |
| I/O | Reserve_Input |  | 1 | B | 3 | 20 |  | High |
| Input | end2 |  | 0 | A | 4 | 95 |  | High |
| Input | rst |  | 0 | A | 2 | 93 |  | High |
| Input | end0 |  | 0 | A | 13 | 100 |  | High |
| Input | clk |  |  |  |  | 13 |  |  |
| Input | end3 |  | 0 | B | 7 | 9 |  | High |
| Input | end1 |  | 0 | B | 8 | 8 |  | High |
| Output/Bidir | out3 |  | 0 | B | 11 | 7 | Fast | High |
| Output/Bidir | out0 |  | 0 | B | 12 | 6 | Fast | High |
| Output/Bidir | out2 |  | 0 | B | 4 | 10 | Fast | High |
| Output/Bidir | out1 |  | 0 | B | 3 | 11 | Fast | High |

For Help, press F1

# Congratulations!

You have completed the Design Implementation and Verification tutorial. In this tutorial you have learned how to:

- choose a device family and select a specific device.
- compile a source file, changing your design entry format into Boolean equations.
- import a test vector file into the project, and then run equation simulation and view the results using the Waveform Viewer.
- use the Constraint Editor to specify pin and node assignments, group assignments, pin reservations, power level settings, output slew-rates and JEDEC file options for the Fitter.
- set optimization options for the Fitter using the Global Optimization dialog.
- run the Fitter and open the Fitter report.
- use the Performance Analyst to analyze the timing results.
- change the Fitter optimization options and re-analyze the timing results.
- backannotate the project assignments and view them using the Constraint Editor.

This tutorial presents the basic operation of a GAL design, focusing on the tasks and design tools needed to implement and verify a GAL design.

## Prerequisites

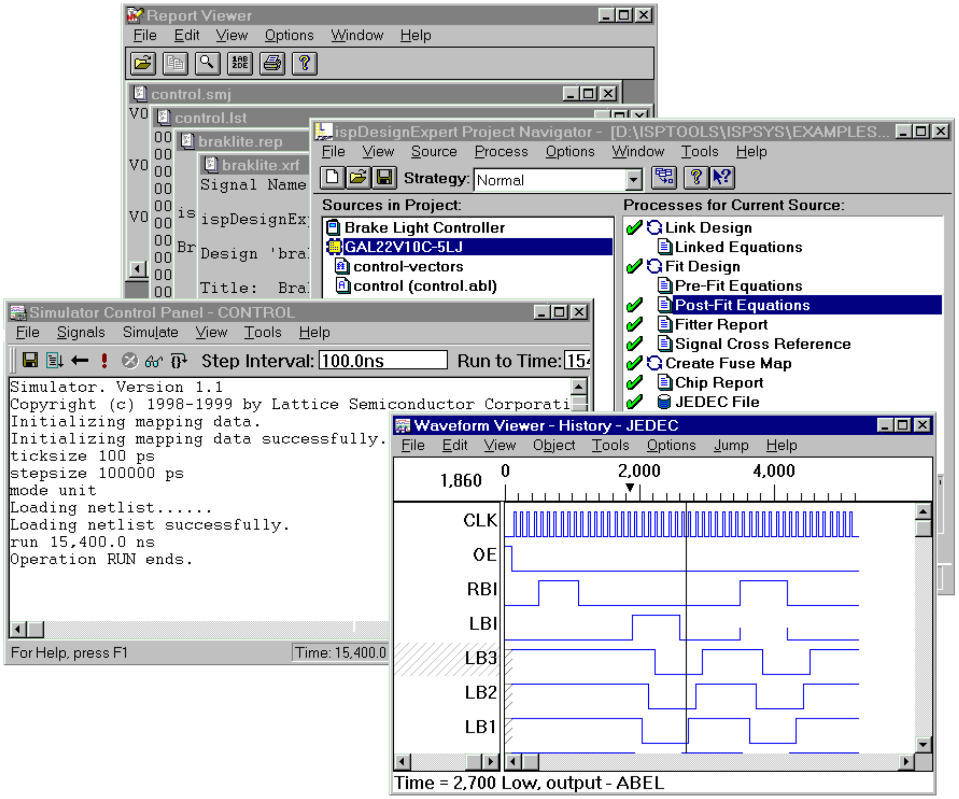
Before attempting this tutorial, you should complete the Schematic and ABEL-HDL Design Entry tutorial.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of steps and tools necessary to implement and verify a GAL design using the ispDesignExpert software.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.



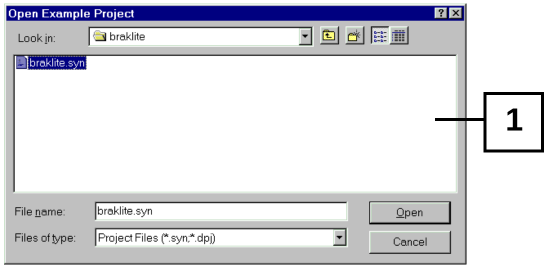
```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporati
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 15,400.0 ns
Operation RUN ends.
```

## Task 1 *Open a Project*

To continue with this tutorial, open an example project.

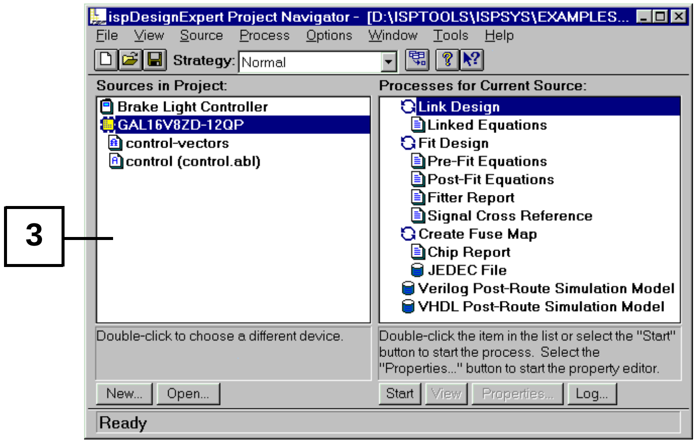
*To open the example project*:

1. Choose **File** ⇒ **Open Example** and select `\ispLSI_GAL\gal\brakelite\braklite.syn`.
2. Click **Open**.
3. The Brake Light Controller project is opened in the Project Navigator.



File name: braklite.syn

Files of type: Project Files (*.syn;*.dpj)


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLES...
File View Source Process Options Window Tools Help
Strategy:
Sources in Project:
Processes for Current Source:
New...
Open...
Start
View
Properties...
Log...
3

Strategy: Normal

Sources in Project:
- Brake Light Controller
- GAL16V8ZD-12QP
- control-vectors
- control (control.abl)

Processes for Current Source:
- Link Design
- Linked Equations
- Fit Design
- Pre-Fit Equations
- Post-Fit Equations
- Fitter Report
- Signal Cross Reference
- Create Fuse Map
- Chip Report
- JEDEC File
- Verilog Post-Route Simulation Model
- VHDL Post-Route Simulation Model

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

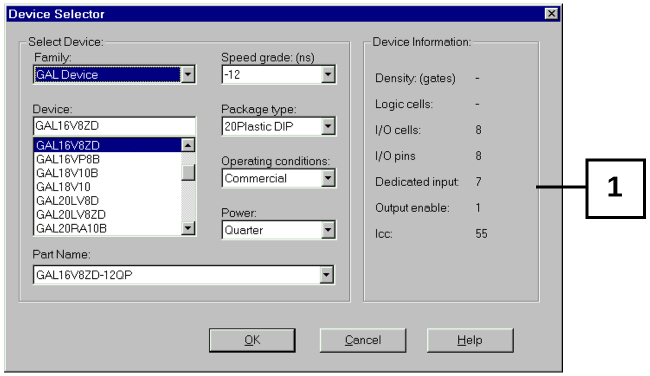
# Task 2 *Change your Device*

The Project Navigator lets you target your design to a specific device at any time during the design process. We have opened an example project with a GAL16V8ZD-12QP device. In this task, you will change to select another desired GAL device for your design.

*To change a device:*

1. In the Sources window, double click the Device icon. The Device Selector dialog box opens. The dialog box shows the available device families and the devices in the selected family.
2. In the Device Selector dialog box, select GAL device family. Select GAL22V10C-5LJ from the Part Name field. Accept the default settings and then click **OK**.
3. The Confirm Changes dialog box appears prompting you to confirm your device change. Click **Yes** to confirm that you wish to change the device. When you change devices, the ispDesignExpert software design environment reconfigures to facilitate designing with the selected device.

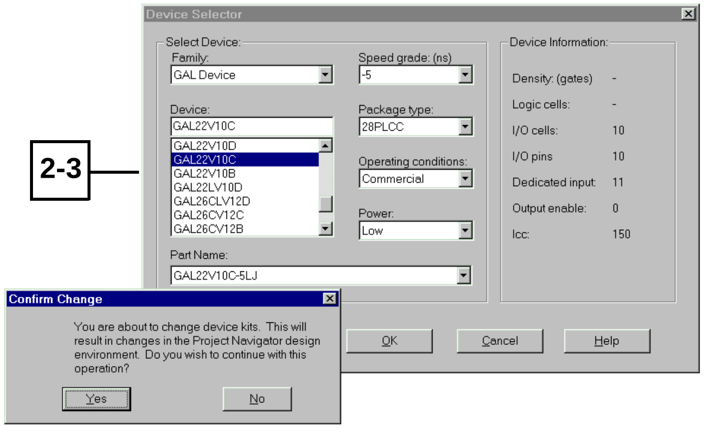
***Note**: Depending on the device you choose, the Confirm Changes dialog box does not appear for all the devices.*



Select Device:
Family: GAL Device
Speed grade: (ns) -12
Device: GAL16V8ZD
GAL16V8ZD
GAL16VP8B
GAL18V10B
GAL18V10
GAL20LV8D
GAL20LV8ZD
GAL20RA10B
Package type: 20Plastic DIP
Operating conditions: Commercial
Power: Quarter
Part Name: GAL16V8ZD-12QP

Device Information:

| | |
|---|---|
| Density: (gates) | - |
| Logic cells: | - |
| I/O cells: | 8 |
| I/O pins | 8 |
| Dedicated input: | 7 |
| Output enable: | 1 |
| Icc: | 55 |



Select Device:
Family: GAL Device
Speed grade: (ns) -5
Device: GAL22V10C
GAL22V10D
GAL22V10C
GAL22V10B
GAL22LV10D
GAL26CLV12D
GAL26CV12C
GAL26CV12B
Package type: 28PLCC
Operating conditions: Commercial
Power: Low
Part Name: GAL22V10C-5LJ

Device Information:

| | |
|---|---|
| Density: (gates) | - |
| Logic cells: | - |
| I/O cells: | 10 |
| I/O pins | 10 |
| Dedicated input: | 11 |
| Output enable: | 0 |
| Icc: | 150 |

Confirm Change

You are about to change device kits. This will result in changes in the Project Navigator design environment. Do you wish to continue with this operation?

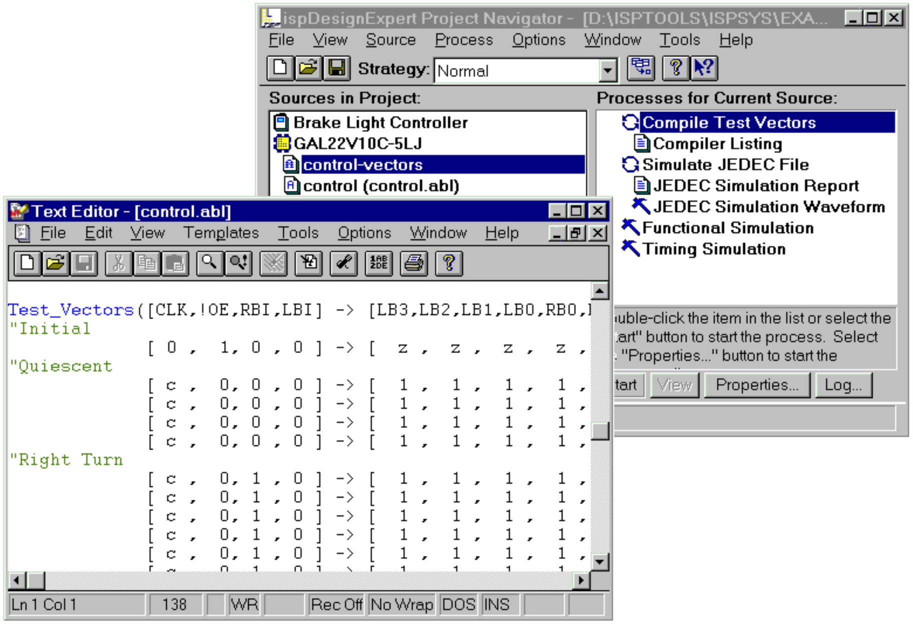
# Task 3 *Run Functional Simulation*

Functional Simulation, pre-route design verification, often occurs before the design has been fitted and routed. It helps you find logical or coding error in early design cycle. Functional Simulation uses test vectors to simulate the design logic or equations, independent of any device. The more comprehensive and detailed your test vectors are, the more useful your simulation results will be.

The Lattice Logic Simulator applies the inputs from the test vectors to the simulated circuit and compares the simulated output with the output specified in the test vectors. If there is any difference, an error is indicated.

Test vectors can be specified in two ways. The most commonly used is to put test vectors into an ABEL-HDL source. The other way is to create a “real” test vector file (*`design`*`.abv`). The advantage of placing test vectors in an ABV file is it can save more time in the simulation process. Once you place test vectors in the ABV file, you will be able to change the test vectors and resimulate without having to recompile the logic. This can make a significant difference in large hierarchical designs.

In this sample project, we have specified the test vectors in the ABEL-HDL source.


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXA...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Brake Light Controller
GAL22V10C-5LJ
control-vectors
control (control.abl)
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Simulate JEDEC File
JEDEC Simulation Report
JEDEC Simulation Waveform
Functional Simulation
Timing Simulation
uble-click the item in the list or select the
art" button to start the process. Select
"Properties..." button to start the
tart
View
Properties...
Log...
Text Editor - [control.abl]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
138
WR
Rec Off
No Wrap
DOS
INS

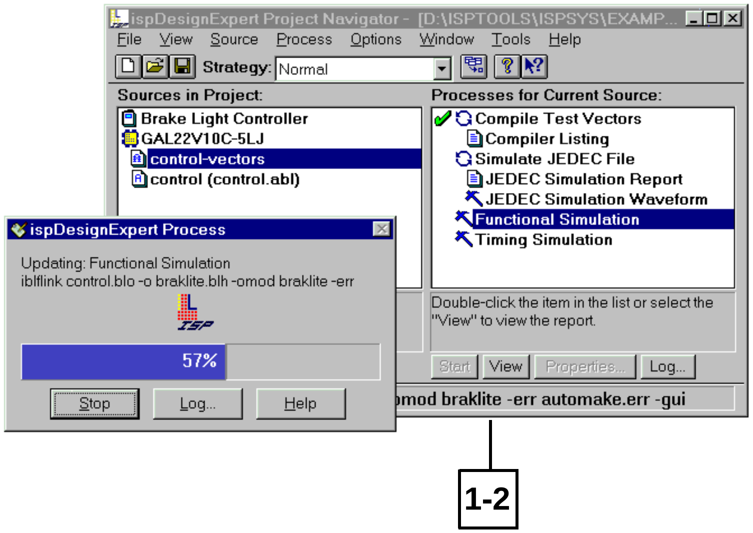
```
Test_Vectors([CLK,!OE,RBI,LBI] -> [LB3,LB2,LB1,LB0,RB0,]
"Initial
             [ 0 ,  1, 0 , 0 ] -> [  z ,  z ,  z ,  z ,
"Quiescent
             [ c ,  0, 0 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 0 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 0 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 0 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
"Right Turn
             [ c ,  0, 1 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 1 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 1 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 1 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
             [ c ,  0, 1 , 0 ] -> [  1 ,  1 ,  1 ,  1 ,
```

# Run Functional Simulation (Continued)

*To run Functional Simulation:*

1. Select the test vector icon from the Sources window of the Project Navigator. Double click the associated Functional Simulation process or click the **View** button at the bottom of the Project Navigator to launch Simulator Control Panel. At this moment, the Simulator starts to get functional netlist information. Because the netlist files have been generated before logic synthesis, partitioning, or fitting is performed, you will be able to find logical or coding errors at an earlier period of the whole design cycle.
2. The ispDesignExpert Process dialog box appears momentarily. When this process is completed successfully, the Simulator Control Panel is launched.
3. In the Simulator Control Panel window, click the **Run** icon from the toolbar or choose **Simulate** ⇒ **Run** to start the simulation.

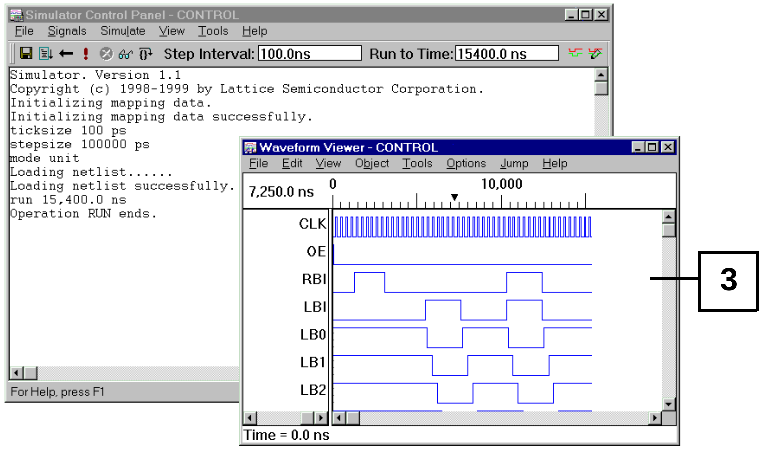
***Note**: Keep the **View** ⇒ **Show Waveforms** menu item checked in the Simulator Control Panel so that the Waveform Viewer will automatically be opened with the waveforms of the simulated signals.*



Double-click the item in the list or select the "View" to view the report.

Updating: Functional Simulation
iblflink control.blo -o braklite.blh -omod braklite -err

...mod braklite -err automake.err -gui

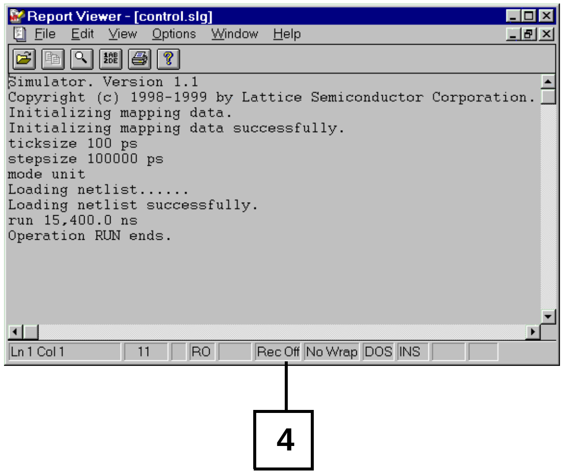

Simulator Control Panel - CONTROL
File Signals Simulate View Tools Help
Step Interval: 100.0ns
Run to Time: 15400.0 ns
For Help, press F1
Waveform Viewer - CONTROL
File Edit View Object Tools Options Jump Help
7,250.0 ns
0
10,000
CLK
OE
RBI
LBI
LB0
LB1
LB2
Time = 0.0 ns
3

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 15,400.0 ns
Operation RUN ends.
```

# Run Functional Simulation (Continued)

4. When the simulation runs to an end, you can compare the Functional Simulation results with the expected values specified in the test vectors. If there is any difference between the simulation results and the specified values such as the stimulation time, signal name, expected values, or actual value, messages will be printed in the Simulator Control Panel window. Or you can view the messages in the LOG file by choosing **View ⇒ Simulator Log.**

Refer to the ***Design Verification Tools User Manual*** for more information on simulation.



```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 15,400.0 ns
Operation RUN ends.
```

# Task 4 *Fit Design*

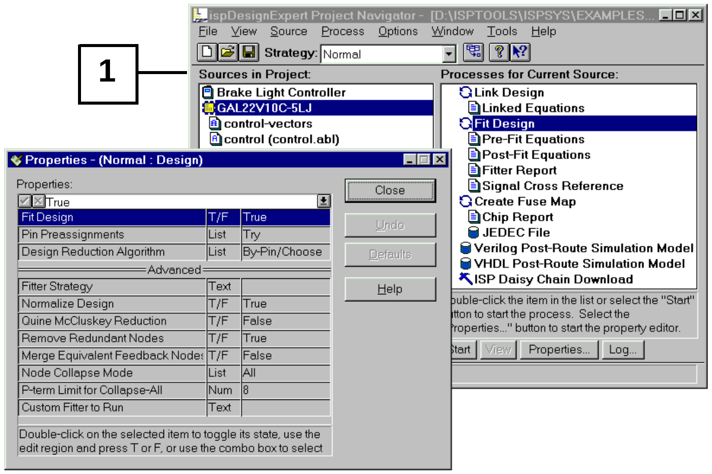
Now you can fit your design to the target device. Use the Fit Design process, you can run the ispExpert Compiler to automatically assign the pins and nodes of your design to physical pins and nodes in the device you have chosen. Several fit strategies can be selected in the Properties dialog box. You can view the Fitter Report of your design after running the Fit Design process.

*To fit your design and view the report:*

1. Select the device icon in the Sources window. In the Processes window, select the Fit Design process. (If you need to change properties associated with this process, click the **Properties** button at the bottom of the Project Navigator or choose **Process** ⇒ **Properties** to open the Properties dialog box. Change the options of the properties. Close the Properties dialog box.) Double click the Fit Design process or click the **Start** button. The ispDesignExpert software starts the fitter process.
2. When the process is finished, double click the Fitter Report process in the Processes window or click the **View** button at the bottom of the Project Navigator to display the Fitter Report (`.fit`) in the Report Viewer. If there is any syntax error in the compilation procedure, the software displays errors in the report and an error indication (red X) appears beside the Fit Design process in the Processes window.
3. Close the Report Viewer.

***Note**: If the target device is among the GAL6001B, GAL6002B, or GAL20XV10B device families, no Fit Design process is available in the Processes window.*

1



uble-click the item in the list or select the "Start" tton to start the process. Select the roperties..." button to start the property editor.

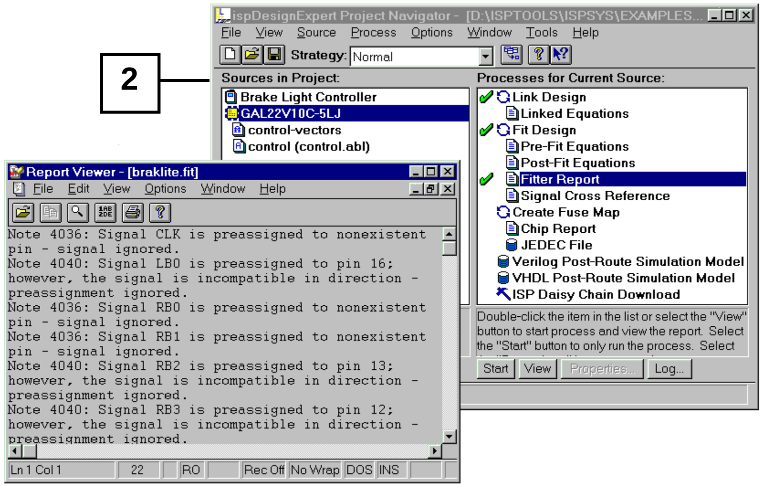
Properties:

☑ ☒ True

| | | |
|---|---|---|
| Fit Design | T/F | True |
| Pin Preassignments | List | Try |
| Design Reduction Algorithm | List | By-Pin/Choose |
| Advanced | | |
| Fitter Strategy | Text | |
| Normalize Design | T/F | True |
| Quine McCluskey Reduction | T/F | False |
| Remove Redundant Nodes | T/F | True |
| Merge Equivalent Feedback Nodes | T/F | False |
| Node Collapse Mode | List | All |
| P-term Limit for Collapse-All | Num | 8 |
| Custom Fitter to Run | Text | |

Double-click on the selected item to toggle its state, use the edit region and press T or F, or use the combo box to select

2


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLES...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Brake Light Controller
GAL22V10C-5LJ
control-vectors
control (control.abl)
Processes for Current Source:
✓ Link Design
Linked Equations
✓ Fit Design
Pre-Fit Equations
Post-Fit Equations
✓ Fitter Report
Signal Cross Reference
Create Fuse Map
Chip Report
JEDEC File
Verilog Post-Route Simulation Model
VHDL Post-Route Simulation Model
ISP Daisy Chain Download
Start View Properties... Log...
Report Viewer - [braklite.fit]
File Edit View Options Window Help
Ln 1 Col 1 22 RO Rec Off No Wrap DOS INS

Double-click the item in the list or select the "View" button to start process and view the report. Select the "Start" button to only run the process. Select

```
Note 4036: Signal CLK is preassigned to nonexistent
pin - signal ignored.
Note 4040: Signal LB0 is preassigned to pin 16;
however, the signal is incompatible in direction -
preassignment ignored.
Note 4036: Signal RB0 is preassigned to nonexistent
pin - signal ignored.
Note 4036: Signal RB1 is preassigned to nonexistent
pin - signal ignored.
Note 4040: Signal RB2 is preassigned to pin 13;
however, the signal is incompatible in direction -
preassignment ignored.
Note 4040: Signal RB3 is preassigned to pin 12;
however, the signal is incompatible in direction -
preassignment ignored.
```

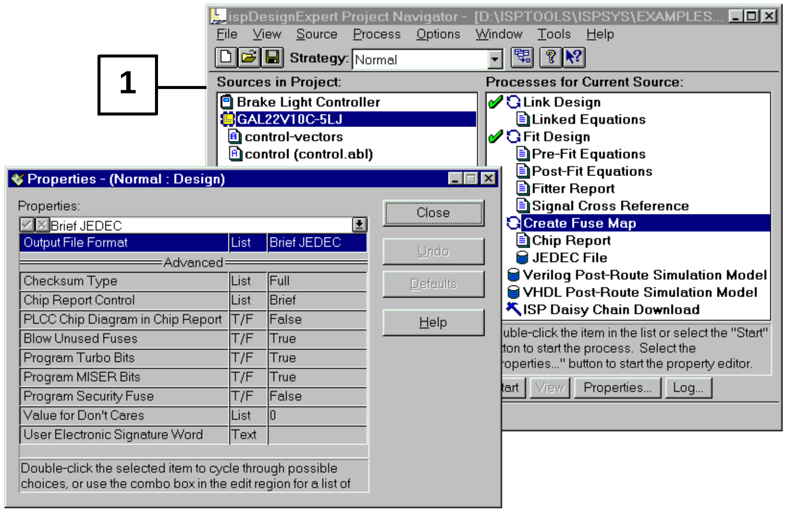
# Task 5 *Create Fuse Map*

After fitting the design, you can create a fuse map in JEDEC format for your design. The resource utilization report will be automatically displayed in the Report Viewer. The JEDEC or PROM file and resource utilization report are generated by the FUSEASM application. Several JEDEC and report properties can be set in the Properties dialog box.

*To create a fuse map and view the JEDEC file:*

1. With the device icon highlighted in the Sources window, select the Create Fuse Map process. (If you need to set properties for this process, click the **Properties** button at the bottom of the Project Navigator or select **Process** ⇒ **Properties**. Change the options of the properties in the prompt Properties dialog box. Close the Properties dialog box.) Double click the Create Fuse Map process or click the **Start** button. This starts the process of creating a fuse map and generating a JEDEC file.
2. When the process is completed successfully, you will find a green check mark beside the Create Fuse Map Select process as well as the JEDEC File process. Select the JEDEC File process and click on the **View** button at the bottom of the Project Navigator. The JEDEC file generated can be viewed in the Report Viewer.

***Note:*** *If your target device is in the GAL6001B, GAL6002B, or GAL20XV10B family, you need to add pin locking to the ABEL-HDL or schematic source file before running the Create Fuse Map process.*



1

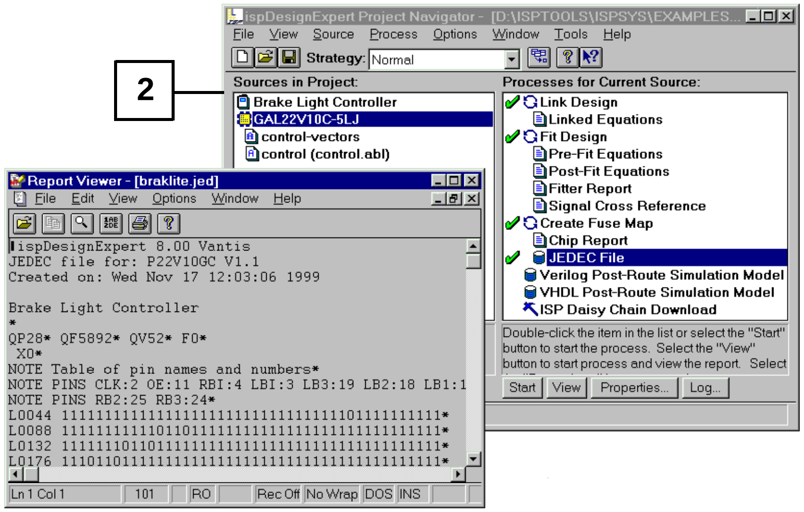
Properties - (Normal : Design)

Properties:

Brief JEDEC

| | | |
|---|---|---|
| Output File Format | List | Brief JEDEC |
| Advanced | | |
| Checksum Type | List | Full |
| Chip Report Control | List | Brief |
| PLCC Chip Diagram in Chip Report | T/F | False |
| Blow Unused Fuses | T/F | True |
| Program Turbo Bits | T/F | True |
| Program MISER Bits | T/F | True |
| Program Security Fuse | T/F | False |
| Value for Don't Cares | List | 0 |
| User Electronic Signature Word | Text | |

Double-click the selected item to cycle through possible choices, or use the combo box in the edit region for a list of



2

Report Viewer - [braklite.jed]

```
ispDesignExpert 8.00 Vantis
JEDEC file for: P22V10GC V1.1
Created on: Wed Nov 17 12:03:06 1999

Brake Light Controller
*
QP28* QF5892* QV52* F0*
 X0*
NOTE Table of pin names and numbers*
NOTE PINS CLK:2 OE:11 RBI:4 LBI:3 LB3:19 LB2:18 LB1:1
NOTE PINS RB2:25 RB3:24*
L0044 11111111111111111111111111111111110111111111*
L0088 11111111110110111111111111111111111111111111*
L0132 11111110110111111111111111111111111111111111*
L0176 11101101111111111111111111111111111111111111*
```

Ln 1 Col 1 | 101 | RO | Rec Off | No Wrap | DOS | INS

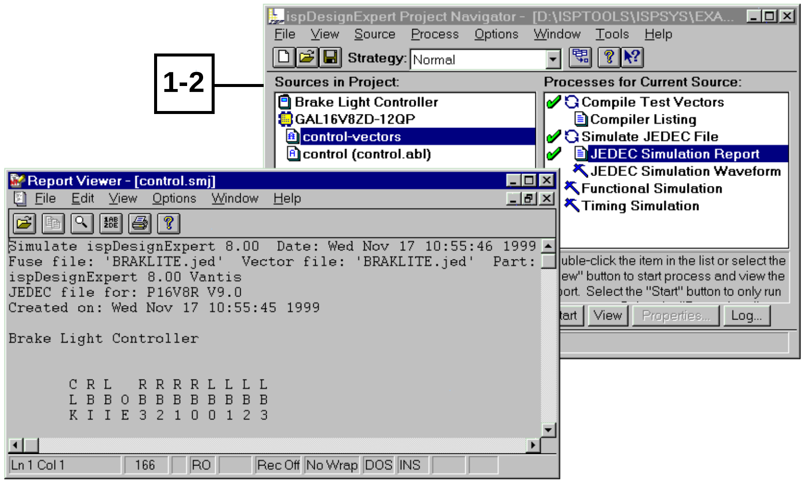
Double-click the item in the list or select the "Start" button to start the process. Select the "View" button to start process and view the report. Select

# Task 6 *Simulate JEDEC Files*

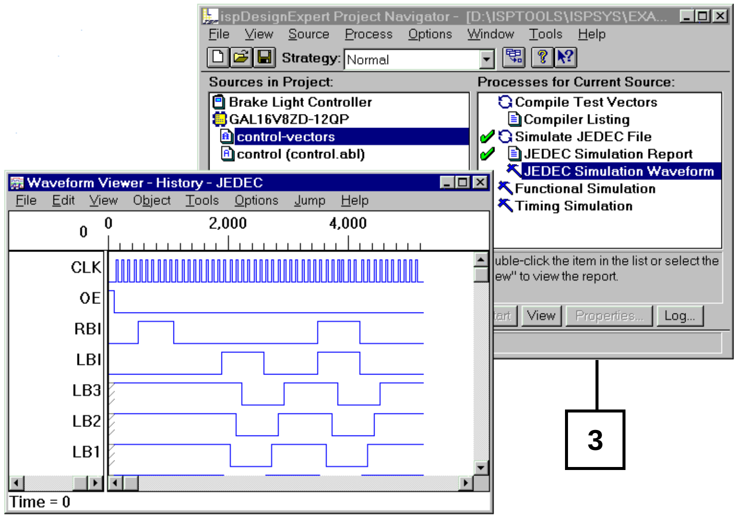
JEDEC simulation uses the test vectors specified in the top-level ABEL-HDL source to simulate your GAL design's JEDEC file as a final indication that the information to be programmed into your GAL is correct.

*To simulate the JEDEC file for your design:*

1. Choose the test vectors icon in the Sources window. Double click the Simulate JEDEC File process from the Processes window or click on the **Start** button at the bottom of the Project Navigator.
2. When the simulation is done, double click the JEDEC Simulation Report process. When the process is completed, the JEDEC Simulation Report (`.smj`) is opened in the Report Viewer.
3. Double click the JEDEC Simulation Waveform process. Or highlight the JEDEC Simulation Waveform process and click the **View** button. The waveforms of the simulated signals are displayed in the Waveform Viewer. Refer to the ***Design Verification Tools User Manual*** for information on how to view waveforms.


1-2
ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXA...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Brake Light Controller
GAL16V8ZD-12QP
control-vectors
control (control.abl)
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Simulate JEDEC File
JEDEC Simulation Report
JEDEC Simulation Waveform
Functional Simulation
Timing Simulation
uble-click the item in the list or select the
ew" button to start process and view the
port. Select the "Start" button to only run
tart View Properties... Log...
Report Viewer - [control.smj]
File Edit View Options Window Help
Ln 1 Col 1 166 RO Rec Off No Wrap DOS INS

```
Simulate ispDesignExpert 8.00  Date: Wed Nov 17 10:55:46 1999
Fuse file: 'BRAKLITE.jed'  Vector file: 'BRAKLITE.jed'  Part:
ispDesignExpert 8.00 Vantis
JEDEC file for: P16V8R V9.0
Created on: Wed Nov 17 10:55:45 1999

Brake Light Controller


       C R L   R R R R L L L L
       L B B O B B B B B B B B
       K I I E 3 2 1 0 0 1 2 3
```


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXA...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Brake Light Controller
GAL16V8ZD-12QP
control-vectors
control (control.abl)
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Simulate JEDEC File
JEDEC Simulation Report
JEDEC Simulation Waveform
Functional Simulation
Timing Simulation
uble-click the item in the list or select the
ew" to view the report.
tart View Properties... Log...
Waveform Viewer - History - JEDEC
File Edit View Object Tools Options Jump Help
0
0
2,000
4,000
CLK
OE
RBI
LBI
LB3
LB2
LB1
Time = 0
3

# Task 7 *Run Timing Simulation*

Post-route timing simulation confirms that your design is compatible with the timing and propagation delays that exist in a specific device.

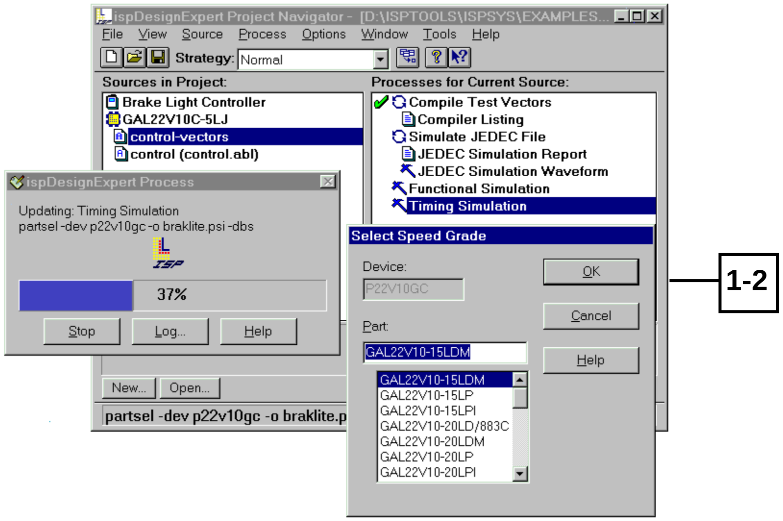
You can specify the test vectors as discussed in Task 3.

*To run Timing Simulation:*

1. Select the test vector icon from the Sources window of the Project Navigator. Double click the associated Timing Simulation process or click the **Start** button at the bottom of the Project Navigator to launch Simulator Control Panel. At this moment, the Simulator starts to get timing netlist information.
2. The ispDesignExpert Process dialog box appears momentarily. The Select Speed Grade dialog box appears. Choose the desired speed of the device from the list and click **OK** to close the dialog box. The process goes until it is completed successfully. The Simulator Control Panel is launched.
3. In the Simulator Control Panel window, click the **Run** icon from the toolbar or choose **Simulate** ⇒ **Run** to start the simulation.
4. When the simulation ends, you can view the simulation results in Waveform Viewer.

***Note**: Keep the **View** ⇒ **Show Waveforms** menu item checked so that the Waveform Viewer will automatically be opened with the waveforms of the simulated signals.*

Refer to the ***Design Verification Tools User Manual*** for more detailed information.


ispDesignExpert Project Navigator - [D:\ISPTOOLS\ISPSYS\EXAMPLES...
File View Source Process Options Window Tools Help
ispDesignExpert Process
Stop
Log...
Help
New...
Open...
Select Speed Grade
OK
Cancel
Help
1-2

Strategy: Normal

Sources in Project:
- Brake Light Controller
- GAL22V10C-5LJ
- control-vectors
- control (control.abl)

Processes for Current Source:
- Compile Test Vectors
- Compiler Listing
- Simulate JEDEC File
- JEDEC Simulation Report
- JEDEC Simulation Waveform
- Functional Simulation
- Timing Simulation

Updating: Timing Simulation
partsel -dev p22v10gc -o braklite.psi -dbs

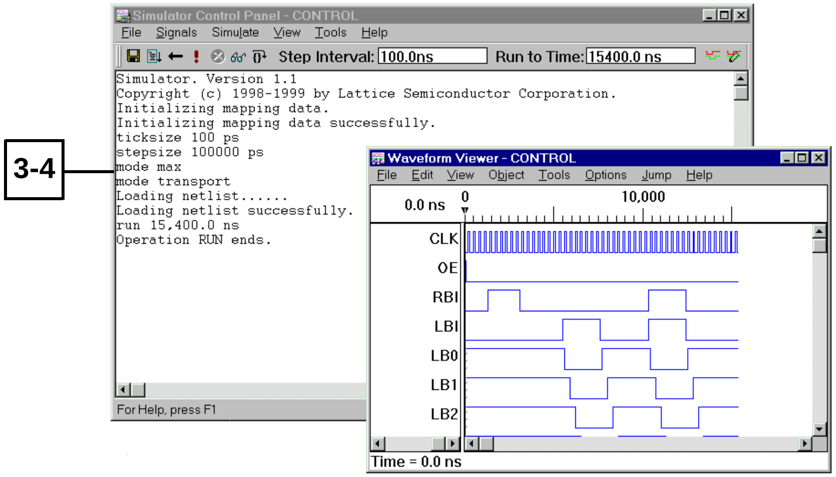
37%

partsel -dev p22v10gc -o braklite.p

Device: P22V10GC

Part: GAL22V10-15LDM

- GAL22V10-15LDM
- GAL22V10-15LP
- GAL22V10-15LPI
- GAL22V10-20LD/883C
- GAL22V10-20LDM
- GAL22V10-20LP
- GAL22V10-20LPI


3-4
Simulator Control Panel - CONTROL
File Signals Simulate View Tools Help
Waveform Viewer - CONTROL
File Edit View Object Tools Options Jump Help
0.0 ns
0
10,000
CLK
OE
RBI
LBI
LB0
LB1
LB2

Step Interval: 100.0ns    Run to Time: 15400.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode max
mode transport
Loading netlist......
Loading netlist successfully.
run 15,400.0 ns
Operation RUN ends.
```

For Help, press F1

Time = 0.0 ns

# Congratulations!

You have completed the Design Implementation and Verification for GAL Devices tutorial. In this tutorial, you have learned how to:

- open an example project in ispDesignExpert
- change the device
- run Functional Simulation
- fit a design
- create a Fuse Map
- simulate JEDEC Files
- run Timing Simulation

# Tutorial 10 Design Implementation and Verification for PAL Devices

This tutorial presents the basic operation of a PAL design, focusing on the tasks and design tools needed to implement and verify a PAL design.

## Prerequisites

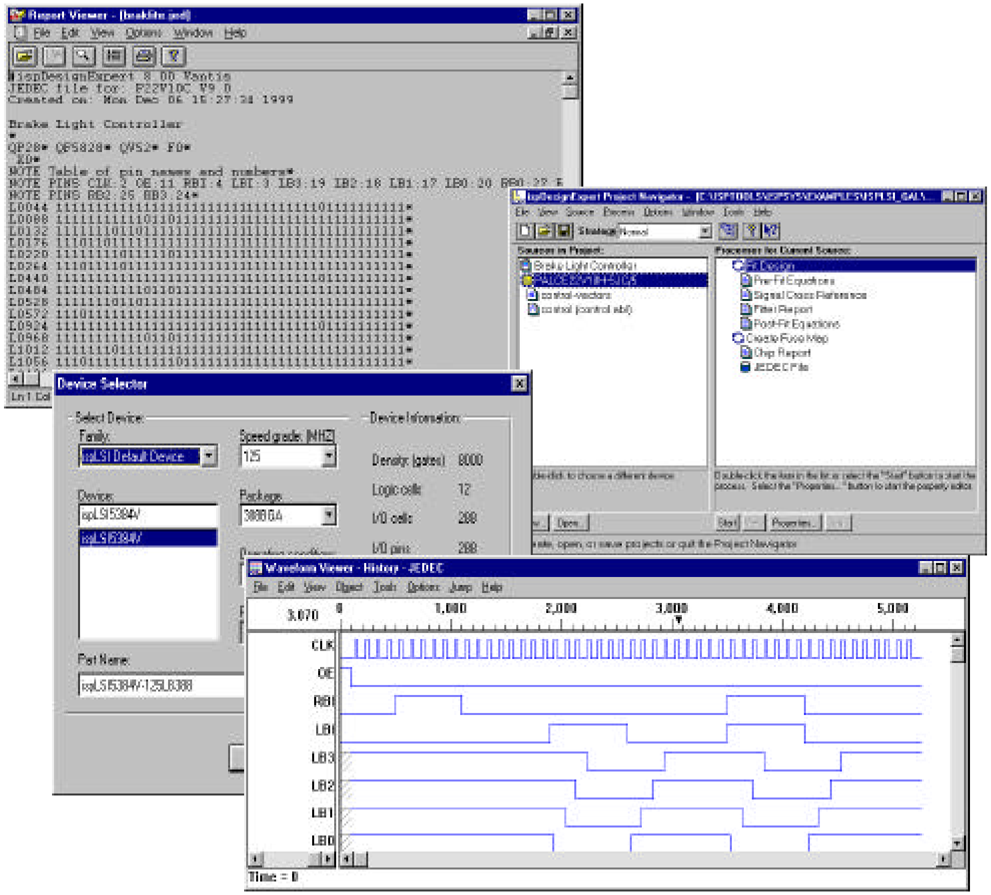
Before attempting this tutorial, you should complete the Schematic and ABEL-HDL Design Entry tutorial.

## Learning Objectives

When you are finished with this tutorial, you should have a basic understanding of steps and tools necessary to implement and verify a PAL design using the ispDesignExpert software.

## Time to Complete This Tutorial

On average, the time to complete this tutorial is about 30 minutes.


Report Viewer - [braklite.jed]
File Edit View Options Window Help
Ln 1 Col

```
#ispDesignExpert 8.00 Vantis
JEDEC file for: P22V10C V9.0
Created on: Mon Dec 06 15:27:38 1999

Brake Light Controller
*
QP28* QF5828* QV52* F0*
 X0*
NOTE Table of pin names and numbers*
NOTE PINS CLK:2 OE:11 RBI:4 LBI:3 LB3:19 LB2:18 LB1:17 LB0:20 RB0:27 F
NOTE PINS RB2:25 RB3:24*
L0044 11111111111111111111111111111111110111111111*
L0088 11111111111101101111111111111111111111111111*
L0132 11111101101111111111111111111111111111111111*
L0176 11101101111111111111111111111111111111111111*
L0220 11111110111101111111111111111111111111111111*
L0264 11101110111111111111111111111111111111111111*
L0440 11111111111111111111111111111111110111111111*
L0484 11111111111101101111111111111111111111111111*
L0528 11111101101111111111111111111111111111111111*
L0572 11101111111111111111111111111111111111111111*
L0924 11111111111111111111111111111111110111111111*
L0968 11111111111101101111111111111111111111111111*
L1012 11111110111111111111111111111111111111111111*
L1056 11101111111111110111111111111111111111111111*
```

ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\ISPLSI_GAL\...
File View Source Process Options Window Tools Help
Strategy: Normal
Sources in Project:
Brake Light Controller
PALCE22V10H-5JC/5
control-vectors
control (control.abl)
Processes for Current Source:
Fit Design
Pre-Fit Equations
Signal Cross Reference
Fitter Report
Post-Fit Equations
Create Fuse Map
Chip Report
JEDEC File
Double-click to choose a different device
Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor
Open...
Start
Properties...
Create, open, or save projects or quit the Project Navigator

Device Selector

Select Device:

Family: ispLSI Default Device

Speed grade: [MHZ] 125

Device: ispLSI5384V

ispLSI5384V

Package: 388BGA

Part Name: ispLSI5384V-125LB388

Device Information:

| | |
|---|---|
| Density: (gates) | 8000 |
| Logic cells | 12 |
| I/O cells: | 288 |
| I/O pins: | 288 |

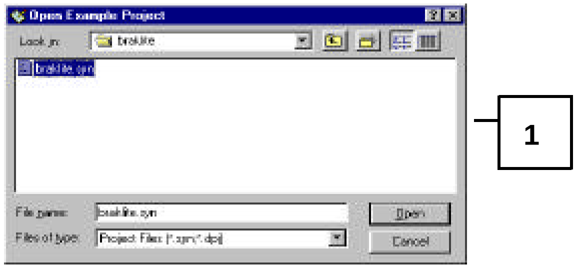
Waveform Viewer - History - JEDEC
File Edit View Object Tools Options Jump Help
3,070
0
1,000
2,000
3,000
4,000
5,000
CLK
OE
RBI
LBI
LB3
LB2
LB1
LB0
Time = 0

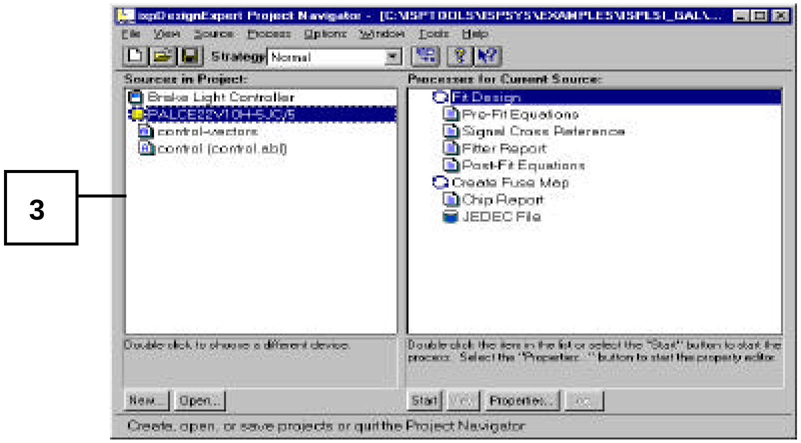
# Task 1 *Open a Project*

To continue with this tutorial, open an example project.

*To open the example project*:

1. Choose **File** ⇒ **Open Example** and select `ispLSI_GAL\GAL\braklite\braklite.syn`.
2. Click **Open**.
3. The Brake Light Controller project is opened in the Project Navigator.





Double click to choose a different device.

Double click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Create, open, or save projects or quit the Project Navigator

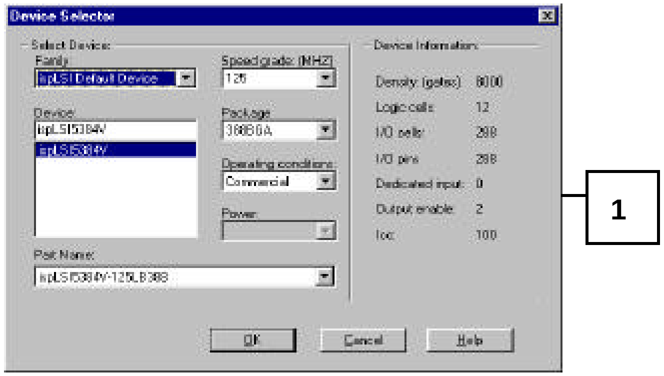
# Task 2 *Change your Device*

The Project Navigator lets you target your design to a specific device at any time during the design process. We have opened an example project with the ispLSI Default device. In this task, you will change to select a desired PAL device for your design.

*To change a device:*

1. In the Sources window, double click the **Default Device**. The Device Selector dialog box opens. The dialog box shows the available device families and the devices in the selected family.
2. In the Device Selector dialog box, select **PAL** device family. Select **PAL22V10** from the Part Name field. Accept the default settings and then click **OK**.
3. The Confirm Changes dialog box appears prompting you to confirm your device change. Click **Yes** to confirm that you wish to change the device. When you change devices, the ispDesignExpert software design environment reconfigures to facilitate designing with the selected device.

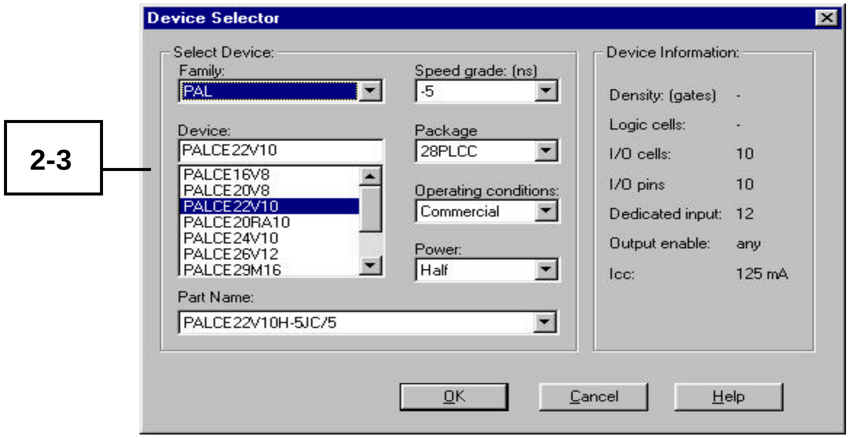
***Note**: Depending on the device you choose, the Confirm Changes dialog box does not appear for all the devices.*



Device Selector

Select Device:
Family: ispLSI Default Device
Speed grade: (MHZ) 125
Device: ispLSI5384V
ispLSI5384V
Package: 388BGA
Operating conditions: Commercial
Power:
Part Name: ispLSI5384V-125LB388

Device Information:
Density (gates) 8000
Logic cells 12
I/O cells 288
I/O pins 288
Dedicated input 0
Output enable 2
Icc 100



Device Selector

Select Device:
Family: PAL
Speed grade: (ns) -5
Device: PALCE22V10
PALCE16V8
PALCE20V8
PALCE22V10
PALCE20RA10
PALCE24V10
PALCE26V12
PALCE29M16
Package: 28PLCC
Operating conditions: Commercial
Power: Half
Part Name: PALCE22V10H-5JC/5

Device Information:
Density: (gates) -
Logic cells: -
I/O cells: 10
I/O pins 10
Dedicated input: 12
Output enable: any
Icc: 125 mA

# Task 3 *Fit Design*

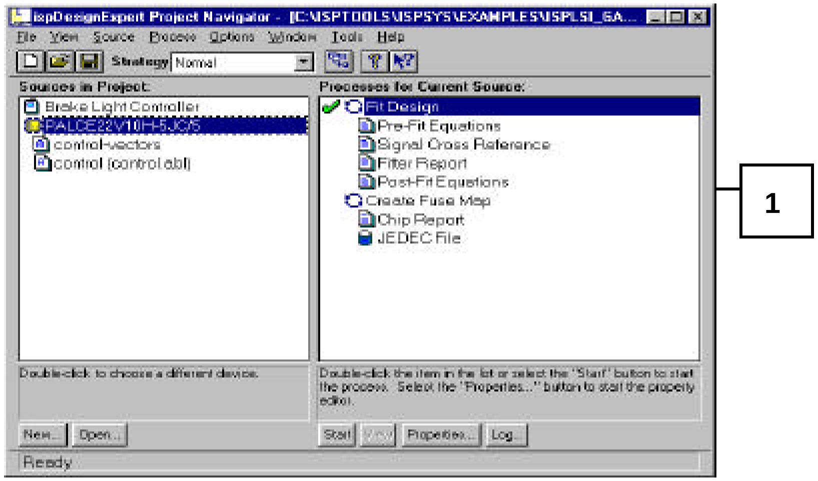
Now you can fit your design to the target device. Use the Fit Design process, you can run the compiler to automatically assign the pins and nodes of your design to physical pins and nodes in the device you have chosen. Several fit strategies can be selected in the Properties dialog box. You can view the Fitter Report of your design after running the Fit Design process.

*To fit your design and view the report:*

1. In the Sources window, select the target device (**PALCE22V10**) if not already selected. In the Processes window, double-click **Fit Design**.
2. When the process is finished, double-click the **Fitter Report** in the Processes window. If there is any syntax error in the compilation procedure, the software displays errors in the report and an error indication (red X) appears beside the Fit Design process in the Processes window.
3. Close the Report Viewer.

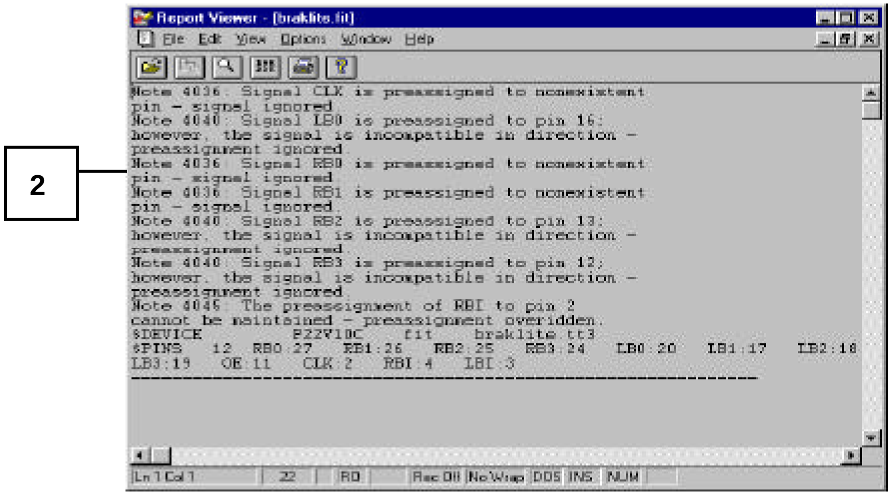
***Note****: If the target device is among the GAL6001B, GAL6002B, or GAL20XV10B device families, no Fit Design process is available in the Processes window*

.



Double-click to choose a different device.

Double-click the item in the list or select the 'Start' button to start the process. Select the 'Properties...' button to start the property editor.


Report Viewer - [braklite.fit]
File Edit View Options Window Help
Ln 1 Col 1 22 RO Rec Off No Wrap DOS INS NUM
2

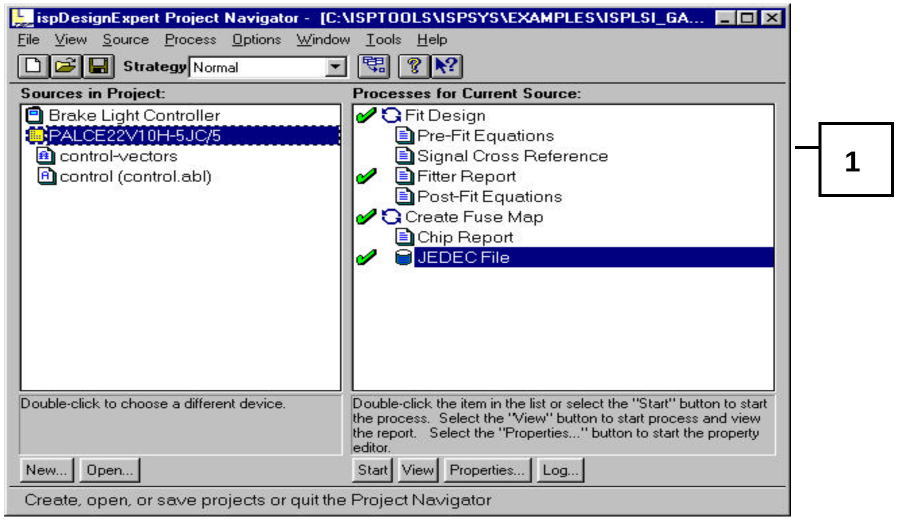
```
Note 4036: Signal CLK is preassigned to nonexistent
pin - signal ignored.
Note 4040: Signal LB0 is preassigned to pin 16;
however, the signal is incompatible in direction -
preassignment ignored.
Note 4036: Signal RB0 is preassigned to nonexistent
pin - signal ignored.
Note 4036: Signal RB1 is preassigned to nonexistent
pin - signal ignored.
Note 4040: Signal RB2 is preassigned to pin 13;
however, the signal is incompatible in direction -
preassignment ignored.
Note 4040: Signal RB3 is preassigned to pin 12;
however, the signal is incompatible in direction -
preassignment ignored.
Note 4046: The preassignment of RBI to pin 2
cannot be maintained - preassignment overidden.
$DEVICE        P22V10C    fit    braklite.tt3
$PINS   12  RB0:27   RB1:26   RB2:25   RB3:24   LB0:20   LB1:17   LB2:18
LB3:19   OE:11   CLK:2   RBI:4   LBI:3
-------------------------------------------------------------------------------
```

# Task 4 *Create Fuse Map*

After fitting the design, you can create a fuse map in JEDEC format for your design. The resource utilization report will be automatically displayed in the Report Viewer. The JEDEC or PROM file and resource utilization report are generated by the FUSEASM application. Several JEDEC and report properties can be set in the Properties dialog box.

*To create a fuse map and view the JEDEC file:*

1. Select the target device (**PALCE22V10**). In the Processes window double-click **Create Fuse Map**. This starts the process of creating fuse map and generating JEDEC file.
2. When the process is completed successfully, a green check mark appears beside the Create Fuse Map as well as the JEDEC File process.
3. In the Processes window select **JEDEC File** and click on the **View** button at the bottom of the Project Navigator. The JEDEC file generated can be viewed in the Report Viewer.


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\ISPLSI_GA...
File View Source Process Options Window Tools Help
Strategy
Sources in Project:
Processes for Current Source:
New... Open...
Start View Properties... Log...
1

Strategy Normal

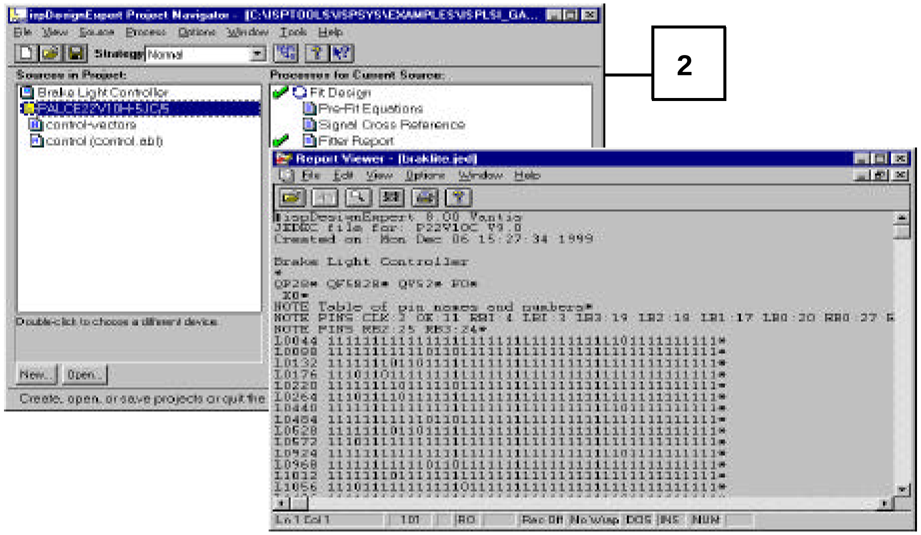
Sources in Project:
- Brake Light Controller
- PALCE22V10H-5JC/5
- control-vectors
- control (control.abl)

Processes for Current Source:
- ✓ Fit Design
  - Pre-Fit Equations
  - Signal Cross Reference
  - ✓ Fitter Report
  - Post-Fit Equations
- ✓ Create Fuse Map
  - Chip Report
  - ✓ JEDEC File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "View" button to start process and view the report. Select the "Properties..." button to start the property editor.

Create, open, or save projects or quit the Project Navigator


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\ISPLSI_GA...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
Brake Light Controller
PALCE22V10H-5JC/5
control-vectors
control (control.abl)
Processes for Current Source:
Fit Design
Pre-Fit Equations
Signal Cross Reference
Fitter Report
Double-click to choose a different device.
New... Open...
Create, open, or save projects or quit the
Report Viewer - [braklite.jed]
File Edit View Options Window Help
Ln 1 Col 1
101
RO
Rec Off
No Wrap
DOS
INS
NUM
2

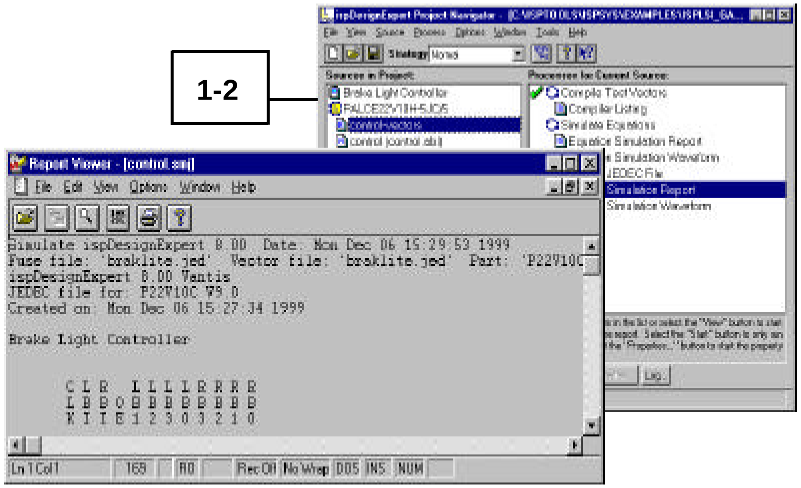
```
ispDesignExpert 8.00 Vantis
JEDEC file for: P22V10C V9.0
Created on: Mon Dec 06 15:27:34 1999

Brake Light Controller
*
QP28* QF5828* QV52* F0*
 X0*
NOTE Table of pin names and numbers*
NOTE PINS CLK:2 OE:11 RBI:4 LBI:3 LB3:19 LB2:18 LB1:17 LB0:20 RB0:27 R
NOTE PINS RB2:25 RB3:24*
L0044 11111111111111111111111111111111101111111111*
L0088 11111111111011011111111111111111111111111111*
L0132 11111110110111111111111111111111111111111111*
L0176 11101101111111111111111111111111111111111111*
L0220 11111111011111101111111111111111111111111111*
L0264 11101111011111111111111111111111111111111111*
L0440 11111111111111111111111111111111101111111111*
L0484 11111111111011011111111111111111111111111111*
L0528 11111110110111111111111111111111111111111111*
L0572 11101111111111111111111111111111111111111111*
L0924 11111111111111111111111111111111101111111111*
L0968 11111111111011011111111111111111111111111111*
L1012 11111110111111111111111111111111111111111111*
L1056 11101111111111101111111111111111111111111111*
```

# Task 5 *Simulate JEDEC Files*

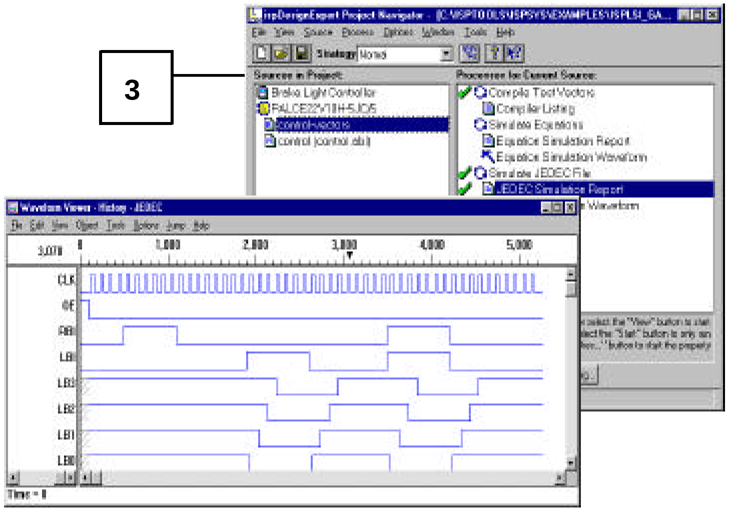
JEDEC simulation uses the test vectors specified in the top-level ABEL-HDL source to simulate your PAL design's JEDEC file as a final indication that the information to be programmed into your PAL is correct.

*To simulate the JEDEC file of your design:*

1. In the Sources window, select **control-vectors**. Double-click **Simulate JEDEC File** in the Processes window.
2. When the simulation is done, double-click **JEDEC Simulation Report** in the Processes window. When the process is completed, the JEDEC Simulation Report (`.smj`) is opened in the Report Viewer.
3. In the Processes window double-click **JEDEC Simulation Waveform**. The waveforms of the simulated signals are displayed in the Waveform Viewer. Refer to the ***Design Verification Tools User Manual*** for information on how to view waveforms.



```
Simulate ispDesignExpert 8.00  Date  Mon Dec 06 15:29:53 1999
Fuse file: 'braklite.jed'  Vector file: 'braklite.jed'  Part: 'P22V10C
ispDesignExpert 8.00 Vantis
JEDEC file for: P22V10C V9.0
Created on: Mon Dec 06 15:27:34 1999

Brake Light Controller


        C L R   L L L L R R R R
        L B B O B B B B B B B B
        K I I E 1 2 3 0 3 2 1 0
```


3
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\ISPLSI_GA...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
Brake Light Controller
PALCE22V10H-5JC/5
control-vectors
control (control.abl)
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Simulate Equations
Equation Simulation Report
Equation Simulation Waveform
Simulate JEDEC File
JEDEC Simulation Report
Waveform
Waveform Viewer - History - JEDEC
File Edit View Object Tools Options Jump Help
3,078
0
1,000
2,000
3,000
4,000
5,000
CLK
OE
RBI
LBI
LB3
LB2
LB1
LB0
Time = 0

# Congratulations!

You have completed the Design Implementation and Verification for PAL Devices tutorial. In this tutorial, you have learned how to:

- open an example project in ispDesignExpert
- change the device
- fit a design
- create a Fuse Map
- simulate JEDEC Files

# Part IV: Simulation with ispDesignExpert

# Tutorial 11 Simulating a Design with the Lattice Logic Simulator

This tutorial shows you how to run the Lattice Logic Simulator for a design implemented in an ispLSI device.

## Prerequisites

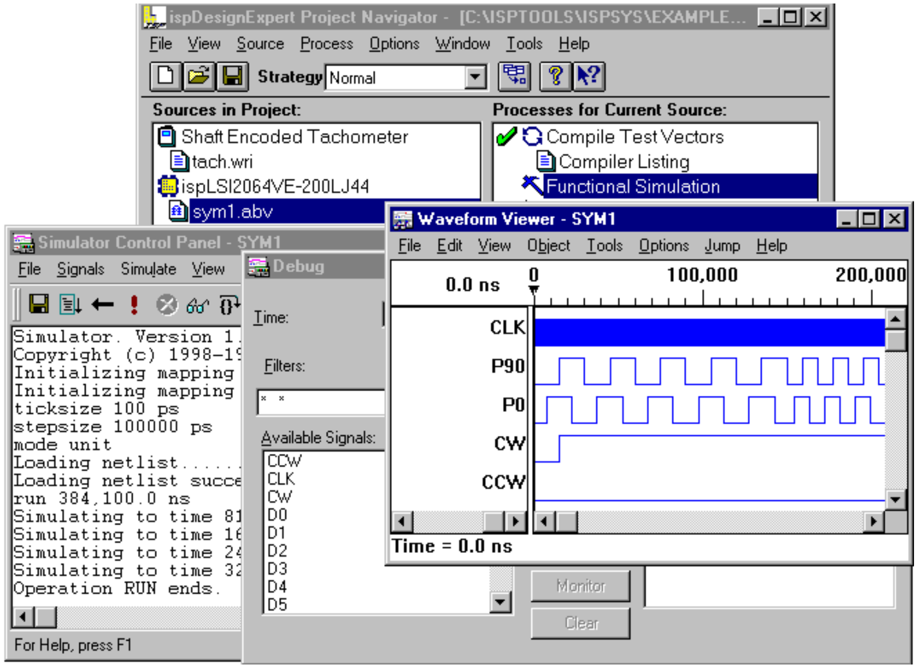
Before attempting this tutorial, you should complete the Design Implementation and Verification for ispLSI Devices tutorial.

## Learning Objectives

When you are finished with this tutorial, you should know how to simulate an ispLSI design in ispDesignExpert. You will also understand how to view the simulation results and use the Lattice Logic Simulator interactive features to debug the design.

## Time to Complete This Tutorial

The time to complete this tutorial is about 30 minutes.



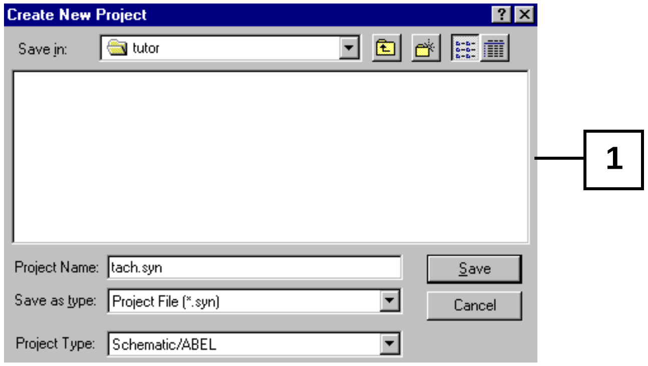
```
Simulator. Version 1.
Copyright (c) 1998-19
Initializing mapping
Initializing mapping
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist succe
run 384,100.0 ns
Simulating to time 81
Simulating to time 16
Simulating to time 24
Simulating to time 32
Operation RUN ends.
```

# Task 1 *Create a New Project in ispDesignExpert*

Create a directory to save your tutorial example. In the example of this tutorial, the directory used is `tutor`.

*To create a new project:*

1. In the Project Navigator, select **File** ⇒ **New Project** to display the Create New Project dialog.
2. Navigate to the `ispTools\ispsys\examples\ispLSI_GAL\abel` directory and create a new folder called `tutor`.
3. Go into the new folder and type the name `tach` for the new project, select `Schematic/ABEL` as the Project Type, and then click **Save** to load the new project into the Project Navigator.
4. Title the project `Shaft Encoded Tachometer` in the Sources window.
5. Double-click the device icon to display the Device Selector dialog and change the device to `ispLSI2064VE-200LJ44`.
6. Select **Source** ⇒ **Import** to open the Import File dialog. Navigate to `ispTools\ispsys\examples\ispLSI_GAL\abel\tach` and select all `.sch` and `.abl` files and then click **Open**.
7. The schematic and ABEL-HDL files are imported as design modules into the Sources window of the Project Navigator.

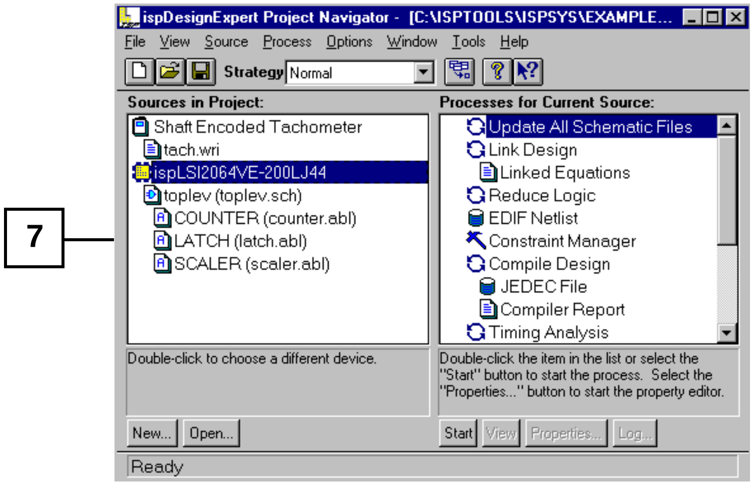


Save in: tutor

Project Name: tach.syn

Save as type: Project File (*.syn)

Project Type: Schematic/ABEL



Strategy Normal

Sources in Project:

- Shaft Encoded Tachometer
- tach.wri
- ispLSI2064VE-200LJ44
- toplev (toplev.sch)
- COUNTER (counter.abl)
- LATCH (latch.abl)
- SCALER (scaler.abl)

Processes for Current Source:

- Update All Schematic Files
- Link Design
- Linked Equations
- Reduce Logic
- EDIF Netlist
- Constraint Manager
- Compile Design
- JEDEC File
- Compiler Report
- Timing Analysis

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

# Task 2 *a) Create ABEL Test Vectors*

Simulation requires a test stimulus file that specifies the inputs for the simulator. Two types of test stimuli that can be accepted by the Lattice Logic Simulator are:

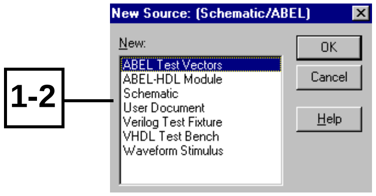
- ABEL test vector file (`.abv` or ***design***`-vectors` in ABEL-HDL source)
- graphic waveform file (`.wdl`)

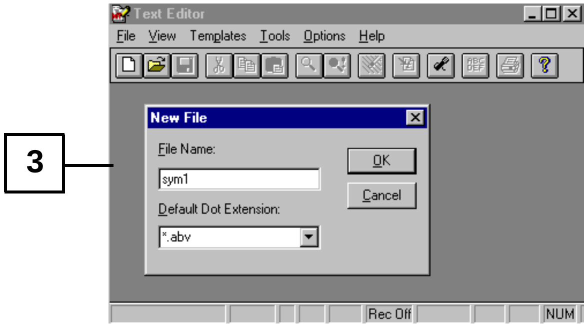
Test vectors can be specified in two ways:

- Place test vectors in an ABEL-HDL source. The Project Navigator will create a dummy test vector file (***design***`-vectors`).
- Place test vectors in a `.abv` file.

*To create an* ***`.abv`*** *file:*

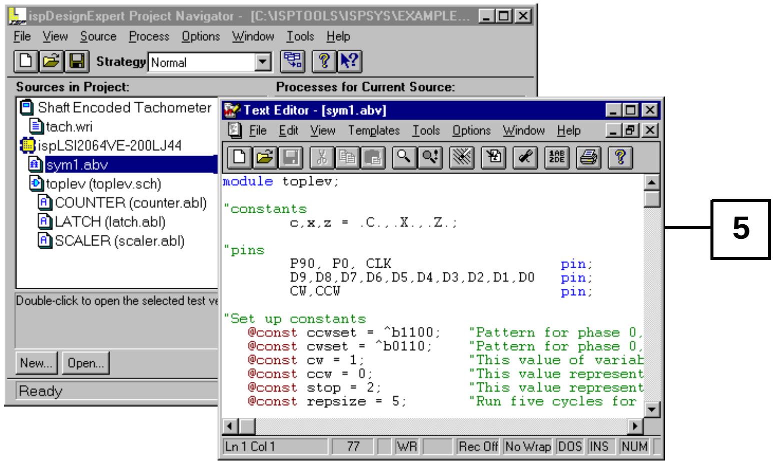
1. From the Project Navigator, select **Source** ⇒ **New** to display the New Source dialog.
2. Click ABEL Test Vectors in the New field, and then click **OK**.
3. This launches the Text Editor, along with the New File dialog. Enter the name for the `.abv` file and then click **OK**. The Text Editor is displayed with the new `.abv` file name.
4. Enter syntax in the Text Editor. (Refer to the `sym1.abv` file in the `ispTools\ispsys\examples\ispLSI_GAL\abel\tach` directory.
5. Select **File** ⇒ **Save** from the Text Editor to save the file. The `.abv` file appears in the Sources window of the Project Navigator.





File Name: sym1

Default Dot Extension: *.abv



```
module toplev;

"constants
        c,x,z = .C.,.X.,.Z.;

"pins
        P90, P0, CLK                    pin;
        D9,D8,D7,D6,D5,D4,D3,D2,D1,D0   pin;
        CW,CCW                          pin;

"Set up constants
   @const ccwset = ^b1100;    "Pattern for phase 0,
   @const cwset = ^b0110;     "Pattern for phase 0,
   @const cw = 1;             "This value of variat
   @const ccw = 0;            "This value represent
   @const stop = 2;           "This value represent
   @const repsize = 5;        "Run five cycles for
```

## b) Create Waveform Stimulus

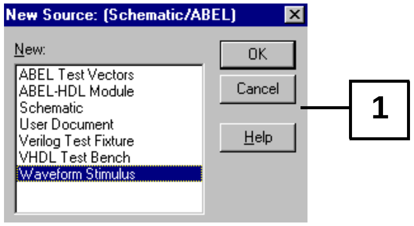
*To create a `.wdl` file:*

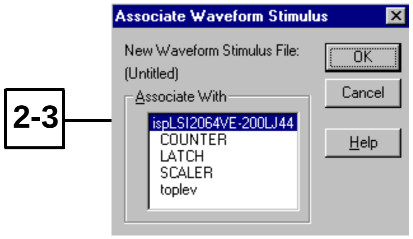
1. From the Project Navigator, select **Source** ⇒ **New** to display the New Source dialog. Click on Waveform Stimulus in the New field and then click **OK**.
2. The associate Waveform Stimulus dialog appears.

***Note**: If you associate the waveform stimulus file with the selected device, both functional and timing simulation are supported in the Processes window. However, if you associate the waveform stimulus file with a design module, only functional simulation is available.*

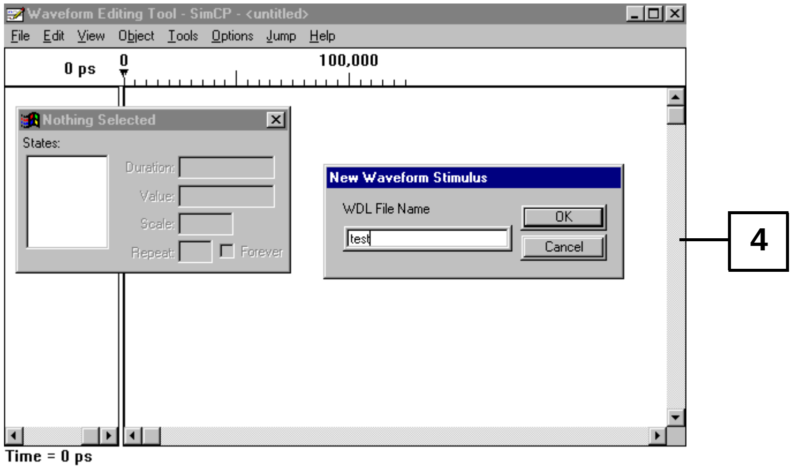
3. Select the source with which you want to associate the `.wdl` file, then click **OK**.
4. The Waveform Editing Tool (WET) appears with the New Waveform Stimulus dialog. Enter the name for the `.wdl` file in the WDL File Name field, and click **OK**. The WET appears with the new `.wdl` file name.

***Tip**: You can use **Source** ⇒ **Import** to add a desired test stimulus from an example project into the Sources window more directly.*





New Waveform Stimulus File:
(Untitled)



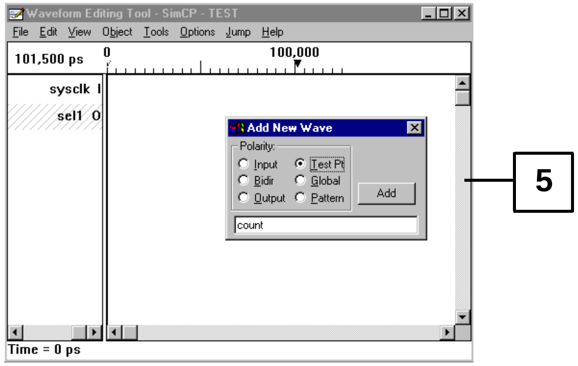
WDL File Name
test

## b) Create Waveform Stimulus (continued)

5. Select **Edit** ⇒ **New Wave** and the Add New Wave dialog box displays. Specify a signal name or a bus name and select the polarity for it, then click the **Add** button to add the name to the display.
6. Or, you can import signal names directly from a `.naf` file using the **Edit** ⇒ **Import Wave** command. In the pop-up Import dialog box, select the signals from the left field you need for the new `.wdl` file and click the **Add** button to add them to the right field. Click the **Show** button to display the desired signal(s) to the Waveform Editing Tool window.

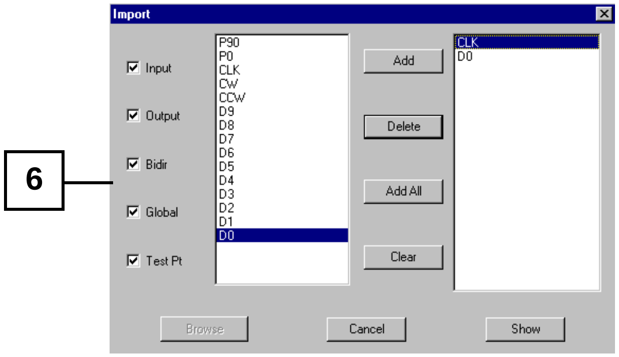
***Note**: If you cannot find a desired `.naf`, open the corresponding source in the Text Editor or the Schematic Editor. Make a modification to that source, which will not change its original functionality. Save the modified source file. Then, by clicking the **Browse** button in the Import dialog box, you will be able to find the relevant `.naf` file in the pop-up Import Naf File dialog box.*

7. In the Waveform Editing Tool, select **Options** ⇒ **Timing Options**. Set appropriate time units and press **Save As Defaults** button.


Waveform Editing Tool - SimCP - TEST
File Edit View Object Tools Options Jump Help
101,500 ps
0
100,000
sysclk I
sel1 0
Add New Wave
Add
Time = 0 ps
5

Polarity: ○ Input ○ Bidir ○ Output ● Test Pt ○ Global ○ Pattern

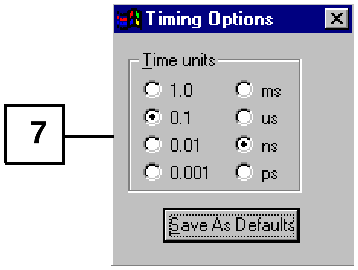
count



☑ Input
☑ Output
☑ Bidir
☑ Global
☑ Test Pt

P90
P0
CLK
CW
CCW
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

CLK
D0



Time units

○ 1.0 ○ ms
● 0.1 ○ us
○ 0.01 ● ns
○ 0.001 ○ ps

# b) Create Waveform Stimulus (continued)

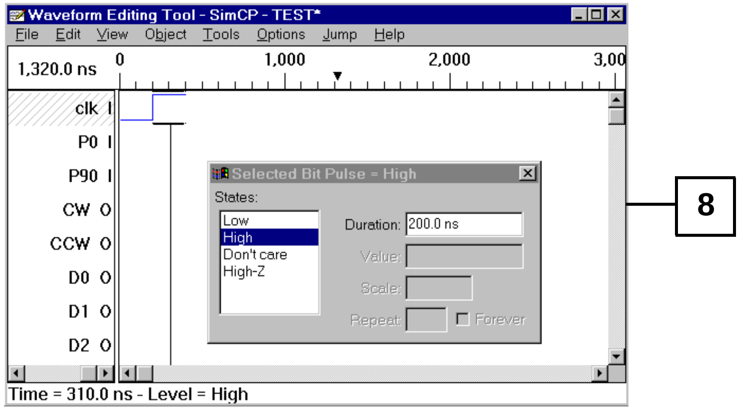
8. In the Waveform Editing Tool window, click on `clk` which you want to create a waveform for. The name is highlighted with light gray diagonal lines. Move the mouse to the waveform section of the window and click where you want the first transition. (You must click in the same row of the highlighted name.) A line is drawn to show the first section (called a Pulse) of the waveform.

***Note**: The Selected Bit Pulse dialog box gives you complete control over the state and duration of each Pulse. Select the state in the States list box for the signal, and specify the duration in the Duration text box.*

9. Click again to create the second transition. The second Pulse is drawn at the opposite state of the first Pulse. Continue clicking to complete the waveform.

***Tips:** You may drag to select any arbitrary section of a waveform (at least across one transition), and specify the repeat times in the dialog box to repeat the pattern automatically.*
*Click and drag the mouse within one pulse. (Do not drag the mouse over the transitions at either end.) The dragged region is converted to the opposite polarity.*

10. Repeat the Step 7 and 8 to complete editing the waveforms of other input signals as you desired.
11. Select **File** ⇒ **Save** from the Waveform Editing Tool to save the changes.


Waveform Editing Tool - SimCP - TEST*
File Edit View Object Tools Options Jump Help
1,320.0 ns
0
1,000
2,000
3,00
clk I
P0 I
P90 I
CW O
CCW O
D0 O
D1 O
D2 O
8

Selected Bit Pulse = High

States: Low, **High**, Don't care, High-Z

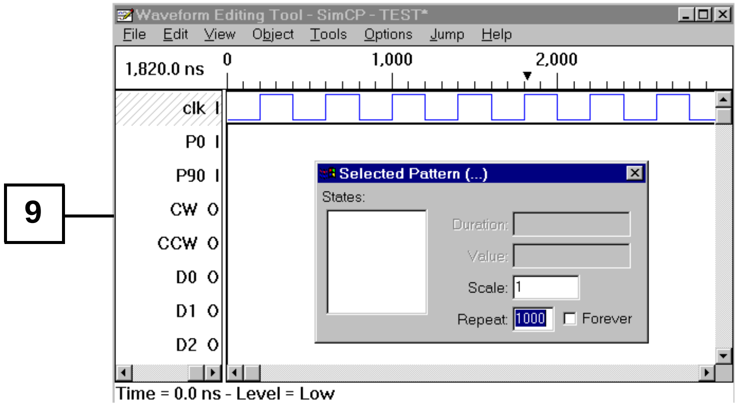
Duration: 200.0 ns

Value:

Scale:

Repeat: □ Forever

Time = 310.0 ns - Level = High


Waveform Editing Tool - SimCP - TEST*
File Edit View Object Tools Options Jump Help
1,820.0 ns
0
1,000
2,000
clk I
P0 I
P90 I
CW O
CCW O
D0 O
D1 O
D2 O
9

Selected Pattern (...)

States:

Duration:

Value:

Scale: 1

Repeat: 1000 □ Forever

Time = 0.0 ns - Level = Low

# Task 3 *Run Functional Simulation and View Simulation Results*

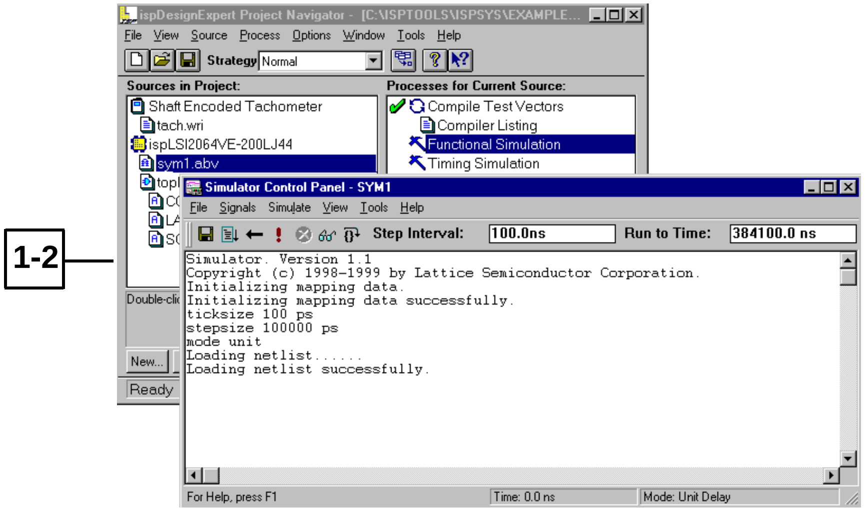
*To run functional simulation:*

1. In the Sources window, select the test stimulus (`.abv` or `.wdl` file).
2. In the Processes window, double-click **Functional Simulation**.

   The Simulator Control Panel is displayed and the netlist is loaded.
3. Click the **Run** icon or select **Simulate** ⇒ **Run** to start simulation.
4. When the message `Operation RUN ends` appears in the Simulator Control Panel, select **Tools** ⇒ **Waveform Viewer** to open the Waveform Viewer with the simulation results.

***Tip**: If you keep **View** ⇒ **Show Waveforms** checked, the Waveform Viewer will be displayed during the simulation to show you the simulation results dynamically.*

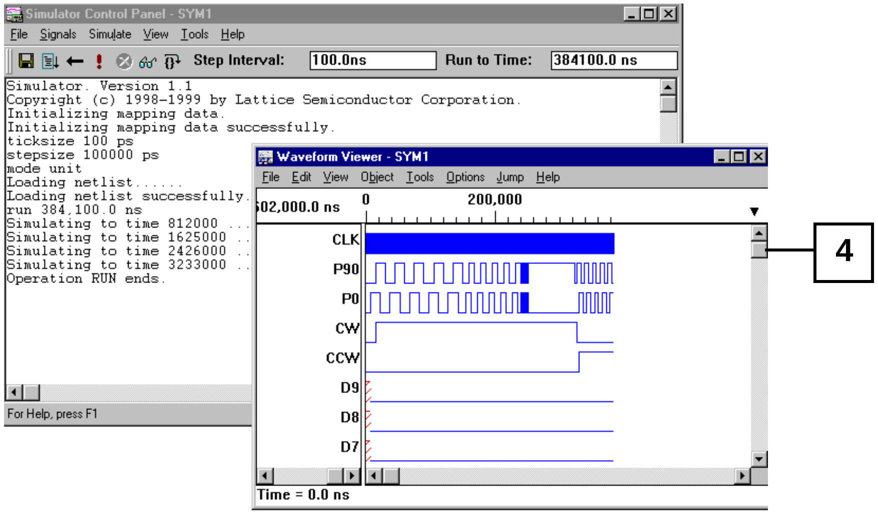
***Note**: All the signals specified in the `.abv` or `.wdl` file will be automatically shown in the Waveform Viewer after simulation. If the Waveform Viewer has been modified and saved for the project, waveforms for the modified signals will be shown after next simulation.*


1-2
ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLE...
File View Source Process Options Window Tools Help
Strategy Normal
Sources in Project:
Shaft Encoded Tachometer
tach.wri
ispLSI2064VE-200LJ44
sym1.abv
topl
Processes for Current Source:
Compile Test Vectors
Compiler Listing
Functional Simulation
Timing Simulation
Double-clic
New...
Ready
Simulator Control Panel - SYM1
File Signals Simulate View Tools Help

Step Interval: 100.0ns Run to Time: 384100.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
```

For Help, press F1 Time: 0.0 ns Mode: Unit Delay


Simulator Control Panel - SYM1
File Signals Simulate View Tools Help
Waveform Viewer - SYM1
File Edit View Object Tools Options Jump Help
502,000.0 ns
0
200,000
CLK
P90
P0
CW
CCW
D9
D8
D7
4

Step Interval: 100.0ns Run to Time: 384100.0 ns

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 384,100.0 ns
Simulating to time 812000 ...
Simulating to time 1625000 ..
Simulating to time 2426000 ..
Simulating to time 3233000 ..
Operation RUN ends.
```

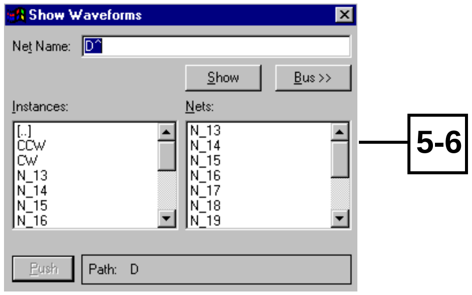
For Help, press F1

Time = 0.0 ns

# Run Functional Simulation and View Simulation Results (continued)

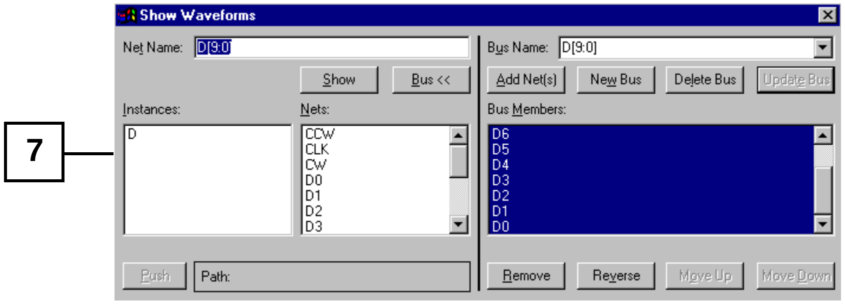
5. If you want to add more waveforms to the Waveform Viewer window to view, you can select **Edit** ⇒ **Show** command and Show Waveforms dialog box appears.
6. The Instances list box initially displays the top level of the hierarchy. Clicking **Push** displays the hierarchical level (if any) below the top level. All signals at a given level are shown in the Nets list box. To add a signal to the display, click on its name, then click the **Show** button. (Or just double-click on the signal's name.) The signal with its waveform is immediately added at the bottom of the Waveform Viewer display.
7. If you want to combine two or more signals into a "bus" display, multi-select the signals you want to create for a bus, choose **Edit** ⇒ **Add to Bus**, the Show Waveforms dialog box appears. You can manually edit the Bus Member list and specify the bus name as you want.
8. Save or update your changes to the bus, then click on the **Show** button to add the bus to the Waveform Viewer display.

*__Tip__: The __View__ commands change the horizontal time dimension. Different time segments of the displayed waveforms can be viewed. The commands of __Zoom In / Zoom Out / Pan / Full Fit__ and the Scroll Bars help you to manipulate the waveform display area.*



Net Name: D*

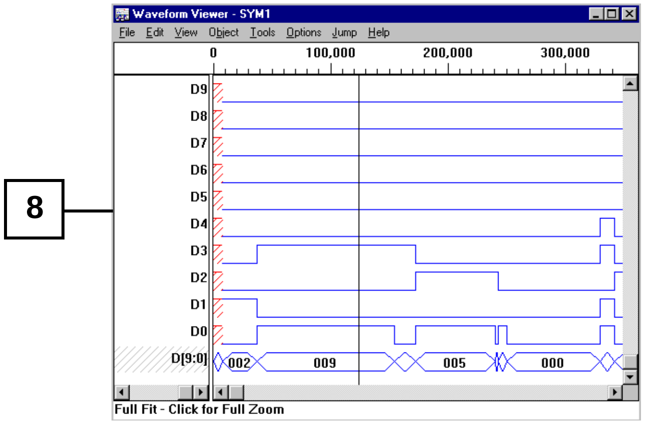
Path: D



Net Name: D[9:0]

Bus Name: D[9:0]

Path:



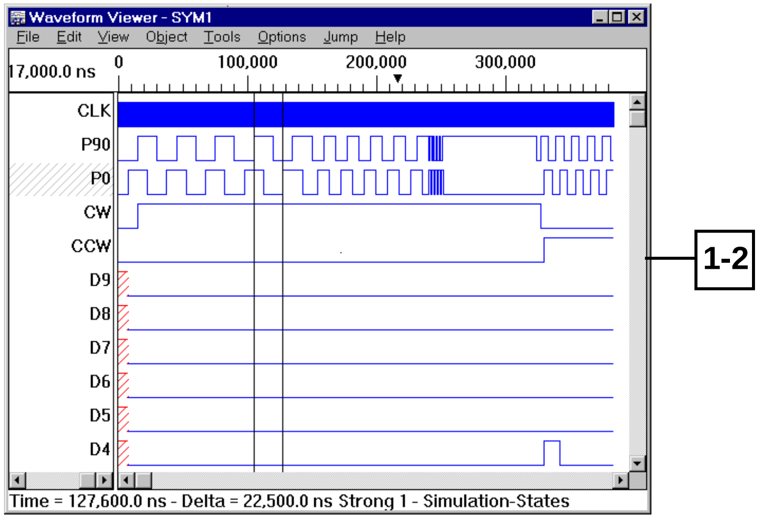
# Task 4 *Analyze Simulation Results*

*To view logic level and time measurements:*

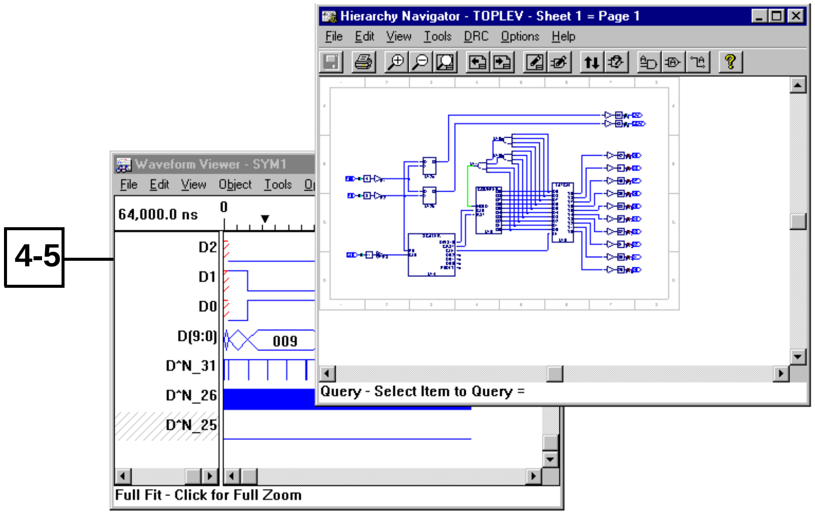
1. Select **Object ⇒ Query,** click on the waveform you want to query. The prompt line display the time and logic level at the cursor position.
2. Move the query cursor to the first event, set the Marker at this location with the **Place Marker** command; Move the query cursor to the second event. The relative time between these two events is shown on the prompt line under the heading ‘Delta’.

*To cross-probe:*

3. In the Project Navigator, select a schematic source.
4. Double-click **Hierarchy Navigator** in the Processes window of the Project Navigator when the Waveform Viewer is running.
5. Select **Tools ⇒ Probe Item**, then click on the desired net in the Hierarchy Navigator and the waveform for that net is added to the display.
6. The logic values determined during simulation are displayed on the schematic loaded in the Hierarchy Navigator. As the query cursor is clicked at different points along the time line, the logic values on the schematic change to those for that simulation time.



Time = 127,600.0 ns - Delta = 22,500.0 ns Strong 1 - Simulation-States


Hierarchy Navigator - TOPLEV - Sheet 1 = Page 1
File Edit View Tools DRC Options Help
Waveform Viewer - SYM1
File Edit View Object Tools O
64,000.0 ns
0
D2
D1
D0
D[9:0]
009
D^N_31
D^N_26
D^N_25
4-5

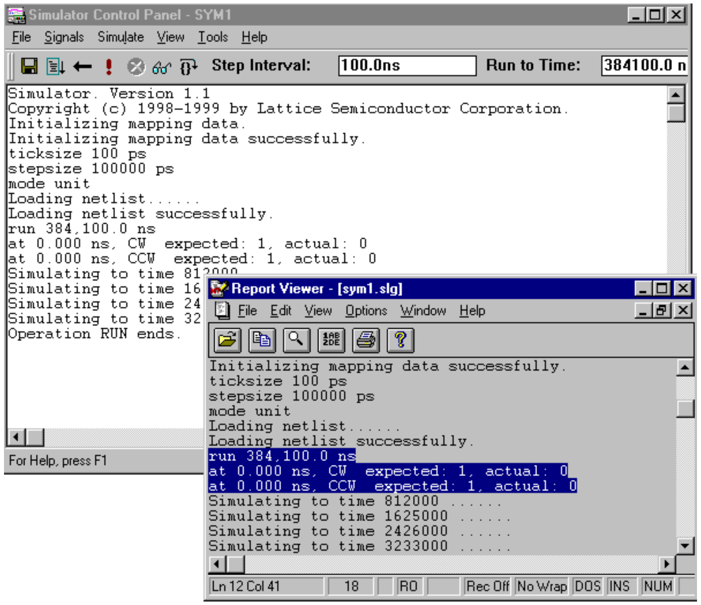
Query - Select Item to Query =

Full Fit - Click for Full Zoom

# Task 5 *Compare Simulation Results with Expected Values*

You can specify the expected values in the `.abv` or `.abl` file for functional simulation. If the actual simulation results are different from the expected values, the Lattice Logic Simulator will display the simulation time, signal name, expected value, and actual value in the Simulator Control Panel window.

The message can also be viewed through the log file that you can access from **View** ⇒ **Simulator Log** in the Simulator Control Panel. Choosing this menu item opens the Report Viewer.


Simulator Control Panel - SYM1
File Signals Simulate View Tools Help
Step Interval: 100.0ns
Run to Time: 384100.0 n
For Help, press F1
Report Viewer - [sym1.slg]
File Edit View Options Window Help
Ln 12 Col 41
18
RO
Rec Off
No Wrap
DOS
INS
NUM

```
Simulator. Version 1.1
Copyright (c) 1998-1999 by Lattice Semiconductor Corporation.
Initializing mapping data.
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 384,100.0 ns
at 0.000 ns, CW  expected: 1, actual: 0
at 0.000 ns, CCW  expected: 1, actual: 0
Simulating to time 812000
Simulating to time 16
Simulating to time 24
Simulating to time 32
Operation RUN ends.
```

```
Initializing mapping data successfully.
ticksize 100 ps
stepsize 100000 ps
mode unit
Loading netlist......
Loading netlist successfully.
run 384,100.0 ns
at 0.000 ns, CW  expected: 1, actual: 0
at 0.000 ns, CCW  expected: 1, actual: 0
Simulating to time 812000 ......
Simulating to time 1625000 ......
Simulating to time 2426000 ......
Simulating to time 3233000 ......
```

# Task 6 *Interactively Debug the Design and Rerun Simulation*

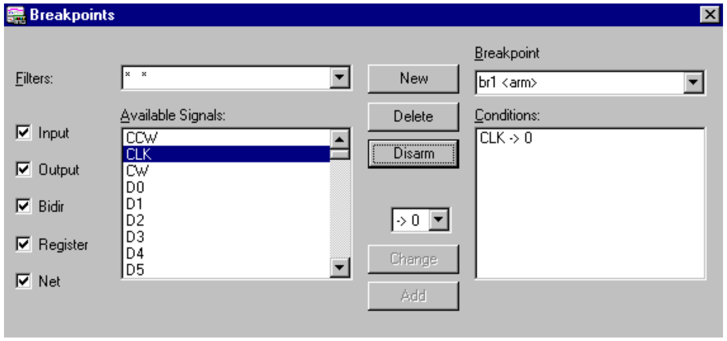
The Lattice Logic Simulator has a full set of interactive features. These features allow you to single-step your design, force and preset signals, and set breakpoints as you debug your design.

The **Signals** ⇒ **Next Test Vector(s)** command in the Simulator Control Panel enables you to do simulation if there are more than one `test_vectors` sections defined in a `.abv` file. Choose the menu item, the simulator starts to read the next `test_vectors` section. Click **Run** to start simulation with the next `test_vectors`.

Breakpoints allow you to stop simulation when a set of signals reach the predefined states. The Breakpoints dialog on the top of the right column of this page allows you to create new breakpoints, edit an existing breakpoint, and arm/disarm breakpoints. You can create breakpoints at any time during the simulation. You can also arm/disarm breakpoints interactively.

*To single-step the design after resetting the simulator:*

1. In the Simulator Control Panel, type 200ns into the Step Interval edit box.
2. Click the **Step** icon or select **Simulate** ⇒ **Step** several times. Each time you step, the simulation advances 200ns in the Simulator Control Panel window. The Waveform Viewer is displayed simultaneously to show the simulation results.



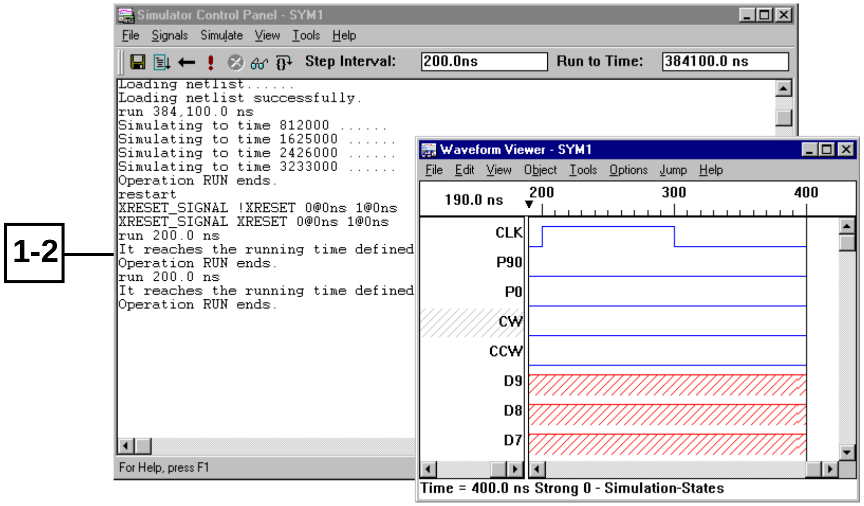
Filters: * *

☑ Input
☑ Output
☑ Bidir
☑ Register
☑ Net

-> 0

Breakpoint: br1 <arm>

Conditions: CLK -> 0


1-2
Simulator Control Panel - SYM1
File Signals Simulate View Tools Help
Waveform Viewer - SYM1
File Edit View Object Tools Options Jump Help
200
300
400
CLK
P90
P0
CW
CCW
D9
D8
D7

Step Interval: 200.0ns

Run to Time: 384100.0 ns

```
Loading netlist......
Loading netlist successfully.
run 384,100.0 ns
Simulating to time 812000 ......
Simulating to time 1625000 ......
Simulating to time 2426000 ......
Simulating to time 3233000 ......
Operation RUN ends.
restart
XRESET_SIGNAL !XRESET 0@0ns 1@0ns
XRESET_SIGNAL XRESET 0@0ns 1@0ns
run 200.0 ns
It reaches the running time defined
Operation RUN ends.
run 200.0 ns
It reaches the running time defined
Operation RUN ends.
```

For Help, press F1

190.0 ns

Time = 400.0 ns Strong 0 - Simulation-States

# Interactively Debug the Design and Rerun Simulation (continued)

Forcing a signal allows you to set its state to a specified value regardless of how it is being driven by the circuit. Presetting a signal momentarily forces a signal to a specified value and then allows the circuitry to take over driving it.

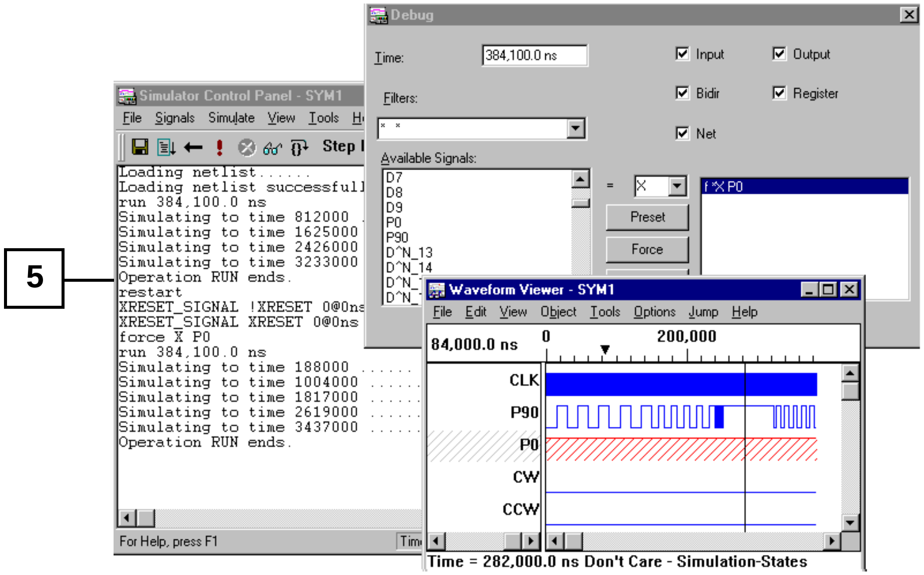
*To force a signal:*

1. Select **Signals** ⇒ **Debug** from the Simulator Control Panel to open the Debug dialog.
2. In the Available Signals list box, highlight `P0`.
3. In the drop-down list beside "=", choose a desired signal state, for example, `X` (Don't Care).
4. Click the **Force** button. The signal appears in the list box on the right field, along with the designation `f X`.

   `f` means forced; `X` indicates the desired state which the signal will be forced to.
5. Click the **Run** icon or select **Simulate** ⇒ **Run** to rerun the simulation.

   The signal `P0` appears in `X` state in the Waveform Viewer window.

***Note**: If there is only one `test_vectors` section in the ABEL test vector file, you need to reset the simulator before you can force a signal. If there are more than one `test_vectors` sections, you can force a signal in the next `test_vectors` without resetting the simulator.*


5
Simulator Control Panel - SYM1
File Signals Simulate View Tools H
Step
Debug
Preset
Force
Waveform Viewer - SYM1
File Edit View Object Tools Options Jump Help
84,000.0 ns
0
200,000
CLK
P90
P0
CW
CCW
For Help, press F1
Tim

```
Loading netlist......
Loading netlist successfull
run 384,100.0 ns
Simulating to time 812000 .
Simulating to time 1625000
Simulating to time 2426000
Simulating to time 3233000
Operation RUN ends.
restart
XRESET_SIGNAL !XRESET 0@0ns
XRESET_SIGNAL XRESET 0@0ns
force X P0
run 384,100.0 ns
Simulating to time 188000 ......
Simulating to time 1004000 .....
Simulating to time 1817000 .....
Simulating to time 2619000 .....
Simulating to time 3437000 .....
Operation RUN ends.
```

Time: 384,100.0 ns

☑ Input ☑ Output

☑ Bidir ☑ Register

☑ Net

Filters: * *

Available Signals:

D7
D8
D9
P0
P90
D^N_13
D^N_14
D^N_
D^N_

= X

f *X P0

Time = 282,000.0 ns Don't Care - Simulation-States

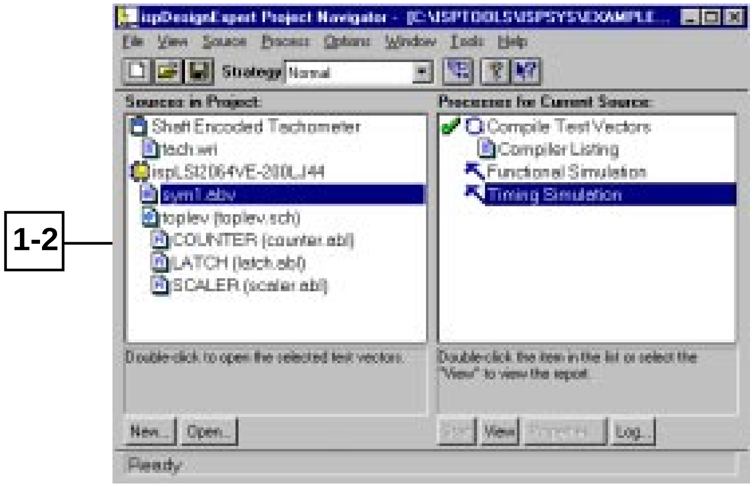
# Task 7 *Run Timing Simulation*

After successfully completing placement and routing in the Compile Design process, ispDesignExpert generates a timing netlist for timing simulation. Timing simulation then proceeds very much as it does for functional simulation.

*To run timing simulation:*

1. In Sources window, select the test stimulus (`.abv` or `.wdl` file).
2. In the Processes window, double-click the Timing Simulation process.
3. The Simulator Control Panel is displayed.

   You can run the simulation and view the simulation results as described in **Task3, "Run Functional Simulation and View Simulation Results."**



Strategy: Normal

Sources in Project:
- Shaft Encoded Tachometer
- tach.wri
- ispLSI2064VE-200LJ44
- sym1.abv
- toplev (toplev.sch)
- COUNTER (counter.abl)
- LATCH (latch.abl)
- SCALER (scaler.abl)

Processes for Current Source:
- ✓ Compile Test Vectors
- Compiler Listing
- Functional Simulation
- Timing Simulation

Double-click to open the selected test vectors.

Double-click the item in the list or select the "View" to view the report.

Ready

# Task 8 *Run the Stand-alone Simulator*

The Lattice Logic Simulator can be invoked in its stand-alone mode by selecting **Tools** ⇒ **Lattice Logic Simulator** from the Project Navigator. The stand-alone simulator enables you to simulate a design or stimulus file outside the current project.

*To run the stand-alone mode simulator:*

1. Select **Tools** ⇒ **Lattice Logic Simulator** from the Project Navigator. The Simulator Control Panel appears in its stand-alone mode.
2. Select **File** ⇒ **Open Design** from the Simulator Control Panel. The Open Design dialog displays.
3. In the Files of type field, select the type of design you want to open.
    - For functional simulation, choose design file `*.edn` or `*.edf`
    - For timing simulation, choose design file `*.sim`

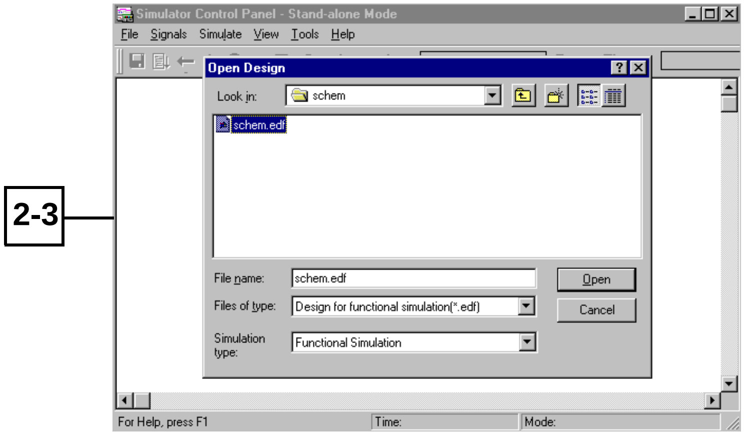
   Select the desired file in the file list window, and click **Open**. The design file is loaded into the Simulator Control Panel window.

***Note**: The **Open Stimulus** command will not be enabled until you have opened a design file.*

4. Select **File** ⇒ **Open Stimulus**, and the Open Stimulus dialog displays.
5. Select a stimulus file (`*.wdl`, `*.abv`, or `*.abl`) and click **Open** to load the stimulus file into the Simulator Control Panel.

***Tip**: The stimulus file must be in the same directory with the loaded design file.*

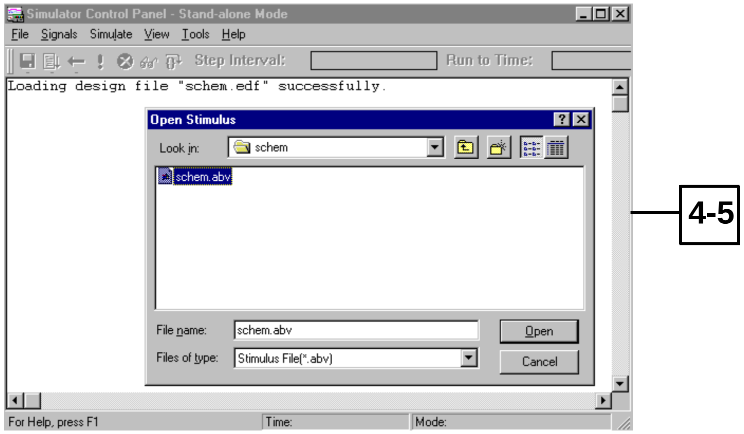
A message “Loading netlist successfully” appears in the Simulator Control Panel window. You can start the simulation as described in the previous tasks.


2-3
Simulator Control Panel - Stand-alone Mode
File Signals Simulate View Tools Help
Open Design
Look in:
schem
schem.edf
Open
Cancel
For Help, press F1
Time:
Mode:

File name: schem.edf

Files of type: Design for functional simulation(*.edf)

Simulation type: Functional Simulation



```
Loading design file "schem.edf" successfully.
```

File name: schem.abv

Files of type: Stimulus File(*.abv)

# Congratulations!

You have completed the Simulating a Design with Lattice Logic Simulator tutorial. In this tutorial you have learned how to:

- create a new project.
- create an ABEL test vector file.
- create a graphic waveform stimulus.
- run functional simulation.
- analyze the simulation results with the Waveform Viewer and the Hierarchy Navigator.
- compare the functional simulation results with the expected values.
- use interactive features to debug the design and rerun simulation.
- run timing simulation.
- run the stand-alone simulator.

# Tutorial 12   Simulating a Design with ModelSim

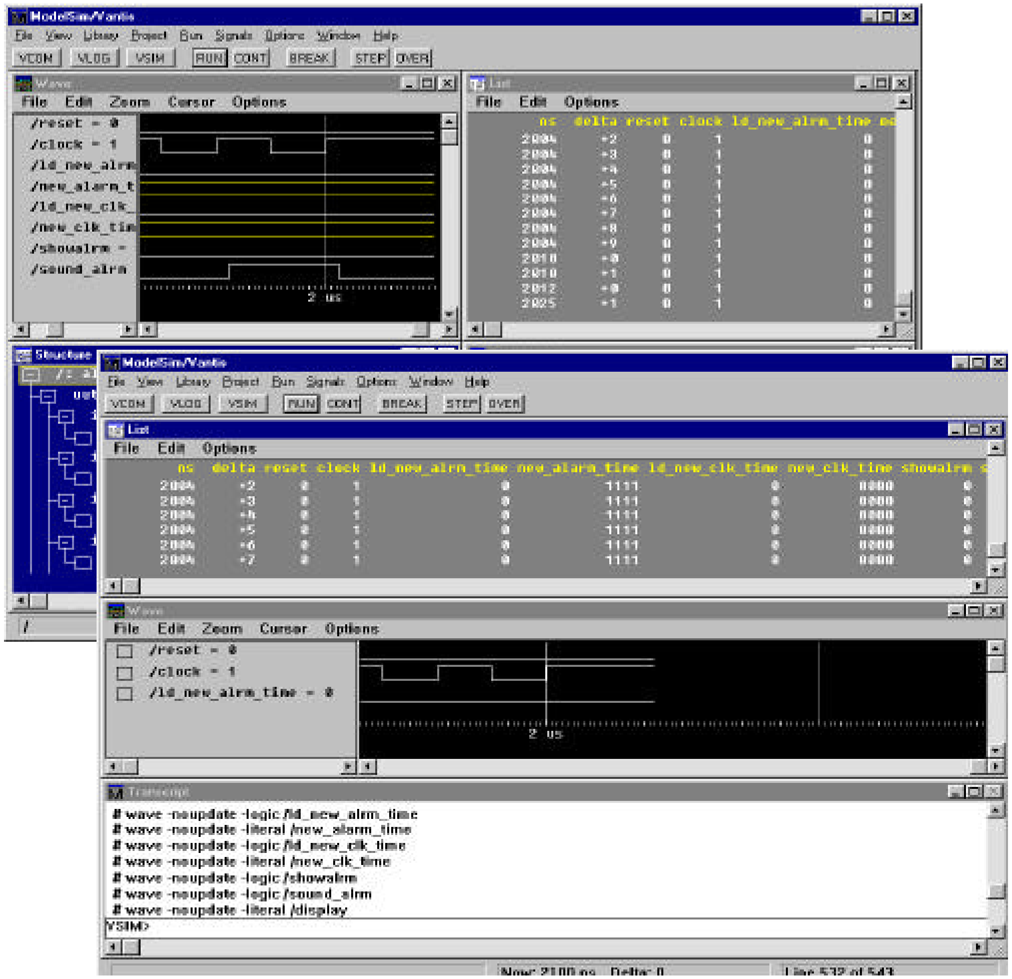
This tutorial shows you how to simulate a gate-level netlist for a Lattice CPLD device after it has been implemented with ispDesignExpert. This tutorial uses a MACH device, begins with a completed VHDL design, and ends when the gate-level netlist file is simulated using Model*Sim.*

## Learning Objectives

When you are finished with this tutorial, you should know how to generate a VHDL netlist and SDF file in ispDesignExpert. You will also understand how to import these files to ModelSim, run a simulation, and view the results.

## Time to Complete This Tutorial

The time to complete this tutorial is about 30 minutes.


ModelSim/Vantis
File View Library Project Run Signals Options Window Help
VCOM VLOG VSIM RUN CONT BREAK STEP OVER
Wave
File Edit Zoom Cursor Options
/reset = 0
/clock = 1
/ld_new_alrm
/new_alarm_t
/ld_new_clk_
/new_clk_tim
/showalrm =
/sound_alrm
2 us
List
File Edit Options
Structure
ModelSim/Vantis
File View Library Project Run Signals Options Window Help
VCOM VLOG VSIM RUN CONT BREAK STEP OVER
List
File Edit Options
Wave
File Edit Zoom Cursor Options
/reset = 0
/clock = 1
/ld_new_alrm_time = 0
2 us
Transcript

```
      ns  delta reset clock ld_new_alrm_time ne
    2004     +2     0     1                0
    2004     +3     0     1                0
    2004     +4     0     1                0
    2004     +5     0     1                0
    2004     +6     0     1                0
    2004     +7     0     1                0
    2004     +8     0     1                0
    2004     +9     0     1                0
    2010     +0     0     1                0
    2010     +1     0     1                0
    2012     +0     0     1                0
    2025     +1     0     1                0
```

```
      ns  delta reset clock ld_new_alrm_time new_alarm_time ld_new_clk_time new_clk_time showalrm s
    2004     +2     0     1                0           1111               0         0000        0
    2004     +3     0     1                0           1111               0         0000        0
    2004     +4     0     1                0           1111               0         0000        0
    2004     +5     0     1                0           1111               0         0000        0
    2004     +6     0     1                0           1111               0         0000        0
    2004     +7     0     1                0           1111               0         0000        0
```

```
# wave -noupdate -logic /ld_new_alrm_time
# wave -noupdate -literal /new_alarm_time
# wave -noupdate -logic /ld_new_clk_time
# wave -noupdate -literal /new_clk_time
# wave -noupdate -logic /showalrm
# wave -noupdate -logic /sound_alrm
# wave -noupdate -literal /display
VSIM>
```

Now: 2100 ns   Delta: 0   Line 532 of 543

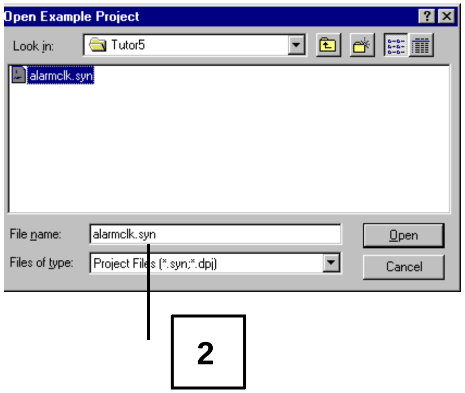
# Task 1 *Create a Structural Netlist in ispDesignExpert*

Before beginning your final verification after a design has been implemented, you must create a simulation netlist.

From the ispDesignExpert program you can output VHDL or Verilog gate-level netlists and Standard Delay Format (SDF) files. These netlists can then be simulated in ModelSim using MACH primitive libraries provided with ispDesignExpert and a user created test bench.

*To create simulation input files*:

1. Start ispDesignExpert, if it is not already running.
2. Choose **File** ⇒ **Open Example** and open the `..\Mach_pal\Tutorial\Tutor5\alarmclk.syn` file.
3. In the Sources window, select the target device. Double-click **Fit Design** in the Processes window.
4. Now you want to create the post-fit timing simulation files. Choose **Tools** ⇒ **Generate Timing Simulation Options**. This dialog lets you specify the format of the simulation file. Leave the default options (VHDL and SDF) and click **OK**.
5. In the Processes window, double-click **Generate Timing Simulation Files**. ispDesignExpert creates two files that you will use later to simulate the design: `alarmclk.vho` (VHDL net list file) and `alarmclk.sdf` (timing delay file).

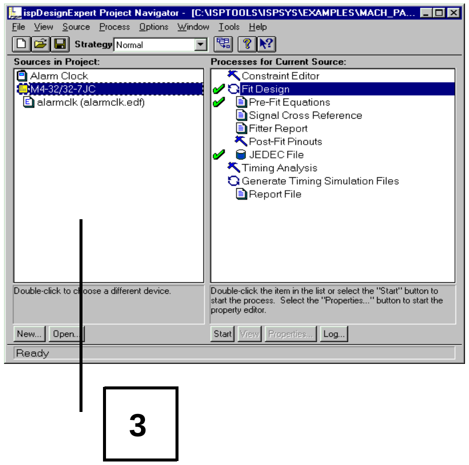


Look in: Tutor5

alarmclk.syn

File name: alarmclk.syn

Files of type: Project Files (*.syn;*.dpj)


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\MACH_PA...
File View Source Process Options Window Tools Help
New... Open...
Start View Properties... Log...
3

Strategy: Normal

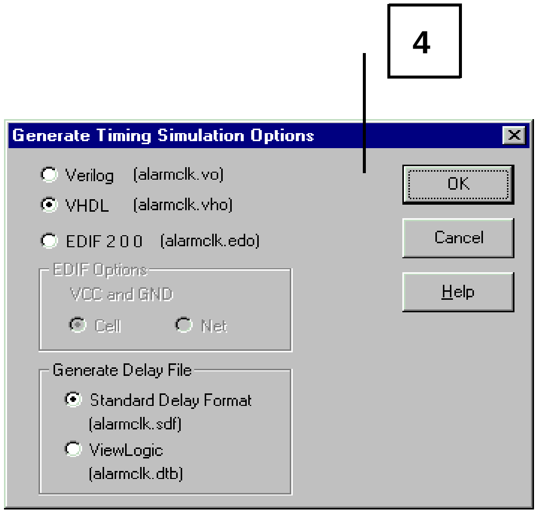
Sources in Project:
- Alarm Clock
- M4-32/32-7JC
- alarmclk (alarmclk.edf)

Processes for Current Source:
- Constraint Editor
- ✓ Fit Design
- ✓ Pre-Fit Equations
- Signal Cross Reference
- Fitter Report
- Post-Fit Pinouts
- ✓ JEDEC File
- Timing Analysis
- Generate Timing Simulation Files
- Report File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

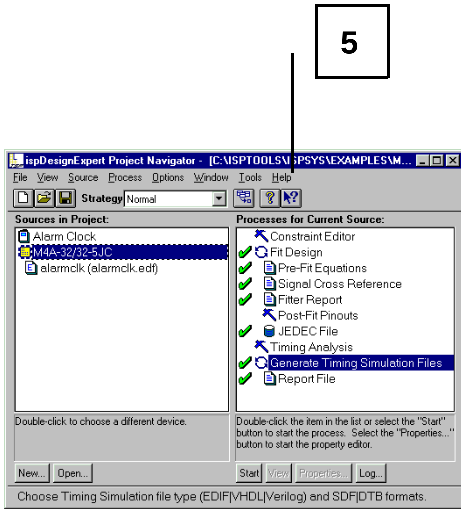
Ready



○ Verilog (alarmclk.vo)
● VHDL (alarmclk.vho)
○ EDIF 2 0 0 (alarmclk.edo)

EDIF Options
VCC and GND
● Cell ○ Net

Generate Delay File
● Standard Delay Format (alarmclk.sdf)
○ ViewLogic (alarmclk.dtb)


ispDesignExpert Project Navigator - [C:\ISPTOOLS\ISPSYS\EXAMPLES\M...
File View Source Process Options Window Tools Help
New... Open...
Start View Properties... Log...
5

Strategy: Normal

Sources in Project:
- Alarm Clock
- M4A-32/32-5JC
- alarmclk (alarmclk.edf)

Processes for Current Source:
- Constraint Editor
- ✓ Fit Design
- ✓ Pre-Fit Equations
- ✓ Signal Cross Reference
- ✓ Fitter Report
- Post-Fit Pinouts
- ✓ JEDEC File
- Timing Analysis
- ✓ Generate Timing Simulation Files
- ✓ Report File

Double-click to choose a different device.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Choose Timing Simulation file type (EDIF|VHDL|Verilog) and SDF|DTB formats.

# Task 2 *Start ModelSim and Create a Project*

*To start ModelSim*:

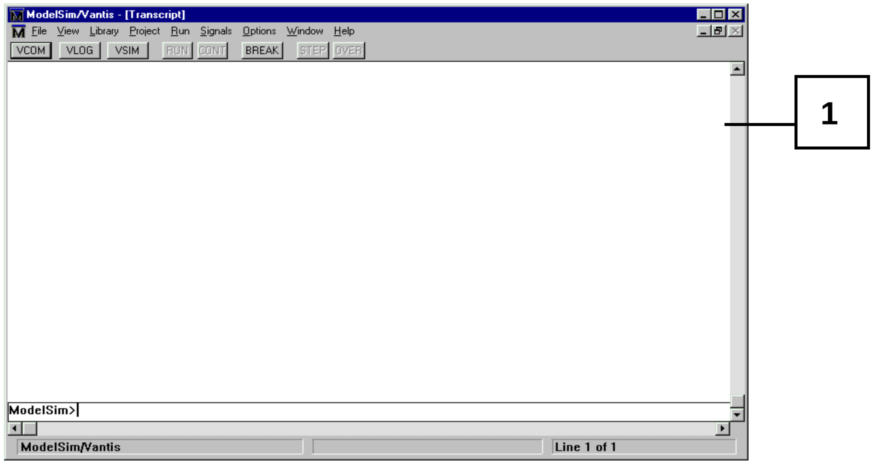
1. In ispDesignExpert, choose **Tools** ⇒ **ModelSim Simulator**. ModelSim starts with the Transcript window open. Maximize the Transcript window.
2. Change to your design directory. Choose **File** ⇒ **Directory** to open the dialog. You should be in the `..\Mach_pal\Tutorial\Tutor5` directory. Click **OK**.
3. Now you need to create a new project file in your working directory. This project file will remember things about your environment (such as window sizes and positions, simulation options, etc.), so that next time you work in this directory, ModelSim will automatically reload your environment for you. Choose **Project** ⇒ **New**. In the dialog, type `modelsim.ini`, and then click **Create**. ModelSim sets the project file to the specified path.

***Note:** ModelSim automatically loads a new project file when you change directories. If there is a modelsim.ini file in the directory you change to, it will be loaded. If there is not one there, the original modelsim.ini file will be loaded. Therefore, to avoid overwriting the original modelsim.ini file, it is important that you create a new file.*

4. Before you can compile a VHDL source file, you need to create a design library to hold the compilation results. Choose **Library** ⇒ **New**. In the dialog, type **work**, and then click **Create**.

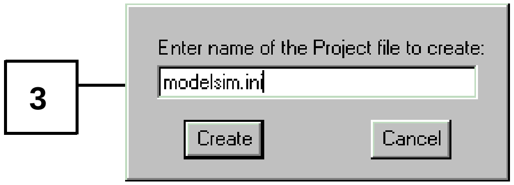
   This creates a VHDL library named *work* under the current directory.

***Note**: To create a library folder, you must use the previous step. You cannot use the DOS "mkdir" command or Microsoft Windows to create this directory.*

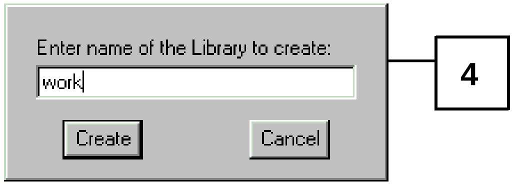


```
ModelSim>
```

ModelSim/Vantis | Line 1 of 1



Enter name of the Project file to create: modelsim.ini



Enter name of the Library to create: work

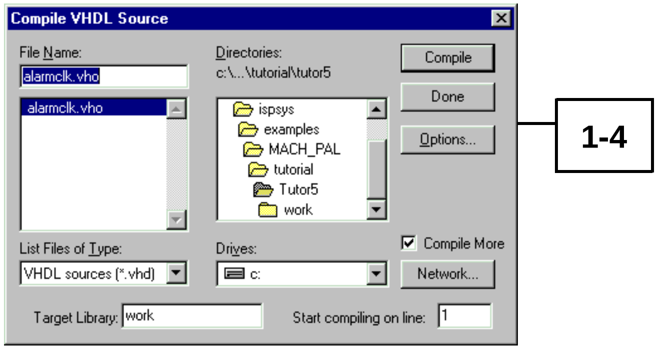
# Task 3 *Compile the Design*

Now you are ready to compile the design. ModelSim compiles one or more VHDL design units with a single invocation of VCOM, the VHDL compiler. The design units are compiled in the order that they appear on the command line. For VHDL, the order of compilation is important – you must compile any entities or configurations before an architecture that references them.

In this tutorial, there are two files that you will compile: `alarmclk.vho`, the VHDL netlist file, and `alarmclk_TB.vhd`, the test bench file.

*To compile the design*:

1. Choose **File** ⇒ **Compile VHDL** to open the dialog.
2. In the File Name field, type `*.vho` and press **Enter** to view the files.
3. Select the `alarmclk.vho` file and click **Compile** to invoke VCOM, the Model Technology VHDL compiler.
4. When the process is complete, click **Done** to close the dialog.
5. Now you have to compile the test bench file. Choose **File** ⇒ **Compile VHDL** to open the dialog again.
6. Select the `alarmclk_TB.vhd` file and click **Compile**.
7. When the process is complete, click **Done** to close the dialog.



Compile VHDL Source

File Name: alarmclk.vho

alarmclk.vho

Directories: c:\...\tutorial\tutor5

ispsys, examples, MACH_PAL, tutorial, Tutor5, work

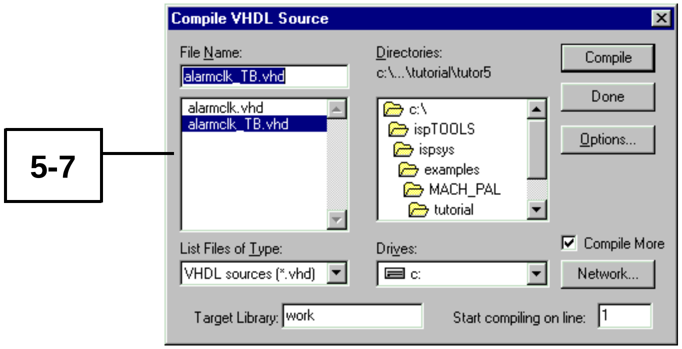
List Files of Type: VHDL sources (*.vhd)

Drives: c:

☑ Compile More

Target Library: work

Start compiling on line: 1



Compile VHDL Source

File Name: alarmclk_TB.vhd

alarmclk.vhd
alarmclk_TB.vhd

Directories: c:\...\tutorial\tutor5

c:\, ispTOOLS, ispsys, examples, MACH_PAL, tutorial

List Files of Type: VHDL sources (*.vhd)

Drives: c:

☑ Compile More

Target Library: work

Start compiling on line: 1

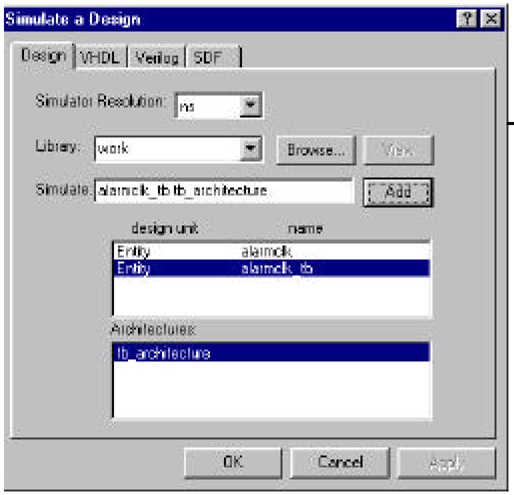
# Task 4 *Prepare to Run the Simulation*

After compiling the design units, you can proceed to simulate your designs with VSIM.

*To start the simulation process*:

1. Choose **File** ⇒ **Simulate** to open the dialog.

   The Simulate a Design dialog has four tabs—Design, VHDL, Verilog, and SDF—that let you select various simulation options.
2. On the Design tab, select the test bench design unit, **alarmclk_tb**.
3. Click **Add** to add the test bench file and the architecture to the timing simulation.
4. On the SDF tab, click **Browse** and select the timing delay file, `..\Tutor5\alarmclk.sdf`.
5. Click **Open** to add the timing delay file to the timing simulation.
6. The Apply to Region field lets you specify the design region to use with the selected SDF options. Type a design module instantiation label: **/UUT**.
7. Click **OK**.



Simulator Resolution: ns

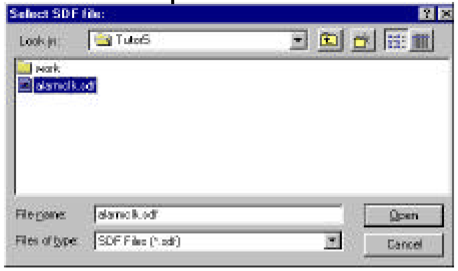
Library: work

Simulate: alarmclk_tb tb_architecture

| design unit | name |
|---|---|
| Entity | alarmclk |
| Entity | alarmclk_tb |

Architectures:

tb_architecture



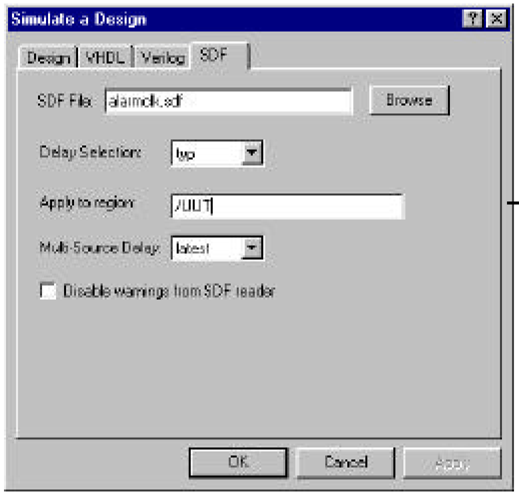
Look in: Tutor5

work

alarmclk.sdf

File name: alarmclk.sdf

Files of type: SDF Files (*.sdf)



SDF File: alarmclk.sdf

Delay Selection: typ

Apply to region: /UUT

Multi-Source Delay: latest

□ Disable warnings from SDF reader

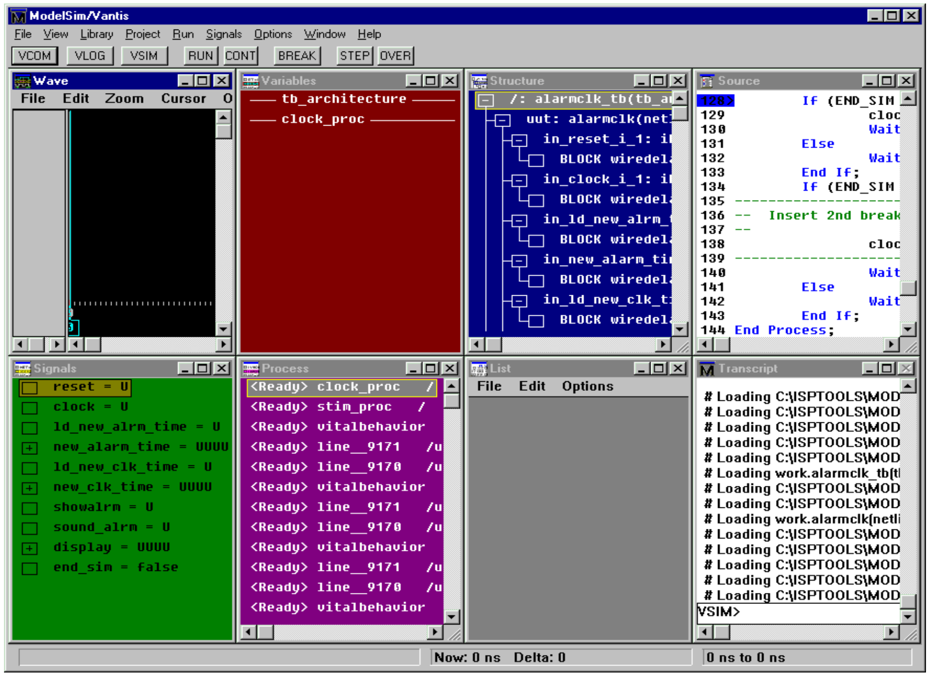
# Task 5 Set up the Windows to View the Results of the Simulation

In addition to the Transcript window, the ModelSim application window also accommodates seven other windows for use during your design compilation, simulation, and debugging. They are the List, Signals, Source, Structure, Process, Variables, and Wave windows.

*To open all windows:*

1. Maximize the ModelSim application.
2. Choose **View** ⇒ **All** to open all of the ModelSim windows.
3. Choose **Window** ⇒ **Tile Vertically** to organize the windows.

***Note**: The windows in your application may not be organized exactly like the picture on the right. That's okay.*



Variables:

```
—— tb_architecture ——
—— clock_proc ——
```

Structure:

```
/: alarmclk_tb(tb_ar
  uut: alarmclk(net
    in_reset_i_1: i
      BLOCK wiredel
    in_clock_i_1: i
      BLOCK wiredel
    in_ld_new_alrm_
      BLOCK wiredel
    in_new_alarm_ti
      BLOCK wiredel
    in_ld_new_clk_t
      BLOCK wiredel
```

Source:

```
128>         If (END_SIM
                    cloc
                    Wait
             Else
                    Wait
             End If;
             If (END_SIM
    -------------------
    --   Insert 2nd break
    --
                    cloc
    -------------------
                    Wait
             Else
                    Wait
             End If;
    End Process;
```

Signals:

```
reset = U
clock = U
ld_new_alrm_time = U
new_alarm_time = UUUU
ld_new_clk_time = U
new_clk_time = UUUU
showalrm = U
sound_alrm = U
display = UUUU
end_sim = false
```

Process:

```
<Ready> clock_proc    /
<Ready> stim_proc    /
<Ready> vitalbehavior
<Ready> line__9171   /u
<Ready> line__9170   /u
<Ready> vitalbehavior
<Ready> line__9171   /u
<Ready> line__9170   /u
<Ready> vitalbehavior
<Ready> line__9171   /u
<Ready> line__9170   /u
<Ready> vitalbehavior
```

Transcript:

```
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading work.alarmclk_tb(t
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading work.alarmclk(netli
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
# Loading C:\ISPTOOLS\MOD
VSIM>
```

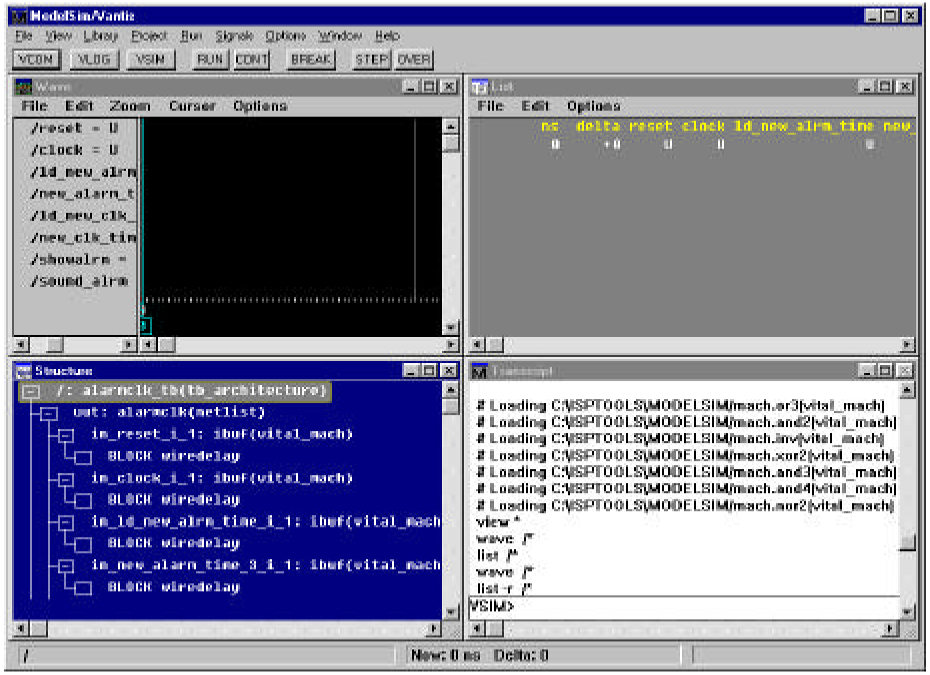
```
Now: 0 ns   Delta: 0
0 ns to 0 ns
```

# Task 6 *Add Signals in Region to Wave and List Windows*

The Wave and List windows let you view the results of your simulation in either waveform or table formats.

*To add signals in region:*

1. Close the **Source**, **Variables**, **Signals**, and **Process** windows.
2. Choose **Window** ⇒ **Tile Vertically** to resize the windows again. Your screen should look something like the one on the right.
3. The Structure window provides a hierarchical view of the structure of your design. A level of hierarchy is created by each HDL item within the design. In the Structure window, select the top-level structure-the test bench (alarmclk_tb).
4. Choose **Signals** ⇒ **Add to Waveform** ⇒ **Signals in Region**. The software displays all signals and nets in the HDL item selected as the current region (alarmclk_tb).
5. Now choose **Signals** ⇒**Add to List** ⇒ **Signals in Region**. The software lists all signals and nets in the HDL item selected as the current region (alarmclk_tb).



```
ns  delta reset clock ld_new_alrm_time new_
 0     +0     U     U                   U
```

```
/: alarmclk_tb(tb_architecture)
  uut: alarmclk(netlist)
    im_reset_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    im_clock_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    im_ld_new_alrm_time_i_1: ibuf(vital_mach
      BLOCK wiredelay
    im_new_alarm_time_3_i_1: ibuf(vital_mach
      BLOCK wiredelay
```

```
# Loading C:\ISPTOOLS\MODELSIM\mach.or3(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.and2(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.inv(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.xor2(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.and3(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.and4(vital_mach)
# Loading C:\ISPTOOLS\MODELSIM\mach.nor2(vital_mach)
view *
wave /*
list /*
wave /*
list -r /*
VSIM>
```

# Task 7 *Specify Simulation Options and Run the Simulation*

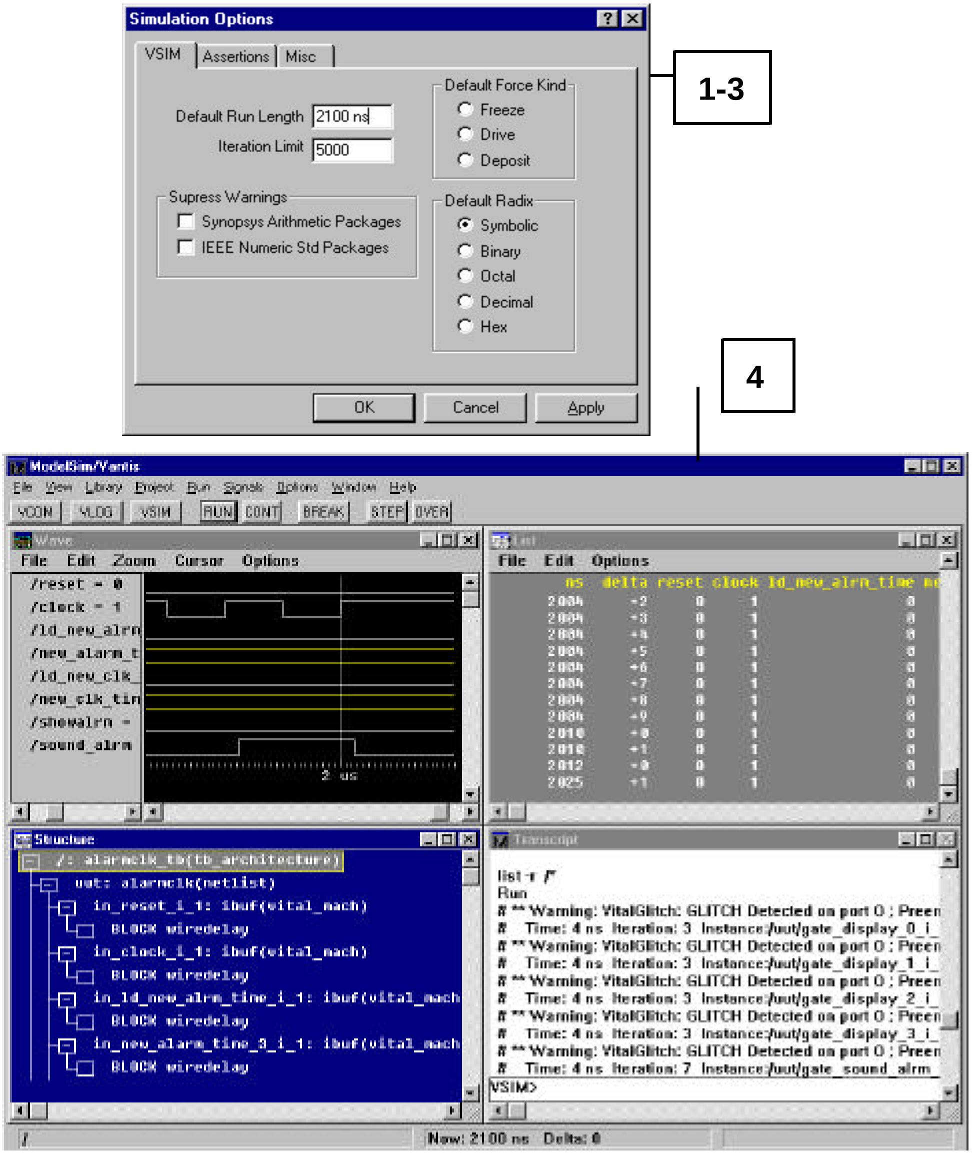
*To specify simulation options*:

1. Choose **Options** ⇒ **Simulation Options** to open the dialog.
2. On the VSIM tab, the Default Run Length is 100 ns. Change this to **2100** ns and click **OK**.
3. A dialog appears asking you "Do you wish to save the new settings in your project file?" Click **Yes**. This saves the setting to the `modelsim.ini` file you created at the beginning of the tutorial.
4. Click **Run**. The **Run** command advances the simulation by the specified number of timesteps (2100 ns).

   Notice the content of the **Wave** and **List** windows has changed.

   The Wave window displays the waveforms of the included signals. The data displayed in this window should match the results you had in your functional simulation, except timing delays have been added.

   Notice that The List window displays the information in table format.



Default Run Length: 2100 ns
Iteration Limit: 5000

Default Force Kind: ○ Freeze ○ Drive ○ Deposit

Supress Warnings: □ Synopsys Arithmetic Packages □ IEEE Numeric Std Packages

Default Radix: ● Symbolic ○ Binary ○ Octal ○ Decimal ○ Hex

```
  ns  delta reset clock ld_new_alrn_time ne
2004    +2    0     1                 0
2004    +3    0     1                 0
2004    +4    0     1                 0
2004    +5    0     1                 0
2004    +6    0     1                 0
2004    +7    0     1                 0
2004    +8    0     1                 0
2004    +9    0     1                 0
2010    +0    0     1                 0
2010    +1    0     1                 0
2012    +0    0     1                 0
2025    +1    0     1                 0
```

```
/: alarmclk_tb(tb_architecture)
  uut: alarmclk(netlist)
    in_reset_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    in_clock_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    in_ld_new_alrm_time_i_1: ibuf(vital_mach
      BLOCK wiredelay
    in_new_alarm_time_3_i_1: ibuf(vital_mach
      BLOCK wiredelay
```

```
list -r /*
Run
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_0_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_1_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_2_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_3_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 7  Instance:/uut/gate_sound_alrm_
VSIM>
```

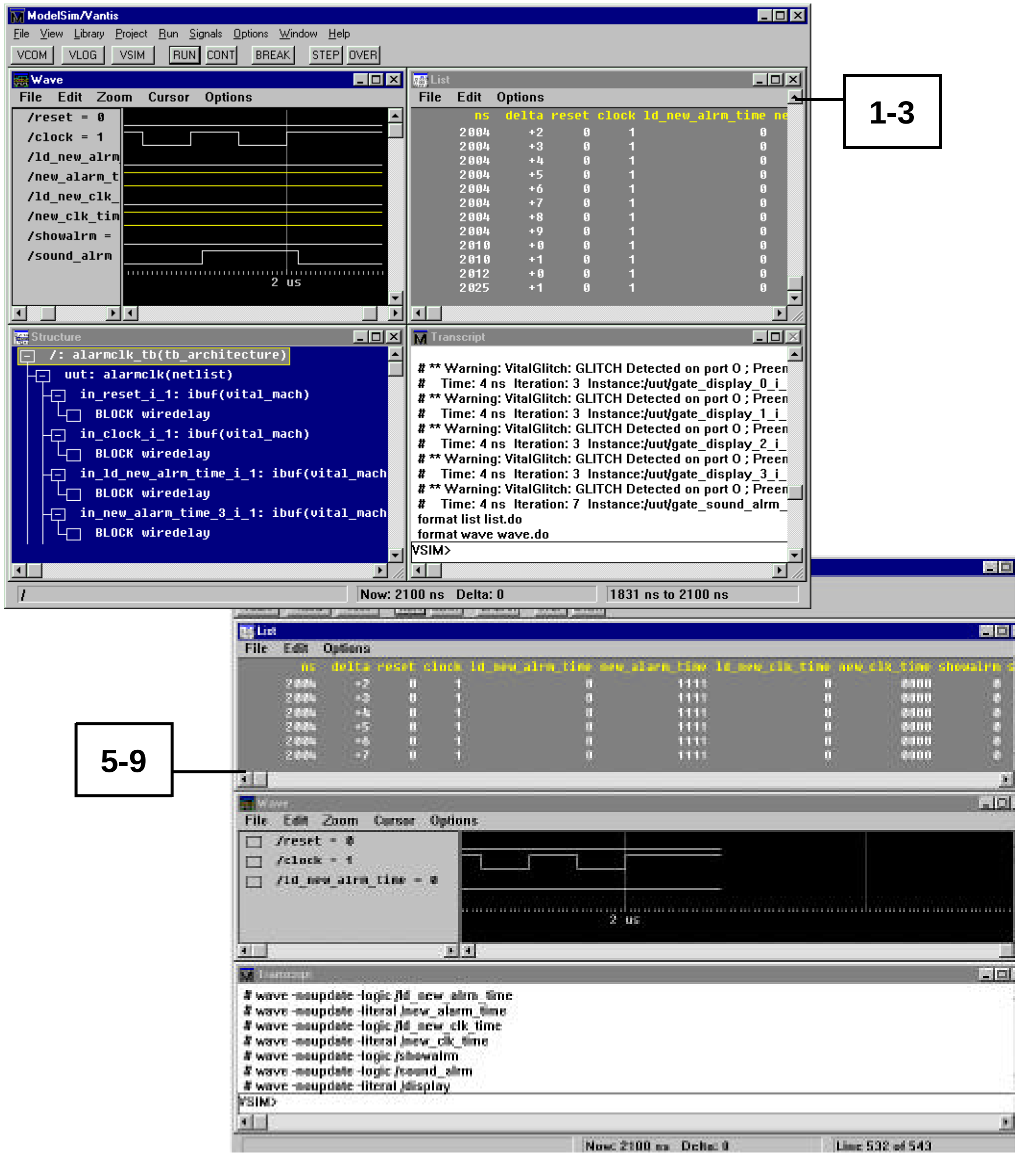
Now: 2100 ns  Delta: 0

# Task 8 *Save the Configuration and Re-run the Simulation*

You can save the List and Wave window configurations. This lets you re-run a simulation more quickly.

*To save the configuration and re-run the simulation*:

1. In the List window, choose **File** ⇒ **Save Configuration** to open the dialog.
2. Make sure you are still in your project directory (Tutor5), and save the file as `list.do`.
3. Follow the same procedure for the Wave window, except name the file `wave.do`.
4. In the main window, choose **File** ⇒ **End Simulation**. Click **Yes** to the question.
5. Now, start a new simulation run using the saved configurations. On the toolbar, click **VSIM** to open the dialog.
6. Add the test bench file (alarmclk_tb) to the simulation and click **OK**.
7. In the Transcript window command line, type **`do list.do`**, and then press **Enter**. The software reloads the saved List configuration.
8. At the command line, type **`do wave.do`**, and then press **Enter**. The software reloads the saved Wave configuration.
9. Click **Run** to run the simulation again. Select **View** ⇒ **List** to view the List window. Notice that the software updates the content of the List and Wave windows.



```
      ns  delta reset clock ld_new_alrm_time ne
    2004     +2     0     1                0
    2004     +3     0     1                0
    2004     +4     0     1                0
    2004     +5     0     1                0
    2004     +6     0     1                0
    2004     +7     0     1                0
    2004     +8     0     1                0
    2004     +9     0     1                0
    2010     +0     0     1                0
    2010     +1     0     1                0
    2012     +0     0     1                0
    2025     +1     0     1                0
```

```
/: alarmclk_tb(tb_architecture)
  uut: alarmclk(netlist)
    in_reset_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    in_clock_i_1: ibuf(vital_mach)
      BLOCK wiredelay
    in_ld_new_alrm_time_i_1: ibuf(vital_mach
      BLOCK wiredelay
    in_new_alarm_time_3_i_1: ibuf(vital_mach
      BLOCK wiredelay
```

```
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_0_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_1_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_2_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 3  Instance:/uut/gate_display_3_i_
# ** Warning: VitalGlitch: GLITCH Detected on port O ; Preen
#    Time: 4 ns  Iteration: 7  Instance:/uut/gate_sound_alrm_
format list list.do
format wave wave.do
VSIM>
```

/ Now: 2100 ns Delta: 0 1831 ns to 2100 ns

```
      ns  delta reset clock ld_new_alrm_time new_alarm_time ld_new_clk_time new_clk_time showalrm s
    2004     +2     0     1                0           1111               0         0000        0
    2004     +3     0     1                0           1111               0         0000        0
    2004     +4     0     1                0           1111               0         0000        0
    2004     +5     0     1                0           1111               0         0000        0
    2004     +6     0     1                0           1111               0         0000        0
    2004     +7     0     1                0           1111               0         0000        0
```

```
# wave -noupdate -logic /ld_new_alrm_time
# wave -noupdate -literal /new_alarm_time
# wave -noupdate -logic /ld_new_clk_time
# wave -noupdate -literal /new_clk_time
# wave -noupdate -logic /showalrm
# wave -noupdate -logic /sound_alrm
# wave -noupdate -literal /display
VSIM>
```

Now: 2100 ns Delta: 0 Line: 532 of 543

# *Congratulations!*

You have completed the Simulating a Design with ModelSim tutorial. In this tutorial you have learned how to:

- create a structural netlist in ispDesignExpert.
- start ModelSim and create a project.
- compile the design.
- prepare to run the design.
- set up the windows to view the results of the simulation.
- add signals in region to the Wave and List windows.
- specify simulation options and run the simulation.
- save the configuration and re-run the simulation.