MOTOROLA

Microprocessor and Memory Technologies Group

Order this document by MC68306UMAD/AD

MC68306

ADDENDUM TO
MC68306 Integrated EC000 Processor User's Manual

September 8, 1995

This addendum to the initial release of the MC68306UM/AD User's Manual provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the AESOP BBS, which can be reached at (800)843-3451 (from the US and Canada) or (512)891-3650. Configure the modem for up to 14.4K baud, 8 bits, 1 stop bit, and no parity. Terminal software should support VT100 emulation. Internet access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

1. Reset and Three-State Outputs

In the signal summary tables beginning page 2-3, most outputs which three-state during bus arbitration also three-state during reset. The DRAM control signals in Table 2-3 on page 2-3 are the exception - these signals are three-stated during reset, but periodically drive for refresh cycles to keep DRAM data alive. The DRAM control signals do not drive for refreshes during bus arbitration, and alternate master tenures greater than the refresh period may result in lost refresh cycles. Use pullups as indicated to keep three-stated signals from inadvertently accessing memory during either bus arbitration or reset.

2. Pullup Recommendations

The pullup resistor recommendations in the signal summary tables beginning page 2-3 are intended as general guidelines only - the specific values shown can be modified to suit individual applications. The values shown were selected to provide reasonable rise times while remaining within DC IOL drive limits.

3. Halt and Three-State Outputs

For section 3.4.3 Halt Operation on page 3-26, the bus interface is in an inactive state during halt. The data bus three-states, and other outputs remain driven.

4. Bus Description Error

In Figure 3-27 on page 3-28, the reset time should be 132 clocks minimum. Also, the note that all control signals go inactive is wrong - all bus control signals, address bus, data bus, etc. go to a high impedance state during reset. The address bus on the MC68306 does not go high impedance between bus cycles, as shown in all bus timing diagrams in Section 3.

5. Crystal Oscillator Recommendations

Crystals for either the CPU oscillator or the serial module oscillator should be specified for parallel resonant operation, with series resistance less than 80Ω.

6. DC Electrical Specifications

The DC electrical specifications on page 8-4, section 8.5 have been changed:

a) The minimum DC Input Low Voltage is GND - undershoot has been listed as a separate spec of -0.3V.

b) The clock inputs EXTAL and X1 are CMOS inputs - Clock Input Low Voltage has been respecified as a function of V_{DD}.

c) Pullup, Pulldown, and Output Current specifications have been added.

d) Power dissipation has been recalculated for a worst case current drain of 100mA at 5.25V (not 5.0V).

DC ELECTRICAL SPECIFICATIONS

Characteristic	Symbol	Min	Max	Unit
Input Low Voltage (except clocks)	V_{IL}	GND	0.8	V
Clock Input High Voltage (EXTAL, X1)	V_{IHC}	0.8*(V_{CC})	V_{CC}	V
Clock Input Low Voltage (EXTAL, X1)	V_{ILC}	0	0.2 *V_{CC}	V
Undershoot		–	–0.3	V
Pullup Current @V_{IN} = 0V $\overline{HALT}$, $\overline{RESET}$, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DTACK}$, $\overline{BERR}$, $\overline{TRST}$, TMS, TDI		–50	–10	µA
Pulldown Current @V_{IN} = V_{CC} TCK		10	50	µA
Output Current $\underline{CLKOUT}$, $\overline{RAS1}$–$\overline{RAS0}$, $\overline{CAS1}$–$\overline{CAS0}$, $\overline{DRAMW}$, A15/DRAMA14–A1/DRAMA0	I_{OH} I_{OL}	8 8	—	mA
Others	I_{OH} I_{OL}	4 4	—	mA
Power Dissipation f= 16.67 MHz	P_D	—	0.525	W

7. Operating Conditions

The following table was omitted from page 8-1:

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	0	70	°C

NOTES:

1. Unused input and bidirectional pins must be terminated to a valid logic one or zero level.

8. Maximum Ratings - Input Voltage

On page 8-1, the maximum input voltage rating is either 7.0V or V_{CC}+0.3V, whichever is less.

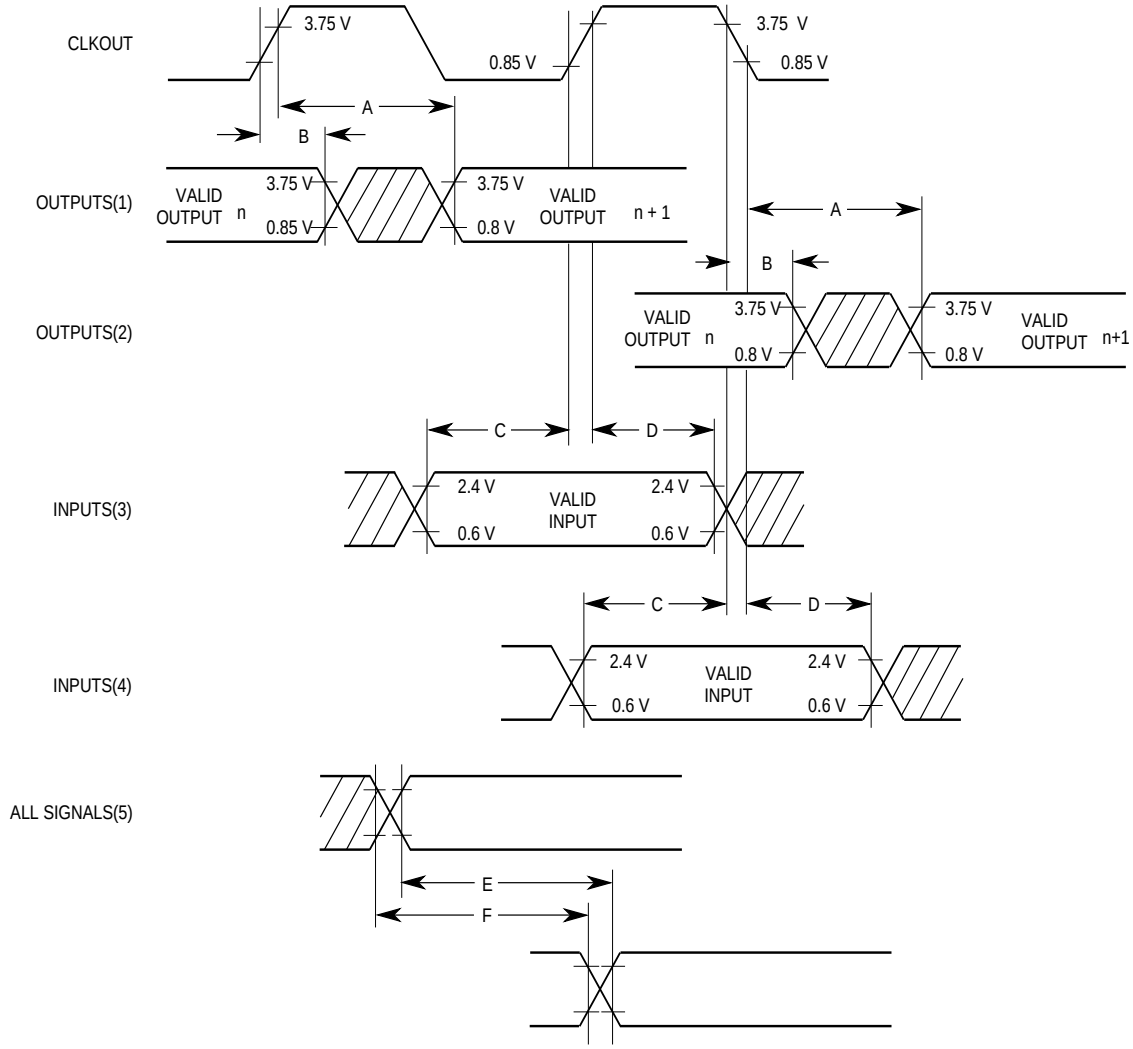
9. New System Interface Specifications

The following new electrical specifications have been added.

Num.	Characteristic	Min	Max	Unit
104	AMODE, $\overline{IRQx}$ Setup and Hold to $\overline{RESET}$ Negation	60	—	ns
105	Port Pin Setup to $\overline{AS}$ Asserted, Port Pin Read	30	—	ns
105A	Port Pin Hold from $\overline{AS}$ Negated, Port Pin Read	30	—	ns
106	$\overline{UDS}$, $\overline{LDS}$ Asserted to Port Pin, Port Write	0	60	ns

10. Drive Levels and Test Points for AC Specifications

The current drive levels and test points for the MC68306 are shown in the revised Figure 8-1 below (page 8-3).



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal invalid to signal invalid specification (maximum or minimum).

FIgure 8-1. Drive Levels and Test Points for AC Specifications

11. Counter/Timer Mode Clock Source Select Bits

In Table 6-10 on page 6-31, the entry under “Clock Source Select Command” for “Crystal or External Clock” with MISC2 = 0 should be “Crystal or External Clock Divided by 16”.

12. Memory Map Error

In Table 5-1 on page 5-2, the entry for address FFFFFFF4/5 should be labeled PORT A PINS and PORT B PINS rather than PORT A PIN ASSIGNMENT and PORT B PIN ASSIGNMENT. Note 4 should read “Duplicate of FFFFF7E0–FFFFF7FF”.

13. DIV and MUL Instructions

The DIVS and DIVU summaries on page 4-9, and the MULS and MULU summaries on page 4-10 incorrectly show longword (.L) variants. The 68EC306 only supports word sized (.W) operations for these instructions.

14. X1/Clock Addition

The last sentence in paragraph 6.2.1 on page 6-4 should read: “If the serial module is not being used at all, the X1/CLK input may be tied to V_{CC} or GND.

15. IP2, OP3 Signal Descriptions

On page 6-6, the following paragraphs should be added:

6.2.11 Channel B Receiver Clock/Timer Clock (RxCB/TCLK/IP2)

This pin can be used as the channel B receiver clock source, the counter/timer clock source, or as a dedicated parallel input. It can generate an interrupt on change-of-state.

6.2.11.1 RxCB. When used for this function, the received data is sampled on the rising clock edge.

6.2.11.2 Timer Clock. When used for this function, the counter/timer decrements on the rising clock edge.

6.2.11.3 IP2. When used for this function, this signal is a general-purpose input.

6.2.12 Parallel Output (OP3)

6.2.12.1 Counter/Timer Output, Channel B Clock Output. This output can be used as the open-drain active-low counter-ready output, the open-drain timer output, the channel B transmitter 1X-clock output, or the channel B receiver 1X clock output.

6.2.12.2 OP3. When used for this function, this output is controlled by bit three in the DUOP register.

16. Receiver Clock Select Error

In Table 6-5 on page 6-25, IP2 can be used as the RxCB clock input. RCS3–RCS0 values 1110 and 1111 are valid for CSRB only, and select IP2–16X and IP2–1X clock sources, respectively. Lack of IP5 prevents use of a 1X transmit clock for the current implementation.

17. Bus Arbitration

For specification 37A on page 8-10 ($\overline{\text{BGACK}}$ Asserted to $\overline{\text{BR}}$ Negated) the minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted. The processor will negate $\overline{\text{BG}}$ and begin driving the bus again if external arbitration logic negates $\overline{\text{BR}}$ before asserting $\overline{\text{BGACK}}$. Figure 8-6 on page 8-10 shows timing for 2-wire bus arbitration ($\overline{\text{BGACK}}$ not used). FIgure 8-7 on the following page shows timing for 3-wire bus arbitration ($\overline{\text{BGACK}}$ used).

18. Omission of Control Bit Definition

In paragraph 7.3 on page 7-4, the following sentences should be added immediately before Table 7-1: “All control bits with overbars, and HiZ, are active low. Their respective output bits are enabled when a zero is shifted into the control bit. The other control bits are active high.”

19. HiZ Control Function

In table 7-2 on page 7-5, the HiZ control function in the boundry scan definition (bit 67) should be shown as active low ($\overline{\text{HiZ}}$) rather than active high (HiZ.)

20. $\overline{\text{ACKx}}$ Assertion Time

$\overline{\text{IACKx}}$ is shown asserted too early in Figure 8-5 on page 8-9. The figure below shows $\overline{\text{IACKx}}$ assertion time (spec 70) correctly referenced to the rising edge of state S4.

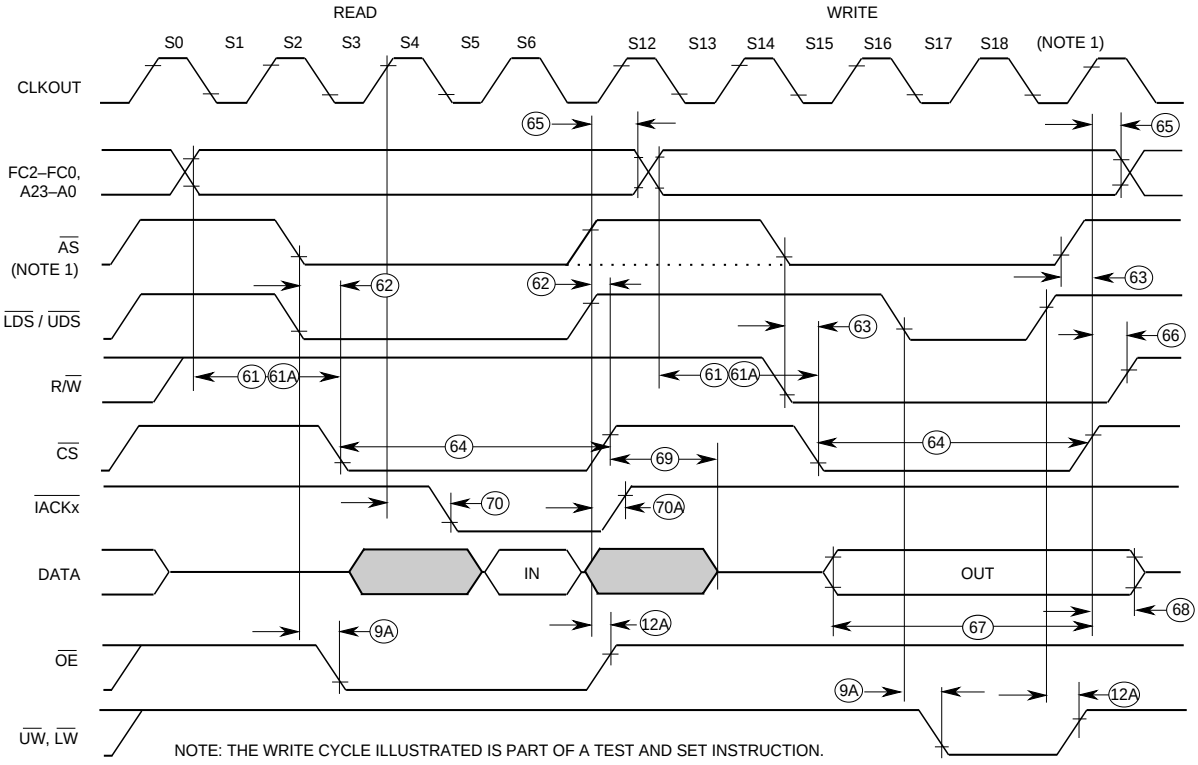


Figure 8-5. Chip Select and Interrupt Acknowledge Timing Diagram

21. Clock Output Timing

The current drive levels and test points for the MC68306 input and output clocks are shown in the revised Figure 8-2 below (see page 8-5.)

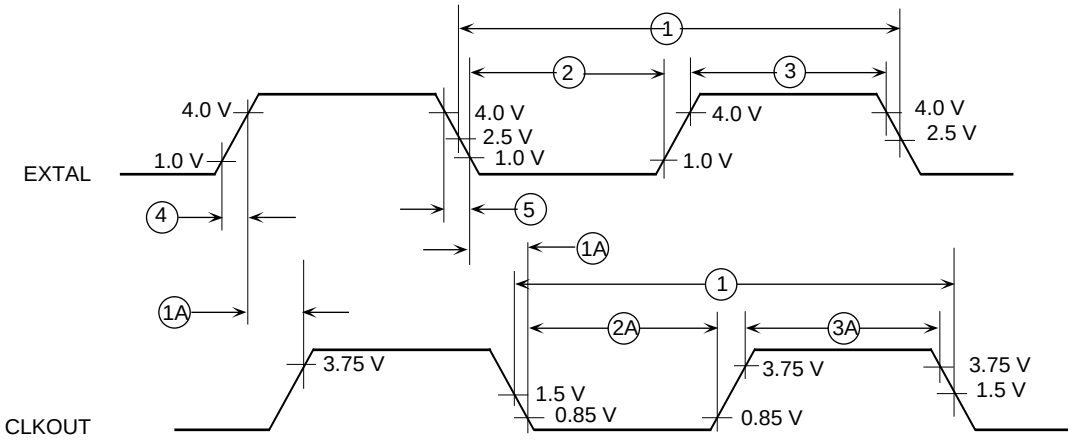
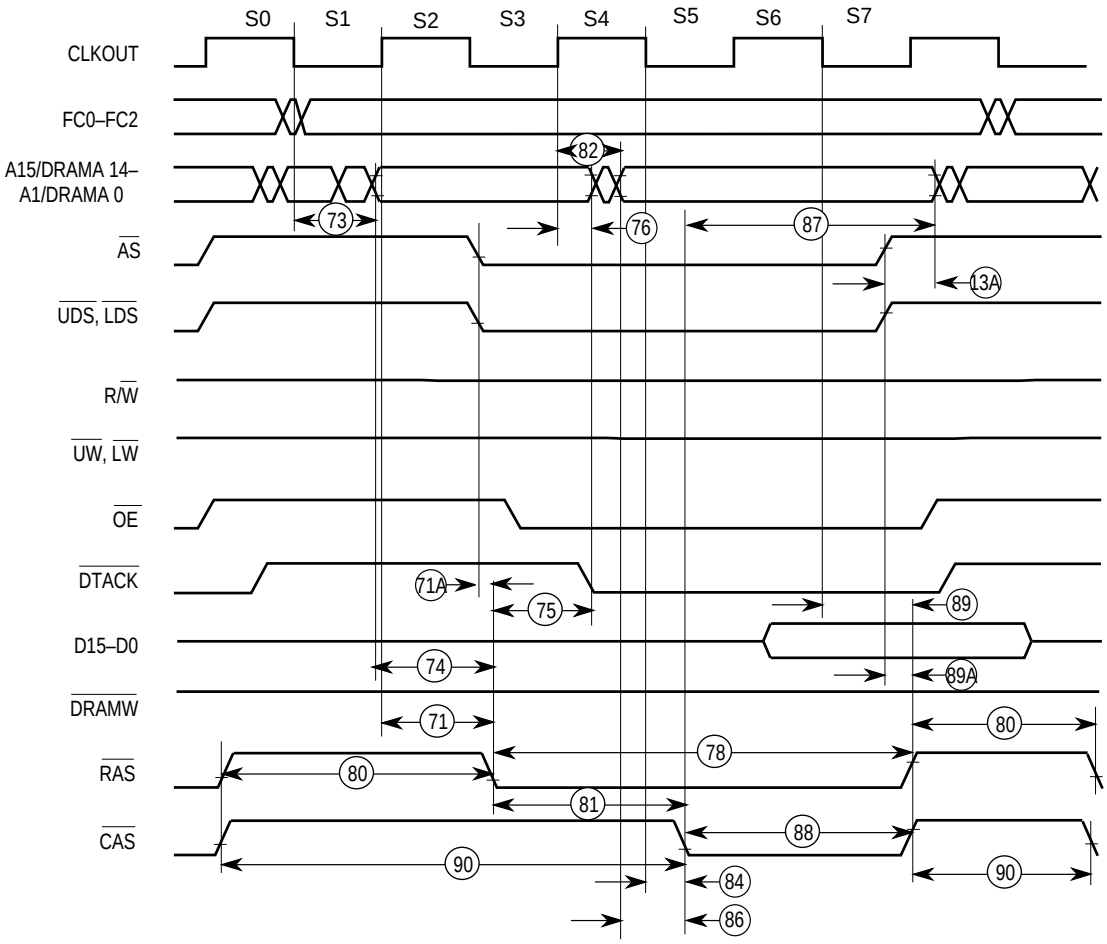


FIgure 8-2. Clock Output Timing

22. DRAM Address Hold Time

Specification 13A below has been added to the AC electrical specifications on page 8-5. A revised figure 8-8 from page 8-13 shows the new specification (address hold from $\overline{AS}$/$\overline{UDS}$/$\overline{LDS}$ negate near state S7).



		16.67 MHz		
Num	**Characteristic**	**Min**	**Max**	**Unit**
13A	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ Negated to Address Invalid, DRAM Cycle	0	—	ns

Figure 8-8. DRAM Timing – 0-Wait Read, No Refresh

23. Interrupt Level Description Error

In paragraph 6.1.4, the last sentence on page 6-3 should read “When an interrupt at this level is acknowledged, the serial module is serviced before the external IRQx of the same level.”

24. Bus Timeout Period Register Address Error

In paragraph 5.2.3 on page 5-4, the bus timeout period register address should be “FFFFFFFD”.

25. Chip Select Configuration Register Reset State Error

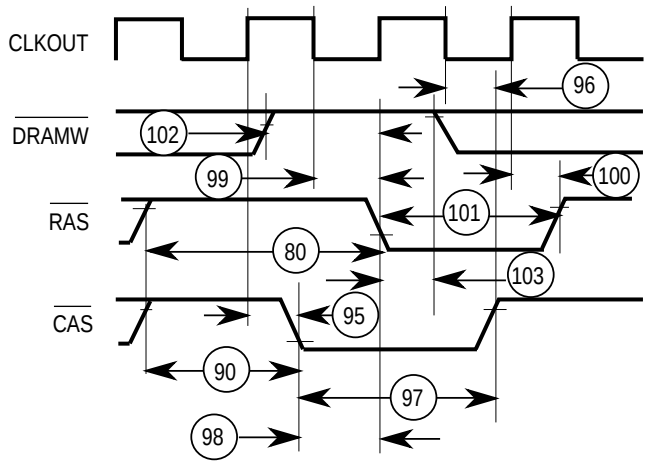
In paragraph 5.2.6.2 on page 5-10, the reset value of CS0 bit 15 (CSR-Chip Select Read enable) is one, not zero.

26. DRAM Refresh Cycles

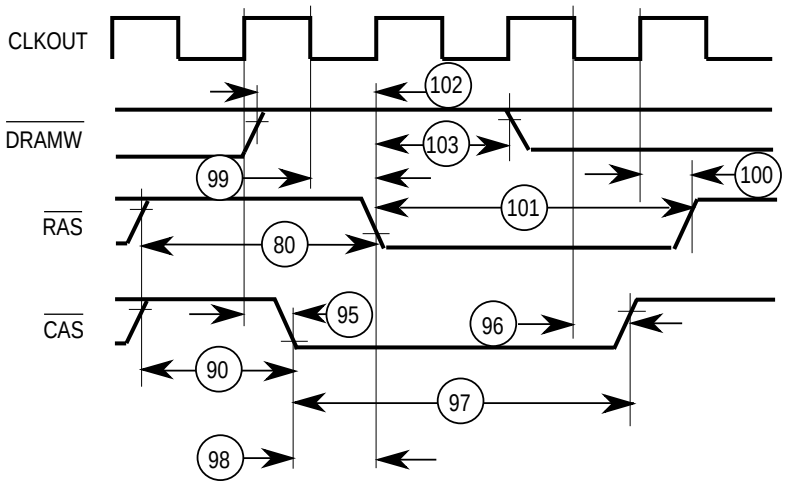
The specifications for DRAM refresh timing in the AC Specifications on page 8-12 and in Figure 8-10 on page 8-14 referenced the wrong clock edges. Corrected specifications and figures are shown below.

AC ELECTRICAL SPECIFICATIONS—DRAM

		16.67 MHz				
		0-Wait		1-Wait		
Num.	Characteristic	Min	Max	Min	Max	Unit
95	CLKOUT High to $\overline{CASx}$ Asserted (Refresh Cycle)	0	20	0	20	ns
96	CLKOUT Low to $\overline{CASx}$ Negated (Refresh Cycle)	0	20	0	20	ns
98	$\overline{CASx}$ Asserted to $\overline{RASx}$ Asserted (Refresh Cycle)	20	60	20	60	ns
99	CLKOUT Low to $\overline{RASx}$ Asserted (Refresh Cycle)	0	30	0	30	ns
100	CLKOUT High to $\overline{RASx}$ Negated (Refresh Cycle)	0	25	0	25	ns
102	$\overline{DRAMW}$ High to $\overline{RASx}$ Asserted (Refresh Cycle)	20	60	20	60	ns



a. 0 - Wait State



b. 1 - Wait State

Figure 8-10. DRAM Timing Refresh

27. DRAM Timing for 1-Wait Access

Figure 8-9 on page 8-14 is missing a wait state - see the revised figure below. Spec 13A has also been added to this figure.

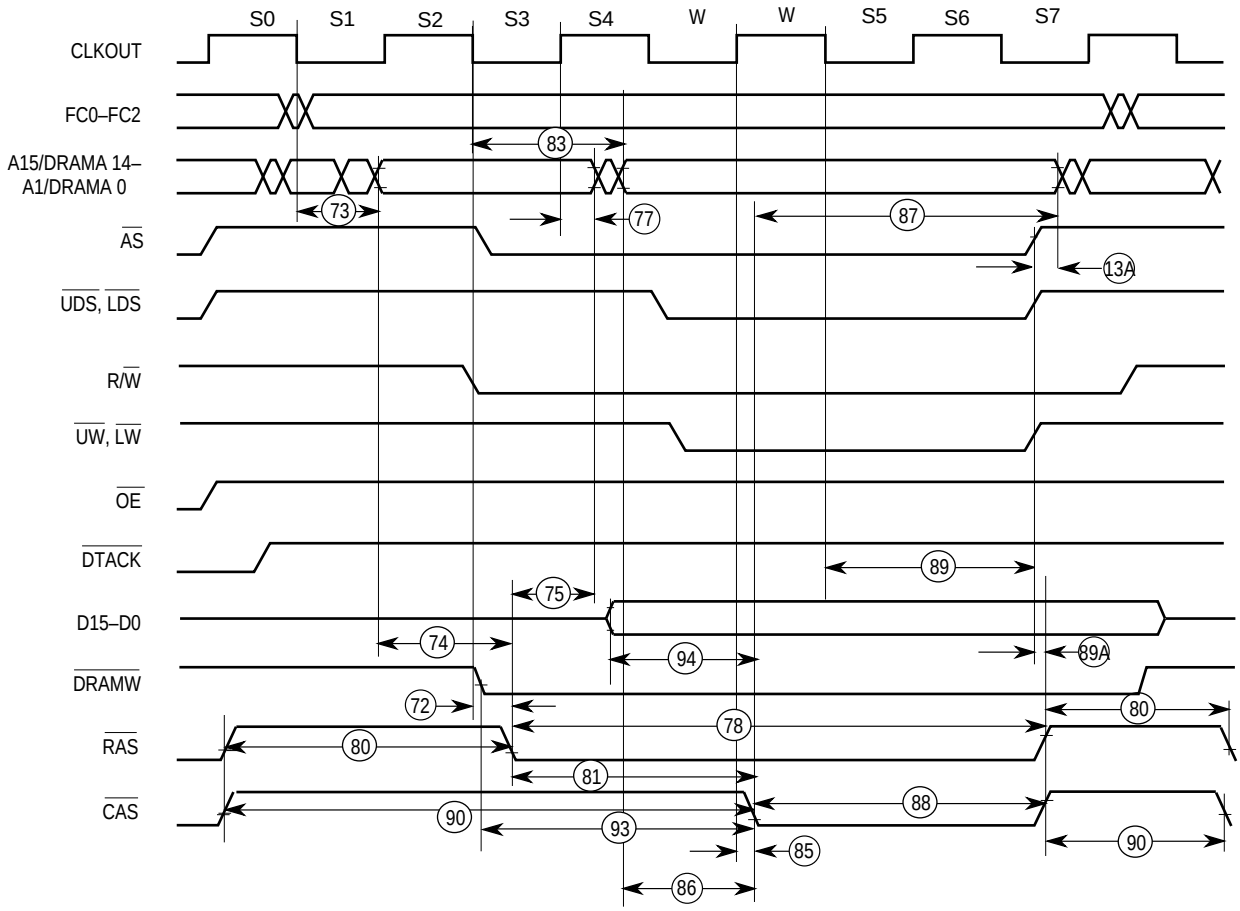


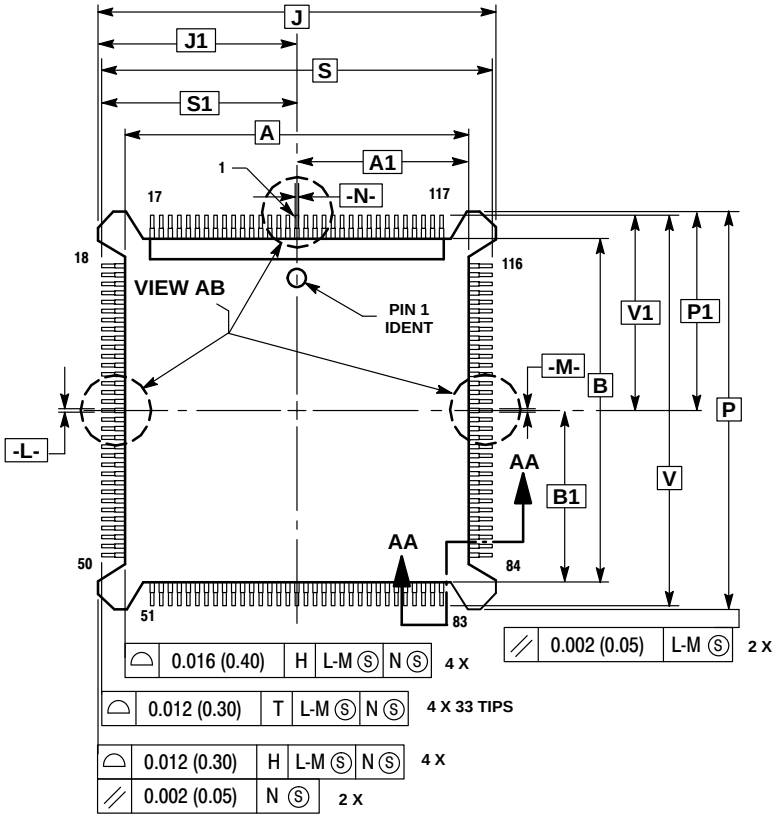
Figure 8-9. DRAM Timing – 1-Wait Write, No Refresh

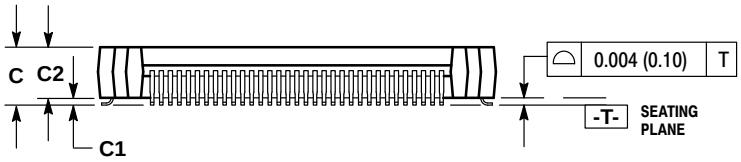
28. Pin Assignment Orientation Error

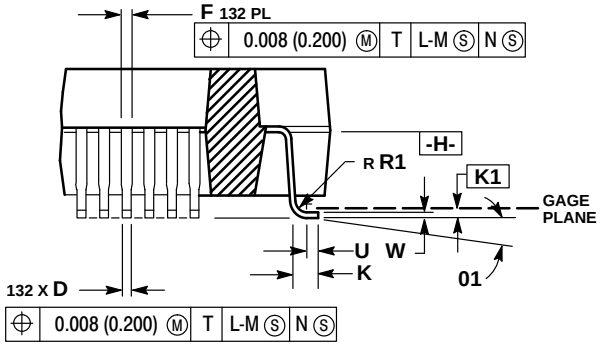
The pin assignment diagram of the 144-Lead Thin Quad Flat Pack (TQFP) on page 9-3 of section 9.2 should be rotated 90 degrees counter clockwise (including pins.) As a result, the pin one dot should be in the lower left hand corner. The part number should still be horizontally displayed in the drawing. All TQFP parts are marked such that pin one is in the lower left hand corner when viewing the part with the markings oriented normally.

29. Package Dimensions Diagram Error

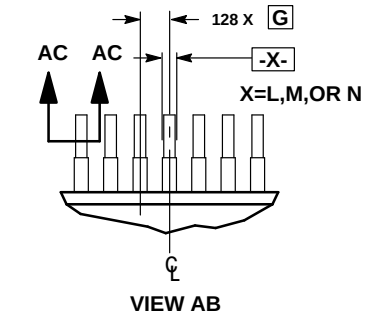
The 132-pin package diagram on page 9-4 shows 32 pins on a side. There are actually 33 pins on a side. The specifications for the case size and pin spacing are correct.

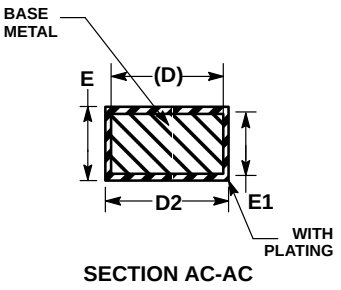






SECTION AA-AA





SECTION AC-AC

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A, B, J, AND P DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.010 (0.25), FOR DIMENSIONS J AND P IS 0.007 (0.18).
4. DATUM PLANE -H- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS -L-, -M-, AND -N- TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -H-.
6. DIMENSIONS U AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIMENSIONS A, B, J, AND P TO BE DETERMINED AT DATUM PLANE -H-.
8. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.019 (0.48).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.950 BSC		24.13 BSC	
A1	0.475 BSC		12.06 BSC	
B	0.950 BSC		24.13 BSC	
B1	0.475 BSC		12.06 BSC	
C	0.160	0.180	4.06	4.57
C1	0.020	0.040	0.51	1.02
C2	0.135	0.145	3.43	3.68
D	0.008	0.012	0.20	0.30
D1	0.012	0.016	0.30	0.41
D2	0.008	0.011	0.20	0.28
E	0.006	0.008	0.15	0.20
E1	0.005	0.007	0.13	0.18
F	0.012	0.014	0.30	0.36
G	0.025 BSC		0.64 BSC	
J	1.100 BSC		27.94 BSC	
J1	0.550 BSC		13.97 BSC	
K	0.034	0.044	0.86	1.11
K1	0.010 BSC		0.25 BSC	
P	1.100 BSC		27.94 BSC	
P1	0.550 BSC		13.97 BSC	
R1	0.015 REF		0.38 BSC	
S	1.080 BSC		27.43 BSC	
S1	0.540 BSC		13.72 BSC	
U	0.025 REF		0.64 REF	
V	1.080 BSC		27.43 BSC	
V1	0.540 BSC		13.72 BSC	

CASE 831A-02
ISSUE B

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan
ASIA-PACIFIC: Motorola Seminconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong

SEMICONDUCTOR PRODUCT INFORMATION