M32C/80 Series

Using DMACII (Burst Transfer)

1. Abstract

This application note describes how to use DMACII in burst transfer.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M32C/80 Series

This program can also be used when operating other microcomputers within the M16C family, provided they have DMACII function. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Detailed description

The following explains an example use of DMACII transfer for the case where when an interrupt request which has had its priority level set to 7 by the interrupt control register occurs, data is transferred from one memory location to another by a DMACII transfer a specified number of times successively.
During a burst transfer, the user program is not executed. Nor are interrupts accepted.

3.1 DMAC II Transfer Mode

This application note example offers functions of single transfer mode shown in Table 1.

Table 1. Selectable Functions in Single Transfer Mode

Item	Definition	Selection
Transfer Block	8 bits	Yes
	16 bits	
Transfer Data	Immediate data	
	Data in memory	Yes
Source Direction	Fixed address	
	Forward address	Yes
Destination Direction	Fixed address	Yes
	Forward address	
Calculation Transfer Function	Without Calculation Transfer Function	Yes
	With Calculation Transfer Function	
End-of-Transfer Interrupt	Interrupts not used	Yes
	Interrupts used	
Chained Transfer Function	Not chain transferred	Yes
	Chain transferred	

3.2 DMAC II Index

The DMAC II index is configured with 8 bytes when interrupts and chain transfers are not used in burst transfer mode. The DMAC II index must be located on the RAM area.

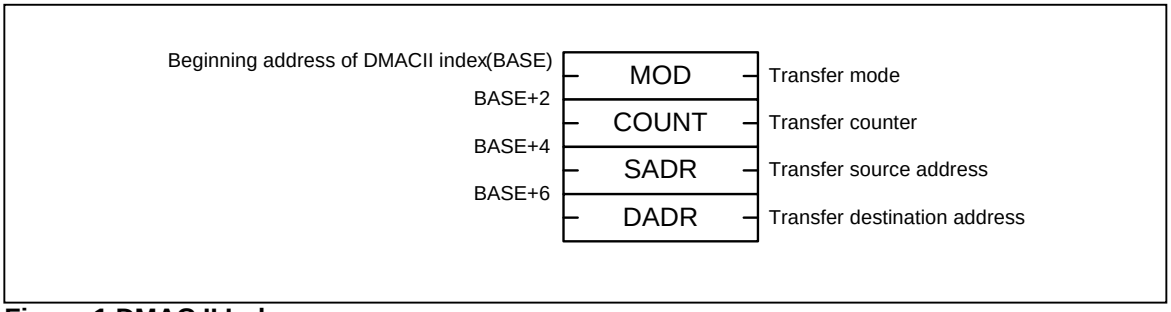


Figure 1.DMAC II Index

3.3 DMAC II Transfer

The interrupt requests from all peripheral functions whose ILVL2–ILVL0 bits in the interrupt control register have been set to “111b” constitute the cause of requests to DMAC II. In this application note, the INT0 interrupt is used for the cause of DMAC II request.

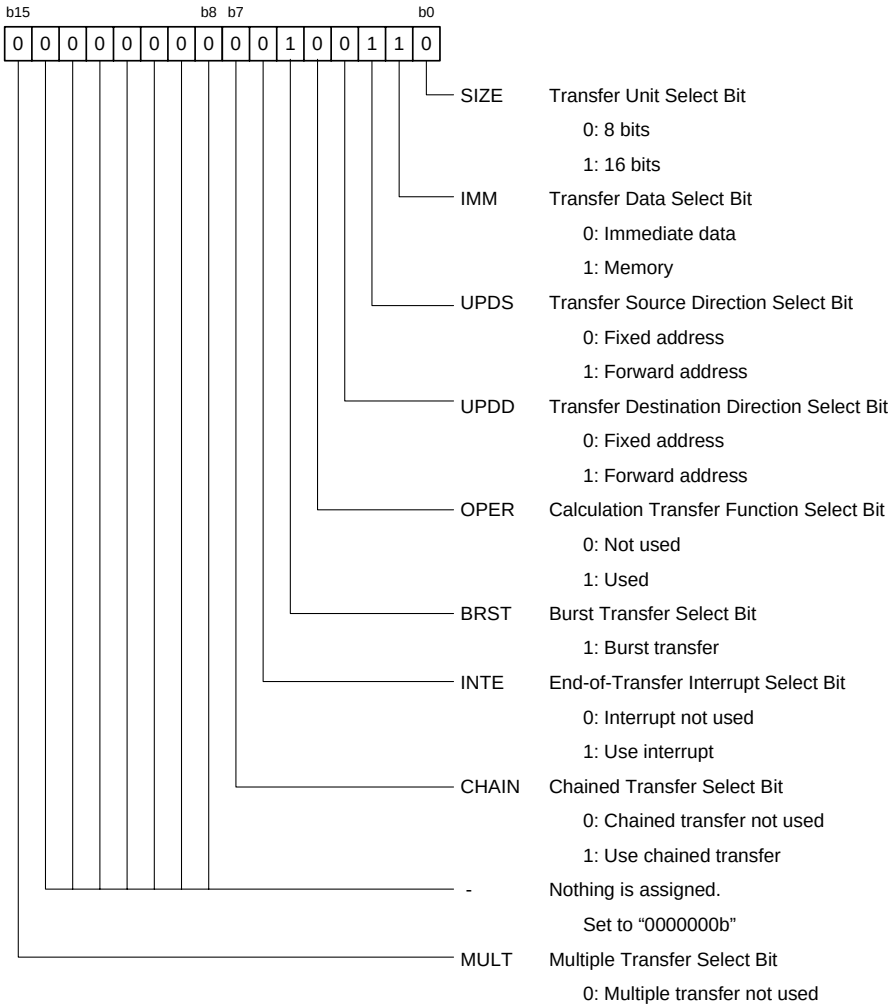
3.4 Setting Up the Relocatable Vector Table

Set the beginning address of the DMAC II index in the interrupt vector for the peripheral function interrupt that constitutes the cause of DMAC II request.

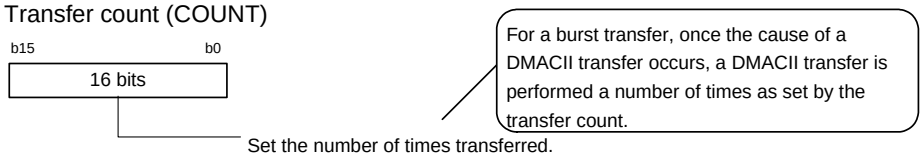
3.5 Register Setting

To enable the operation defined in "Section 3. Detailed description", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M32C/80 Series HARDWARE MANUAL.

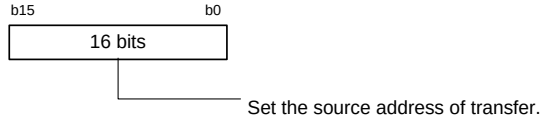
(1) Transfer mode (MOD)



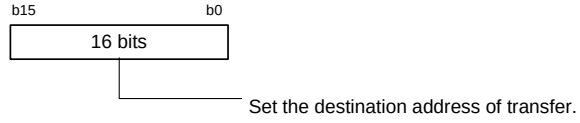
(2) Transfer count (COUNT)



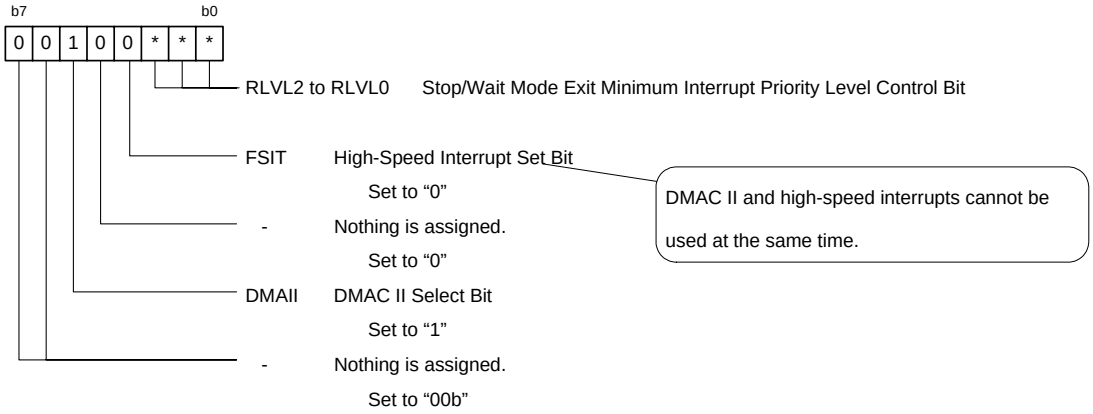
(3) Transfer source address (SADR)



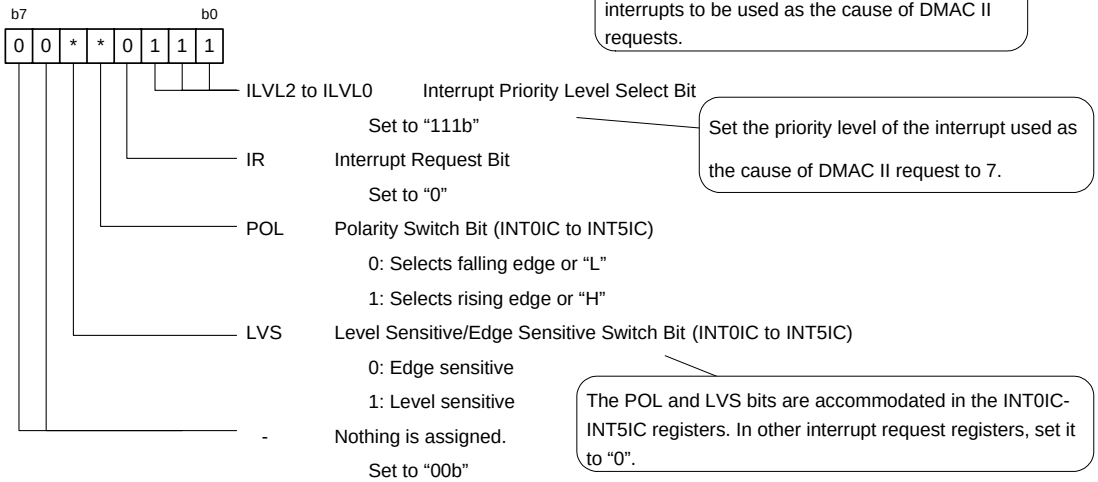
(4) Transfer destination address (DADR)



(5) RLVL register



(6) Interrupt Control Register



4. Example of a Sample Program

4.1 C language source

```
/************************************************************************
/*  FILENAME: rej05b0639_src.c                                          *
/*  Ver : 1.00                                                        *
/*  FUNCTION: DMACII(Burst Transfer)                                     *
/************************************************************************/
/******************************/
/*   include file            */
/******************************/
#include <stdio.h>
#include "sfr32c83.h"

/******************************/
/*   DMACII                 */
/******************************/
struct{
   union {
      struct{
         char    size:1;        /* Transfer Unit Select Bit */
         char    imm:1;         /* Transfer Data Select Bit */
         char    upds:1;        /* Transfer Source Direction Select Bit */
         char    updd:1;        /* Transfer Destination Direction Select Bit */
         char    oper:1;        /* Calculation Transfer Function Select Bit */
         char    brst:1;        /* Burst Transfer Select Bit */
         char    inte:1;        /* End-of-Transfer Interrupt Select Bit */
         char    chain:1;       /* Chained Transfer Select Bit */
         char    reserve:7;
         char    mult:1;        /* Multiple Transfer Select Bit */
      }bit;
      unsigned short  all;
   }mod;
   unsigned short count;          /* Transfer count */
   unsigned char near *sadr;      /* Transfer source address */
   unsigned char near *dadr;      /* Transfer destination address */
}dm_index;

/*  Transfer data array */
static unsigned char near data[5] = {0x11,0x22,0x33,0x44,0x55};

/* Transfer destination */
static unsigned char near dest;

/******************************/
/*   main                   */
/******************************/
void main(void){
   asm("   fclr    i   ");    /* Interrupt disable */
   /*  DMACII setting  */
   dm_index.mod.all = 0x0026;  /* Transfer Unit:      8bit    */
                          /* Transfer Data:      Memory  */
```

```
                        /* Transfer Source:    Forward */
                        /* Transfer Destination:Fixed   */
                        /* Calculation Transfer:None    */
                        /* Burst Transfer:     Burst   */
                        /* Interrupt:          None    */
                        /* Chained Transfer:    None    */
                        /* Multiple Transfer:   None    */

    dm_index.count = 5;        /* number of transfer  = 5 */
    dm_index.sadr = data;      /* Source of transfer  = beginning address of the data array */
    dm_index.dadr = &dest;     /* Destination of transfer = dest */

    /*  Set the interrupt used for DMAC II  */
    rlvl = 0x20;             /* Interrupt priority level 7 is used for DMAC II transfers */

    int0ic = 0x07;            /* INT0 interrupt level 7 (used for DMACII) */

    while(1);
}
```

4.2 Relocatable Vector Tables

```
    ;-----------------------------------------------------------------
    ; variable vector section
    ;-----------------------------------------------------------------
            .section  vector,ROMDATA              ; variable vector table
            .org      VECTOR_ADR

            .lword    dummy_int          ; BRK (software int 0)
            .lword    dummy_int          ;
            .lword    dummy_int          ;
            .lword    dummy_int          ;
            .lword    dummy_int          ;
            .lword    dummy_int          ;
            .lword    dummy_int          ;
            .lword    dummy_int          ; DMA0 (software int 8)
    ;
    ;
    ;                         (Omission)
    ;
    ;
            .lword    dummy_int          ; INT5 (software int 26)
            .lword    dummy_int          ; INT4 (software int 27)
            .lword    dummy_int          ; INT3 (software int 28)
            .lword    dummy_int          ; INT2 (software int 29)
            .lword    dummy_int          ; INT1 (software int 30)
            .glb      _dm_index
            .lword    _dm_index          ; INT0 (software int 31)
            .lword    dummy_int          ; TIMER B5 (software int 32)
    ;
    ;
    ;                         (Omission)
    ;
    ;
```

5. Reference

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Hardware Manual

M32C/80 Group Hardware Manual
(Use the latest version on the home page: http://www.renesas.com)

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