Cinnamon Bay

Single Board Computer

Thermal Application Note
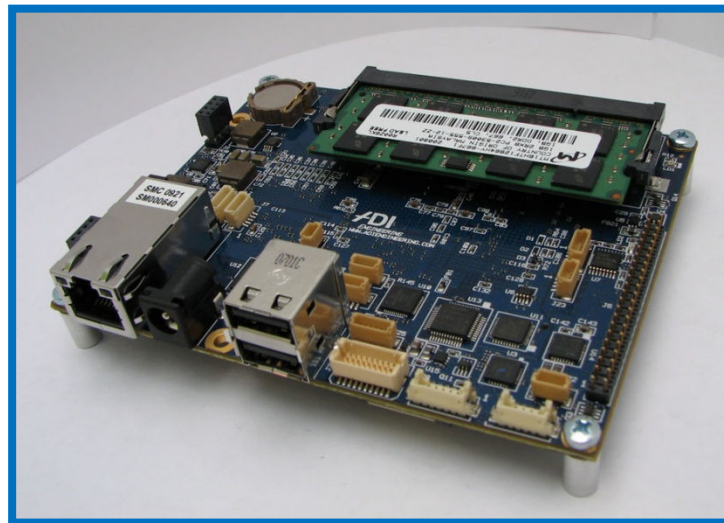
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Revision History

Date	Revision	Section	Remarks
10/21/2009	R100	All	Initial Release

1 INTRODUCTION

One of the most challenging aspects of embedded computer design is ensuring each component in the system stays within its operational temperature range. ADI Engineering's Cinnamon Bay Single Board Computer (CB SBC) utilizes an Intel® Atom^{TM} Z5xx series processor and the Intel® System Controller Hub US15W(P). The Atom processor and SCH chipset are designed for the mobile computing market and thus deliver high performance in a relatively low power package. But the high performance per watt efficiency alone does not guarantee the processor and chipset on a CB SBC will stay within its temperature limits for every application. System Engineers will have to factor in variables such as the chassis the CB SBC is put in, the ambient temperature, available airflow, and performance requirements to determine an adequate thermal solution for their particular application.

The objective of this document is to provide CB SBC system designers with information about the thermal characteristics of the hardware along with the thermal management options available in software (BIOS and Operating System).

1.1 Terms/Acronyms

Before detailing the thermal characteristics of the CB SBC hardware, it is critical to have a solid understanding of the terminology. This section lists acronyms used throughout this document, but more importantly, defines key concepts.

T_A	Ambient Temperature. The measured temperature locally surrounding the CB SBC circuit board
T_J	Junction Temperature. The hottest temperature inside an integrated circuit.
T_{J-MAX}	Maximum rated Junction Temperature. Exceeding a semi-conductor's specified maximum temperature could result in decreased performance, unreliable operation, or permanent component damage.
T_{CASE}	Case Temperature. The temperature measured at the geometric center of the top of an integrated circuit's case or die.
TIM	Thermal Interface Material. A thermally conductive compound between an integrated circuit and its heatsink. This material fills the air gaps and voids to enhance the transfer of heat from the integrated circuit to the heatsink.
TDP	Thermal Design Power. A power dissipation target based on worst-case applications. Thermal solutions should be designed to dissipate the thermal design power.
MSR	Model Specific Register. Control and status registers available to software for a particular processor implementation.
EIST	Enhanced Intel Speedstep Technology. A method for the switching a processor's voltage and frequency with response to load.
DTS	On-die Digital Thermal Sensor. Provides software an accurate measurement of the processor core temperature.
TM	Thermal Monitor. An on-die temperature sensor that is factory calibrated to trip when the processor's core temperature crosses a thermal limit. Two automatic protection schemes, TM1 and TM2, can be enabled to respond to a Thermal Monitor trip.

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CB	Cinnamon Bay
SBC	Single Board Computer
SCH	System Controller Hub. Combines the functionality traditional found in a North Bridge (high speed I/O such as memory and graphics) and South Bridge (low speed I/O)
PSV	Passive cooling threshold. Thermal trip point setting used to configure the temperature that processor clock throttling is initiated.

1.2   Reference Documents

Document Title	Document Number
Cinnamon Bay Single Board Computer Hardware User's Manual	45700-0001
Intel® Atom^{TM} Processor Z5xx Series datasheet.	319535-002US
Intel® Atom^{TM} Processor Z5xx Series datasheet Addendum for Z5xxP processors.	321423
Intel® System Controller Hub (SCH) Datasheet	319537-001US
Intel® System Controller Hub (SCH) Datasheet Addendum for US15WP and US15WPT	321422-001
Intel® IA-32 Architectures Software Developer's Manual. Volumes 3A and 3B.	253668-031US 253669-031US
Advanced Configuration and Power Interface (ACPI) Specification	Rev 3.0b

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2   THERMAL OVERVIEW

The four hottest IC's (the ones most likely to exceed a temperature rating) on the CB SBC are: the Atom Z5xx processor, US15W(P) System Controller Hub, Power Management IC, and the Gigabit Ethernet Controller.

ADI has conducted extensive worst case temperature testing and has found that the Power Management chip and Ethernet controller remain within temperature specifications at rated ambient temperature and zero airflow. So the system designer's job to keep those two ICs in spec is straightforward and requires no effort beyond keeping the ambient temperature around the SBC below its rating (85C for the SBC520PT and 70C for the other SBC variants).

The thermal solution for the processor and SCH is not always as straight forward. The system designer will have to consider several factors to determine if additional passive cooling (heatsink) or active cooling (fan) is required for their particular application. Those factors include:

- Processor loading

- Number of peripheral components (hard disk drives, flat panel displays, UBS devices, etc..).

- Whether or not software reduced performance is an acceptable means to reduce temperature.

The remainder of this document will focus on the hardware and software mechanisms available to the CB SBC system designer to maintain the processor and SCH within their rated temperature limits. Where applicable, case studies will be presented to illustrate how the three factors listed above effect the processor and SCH temperature. Hopefully the data collected from the case studies will give system engineers some pre-design insight into whether or not additional cooling (i.e. a heatsink) will be required for their particular application.

2.1   Temperature Monitoring

2.1.1   Digital Thermal Sensor (DTS)

The preferred method for monitoring the CB SBC's processor temperature is through an on-die temperature sensor that Intel has dubbed the "Digital Thermal Sensor". Intel recommends using the DTS because of its close proximity to the hottest portions of the die. The DTS can be read by software using a model-specific register (MSR). Specifically, the DTS value is located in bits 22 to 16 of the IA32_THERM_STATUS register (0x019C). See section 14.5.5.2 in Volume 3A of the Architectures Software Developer's Manual for additional details of the MSR that contains the DTS.

One important aspect of the DTS is that it does not read the absolute temperature of the processor. Rather it reads the temperature relative to the maximum junction temperature of the device. So a value of 0 in the DTS indicates the processor die temperature is at its rated value.

Therefore, when software is calculating absolute processor temperature based on the DTS reading, it is important for software to factor in which processor is on the CB SBC. The Z520PT processor found on the CB SBC A520PT (Extended Temperature) has a T_{J-MAX} of 110C while the other CB SBC variants have a T_{J-MAX} of 90C.

CB Variant	Processor	T_{J-MAX}	Equation for Software
SBC A530P	Intel® Atom Z530P	90C	$T_{ABS} = 90C - DTS$
SBC A510P	Intel® Atom Z510P	90C	$T_{ABS} = 90C - DTS$
SBC A520PT	Intel® Atom Z520PT	110C	$T_{ABS} = 110C - DTS$

Table 1 Maximum Operating Conditions

2.1.2   ACPI Thermal Zone

The ACPI specification defines interfaces that allow the operating system to be involved with system cooling properties. In order for the operating system to respond to system variations and make cooling decisions, it first must be capable of getting accurate temperature data for each "zone" in its control. For the CB SBC, there is only one thermal zone and it corresponds to the processor and is based on the DTS reading.

To relieve the processor from the overhead of having to periodically poll the DTS for the current processor temperature, the BIOS implements a system to asynchronously notify the operating system whenever a meaningful change in the zone's temperature occurs. The BIOS contains a table of "thresholds". Any time the processor temperature crosses one of these thresholds, the BIOS fires an interrupt to the operating system along with the current temperature. The operating system's interrupt routine will then update the ACPI thermal zone temperature with the new value.

The BIOS image that is loaded at the factory contains the following thresholds:

C-Temp SBC's		
Current Temp	Low Temp	High Temp
25	0	30
35	15	45
45	25	55
55	35	65
65	45	75
75	55	85
85	65	90
90	75	90

I-Temp SBC's		
Current Temp	Low Temp	High Temp
25	0	30
35	15	45
45	25	55
55	35	65
65	45	75
75	55	85
85	65	95
95	75	110
110	85	110

Table 2 ACPI Thermal Zone Thresholds

2.1.3   Intel® Thermal Monitor

The Atom Z5xx series processors contain a second temperature sensor that is factory calibrated to trip when the processor's core temperature crosses a thermal limit. If the thermal monitor senses the silicon has reached its maximum operating temperature, it activates a Thermal Control Circuit (TCC) to reduce the processor temperature by modulating the processor's core clock or by initiating an Enhanced Intel SpeedStep Technology transition. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable and corresponds to the DTS reading a value of 0.

2.1.4   Thermal Diode

In addition to the Digital Thermal Sensor, the processor also contains an on-die PNP transistor whose base emitter junction is used as a thermal diode. On a CB SBC, the thermal diode is read from an off-die remote temperature sensor (SA56004X from NXP). The remote temperature sensor is accessed over the SMBus and it can be setup to assert an interrupt for an over temperature condition and a second independent interrupt to alert the system of critical temperature. The SA56004X operates over a range of -40 to +125C with 11-bit resolution (0.125C). It can accurately sense the temperature of the processor's thermal diode within +/- 1C.

Unlike the DTS which is tightly integrated with ACPI (and therefore the BIOS and OS), an application that wishes to utilize the thermal diode will have to implement the code necessary to poll the SA56004X and work with the operating system to manage cooling schemes.

2.2   Hardware Initiated Thermal Management Mechanisms

This section briefly describes the TM1, TM2, and Catastrophic Shutdown mechanisms built into the Intel Atom architecture. These mechanisms allow the processor to automatically protect itself from over temperature stresses. TM1 and TM2 can be individual disabled in the BIOS, but simultaneously disabling both TM1 and TM2 is considered operating out of specification. Intel recommends both TM1 and TM2 be enabled. If the reader desires a more detailed discussion of TM1 and TM2, please refer to section 5.1.2 of the Intel Atom Datasheet.

2.2.1   Thermal Monitor 1 (TM1)

The Intel Thermal Monitor described above in Section 2.1.3 will activate a Thermal Control Circuit (TCC) when the processor's core temperature reaches its maximum operating value. If the TCC is activated while TM1 is enabled in the BIOS, the processor's core clocks will be modulated by turning them off and on at a 50% duty cycle. The 50% duty cycle is programmed at the factory and cannot be altered.

2.2.2   Thermal Monitor 2 (TM2)

Where TM1 changes the clocks duty cycle to help reduce the processor's core temperature, TM2 reduces the processor's clock frequency. If the TCC is activated while TM2 is enabled in the BIOS, the processor will perform an Enhanced Intel SpeedStep Technology (EIST) transition to the Lowest

Frequency Mode. For more details on EIST, see section 14.1 in volume 3A of the IA-32 Architectures Software Developer's Manual.

2.2.3   Catastrophic Shutdown

The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set to trip well above the normal operating range (~125C). The processor will stop all execution when it invokes this catastrophic shutdown mechanism. Once tripped, instructions are halted until after the next reset cycle. The catastrophic shutdown mechanism is always enabled.

2.3   Software Based Thermal Management

In addition to the automatic thermal management modes described above in section 2.2, there are two mechanisms for controlling the processor's thermal output via software.

2.3.1   On Demand Clock Modulation

The CB SBC architecture provides a mechanism to throttle the processor's clock at a configurable thermal trip set point. This throttling feature that Intel refers to as On Demand Clock Modulation is what allows an ACPI passive cooling strategy to be implemented. The passive cooling threshold (PSV) is selected in the BIOS setup screen under the Power --> Advanced CPU --> Thermal Trip Point Setting menu.

Each time the ACPI thermal zone temperature is updated (see section 2.1.2), the ACPI thermal zone temperature is compared to the PSV. If the ACPI thermal zone temperature exceeds the PSV, the system invokes On Demand Clock Modulation to reduce the processor clock duty cycle.

2.3.2   Custom Thermal Management Strategy

Because the processor makes it possible to read its die temperature through a MSR and also allows software to invoke On-Demand Clock Modulation, TM1, and TM2 through MSRs, custom software can be created to implement an application specific thermal management strategy. For a detailed discussion of the applicable MSRs, see chapter 14 in volume 3A of the Architectures Software Developer's Manual and Appendix B in volume 3B of the Architectures Software Developer's Manual.

3 CB SBC THERMAL CASE STUDIES

3.1 SBC A530P Case Studies

### 3.1.1 Heavily Loaded SBC A530P operating at 100% CPU Utilization

3.1.1.1 System Configuration

CB SBC A530P, 2GB SODIMM, 2.5" PATA HDD, micro-SD card, two USB 2.0 devices plus USB keyboard and mouse, Gigabit Ethernet connection, and LVDS flat panel display with backlight. Zero air flow. BurnInTest software from Passmark used to maintain the CPU at 100% loading including 2D and 3D video, floating point and integer calculations, RAM torture tests, continuous HDD and micro-SD card write-read-verify operations, continuous Gigabit Ethernet traffic, and near maximum throughput on the USB 2.0 devices.

A type K thermocouple was attached to the top center of the SCH to read its case temperature. The processor's on-die DTS was used to for reading the processor's junction temperature. Both of the processor's hardware thermal protection mechanism (TM1 and TM2) were enabled in the BIOS.

The test was conducted both with and without the optional heat spreader plate that is available through ADI Engineering (see Appendix I for more details of the ADI Engineering heat spreader). Data from both test cases is shown below.

3.1.1.2 Results

Processor and SCH Temp vs Ambient (with heat spreader installed)
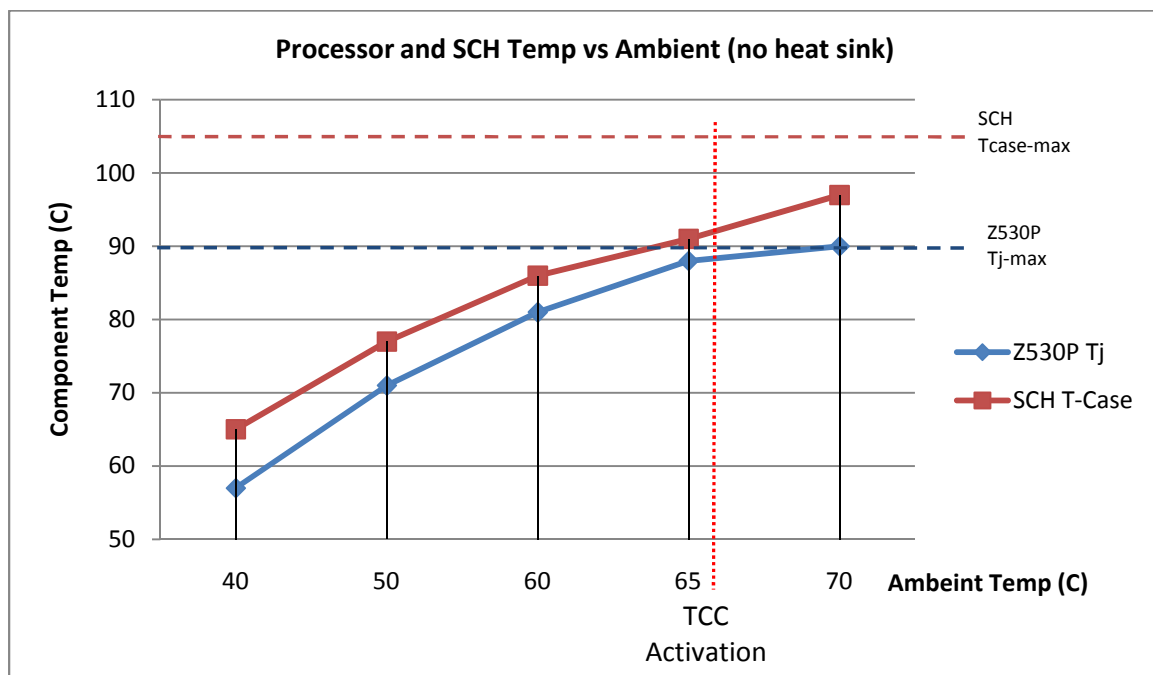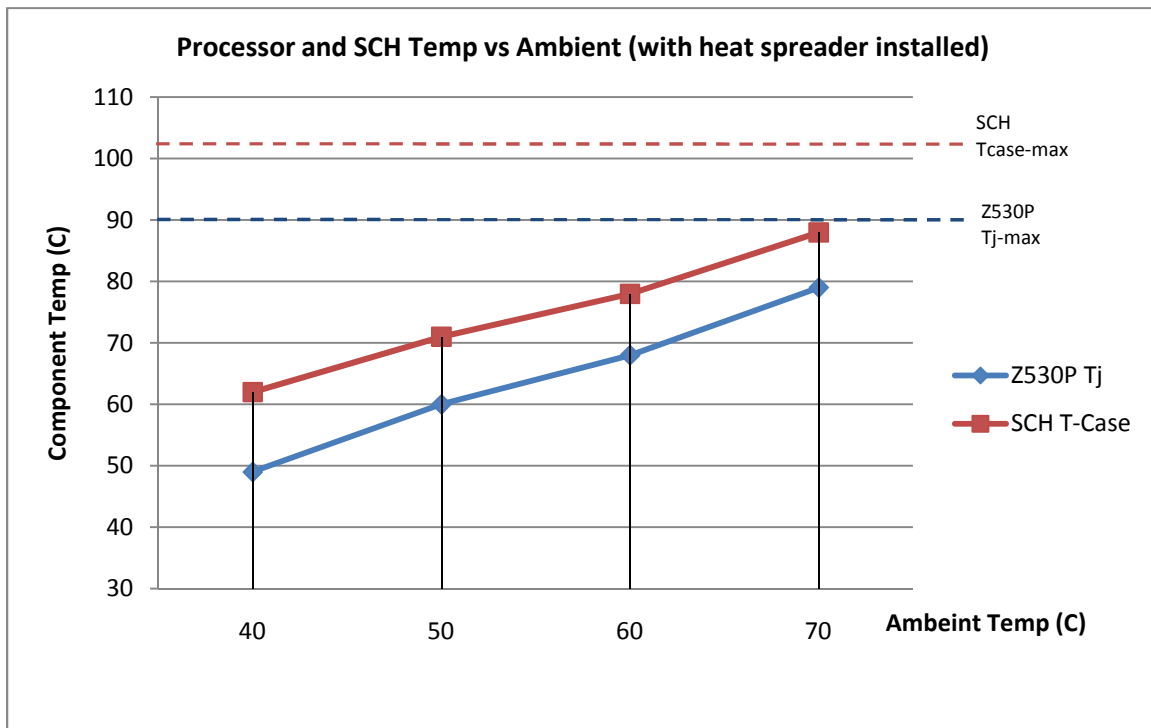
3.1.1.3   Conclusion

It can be seen that running a heavily loaded CB SBC A530P at 100% CPU utilization in a zero air-flow environment without a heat spreader plate and no ACPI passive cooling (throttling), the TCC will become active at an ambient temperature of ~65C. After the ambient temperature increases above 65C, the TM1 and TM2 mechanism prove to be effective at keeping the processor and SCH temperatures within thermal limits for the full commercial ambient temperature range (although at reduced performance). Using the standard ADI heat spreader plate, it can be seen that even under these extreme conditions, the processor and SCH temperatures are maintained well below their limits without activating the TCC.

3.1.2   Heavily Loaded SBC A530P operating at "realistic" CPU Utilization

3.1.2.1   System Configuration

The system setup is very similar to that presented in 3.1 (CB SBC A530P, 2GB SODIMM, 2.5" PATA HDD, micro-SD card, two USB 2.0 devices plus USB keyboard and mouse, Gigabit Ethernet connection, and LVDS flat panel display with backlight in a zero air flow environment). But in this case study, the processor was not run full bore at 100% utilization at all times. Processing loading was varied from ~10% utilization up to ~50% utilization to create an average processor loading between 25 and 30 percent.

3.1.2.2   Results

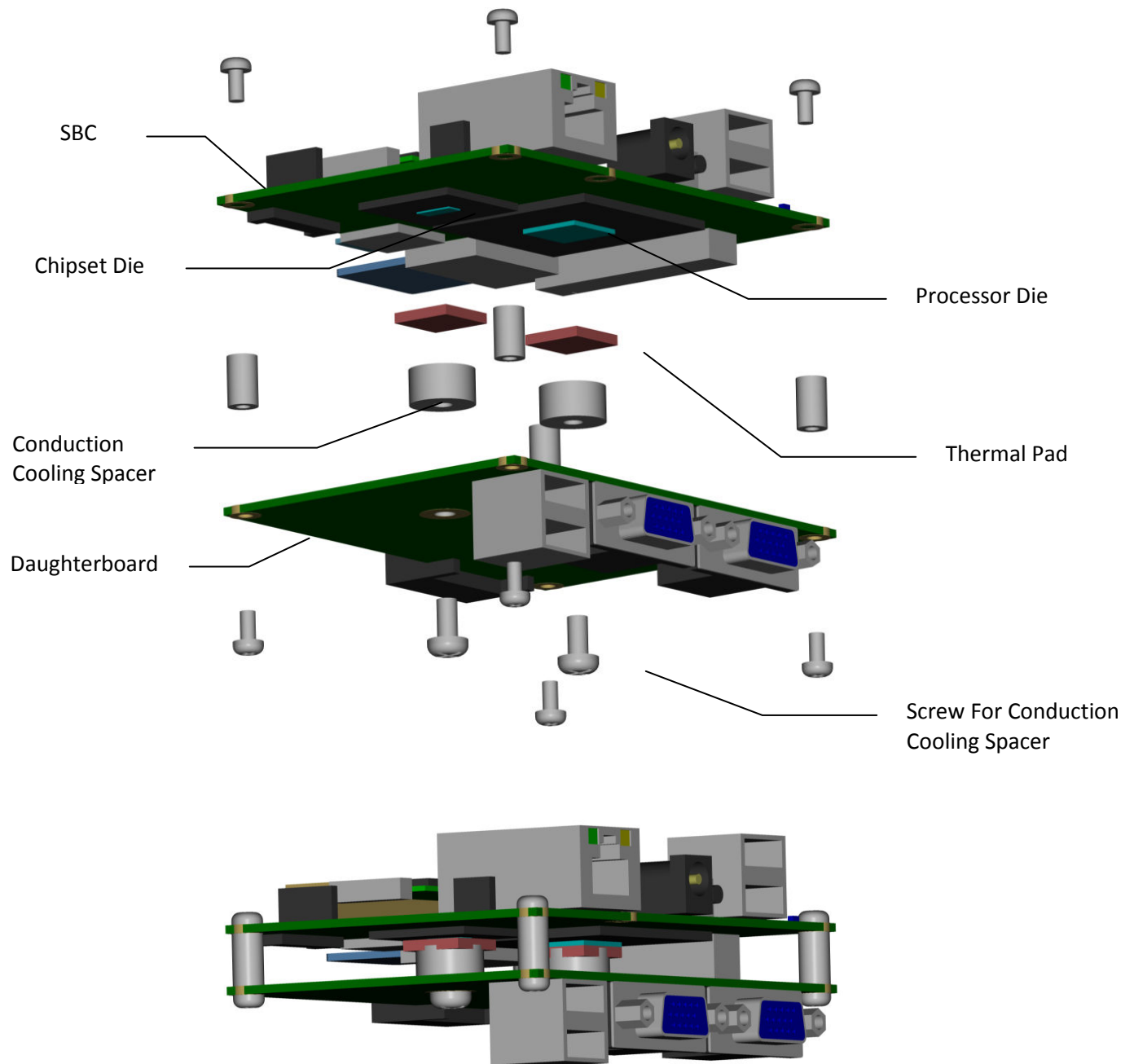| Ambient	Processor Tj	SCH T_{CASE}
70C	88C	96C

3.1.2.3   Conclusion

With this more realistic load profile, it was demonstrated that SCB A530P with a rich set of peripheral devices can operate at the rated commercial temperature range without any passive or active cooling mechanisms. Although operating close to the processors Tj-max, the limit was never reached and therefore the TM1 and TM2 mechanisms did not activate.
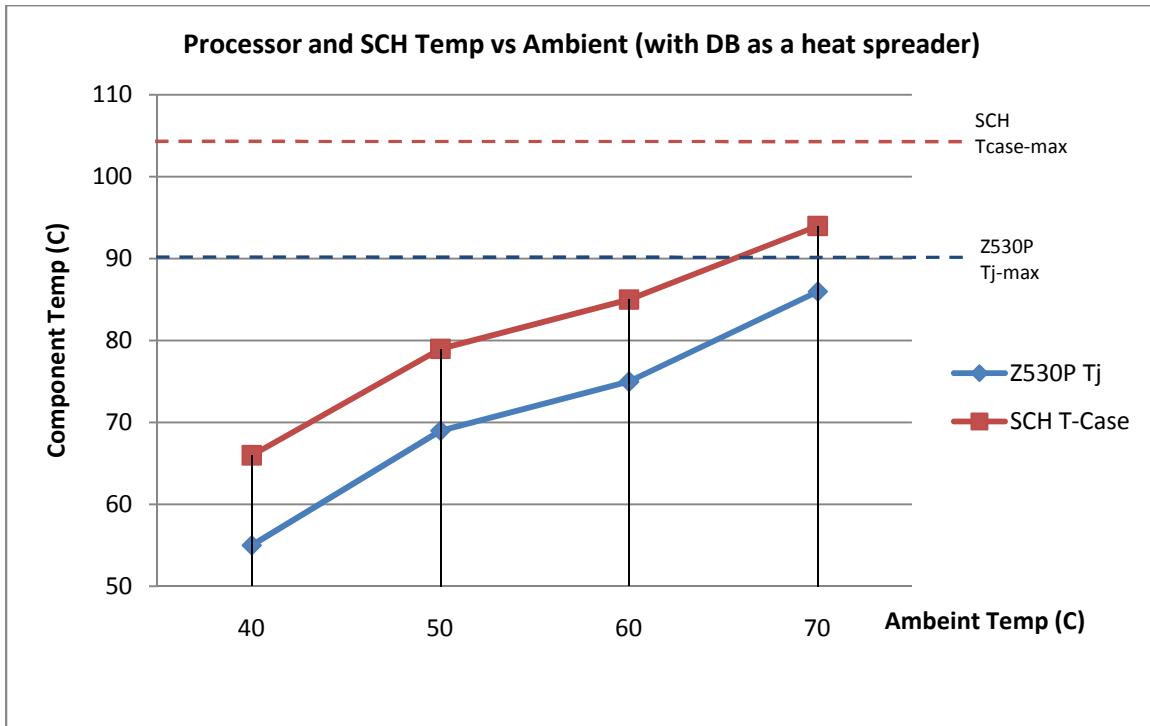
3.1.3   Heavily Loaded SBC A530P operating at 100% CPU Utilization using a VGA/DVI Expansion DB as a heat spreader

3.1.3.1   System Configuration

An Expansion Daughterboard was added to the system studied in 3.1. Between the SBC and it's daughterboard, two spacers and a Thermal interface Material were inserted to conduct heat from the SCH and processor die's into ground planes on the Expansion Daughter Board. See the figure below for an illustration of this SBC / DB mating. The Daughter Board was used to drive a desktop monitor (in addition to the flat panel display) and contained an active Gigabit Ethernet card in its PCIE x1 slot. Much like the test conducted in section 3.1, processor loading was kept at 100% throughout this test case.

SBC

Chipset Die

Processor Die

Conduction
Cooling Spacer

Thermal Pad

Daughterboard

Screw For Conduction
Cooling Spacer

3.1.3.2   Results

Processor and SCH Temp vs Ambient (with DB as a heat spreader)

3.1.3.3   Conclusion

Although the margins are not quite as wide as with the heat spreader plate, this test demonstrates that the Expansion Daughterboard is an effective heat spreader. Even in this extreme case, the processor die temperature and SCH case temperature stayed below their limits without needing to invoke the TCC (TM1/TM2).
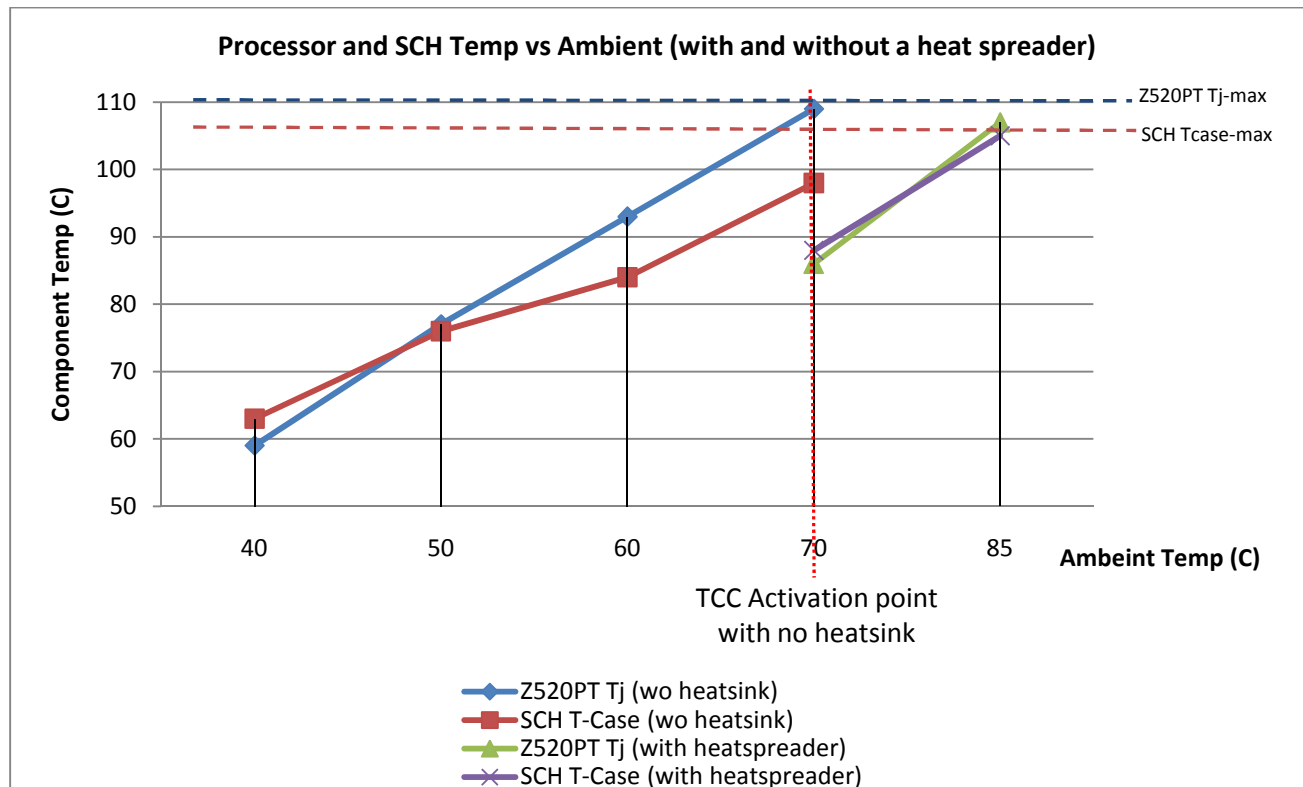
3.2   SBC A520PT Case Study

3.2.1   Heavily Loaded SBC A520PT operating at 100% CPU Utilization

3.2.1.1   System Configuration

The setup for this case study is nearly identical to the system presented in 3.1.1 except the SBC is a high-temp A520PT variant.

3.2.1.2 Results

Processor and SCH Temp vs Ambient (with and without a heat spreader)

3.2.1.3 Conclusion

It can be seen that running a heavily loaded CB SBC A520PT at 100% CPU utilization in a zero air-flow environment without a heat spreader plate and no ACPI passive cooling (throttling), the TCC will active at an ambient temperature of ~70C. For this system, heat-sinking the processor and SCH is required when the ambient temperature is above 70C. With the heat spreader installed, it can be seen that at 85C ambient, the processor and SCH temperatures are maintained below their limits without activating the TCC.

4 CUSTOMER SUPPORT

This section describes the customer support for the product.

4.1 Authorized ADI Engineering Distributors

Primary support for your Cinnamon Bay SBC is provided by the authorized ADI distributor you purchased your product from. Please contact your distributor for technical support, customer service, RMAs or other assistance.

4.2 ADI Engineering Web Site

The ADI Engineering web site contains technical documentation, quick start guides, FCC and CE test reports, and other resources to assist in your usage of Cinnamon Bay SBC.

http://www.adiengineering.com/php-bin/ecomm4/productDisplay.php?category_id=25&product_id=91

4.3 ADI Engineering FTP Site

The ADI Engineering FTP site is a repository for all product documentation, user manuals, software downloads including drivers, patches, etc. Login is anonymous and free.

ftp://ftp.adiengineering.com

4.4 ADI Engineering Message Board

The ADI Engineering Message Board is a public discussion forum for ADI product related technical questions, moderated and answered by ADI technical support staff. Registration to use the Message Board is free.
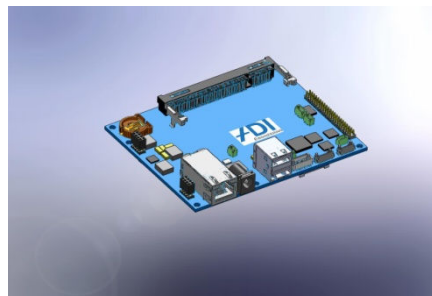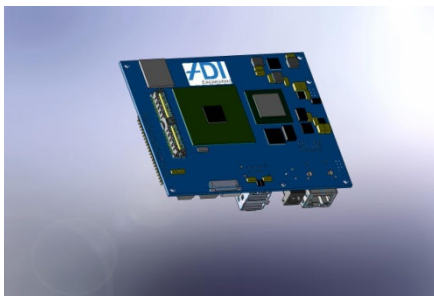
http://www.adiengineering.com/vanilla/

4.5 ADI Engineering Customer Service

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Telephone: 434.978.2888

Hours: 9AM to 5PM EST M-F

4.6 3D Models

ADI Engineering can provide a 3D model of the SBC for a more detailed mechanical analysis.

A. APENDIX I

A Heat Spreader Plate is available from ADI Engineering for the CB SBC family.   The heat spreader plate is an anodized aluminum plate with the same form factor as the SBC. It is connected to the SCH and Processor Die through spacers and a Thermal Interface Material.