

# **AX222**User Manual

[AX222-UM-003-EN]

Rev 0.0.3 January 2012

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# **AX222 SD/MMC/MS Card Reader** Controller



#### **High performance SOC**

#### **USB Features**

- Support USB specification v2.0
- Support USB Storage Class specification v1.0

#### **SD Card Features**

- Support SD specification v2.0
- Support SDHC card up to 32GB
- **Support write protection**
- Support hot plug and removal

#### **MMC Card Features**

- **Support MMC specification v4.2**
- Support MMC card up to 32GB
- Support hot plug and removal

#### MS/MSPRO Features

- Support MS specification v1.43
- Support MSPRO specification v1.03
- Support MS PRO-HG Duo specification v1.01
- Support 1/4/8 bit bus mode
- Support card up to 32GB

#### **LED Driver IO**

**Dual voltage regulator** 

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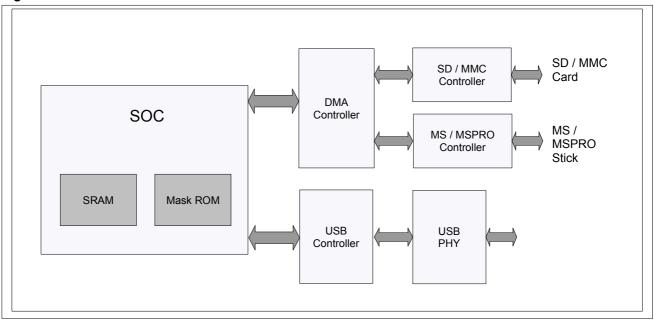
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# **1 Architecture Overview**

# 1.1 System architecture

Figure 1-1: AX222 hardware architecture



# **2 PIN DEFINITIONS**

### 2.1 Pin Assignment

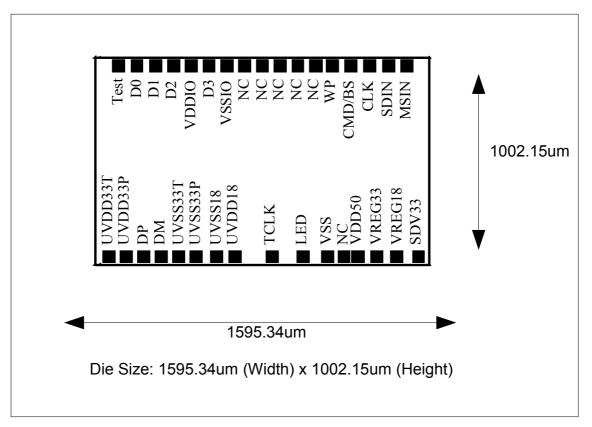


Table 2-1: Pad Coordinates

Pin No.	Name	X-axis (um)	Y-axis(um)
1	UVDD33T	39.8	38.7
2	UVDD33P	123.8	38.7
3	DP	208.4	38.7
4	DM	292.9	38.7
5	UVSS33T	376.2	38.7
6	UVSS33P	460.5	38.7
7	UVSS18	559.9	38.7
8	UVDD18	645.7	38.7
9	TCLK	824.9	38.7
10	P1.2/LED	973.2	38.7

VSS	1093.1	38.7
VDD50/NC	1170.5	38.7
VDD50	1238.4	38.7
VREG33	1328.1	38.7
VREG18	1423.3	38.7
SDV33	1529.0	38.7
P1.3/MSIN	1474.2	942.7
P1.4/SDIN	1385.5	942.7
P1.0/CLK	1295.3	942.7
P1.1/CMD/BS	1203.0	942.7
P1.6/WP	1114.8	942.7
P0.7/NC	1034.8	942.7
P0.6/NC	949.4	942.7
P0.5/NC	863.3	942.7
P0.4/NC	777.9	942.7
P1.7/NC	693.5	942.7
VSSIO	608.0	942.7
P0.3/D3	523.2	942.7
VDDIO	436.8	942.7
P0.2/D2	352.2	942.7
P0.1/D1	265.5	942.7
P0.0/D0	176.6	942.7
P1.5/Test	86.3	942.7
	VDD50/NC VDD50 VREG33 VREG18 SDV33 P1.3/MSIN P1.4/SDIN P1.0/CLK P1.1/CMD/BS P1.6/WP P0.7/NC P0.6/NC P0.5/NC P0.4/NC P1.7/NC VSSIO P0.3/D3 VDDIO P0.2/D2 P0.1/D1 P0.0/D0	VDD50/NC         1170.5           VDD50         1238.4           VREG33         1328.1           VREG18         1423.3           SDV33         1529.0           P1.3/MSIN         1474.2           P1.4/SDIN         1385.5           P1.0/CLK         1295.3           P1.1/CMD/BS         1203.0           P1.6/WP         1114.8           P0.7/NC         1034.8           P0.6/NC         949.4           P0.5/NC         863.3           P0.4/NC         777.9           P1.7/NC         693.5           VSSIO         608.0           P0.3/D3         523.2           VDDIO         436.8           P0.2/D2         352.2           P0.1/D1         265.5           P0.0/D0         176.6

# 2.2 Pad Descriptions

Name	Pad #	Nature	Functions
UVDD33T	1	Р	PHY analog power input (Double-bond with UVDD33P)
UVDD33P	2	Р	PHY analog power input (Double-bond with UVDD33T)
DP	3	Ю	USB D+
DM	4	Ю	USB D-

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LIVECCAT		Ъ	DIIV analog ground (Dauble hand with LIV/CCCCD)	
UVSS33T	5	P	PHY analog ground (Double-bond with UVSS33P)	
UVSS33P	6	Р	PHY analog ground (Double-bond with UVSS33T)	
UVSS18	7	Р	1.8V Digital power ground	
UVDD18	8	Р	1.8V Digital power input	
TCLK	9	I	Test mode external clock	
P1.2/LED	10	Ю	Port 1 pin 2 – LED0 indication or serial port	
vss	11	Р	Regulator ground	
VDD50/NC	12	Р	NC	
VDD50	13	Р	Regulator 5V power input	
VREG33	14	Р	Regulator 3.3V power output (for external capacitor connection)  Note: VREG33 is short-circuit with VDDIO	
VREG18	15	Р	Regulator 1.8V power output (for external capacitor connection)	
SDV33	16	Р	SD/MMC/MS card output 3.3V power	
P1.3/MSIN	17	Ю	Port 1 pin 3 – MS card insertion indication signal	
P1.4/SDIN	18	Ю	Port 1 pin 4 – MDC card insertion indication signal	
P1.0/CLK	19	Ю	Port 1 pin 0 – MDC/MS clock	
P1.1/CMD/BS	20	Ю	Port 1 pin 1 – MDC command, MS BS	
P1.6/WP	21	Ю	Port 1 pin 6 – MDC write protect	
P0.7/NC	22	Ю	Port 0 pin 7 – NC	
P0.6/NC	23	Ю	Port 0 pin 6 – NC	
P0.5/NC	24	Ю	Port 0 pin 5 – NC	
P0.4/NC	25	Ю	Port 0 pin 4 – NC	
P1.7/NC	26	Ю	Port 1 pin 7 – NC	
VSSIO	27	Р	Digital ground	
P0.3/D3	28	Ю	Port 0 pin 3 – MDC/MS data 3	
VDDIO	29	Р	Digital I/O 3.3V power input	
P0.2/D2	30	Ю	Port 0 pin 2 – MDC/MS data 2	
P0.1/D1	31	Ю	Port 0 pin 1 – MDC/MS data 1	
P0.0/D0	32	Ю	Port 0 pin 0 – MDC/MS data 0	
P1.5/Test	33	IO	Port 1 pin 5 – Test Pin	

### **3 DIE SCHEMATICS**

#### 3.1 SD/MMC/MS 4-bit Mode

Figure 3-1: Valid pads for SD/MMC/MS 4-bit mode

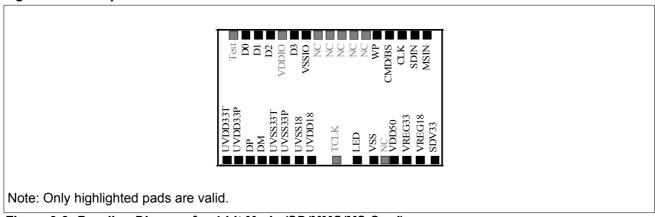


Figure 3-2: Bonding Diagram for 4-bit Mode (SD/MMC/MS Card)

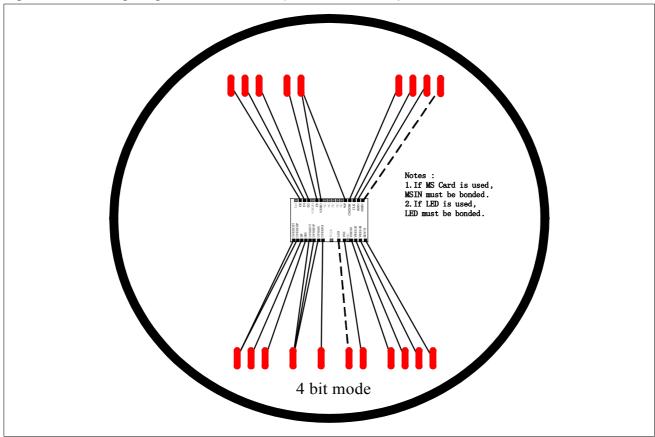
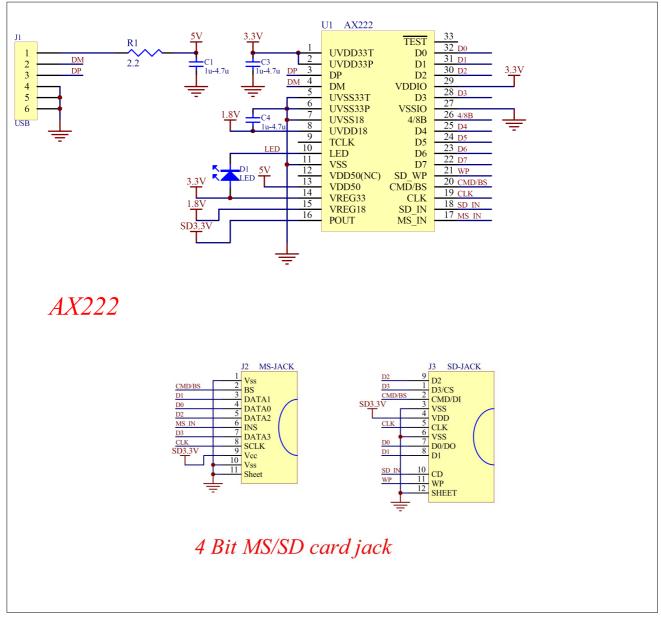


Figure 3-3: Schematic for SD/MMC/MS 4-bit mode



#### Note:

- 1. Choose R1, C1, C3 and C4 according to your needs. Lower value can minimize cost, while a higher value can provide stability.
- 2. Place C3 close to pin 2, and C4 close to pin 11. Routing for 3.3V and 1.8V should be as short as possible.

3. NC = Not Connected.

### 3.2 Electrical Characteristics

Table 3-1: Absolute maximum ratings

Symbol	Descriptions	Min	Тур	Max	Units	Conditions
V <sub>ESD</sub>	Electrical Discharge Voltage	-	Passed 8k	-	V	
T <sub>STOR</sub>	Storage Temperature	-40	-	125	°C	
T <sub>AMB</sub>	Ambient Temperature	0	-	70	°C	

Table 3-2: Electrical Characteristics (Standard testing condition at 25°C)

Symbol	Descriptions	Min	Тур	Max	Units	Conditions
USBVDD	USB supply voltage	4.5	5	5.5	V	
I <sub>DD</sub>	Operating current		56	-	mA	No cards inserted
I <sub>SUP</sub>	Operating current at suspend mode	-	0.37	-	mA	No cards inserted
Operating current with SD card inserted		-	62	-	mA	No read/write operation

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Table 3-3: Oscillator Characteristics (Standard testing condition at 25°C)

Symbol	Descriptions	Conditions	Min	Тур	Max	Units
F <sub>DT</sub>	MCLK Frequency	Data transaction mode	-	-	48	MHz
F <sub>ID</sub>	MCLK Frequency Identification mode		-	-	235	KHz
T <sub>SET</sub>	COMMAND/DAT setup time		6	-	-	ns
T <sub>HOLD</sub>	COMMAND/DAT hold time		3	-	-	ns
T <sub>DELAY</sub>	COMMAND/DAT output	Data transaction mode	-	-	14	ns
dela	delay time	Identification mode	-	-	50	ns

Figure 3-4: Timing diagram for SD/MMC normal speed read/write operation

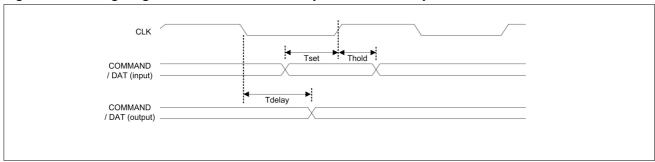
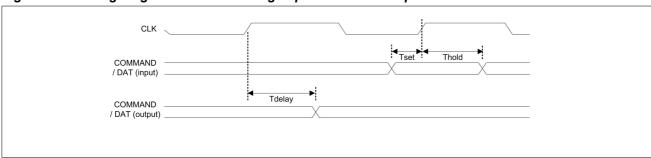
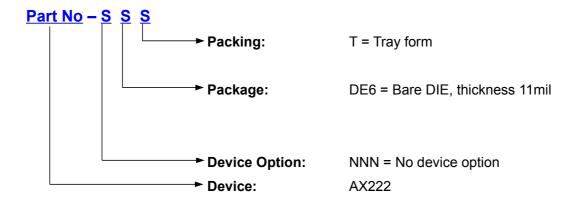


Figure 3-5: Timing diagram for SD/MMC high speed read/write operation



# 4 Ordering Code



Ordering Code	Brief Description	
AX222-NNNDE6T	Bare 11mil	

Please contact sales office (<u>sales@appotech.com</u>) for ordering procedures.

# 5 Appendix I Revision History

Date	Version	Comment	Revised by
2010-12-07	0.0.1	<ol> <li>Change Format</li> <li>Rename to AX222</li> </ol>	Rimsky Cheng
2010-08-11	0.0.2	Add ordering code	Erica Cheong
2012-01-18	0.0.3	1. Update logo	Karen Keung

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