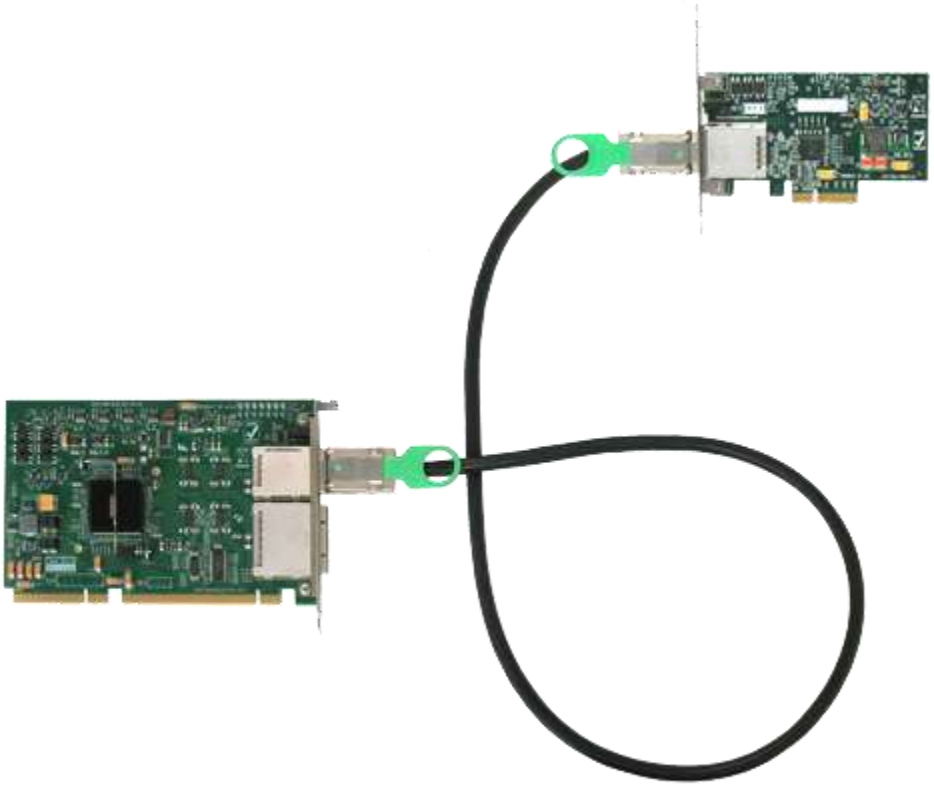


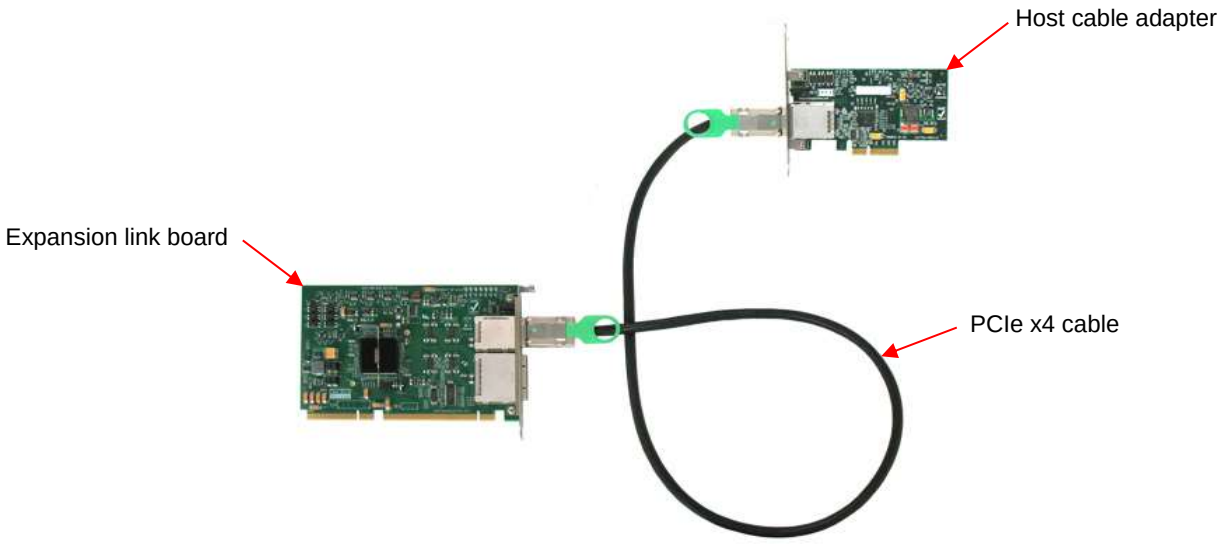
User Manual,
Expansion Kit, Server To SHB Backplane

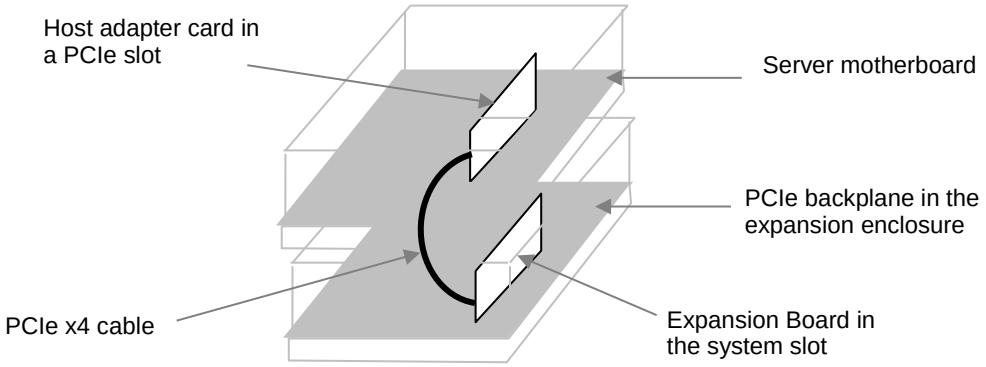
(OSS-KIT-EXP-1500)

Table of Contents

1.a. Description

The PCIe x4 Gen 2 expansion kit is used to extend the PCI express bus from a host server to an external expansion chassis. The host adapter card installs into a PCIe x4, x8, or x16 slot of the server mother board. It then cables to a downstream expansion board and installs in the SHB slot of the backplane and provides primary fan-out switch to support multiple configurations of PCI express expansion slots.

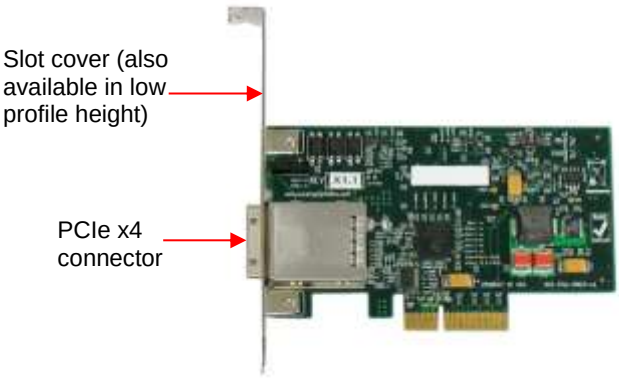


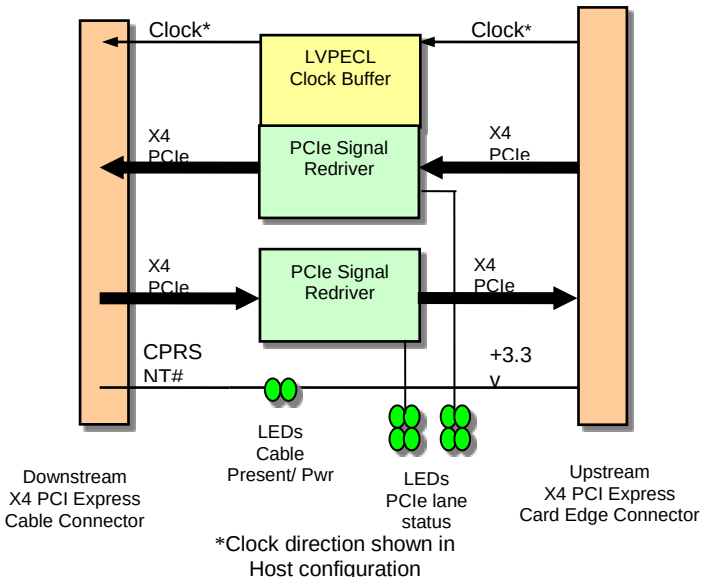


2. Components

2.a. Host cable adapter

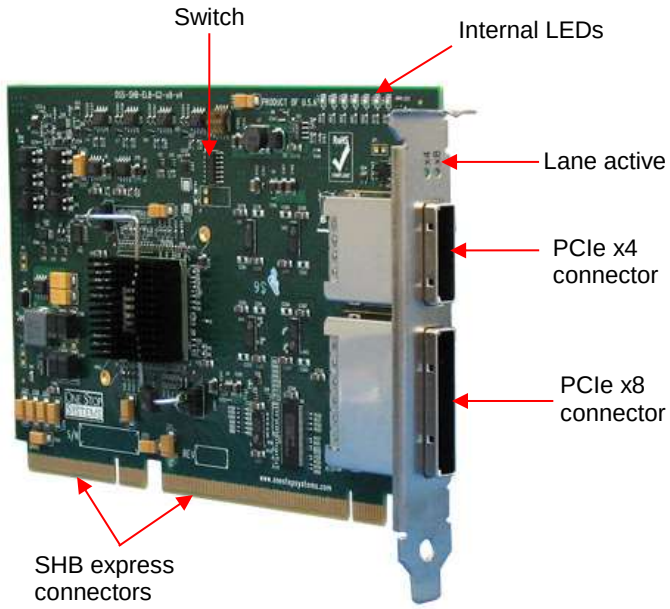
The PCIe x4 host adapter inserts into the host computer's PCIe x4, x8 or x16 slot.

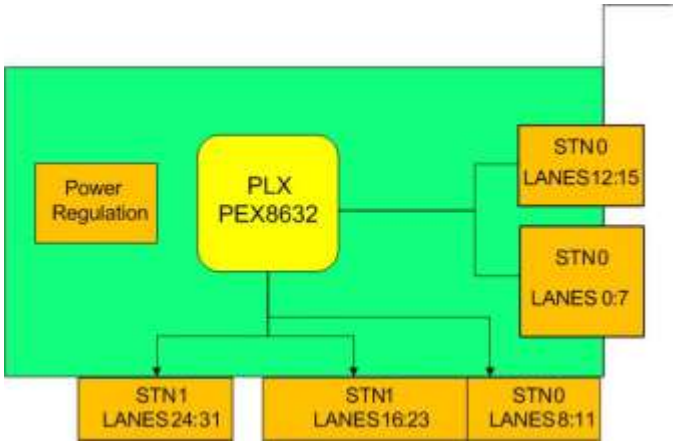




2.b. Expansion link board

The expansion link board installs in the extending or system PCIe goes to all available slots on the expansion backplane and can control multiple configurations of PCIe expansion slots.





2.c. Host Adapter Specifications

Electrical/Mechanical Specifications	
Form Factor:	PCIe x4 add-in card
Dimensions (H x L):	2.2 x 4.5 inches (55 x 114mm)
Front Panel Connectors:	One PCIe x4 cable connector
Front Panel Indicators:	Power On / Cable Present LEDs
Power Consumption (designed to meet the following conditions) 3.75W typical, 3.3@1.3A	
Operating Environment (designed to meet the following conditions)	
Temperature Range:	0° to 50°C (32° to 122°F)
Relative Humidity:	10 to 90% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Redriver: Pericom PI2EQX5804	
Agency Compliance: UL60950.FCC Class B, CE safety and emissions	

2.d. Expansion link board specifications

Form Factor	• MPIC1.3 G SHB Express system slot compliant
Slot Type	System slot for the expansion chassis
Dimensions (H x L)	4.375 x 6.600 in (111 x 161 mm) 1 slot wide
Switch	PLX PEX8632 32 lane switch
Upstream Interface	x8 PCI Express over cable
Downstream Interface	20 lanes of PCI Express are auto configurable on the card edge connectors as: • One x16 and one x4 PCIe links • Two x8 and one x4 PCIe links • Five x4 PCIe links
Front Panel Connector	Molex 75586-0007(8) and 75586-0010(x4)
Front Panel Indicators	• 8 Upstream Lane Active Indicators (Green)
Internal Indicators	• Power In-range Indicators for +12V, +3.3V & VTT (Red/Green) • Power on indicator for +1V (Green) • Bank of 5 board status indicators (Red)
Optional Features	• Switch Control: 3 banks of DIP switches for PEX8632 configuration • Switch Debug Port: Internal JTAG communications header • Heat Sink:On-board fan header provided for optional heat sink fan
Power Consumption	• 9W typical, 11.4W max • +12V @ 0.675A max, 3.3V @ 1.0 A max, 5Vaux @ 2.5mA max
Designed to meet the following	• Temperature Range:0° to 55 °C (32° to 122°F) • Relative Humidity:10 to 90% non-condensing • Shock:30g acceleration peak (11ms pulse) • Vibration: 5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration • Pending Compliance:UL 60950, FCC Class B, CE safety and emissions

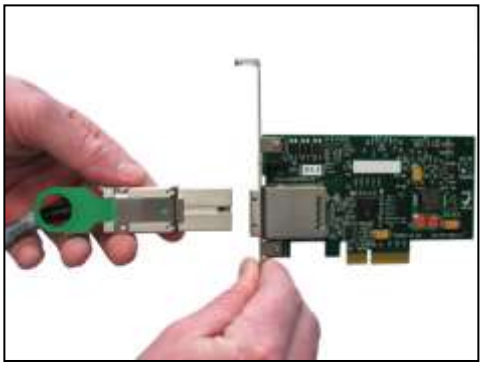
3. Installation Instructions

3.a. Installing the Adapter Kit

1) Insert the host cable adapter into an appropriate PCIe slot of the host computer. NOTE: For example, a PCIe x8 host board can be inserted into a PCIe x4, x16 or a x8 slot. It will still operate at x4 speeds.

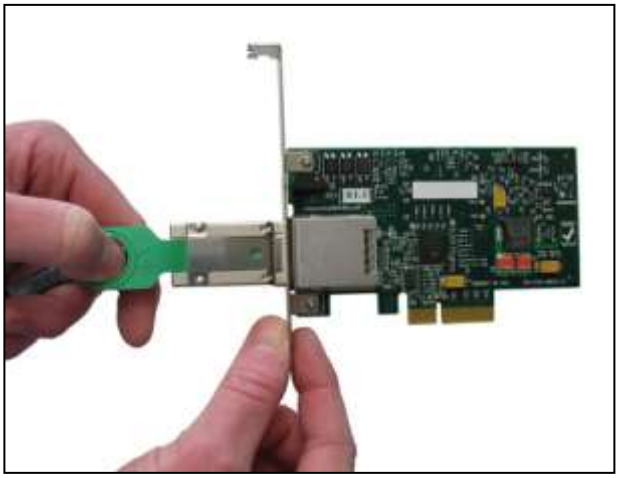
3.b. When using with the 2-slot Backplane:

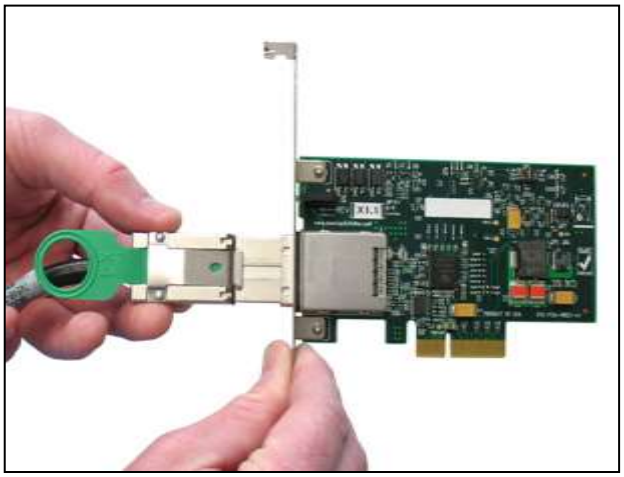
2) Insert the expansion link board into the SHB slot on the chosen backplane.
3) Connect the PCIe cable to both cable adapters.
    a) Pull back on tab, lifting prongs that insert in the holes on the PCIe connector.
    b) Push in the connector
    c) Release green thumb tab insuring that the prongs are fully engaged in the mating connector.
    d) Test by pulling back on the connector



3.d. Removing PCIe cable:

1) To remove PCIe cable pull back on green thumb tab to release metal pins and gently separate.





4. Technical Information

The transmit and receive signals on the OSS-HIB25-x4 are driven and conditioned by Pericom redriver chips. Adjustments can be made to equalization, de-emphasis and output swing. These controls are factory set by the use of zero Ohm resistors. In the following tables a 0 indicates that a zero Ohm resistor has been installed and a 1 indicates no resistor. In rare cases, mostly where non-OSS equipment is used with the OSS-HIB25-x4, these adjustments may need to be changed. The following tables are made available for this purpose. It is highly recommended to contact OSS customer support before making changes to these settings.

4.a. Signal Adjustment

Equalizer Selection

SEL_ 2[A:D]	SEL_ 1[A:D]	SEL_ 0[A:D]	@1.25 GHZ	@2.5 GHZ	
0	0	0	0.5dB	1.2dB	Edge Default
0	0	1	0.6dB	1.5dB	
0	1	0	1.0dB	2.6dB	
0	1	1	1.9dB	4.3dB	
1	0	0	2.8dB	5.8dB	
1	0	1	3.6dB	7.1dB	Cable Default
1	1	0	5.0dB	9.0dB	
1	1	1	7.7dB	12.3dB	

De-emphasis Adjustment

D2_[A:D]	D1_[A:D]	D0_[A;D]	De-emphasis	
0	0	0	0dB	SW=ON Default
0	0	1	-2.5dB	
0	1	0	-3.5dB	
0	1	1	-4.5dB	
1	0	0	-5.5dB	
1	0	1	-6.5dB	SW=OFF Default
1	1	0	-7.5dB	
1	1	1	-8.5dB	

Output Swing Control

S_1[A:D]	S_0[A:D]	Swing (Diff. VPP)	
0	0	1V	Cable Default
0	1	05V	
1	0	0.7V	Edge Default
1	1	0.9V	

4.b. Pin Assignments

Host and Target card connectors PCIe x8 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Operation:

1) Plug in expansion system and turn the power supply on.
2) Power up host computer.
3) The expansion system will power up.

Pin-out for the PCIe x4 Card Edge Connector on the Host Cable Adapter

Pin #	Side B		Side A	
	Name	**Description**	**Name**	**Description**
1	N/C	N/C	PRSNT1#	Hot-Plug presence detect
2	N/C	N/C	N/C	N/C
3	N/C	N/C	N/C	N/C
4	GND	Ground	GND	Ground
5	NC	N/C	N/C	Not connected
6	N/C	N/C	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	N/C	Not connected
9	N/C	Not connected	N/C	Not connected
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	N/C	N/C	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

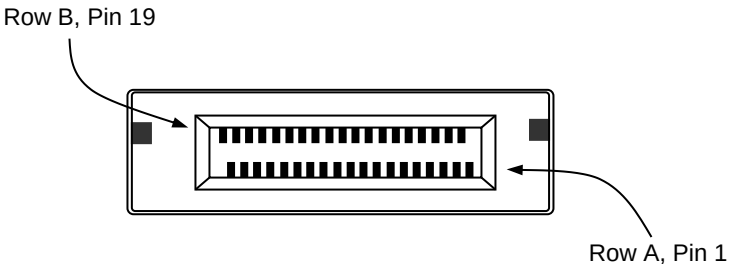
Notes:
1. Optional signals that are not implemented are left as no connects on the board side connector.

2. Reserved signals are no connects on the board side connector.

3. Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4. Board side pin-outs on both sides of the Link are identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

4.c. PCI Express x4 Connector Pin Assignment



4.d. Pin-out for the PCIe x4 Cable

Pin #	Cable Side 1		Cable Side 2	Pin #
A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6

Pin #	Cable Side 1		Cable Side 2	Pin #
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLK+	Differential Pair	CREFCLK+	A14
A15	CREFCLK		CREFCLK-	A15
A17	SB_RTN	Hook-up Wire	SB_RTN	A17
A18	CPRSNT#	Hook-up Wire	CPRSNT#	A18
A19	CPWRON	Hook-up Wire	CPWRON	A19
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NC	PWR	B14
B15	PWR	NC	PWR	B15
B16	PWR_RTN	NC	PWR_RTN	B16
B17	PWR_RTN	NC	PWR_RTN	B17
B18	CWAKE#	Hook-up Wire	CWAKE#	B18
B19	CPERST#	Hook-up Wire	CPERST#	B19
Back shell	Chassis Ground	Overall Cable Braid	Chassis Ground	Back shell

4.e. Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset

4.f. Expansion link board switch settings

Downstream PCIe ports hardware strapping logic

CFG(0:2)			BP PORT CFG				
0	1	2	A0	A1	A2	A3	B0
0	0	0	x4	x4	x4	x4	x4
0	1	0	x8	0	x4	x4	x4
0	1	1	x8	0	x8	0	x4
1	x	x	x16	0	0	0	x4

5. Ordering Information

OSS-KIT-EXP-1500

OSS-KIT-EXP-1500 kit includes a PCIe x4 Gen 2 host cable adapter, a PCIe x4/x8 expansion link board, and a PCIe x4 2M cable.