Appendix A, B, E and G

Appendix A – EOS 09-0043 FUN-LV Dual-terminal Power Electronics Device

Appendix B – EOS 09-0042 FUN-LV Multi-terminal Power Electronics Device

Appendix E – Testing of Soft Open Point PED

Appendix G – Autonomous Power Transfer Report

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ENGINEERING OPERATING STANDARD

EOS 09-0043

FUN-LV DUAL TERMINAL POWER ELECTRONICS DEVICE

Network(s): LPN and SPN

Summary: This document provides guidance and information in the operation of dual-terminal power electronics devices (PED) in London and Brighton installed for the Flexible Urban Networks-LV (FUN-LV) project. It provides the procedures necessary to avoid danger and allow safe working.

Owner:	Peter Lang	**Date:**	13/04/2015
Approved By:	Barry Hatton	**Approved Date:**	28/04/2015

This document forms part of the Company's Integrated Business System and its requirements are mandatory throughout UK Power Networks. Departure from these requirements may only be taken with the written approval of the Director of Asset Management. If you have any queries about this document please contact the author or owner of the current issue.

Applicable To

UK Power Networks

- ☐ All UK Power Networks
- ☒ Asset Management
- ☒ Capital Programme
- ☒ Connections
- ☒ HSS&TT
- ☒ Network Operations
- ☐ UK Power Networks Services
- ☒ Other

External

- ☐ G81 Website
- ☐ Contractors
- ☐ ICPs/IDNOs
- ☐ Meter Operators

Revision Record

Version	1.0	**Review Date**	28/04/2016
Date	13/04/2015	**Author**	Peter Lang
New document to cover the approval of the Dual-Terminal Power Electronics Device to be connected to LV Networks.			
Version		**Review Date**	
Date		**Author**	

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1 Introduction

The overarching aim of the Flexible Urban Networks - LV (FUN-LV) project is to explore the use of power electronics to enable deferral of reinforcement and facilitate the connection of low carbon technologies and distributed generation in urban areas, by meshing existing radial networks, and by removing boundaries within existing meshed networks. The project will do this by trialling three different types of power electronics device, that is, Methods 1, 2 and 3 across 36 trial sites, 24 in London and 12 in Brighton.

The dual-terminal power electronics device (PED), as specified in EDS 09-0040 'Dual Terminal Power Electronics Device', is the project's Method 2. Four units will be installed in the interconnected LV networks of London, four units in the radial London LV network and four units in the radial Brighton LV network. Each PED is installed on the pavement and shares the capacity between two substations. The transformer demand is monitored at each substation and is sent to the PED that determines whether capacity sharing is required.

LV monitoring systems have been installed at each substation in the trial to determine the demand of the transformer and guard the current flow of the "spine" circuit.

Figure 1 - Visualisation of PED installed on pavement

2 Scope

This standard has been published because UK Power Networks is installing novel LV power electronics devices into distribution substations in London and Brighton as Soft Open Points, which allow capacity sharing without increasing the fault level. These devices are novel and as such are not covered by any existing manuals or guidance documents. Operational staff and Network Control need to know what to do to ensure safety is maintained.

The expectation is that if a PED needs to be maintained or replaced then Turbo Power Systems (the Supplier) will carry out the actual work. UK Power Networks' operational staff will isolate and make the equipment safe before it is maintained.

This document does not cover the installation or commissioning of the PED.

This document is intended for internal use only.

3 Glossary and Abbreviations

Term	Definition
CB	Circuit Breaker
DMS	Distribution Management System
Ellipse	UK Power Networks' asset register soon to be integrated into SAP as per Business Transformation.
FUN-LV	Flexible Urban Networks - LV
HMI	Human Machine Interface
IGBT	Insulated Gate Bipolar Transistor
LCNF	Low Carbon Networks Fund
LPN	London Power Networks
NetMap	UK Power Networks' graphical information system (GIS).
PED	Power Electronics Device
PLC	Programmable Logic Controller
PowerOn fusion	UK Power Networks' network management system.
RTU	Remote Telemetry Unit
S/S A	This substation is the one where the PED is normally installed.
S/S B and S/S C	These substations are the donor substations connected via the Spine circuits.
SCM Server	Software Configuration Management Server
SOP	Soft Open Point
SPN	South Eastern Power Networks
UK Power Networks	UK Power Networks (Operations) Ltd consists of three electricity distribution networks: • Eastern Power Networks plc (EPN). • London Power Network plc (LPN). • South Eastern Power Networks plc (SPN).
VT	Voltage Transformer or Voltage Transducer

4 Definitions

Soft Open Point	A point on the network where two networks are joined together to share capacity without increasing the prospective short circuit current.
Spine circuit	This is the LV feeder that joins two distribution substations together to enable capacity sharing. Based on LPN interconnected LV network design terminology.
Supplier	Turbo Power Systems (TPS)

5 Basic Description

The dual-terminal PED consists of two 240kW inverters joined to a common dc busbar and a neutral inverter. The power converters are mounted directly on the reverse side of the heat sink. The PED is forced air cooled. The basic operation of power electronics is described in Appendix C.

The cabinet comprises five enclosures: one control; two filter; and two inverter enclosures.

The PED controller receives measured demand values from remote substations and local analogues. An algorithm developed by Imperial College takes these values and determines which function should be delivered.

The expected functions are:

1. Real power transfer;
2. Reactive power support;
3. Voltage support;
4. Power factor correction and improvement;
5. Phase imbalance improvement;
6. Loss reduction;
7. Harmonic content improvement.

Current can be taken from and exported to either inverter. The neutral inverter is required to perform the advanced functions 4 - 7. The neutral inverter is housed in one of the main converter enclosures. The overall dimensions of the cubicle are length 1200mm, height 1586mm and depth 800mm. All enclosures are designed to meet IP65.

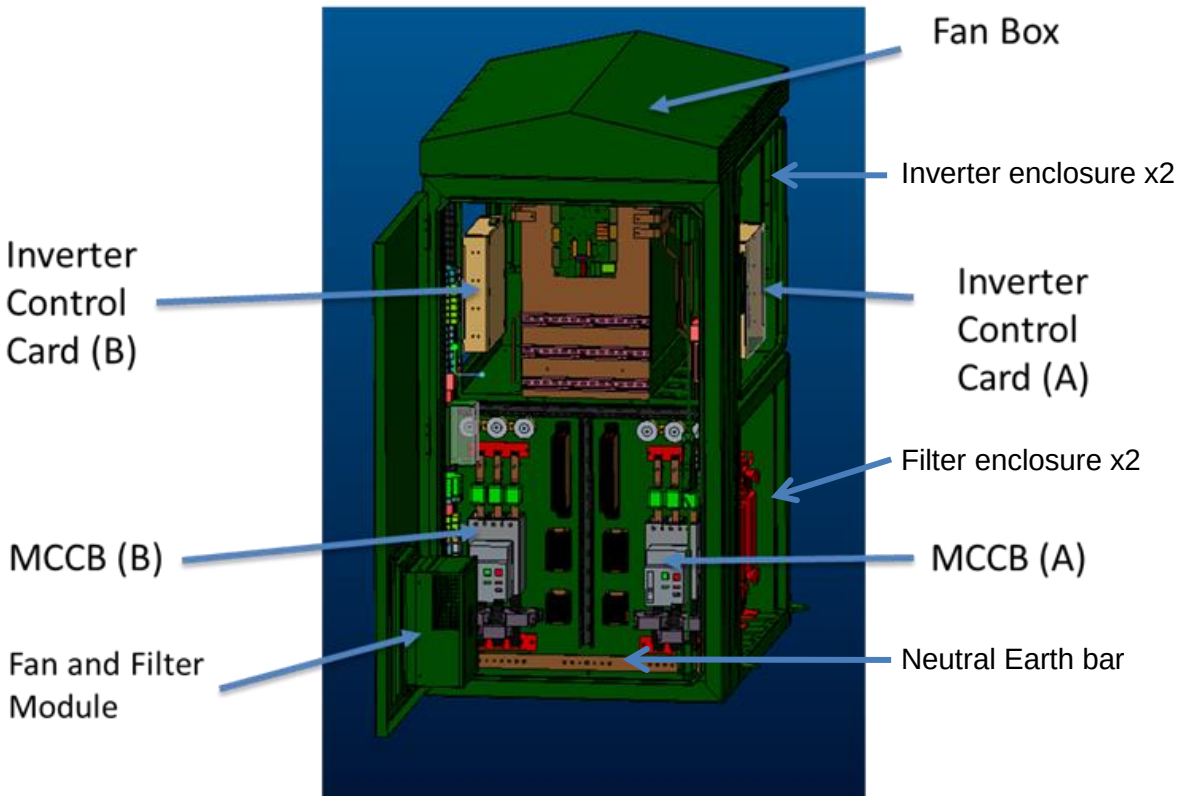


Figure 2 - Control Enclosure Internal View

6 Site Locations

The aim of the FUN-LV project is to carry out the assessment of benefits to be expected by the installation of the PEDs. LV monitoring devices will be installed in the substations listed below to provide the necessary evidence to complete the business case and demonstrate that power electronics is able to realise benefits when connected to a LV network.

Table 1 – SPN radial sites

ID	S/S A	S/S B
2.1	523338 - Duke Street [T1]	523653 - Churchill Square East [T2]
2.2	523446 - Frederick Street [T1]	522075 - North Gardens [T1]
2.3	523099 - West Hill Road [T2]	524252 - Buckingham Street [T1]
2.4	523547 - St. Margarets Place [T2]	523623 - Cannon Place [T1]

Table 2 – LPN radial sites

ID	S/S A	S/S B
2.1	90940 - Electric Ave R/O 37	90941 - Electric Lane Ex Supermarket
2.2	67059 - Sutherland Road Brodwick House	67052 - Roman Road R/O Dennis House
2.3	06287 - Morden Road West	06507 - Morden Rd 141
2.4	91045 - Loughborough Park GPO Depot	91043 - Loughborough Park Guinness

Table 3 – LPN interconnected sites

ID	S/S A	Affected Sites
2.1i	31529 - Piccadilly Ritz Hotel	36300 - Berkeley St 40-50 31550 - Stratton St Stratton Hse
2.2i	36611 - Arlington St Arlington House No2 (RES)	31463 - Arlington St 20 Arlington Hse 31464 - Arlington St 9-10
2.3i	36041 - Duke Of York St 11-14	34673 - Jermyn St Princes Hse 31516 - Piccadilly 177 French Railways 31518 - Piccadilly 203 Simpsons 36540 - Piccadilly 200 34987 - Jermyn St 85-87
2.4i	36785 - Portman Close 26-34 (RES)	34123 - Portman Sq 14 Fitzhardinge Hse 34145 - George St 67-69 34665 - Baker St 18-20

7 Access

On the external doors of each of these substations a label will be placed informing operational staff that this substation is part of the FUN-LV trial. Labels will also be placed in link boxes indicating that that link box is part of the FUN-LV demonstration and the control engineer should be contacted before any linking takes place. Copies of these labels are contained in Appendix B.

The pavement mounted PED will have locked doors on three sides. The control enclosure door allows access to the circuit breakers. The larger side doors have the power electronics components and active filters. Secondary isolation barriers are present behind each door to prevent contact with live parts when doors are open.

8 Method of Connection

A 185mm^2 cable will be terminated into the lower main enclosure. The flexible copper connections pass through into the control enclosure where the circuit breakers are housed.

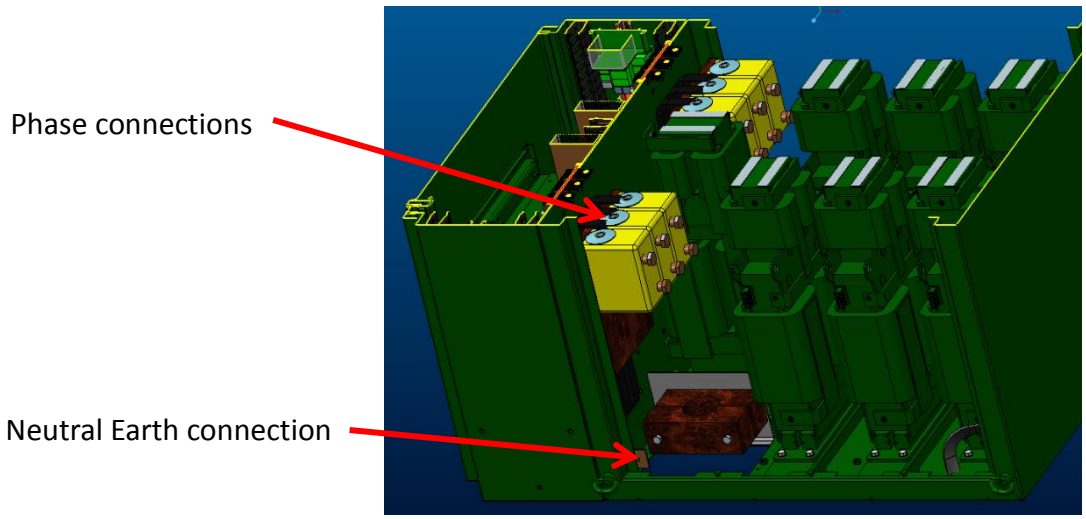


Figure 3 - Cable entry (mirrored on other side)

9 Air Cooling

The PED is forced air cooled with unfiltered air being drawn in from the bottom, passed over the filters and inverters and vented from the top. Filtered forced air passes through the control enclosure and the internal heat sink surface.

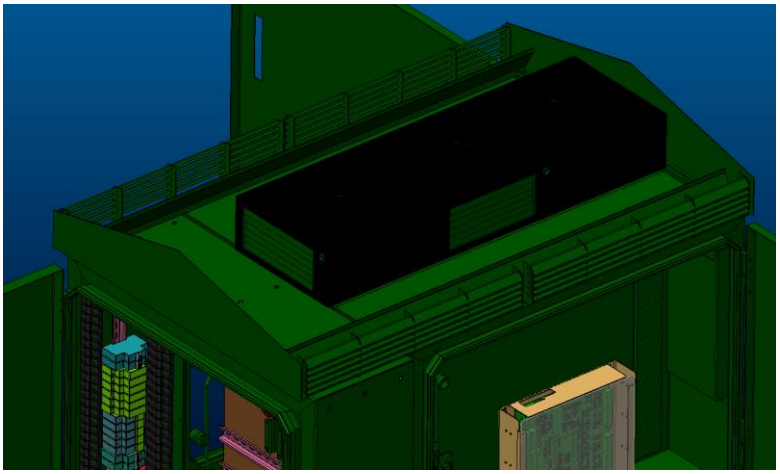


Figure 5 - Fan Box With Top Skin Removed to Show Internal Fan Plenum Chambers

Figure 4 - Long-life fans positioned in fan box

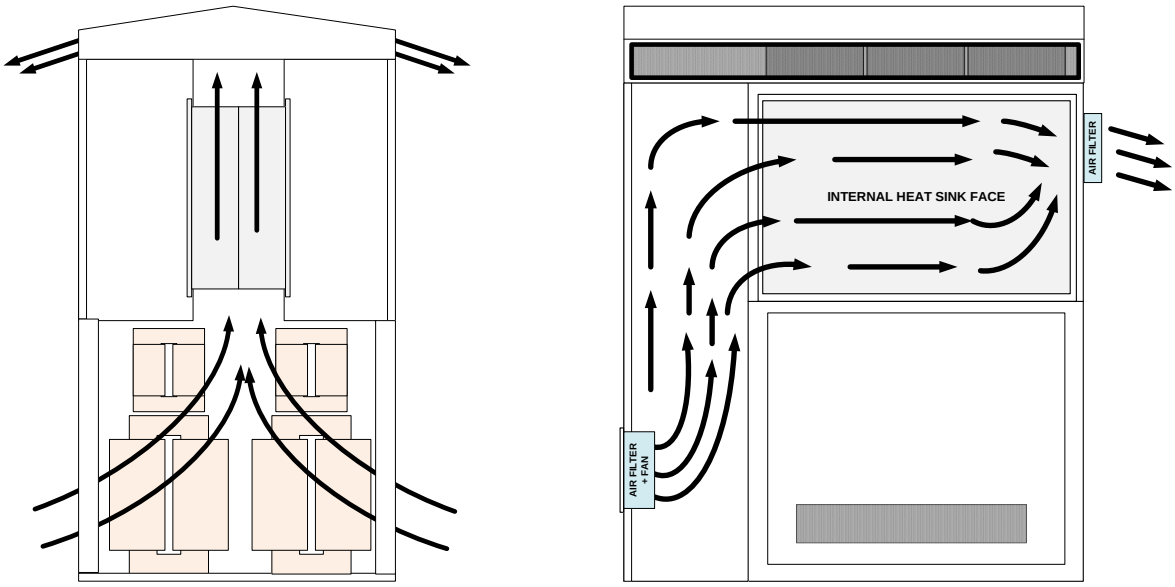


Figure 6 - Forced air cooling arrangements (Unfiltered and filtered for power electronics)

10 Maintenance

The maintenance strategy is one of substitution where if there is faulty equipment, the whole cubicle will be disconnected from the underground cables and replaced. The faulty unit will be sent to the Supplier for repair.

11 LV Monitoring Systems

An Ormazabal or GMC-I Prosys LV monitoring system is being used to monitor the real and reactive power demand on each transformer as well as flowing through the spine circuits. This system is reusing legacy equipment from a previous LCNF project and new single card monitoring units, each with a 3G communications link. EOS 01-0053 'Installation and Operation of Monitoring Equipment on LV Distribution Equipment' describes the methods of installation, operation and decommissioning.

In the case of open boards where the LV transformer tails are safely accessible to fit the Rogowski current sensor, then one monitor will monitor the transformer demand and a second will monitor the spine circuit.

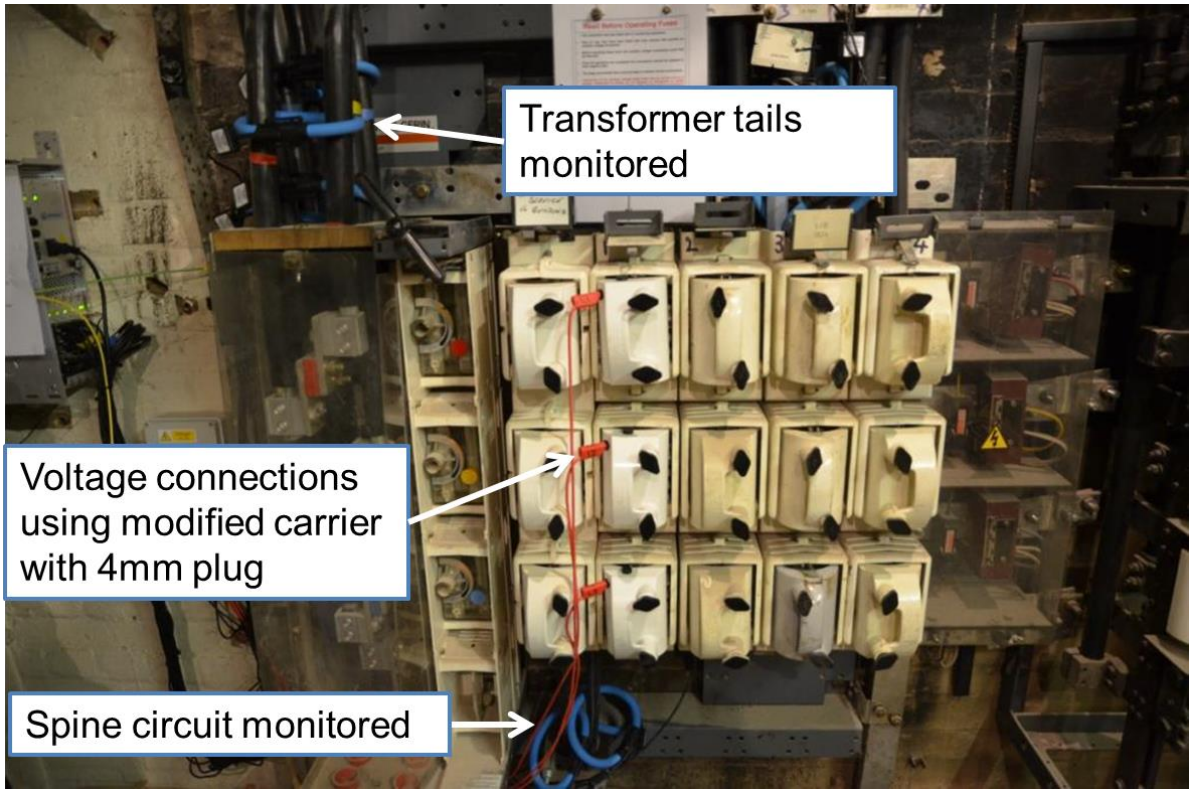


Figure 7 - LV monitoring for both substations

In the case of confined modern pillar where access to the transformer tails is difficult, then all the outgoing ways will need to be monitored. Legacy four card monitoring units will be reused in this situation.

Under normal operations it should not be necessary to remove the Rogowski coils. However to measure real and reactive power a voltage measurement is required. The modified fuse carrier with 4mm plug should be used with the spine circuit. In the event that a modified fuse carrier needs to be removed (following the procedure in EOS 01-0053), the PED will be disabled beforehand by the Control Engineer. It is essential that the phasing of the voltage leads is maintained to provide correct real and reactive power analogues.

12 Protection

The control and protection system is housed at one end of the cubicle with two 3-phase 3-pole circuit breakers (ABB T5S 630), which has auxiliary contacts which receive signals from the control and protection system.

The control system constantly monitors the power electronics and other auxiliary equipment. When a fault is detected it trips the circuit breakers removing the PED from the network. As no customers are fed through the PED, this operation does not generate any customer interruptions. An alarm is sent to the control room.

13 Visualisation

FUN-LV will deliver an advanced DMS PowerOn control system. GE is creating an enhanced LV network representation, similar to Geoview, but allows devices to be controlled and analogues to be visualised. Each PED will be placed on the diagram with measured values being visible at selected levels of magnification.

The trials in Brighton will be managed by the SPN LV Control Engineers.

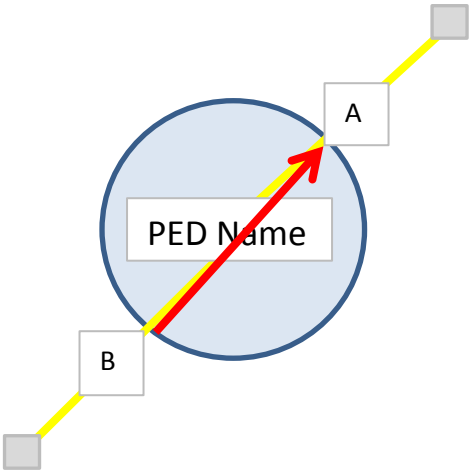


Figure 9 - PowerOn PED Symbol

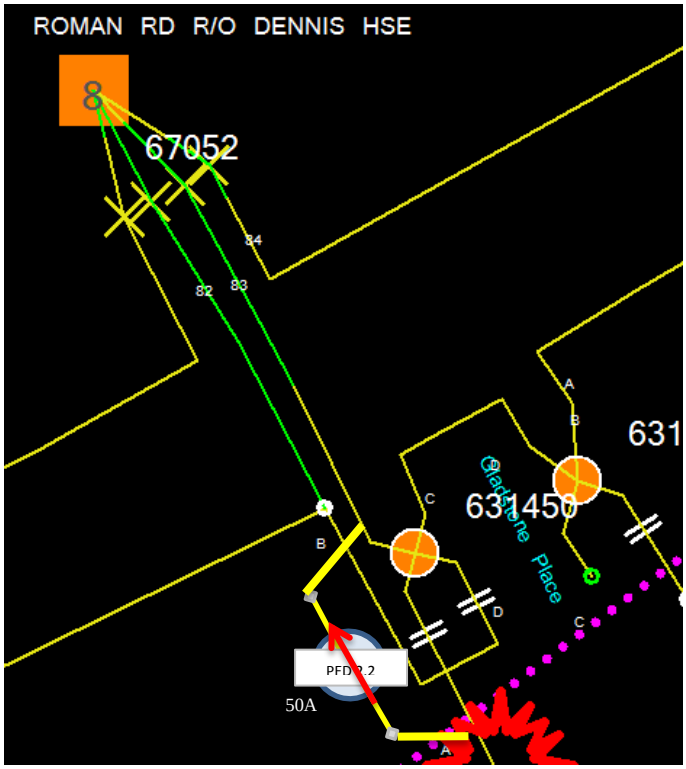


Figure 8 - Example of PED Symbol

14 Communications

As mentioned in section 11 LV Monitoring Systems the LV monitoring unit has an internal modem has a 3G sim card that communicates with the RTU located at Finsbury Market (for London trials) or Ipswich (for Brighton trials).

The PED has its own modem and 3G sim card to receive the demand analogues and send alarms and measured values to the control room and stored in PI.

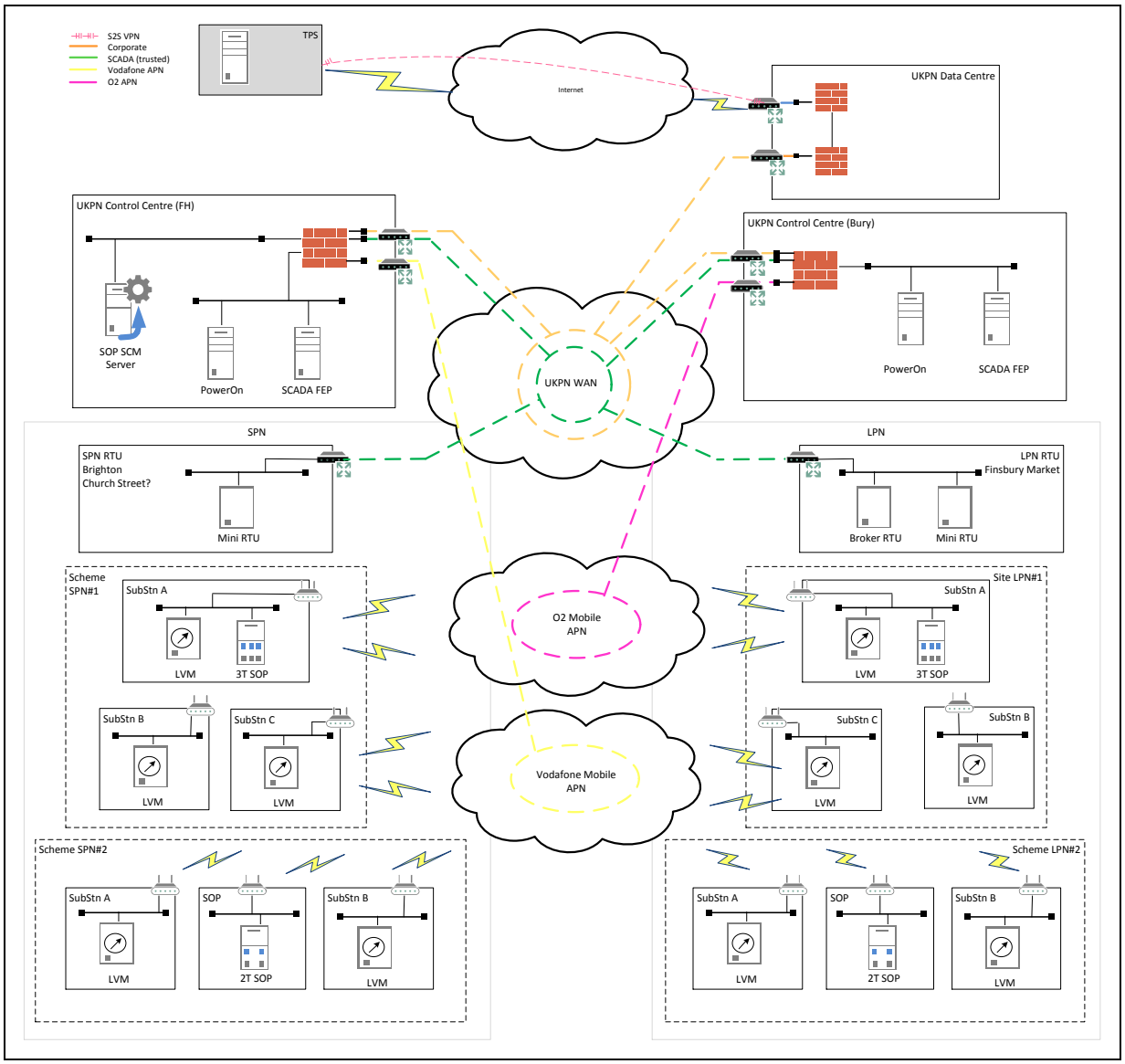


Figure 10 – Communications architecture

As can be seen the Supplier can only provide firmware updates via the UKPN data centre. These updates will be copied to the SCM server where they can be distributed at agreed times. The PED system can only be updated if its control system has been disabled by the Control Engineer.

15 Operations

At any time the control engineer can disable the PED if he believes it is not operating correctly.

The control engineer shall have remote control of the PED and visibility of its transfers. PED has an autonomous algorithm that constantly monitors signals from the Control Engineer. When the system is enabled the algorithm receives transformer demands from both substations and currents from the spine circuits, and determines the necessary action for the function that has been enabled.

During office hours a Control Engineer can contact one of the FUN-LV team members for advice. Outside office hours the PED can be switched off remotely and contact made the following day.

Functions can be enabled and disabled as determined by the Control Engineer are:

System Enable	Switch PED on or off
Real Power Transfer Enable	Real power transfer on or off
PED Reactive Power Support Enable	Reactive power support on or off
Voltage Support Enable	Voltage support on or off
Power Factor Correction Enable	Power factor correction on or off
Phase Imbalance Improvement Enable	Phase imbalance improvement on or off
Harmonic Improvement Enable	Harmonic improvement on or off

Each of these functions can be independently controlled. Initially only one function will be enabled at any one time. For example, if real power transfer is enabled, then the measured demands are compared to the transformer rating and an amount of capacity sharing takes place. If both transformers are within their ratings then the PED remains in an “active standby” mode and continues to monitor transformer demand.

As experience is increased the algorithm controlling the PED will be enhanced to autonomously select the functions to maximise the benefits.

If the LV network needs to be reconfigured and one of the monitored substations will be no longer electrically connected to the PED, then before any linking operations are carried out, the PED shall be disabled using the System Enable control. Once the reconfigured network arrangement is complete, the Port Enable control should switch off the Port that will be no longer involved in capacity sharing. Once the PED is switched on again using the System Enable control the PED will operate as a two terminal PED with all functions available.

16 Training

Directors and Line managers are responsible for ensuring that suitable and sufficient training is given to all staff involved in the project full records of training keep on the Learning Management System (LMS).

Control Engineers will be familiarised with the monitoring and remote control of the PED.

Field staff will be familiarised with the local operations.

17 Network Faults

The PED will sense short current bursts (a few cycles in duration) indicative of an incipient fault. Incipient faults are difficult to identify as they do not cause LV fuses to operate. It is only when these faults currents are sustained for longer periods that they result in nuisance transient fault, where no fault is found, or a permanent fault requiring a repair. The PED will attempt to ride-through these short current bursts, but it will protect itself should the currents cause the power electronics to heat up. The PED will automatically restart up to a maximum number of restarts after which it will lock-out. Operational staff will need to reset the device after an investigation using power quality devices (e.g. Ranger PM 7000) to determine the likely location of the incipient fault.

The PED can only join circuits that are energised from distribution substations. Customers connected to an islanded network cannot be supplied through the PED, because the PED does not deliver fault current. Low fault level would prevent customers' protective equipment from operating for a customer fault.

If a single phase to earth fault should occur, the PED will sense the fault, stop conducting current within 10ms and open the affected port circuit breaker. The LV fuse will operate in accordance with its protection characteristic.

For a phase to phase fault the PED local VTs will sense two phases are similar, stop conducting current within 10ms and open the affected port circuit breaker.

For a three phase fault the PED will sense the fault, stop conducting current within 10ms and open the affected port circuit breaker. The LV fuse will operate in accordance with its protection characteristic.

For an open circuit fault the PED local VTs will sense phases are no longer 120° apart, stop conducting current within 10ms and open the affected port circuit breaker.

For a neutral fault the PED will continue to control the voltages.

On the London interconnected network where, following a HV fault, the existing LV groups of substations support one another, the PED crossing a boundary will continue to support the groups.

On radial networks, following a HV fault, the customers connected to the affected substation will be off supply because the PED cannot supply an islanded network.

If the LV network is reconfigured, e.g. by changing open points in link boxes, then the functions delivered by the PED need to be considered. If substation B is no longer directly connected to the PED via a spine circuit, it can no longer deliver capacity sharing. Only functions that rely on local measurements can be enabled.

Labels will be placed in link boxes indicating that that link box is part of the FUN-LV demonstration and the Control Engineer should be contacted before any linking takes place.

If a substation has a mobile generator supplying customers then as the transformer demand cannot be determined, only functions that rely on local measurements can be enabled for that port.

18 Software Upgrade

A procedure to upgrade the software on the PED PLC including the algorithm has been developed preventing the need to carry out a site visit. The PED must be disabled by Control and a programme update flag set allowing a script to run from the Software Configuration Manager Server

19 Points of Isolation

The control engineer sends a “System disabled” to the PED. The PED control system reduces transfers and sets the PED to standby mode and opens the remote control circuit breakers within the PED. The Control Engineer will be able to confirm the CB status is open. Field staff can now confirm the CB status by opening the PED control panel door. Fuselinks can be removed to establish the point of isolation as per the Distribution Safety Rules.

20 Asset Registration

All assets connected to distribution networks must be registered in the Asset Management System (previously Ellipse) in accordance with EOP 12-0215 ‘Asset Registration - Recording New or Amended Asset Information in Ellipse’. A template will be prepared to register each installation.

21 PowerOn and Netmap

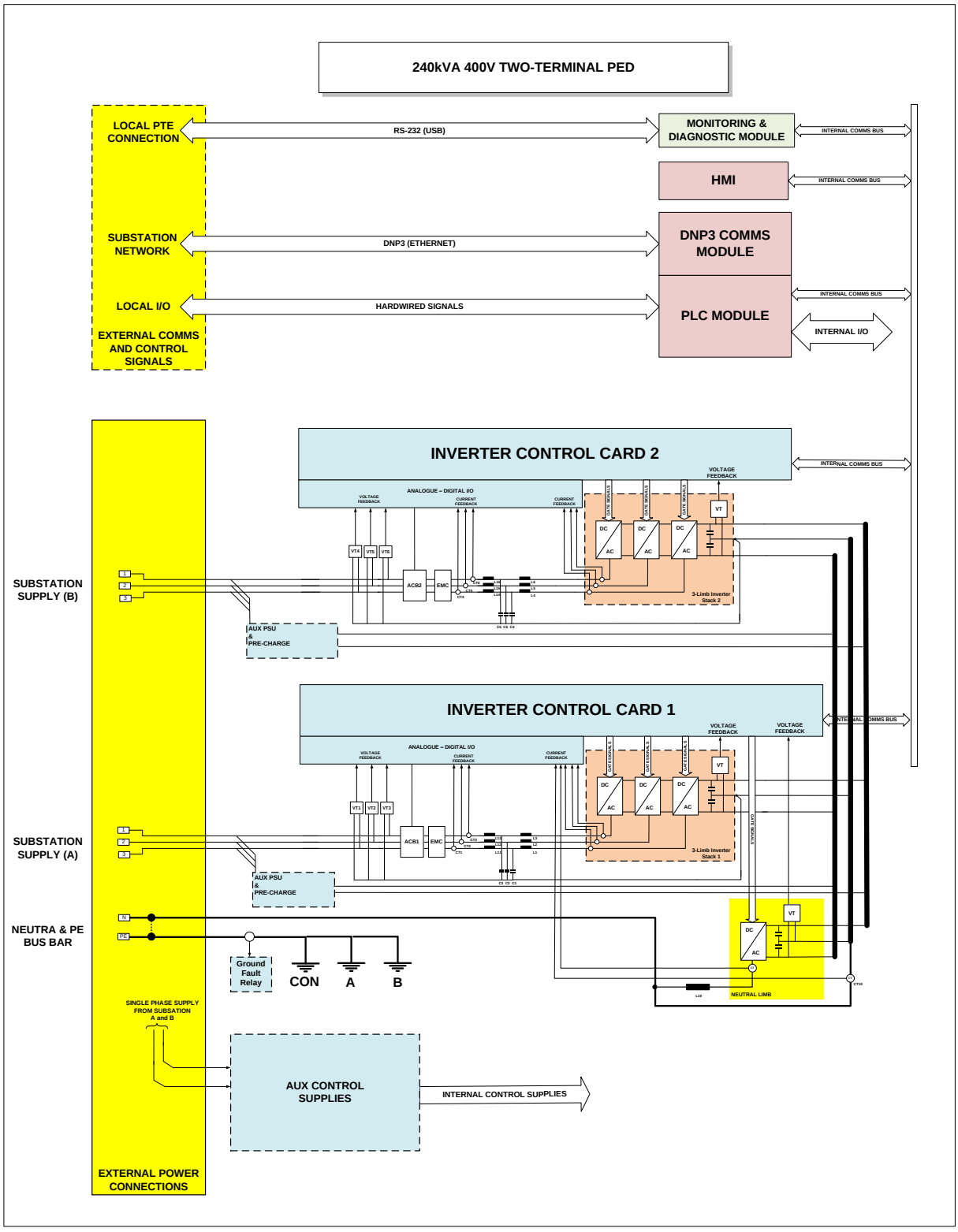
GE have produced an Advanced DMS system which has a dynamic LV network diagram with functionality similar to the HV network diagram, showing energised states, current flows and voltage analogues.

The Netmap diagram will show the position of the PED and the cable jointing that has been installed.

22 References

DSR	Distribution Safety Rules
EDS 09-0040	Dual-terminal Power Electronics Device
EOP 12-0215	Asset Registration - Recording New or Amended Asset Information in Ellipse
EOS 01-0053	Installation and Operation of Monitoring Equipment on LV Distribution Equipment
FUNLV_SP_WS1_Site selection 2.1 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.2 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.3 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.4 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.1 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.2 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.3 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.4 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.1i (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.2i (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.3i (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 2.4i (LPN)_V1.00	

Appendix A General Arrangement



Appendix B Substation Labels

Label for substation doors

This substation contains

LV monitoring equipment which is part of the

FUN-LV project.

Contact Control before entry.

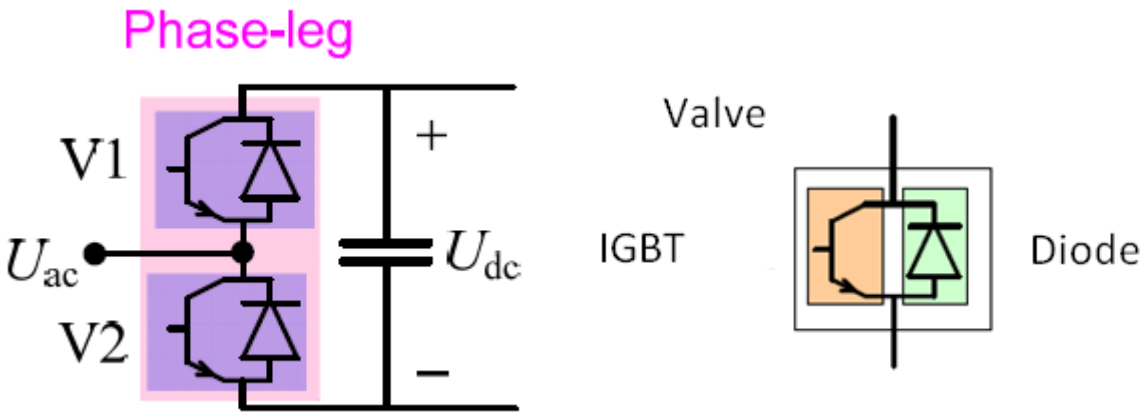
Label for link boxes

This link box is connected to network which is part of the FUN-LV project.

Contact Control before linking.

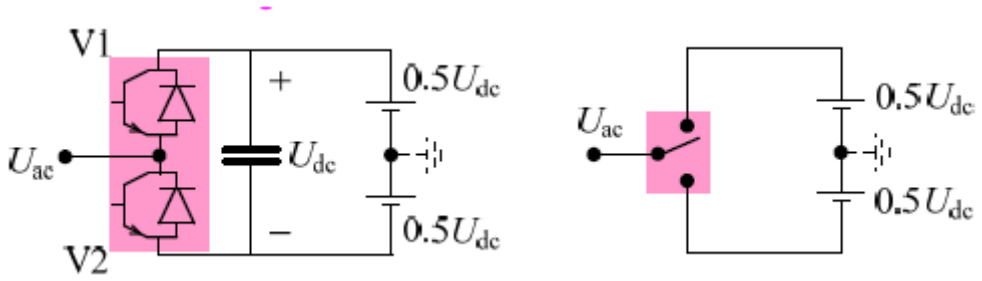
Appendix C Basic Power Electronics Switching

The PED consists of three voltage sourced converters. Each port has three phase legs, each phase leg consisting of two series connected 'valves'.

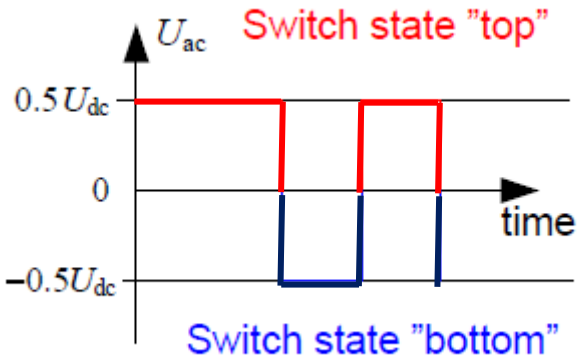


These valves, V1 and V2, consist of an Insulated Gate Bipolar Transistor (IGBT) and an anti-parallel diode. Each IGBT can only conduct in one direction. The inclusion of the anti-parallel diode deals with transient voltages that occur when the IGBT is turned off and enable current flow in the reverse direction. This diode is termed the 'freewheeling' diode.

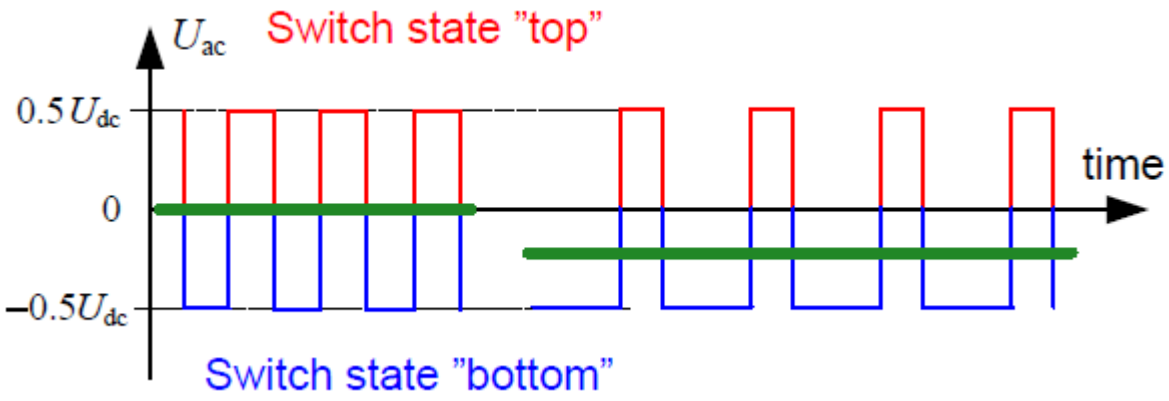
If the phase leg is considered as a mechanical switch as opposed to two IGBT containing valves, then the following can be realised;



It can be seen from the above representation that the current can either be made to flow and create either a +0.5dc voltage or -0.5dc voltage as demonstrated below.

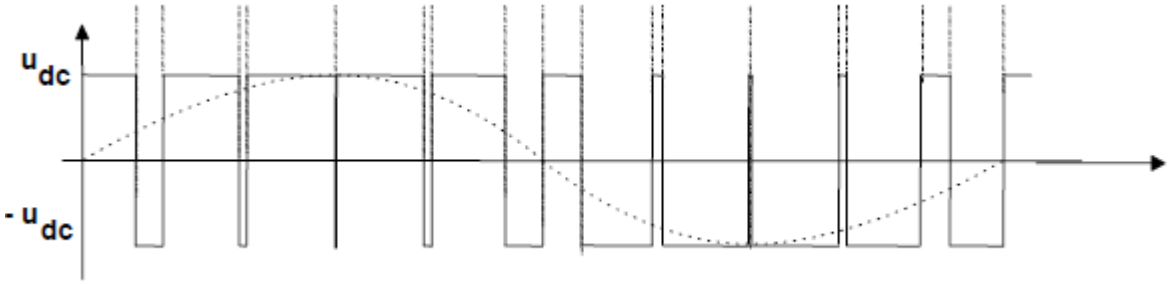


By operating the mechanical switch in the top or bottom instances, the above waveform with time can be realised. This 'digital' voltage control signal operates at 5kHz. The wave shape is achieved by changing the duration each of the switches operates for, using Pulse Width Modulation (PWM) control.



By controlling the width of the pulses, the average output DC voltage is varied, this is demonstrated in the change in level of the green trace.

Through a higher resolution of PWM, an AC waveform can be built up from the PWM controlled DC.



Because the firing of the IGBT's is entirely variable with time, the precise firing angle can be altered.

Depending how the waveform is generated and its difference in phase angle will determine which function is delivered. For example, having the waveform in advance of the network voltage reference results in power export.

Appendix D Asset Registration

Asset Registration will be carried out in accordance with EOP 12-0215.

The following template needs to be completed.

Field	Description
Asset number	
Location	
Maker	Turbo Power Systems (TPS)
Type	Dual-terminal power electronics device
Serial Number	
Operating voltage	400V
Current rating	370A
Year of manufacture	2015
Port A circuit name	
Port B circuit name	

Appendix E Example of Operational Instruction Card

Read Before Any Operational Activity

This substation has a power electronics device (PED) connected to one of its feeders. **Contact LV Control informing them of "Staff on site".**

You can work in this substation without having to switch off this device.

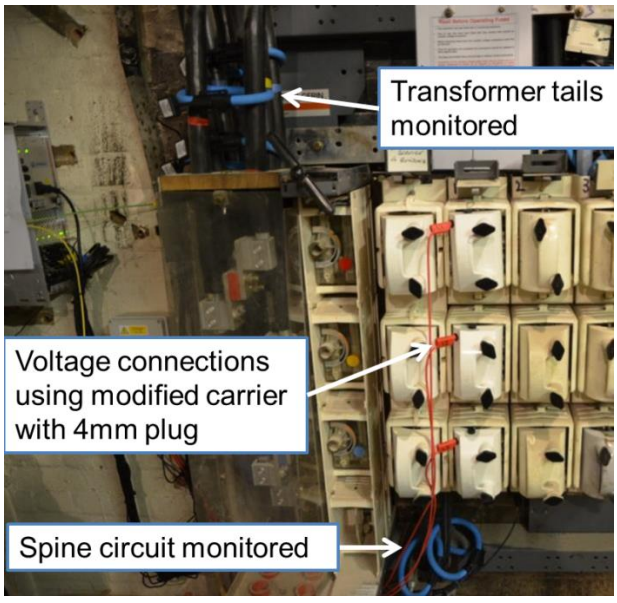
The PED requires the transformer demand which is measured using the LV monitoring equipment. See EOS 01-0053.

If you need to work on the circuit with the LV monitoring equipment contact LV Control who will switch off the PED. Once the PED is disabled, conventional fusing and linking can take place.

In the event of a LV fault affecting the sharing circuit, the PED will shutdown automatically. Once the fault has been repaired the PED can be returned to service.

Engineering Operating Standard 09-0043 has being written explaining how to operate this device.

If you need further information please contact Control in the first instance who will contact one of the FUN-LV team.



LV distribution board connections

Dual terminal PED

Document Number: EOS 09-0042

Version: 1.0

Date: 13/04/2015

ENGINEERING OPERATING STANDARD

EOS 09-0042

FUN-LV MULTI-TERMINAL POWER ELECTRONICS DEVICES

Network(s): LPN, SPN

Summary: This document provides guidance and information in the operation of multi-terminal power electronics devices (PED) in London and Brighton installed for the Flexible Urban Networks-LV (FUN-LV) project. It provides the procedures necessary to avoid danger and allow safe working.

Owner:	Peter Lang	**Date:**	13/04/2015
Approved By:	Barry Hatton	**Approved Date:**	28/04/2015

This document forms part of the Company's Integrated Business System and its requirements are mandatory throughout UK Power Networks. Departure from these requirements may only be taken with the written approval of the Director of Asset Management. If you have any queries about this document please contact the author or owner of the current issue.

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Revision Record

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Date	13/04/2015	**Author**	Peter Lang
New document to cover the approval of the Multi-Terminal Power Electronics Device to be connected to LV networks.			
Version		**Review Date**	
Date		**Author**	

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1 Introduction

The overarching aim of the Flexible Urban Networks - LV (FUN-LV) project is to explore the use of power electronics to enable deferral of reinforcement and facilitate the connection of low carbon technologies and distributed generation in urban areas, by meshing existing radial networks, and by removing boundaries within existing meshed networks. The project will do this by trialling three different types of power electronics device, that is, Methods 1, 2 and 3 across 36 trial sites, 24 in London and 12 in Brighton.

The multi-terminal power electronics device (PED), as specified in EDS 09-0039, is the project's Method 3. Four units will be installed in the interconnected LV networks of London, four units in the radial London LV network and four units in the radial Brighton LV network. Each PED is installed in a distribution substation and shares the capacity between the substation in which it is located and two other substations. The transformer demand is monitored at each of the three substations and is sent to the PED, which determines whether capacity sharing is required.

LV monitoring systems have been installed at each substation in the trial to determine the demand of the transformer and guard the current flow of the "spine" circuit.

2 Scope

This standard has been published because UK Power Networks is installing novel LV power electronics devices into distribution substations in London and Brighton as Soft Open Points, which allow capacity sharing without increasing the fault level. These devices are novel and as such are not covered by any existing manuals or guidance documents. Operational staff and Network Control need to know what to do to ensure safety is maintained.

The expectation is that if a PED needs to be maintained or replaced then Turbo Power Systems (the Supplier) will carry out the actual work. UK Power Networks' operational staff will isolate and make the equipment safe before it is maintained.

This document does not cover the installation or commissioning of the PED.

This document is intended for internal use only.

3 Glossary and Abbreviations

Term	Definition
CB	Circuit Breaker
DMS	Distribution Management System
Ellipse	UK Power Networks' Asset Register soon to be integrated into SAP as per Business Transformation.
FUN-LV	Flexible Urban Networks - LV
HMI	Human Machine Interface
IGBT	Insulated Gate Bipolar Transistor
LCNF	Low Carbon Networks Fund
LPN	London Power Networks
NetMap	UK Power Networks' graphical information system (GIS).
PED	Power Electronics Device
PLC	Programmable Logic Controller
PowerOn fusion	UK Power Networks' DMS.
RTU	Remote Telemetry Unit
S/S A	This substation is the one where the PED is normally installed.
S/S B and S/S C	These substations are the donor substations connected via the Spine circuits.
SCM Server	Software Configuration Management Server
SOP	Soft Open Point
SPN	South Eastern Power Networks
UK Power Networks	UK Power Networks (Operations) Ltd consists of three electricity distribution networks: • Eastern Power Networks plc (EPN). • London Power Network plc (LPN). • South Eastern Power Networks plc (SPN).
VT	Voltage Transformer or Voltage Transducer

4 Definitions

LV Only substation	This is a LPN substation containing a LV distribution board only with space available for a transformer and RMU.
Soft Open Point	A point on the network where two networks are joined together through power electronics to share capacity without increasing the prospective short circuit current.
Spine circuit	This is the LV feeder that joins two distribution substations together to enable capacity sharing. Based on LPN interconnected LV network design terminology.
Supplier	Turbo Power Systems (TPS)

5 Basic Description

The multi-terminal PED consists of three 400kW inverters joined to a common DC busbar and a neutral inverter. The basic operation of power electronics is described in Appendix C. The PED controller receives measured demand values from remote substations and local analogues. An algorithm developed by Imperial College takes these values and determines which functions have been enabled.

The expected functions are:

1. Real power transfer;
2. Reactive power support;
3. Voltage support;
4. Power factor correction and improvement;
5. Phase imbalance improvement;
6. Loss reduction;
7. Harmonic content improvement.

Current can be taken from and exported to any combination of the three inverters as long as the sum of the currents is zero after losses are taken into account.

The neutral inverter is required to perform the advanced functions 4 to 7. Early versions of the algorithm are restricted to functions 1 to 3.

To prevent common mode currents each inverter cubicle has a line filter (150 uH - 240 uF (star) - 30 uH) that is liquid cooled to maintain its 577A rating.

The conversion from AC to DC across each inverter is calculated to be greater than 96% efficient. 4% Losses of 400kW is 16kW in the form of heat that needs to be dissipated. A closed water cooling system with a heat exchanger is connected to the PED. The power supply to the cooling system is derived from the PED. Further information in section 12.

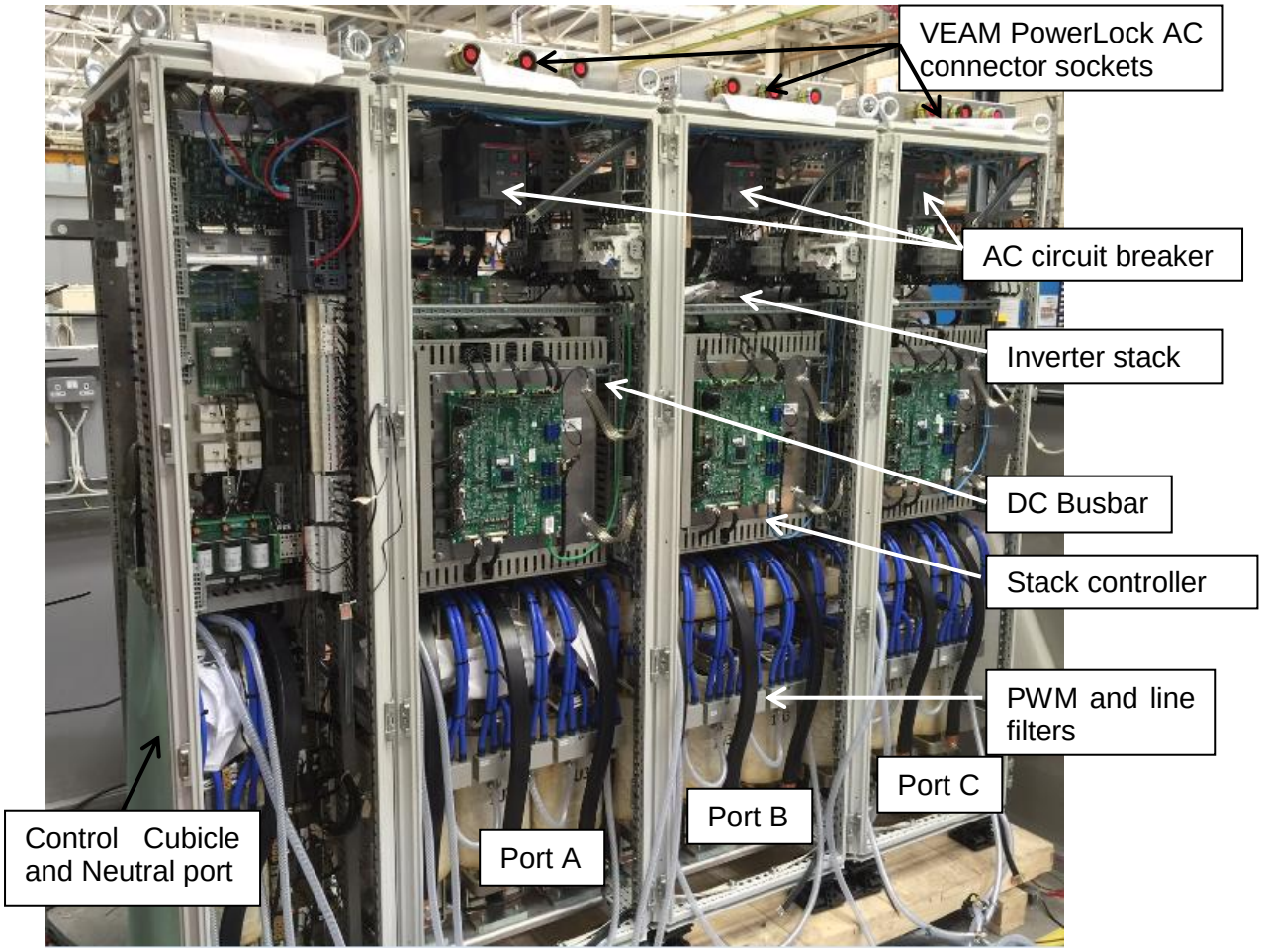

Figure 1 - Three terminal PED (doors removed)

6 Site Locations

The aim of the FUN-LV project is to carry out the assessment of benefits delivered by power electronics connected to a LV distribution network. LV monitoring devices will be installed in the substations listed below to provide the transformer demand and current of the spine circuit to drive the PED algorithm. This data will provide the necessary evidence to complete the business case and demonstrate that power electronics is able to realise benefits when connected to a LV network.

Table 1 - SPN radial sites

ID	S/S A and PED location	S/S B	S/S C
S3.1	523637 - Prudential North Street (T1)	522941 - Vokins (T1)	523230 - New Road (T1)
S3.2	522916 - Robert Street (T1)	521244 - Marlborough Place (T1)	523193 - Gloucester Street (T1)
S3.3	523036 - Church Street (N2)	523259 - King Street (T1)	523615 - Bond Street (T1)
S3.4	523025 - Kings Road (T1+T2)	523751 - West Street 77 (T1)	523173 - Black Lion Street (T1)

Table 2 - LPN radial sites

ID	S/S A	S/S B	S/S C	S/S PED
L3.1	07141 - Felsham Rd 124	07863 - Bemish Rd R/O 28	07132 - Biggs Row (G)	07141 - Felsham Rd 124
L3.2	30792 - Shirland Rd Charfield Ct	30759 - Shirland Rd 41	30157 - Amberley Rd Local	30123 - Ellwood Ct Shirland Rd (LV Only)
L3.3	06194 - Bushey Rd East (G)	06602 - The Chase (G)	06627 - Whatley Ave (G)	08070 - Bushey Rd West (LV Only)
L3.4	90415 - Fiveways Guinness Trust (G)	90272 - Minet Rd Loughborough School	90325 - Rupert Gardens (N/A)	90260 - Loughborough Rd Newark House (LV Only)

Table 3 - LPN interconnected sites

ID	S/S A	S/S B	S/S C	S/S PED
L3.1i	24410 - Shaftesbury Ave 125	24409 - Stacey St	31023 - Charing X Rd 82	24410 - Shaftesbury Ave 125
L3.2i	34179 - Bulstrode St Clifton Ford Hotel	34146 - 9 Thayer St	34174 - Welbeck St 33-35 And 34172 Westmoreland St National Heart Hosp.	34179 - Bulstrode St Clifton Ford Hotel
L3.3i	30107 - Nutford Pl Holiday Inn (G)	34300 - Forset St Coopers Stores	34317 - Edgware Rd 112-130	30107 - Nutford Pl Holiday Inn (G)
L3.4i	34725 - Pall Mall 83 RAC	31511 - Pall Mall 45-47 or 31511 - Pall Mall 100 or 36223 - Pall Mall 36	36643 - Pall Mall 80-82 and 31511 - Pall Mall 45-47	34725 - Pall Mall 83 RAC

A site approval document has been prepared for each trial, detailing the expected benefits.

7 Access

On the external doors of each of these substations a label will be placed informing staff that this substation is part of the FUN-LV trial. At S/S A substations a notice will warn staff that a PED has been installed. **Staff can safely enter these substations and carry out their normal duties without switching off the PED.** Labels will also be placed in link boxes indicating that that link box is part of the FUN-LV demonstration and the Control Engineer should be contacted before any linking takes place. Copies of these labels are contained in Appendix B.

8 Method of Connection

Each PED is connected to the LV distribution board in S/S A or a LV only substation using 240mm^2 flexible copper cables. Each end of the flexible cable is fitted with VEAM PowerLock connection plugs similar to those used to connect mobile generators. Modified fuse carriers with a socket connection will replace the existing fuse carriers connected to the Spine Circuits. The modified fuse carriers to LV busbar shall have the same size fuselink as the existing fuse carrier, whereas the modified fuse carriers to substations B and C shall have dummy fuselinks fitted. The ten cables will be cleated to the floor or ceiling between the PED and the LV distribution board (three phase single core cables per LV way plus one common combined neutral earth cable using a mechanical clamp).

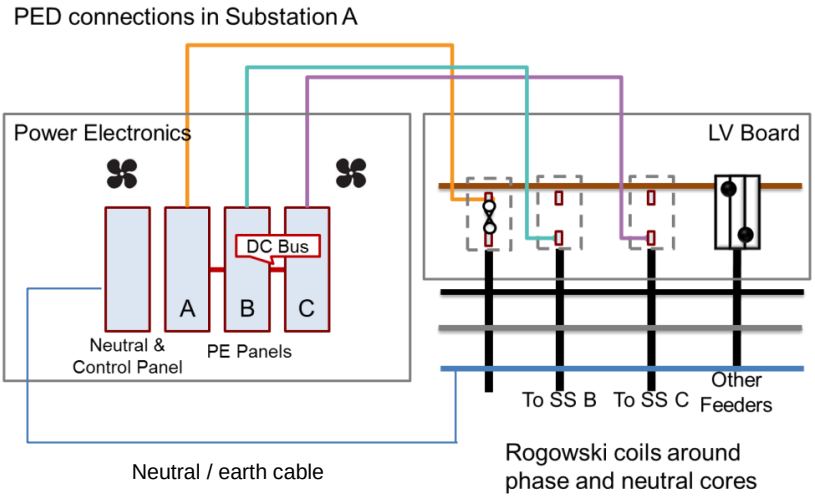

Figure 2 - Single line AC connections

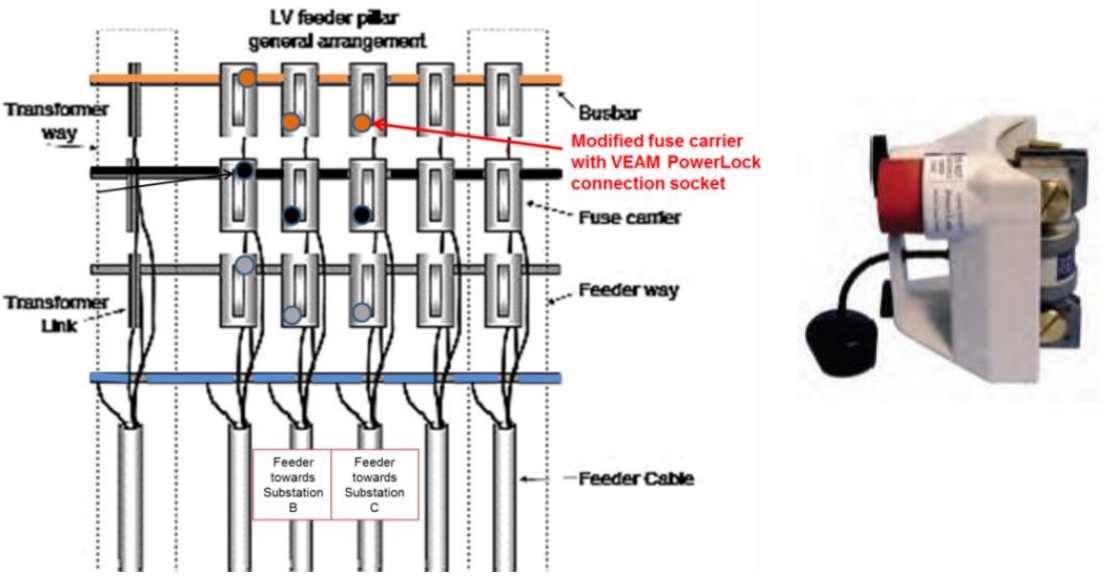

Figure 3 - LV distribution board with modified fuse carriers

In the event that modified fuse carriers do not fit e.g. a legacy Lucy Oxford LV distribution board with ten inch ceramic fuse carriers (Church Street SPN 523036) then short 660A horizontal clamps shall be used. This clamp is also used for the neutral bar connection.

Figure 4 Short 660A horizontal clamp

The nine phase cables will be supported on wooden frames or suspended from the ceiling to remove excessive weight hanging on the PowerLock connection plugs, modified fuse carriers and horizontal clamps. There is only one combined neutral earth connection between the PED and the LV distribution board.

The doors of the free-standing LV distribution board can be removed as this presents no greater risk than an open board. This allows the cables to enter the fuse carrier without excessive bends.

The power supply to the PED is derived via the cables from the LV distribution board. The three phases from each feeder are combined together, such that if the supply at S/S A is interrupted, the PED can continue to operate and share capacity between S/S B and C.

The power supply for the cooling system is derived from the PED three phase auxiliary supply. If the supply at S/S A is interrupted the heat exchanger can continue to operate.

9 Protection

The control and protection system is housed in the left most panel (see Figure 1). Each port cubicle has a three phase three pole circuit breaker (ABB T5S 630), which has auxiliary contacts which receive trip signals from the control and protection system.

The control system constantly monitors the power electronics and other auxiliary equipment. When a fault is detected it trips the circuit breakers removing the PED from the network. As no customers are fed through the PED, this operation does not generate any customer interruptions. An alarm is sent to the control room.

The DC busbars (positive, neutral and negative) and other internal power electronics components are supported on insulated plastic blocks and isolated from earth. The panels are connected via a bolted connection to the LV distribution board Neutral Earth busbar. The residual current is calculated and used to protect the unearthed power electronics components.

In an emergency operational staff have an emergency stop button installed on the PED door that trips the circuit breakers.

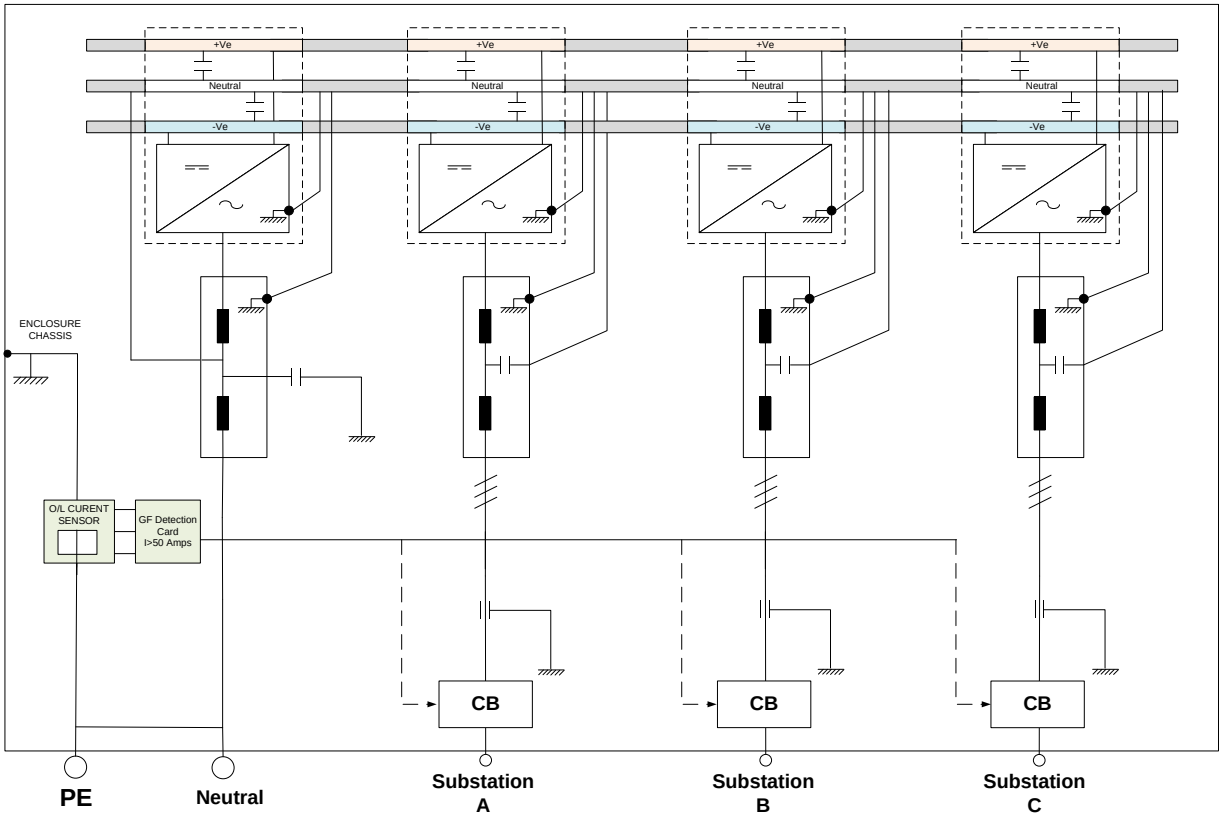

Figure 5 – Filters and Inverters single line diagram

10 LV Monitoring Systems

An Ormazabal or GMC-I Prosys LV monitoring system is being used to monitor the real and reactive power demand on each transformer as well as flowing through the spine circuits. This system is re-using legacy equipment from a previous Low Carbon Networks Fund (LCNF) project and new single card monitoring units, each with a GPRS communications link. EOS 01-0053 'Installation and Operation of Monitoring Equipment on LV Distribution Equipment' describes the methods of installation, operation and decommissioning.

In the case of open boards where the LV transformer tails are safely accessible to fit the Rogowski current sensor, then one monitor will monitor the transformer demand and a second will monitor the spine circuit.

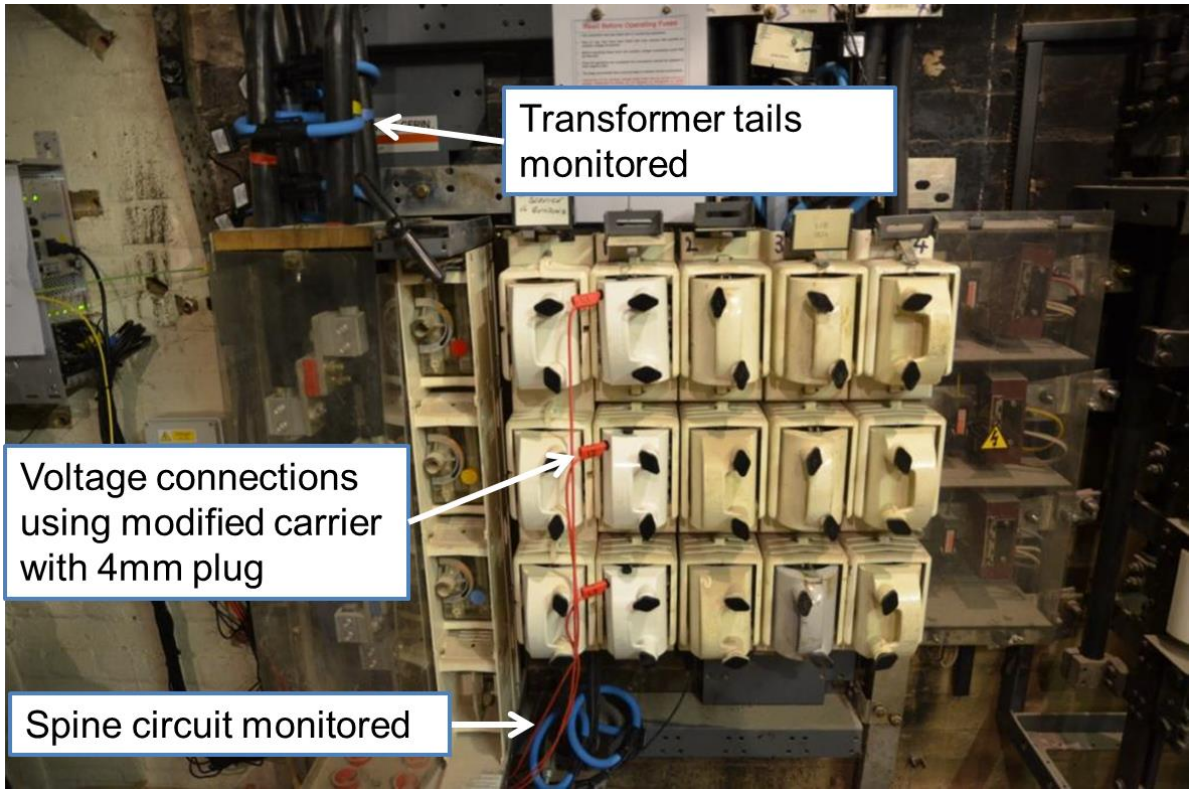

Figure 6 - LV monitoring for Substation B and C

In the case of confined modern pillar where access to the transformer tails is difficult, then all the outgoing ways will need to be monitored. Legacy Ormazabal four card monitoring units will be reused in this situation.

Under normal operations it should not be necessary to remove the Rogowski coils. However to measure real and reactive power a voltage measurement is required. Modified fuse carriers with 4mm plug can replace any set of standard fuse carriers. In the event that a modified fuse carrier needs to be removed (following the procedure in EOS 01-0053), the PED will be disabled beforehand by the Control Engineer. It is essential that the phasing of the voltage leads is maintained to provide correct real and reactive power analogues.

11 Visualisation

FUN-LV will deliver an advanced DMS PowerOn control system. GE will create an enhanced LV network representation, similar to Geoview, but allows devices to be controlled and analogues to be visualised. Each PED will be placed on the diagram with a Combined Control and Analogue Box (Figure 11) displaying measured values.

The trials in Brighton will be managed by SPN LV Control Engineers.

12 Cooling System

The cooling system of the PED consists of a water/glycol coolant that is pumped through the power electronics and filters to a heat exchanger that vents warm air out of the substation, to keep the PED components cool and maintain its rating. The cooling system is monitored and will send a temperature reading to the control room which will be stored in PI. This will allow the performance of the PED to be analysed.

The coolant tank is integral with the fan cooling unit.

If the heat exchanger fails the PED can continue to operate at a lower capacity transfer preventing the components from overheating. If however the upper temperature threshold is reached the PED will shut itself down and await the fault resolution.

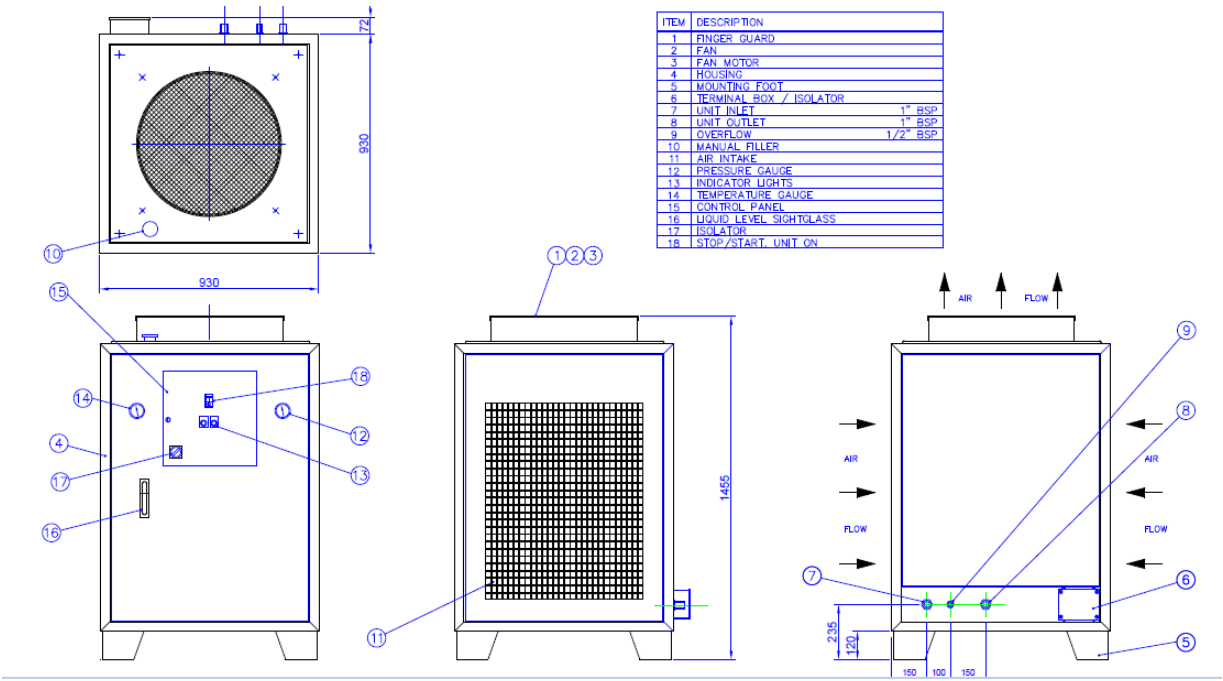

Figure 7 - Cooling system

13 Communications

As mentioned in Section 10 LV Monitoring Systems the LV monitoring unit has an internal modem with a 3G sim card that communicates with the RTU located at Finsbury Market (for London trials) or Ipswich (for Brighton trials).

The PED has its own modem and 3G sim card to receive the demand analogues and send alarms and measured values to the control room and stored in PI.

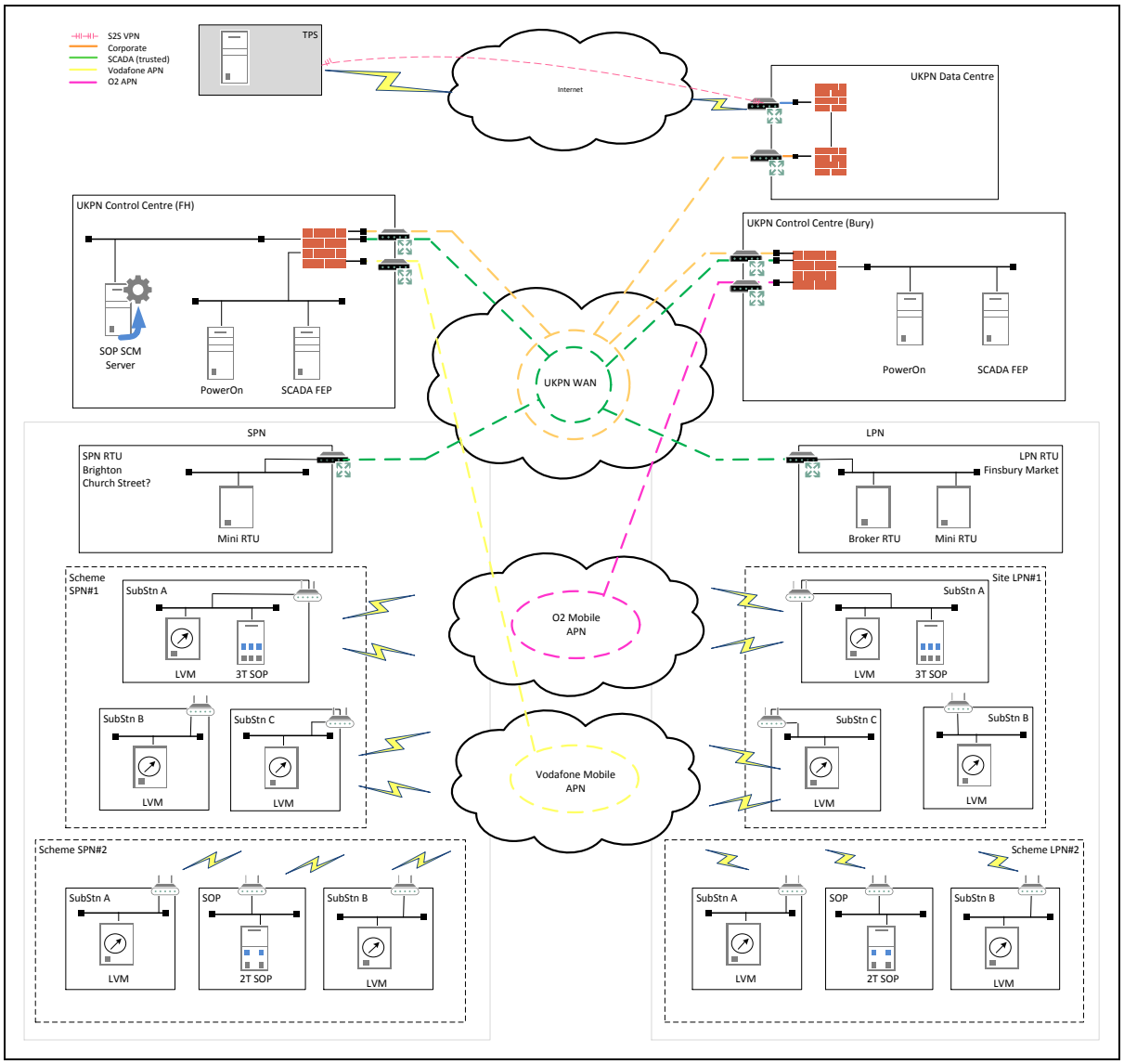

Figure 8 – Communications architecture

As can be seen the Supplier can only provide firmware updates via the UKPN data centre. These updates will be copied to the SCM server where they can be distributed at agreed times. The PED system can only be updated if its control system has been disabled by the control engineer.

Should the communications fail between the LV monitoring units and the RTU the algorithm will identify that which port has “loss of comms” and only functions that rely on local measurements will be delivered by that port. If communications fail between the PED and the RTU then all ports will only deliver functions that rely on local measurements.

14 Operations

At any time the control engineer can disable the PED if he believes it is not operating correctly using the System Enable control.

The Control Engineer shall have remote control of the PED and visibility of its transfers.

The main controls are:

System Enable	Switch PED on or off
Port A Enable	Switch port A on or off
Port B Enable	Switch port B on or off
Port C Enable	Switch port C on or off

During office hours a Control Engineer can contact one of the FUN-LV team members for advice. Outside office hours the PED can be switched off remotely and contact made the following day.

PED has an autonomous algorithm that constantly monitors enable/disable controls from the PowerOn ADMS control system. When the system is enabled the algorithm receives transformer demands from the three substations and currents from the spine circuits (at around one minute intervals) and determines the necessary action for the function that has been enabled.

During the demonstration phase of the project, Network Control has indicated that they only wish to enable/disable the PED. The FUN-LV project team shall have remote access of the local HMI on the PED to allow them to select the functions listed below.

Per Port functions can be enabled and disabled using controls, as required. These are:

Real Power Transfer Enable	Real power transfer on or off
PED Reactive Power Support Enable	Reactive power support on or off
Voltage Support Enable	Voltage support on or off
Power Factor Correction Enable	Power factor correction on or off
Phase Imbalance Improvement Enable	Phase imbalance improvement on or off
Harmonic Improvement Enable	Harmonic improvement on or off
Transformer Equalisation Enable	Transformer equalisation on or off

Each of these functions can be independently controlled. Initially only one function will be enabled at any one time. For example, if real power transfer is enabled, then the measured demands are compared to the transformer rating and a calculated amount of capacity sharing takes place. If all three transformers are within their ratings then the PED remains in an “active standby” mode and continues to monitor and compare transformer demand.

As experience is increased the algorithm controlling the PED will be enhanced to autonomously select the functions to maximise the benefits.

If the LV network needs to be reconfigured and one of the monitored substations will be no longer electrically connected to the PED, then before any linking operations are carried out, the PED shall be disabled using the System Enable control. Once the reconfigured network arrangement is complete, the Port Enable control should switch off the Port that will be no longer involved in capacity sharing. Once the PED is switched on again using the System Enable control the PED will operate as a two terminal PED with all functions available.

Before the LV network is returned to normal the PED should be switched off, the Port enabled and the PED switched on again and return to normal multi-terminal operation.

15 Network Faults

The PED will sense short current bursts (a few cycles in duration) indicative of an incipient fault. Incipient faults are difficult to identify as they do not cause LV fuses to operate. It is only when these faults currents are sustained for longer periods that they result in nuisance transient fault, where no fault is found, or a permanent fault requiring a repair. The PED will attempt to ride-through these short current bursts, but it will protect itself should the currents cause the power electronics to heat up. The PED will automatically restart up to a maximum number of restarts after which it will lock-out. Operational staff will need to reset the device after an investigation using power quality devices (e.g. Ranger PM 7000) to determine the likely location of the incipient fault.

The PED can only join circuits that are energised from distribution substations. Customers connected to an islanded network cannot be supplied through the PED, because the PED does not deliver fault current. Low fault level would prevent customers' protective equipment from operating for a customer fault.

If a single phase to earth fault should occur, the PED will sense the fault, stop conducting current within 10ms and open the affected port circuit breaker. The LV fuse will operate in accordance with its protection characteristic.

For a phase to phase fault the PED local VTs will sense two phases are similar, stop conducting current within 10ms and open the affected port circuit breaker.

For a three phase fault the PED will sense the fault, stop conducting current within 10ms and open the affected port circuit breaker. The LV fuse will operate in accordance with its protection characteristic.

For an open circuit fault the PED local VTs will sense phases are no longer 120° apart, stop conducting current within 10ms and open the affected port circuit breaker.

For a neutral fault the PED will continue to control the voltages.

On the London interconnected network where, following a HV fault, the existing LV groups of substations support one another, the PED crossing a boundary will continue to support the groups.

On radial networks, following a HV fault, the customers connected to the affected substation will be off supply because the PED cannot supply an islanded network.

Following the clearance of the fault, the two unaffected ports can continue to operate delivering all functions.

If the LV network is reconfigured, e.g. by changing open points in link boxes, then the functions delivered by the PED need to be considered. If substation B is no longer directly connected to the PED via a spine circuit, it can no longer deliver capacity sharing. Only functions that rely on local measurements can be enabled for that port.

Labels will be placed in link boxes indicating that that link box is part of the FUN-LV demonstration and the control engineer should be contacted before any linking takes place.

If a substation has a mobile generator supplying customers then as the transformer demand cannot be determined, only functions that rely on local measurements can be enabled for that port.

16 Software upgrade

A procedure to upgrade the software on the PED PLC including the algorithm has been developed preventing the need to carry out a site visit. The PED must be disabled by Control and a programme update flag set allowing a script to run from the Software Configuration Manager Server Refer to Figure 8.

17 PowerOn, Netmap and Geofield

GE have produced an Advanced DMS system which has a dynamic LV network diagram with functionality similar to the HV network diagram, showing energised states, current flows and voltage analogues.

The Netmap diagram will not show any network changes as they all occur within the substation.

18 PowerOn PED symbol

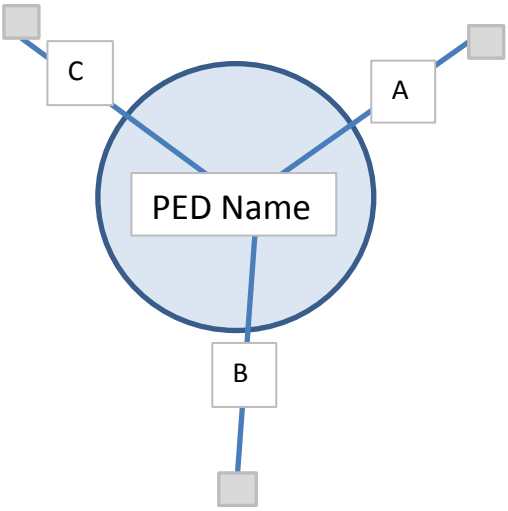

Figure 9 - PowerOn PED Symbol

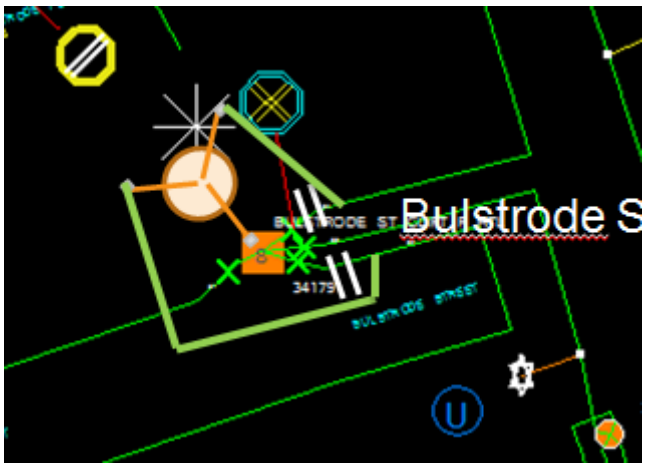

Figure 10 - Example of PED Symbol

Selecting the PED symbol on the diagram a menu appears allowing the control engineer to navigate to a PED details view similar to control and analogue box. This box displays the measured analogue values from the LV monitoring systems and the PED ports. The PED can be disabled by selecting the controls menu.

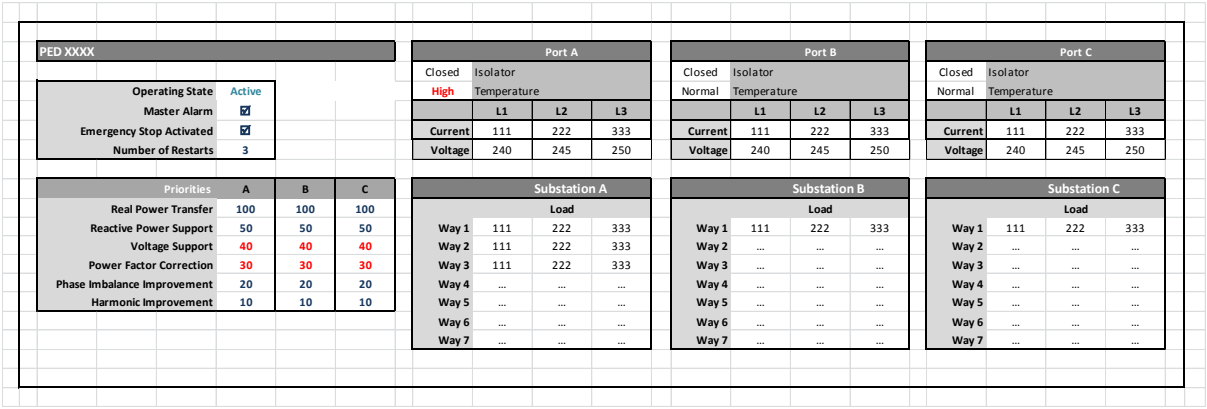

Figure 11 - Combined Control and Analogue Box

19 Training

Directors and Line Managers are responsible for ensuring that suitable and sufficient training is given to all staff involved in the project. Full records of training are kept on the Learning Management System (LMS).

Control Engineers will be familiarised with the monitoring and remote control of the PED.

Operational staff will be familiarised with the local operations.

20 Points of Isolation

When the control engineer sends a “System disabled” control to the PED:

- The PED control system reduces transfers;
- Sets the PED to standby mode; and
- Opens the circuit breakers within the PED.

The Control Engineer will be able to confirm the CB status is open.

21 Asset Registration

All assets connected to distribution networks must be registered in the Asset Management System (previously Ellipse) in accordance with EOP 12-0215 ‘Asset Registration - Recording New or Amended Asset Information in Ellipse’. A template has been prepared to register each PED installation as defined in Appendix D.

22 References

DSR	Distribution Safety Rules
EDS 09-0039	Multi-terminal Power Electronics Device
EOP 12-0215	Asset Registration - Recording New or Amended Asset Information in Ellipse
EOS 01-0053	Installation and Operation of Monitoring Equipment on LV Distribution Equipment
FUNLV_SP_WS1_Site selection 3.1 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.2 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.3 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.4 (SPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.1 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.2 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.3 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.4 (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.1i (LPN)_V1.00	
FUNLV_SP_WS1_Site selection 3.2i (LPN)_V1.00	
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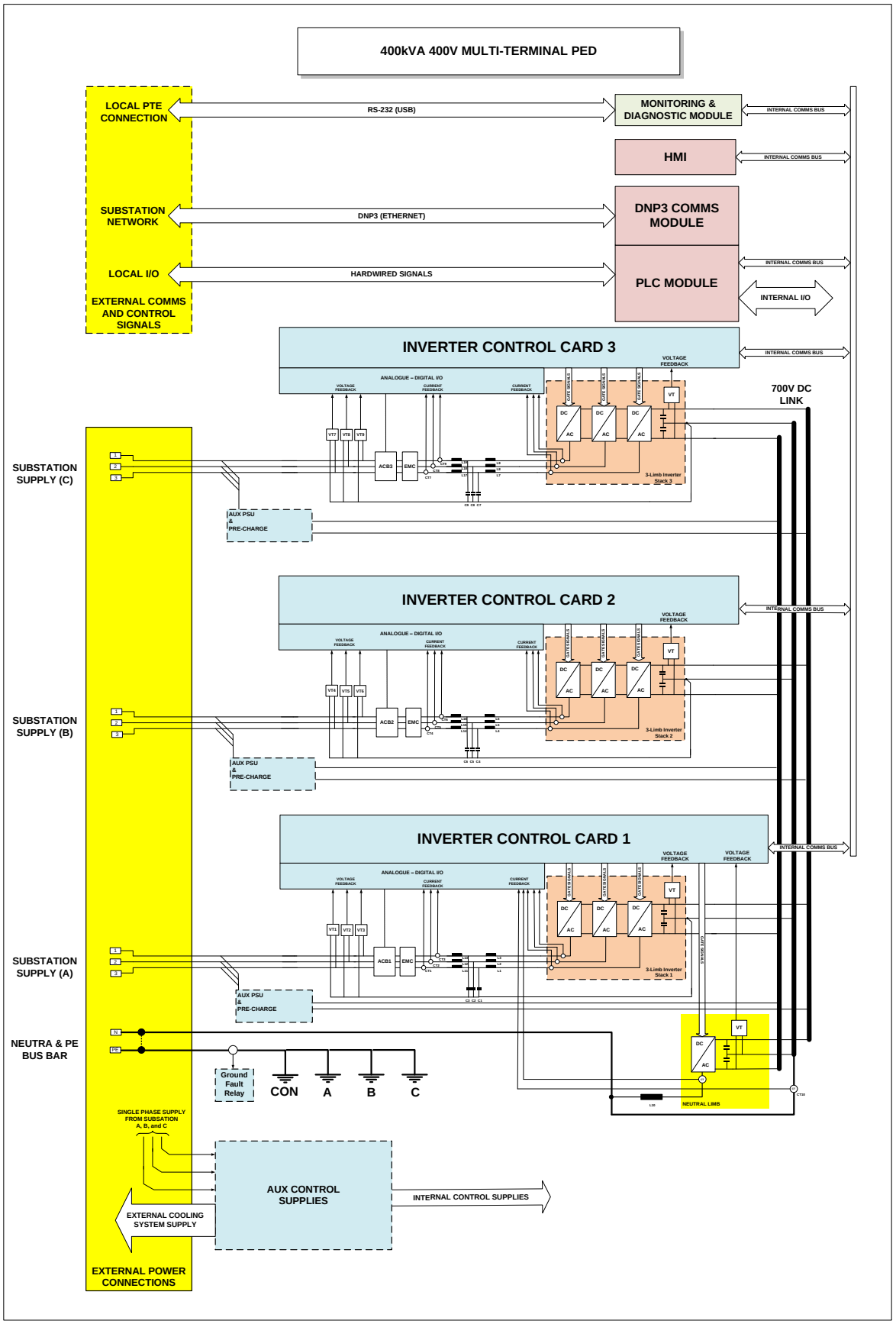
FUNLV_SP_WS1_Site selection 3.4i (LPN)_V1.00	

Appendix A General Arrangement



Appendix B Substation and link box Labels

Label for substations B and C

This substation contains

LV monitoring equipment which is part of the

FUN-LV project.

Contact Control before entry.

Label for substation A

This substation contains a

Power Electronics Device which is part of the

FUN-LV project.

Contact Control before entry.

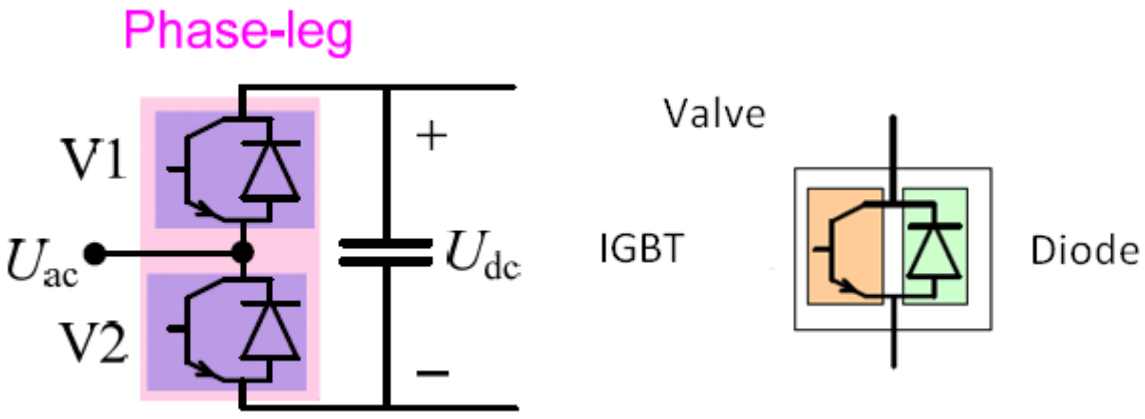
Label for link boxes

This link box is connected to network which is part of the FUN-LV project.

Contact Control before linking.

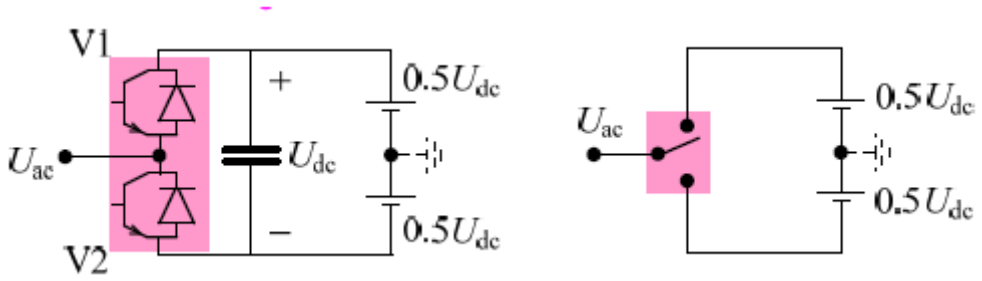
Appendix C Basic Power Electronics Switching

The PED consists of three voltage sourced converters. Each port has three phase legs, each phase leg consisting of two series connected 'valves'.

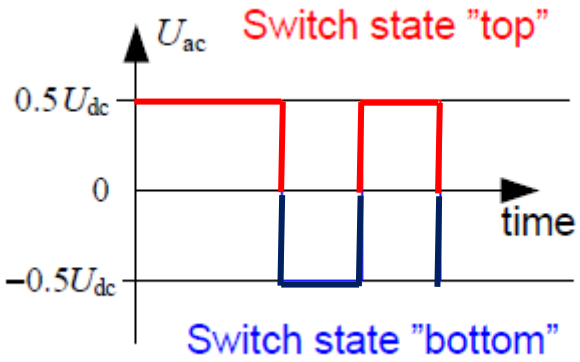


These valves, V1 and V2, consist of an Insulated Gate Bipolar Transistor (IGBT) and an anti-parallel diode. Each IGBT can only conduct in one direction. The inclusion of the anti-parallel diode deals with transient voltages that occur when the IGBT is turned off and enable current flow in the reverse direction. This diode is termed the 'freewheeling' diode.

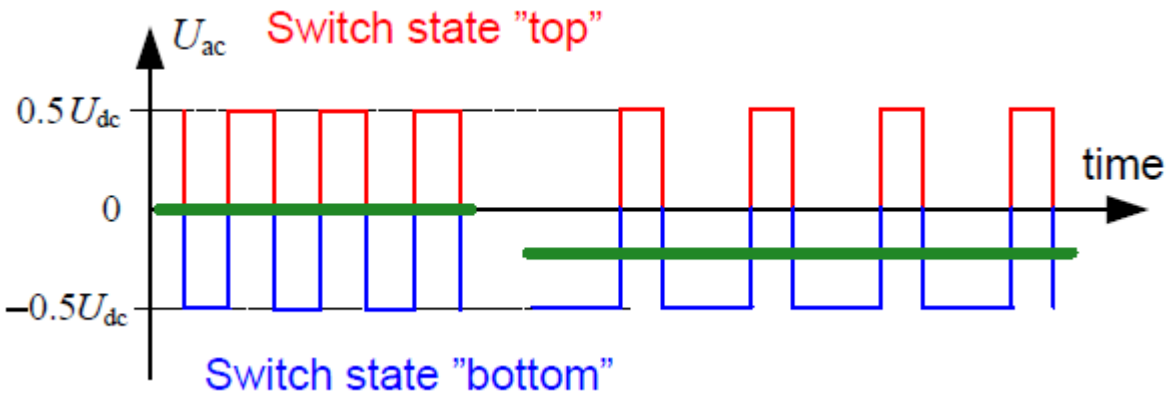
If the phase leg is considered as a mechanical switch as opposed to two IGBT containing valves, then the following can be realised;



It can be seen from the above representation that the current can either be made to flow and create either a +0.5dc voltage or -0.5dc voltage as demonstrated below.

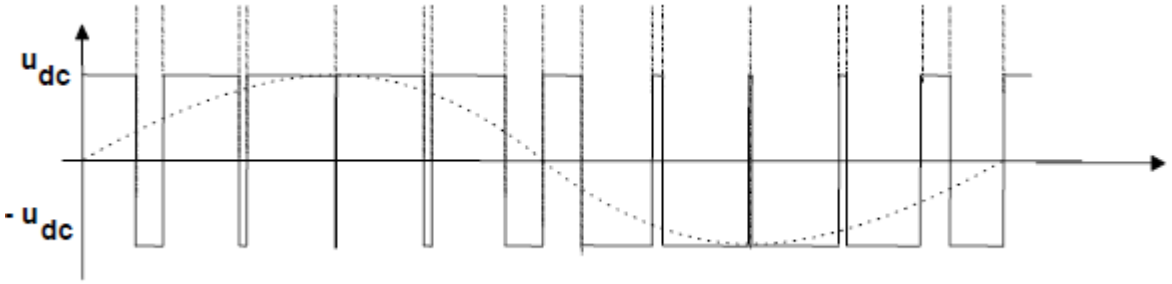


By operating the mechanical switch in the top or bottom instances, the above waveform with time can be realised. This 'digital' voltage control signal operates at 5kHz. The wave shape is achieved by changing the duration each of the switches operates for, using Pulse Width Modulation (PWM) control.



By controlling the width of the pulses, the average output DC voltage is varied, this is demonstrated in the change in level of the green trace.

Through a higher resolution of PWM, an AC waveform can be built up from the PWM controlled DC.



Because the firing of the IGBT's is entirely variable with time, the precise firing angle can be altered.

Depending how the waveform is generated and its difference in phase angle will determine which function is delivered. For example, having the waveform in advance of the network voltage reference results in power export.

Appendix D Asset Registration

Asset Registration will be carried out in accordance with EOP 12-0215.

The following template needs to be completed.

Field	Description
Asset number	
Location	
Maker	Turbo Power Systems (TPS)
Type	Multi-terminal power electronics Device
Serial Number	
Operating voltage	400V
Current rating	550A
Year of manufacture	2015
Port A circuit name	
Port B circuit name	
Port C circuit name	

Appendix E Example of Operational Instruction Card

Read Before Any Operational Activity

This substation has a power electronics device (PED) that shares capacity between substations. **Contact LV Control informing them of "Staff on site".**

You can work in this substation without having to switch off this device.

If you need to work on one of the circuits with modified fuse carriers contact LV Control who will switch off the PED.

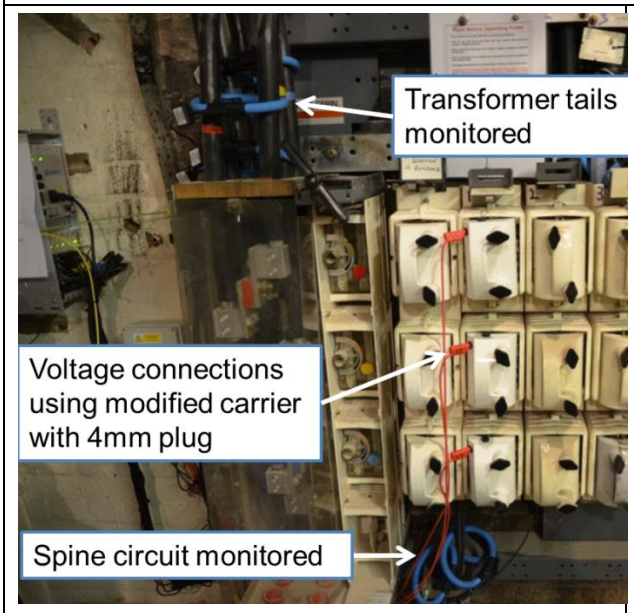
The PED requires the transformer demand which is measured using the LV monitoring equipment. See EOS 01-0053.

If you need to work on the circuit with the LV monitoring equipment contact LV Control who will switch off the PED. Once the PED is disabled, the cables from the PED to the distribution board can be removed allowing conventional fusing and linking to take place.

In the event of a LV fault affecting the sharing circuit, the PED will shutdown automatically. Once the fault has been repaired the PED can be returned to service.

Engineering Operating Standard EOS 09-0042 has being written explaining how to operate this device.

If you need further information please contact Control in the first instance who will contact one of the FUN-LV team.



LV distribution board connections

Multi terminal PED (doors removed)

UNIVERSITY of STRATHCLYDE
POWER NETWORKS DEMONSTRATION CENTRE

Testing of Soft Open Point Power Electronic Device

Document No.: **PNDC/UKPN-001/FR-01**

Classification: **Unrestricted**

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1 EXECUTIVE SUMMARY

The objective of this project is to test UKPN's Soft Open Point (SOP) Power Electronic Device (PED) under different network operational scenarios at the Power Networks Demonstration Centre (PNDC). The test programme is designed to evaluate the SOP's response to typical network events in order to better understand its operation prior to it being deployed on UKPN's Low Voltage (LV) network. By testing at the PNDC, the evaluation of the SOP's response can be accelerated by applying many different network events in succession, as opposed to waiting for them to occur 'naturally' when the unit is operating within UKPN's LV network. This also allows the SOP operation in situations that may seldom be encountered in practice to be evaluated.

The SOP is designed to allow meshed/interconnected LV network operation and control of power flow across the "open point". The SOP facilitates: voltage support and improved voltage profiles; deferred or avoided investment in reinforcement and installation of additional LV network infrastructure; reactive power support independent of real power transfer; phase unbalance improvement by injection of negative- and zero-sequence currents by the SOP; harmonic current compensation/improvement and current-limiting during faults.

During testing the SOP's electrical response was monitored using calibrated power quality analysers at the SOP output terminals. The SOP's surface temperature, audio noise and Electromagnetic Field (EMF) output were recorded at different levels of power output. The test programme involved evaluating the SOP's capability to:

1. Transfer three phase active power at different levels over extended time periods (up to 5 hours)
2. Transfer three phase reactive power at different levels
3. Transfer single phase active and reactive power
4. Support network voltage
5. Respond safely to network frequency variations and network faults (400 V and 11 kV)
6. Operate as an "End to End" solution. This relates to the SOP's capability to monitor the network and for the SOP's algorithm based control system to operate correctly based on the network information.

This exercise has shown that the SOP behaves as expected in several cases. However, there are a number of areas where unexpected, or out-of-specification behaviour, was observed. The unexpected responses primarily relate to the SOP: tripping unexpectedly, power output oscillating, failing to supply a reactive load, failing to operate at expected voltage/frequency thresholds and failing to inject a stable output current when operating with the algorithm enabled. More information on these issues are listed in the report conclusions and summary (section 5). For many of these issues, solutions have been proposed that could be incorporated into the next version of the SOP hardware and/or control algorithm.

Table of Contents

GLOSSARY

AC	Alternating Current
AVR	Automatic Voltage Regulator
DC	Direct Current
DSP	Digital Signal Processor
FR	Final Report
FUN-LV	Flexible Urban Networks - Low Voltage
GM	Ground Mounted
HMI	Human Machine Interface
ICCs	Inverter Control Cards
LAN	Local Area Network
MCB	Miniature Circuit Breaker
MG	Motor Generator
PED	Power Electronic Device
PED	Power Electronic Device
pf	Power Factor
PLL	Phase locked loop
PNDC	Power Networks Demonstration Centre
PSU	Power Supply Unit
RMS	Root Mean Square
RTU	Remote Terminal Unit
SOP	Soft Open Point
THD	Total Harmonic Distortion
THDi%	Total Harmonic Distortion of current expressed as a percentage of the fundamental
THDv%	Total Harmonic Distortion of voltage expressed as a percentage of the fundamental
PLC	Programmable Logic Controller
TPS	Turbo Power Systems
UKPN	United Kingdom Power Networks

2 INTRODUCTION

The objective of this project is to test a Soft Open Point (SOP) Power Electronic Device (PED) under different network operational scenarios at the PNDC. The report is separated into the following sections:

Section 3 of this report presents a brief overview of how the SOP operates and the SOP Human Machine Interface (HMI) used during testing. This overview considers aspects of the HMI that are relevant to the testing presented in this report. A more detailed description of the HMI is available in Appendix A.

The first part of Section 4 contains a description of the test configuration used during the SOP test programme. It should be noted that this default configuration was modified as required for each test. The subsections within Section 4 relate to specific tests within the overall programme. Each subsection contains:

- An introduction explaining the objective of the test and the aspect of the SOP that is being evaluated by completing the objective.
- A method section with a breakdown of each step in the test.
- A results section with graphs of the data recorded during the test from the power quality analysers, EMF, temperature and audio measurement equipment.
- An analysis section where the data presented in the results section is reviewed.
- A conclusions section with a list of the key findings from the test.

Section 5 contains a summary of the key findings from the report.

3 SOP OPERATION

The SOP is a power electronic device designed to be installed at normally open points within a power network. The SOP tested at the PNDC is a three terminal device, which contains three, three phase inverters connected via a DC link. This configuration allows bi-directional power flow between the three terminals of the inverter, as illustrated in Figure 1. In the scenario shown in Figure 1 inverter A is importing power and inverter B and inverter C are exporting power. Each of the Powerlock cable connections shown in the diagram include three separate phase cables, one neutral cable and one earth cable.

This diagram also shows the SOP DNP3 based communication and monitoring system including: the current clamps, the voltage probes, the LV monitoring units, and the RTU. The LV monitoring units aggregate analogue current signals (from current clamps at different points on the network) and analogue voltage signals (from the terminals of the SOP). These monitoring units convert the analogue voltage and current data to a DNP3 signal and via DNP3 transfer it to the Remote Terminal Unit (RTU). The RTU aggregates the data and passes the DNP3 signal to the PLC within the SOP. It's not shown on this diagram but the RTU has an internet connection for remote monitoring and control. The PLC contains the SOP algorithm. The SOP algorithm is a supervisory control system that makes control decisions related to voltage support, load support, reactive power support and phase unbalance. It makes these control decisions based on measurement data it receives from the RTU and from local measurements within the SOP hardware. To implement these control decisions the algorithm sends set points to the Inverter Control Cards (ICCs) contained within each of the inverter units. The ICCs implement the set points from the PLC by control of the inverters. The ICCs also implement control actions based on local measurements within the SOP e.g. the protection functionality related to overcurrent and over/under frequency protection is implemented by the ICC based on measurements taken at the terminals of each inverter.

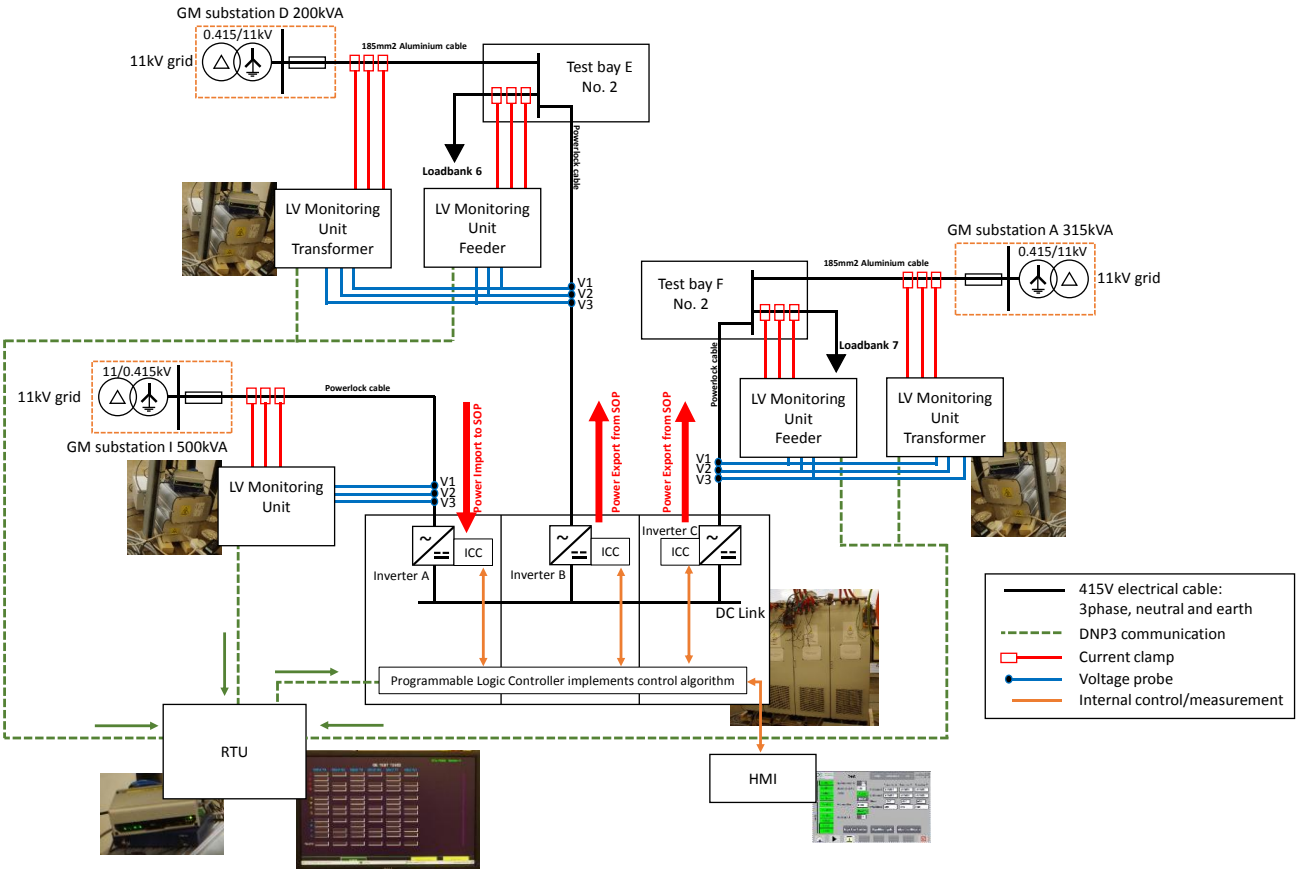


Figure 1: LV monitoring unit, RTU and control system configuration (test configuration at the PNDC)

The objective of the SOP is to enable meshed/interconnected network operation and control of power flow across the "open point". By enabling power flow across the open point the SOP can provide:

- Voltage support and improved voltage profiles;
- Deferred or avoided investment in reinforcement and installation of additional LV network infrastructure;
- Reactive power support independent of real power transfer;
- Phase unbalance improvement by injection of negative- and zero-sequence currents by the SOP;

A typical operation for the SOP is to reduce loading on a transformer (to avoid the need for additional network reinforcement or demand disconnection). This can be illustrated with the network configuration shown in Figure 1. If Substation D is loaded beyond its 200 kVA rating, the LV monitoring Unit on Substation D measure and transmits that data to the RTU (where the data is aggregated) and the RTU transfers that data to the Programmable Logic Controller (PLC) within the SOP. The algorithm running on the PLC detects that the pre-programmed threshold associated with transformer load support (*Feeder import trip*) has been exceeded and sends a control set point to the ICCs. Inverter B is controlled to export power in order to reduce the load on substation D and inverter A is controlled to import power to compensate for the export at inverter B.

In the prototype unit tested at the PNDC inverter A acts as the 'slack bus' compensating for the import/export at inverter B and inverter C. The SOP manufacturer Turbo Power Systems (TPS) have advised that in the final version of the SOP there is not a dedicated 'slack bus' inverter and the algorithm will control the import/export of each inverter based on inverter availability and network constraints. The SOP voltage support, reactive power support, and phase unbalance improvement operate on the same principle as the transformer load support.

The prototype unit that was tested at the PNDC can also be controlled manually via the SOP HMI to inject or export power at inverter B and inverter C, this is discussed in the following section.

As this is a prototype unit there was no operation manual available from the manufacturer (TPS) prior to commencing testing. Before testing was started, a basic user guide for using the SOP at the PNDC facility was prepared by TPS and PNDC. This guide was revised as testing progressed and the final version of the guide is available in Appendix C.

3.1 SOP user interface

From the HMI SOP user interface, shown in Figure 2, the SOP can be controlled to inject three phase active and reactive power from inverter B and inverter C by specifying figures in the cells shown in Figure 2. Inverter A compensates for the control of inverter B and C and therefore cannot be controlled e.g. if inverter B, P_{demand} is set to 50 kW then inverter A will compensate by automatically setting to -50 kW. The first stage in starting the SOP is to select the enable button on the HMI interface (refer to Appendix C for a breakdown of the start-up procedure). Selecting the enable button will turn on the SOP and connect it to the 3 incoming 3 phase grids in the correct sequence. After the SOP has completed the start-up sequence it will begin drawing power from the network to supply the SOP LCL filter and power electronics. At this stage the SOP can be controlled to transfer power between the inverter terminals.

Please note: during the testing procedure TPS modified the HMI interface, Figure 2 shows the original interface, the final version of the interface is shown in Appendix A. The HMI also gives several indicators of the status of the unit including the state of each inverter and whether the inverter is communicating with the control system (heartbeat indicator). Each inverter state is identified by a three digit number, the first number indicates the state of the PLC within the inverter and the second two digits indicate the state of the inverter. A summary of the state codes and their associated meanings (as provided by TPS) is presented in Table 1 and Table 2.

The HMI interface also enables the user to configure settings within the SOP control algorithm. More information about how the algorithm settings can be modified is specified in Appendix A.

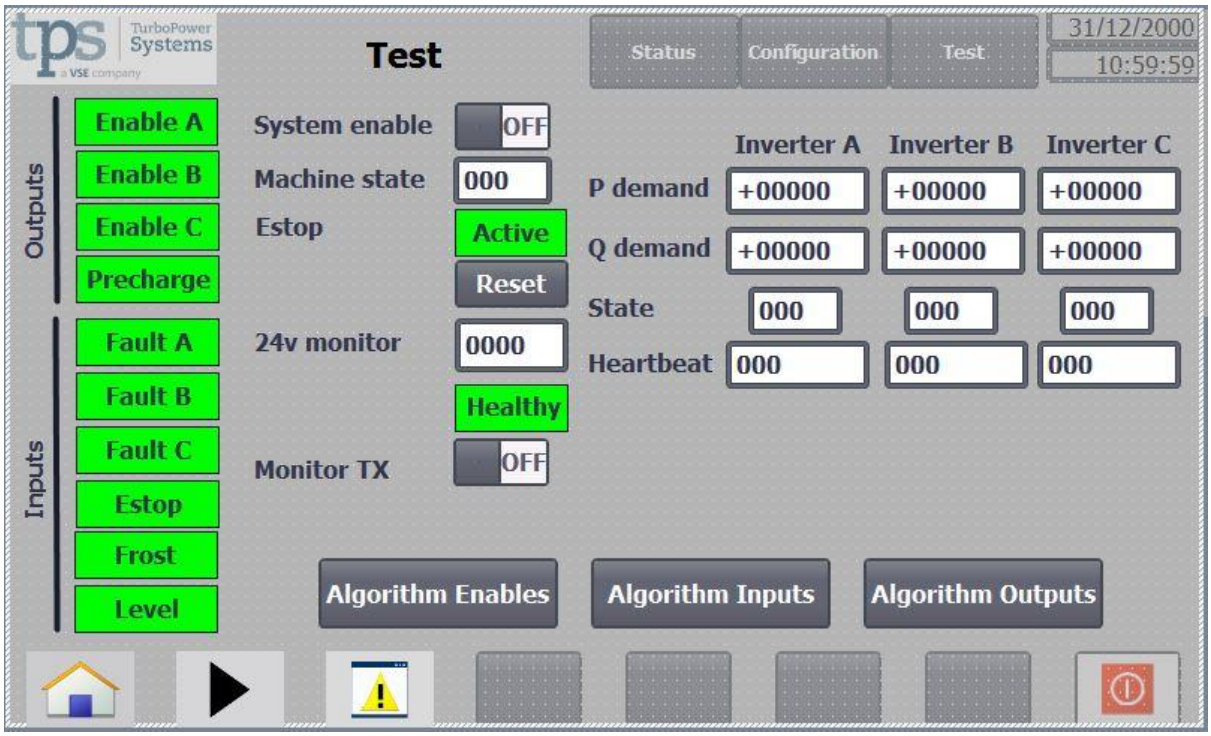


Figure 2: SOP HMI

Table 1: SOP HMI PLC State – digit #1 (PLC State)

Digit	Meaning
0	Waiting for start
1	Assign DC Link Controller
2	Pre-charge
3	Connect DC Link Controller
4	Start Power Controllers
5	Connect Power Controllers
6	Running
7	Shut Down Power Controllers
8	Shut Down DC Link Controller

Table 2: SOP HMI Inverter State – digit #2 (PLC State)

Digit	Meaning
0	Power Up LAN
1	Waiting for LAN
2	Waiting for LAN Messages from PLC
3	Waiting for Mode Assignment
10	DC Link Controller, waiting for start command
11	DC Link Controller, Pre-charge dc link
12	DC Link Controller, Connected
13	DC Link Controller, Inhibited
14	DC Link Controller, Locked Out
15	DC Link Controller, Emergency Stop
20	Power Controller, waiting for operating conditions
21	Power Controller, Synchronise with grid
22	Power Controller, Connected
23	Power Controller, Inhibited
24	Power Controller, Locked Out
25	Power Controller, Emergency Stop

3.2 SOP Settings

The SOP settings were modified using the HMI (from the default settings on delivery) during testing under the guidance of TPS and also directly by TPS after development work. The settings were altered in different test scenarios to correct unexpected behaviour or to configure a threshold to be exceeded for the purposes of the test e.g. in the End to end test, the value of *'Feeder import trip'* was reduced so that it would be exceeded when a load was applied to the network. This variable is a current threshold, if the current import from the transformer exceeds this threshold the SOP will begin injecting current to reduce the current contribution from the transformer.

A full description of each of the display and configuration (parameter modification) screens as well as default values for each of the parameters is given in Appendix A. Where a parameter has been modified specifically for the test it will be specified in the test 'method' section.

4 TEST SETUP AND RESULTS

The SOP is connected to the PNDC electrical network as shown in Figure 3. The 11kV configuration of the PNDC electrical network is shown in Figure 4. This diagram shows the 11kV network configuration for the first three tests: the balanced three phase load test, Load cycle test 1 and load cycle test 2. In the later tests (from the three phase reactive power support test onward) the PNDC 11kV network was supplied from the MG Set, this was a network operation decision and did not influence the testing plan. There were two reasons for using the MG Set in the later tests: (1) the MG set allows the network voltage to be modified faster than manually changing the tap setting of the isolation transformer (used to change the voltage of the network while grid connected) and (2) the MG set enables the voltage of the network to be changed in smaller increments. The greater control afforded by using the MG set allowed the network voltage to be decreased until the power oscillations observed in the SOP output (previously occurring at high voltages) were no longer observed. A photograph of the test setup is shown in Figure 5.

The 11kV configuration was modified for several of the tests including the: phase unbalance improvement test (single phase real power support), single phase reactive power support test, Voltage support test, and End to end test.

The SOP contains three, three phase inverters linked together internally via a common DC bus. The inverters are connected to the PNDC network using the VEAM PowerLock connection system [1]. The connection to the SOP includes three separate single phase cables, one neutral connection and one earth connection. Inverter A is connected directly to the LV side of the 500 kVA substation I, Inverter B is connected to the PNDC test bay E No. 2 which is connected via the PNDC network to the 200 kVA substation D, and inverter C is connected to the PNDC test bay F No.2 which is connected via the PNDC network to the 315 kV substation A. Also connected to the SOP are:

1. A coolant system for cooling the power electronics within the SOP. This coolant system circulates water around the cabinets and utilises an extractor fan to dissipate heat from the water.
2. LV monitoring units for monitoring voltage and current on the cables: (1) coming from the transformer into the test bay and (2) from the test bay to the load bank, as shown in Figure 1.
3. An HMI touch screen display. The HMI is a touch screen interface that allows the user to control the SOP's balanced three phase active and reactive power transfer from inverter B and C within the SOP. For example, using the HMI, the user could specify a value for $P_{inverter\ B}$ of 50 kW. The SOP would then import 50 kW from inverter A to accommodate this command.
4. An emergency stop push button. The emergency stop trips the MCBs on each of the inverters' incoming feeders within the SOP and also sends a command to stop the SOP via software. The emergency stop was tested at the start of each test day prior to beginning testing. To confirm the emergency stop was working the following indicators were noted:
    a. There is an audible noise as the CBs open
    b. The 'state' of the SOP displayed on the HMI changes to: 15 25 25
    c. The DC bus voltage falls to 650 V from the previous pre-charge state. The pre-charge state prior to the CBs opening is 750 V. The DC bus falls to 0 V after the 11 kV network is de-energised. The DC bus does not fall to 0 V when the CBs are open because the DC link supply bypasses the CB circuit.
5. Three FLUKE Power Quality Analyser 435-II monitoring units were used to record voltage, current, real and reactive power, voltage and current harmonics at the three terminals of the SOP. The voltage probes from each FLUKE were connected to the neutral plate mounted externally on the SOP, the earth plate (also mounted externally from the SOP), and to each of phases within the SOP cabinets. Current transformer clamps (FLUKE i1000s clamps) were installed on the PowerLock cables connecting to each inverter on each phase and the neutral. The FLUKEs were configured to take recordings of average values over intervals of 5 s.

For all test results reported the following convention is used to indicate direction of power flow:

Table 3: Power flow convention in relation to HMI interface

HMI setting	Power flow direction from SOP inverter	Graph value
Positive	Export	Positive
Negative	Import	Negative

During the commissioning stage and prior to commencing the first test, it was found that the SOP was not functioning effectively at the default network voltage level. TPS asked that the voltage of the network be reduced. To accommodate this, the tap setting of the 11/11 kV isolation transformer feeding the 11 kV network was decreased to lower the voltage of the LV network for most of the test programme, the original voltage was 250 V and the final voltage (after tap reduction) was 235 V. This temporarily resolved the issue which was later solved by TPS by (1) increasing the voltage output limits on the resonant controllers within the SOP and at a later stage (2) applying a further increase to the voltage output limits on the resonant controllers and also increasing the upper limit of the DC link Voltage (increased to 775Vdc). Both limits were increased by changing the settings on the SOP ICCs.

TPS have advised that the resonant controller is a feedback controller that produces a sine wave output based on input control values. There is a dedicated resonant controller for each inverter. The oscillation in the power output from the inverters was caused by the resonant controllers reaching their upper limits when the inverters were controlled to export power (i.e. increase their AC terminal voltage). In the later tests the upper limits of both the resonant controllers and the DC link voltage were increased to allow the inverters to export power (by increasing their AC terminal voltage) when the network voltage was at higher voltage levels i.e. greater than 235 V.

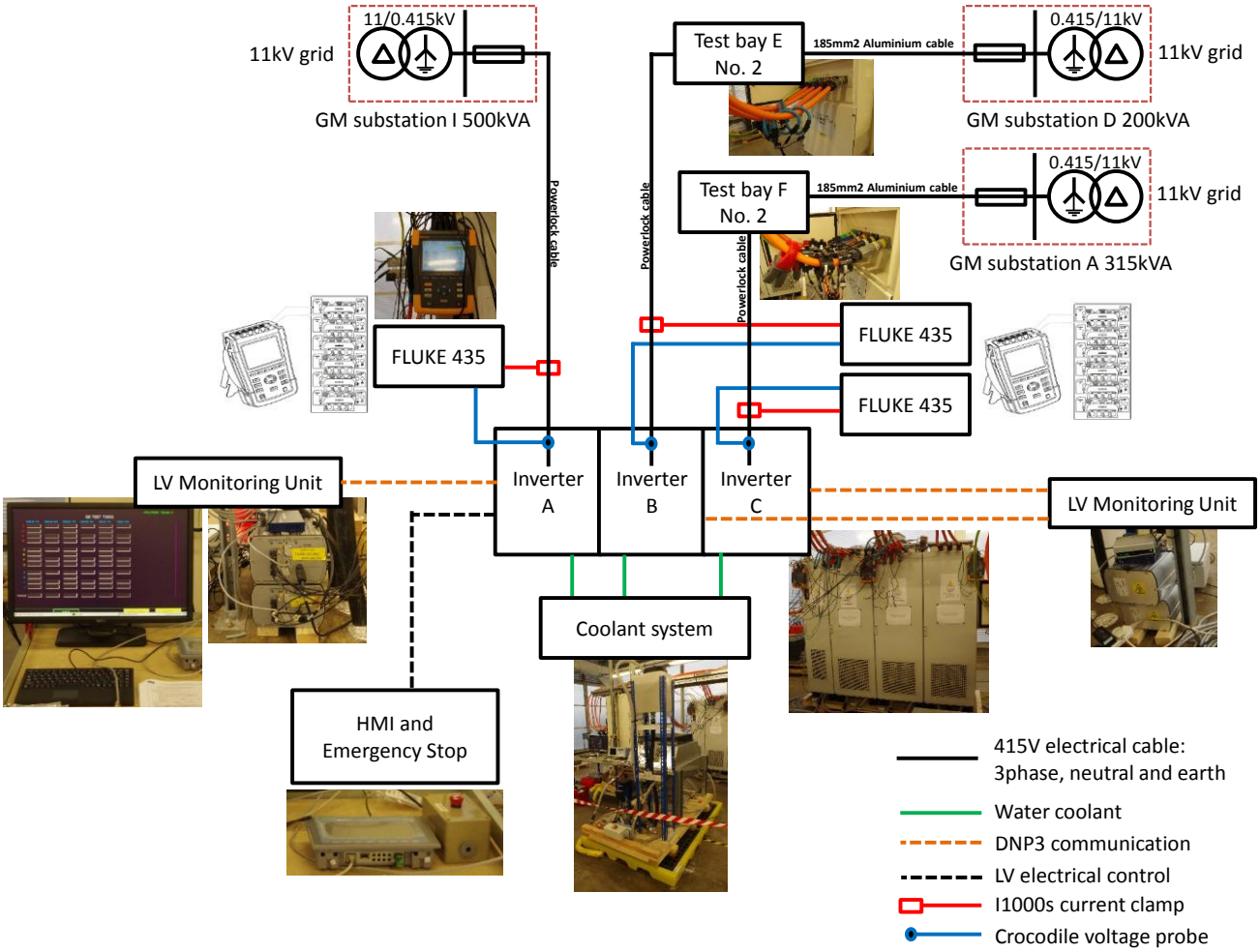


Figure 3: Test configuration line diagram (test configuration at the PNDC)

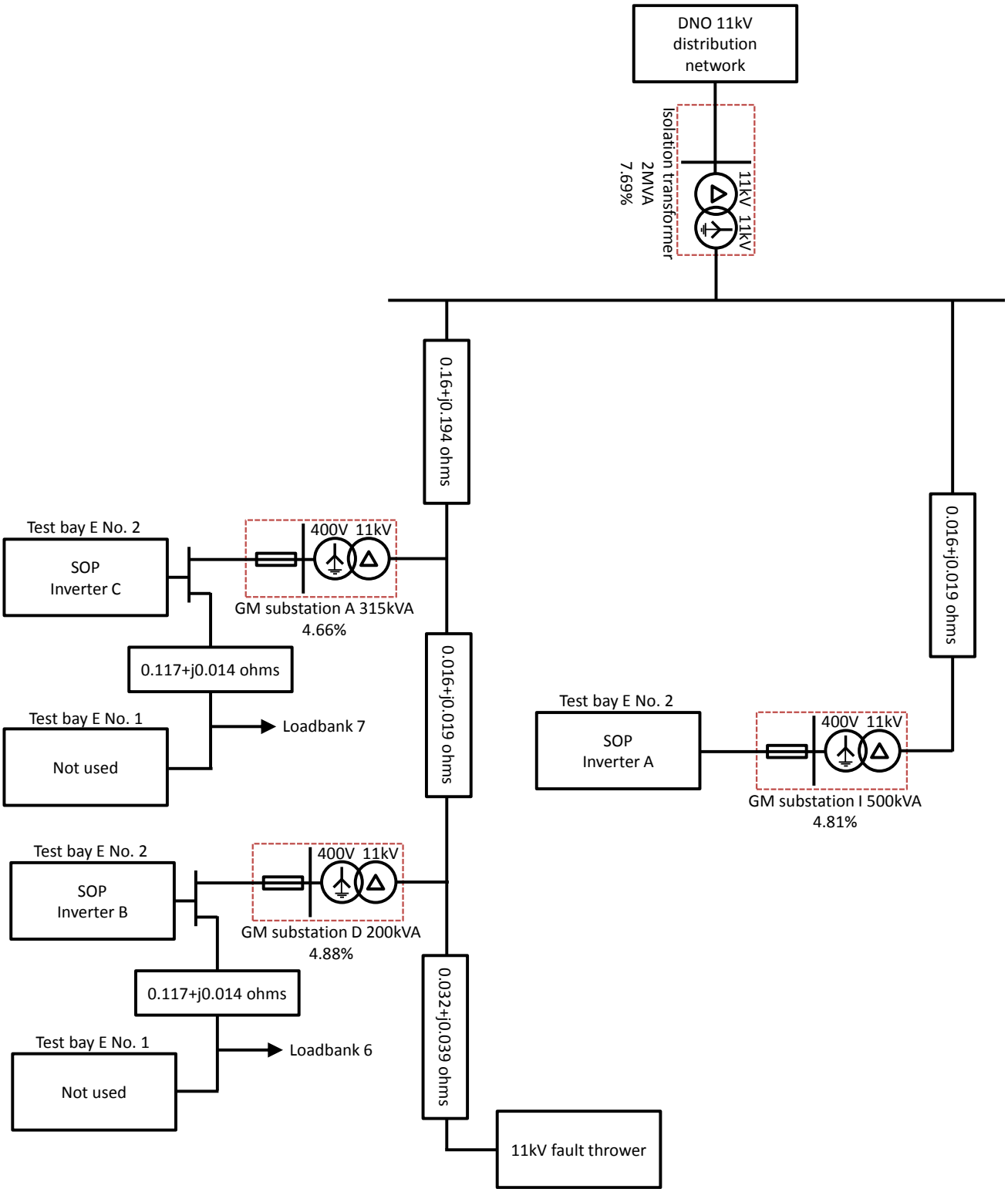


Figure 4: 11kV test configuration line diagram (test configuration at the PNDC)

Figure 5: Test configuration photograph

4.1 Balanced three phase load test

The objective of this test is to record the operation of the SOP when the three phase active power output from the SOP is controlled using the HMI. The SOP was controlled to export varying levels of balanced three phase active power from each inverter in turn. The amount of power the SOP was controlled to export (into the network) was based on the rating of the transformer each inverter was connected to e.g. inverter B (within the SOP) was connected to substation D which has a rating of 200 kVA, therefore inverter B was controlled to export up to 200 kVA at a pf of 1.

As specified in section 3, inverter A cannot be controlled directly. To achieve the objective of this test inverter A was controlled to export active power by setting a negative power on inverter B and inverter C. This meant inverter B and inverter C imported active power. To balance the import at inverter B and C, inverter A was controlled (by the SOP control system) to export power.

This test evaluates the SOP's capability to transfer power from one inverter to another based on the HMI setting (or "commanded" operation), this test does not evaluate the SOP's automatic mode of operation, where it responds to measured and detected conditions automatically using its control scheme and embedded algorithms control system. The testing plan is specified in [2] and the log from the test is listed in the following section.

4.1.1 Log of test procedure

The list below describes the procedure followed during testing (as specified in the testing plan [2]).

1. The SOP was enabled, as specified in the introduction of section 3 enabling the SOP begins the start-up sequence and brings it to a ready state where it can be controlled to transfer power between the inverter terminals.
2. Using the SOP HMI inverter B was set to export +50 kW (from 0 kW in one 50 kW step). See Figure 6 for the three phase active power response recorded from this test.
3. Using the SOP HMI the inverter B setting was increased to export +200 kW (in steps of +50 kW).
4. This power injection was maintained at +200 kW export for 10 mins and then decreased via the HMI to 0 kW in one step.
5. Using the SOP HMI inverter B and inverter C were set to:
    a. Inverter B export +50 kW (from 0 kW in one 50 kW step).
    b. Inverter C export +80 kW (from 0 kW in one 80 kW step).
6. Using the SOP HMI inverter C was increased in 50 kW steps to export +315 kW (final step from 280 kW to 315 kW). This equates to 100 % capacity of substation A.
7. Using the SOP HMI inverter C was decreased to export +126 kW in one step (40 % capacity of substation A).
8. Using the SOP HMI inverter C was decreased to export +80 kW in one step (25 % capacity of substation A).
9. Using the SOP HMI inverter B was increased in 50 kW steps to export +200 kW (100 % capacity of substation A).
10. Using the SOP HMI inverter B was decreased to export +80 kW (40 % capacity of substation A).
11. Using the SOP HMI inverter B (substation D) and inverter C (substation A) were set to 0 kW in one step.
12. As specified in section 3.1, because inverter A (substation I) is the 'slack' bus that imports or exports power to compensate for the exported/imported powers of inverters B and C, the HMI does not allow the user to specify a power import of export at inverter A. In order to control inverter A to inject power, inverter B and inverter C were set to negative values on the HMI interface.
13. Using the SOP HMI inverter B was increased in -50 kW steps to import -160 kW (last step of -10 kW).
14. Using the SOP HMI inverter C was increased in -50 kW steps to -160 kW (last step of -10 kW).
15. This resulted in inverter A injecting 320 kW to compensate.
16. Using the SOP HMI inverter B (substation D) and inverter C (substation A) were set to 0 kW in one step.

17. The SOP was disabled via the HMI at 12:50.

4.1.2 Results

As the SOP was controlled to inject **balanced** three phase power, the voltage, current, power and harmonic differences between phases (on the same inverter) was negligible and therefore they have not been reported here. To compare the relative inputs and outputs between the SOP inverters, the voltage, current and harmonic recordings for phase A of each inverter have been graphed below. For a breakdown of the test procedure please refer to the following 'Analysis' section. An annotated break down of this response is given in the following Analysis section.

The three phase active power recorded at each SOP inverter is shown in Figure 6. It should be noted that the SOP did not meet the settings defined via the HMI e.g. at 11:55 inverter B was set to export +200 kW but the measured response was approximately 164 kW. The cause of this discrepancy appears to be due to the upper limit on the resonant controller being set too low. In Load cycle test 1, the discrepancy between HMI set values and the measured values is also observed but in Load cycle test 2 (after the upper limits on the resonant controller have been increased) the discrepancy between the set and measured value is reduced to 5.5 kW. TPS have advised that this smaller discrepancy is likely to be due to the power requirements of the SOP LCL filter and power electronics.

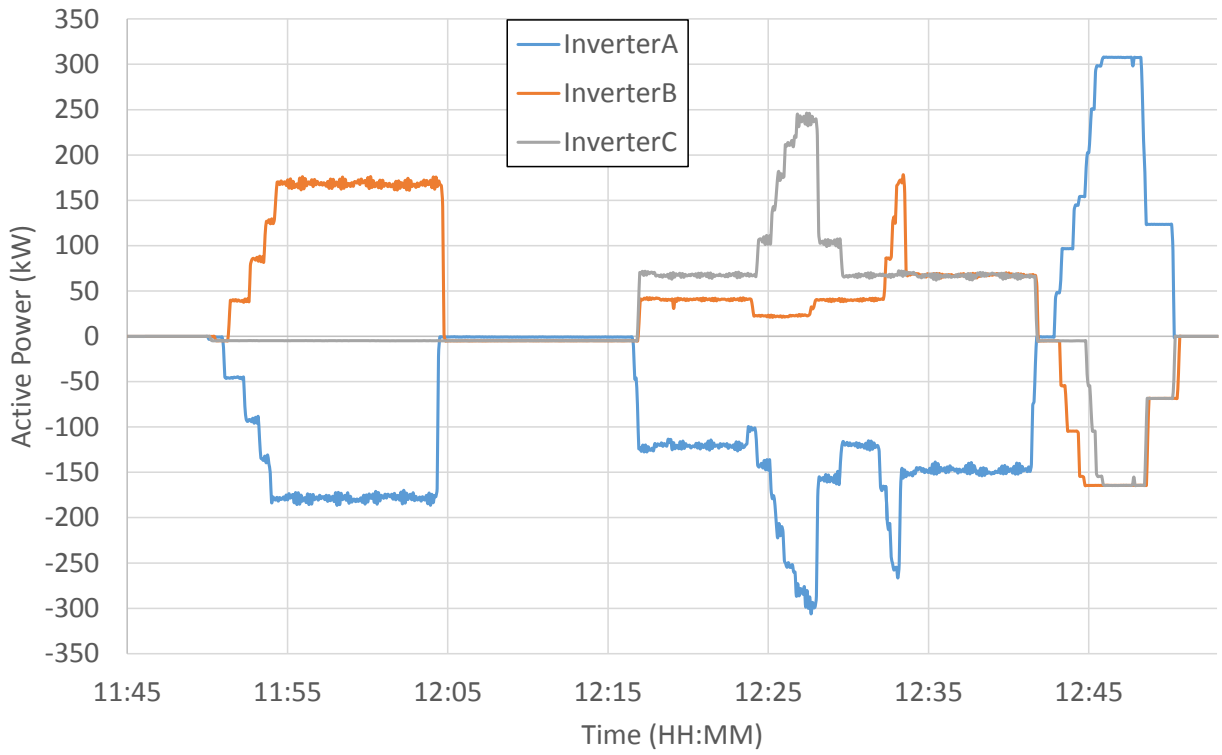


Figure 6: Three phase active power recorded at SOP terminals

The phase A RMS voltage recorded at each SOP inverter is shown in Figure 7. The y-axis has been scaled to illustrate the voltage difference between the inverters, the voltage prior to 11:42 and post 13:24 was recorded at 0 V.

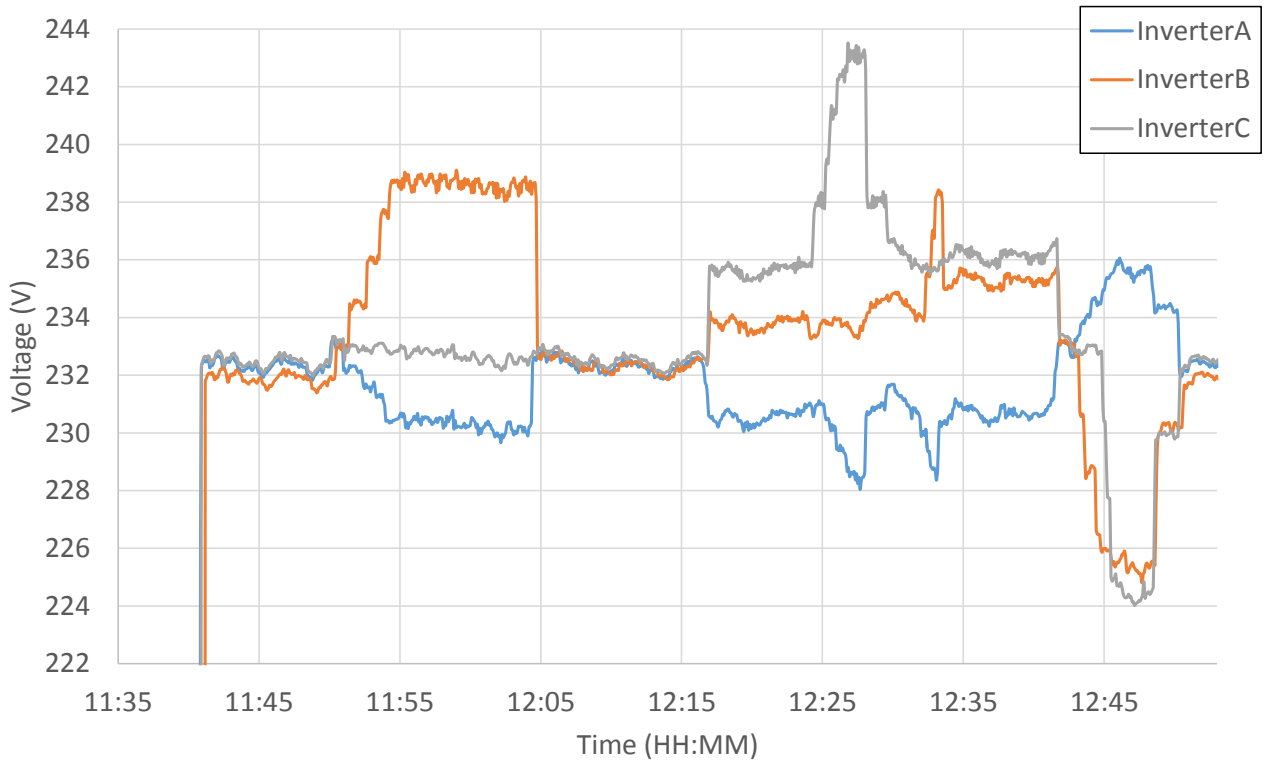


Figure 7: Phase A RMS voltage recorded at SOP terminals

The phase A RMS current recorded at each SOP inverter is shown in Figure 8.

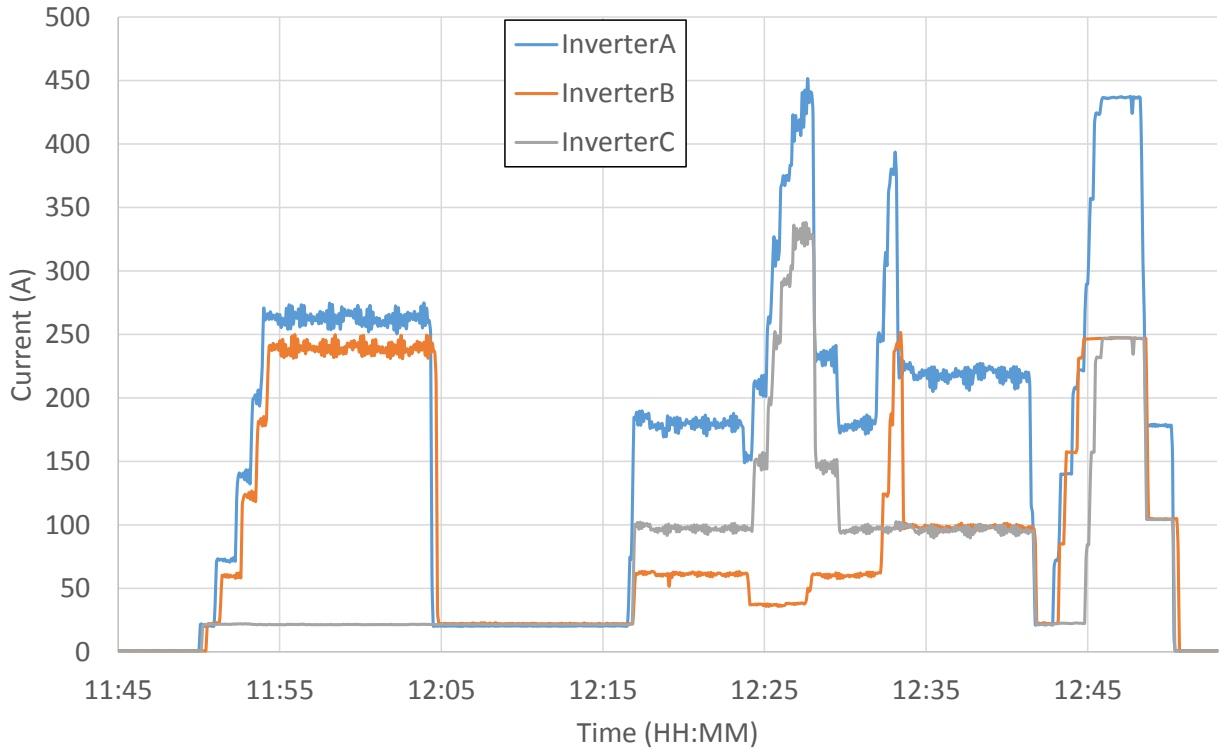


Figure 8: Phase A current recorded at SOP terminals

The three phase reactive power recorded at each SOP inverter is shown in Figure 9. It should be noted that the reactive power of the SOP was not controlled via the HMI during this test.

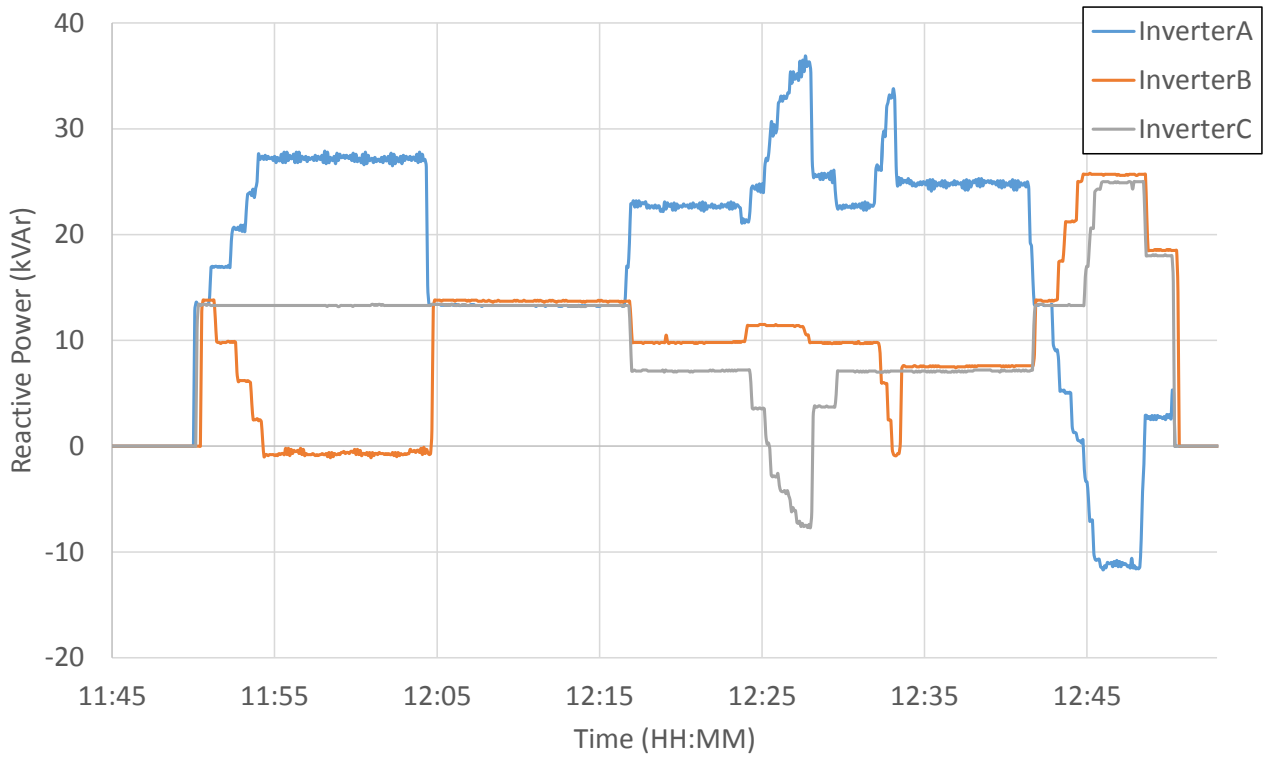


Figure 9: Three phase reactive power recorded at SOP terminals

The phase A Voltage Total Harmonic Distortion (THDv%) recorded at each SOP inverter is shown in Figure 10. The THDv% is the total harmonic distortion of voltage expressed as a percentage of the fundamental. It can be observed that the THDv% of the SOP increases as the injected active power increases as expected. In fact as the current injected by the SOP in the network increases, the impact on the THDv% increases, as the current injected is a source of harmonics. For example, at 12:10 inverter B on the SOP HMI is set to 0 kW and 0 kVAr, at this time the THDv% of inverter B is lower than at 12:47 when the inverter B is set on the SOP HMI to export +200 kW.

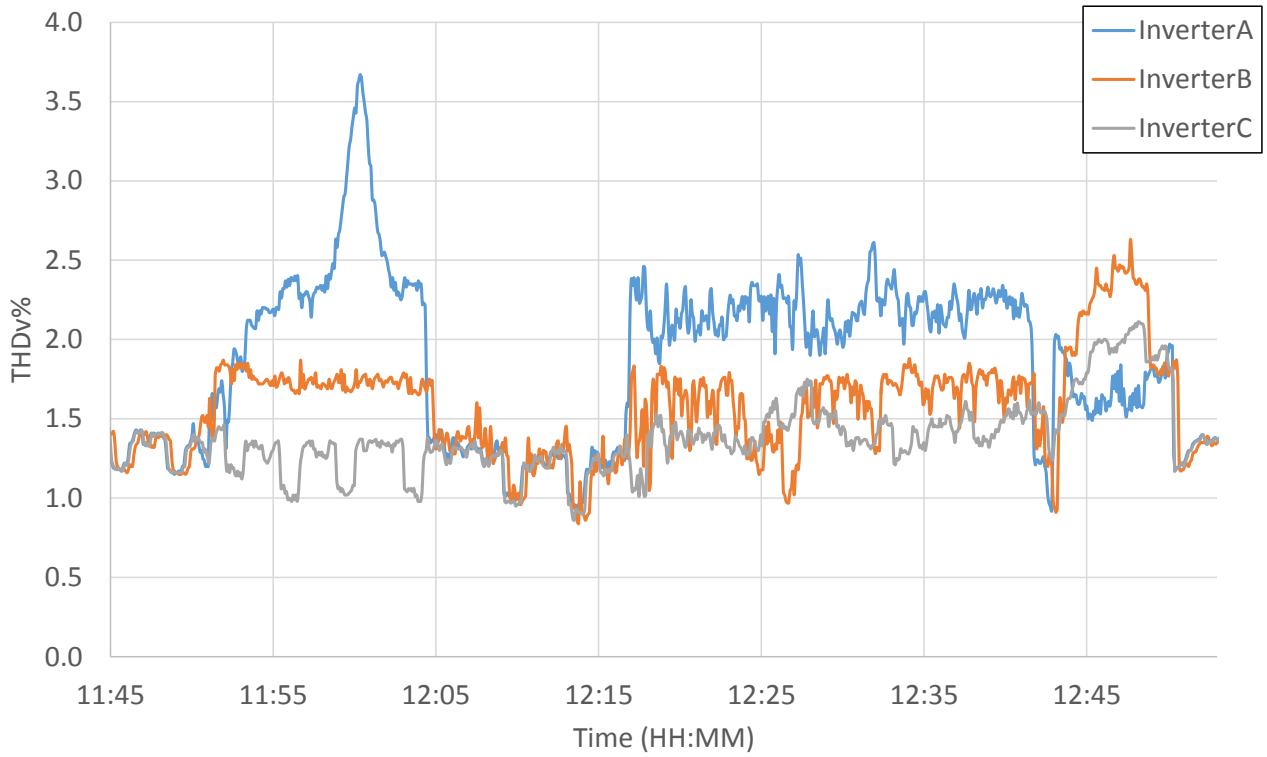


Figure 10: Phase A THDv% recorded at SOP terminals

The phase A THDi% recorded at each SOP inverter is shown in Figure 11. The THDi% is the total harmonic distortion of current expressed as a percentage of the fundamental. It can be observed that the high THDi% occurs when the SOP is disabled (using the HMI) as opposed to when the SOP is enabled. For example, before 11:50 the SOP is disabled and it can be observed that there is a higher THDi% response than when the SOP is enabled after 11:55.

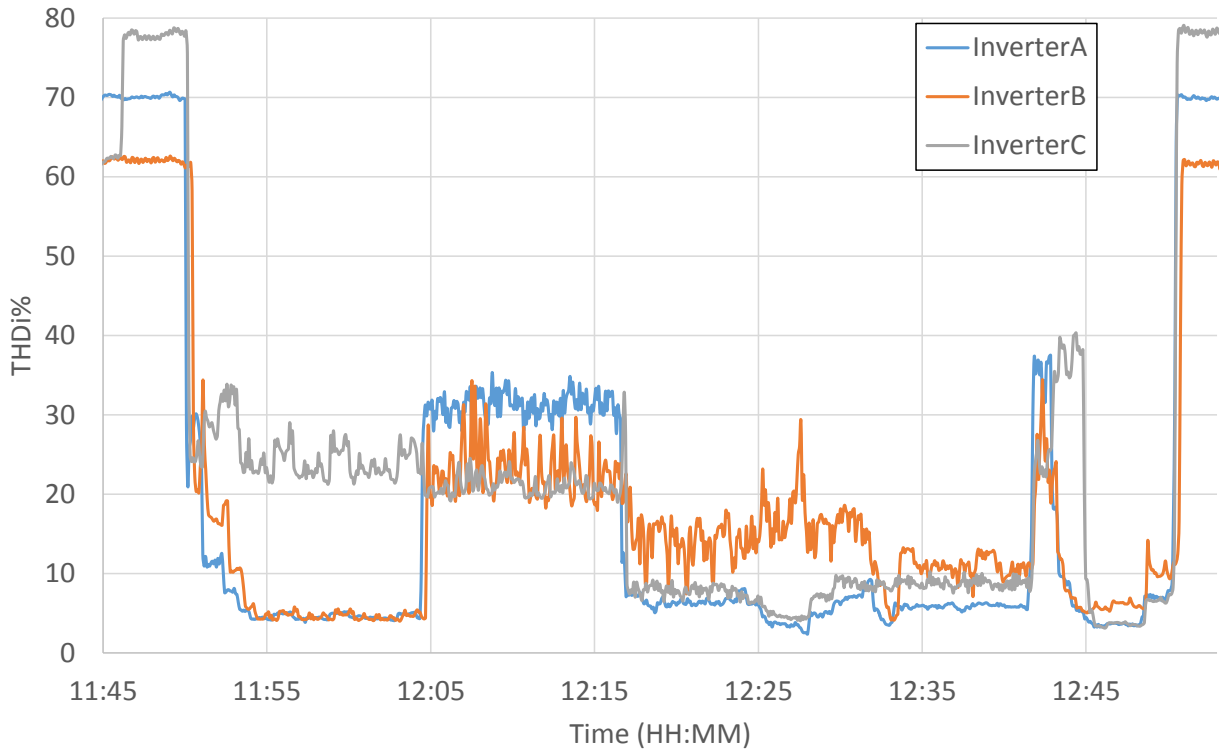


Figure 11: Phase A THDi% recorded at SOP terminals

4.1.3 Analysis

To illustrate the different stages of the testing plan, the active power recording shown in Figure 6 has been separated into two graphs shown in Figure 12 and Figure 13. Figure 12 shows steps 1-3 of the testing plan where inverter B was controlled via the HMI to export +200 kW for 10mins. This is a sub set of the response shown in Figure 6. This graph shows the total three phase active power **export** of approximately 170 kW from inverter B and a total three phase active power **import** of approximately 180 kW from inverter A over 10mins. As mentioned in the results section, the cause of this discrepancy appears to be due to the upper limit on the resonant controller being set too low. In Load cycle test 1, the discrepancy between HMI set values and the measured values is also observed but in Load cycle test 2 (after the upper limits on the resonant controller have been increased) the discrepancy between the set and measured value is reduced to 5.5kW. TPS have advised that this smaller discrepancy is likely to be due to the power requirements of the SOP LCL filter and power electronics.

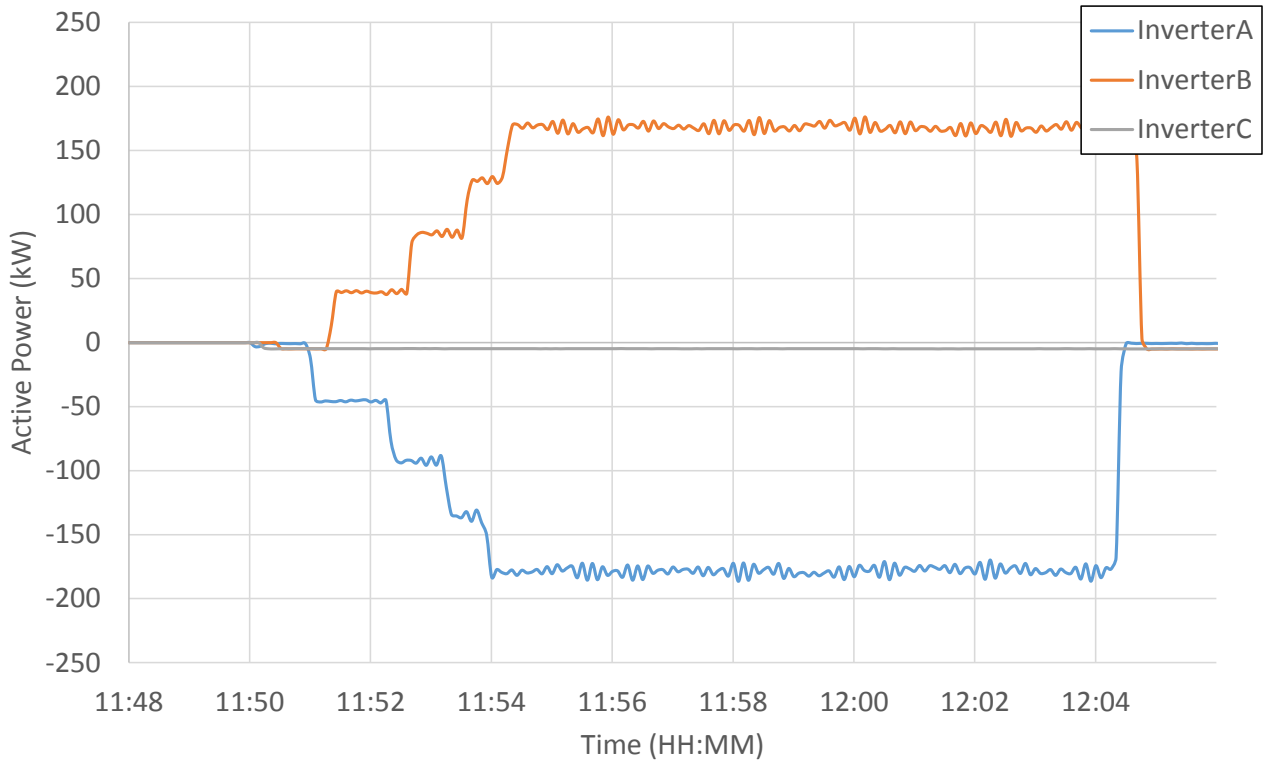


Figure 12: Total three phase active power (test log steps 1-3)

Figure 13 shows steps 4-17 of the testing plan and has been annotated to show the different power settings on the HMI. This is a sub set of the response shown in Figure 6. It should be noted that the oscillation in the active power recording does not occur after 12:42. In this part of the test inverter B and inverter C are set to import -160 kW via the HMI. The negative setting of both inverters appears to be linked to a reduction in oscillation in the power output.

The cause of the oscillation was later found to be as a result of the resonant controller and DC link thresholds being set too low. The upper limits of both were reached when the inverters were controlled to increase their AC terminal voltage to export power.

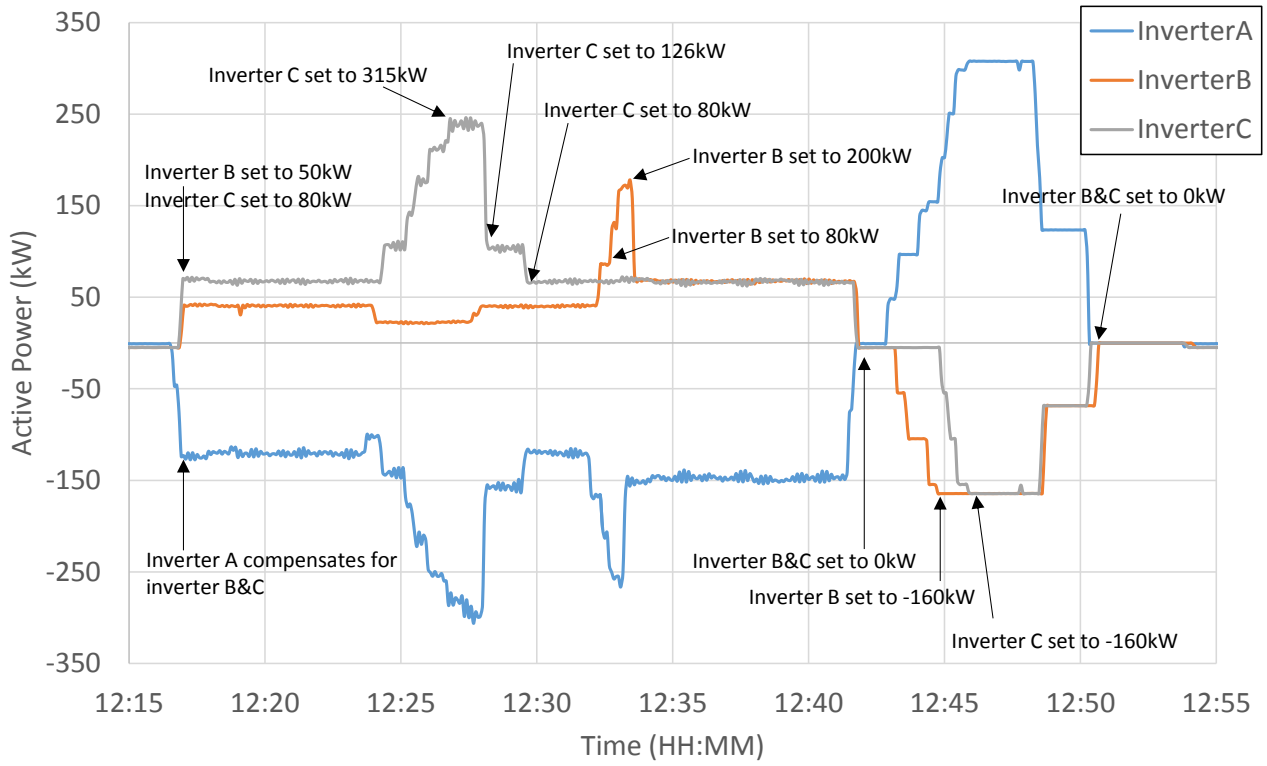


Figure 13: Total three phase active power (test log steps 4-15)

The results from this test indicated that when the SOP is enabled and prior to the SOP being controlled to import or export power (i.e. power settings are 0 kW and 0 kVAr on HMI) the SOP begins importing and exporting active and reactive power (a net total of active power of 11kW is consumed which attributed to the power requirement of the SOP i.e. the LCL filter and power electronics), as shown in Figure 14 and Figure 15. TPS have advised that this power transfer is related to the power requirements of the SOP to turn on and operate in a standby mode i.e. without actively transferring power either due to manual (via HMI) or algorithm control.

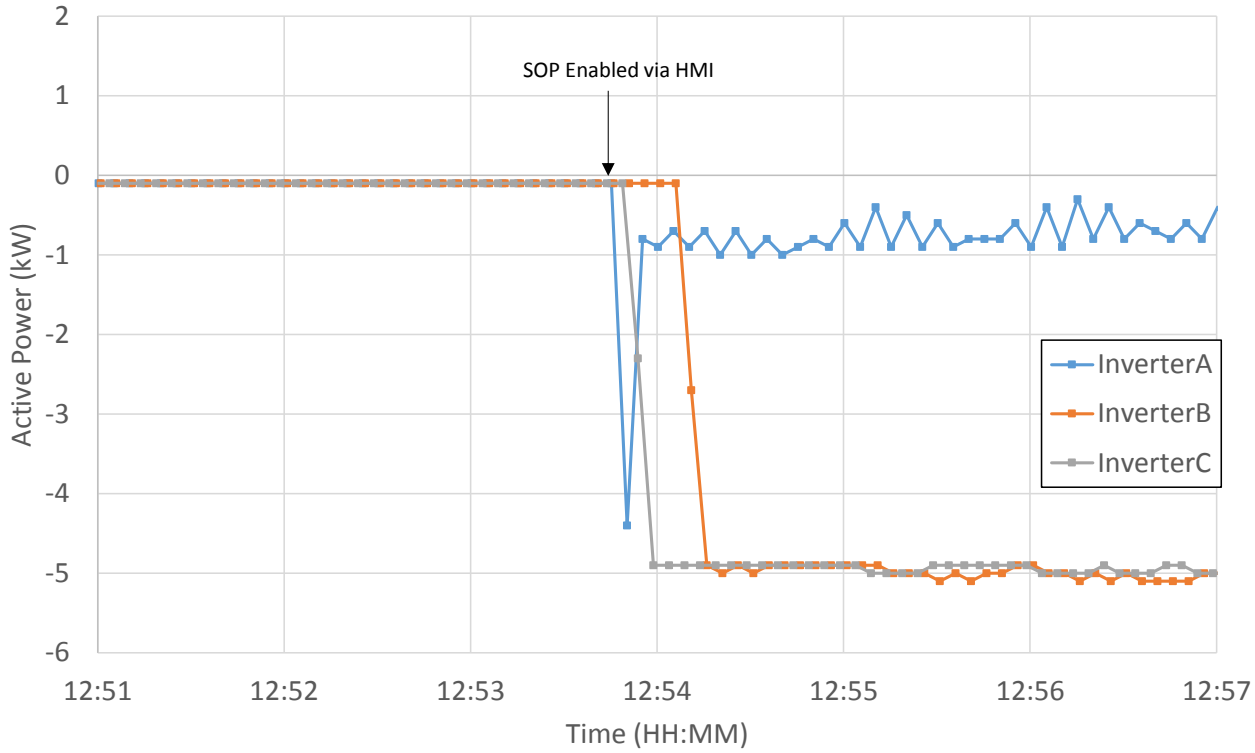


Figure 14: Total three phase active power at enable

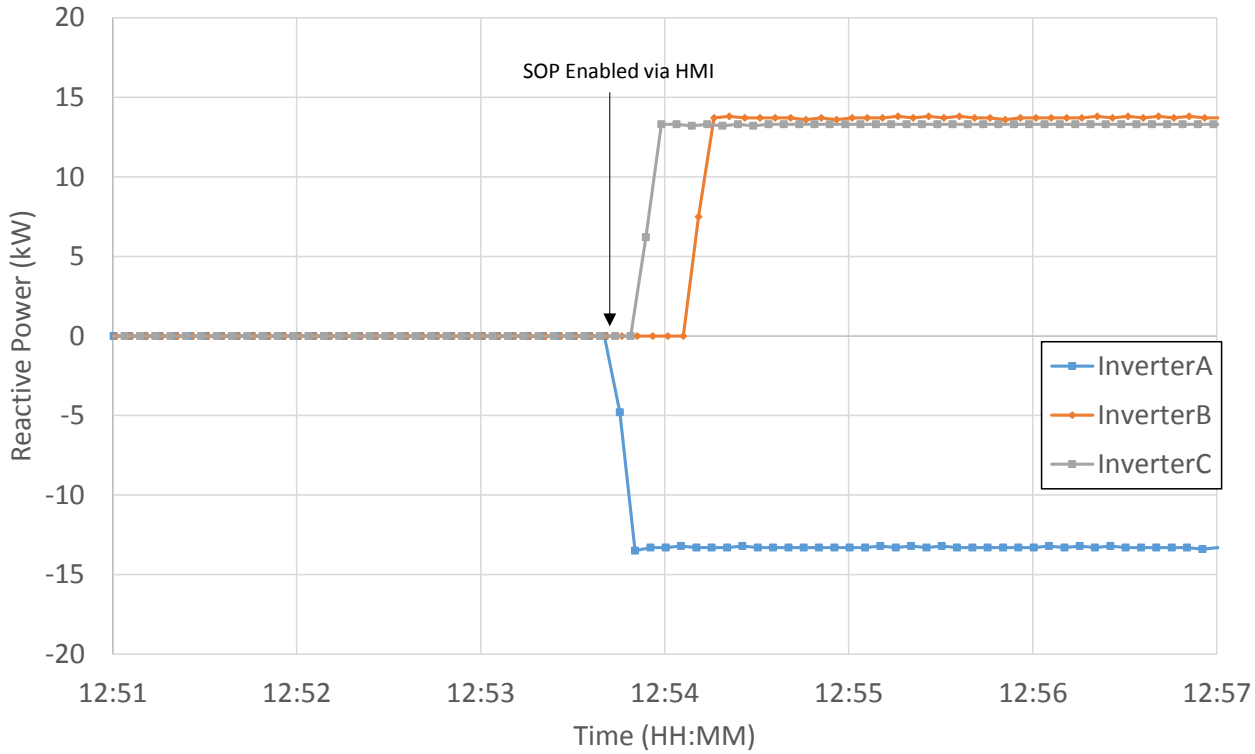


Figure 15: Total three phase reactive power at enable

4.1.4 Conclusions

This test evaluates the SOP's capability to transfer power from one terminal to another based on the HMI settings. The test results confirm that, when controlled to do so by the HMI, the SOP is capable of

transferring three phase active power up to the limits tested. The test results also highlighted two points relating to the SOP response:

1. There is an oscillation in the power output of the SOP on each inverter. The oscillation is observed when inverter B and inverter C are set to positive values on the HMI but not when they are set to negative values. The cause of the oscillation was later found to be as a result of the resonant controller and DC link thresholds within the SOP being set too low. These thresholds were increased in a later test and this was observed to resolve the problem for the remaining tests within the testing plan. Please note that this update was applied in two stages: (1) The voltage limit on the resonant controllers was increased prior to starting load cycle test 1 and (2) The voltage limit on the resonant controller was increased (again) and the DC link voltage upper limit was also increased prior to starting the phase unbalance improvement test. The impact of these updates on the SOP response is reported in the corresponding test sections.
2. The results from this test indicated that when the SOP is enabled and prior to the SOP being controlled to import or export power (i.e. power settings are 0 kW and 0 kVAr on HMI) the SOP begins importing and exporting active and reactive power. TPS have advised that this power transfer is related to the power requirements of the SOP to turn on and operate in a standby mode i.e. to supply power to the SOP LCL filters and power electronics without actively transferring power either due to manual (via HMI) or algorithm control.

4.2 Load cycle test 1

The objective of this test is to record the operation of the SOP when inverter A is controlled to follow the current (A) profile listed below:

- 2 h at 450 A
- 1 h at 225 A
- 2 h at 450 A.

In this test the FLUKE 435 power quality analysers were used to record power quality at the terminal of the SOP. The audio noise, surface temperature and EMF were recorded at locations on and around the SOP as shown in Figure 16. The blue circles indicate EMF and audio measurement locations and the red circles indicate surface temperature measurement locations.

This test evaluates the SOP's capability to supply there phase active power over an extended timescale. This test also evaluates the audio noise generated by the SOP at different power outputs, the temperature the surface of the SOP reaches when supplying power over an extended period; and the EMF generated by the SOP at different power outputs. The testing plan is specified in [2] and the log from the test is listed in the following section.

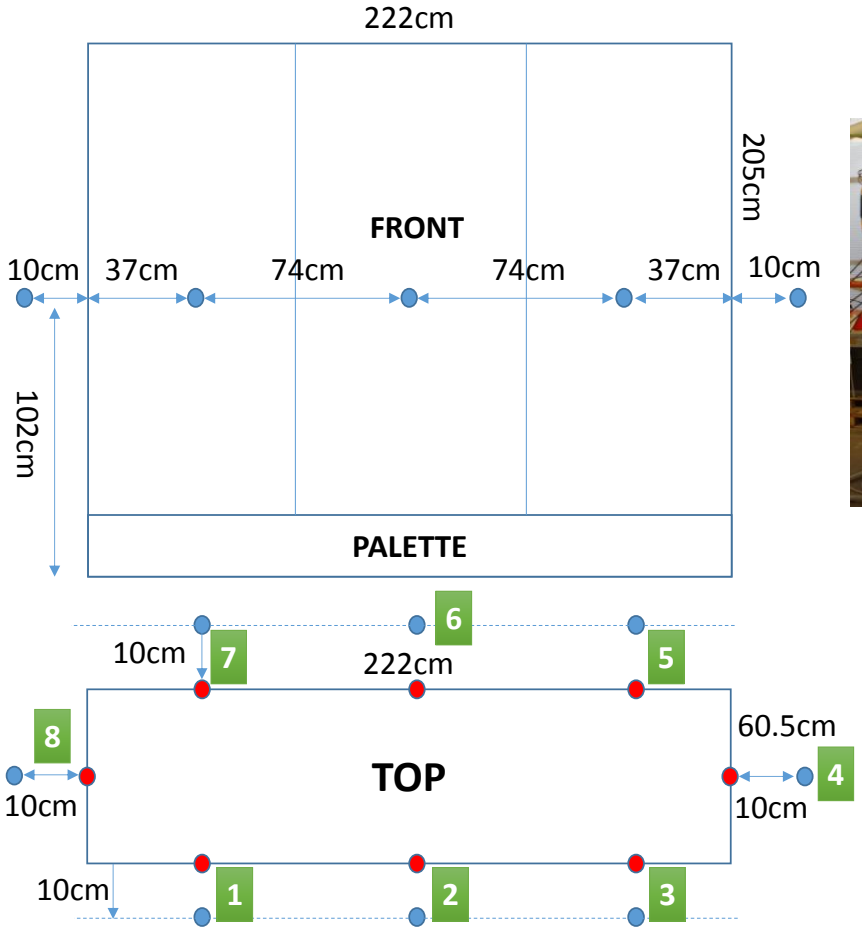


Figure 16: Audio noise, surface temperature and EMF measurement locations

4.2.1 Log of test procedure

The list below describes the procedure followed during testing (as specified in the testing plan [2]).

1. The SOP was enabled (see introduction of section 3 for explanation).
2. Using the SOP HMI inverter B and inverter C were set to:
    a. Inverter B (substation D) export set to +50 kW (from 0 kW in one 50 kW step).

   b. Inverter C (Substation A) export set to +80 kW (from 0 kW in one 80 kW step).
3. Using the SOP HMI inverter B and inverter C were increased to export +170 kW (in one step).
4. Note: At this stage of testing the current injection of 450 A was not achieved at inverter A (substation I) and the recorded current was oscillating up to approximately 427 A and down to approximately 361 A. TPS have suggested that the oscillating current is a result of the controller within the SOP being set to operate too quickly or too slowly. He also suggested that there may have been a software limit within the SOP controller that is preventing the 450 A export being achieved. A software update was installed at the end of this test day to address these issues. This software update resolved the problem (as demonstrated in section 4.3 Load cycle test 2).
5. These SOP HMI settings were maintained for 2 hours.
6. During this period the EMF measurements (recorded using Metrix VX0100 Electric Field Tester[1]) and audio measurements (AMPROBE SM-10 Sound Level Meter[2]) were taken.
7. Temperatures were recorded every 30mins from the beginning of the test (recorded using Testo 905-T2 surface temperature sensor[3]).
8. After 2h the HMI settings of inverter B and inverter C were reduced to:
   a. Inverter B (substation D) export set to +50 kW (from +170 kW in one step).
   b. Inverter C (Substation A) export set to +80 kW (from +170 kW in one step).
9. These HMI settings were maintained for 1 hour.
10. Using the SOP HMI inverter B and inverter C were increased to export +170 kW (in one step).
11. These HMI settings were maintained for 2 hours.
12. The HMI settings of inverter C was set to 0 kW (in one step) and the HMI settings of inverter B was maintained at export +170 kW.
13. During this period the EMF measurements and audio measurements were re-taken (at the reduced SOP power output).

4.2.2 Results and Analysis

During the test the following points were noted:

1. The SOP tripped unexpectedly three times during the test. TPS have been consulted and have been unable to identify a cause for the trips. They have advised that they have resolved issues relating to the inverter IGBTs and MCCB closing circuitry maloperating and this may have been a cause for the uncontrolled trips. Under the guidance of TPS the SOP was restarted following the process listed below:
   a. SOP trip 1 – SOP restarted by disabling and then re-enabling the SOP using the HMI interface.
   b. SOP trip 2 – SOP current injection dropped to zero but returned to nominal without external intervention.
   c. SOP trip 3 – SOP restarted by disabling and then re-enabling the SOP using the HMI interface.
2. At the end of this test, operational control of the SOP was returned to TPS and a software update was applied to the SOP. This update increased the voltage output limit on the resonant controllers. As will be observed in the "load cycle test 2" graphs this setting change removed the power oscillations observed during this test (see the introduction on the test setup at the beginning of section 4 for an explanation of the purpose of the resonant controller).

The power quality, temperature, audio and EMF data from the test is graphed below. The phase A RMS voltage recorded at each SOP inverter is shown in Figure 17. It can be observed from this graph that the recorded voltage increases as the test progresses (by approximately 4 V). The cause of this voltage ramp is unknown, TPS have advised that the SOP should not have caused this voltage rise. In this test the PNDC network is grid

[1] http://www.test-meter.co.uk/metrix-biotest-vx0100-electric-field-strength-meter/

[2] http://www.amprobe.com/amprobe/auen/environmental-test/sound/amp-sm-10.htm?pid=73334

[3] http://www.testolimited.com/testo-905-t2-compact-surface-thermometer

connected (i.e. not supplied via the MG set) and it is therefore probable that this voltage increase was caused by external network events and not influenced by the SOP control. It can also be observed that when the SOP tripped unexpectedly a step change in voltage was observed on all inverters e.g. between 13:08 and 13:13. Please note: as previously stated the voltage is measured at the terminals of the SOP and is influenced by (1) the SOP injecting or exporting power and (2) the PNDC network. When the SOP trips unexpectedly and stops injecting or exporting power the voltage at the terminals of all of the SOP inverters returns to the PNDC network voltage.

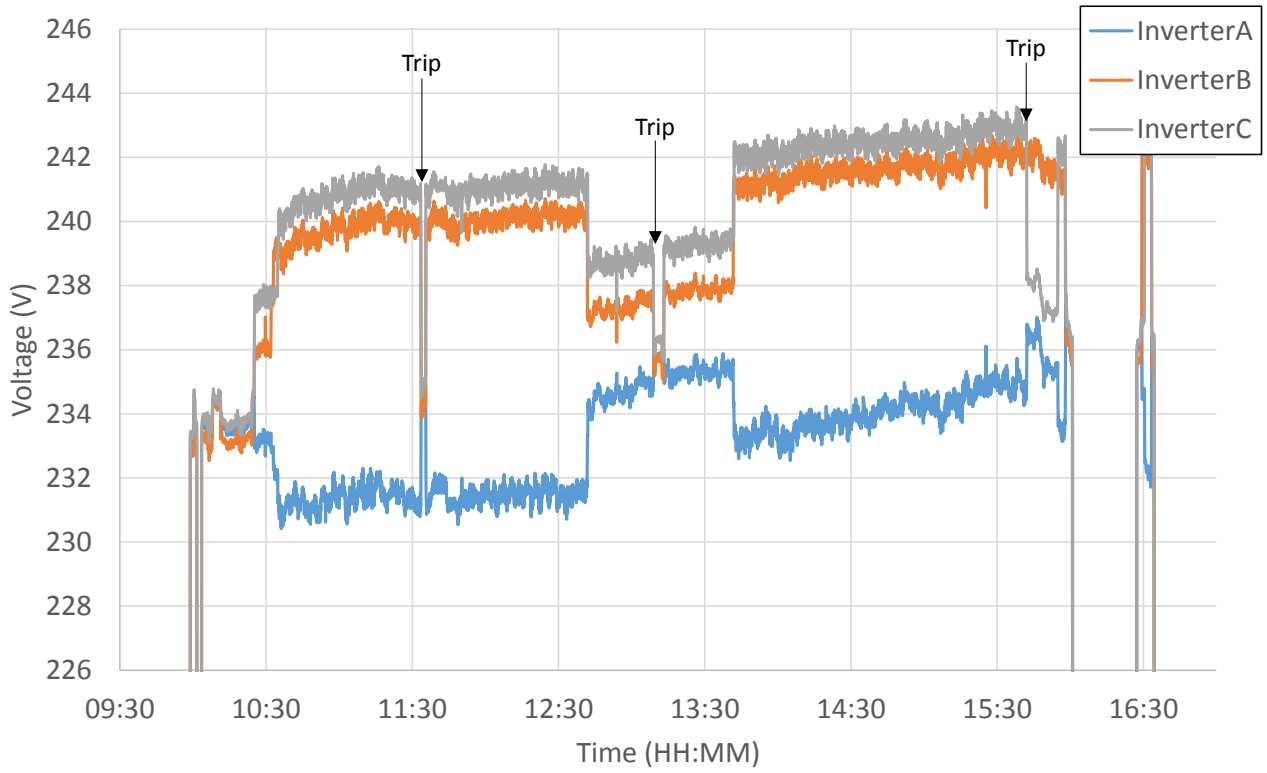


Figure 17: Phase A RMS voltage recorded at SOP terminals

The phase A RMS current recorded at each SOP inverter is shown in Figure 18. As in the voltage response the current is observed to change as the test progresses. It is probable that this was also caused by external network events changing the voltage of the network and hence the voltage at the terminals of the SOP. The SOP is controlled to inject constant active power, as the voltage of the network increases the SOP control reduces current injection to maintain constant power injection. In the third load step the current on all inverters is observed to decrease as the test progresses (13:45 onward). The unexpected SOP trip events are observed as periods of zero current injection in this graph.

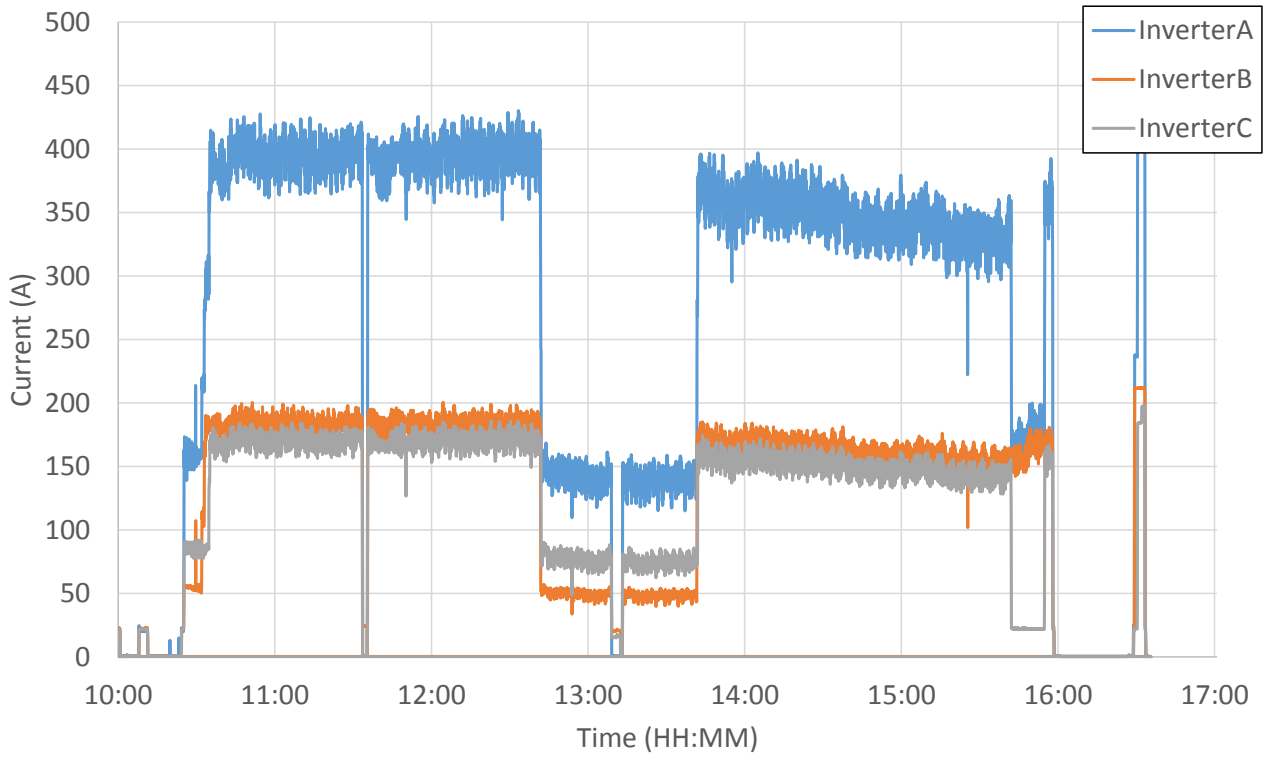


Figure 18: Phase A RMS current recorded at SOP terminals

The active and reactive power recorded at each SOP inverter is shown in Figure 19 and Figure 20. Both graphs follow the trend observed in the voltage and current graphs.

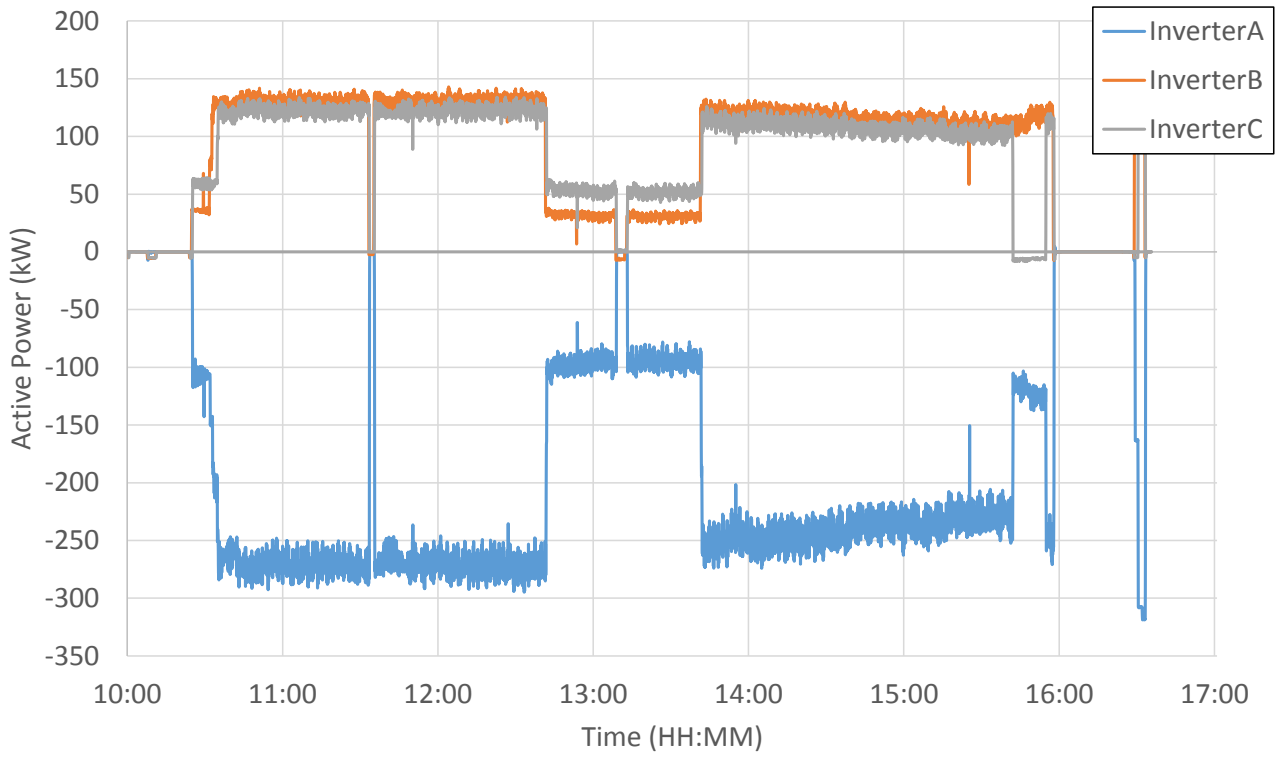


Figure 19: Three phase active power recorded at SOP terminals

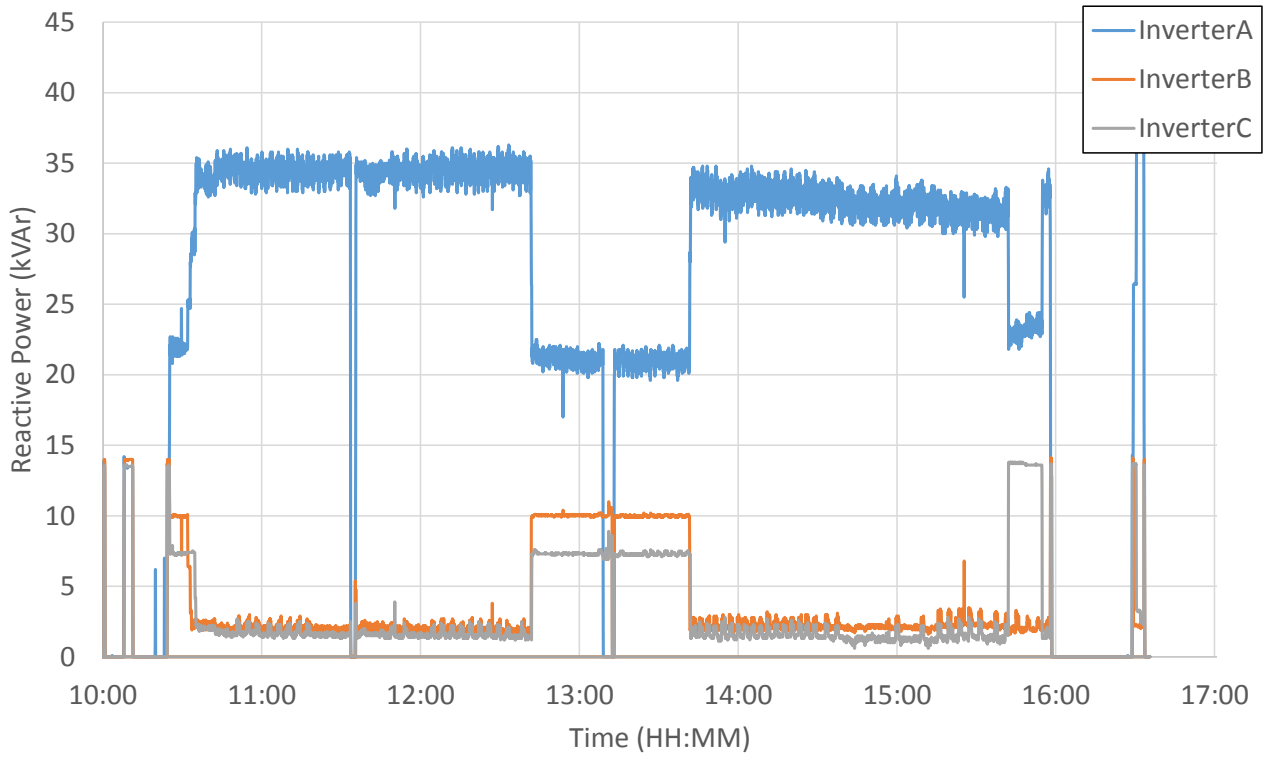


Figure 20: Three phase reactive power recorded at SOP terminals

The THDv% and THDi% recorded at each SOP inverter is shown in Figure 21 and Figure 22. By comparing Figure 20 and Figure 17 it can be observed that the periods of high THDv% correspond to periods when the PNDC network is de-energised e.g. from 16:00 to 16:30. By comparing Figure 22, Figure 17 and Figure 19 it can be observed that periods of high THDi% also correspond to periods when the network is de-energised (e.g. from 16:00 to 16:30) and also when the SOP is disabled via the HMI e.g. 13:11 to 13:13.

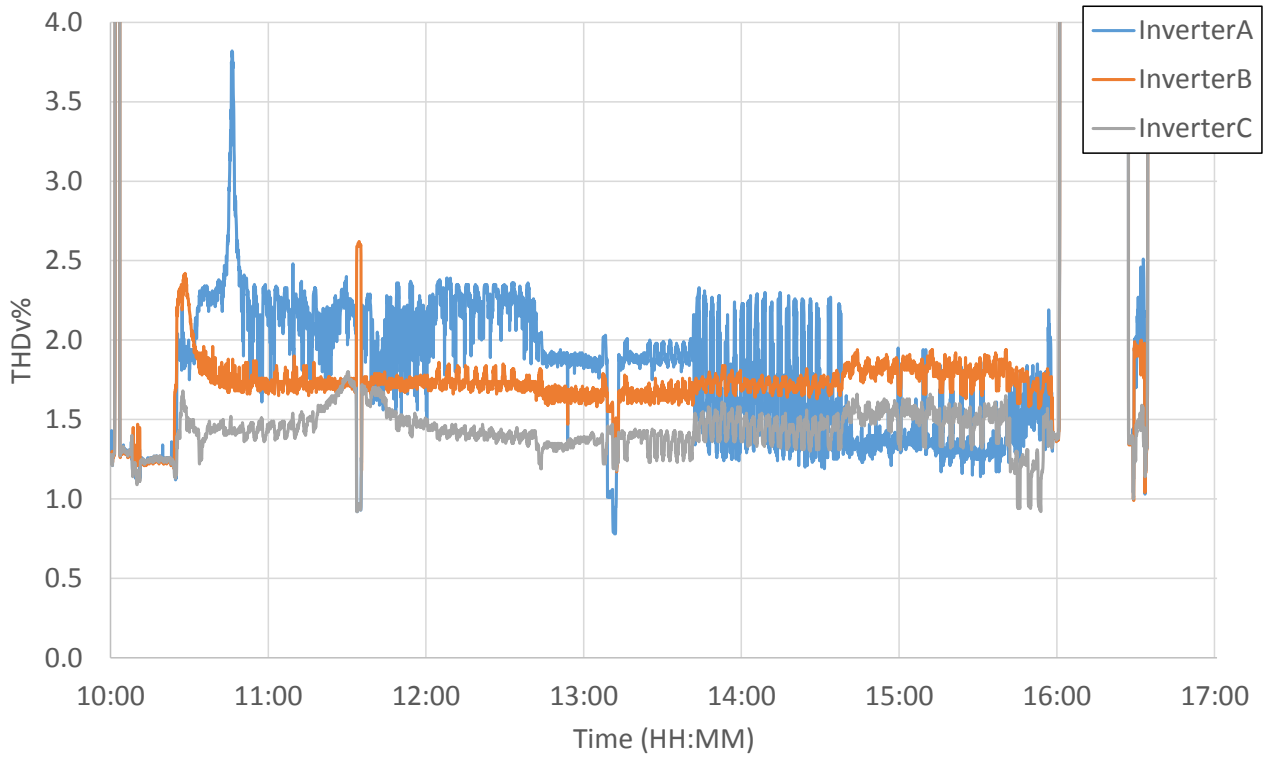


Figure 21: Phase A THDv% recorded at SOP terminals

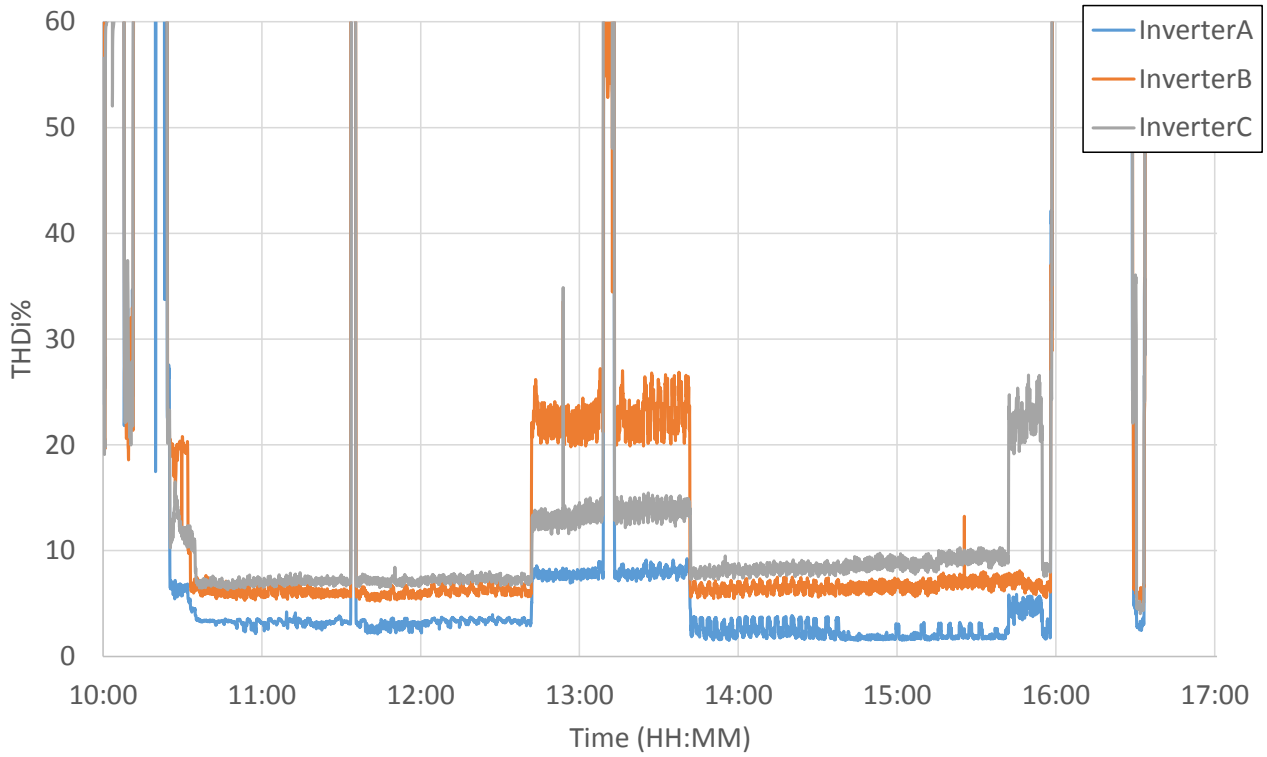


Figure 22: Phase A THDi% recorded at SOP terminals

As discussed in the method section, surface temperatures were recorded at 30min intervals at the locations shown in Figure 16. The recorded temperature data is shown in Figure 23. It can be observed that the highest average temperature is achieved at approximately 4 h 30 mins into the test and the highest temperature is

observed at location 4. The temperature at all locations continues to increase over the first 2 h period when the HMI inverters B and C are both set to export +170 kW. When the HMI setting of inverter B and C are decreased in the middle period (02:00-03:00) the temperature is observed to fall at all locations. When the power output is again increased (to 170 kW from inverter B and C) over the last 2 h period the temperature is again observed to increase. It can be surmised from this response that, as one would expect, the surface temperature of the SOP will increase in relation to the power output.

The specification provided by TPS states that the surface temperature of the SOP should not exceed +20 °C of ambient. The ambient temperature was in excess of 4 °C for the duration of the test therefore this limit was never exceeded. This is also true when the test is repeated in section 4.3.

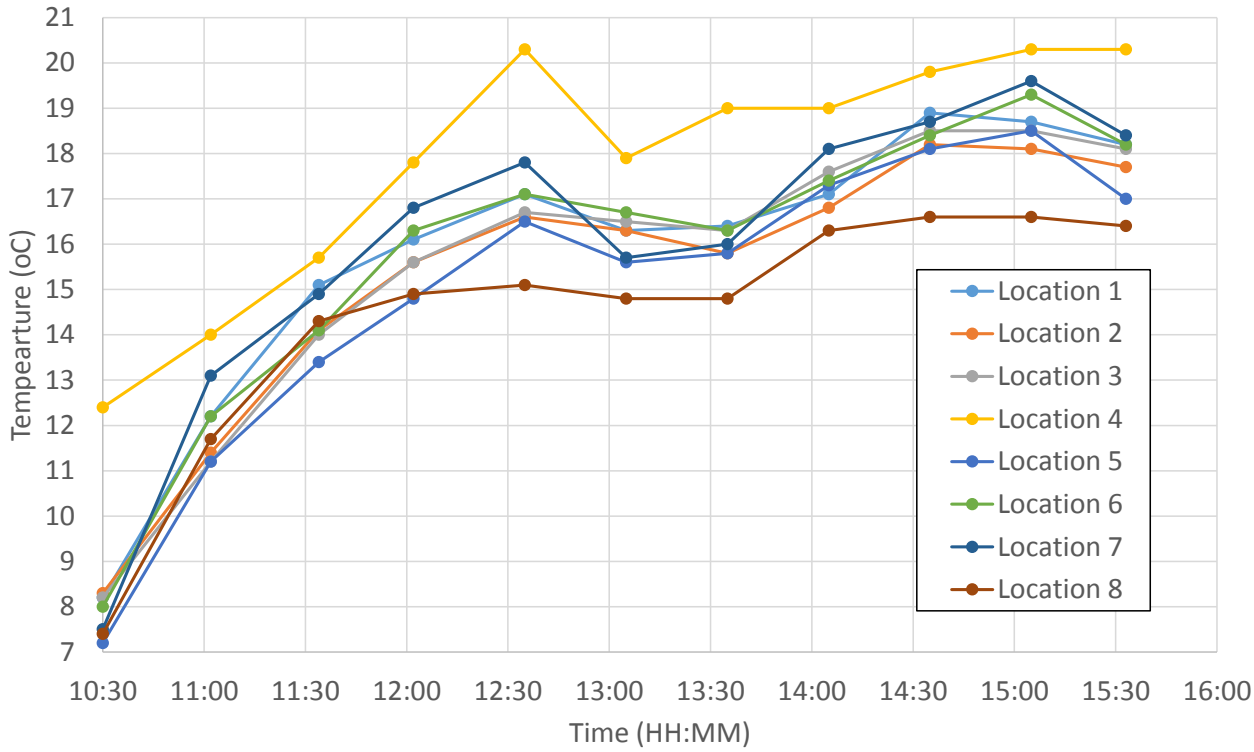


Figure 23: Temperature measurements on SOP surface

The audio noise measurements, recorded for HMI settings of Inverter B and inverter C set to export +170 kW, are shown in Figure 24. *"An 'A-weighting' is used to measure average noise levels and a 'C-weighting' to measure peak, impact or explosive noises"* [3]. The weighting is a scaling factor applied to the instrument recorded sound levels to account for the human ears perception of loudness as a function of frequency [4, 5]. By convention the A weighting is commonly used for evaluating the environmental and industrial impact of noise on hearing damage as it closely emulates the frequency sensitivity of the human ear. The C weighting is weighted more towards peak sound levels i.e. loud noise levels [4, 5].

It was noted that the SOP produced a high pitched audio noise during the test and an audio noise of a similar frequency could be observed at the substation transformers connected to the SOP: substation A (inverter C), substation D (inverter B) and substation I (inverter A). The frequency of the noise was not recorded, however, the A weighted and C weighted audio noise was recorded using the AMPROBE SM-10 Sound Level Meter as shown in Figure 24. The maximum audio levels were 73.6 dB(A) and 75.6 dB(C). This is less than the lower threshold limits at which preventive action must be taken as specified by the Control of Noise at Work Regulations 2005 [6], in this standard the limits are 80 db(A) and 135 db(A).

From Figure 24, it can be observed that in nearly all cases the C weighting is higher than the A weighting and the higher audio recordings are at positions 1-4 and 8. This is likely to be due to these positions being closer to the coolant system which generates noise via the integrated pump and fan. The AMPROBE SM-10 Sound

Level Meter user manual [7] indicates that a higher C rating than A rating is indicative of a large amount of low-frequency noise.

The audio noise measurements, recorded at HMI settings of inverter B set to export +170 kW and inverter C set to 0 kW, are shown in Figure 25. It can be observed that the ratio of noise between locations is similar to the response observed in Figure 24, however the noise level is less (at the lower power export settings) for nearly all locations. This suggests that, as one would expect, the noise level increases as the SOP is controlled to output more power.

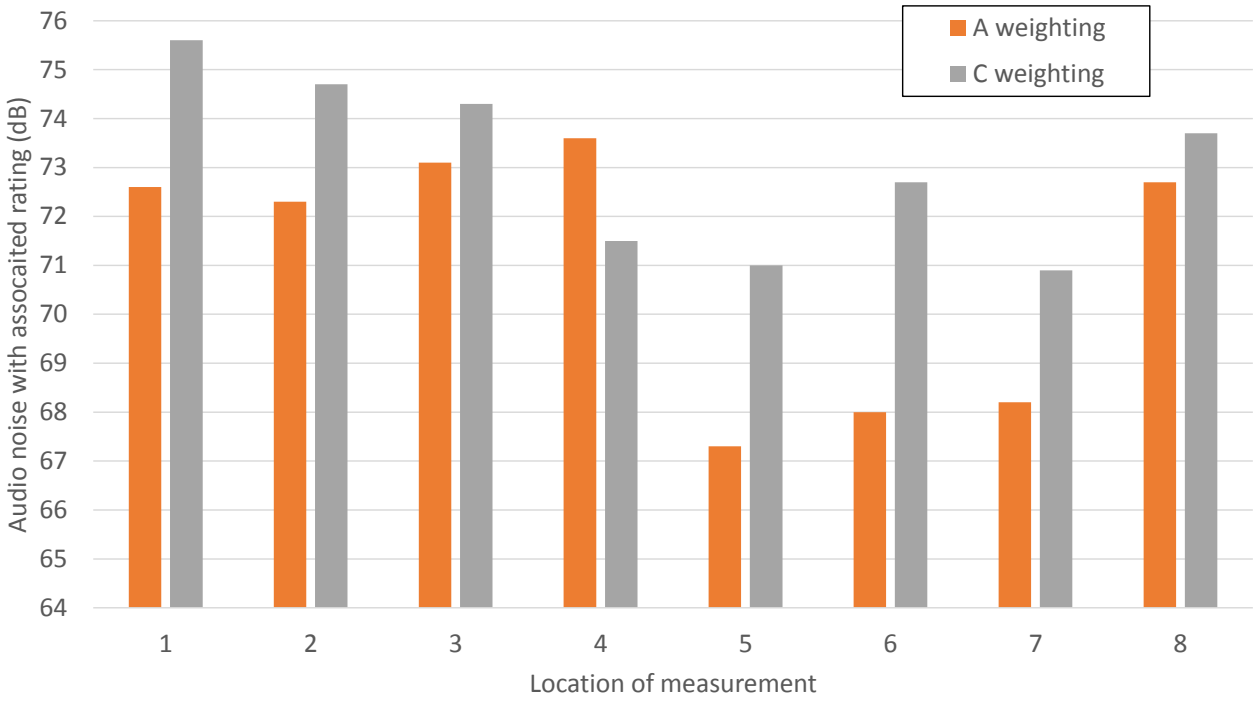


Figure 24: Noise measurement at HMI setting: inverter B and inverter C set to export +170 kW

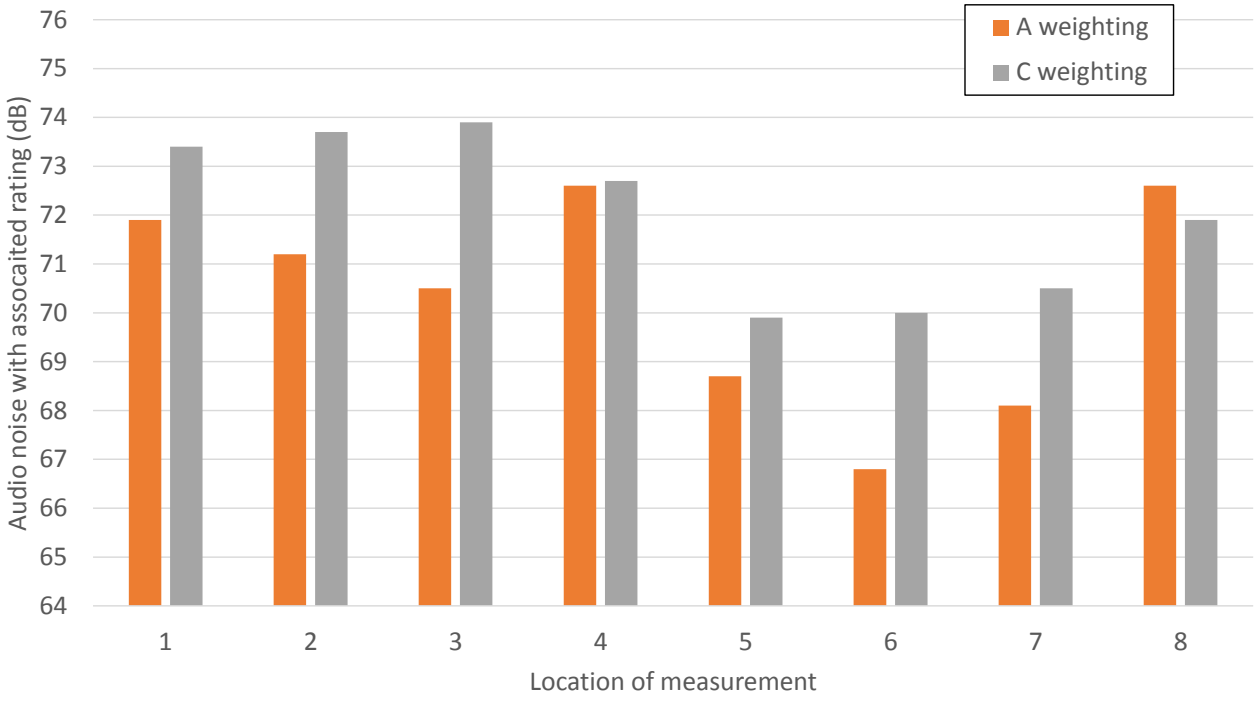


Figure 25: Noise measurement at HMI setting: inverter B set to export +170 kW and inverter C set to 0 kW

The EMF measurements recorded at (1) HMI setting of inverter B and inverter C set to export +170 kW (100 % loading) and (2) inverter B set to export +170 kW and inverter C set to 0 kW (50 % loading) are shown in Figure 26. It can be observed that in nearly all cases the EMF is higher at the higher power outputs, as would probably be expected. It can also be observed that the highest measurement was observed at location 4, the cause of this higher reading is unknown. The 1998 ICNIRP exposure guidelines [8] specify that the electric field should not exceed 9.0 kV/m. It can be observed that this electric field limit is not exceed for any location or power injection setting.

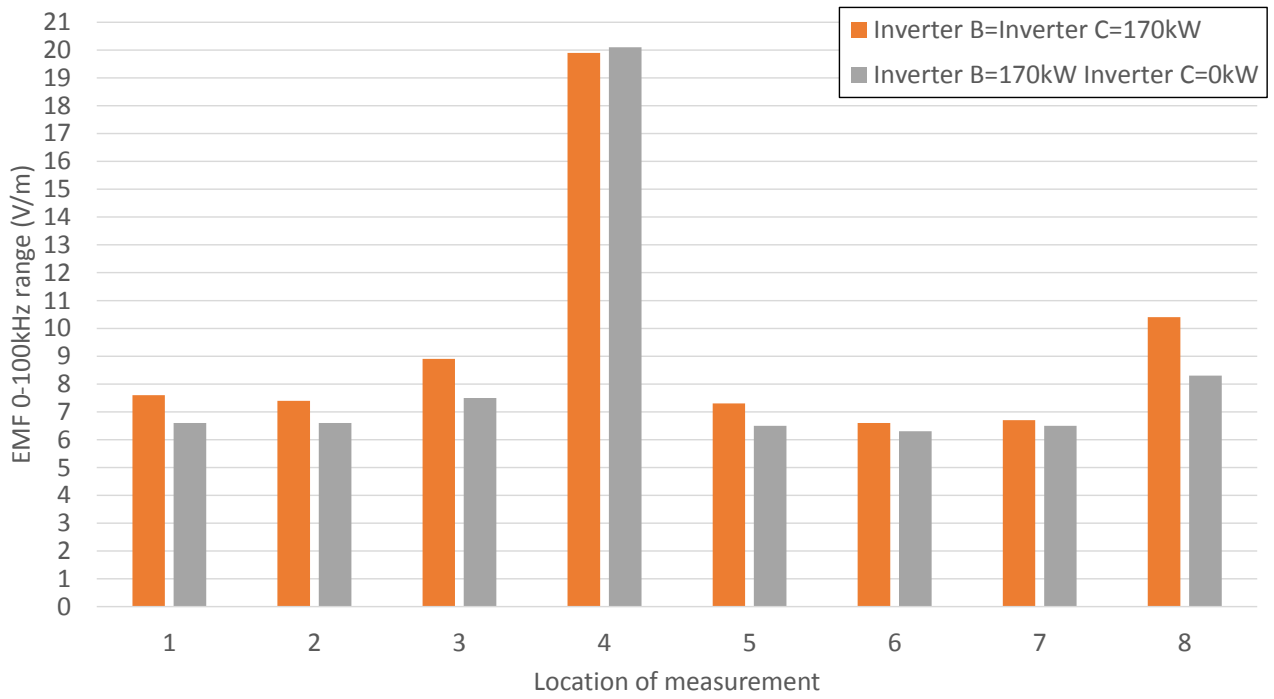


Figure 26: EMF measurements (0-100kHz range)

4.2.3 Conclusions

The test results confirm that, when controlled to do so, the SOP is capable of transferring three phase active power over a 5 h period. It should be noted that during this test oscillations were observed in the real and reactive power output from the SOP and the SOP tripped three times. The cause of these trip events is unknown, TPS have been consulted and have been unable to identify a cause for the trips. They have advised that they have resolved issues relating to the inverter IGBTs and MCCB closing circuitry maloperating since this test and these problems may have caused the uncontrolled trips.

The test results also show that the maximum temperature the SOP reached over this test period was 20.3 °C, this was recorded at location 2 at 2 h and 4.5-5 h into the test. The maximum audio noise was recorded as 75.6 dB(C) at maximum power output at location 1. The maximum EMF was recorded as 20.1 V/m at 50 % loading (inverter B export +170 kW and inverter C 0 kW), at location 4. The max temperature complies with UKPN's requirement that the SOP does not exceed +20 °C of ambient; the maximum audio noise (A and C weightings) comply with the Control of Noise at Work Regulations 2005 [6]; and the EMF measurements were found to comply with the electric field limits specified in the 1998 ICNIRP exposure guidelines [8].

4.3 Load cycle test 2

This test is a repeat of the previous load cycle test and the objective of this test is the same. The motivation for repeating the test is to evaluate the consistency of the SOP response when the SOP is controlled to inject the same current profile. After the software update by TPS (voltage output limit on the resonant controllers increased) a secondary objective of this test is to evaluate the change in response as a result of the update. Load cycle test 1 was completed on the 13th February 2015 and Load cycle test 2 was completed on the 16th of February 2015.

4.3.1 Log of test procedure

The method in this test follows the same procedure as in the previous load cycle test. However because of the software update the HMI settings were changed to export +148 kW on inverter B and C to achieve the desired 450 A current at inverter A. Assuming a voltage of 230 V (the voltage varies with SOP power injection), this equates to a loss of approximately 14 kW between the setting on the HMI and the expected current output. As previously mentioned, this loss is attributed to the power requirements of the SOP LCL filters and power electronics.

As in the previous test, the SOP tripped unexpectedly several times without external control to do so. A list of these trip events is included below (with action taken):

1. SOP trip 1 (2 h 14 min into the test). Remedial action – attempted to re-enable the SOP via the HMI interface but the SOP did not re-enable. On the HMI the following states were noted: inverter A '11' (indicates pre-charge), inverter B '20' (indicates waiting for connection) and inverter C '20' (indicates waiting for connection). The 11 kV network was de-energised and re-energised after 20 s and the SOP started operating again after it was manually re-enabled.
2. SOP trip 2 (3 h 32 min into the test). Remedial action – On the HMI it was noted that the 'heartbeat' counter was still incrementing indicating that communication was still operational. TPS diagnostics indicated the fault as DC link undervoltage. SOP was restarted by disabling and then re-enabling on the HMI.
3. SOP trip 3 (4 h 38 min into the test). Remedial action – SOP was restarted by disabling and then re-enabling on the HMI.
4. SOP trip 4 (4 h 45 min into the test). Remedial action – SOP was restarted by disabling and then re-enabling on the HMI.

4.3.2 Results and Analysis

The power quality, temperature, audio and EMF test data is graphed below. There were several changes observed in the response when compared with the previous load cycle test (load cycle test 1), these changes are listed below:

1. The oscillation in the voltage waveform was still observed but the rate of change in the oscillation was reduced. This is likely to be as a result of the software update that was applied at the end of load cycle test 1 (voltage output limit increased on the resonant controllers).
2. The oscillation in current, active power and reactive power waveforms were also reduced to a negligible level. This is also likely to be as a result of the software update (voltage output limit increased on the resonant controllers).
3. The average magnitude of the THDv% and THDi% are similar for both tests but the oscillation in magnitude was reduced in test 2.
4. The maximum temperature was approximately 1 °C higher in test 2 and it occurred 30 mins earlier in the test. The disparity between the tests is likely to be influenced by the erratic nature of the SOP unexpected trip events and also by the ambient temperature of the test environment. As in the previous test the max temperature complies with UKPN's requirement that the SOP does not exceed +20 °C of ambient.
5. The audio noise measurements are similar for both tests. Any small disparity between the tests is likely to be caused by (1) variations in ambient noise and (2) measurement error. As in load cycle test

1 the audio noise is less than the lower threshold limits at which preventive action must be taken as specified by the Control of Noise at Work Regulations 2005 [6], in this standard the limits are 80 db(A) and 135 db(A).

6. The trend of EMF measurement with regards to measurement location is consistent between both tests. However, it can be observed that the difference between the maximum and minimum values is larger when the HMI is set to Inverter B export +170 kW and inverter C set to 0 kW. The cause of this disparity is unknown but may be influenced by ambient EMF generated by other test equipment (the test area was not shielded from outside interference). As in the previous test the EMF measurements were found to comply with the electric field limits specified in the 1998 ICNIRP exposure guidelines [8]

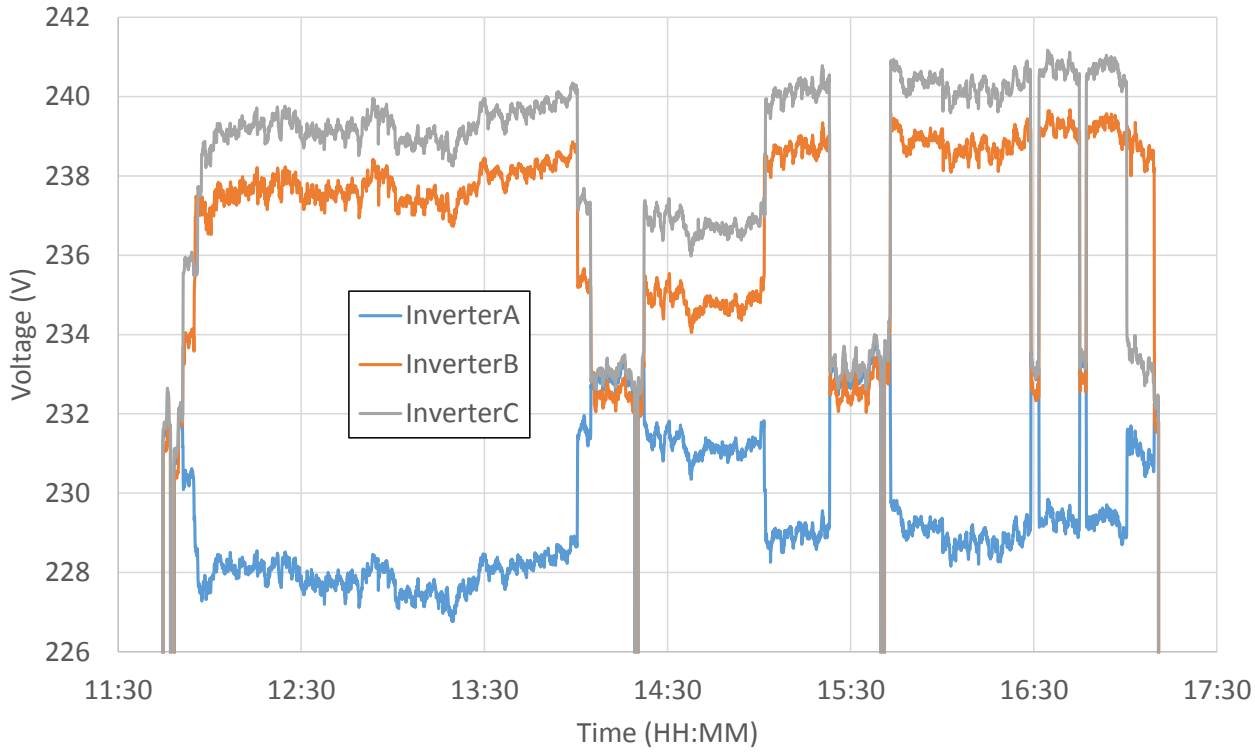


Figure 27: Phase A RMS voltage recorded at SOP terminals

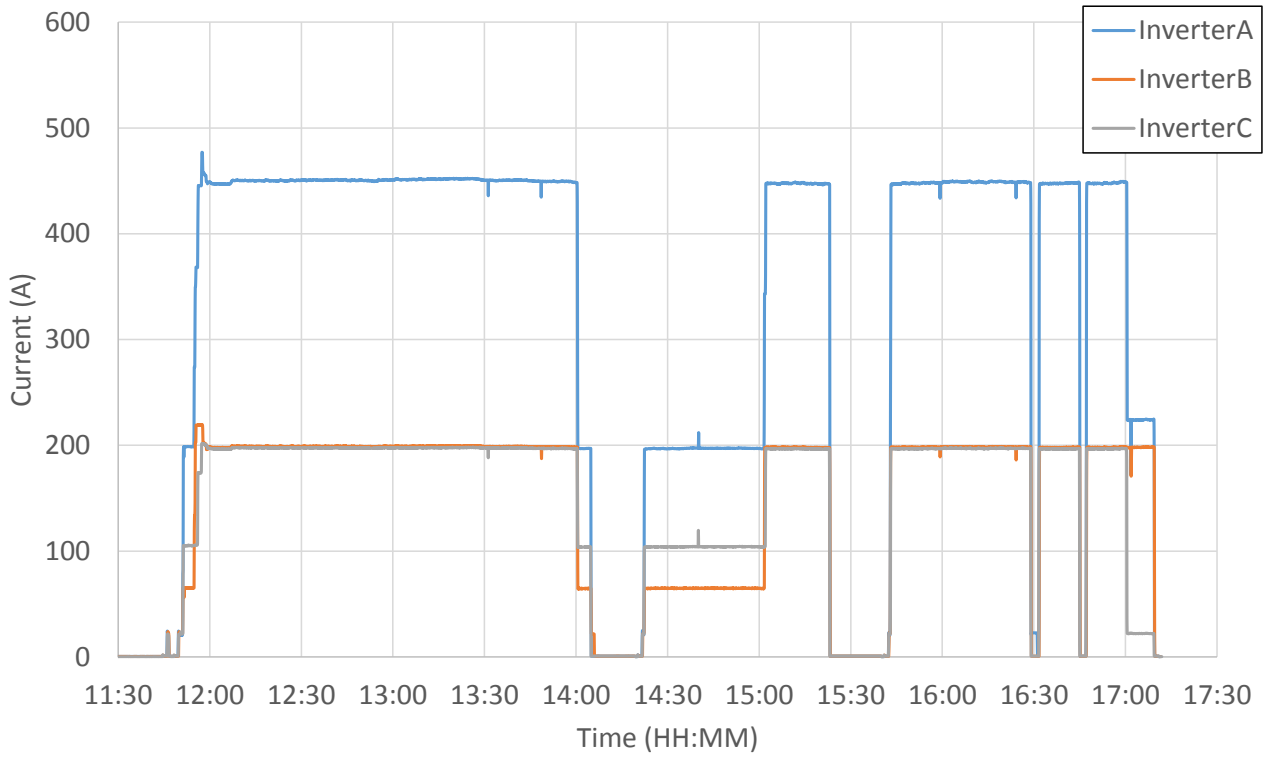


Figure 28: Phase A RMS current recorded at SOP terminals

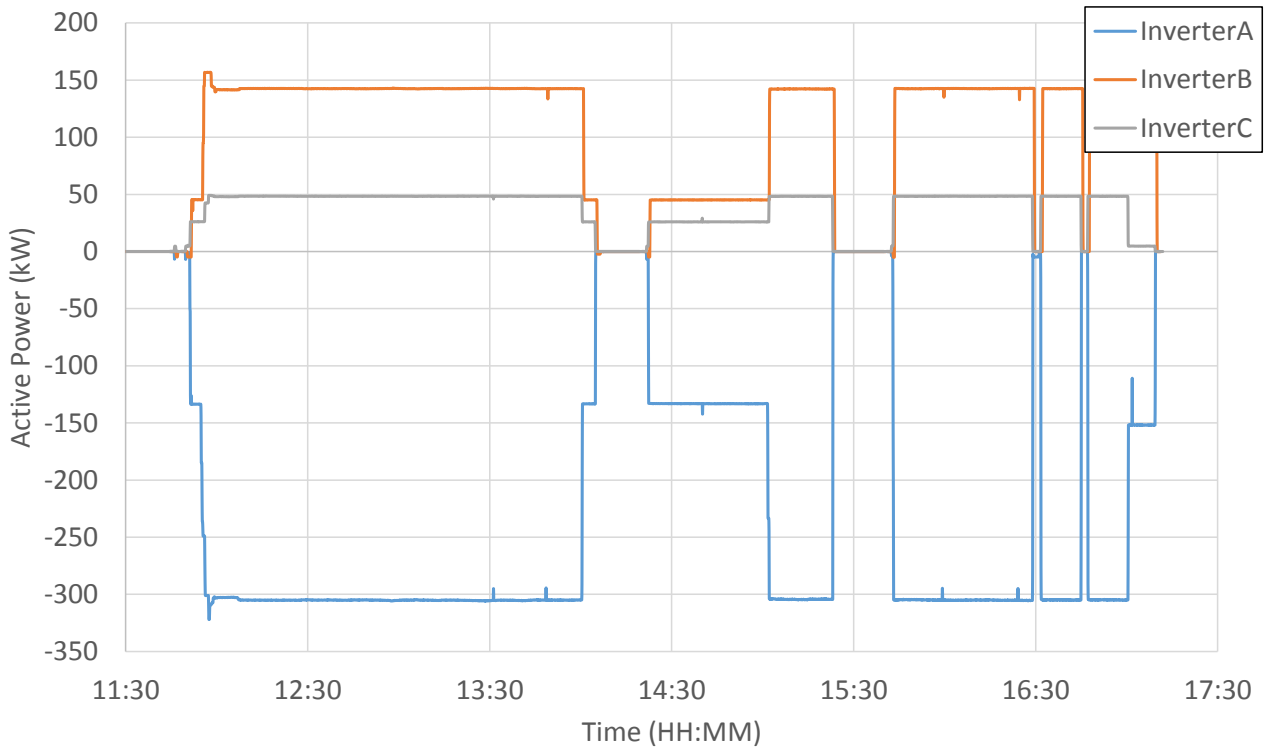


Figure 29: Three phase active power recorded at SOP terminals

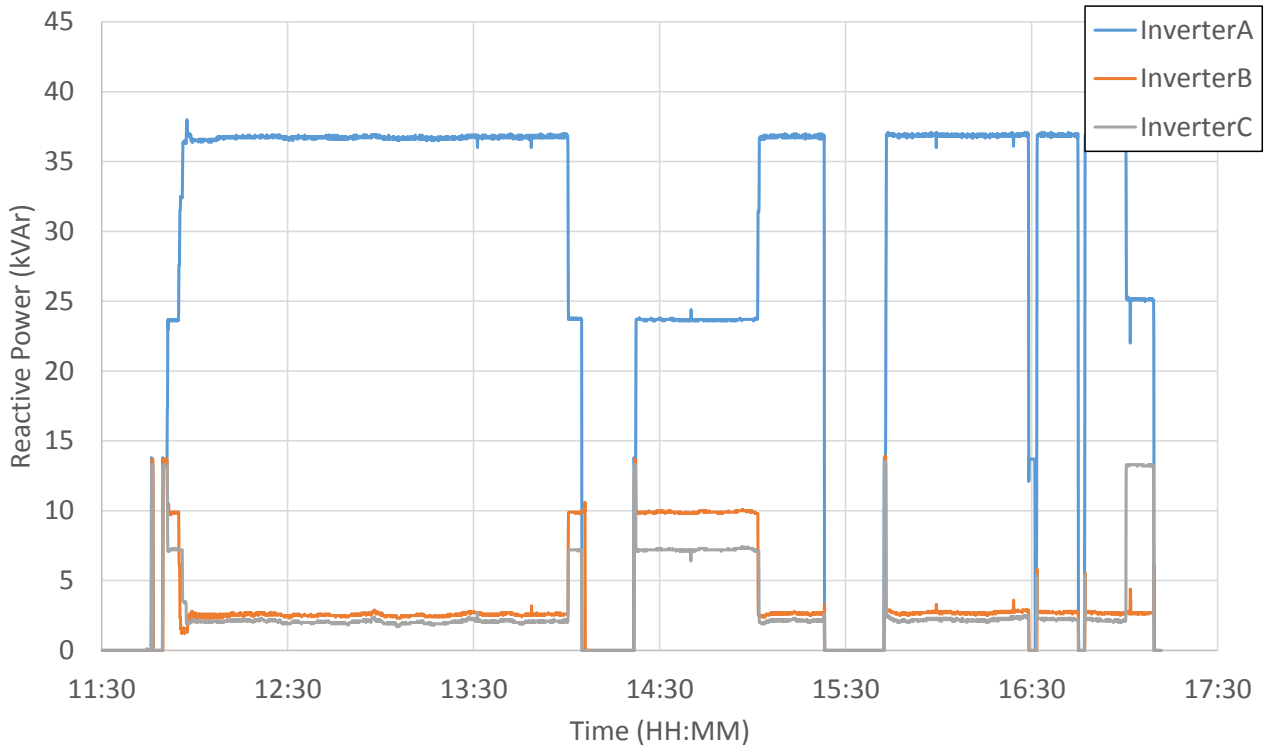


Figure 30: Three phase reactive power recorded at SOP terminals

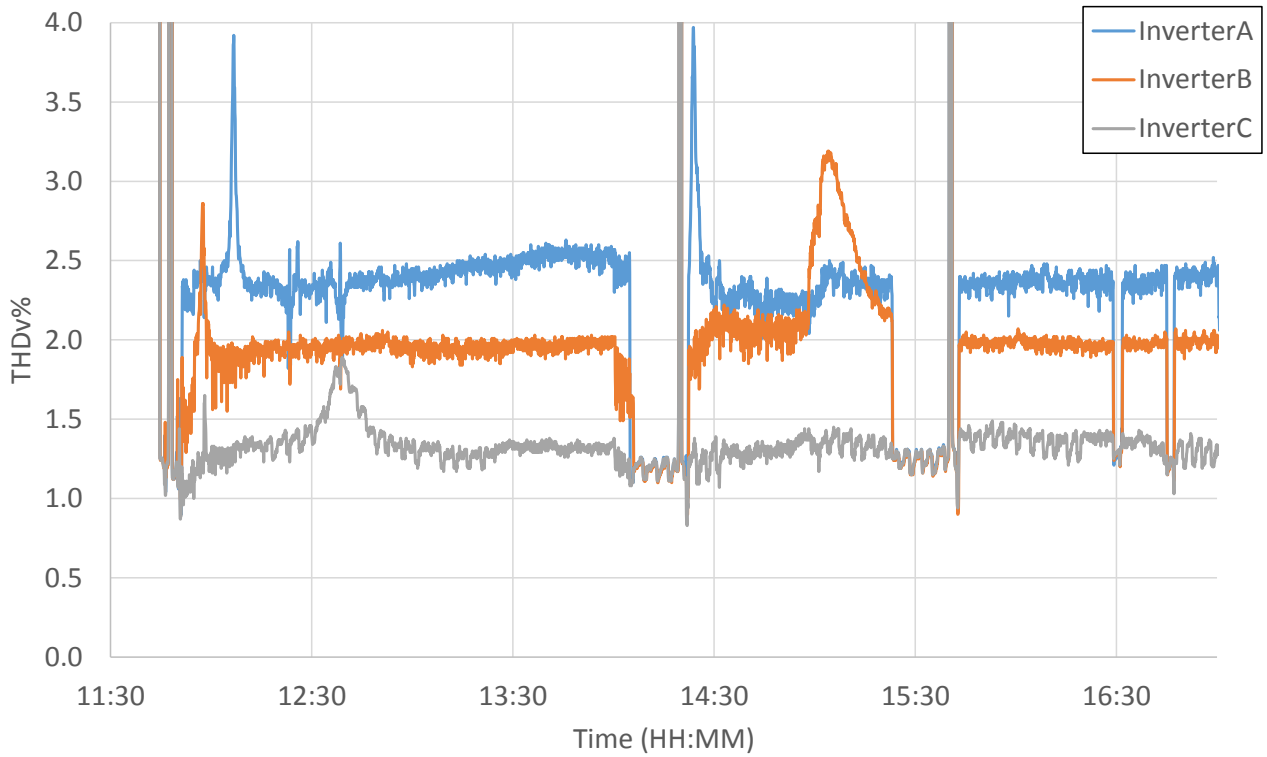


Figure 31: Phase A THDv% recorded at SOP terminals

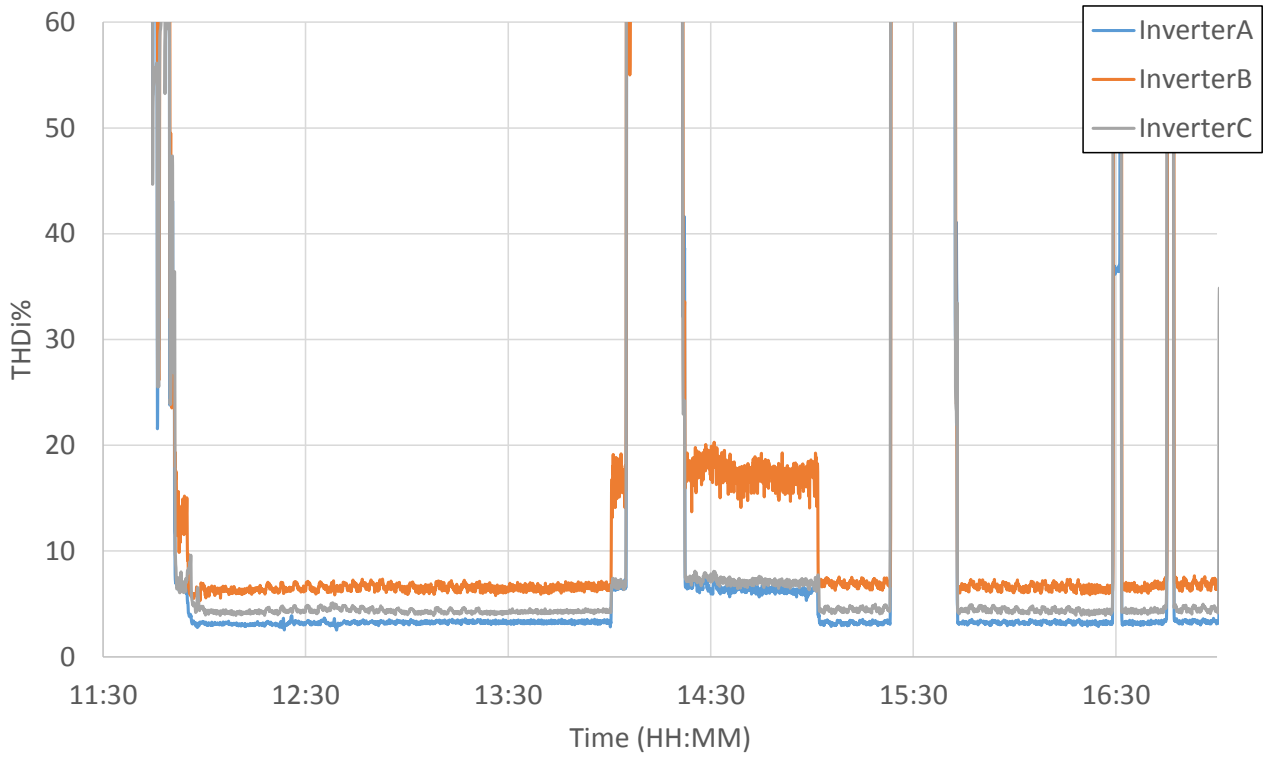


Figure 32: Phase A THDi% recorded at SOP terminals

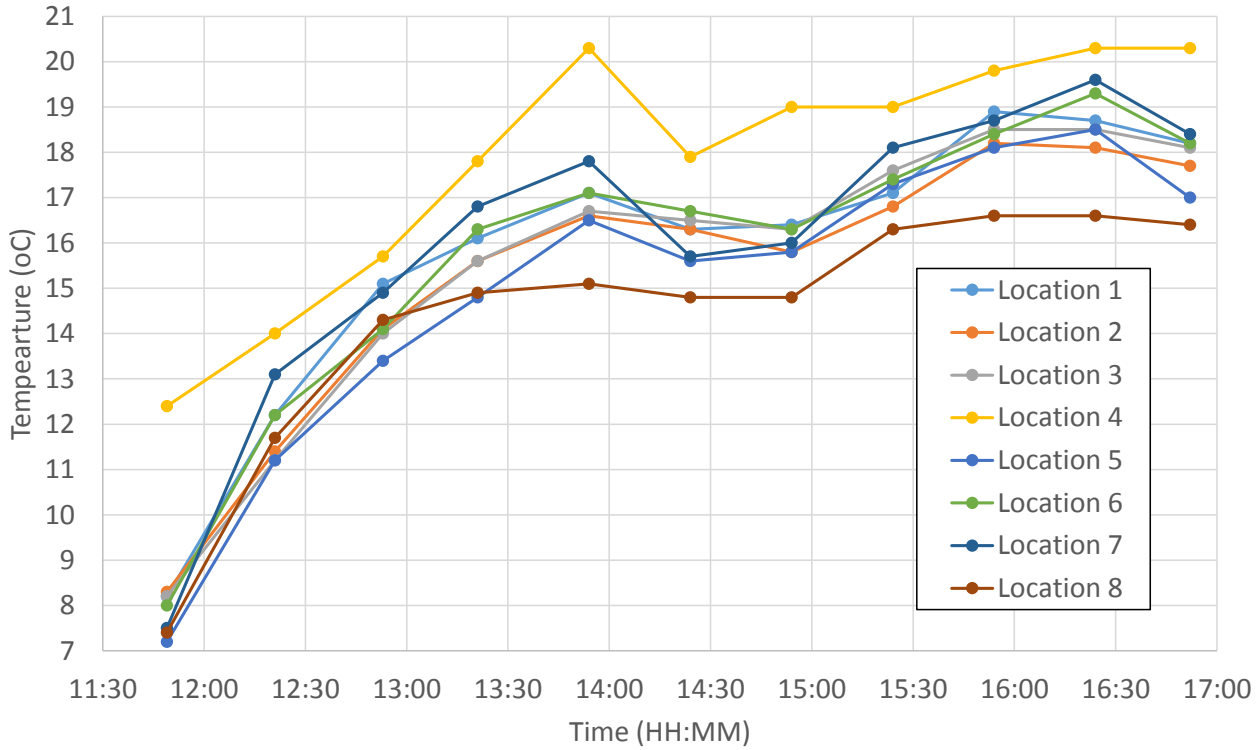


Figure 33: Temperature measurements on SOP surface

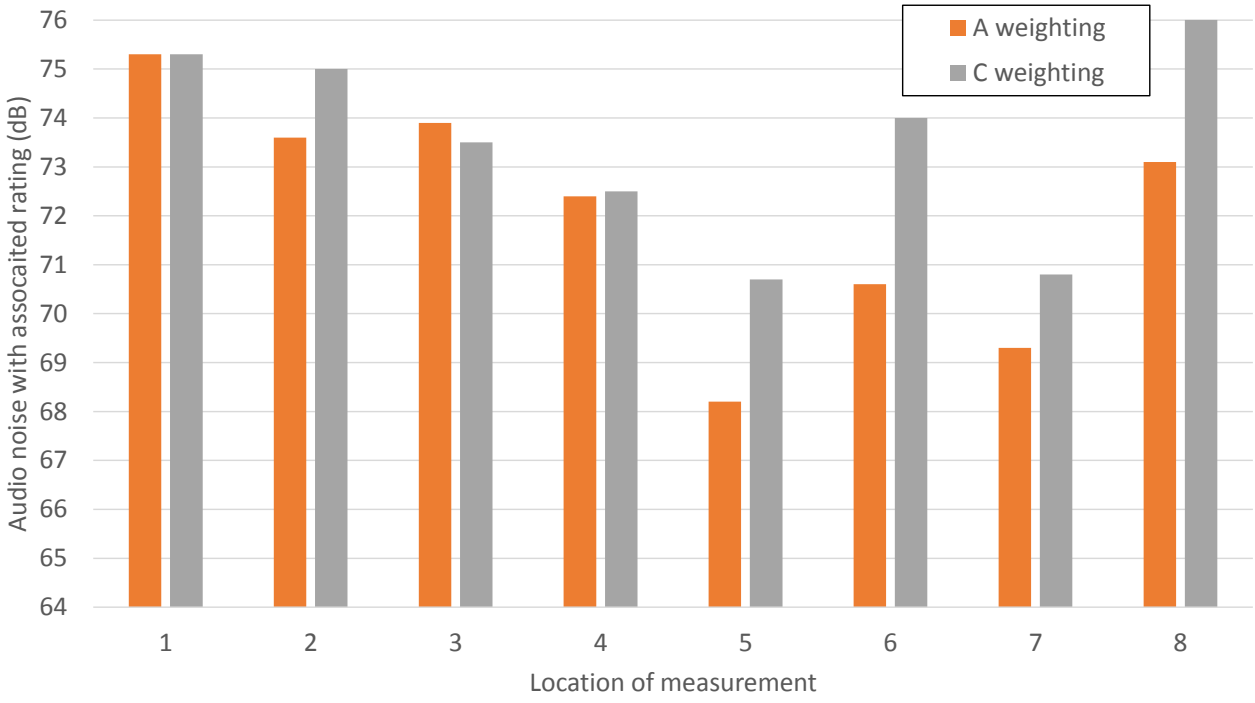


Figure 34: Noise measurements (A and C weightings) at HMI setting Inverter B = inverter C = 170 kW

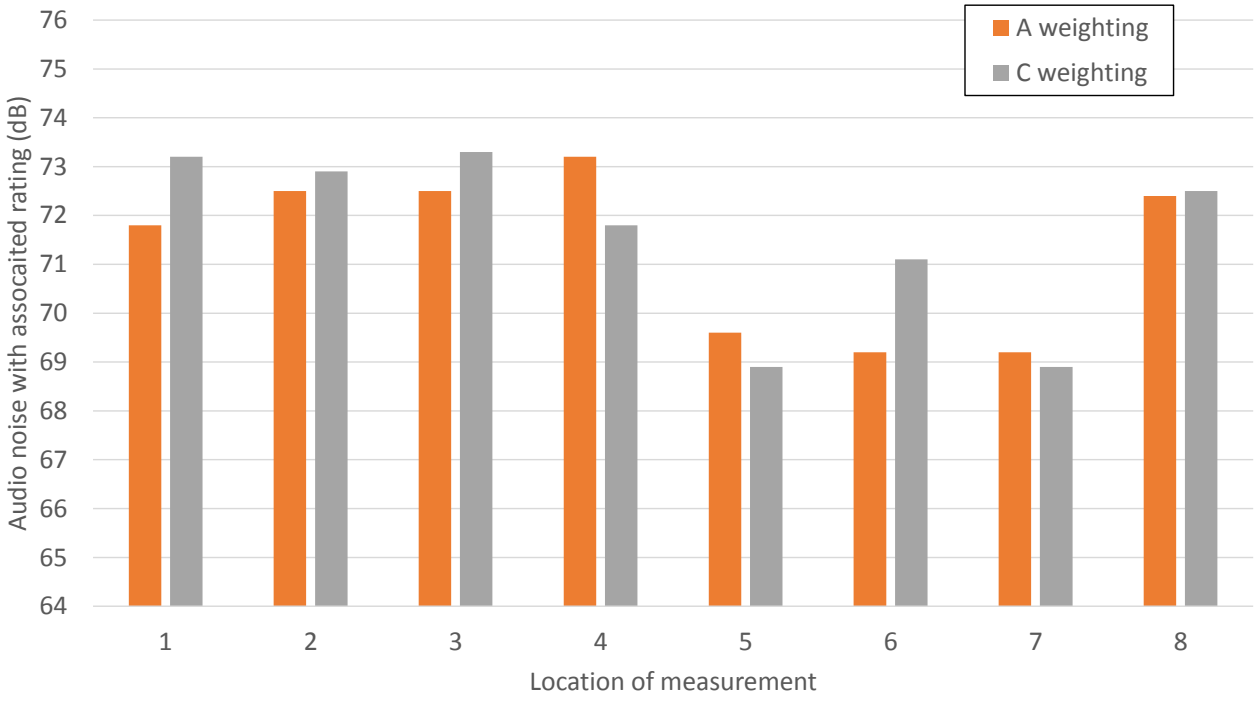


Figure 35: Noise measurements (A and C weighting) at HMI setting Inverter B = 170 kW and inverter C = 0 kW

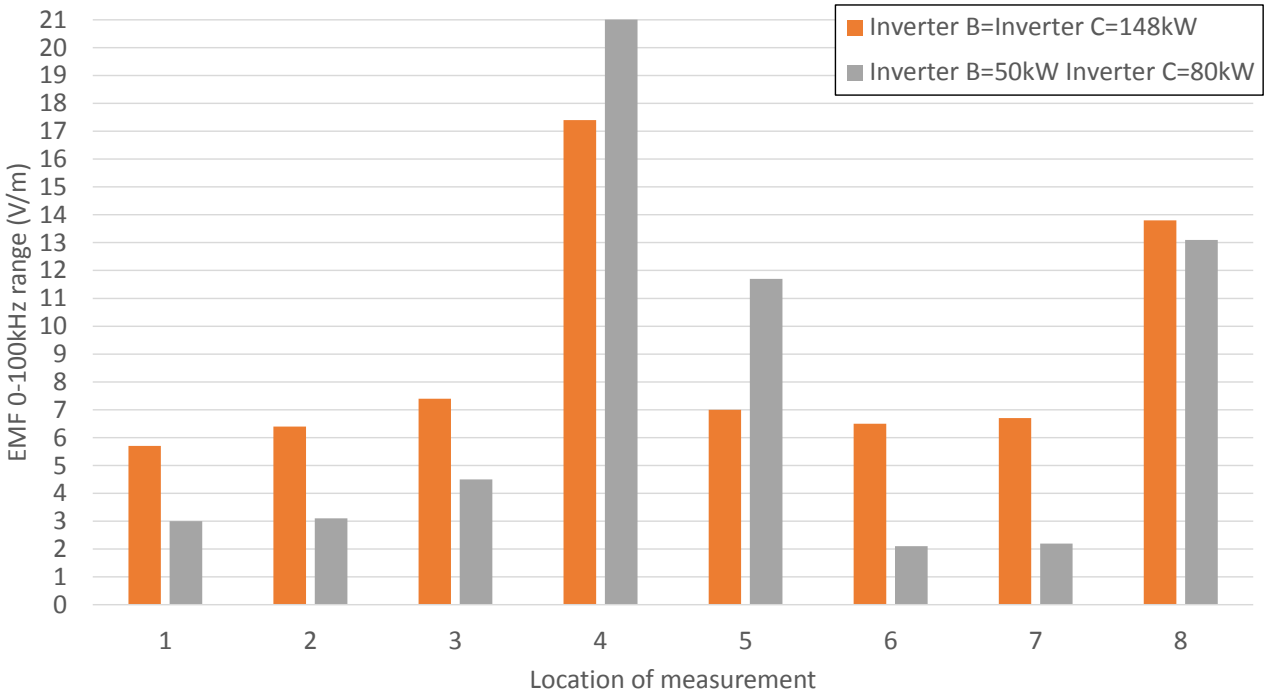


Figure 36: EMF measurements (0-100kHz range)

4.3.3 Conclusions

This test was a repeat of the previous load cycle test and the objective of the test was the same. The motivation for repeating the test was to evaluate the consistency of the SOP response when the SOP was controlled to inject the same current profile. After the software update by TPS (voltage output limit on the resonant controllers increased) a secondary objective of this test was to evaluate any changes in response as a result of the update.

The test results confirm that the software update implemented at the end of load cycle test 1 removed the power oscillations observed in the previous load cycle test. The update also removed the offset between the power settings on the HMI and the measured power values.

The trends observed in the temperature, audio and EMF recordings were observed to remain consistent with minor disparities being attributed to:

- The SOP unexpected trips
- Changes in the ambient temperature of the test environment
- Variations in ambient noise
- Ambient EMF generated by other test equipment

As in the previous load cycle test, the SOP was observed to trip unexpectedly during this test. As with the previous test the cause of these trip events is unknown, TPS have been consulted and have been unable to identify a cause for the trips but advise they have resolved issues relating to the inverter IGBTs and MCCB closing circuitry maloperating since this test and these problems may have caused the uncontrolled trips.

Also as in the previous test the max temperature was noted to comply with UKPN's requirement that the SOP does not exceed +20°C of ambient; the maximum audio noise (A and C weightings) comply with the Control of Noise at Work Regulations 2005 [6]; and the EMF measurements were found to comply with the electric field limits specified in the 1998 ICNIRP exposure guidelines [8].

4.4 Three phase reactive power support test

The objective of this test was to record the operation of the SOP when it was controlled to inject three phase reactive power from inverter C. This test evaluated the capability of the SOP to inject three phase reactive up to +50 kVAr and -50 kVAr while exporting +80 kW from inverter B and +126 from inverter C. The desired behaviour from the SOP in this test is to inject reactive power as controlled to do so via the HMI. The testing plan is specified in [2] and the log from the test is listed in the following section.

4.4.1 Log of test procedure

The list below describes the procedure followed during testing (as specified in the testing plan [2]). Please note that the DNP3 communication module was not operational at the time of this test and was disconnected by TPS prior to this test commencing.

1. The SOP was enabled (see introduction of section 3 for explanation).
2. Prior to starting the test it was observed that the active power output from the SOP was oscillating, as shown in Figure 37. From 12:52 to 13:02 the SOP HMI was set to: inverter B export +50 kW and inverter C set to 0 kW. From 13:03 to 13:05 the SOP HMI was set to: inverter B set to 0 kW and inverter C export +50 kW. The settings were varied in this manner to attempt to diagnose if the oscillations could be attributed to a specific inverter. In an attempt to reduce the SOP oscillation the network voltage was reduced from 250 V to 235 V (at 12:56) by changing the tap position on the PNDC 11 kV/11 kV isolation transformer. Prior to 12:56 the power output from the SOP has a large oscillation and post 12:56 the oscillation is reduced and the SOP output power is observed to increase. From this graph it can be concluded that at higher voltages the SOP power output will oscillate. TPS advised that this oscillation issue is related to the SOP DC link threshold and can be resolved by increasing the 'allowed' threshold of the DC link in the SOP control software.

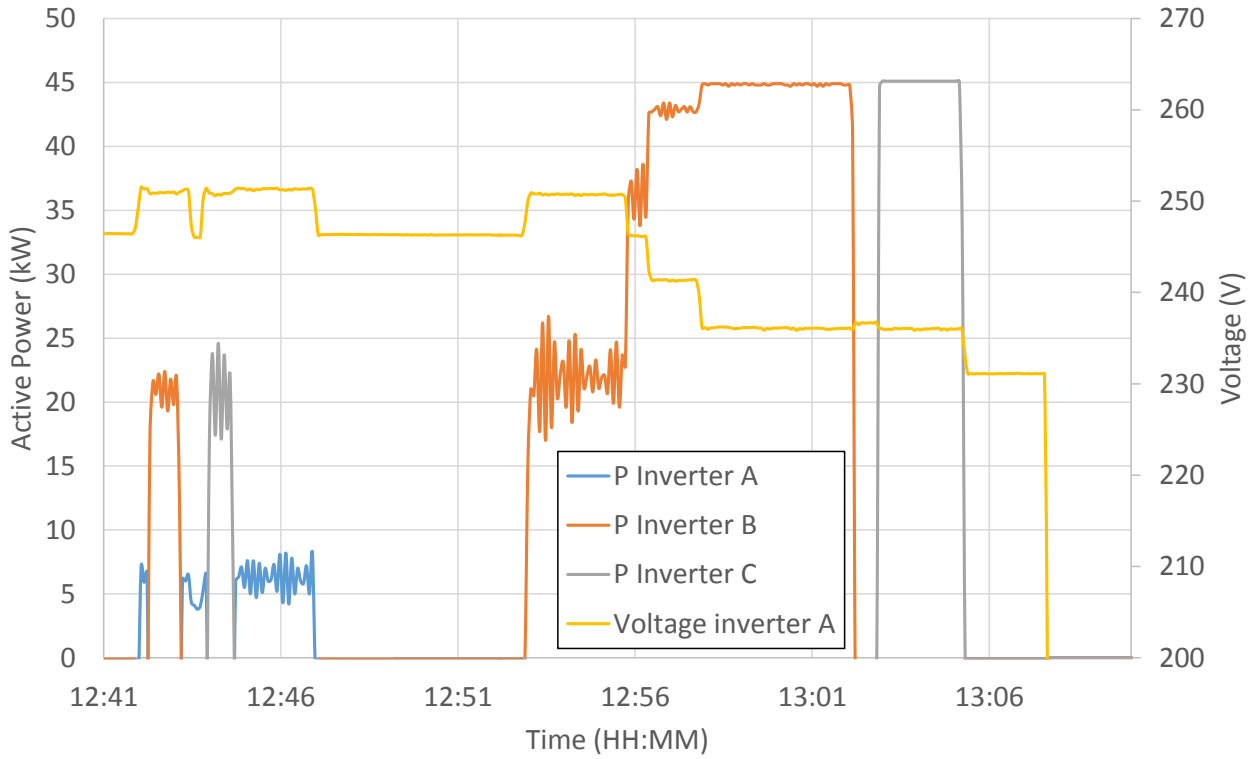


Figure 37: Pre-reactive power test: Total three phase active power output from SOP

3. After the voltage was reduced the test was started. The SOP response can be seen in Figure 38, Figure 39 and Figure 40.
4. The SOP HMI was set to:

a. Inverter B export +80 kW.
b. Inverter C export +126 kW.

5. From 14:19 using the SOP HMI the reactive setting of inverter C was increased up to export +50 kVAr in steps of 10 kVar. The final setting of inverter C was: +126 kW and 50 kVAr.
6. At 14:32 using the SOP HMI the reactive setting of inverter C was set to export +126 kW and 0 kVAr
7. At 14:33 using the SOP HMI the reactive setting of inverter C was set to export +126 kW and +50 kVAr.
8. At 14:34 using the SOP HMI the reactive setting of inverter C was set to export +126 kW and 0 kVAr and then the SOP was manually disabled.
9. At 14:37 the SOP was manually re-enabled.
10. From 14:39 using the SOP HMI the reactive setting of inverter C was increased up to import -50 kVAr in steps of -10 kVar. The final setting of inverter C was 126 kW and -50 kVAr.

4.4.2 Results and Analysis

The power quality data from the test is graphed below. Figure 38 shows the total three phase active power output measured at the inverter terminals of the SOP. During the test the SOP was controlled via the HMI to inject a constant three phase active power output of +80 kW from inverter B and +126 kW from inverter C. From Figure 38 it can be observed that the active power output does not remain constant as the reactive power output is changed. It can also be observed that the active power transfer on inverter C and inverter A began oscillating with increasing magnitude when the HMI setting is increased from step -30 kVAr up to -50 kVAr (14:40 to 14:50).

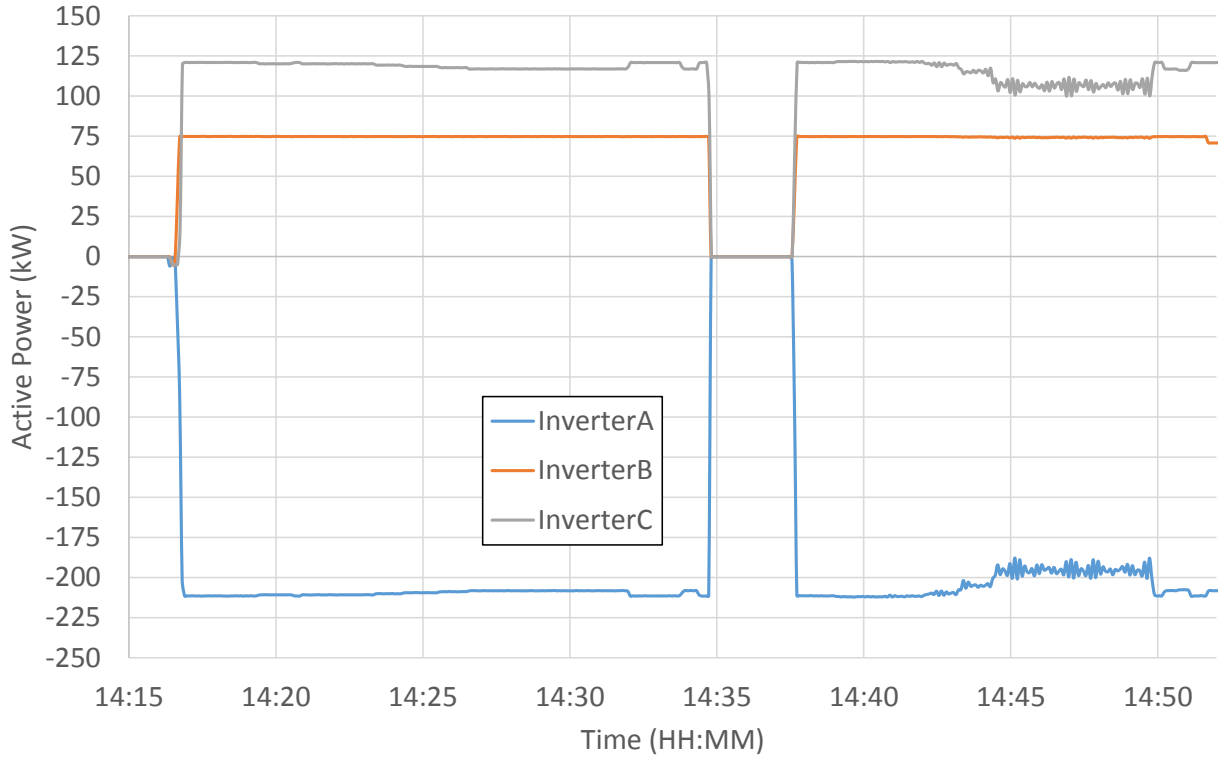


Figure 38: Total three phase active power SOP terminals

The reactive power steps described in the method section can be observed in Figure 39. It should be noted that the polarity indicated on the HMI appears to be wrong (i.e. reversed). This is indicated by two aspects of the recording:

1. The reactive power recording shown in Figure 39 is negative when the HMI is set to a positive value i.e. the HMI setting is increased from 0 to +50 kVAr from 14:19 to 14:27. The active power polarity for this same test is observed to be correct (as shown in Figure 38).

2. The voltage response (also shown in Figure 39) decreases as the HMI setting is increased from 0 to +50 kVAr (14:19 to 14:27). A voltage decrease should correspond to reactive power going into and not out of the SOP.

The same reversal of expected polarity is observed when the HMI setting is decreased from 0 to -50 kVAr from 14:38 to 14:45.

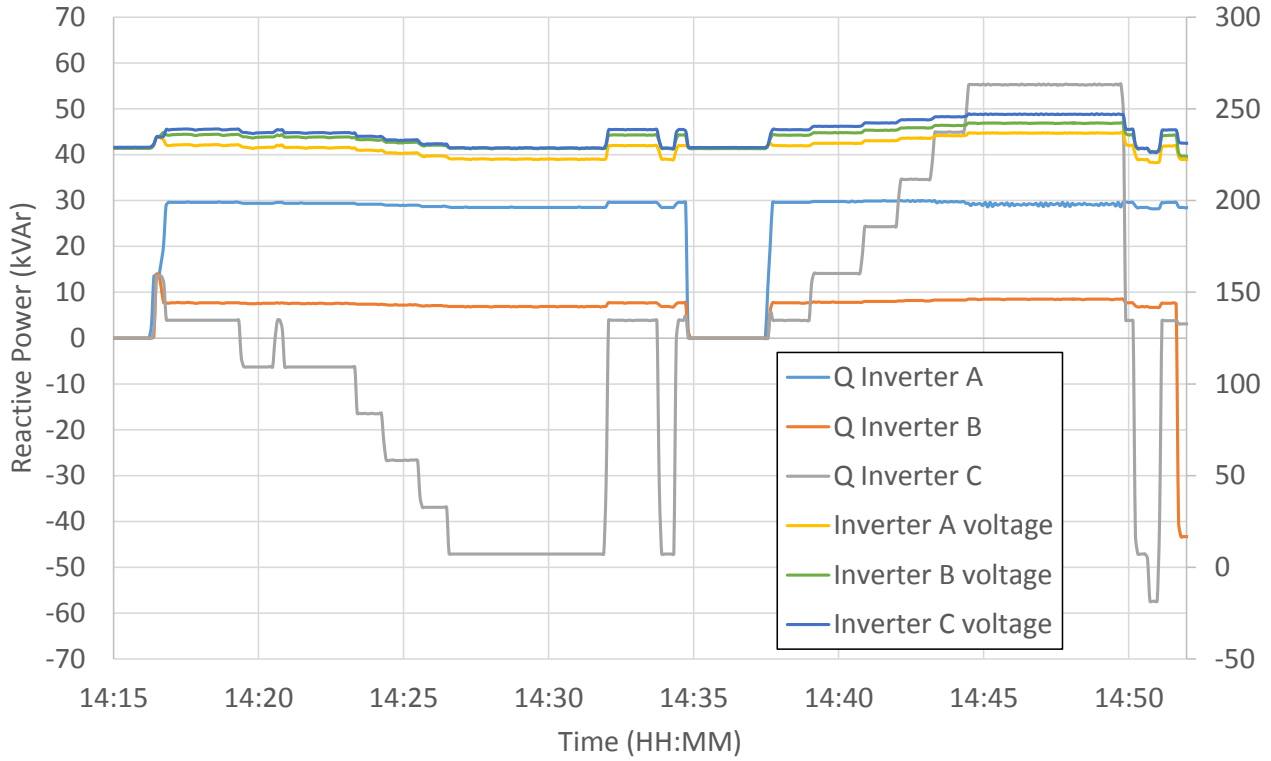


Figure 39: Total three phase reactive power SOP terminals

The phase A current transfer at the SOP inverters is shown in Figure 40. It can be observed that the current magnitude matches the trends observed in Figure 38.

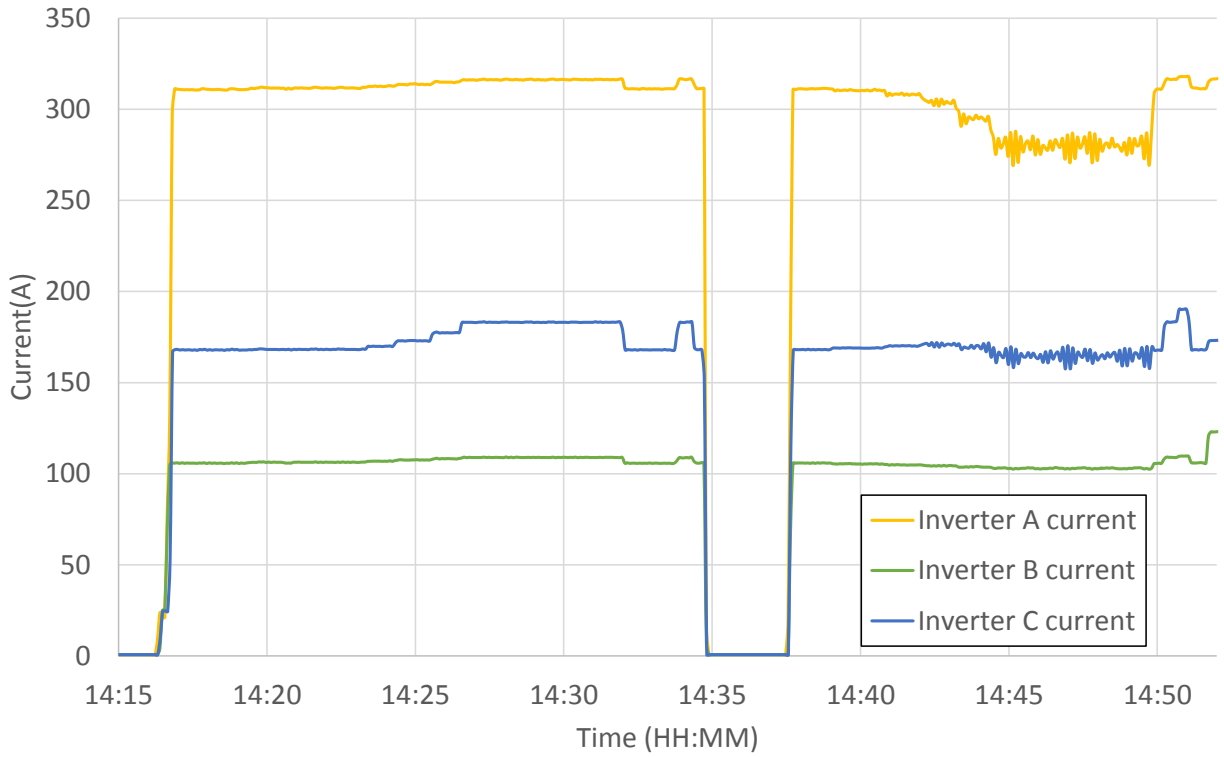


Figure 40: Phase A RMS current measured at SOP terminals

4.4.3 Conclusions

This test evaluated the capability of the SOP to export three phase reactive power. The test results confirm that the SOP is capable of exporting three phase reactive power up to +50 kVAr and -50 kVAr (while also exporting +126 kW) when controlled to do so via the HMI. However, the results recorded from this test have indicated two factors of note relating to the operation of the SOP:

1. At the HMI setting of inverter C +126 kW and -50 kVAr the SOP current output was observed to oscillate. The cause of this oscillation is related to the SOP DC link threshold and was resolved at a later stage in the test program by increasing the 'allowed' threshold of the DC link in the ICCs. It should be noted that the same oscillation was not observed at the other maximum reactive output setting (i.e. HMI setting +126 kW and +50 kVAr). Please note, due to the reversed polarity of the HMI interface at this HMI setting (i.e. HMI setting +126 kW and +50 kVAr) the SOP was importing reactive power.
2. When the SOP was initially controlled to inject active power the SOP was also observed to inject reactive power from all three inverters: inverter A exporting +30 kVAr, inverter B exporting +7.7 kVAr and inverter C exporting +3.9 kVAr. This offset influenced the control of the SOP by introducing an offset on all settings i.e. a setting of inverter C +50 kVAr equated to a response of -47.1 kVAr and a setting of inverter C -50 kVAr equated to a response of +55.4 kVAr.

4.5 Additional test: repeat of EMF and audio tests and measurements at increasing distances from SOP

This test is a repeat of the EMF and audio measurement test (completed earlier in this report) at increased distances from the SOP. The new distances were specified by TPS and the objective of this test is to gain an understanding of how the audio noise and EMF change at further distances from the surface of the SOP. A second objective of this test is to evaluate whether noise and EMF levels specified by TPS would be exceeded for the distances specified in this test. The desired behaviour from the SOP in this test is for the EMF and audio measurements to remain within the limits specified in relevant standards and requirements. The testing plan is specified in [2] and the log from the test is listed in the following section.

4.5.1 Log of test procedure

The measurement points for the additional EMF and audio measurement test are shown in Figure 41. It should be noted that due to the size of the test cell, the original testing plan specified measurements with a maximum distance of 10 cm from the surface of the SOP. It was agreed to repeat the measurements at further distances from the SOP with the understanding that obstacles and other equipment in the immediate vicinity of the test cell may influence the validity of the measurements.

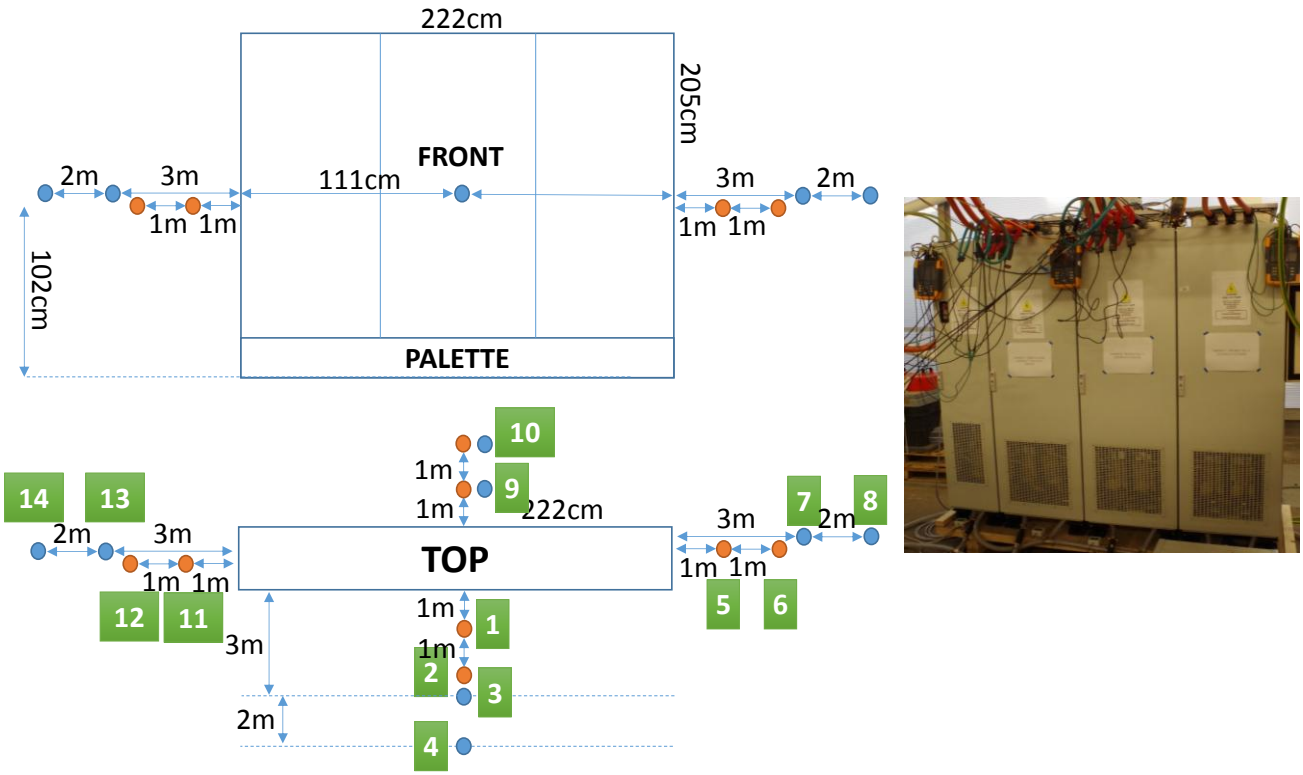


Figure 41: Audio noise and EMF measurement locations – additional test

The list below describes the procedure followed during testing (as specified in the testing plan [2])

1. The SOP was enabled (see introduction of section 3 for explanation).
2. The SOP HMI was set to (note the reactive component was not controlled during this test):
    a. Inverter B export +148 kW.
    b. Inverter C export +148 kW.
3. The EMF was measured at the locations indicated with the orange circles and noise levels were measured at the locations indicated with the blue circles shown in Figure 41. Using the built-in functionality of the sound probe, the following was measured: (1) Maximum sound level for A weighting over 30 s duration and (2) Maximum sound level for C weighting over 30 s duration. Using

the built in functionality of the EMF meter the EMF reading was measured over the 0 Hz to 100 kHz frequency range.

4. The SOP HMI was set to:
    a. Inverter B export +74 kW.
    b. Inverter C export +74 kW.
5. EMF and noise level measurements were repeated.

4.5.2 Results and Analysis

The audio noise measurements recorded for the HMI setting of inverter B and inverter C set to export +148 kW are shown in Figure 42. As with the previous test it can be observed that in all cases the C weighting is higher than the A weighting and the higher audio recordings are observed at the location closest to the coolant system (position 3 and 4). As expected the locations closer to the SOP have a higher associated noise level i.e. 3 is closer than 4, 7 is closer than 8 etc. It can be observed that with the increased distance in this test nearly all the audio measurements recorded in this test are less than those recorded previously. This observation is also true for the reduced power output test shown in Figure 43. The exception to this rule is location 3 where the C weighting is higher than the previous recordings. This may be due to the close proximity to the coolant system at this measurement location (with associated pump and fan noise).

The audio noise measurements recorded at the HMI setting of inverter B and inverter C set to export +74 kW are shown in Figure 43. It can be observed that the ratio of noise between locations is similar to the response observed in Figure 42 however the noise level is less for nearly all locations. This agrees with the previous conclusion that the noise level increases as the SOP is controlled to output more power (sections 4.2 and 4.3).

The noise specification provided by TPS states that the noise level should remain less than 56 dBA (A weighting) when measured five meters from the SOP. It can be observed that the noise measurements (A weighting) recorded in this test exceed this limit at all locations and for both power output levels.

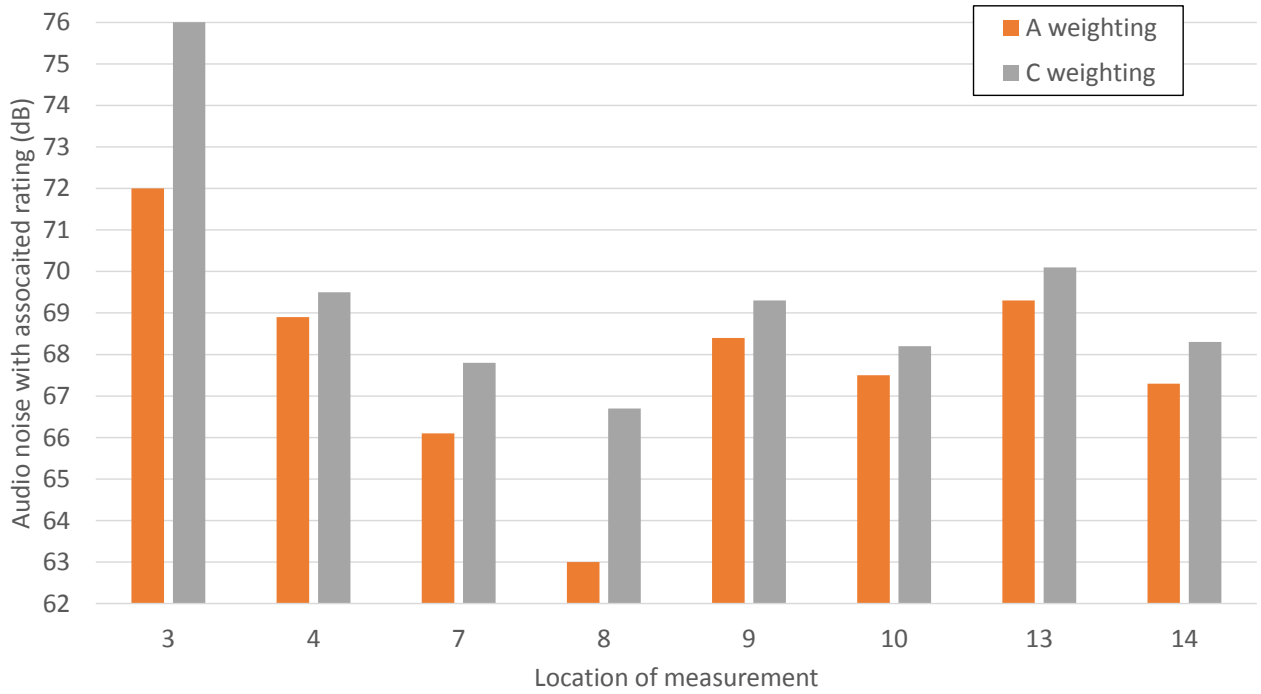


Figure 42: Noise measurement at HMI setting Inverter B and Inverter C export +148 kW

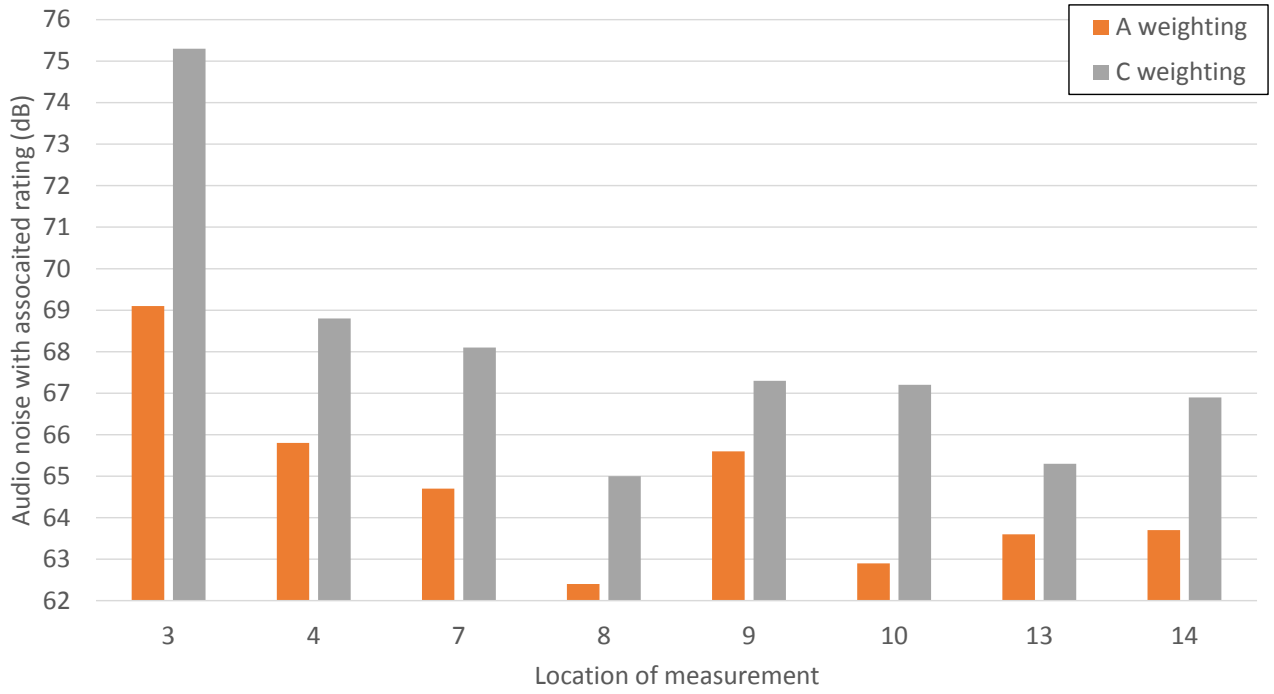


Figure 43: Noise measurement at HMI setting Inverter B and Inverter C export +74 kW

The EMF measurements recorded at the HMI setting of inverter B and inverter C set to export +170 kW (100 % loading) and inverter B and inverter C set to export +74 kW (50 % loading) is shown in Figure 44. It can be observed that in nearly all cases the EMF is higher at the higher power output. It can also be observed that the highest measurement was observed at location 11, the cause of this higher reading is unknown but it does correspond to a high reading for this location of the SOP (right hand side) in the previous EMF measurements (sections 4.2 and 4.3). Unexpectedly location 2 has a higher EMF reading than location 1 which is physically closer to the SOP. The cause of this higher than expected measurement is attributed to the measurement location being in close proximity to the coolant system.

The EMF specification provided by TPS (taken from 1998 ICNIRP exposure guidelines [8]) states that the electric field should not exceed 9.0 kVm^{-1} for 1 m and 2 m measurements from the device. It can be observed that this limit is not exceeded for any location or any power output level in this test.

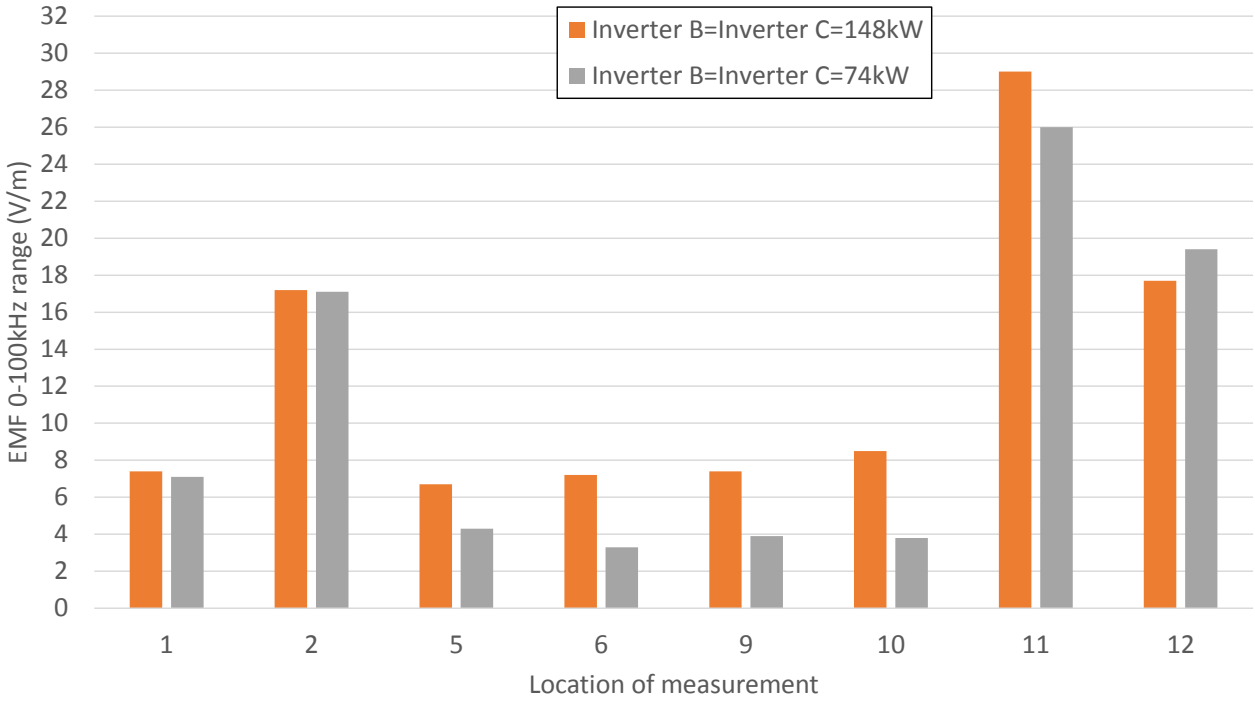


Figure 44: EMF measurements (0-100kHz range)

4.5.3 Conclusions

This test is a repeat of the EMF and audio measurement test (completed earlier in this report) at increased distances from the SOP. This test evaluates how the EMF and audio measurements would change at distances further from the SOP, whether the limits specified by TPS relating to EMF and audio would be exceeded, and whether the EMF and audio measurements exceed relevant standards i.e. Control of Noise at Work Regulations 2005 [6] and 1998 ICNIRP exposure guidelines [8].

The results show that in all locations and for both power output levels the noise limit specified by TPS is exceeded however the results also show that the maximum audio noise (A and C weightings) comply with the Control of Noise at Work Regulations 2005 [6] which have a higher limit than that specified by TPS.

The EMF measurement limit specified by TPS is not exceeded for any location or power output level (taken from 1998 ICNIRP exposure guidelines [8])

4.6 Phase unbalance improvement test (single phase real power support)

The objective of this test is to record the operation of the SOP when a single phase primarily resistive load is connected to the 400 V side of substation A as shown in Figure 45. This test evaluated the SOP's ability to provide power to the single phase load. The desired behaviour from the SOP in this test is to supply active power to the resistive load to reduce phase voltage imbalance. The testing plan is specified in [2] and the log from the test is listed in the following section.

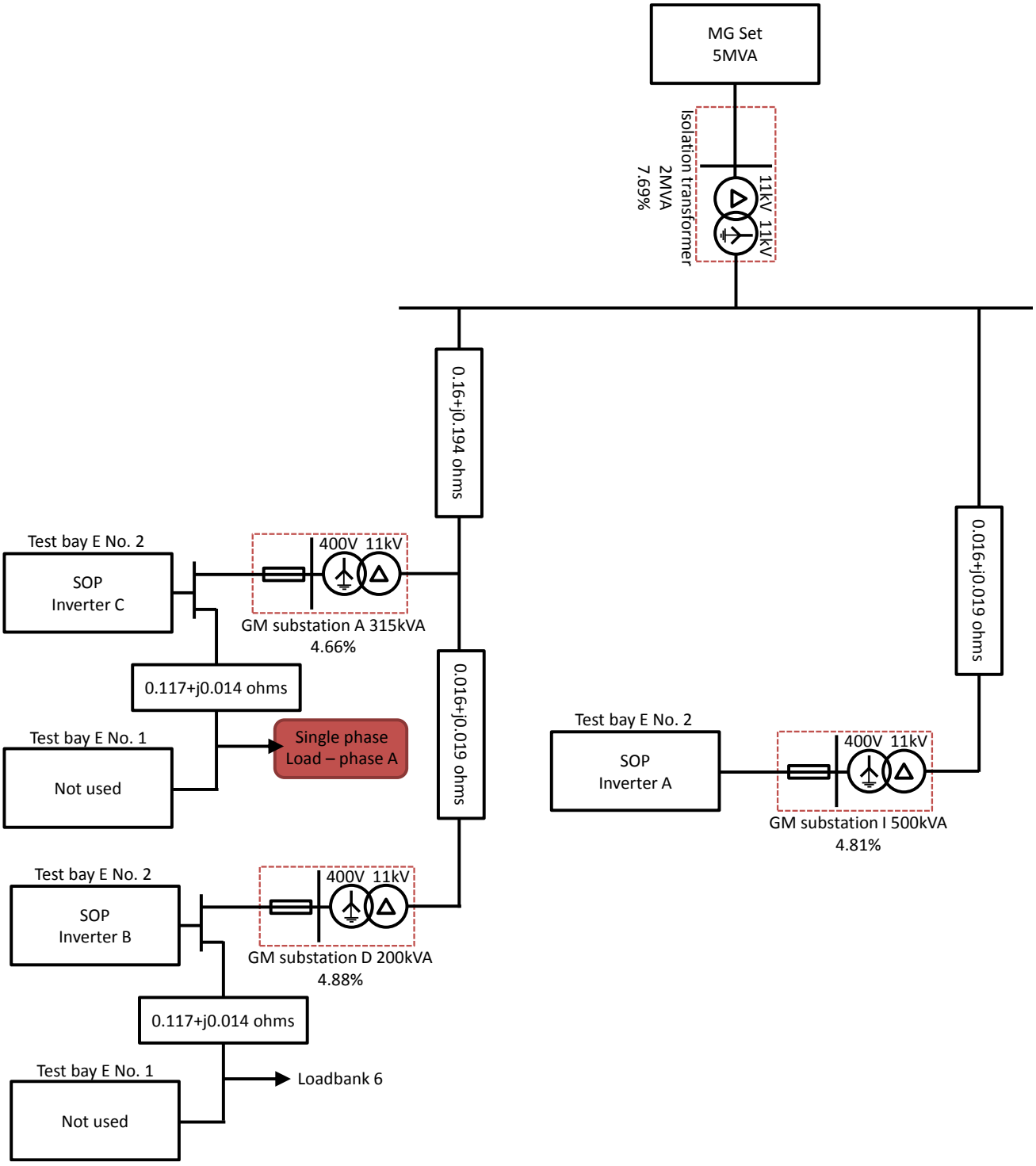


Figure 45: PNDC network configuration for phase unbalance improvement test

4.6.1 Log of test procedure

Prior to the start of this test TPS increased the upper limits on the resonant controllers (this is a further increase from that implemented at the end of Load cycle test 1) and the upper limits on the DC link voltage (up to 775 Vdc) by increasing the upper limits on the SOP ICCs. TPS have advised that this is the highest levels that could be achieved without altering the resistors for the hardware trip on the ICC. This enabled the SOP to operate at higher LV network voltages without producing harmonics on the power output. The update was tested by operating the SOP at a higher network voltage, as described in the procedure listed below. The SOP terminal phase voltage recorded during this test is shown in Figure 46 and the active power output from the SOP is shown in Figure 47.

1. PNDC network energised at 11:36.
2. HMI hearbeats detected. Enabled SOP via HMI at 11:37.
3. Noted HMI state of 12 22 22.
4. The TPS diagnostic equipment (PTE) was observed to be non-operational due to an unknown fault. TPS and PNDC agreed to continue with the test without the PTE operational.
5. At 11:36 observed network voltage of 232V and confirmed DC link is stable using TPS monitoring equipment.
6. At 11:42 using HMI set :
    a. Inverter B export to +100 kW.
    b. Inverter C export to +100 kW.
7. This was sustained for a period of 1 min.
8. At 11:44 using HMI set:
    a. Inverter B to 0 kW.
    b. Inverter C to 0 kW.
9. At 11:46 TPS wanted to check the voltage so the above step was repeated by setting HMI:
    a. Inverter B export to +100kW.
    b. Inverter C export to +100kW.
10. Phase voltages were observed as: inverter A 228 V, inverter B 235 V, and inverter C 235 V.
11. At 11:47 via the HMI set:
    a. Inverter B to 0 kW.
    b. Inverter C to 0 kW.
12. Increased PNDC network voltage to 240V and the following phase voltages were observed: inverter A 242V, inverter B 242 V, inverter C 242 V.
13. At 11:51, to determine if the SOP terminal voltage changes when the SOP is disabled, the SOP was disabled and it was noted the network voltage decreased to approximately 237 V on all inverters.
14. At 11:53 the network voltage was increased to approximately 242V on all inverters with the SOP disabled.
15. At 11:53 SOP was enabled via HMI.
16. The HMI state (after 20secs) was confirmed as 12 22 22. It was noted that the DC link voltage was 770 V.
17. At 11:55 it was noted that the inverter voltages were at 247V. From this response it was concluded that enabling the SOP increases the inverters terminal phase voltage by approximately 5V.
18. At 11:55 via the HMI set:
    a. Inverter B export +100kW.
    b. Inverter C export +100kW.
19. At 11:57 it was noted that the inverter phase voltages were: inverter A 243 V, inverter B 250 V and inverter C 250 V.
20. It was noted that the power output was stable i.e. no oscillations. This was not observed previously at these voltage levels.
21. At 12:00 via HMI set:
    a. Inverter B 0kW.
    b. Inverter C 0kW.

22. At 12:01 the SOP was disabled via the HMI.
23. At 12:03 the network voltage was set to approximately 246V on all inverters. Please note: due to the 5 V increase observed when the SOP is enabled it was suspected when the SOP was re-enabled the SOP would trip out.
24. Enable SOP via HMI at 12:03.
25. SOP tripped out at 12:04.
26. Disabled SOP via HMI at 12:05.
27. Last voltage recorded on power quality analyser 251V on inverter A.
28. A DC link overvoltage error was observed on inverter B and inverter C on TPS's diagnostic interface. A grid frequency high error was observed on inverter A on the same interface.
29. SOP was re-enabled via HMI at 12:07.
30. 251V observed on all inverters at 12:08.
31. This was sustained for a period of 1 min.
32. At 12:10 set HMI to:
    a. Inverter B export +100 kW.
    b. Inverter C export +100 kW.
33. Inverter tripped out at 12:11.
34. SOP re-enabled without external intervention at 12:11.
35. SOP tripped off at 12:11 (HMI export settings still applied at this stage)
36. At 12:12 via HMI set:
    a. Inverter B 0 kW.
    b. Inverter C 0 kW.
37. Enabled SOP via HMI at 12:12. State 3 3 3 observed.
38. SOP turned on and state observed as 12 22 22 via HMI.
39. To determine whether a lower level of export would still result in a trip out, at 12:13 via HMI set:
    a. Inverter B export +10kW.
    b. Inverter C export +10kW.
40. Observed voltage at 251V on all inverters.
41. SOP tripped off at 12:15.
42. SOP disabled via HMI at 12:16.
43. Inverter B and inverter C set to 0kW at 12:16.
44. PNDC network de-energised at 12:22.

These results show that with the update to the resonant controller and DC link threshold the SOP will operate at higher voltages without harmonics in the SOP power output (observed in earlier tests). However, the SOP was observed to trip out when the network phase voltage was set to 246 V and the SOP was controlled to inject active power. This is an area that may require further investigation as the SOP tripping out (as observed in this test) is likely to occur on networks where the voltage is being run in excess of 246 V.

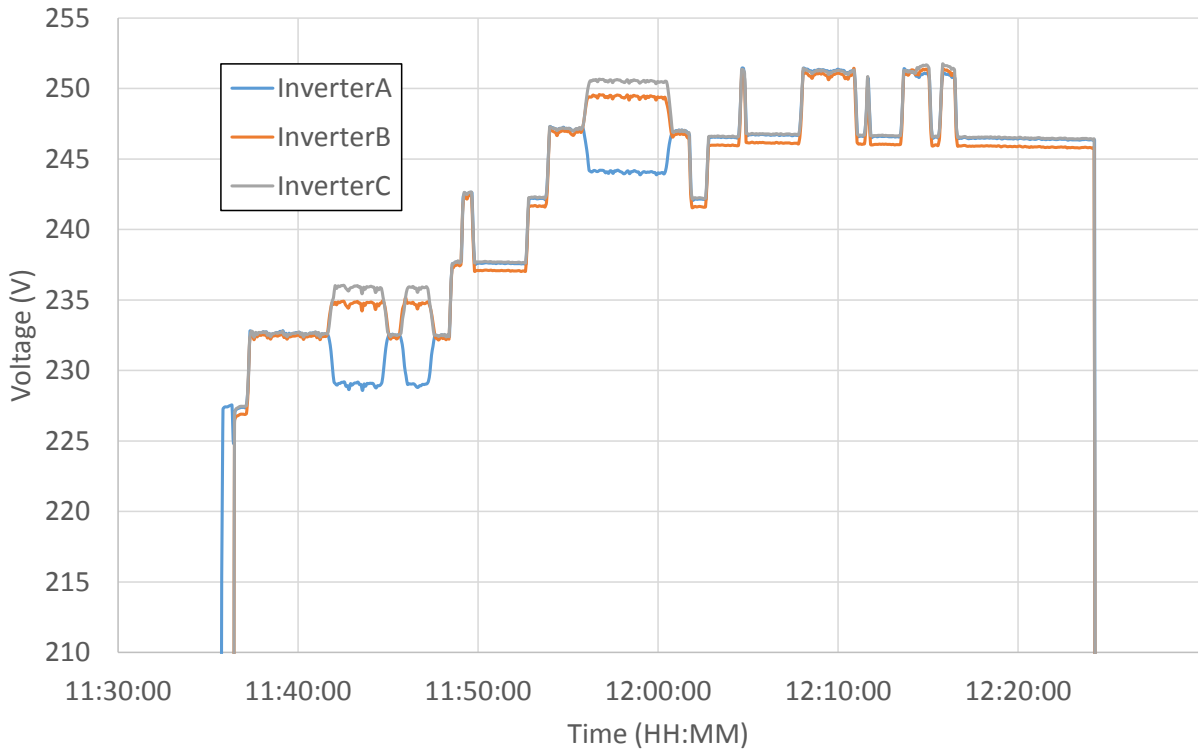


Figure 46: Phase A RMS voltage recorded at SOP terminals

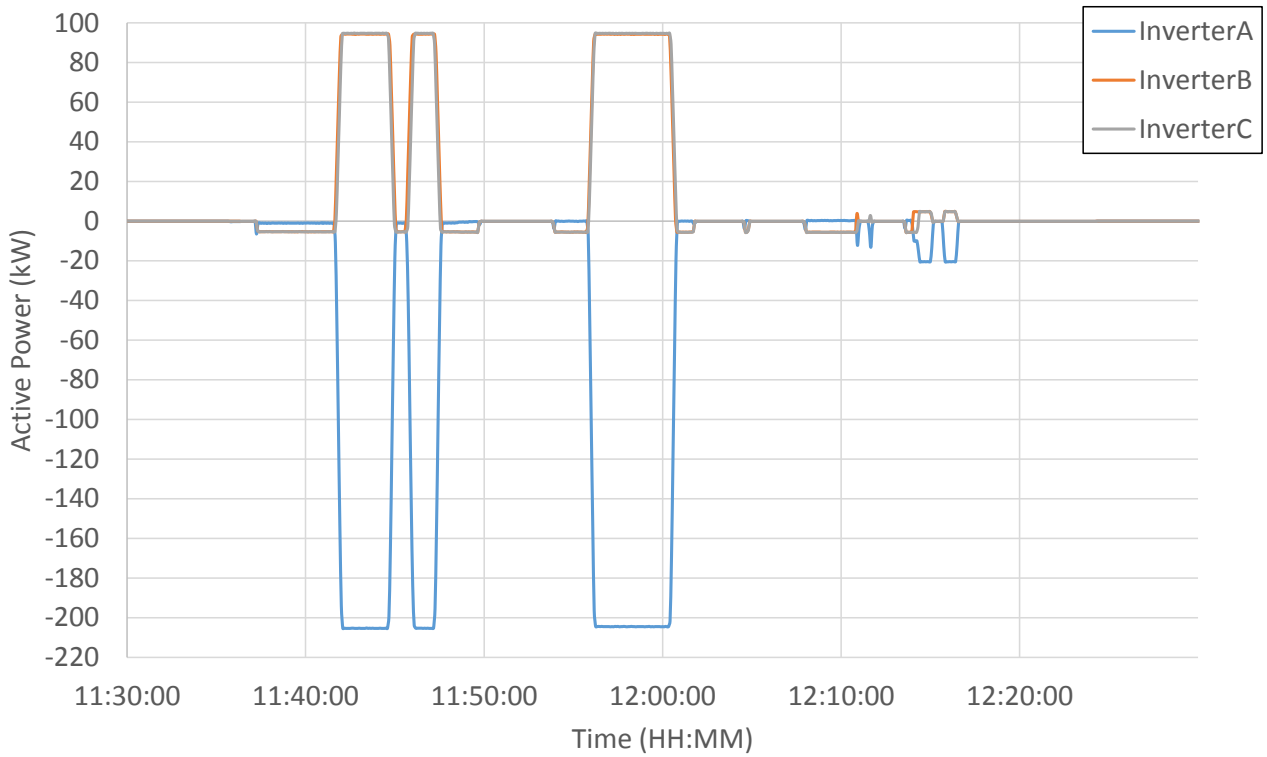


Figure 47: Three phase active power recorded at SOP terminals

After the resonant controller and DC link threshold modification update had been evaluated the phase unbalance test was started. In this test the initial power output from the SOP was controlled using the HMI. A single phase load was then applied to the SOP using a series of load banks connected in parallel (as shown in Figure 45):

1. The SOP was enabled (see introduction of section 3 for explanation)

2. The SOP HMI was set to:
    a. Inverter B export +64 kW and +48 kVAr
    b. Inverter C export +202 kW and +152 kVAr.
3. At substation A, the real and lagging reactive demand on phase A (using load banks) was increased with steps of 5 kW + 1 kVAr up to an additional 50 kW + 10 kVAr, starting from 0 kW and 0 kVAr.

4.6.2 Results and Analysis

The test was first run with the SOP disconnected and one FLUKE 435 power quality analysers was deployed to monitor the terminals of the load bank. The test was then repeated with the same load profile and the SOP connected. The recording of the load profile with the SOP disconnected is shown in Figure 48. Please note that the load was controlled to step in 5 kW/1 kVAr increments from 0 kW/0 kVAr to 50 kW/10 kVar, but due to limitations within the load bank control system there was some error associated with each step e.g. load profile step 1 was controlled to 5 kW/1 kVAr but the observed step (from Figure 48) was 8.4 kW/1.4 kVAr.

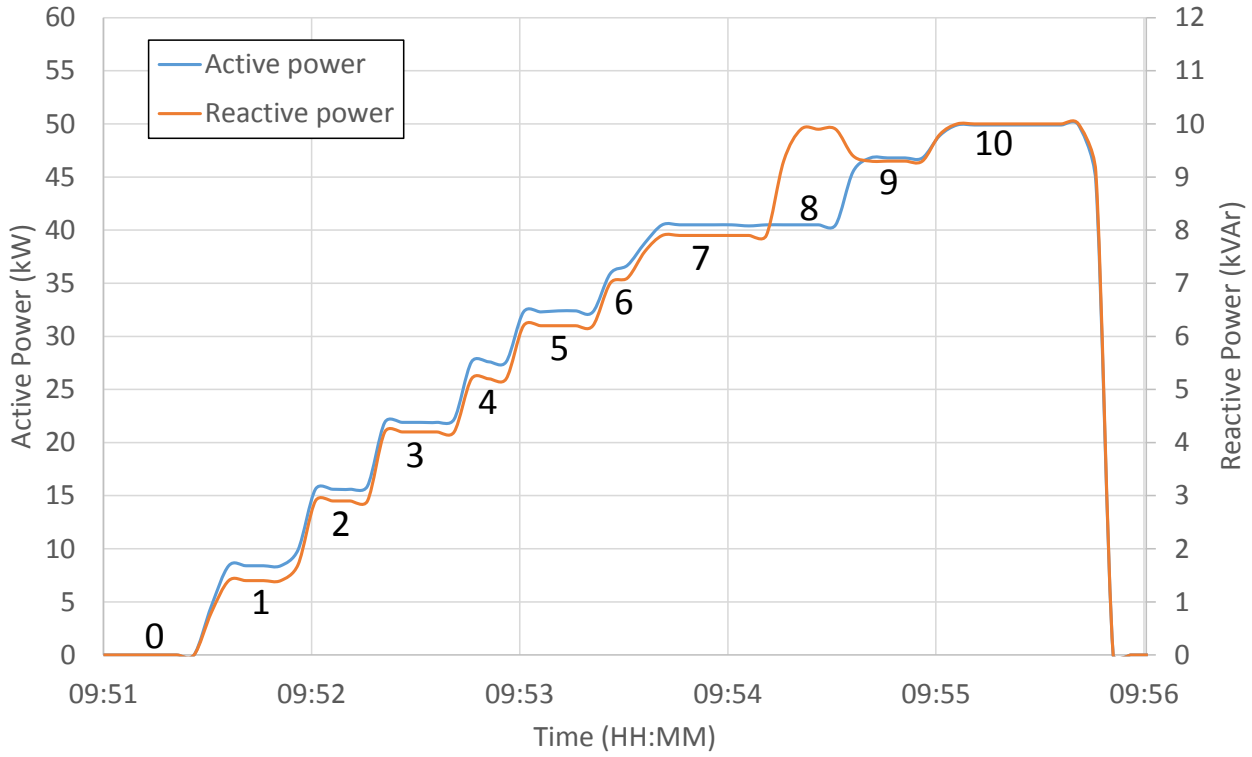


Figure 48: Load profile for phase unbalance test

The phase A voltage recorded at each SOP inverter is shown in Figure 49. In this graph it can be observed how the voltage at the terminals of the SOP decreases as the load on phase A of inverter C is increased. There are several points to note from this test:

1. When the SOP is enabled via the HMI the voltage at the terminals of the SOP increases by approximately by 5V. This can be observed at 10:36. TPS have advised that this may be caused by the SOP applying phase correction.
2. At load profile step 8 (40.5 kW/9.9 kVAr) or higher the SOP will trip due to neutral overcurrent protection. This was observed by TPS using the diagnostic equipment associated with the SOP. These trips can be observed as voltage spikes at 11:04, 11:54 and 12:17. This Neutral Current protection response may have been a result of the higher than anticipated reactive power increment at step 8.
3. When the load (via the load bank) is increased it results in a voltage drop on all inverter terminals, however the load steps are most pronounced on the inverter that is loaded (inverter C) where the step change in load can be observed.

4. At higher loads the SOP current continued increasing beyond the initial load step. This can be observed as a ramping voltage when load step 8 was applied from 11:42 to 11:48 and when load step 9 was applied between 11:48 and 11:54.

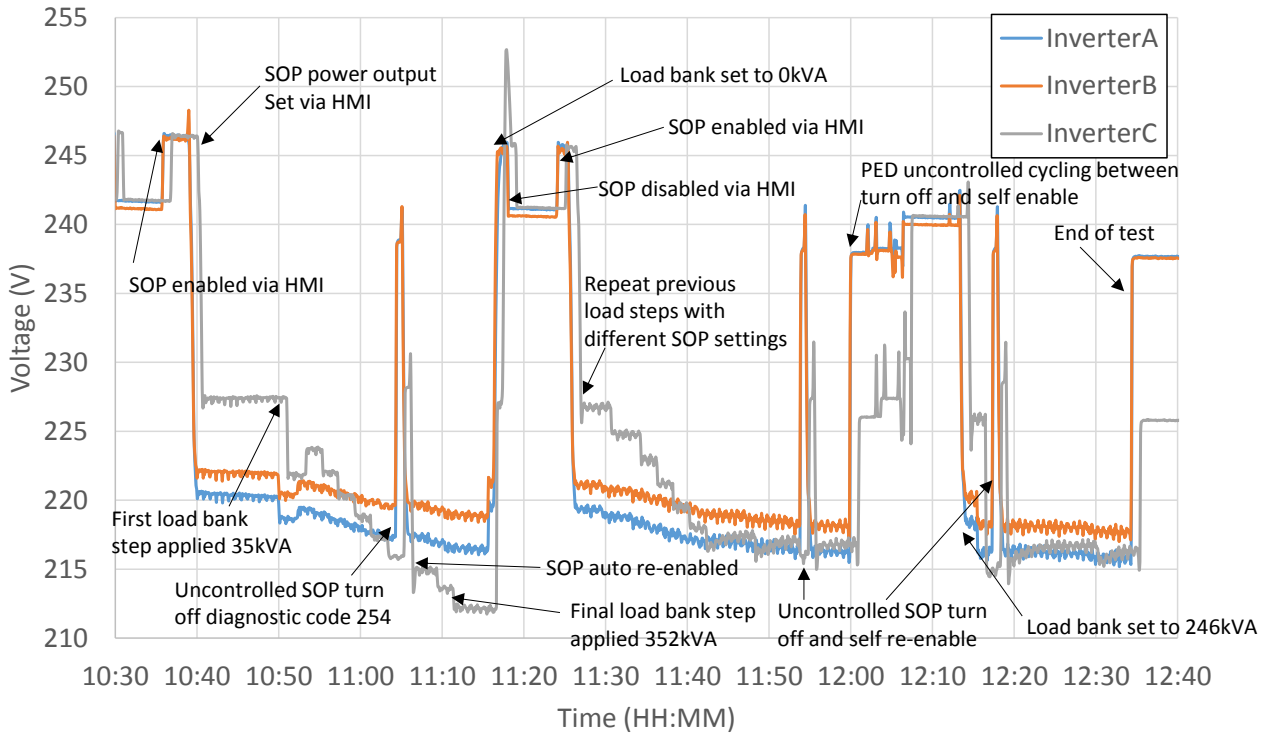


Figure 49: Phase A RMS voltage recorded at SOP terminals

The three phase current recorded at inverter A of the SOP is shown in Figure 50. In this graph it can be observed that:

1. The inverter tripping (due to neutral overcurrent protection) is observed as zero current dips. TPS have advised that the neutral overcurrent protection setting is 200 A, however, the neutral overcurrent recorded at the time of the inverter tripping is recorded as 43.3 A in the first test and 49.8 A in the second test. This is an area that may require further investigation.
2. In the first test (10:40 to 11:18) the SOP does not inject current into phase A as the load is increased. During this test it was observed that the SOP does not breach the voltage threshold. In order to evaluate the SOP's capability to support a single phase load this threshold was reduced prior to the second test (11:27 to 12:01). The original threshold settings on the HMI and the modified settings are given in Table 4, see Appendix A for a more detailed explanation of these thresholds. Please note: that the values are rounded to integers when the HMI interprets them and the thresholds have a greater than/less than relationship. This means that if the V0 set and V0 reset thresholds are set to 2 V the measured zero sequence voltage needs to be 3 V to exceed the V0 set threshold and 1 V to be less than the V0 reset threshold.

Table 4: HMI settings for phase unbalance improvement test

Setting name	Original	Final
V0 set	5V	2V
V2 set	2V	2V

3. In the second test it can be observed that the SOP begins injecting current into phase A at load profile step 6 (36.7 kW/7.1 kVAr).

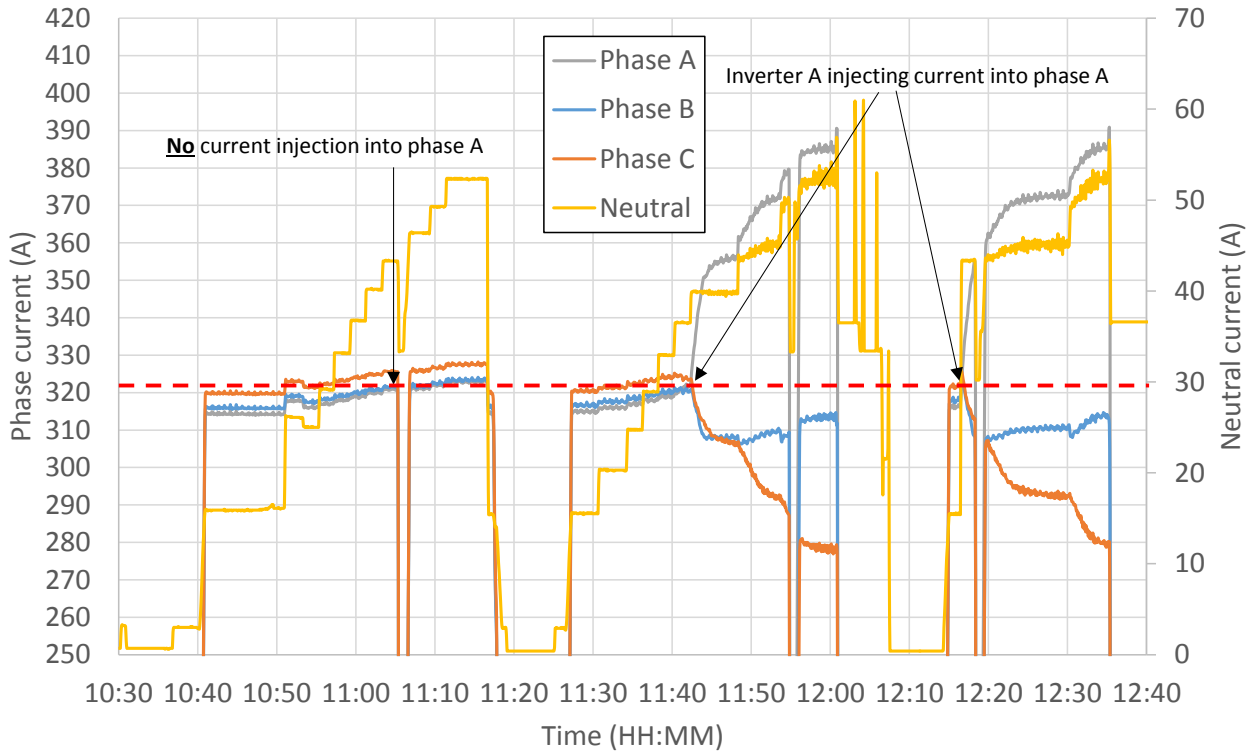


Figure 50: Inverter C RMS current: three phase and neutral

The phase voltages and phase A current at the time the SOP begins injecting current is shown in Figure 51. It can be observed that that the phase A voltage at this time is approximately 216.32V. The zero sequence voltage is calculated using the following script (provided by Imperial College London):

```
SOP_V_L1 = [Vrms_L1, 0]
SOP_V_L2 = [Vrms_L2, -2*pi/3]
SOP_V_L3 = [Vrms_L2, 2*pi/3]

SOP_V0_x = SOP_V_L1(1)*cos(SOP_V_L1(2)) + SOP_V_L2(1)*cos(SOP_V_L2(2)) + SOP_V_L3(1)*cos(SOP_V_L3(2));
SOP_V0_y = SOP_V_L1(1)*sin(SOP_V_L1(2)) + SOP_V_L2(1)*sin(SOP_V_L2(2)) + SOP_V_L3(1)*sin(SOP_V_L3(2));

SOP_V0_Dbl = sqrt(SOP_V0_x*SOP_V0_x+SOP_V0_y*SOP_V0_y);
SOP_V0 = int16(SOP_V0_Dbl);
```

Using this calculation the algorithm will interpret the recorded phase voltages in Figure 51 as a zero sequence voltage of V0 equal to 9 V. The threshold for the algorithm is V0 equal to 2 V. This would suggest that the algorithm should have operated at an earlier step. After consultation with Imperial College London it is proposed that the cause of this error is within the algorithm or the current measurements of the SOP.

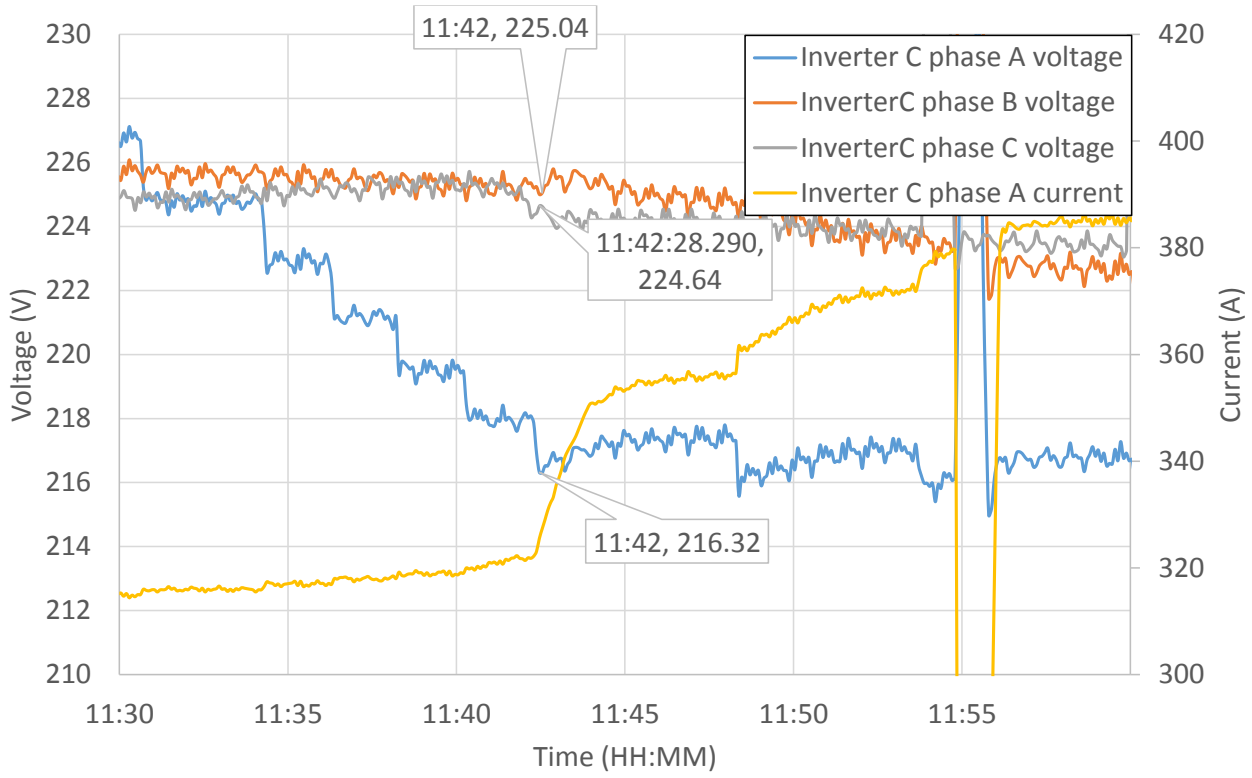


Figure 51: Inverter C RMS phase voltage and RMS phase A current

The same response in the current injection is also observed in the three phase active power injected by the SOP as shown in Figure 52. It should be noted that the total active power is constant for each inverter on the SOP it's the current per phase that changes when a single phase load is applied (as can be observed in Figure 52).

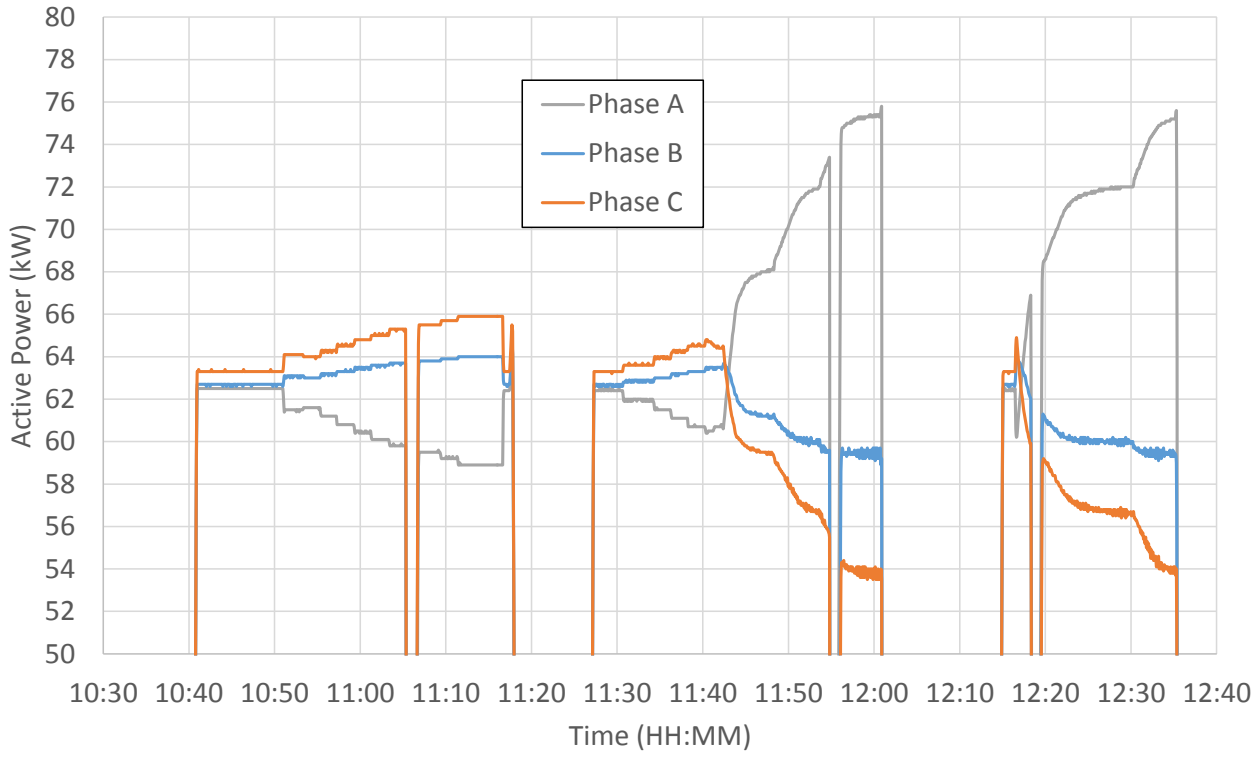


Figure 52: Inverter A three phase active power

4.6.3 Conclusions

The first part of this test evaluated the SOP response after the TPS update (update applied to the resonant controller and DC link threshold). It was observed that with the update applied the SOP will operate at higher voltages without harmonics in the SOP power output (observed in earlier tests). However, the SOP was observed to trip out when the network phase voltage was set to 246 V and the SOP was controlled to inject active power. This is an area that may require further investigation as the SOP tripping out (as observed in this test) is likely to occur on networks where the voltage is being run in excess of 246 V.

The second part of this test evaluated the SOP's ability to provide power to a single phase primarily resistive load. The SOP algorithm detects the unbalanced load by calculating the zero sequence voltage from the measured phase A, B and C voltages. If the zero sequence voltage exceeds a pre-set value (defined in the algorithm) the algorithm controls the SOP to transfer power to the load. The test results confirmed that the SOP will supply a single resistive phase load when the algorithm's zero sequence threshold is exceeded (which is interpreted as an unbalance load and therefore the SOP will try to address that by injecting current). It should be noted that based on the algorithm's calculation for determining the zero sequence voltage (based on phase voltage measurements) the SOP should have operated at a lower level of unbalance than it did in the test. It should also be noted that the neutral current protection was observed to operate unexpectedly at high single phase loads, however the neutral overcurrent protection was set to 200 A and the measured neutral overcurrent was measured as 43.3 A in the first test and 49.8 A in the second test. This is an area that requires further investigation. TPS has advised that the neutral current protection threshold could be increased without detrimentally impacting the protection scheme of the SOP.

4.7 Single phase reactive power support test

The objective of this test is to record the operation of the SOP when a single phase primarily inductive load is connected at the 400 V side of substation A as shown in Figure 53. This test evaluated the SOP's ability to provide power to the single phase load. This network configuration is identical to the configuration used in section 4.6 however in this case the single phase load is controlled to be a inductive load instead of the purely resistive load used in the previous test. The desired behaviour from the SOP in this test is to inject reactive power to supply the single phase load. The testing plan is specified in [2] and the log from the test is listed in the following section.

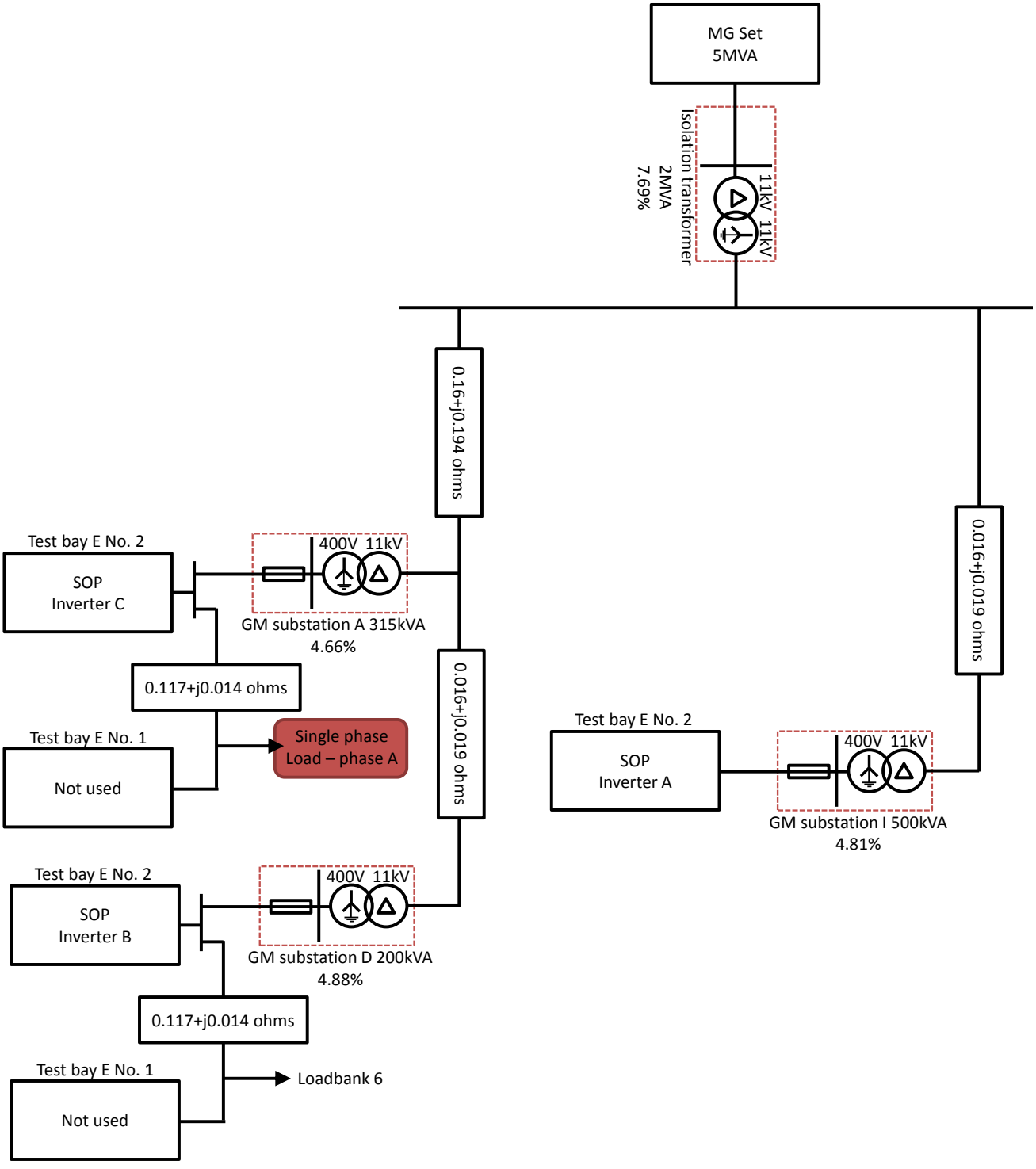


Figure 53: PNDC network configuration for single phase reactive load test

4.7.1 Log of test procedure

As in the previous single phase load test (phase unbalance improvement) several load banks were connected in parallel to achieve the desired load capacity. To ensure an accurate recording of the load profile the test was first run with the SOP disconnected and one FLUKE 435 power quality analyser deployed to monitor the terminals of the load bank. The SOP was then connected and the test was repeated using the same load profile. The recording of the load profile with the SOP disconnected is shown in Figure 54.

Please note: the load was controlled to step in 10 kVAr increments from 0 kVAr to 50 kVAr but due to limitations within the load bank control there was some error associated with each step e.g. load profile step 1 was controlled to 10 kVAr and the observed step (from Figure 54) was 12 kVAr and 0.7 kW. Due to nature of the winding used to implement reactive load there will always be a restive element to any reactive load applied, the reverse is true for a resistive load.

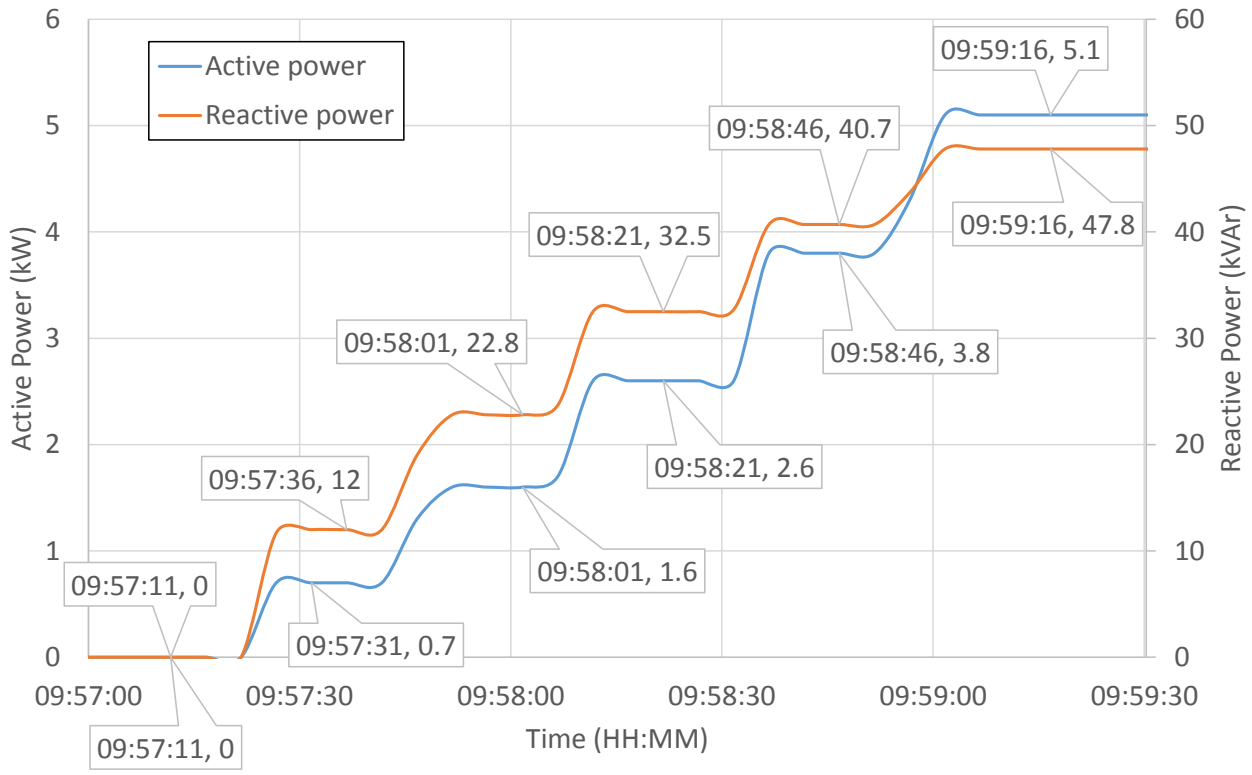


Figure 54: Load profile for phase single phase reactive power test

The list below describes the procedure followed during testing (as specified in the testing plan [2]).

1. The SOP was enabled at 12:54 (see introduction of section 3 for explanation).
2. At 12:46, load step 1 (12 kVAr and 0.7 kW on phase A) from the load profile shown in Figure 54 was applied at the single phase load location shown in Figure 53.
3. At this load step it was noted on inverter C, phase A, that the current started a ramped increase as shown in Figure 56, this caused a ramped increase in the voltage on phase A as shown in Figure 55. The associated active power injection is shown in Figure 57 and reactive power injection is shown in Figure 58. It can be observed that the active power response follows the current injection profile Figure 56. The reactive power response is an increase in the loaded phase (A) and reversal of reactive power on the unloaded phases (B and C). This is followed by a ramped change on all phases: A to 1 kVAr, B to 1.4 kVar and C to 2 kVar, the cause of this response is unknown. The desired behaviour of the SOP is stable reactive power injection in proportion to the applied inductive load.
4. The SOP was observed to unexpectedly trip off at 13:04.
5. At this point the test was stopped. From this response and a discussion with TPS it was concluded that the cause of the uncontrolled SOP trip off was caused by neutral overcurrent protection operating. It

is believed that the reason the SOP continued to increase and did not achieve a stable current injection is because at this stage in the test the DNP3 communication system was not operational. Therefore the algorithm running on the PLC within the SOP did not achieve the necessary 'reset' threshold needed to stop current injection. In the End to End test (reported in section 4.9) the DNP3 communication system was operational and a three phase reactive load was applied. In this instance the SOP does not support the reactive load. This suggests that there may be a problem relating to the reactive power support part of the algorithm as it is has already been demonstrated that the SOP hardware is capable of injecting reactive power up to: Q_{3phase} of -47.1 kVAr and Q_{3phase} of 55.4 kVAr in section 4.4.

4.7.2 Results and Analysis

The phase A voltage recorded at each SOP inverter is shown in Figure 55.

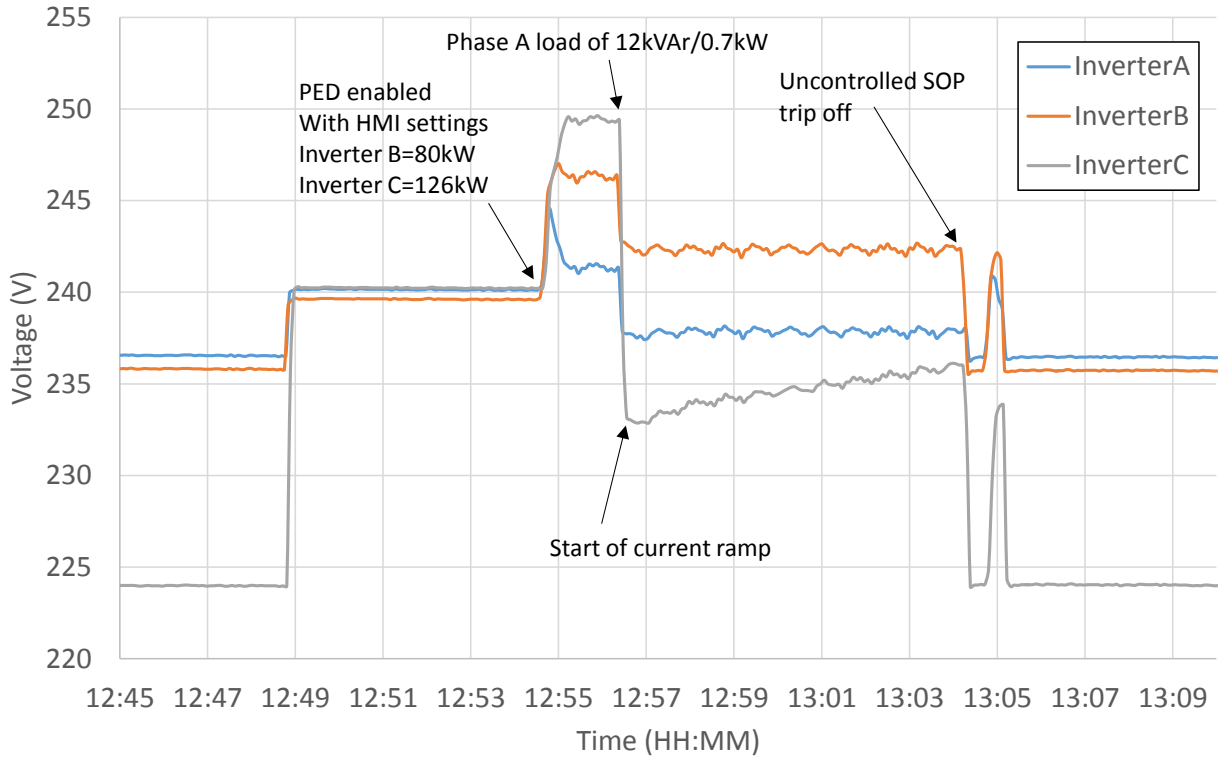


Figure 55: Phase A RMS voltage recorded at SOP terminals

The RMS phase current recorded at inverter C is shown in Figure 56.

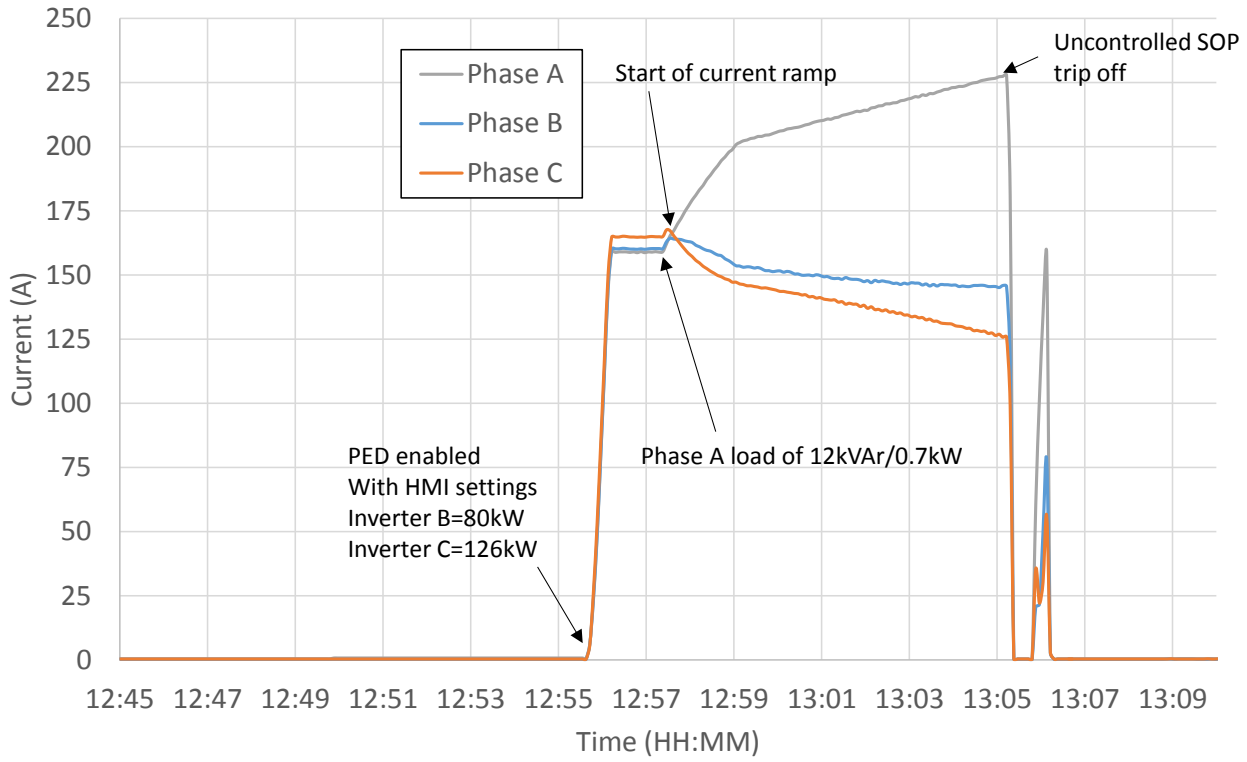


Figure 56: Three phase RMS current recorded at SOP inverter C

The three phase active power recorded at inverter C is shown Figure 57.

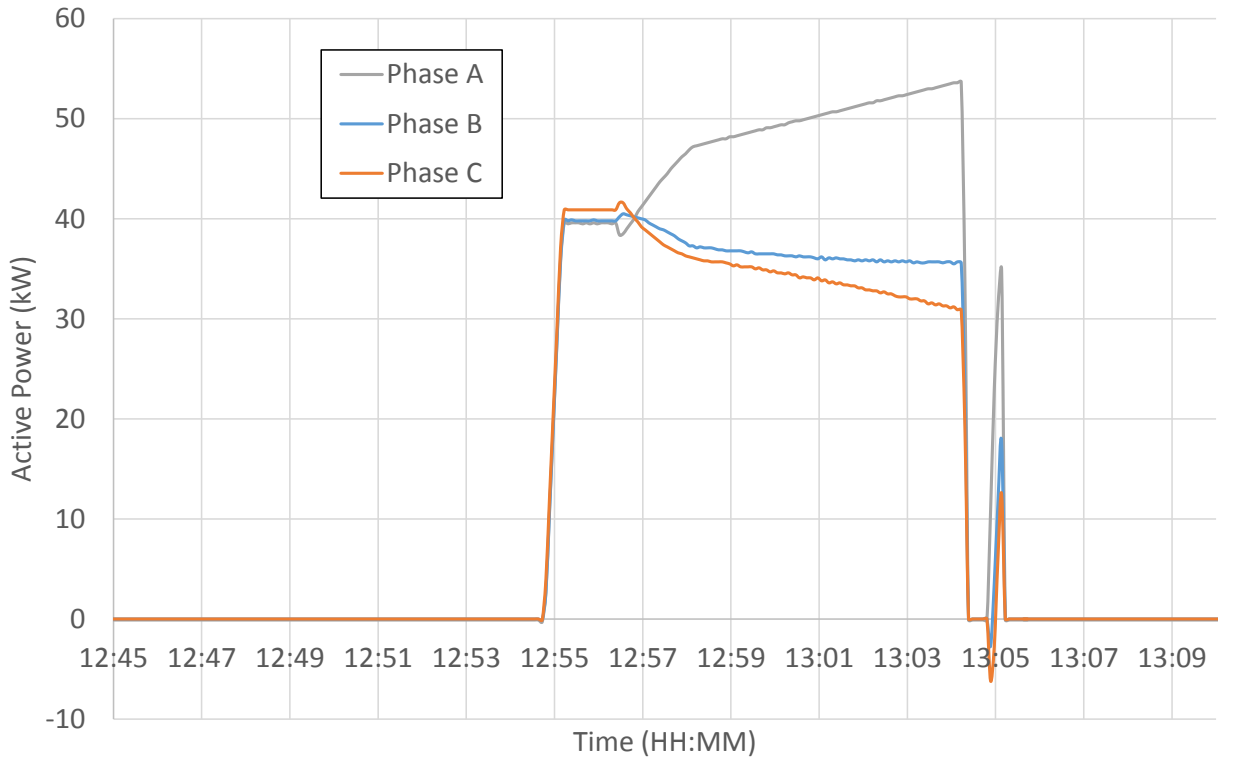


Figure 57: Three phase active power recorded at SOP inverter C

The three phase reactive power recorded at SOP inverter C is shown Figure 58.

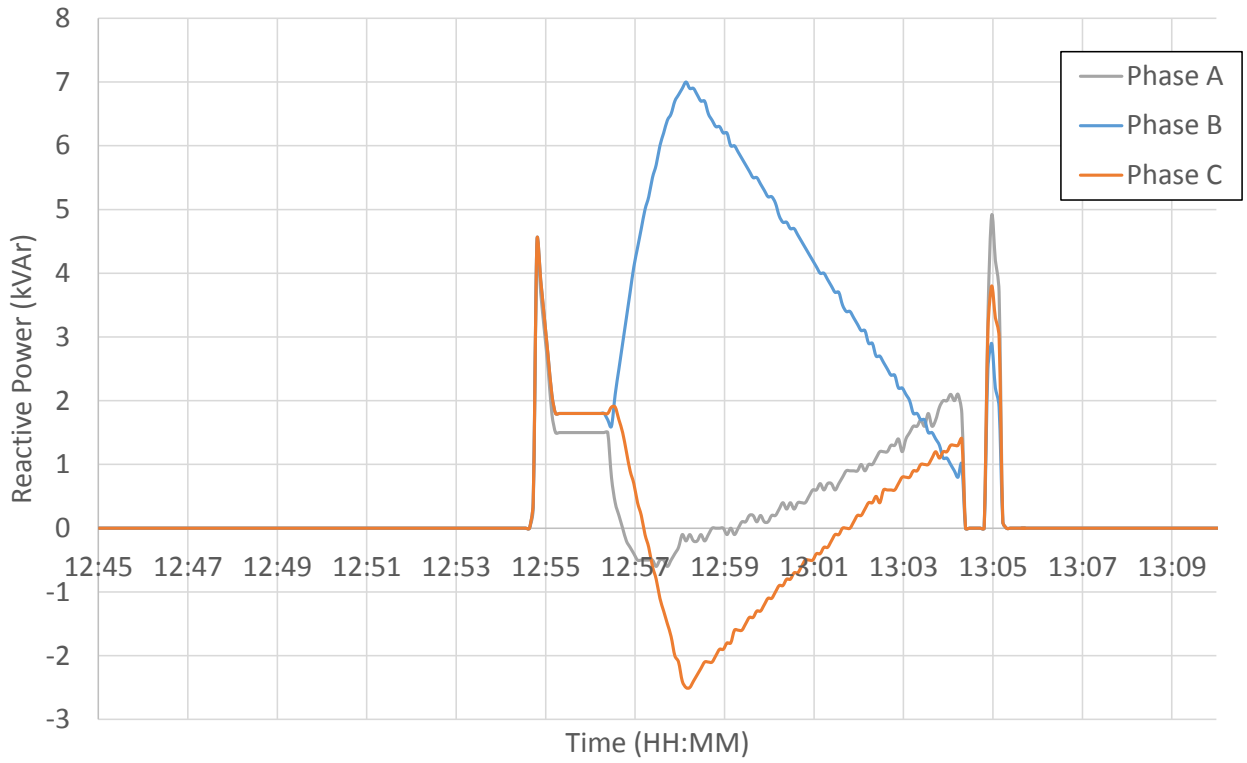


Figure 58: Three phase reactive power recorded at SOP inverter C

4.7.3 Conclusions

It has been demonstrated earlier in this report that the SOP hardware is capable of importing and exporting reactive power (section 4.4). This test demonstrates that the SOP is not responding as expected to a single phase primarily inductive load. This may partially be due to the DNP3 communication system not being operational at the time of this test. However, as will be demonstrated later in this report (in section 4.9), when the DNP3 communication system is operational the SOP again did not respond to support a three phase primarily inductive load. As the hardware has already been tested this suggests the problem may be related to a control issue in the algorithm.

4.8 Voltage support test

The objective of this test is to record the operation of the SOP when the network voltage at one of the SOP inverters is increased and decreased above and below nominal. The expected operation of the SOP is to transfer power (directionality is dependent on undervoltage or overvoltage) to maintain the inverter terminal voltage when a voltage threshold is reached (upper and lower thresholds). The testing plan is specified in [2] and the log from the test is listed in the following section. For the purposes of this test the SOP inverter that was tested is inverter B, as shown in Figure 59.

This test evaluates the SOP's ability to detect a voltage change and implement corrective action to maintain the inverter terminal voltage at upper and lower voltage thresholds.

4.8.1 Log of test procedure

The network configuration for the voltage support test is shown in Figure 59. The voltage at the terminals of inverter B was modified by increasing and decreasing the three phase Automatic Voltage Regulator (AVR) shown in the diagram.

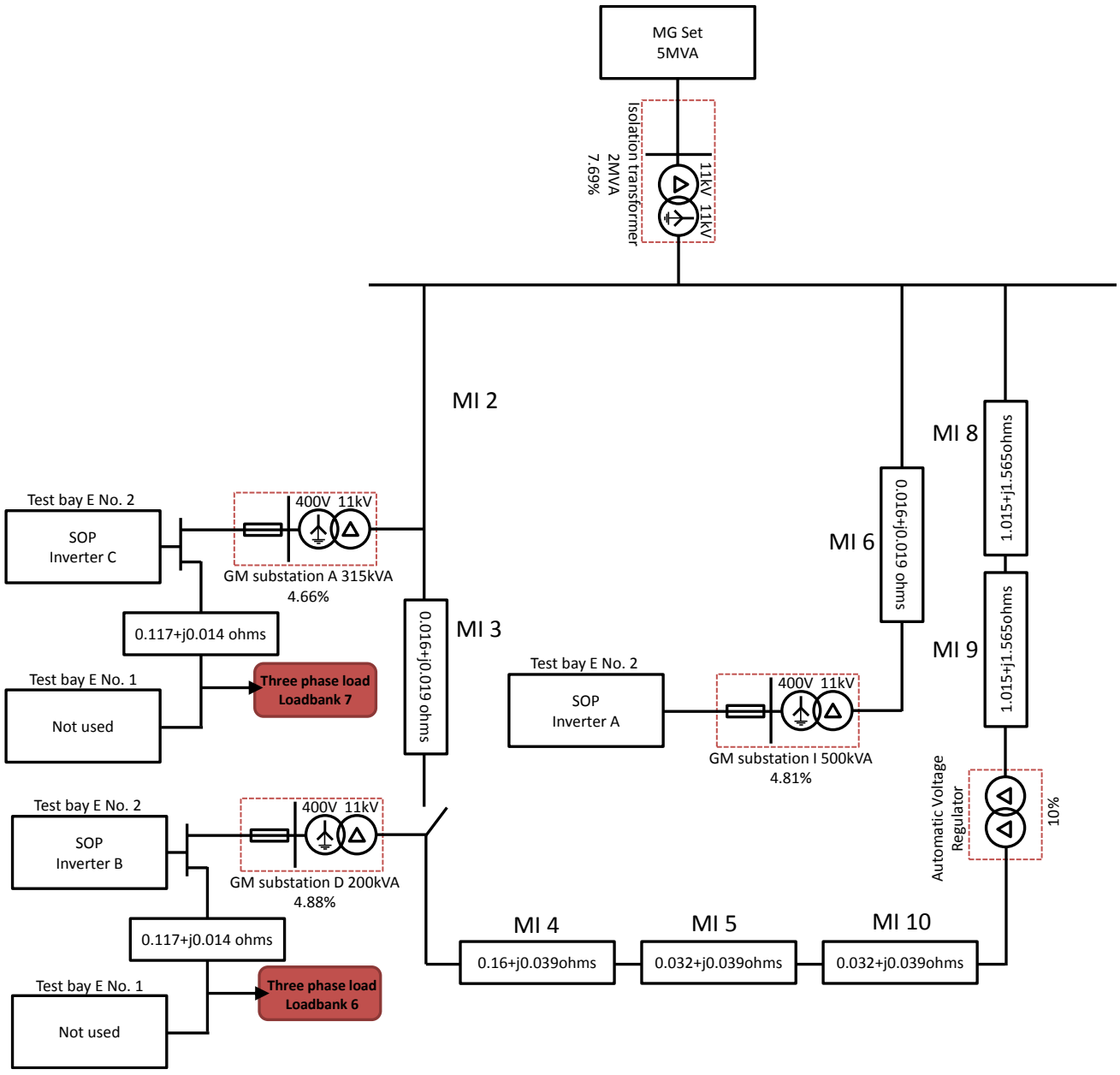


Figure 59: Network configuration for voltage support test

The list below describes the procedure followed during testing:

1. The SOP was enabled (see introduction of section 3 for explanation).
2. The network voltage was reduced until a voltage of 234 V was observed on all inverter terminals (15:50).
3. Loadbank 6 and load bank 7 were controlled to each apply a 40 kVA 0.8 pf load.
4. The voltage was observed to drop on all SOP terminals. The phase A voltages were noted as: Inverter A=228 V, inverter B=225 V and inverter C=225 V.
5. The AVR was reduced by 1 tap (-1 taps) and a voltage drop of 3V was observed on inverter B. Voltage at inverter B=222 V (15:59).
6. This voltage level was maintained for 1 min.
7. The AVR was reduced by 1 tap (-2 taps). Voltage at inverter B=219 V at 16:01.
8. This voltage level was maintained for 1 min.
9. The AVR was reduced by 1 tap (-3 taps). Voltage at inverter B=218 V at 16:03.
10. Observed SOP injecting power to support voltage (as expected)
11. The AVR was reduced by 1 tap (-4 taps). Voltage at inverter B=218 V at 16:06.
12. Observed SOP injecting additional power to support voltage (as expected).
13. It was noted that two of the phases on the AVR had not been tapped down. These phase were tapped down (at 16:13) so all AVR phases tapped to -4.
14. Observed more power transfer from SOP at 16:14. Observed voltage at inverter B=219 V at 16:15.
15. The AVR was reduced by 1 tap (-5 taps). Voltage at inverter B=219 V at 16:16.
16. In order to demonstrate the impact of the SOP reaching its power output limit the power output limit of the SOP was artificially limited to 120 kW (via the HMI). The expected response is that the SOP voltage will drop when the power output limit is reached and the AVR voltage is controlled to decrease further. The AVR tap was then decreased further to (-10 taps) and then the tap was then increased in the positive direction as listed below:
17. Reduced AVR by 1 tap (-6 taps). Voltage at inverter B=217 V at 16:22.
18. Reduced AVR by 1 tap (-7 taps). Voltage at inverter B=216 V at 16:25.
19. Reduced AVR by 1 tap (-8 taps). Voltage at inverter B=215 V at 16:27.
20. Reduced AVR by 1 tap (-9 taps). Voltage at inverter B=213 V at 16:28.
21. Reduced AVR by 1 tap (-10 taps). Voltage at inverter B=212 V at 16:29.
22. Reduced AVR by 1 tap (-11 taps). Voltage at inverter B=210 V at 16:31.
23. Increase AVR by 1 tap (-10 taps). Voltage at inverter B=212 V at 16:36.
24. Increase AVR by 2 taps (-8). Voltage at inverter B=215 V at 16:38.
25. Increase AVR by 2 taps (-6). Voltage at inverter B=218 V at 16:39.
26. Increase AVR by 2 taps (-4). Voltage at inverter B=222 V at 16:40.
27. Increase AVR by 2 taps (-2). Voltage at inverter B=225 V at 16:42.
28. Increase AVR by 2 taps (0). Voltage at inverter B=229 V at 16:42.
29. Increase AVR by 2 taps (+2). Voltage at inverter B=230 V at 16:43.
30. Increase AVR by 2 taps (+4). Voltage at inverter B=232 V at 16:46.
31. Increase AVR by 2 taps (+6). Voltage at inverter B=236 V at 16:47.
32. Increase AVR by 2 taps (+8). Voltage at inverter B=240 V at 16:47.
33. Increase AVR by 2 taps (+10). Voltage at inverter B=243 V at 16:48.
34. Increase AVR by 2 taps (+12). Voltage at inverter B=244 V at 16:49.
35. Increase AVR by 2 taps (+14). Voltage at inverter B=247 V at 16:50.
36. Observed that the SOP is absorbing power to limit voltage increase and at this stage the SOP has immediately reached its power absorption limit.
37. Increase AVR by 2 taps (+16). Voltage at inverter B= 249 V at 16:54. Tap limit reached.
38. Decrease AVR by 3 taps (+13). Voltage at inverter B=243 V at 16:57.
39. Decrease AVR by 3 taps (+10). Voltage at inverter B=236 V at 16:57.
40. Did not observe SOP backing off (i.e. reducing power import) as expected.
41. Decrease AVR by 3 taps (+7). Voltage at inverter B=230 V at 16:59.
42. Decrease AVR to nominal taps (0). Voltage at inverter B=218 V at 17:01.

43. Note: the SOP did not back off early enough as the SOP terminal voltage is now below nominal (230 V) and the SOP is still absorbing active power. The SOP should have stopped absorbing active power at this voltage level.
44. Disabled SOP via HMI and observed power import/export decrease 0 kW and 0 kVAr.
45. Controlled shutdown at 17:04.

4.8.2 Results and Analysis

The phase A voltage profile at each SOP inverter is shown in Figure 60. The different stages of the test are annotated. From this diagram it can be observed that the SOP does not stop absorbing power (as expected) when the AVR is reduced to tap position 0 (nominal tap). This is indicated by a lower recorded voltage at tap position 0 (17:01).

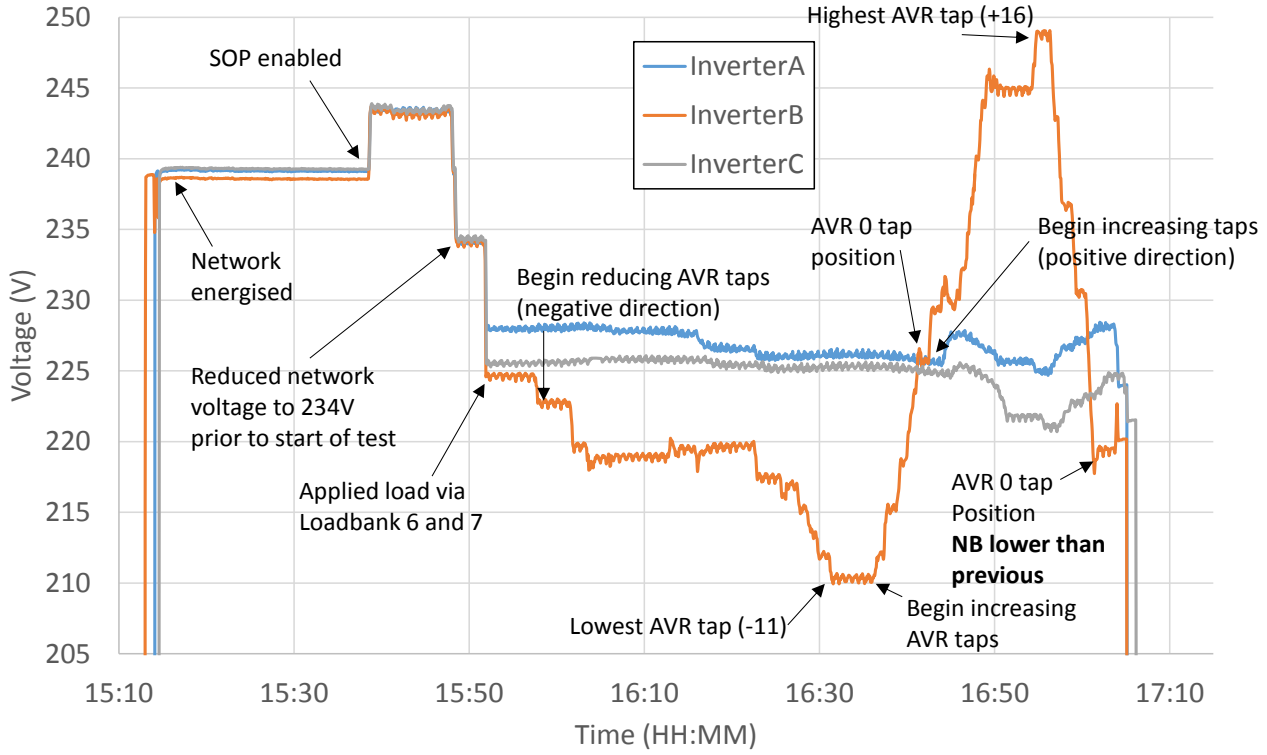


Figure 60: SOP phase A RMS inverter terminal voltage

The phase A current profile at each SOP inverter is shown in Figure 61. The phase A voltage at inverter B has been superimposed onto this graph to show how current transfer changes when the voltage is varied.

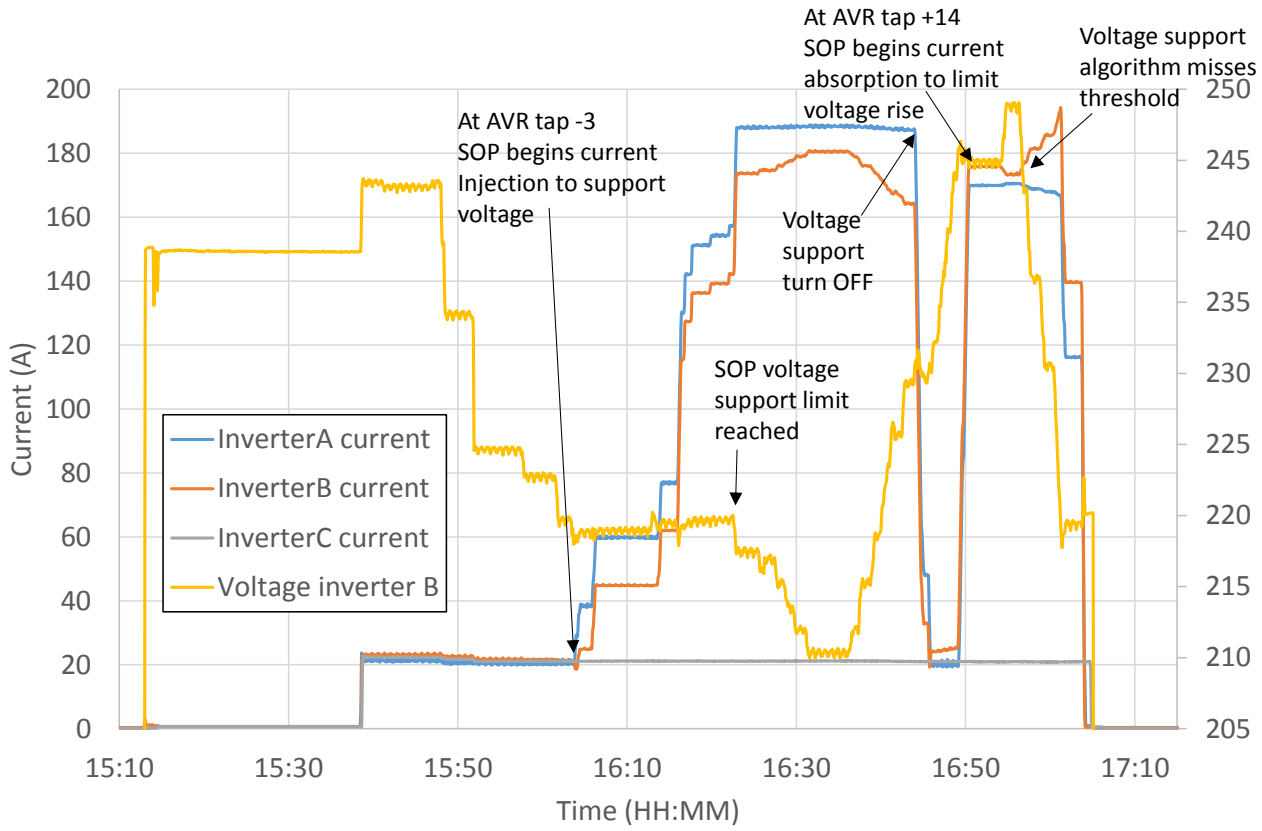


Figure 61: SOP phase A RMS current and inverter B phase A RMS voltage

The total three phase active power transfer at each SOP inverter is shown in Figure 62. It can be observed that as the voltage is reduced at inverter B, inverter B begins to export active power and as the voltage is increased, inverter B begins to import active power. Inverter A compensates for the active power transfer at inverter B. It should be noted that when the voltage is decreased in steps the active power export follows the voltage step changes. However, when the voltage is increased in steps the active power transfer immediately reaches the upper transfer limit when the voltage threshold is exceeded.

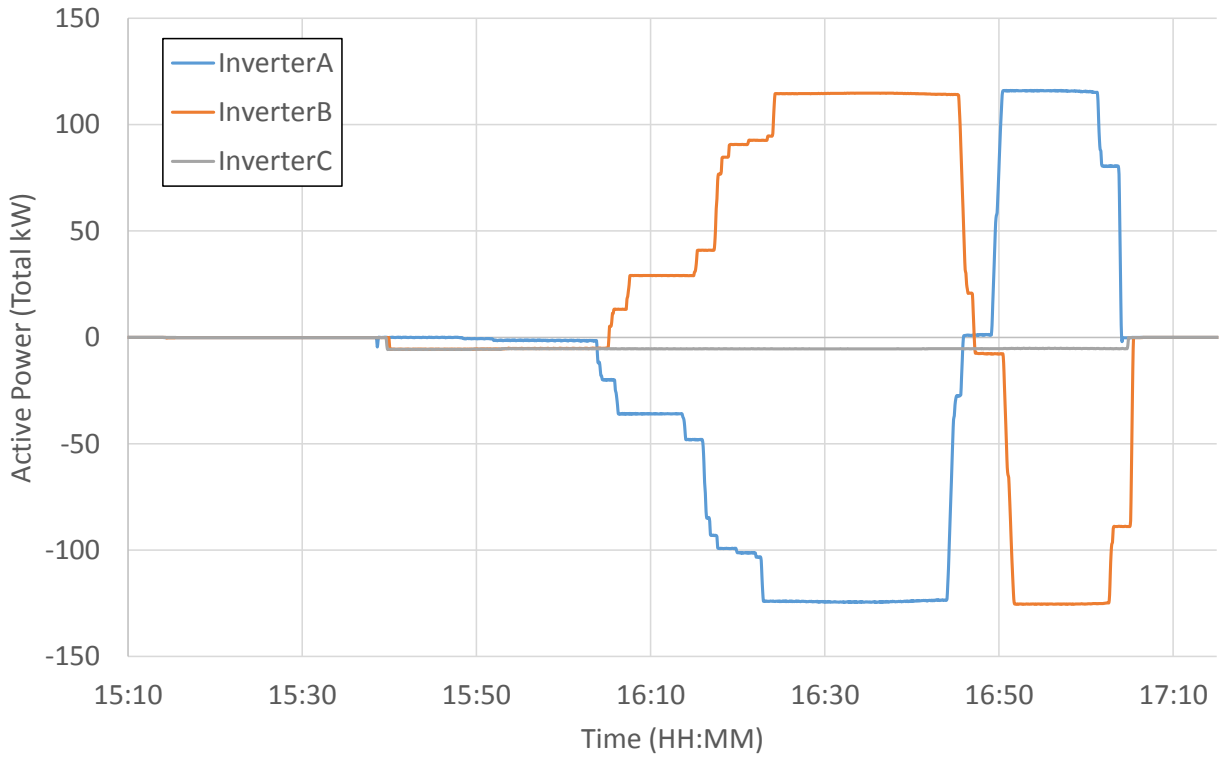


Figure 62: Total three phase active power from SOP

The total three phase reactive power transfer at each SOP inverter is shown in Figure 63. The reactive power transfer remains positive (i.e. out of the SOP) for the duration of the test. When the voltage on inverter B is decreased the reactive power transfer from inverter B decreases and when the voltage increases the reactive power transfer from inverter B increases. Inverter A appears to compensate for the reactive power transfer at inverter B.

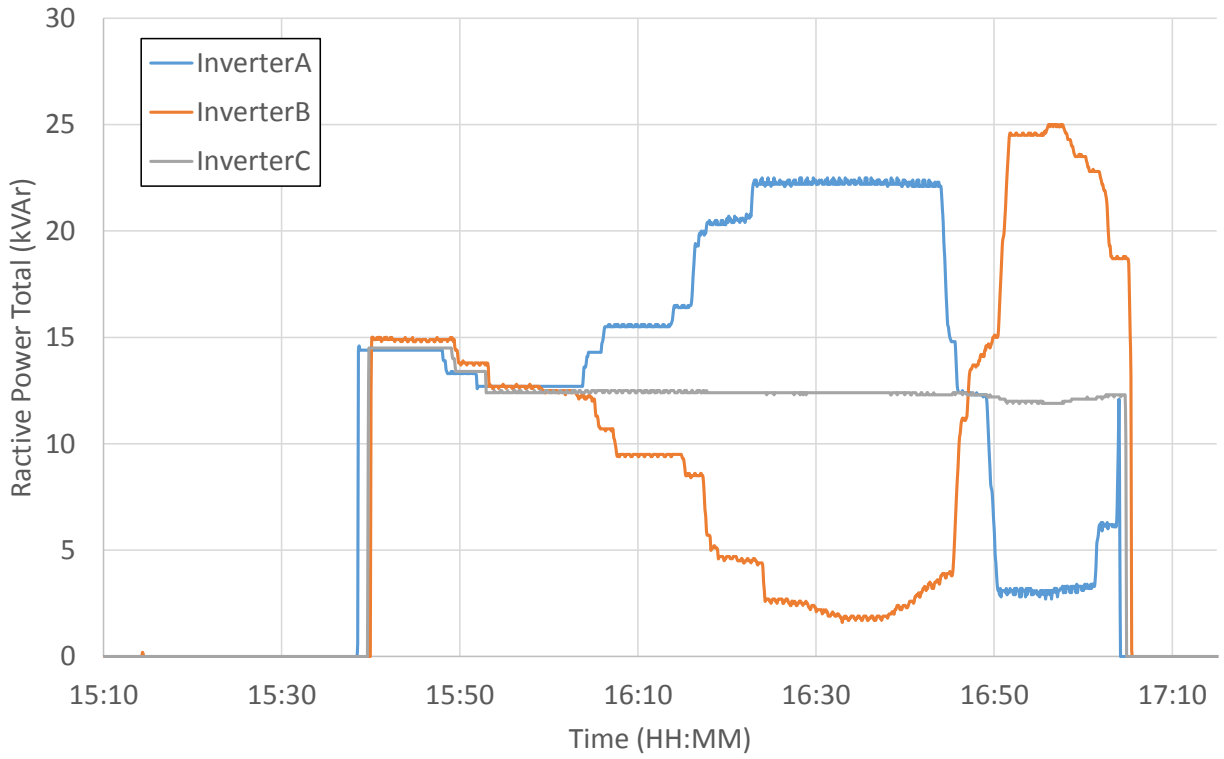


Figure 63: Total three phase reactive power from SOP

4.8.3 Conclusions

This test evaluates the SOP's ability to detect a voltage change and implement corrective action to maintain the inverter terminal voltage at upper and lower voltage thresholds. The SOP supported the voltage by transferring power, though not entirely as expected. It should be noted that the SOP did not stop taking corrective action (power transfer) when the upper voltage reset threshold was reached. It has been advised by Imperial College London, responsible for the development of the algorithm, that this issue likely to be caused by an error in the algorithm and this will be addressed in the next version of the algorithm v1.5.

4.9 End to end test

The objective of this test was to record the operation of the SOP when the load on a substation increased beyond a pre-set threshold (defined in the algorithm). The expected of the operation of the SOP is to inject current to reduce the loading on the substation when the pre-set threshold is breeched. For the purposes of this test the substation is substation D and the SOP inverter is inverter B, as shown in Figure 64. The threshold, as defined in the algorithm, is *transformer import trip* (see Appendix A). The current measured by the 'LV Monitoring Transformer Unit' at substation D is compared to the *transformer import trip* setting corresponding to substation D. If the measured current is in excess of the threshold the SOP will inject current. The testing plan is specified in [2] and the log from the test is listed in the following section.

This test evaluated the SOP communication systems ability to monitor the load current and transfer this information via the DNP3 communication system to the SOP algorithm. This test also evaluated the SOP algorithms response to this information.

4.9.1 Method

The network configuration for the End to End test is shown in Figure 64. In this test load bank 6 was controlled to test the SOP's response to a load increase. Loadbank 7 was not used in this test.

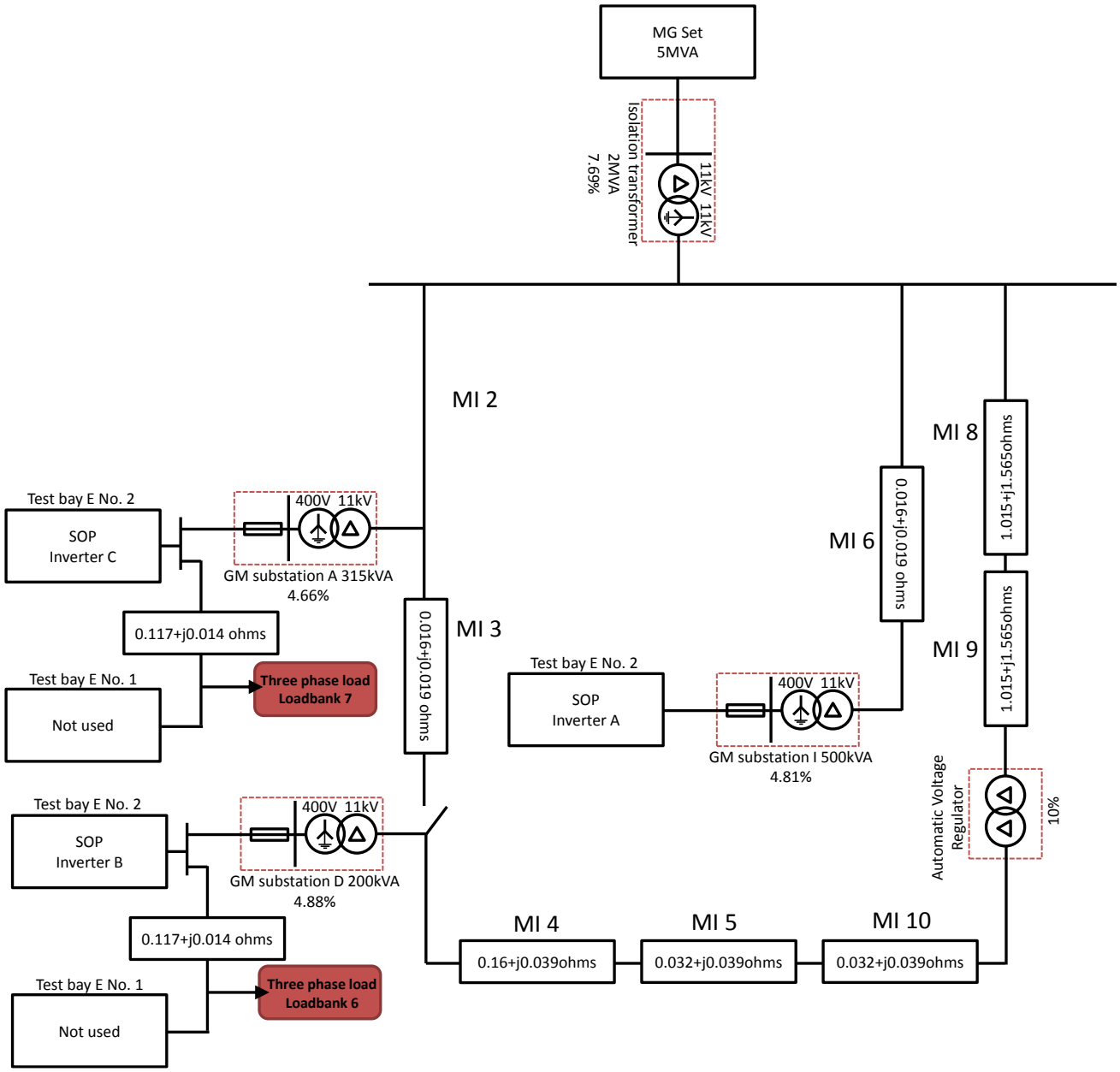


Figure 64: PNDC electrical network configuration for End to End test

The SOP configuration for the end to end test is shown in Figure 65. It can be observed that the current clamps associated with the LV monitoring units are installed on the cable from the test bay to the transformer and from the test bay to the load bank for both Substation D and Substation A. Substation I is directly connected to the SOP i.e. there is not a test bay node as there is for substation D and substation A. For this reason there is only one set of current clamps rather than the two installed at each of the other substations. All the voltage measurements are taken at the terminals of the SOP. An explanation of the operation of the DNP3 monitoring and control system is included in section 3.

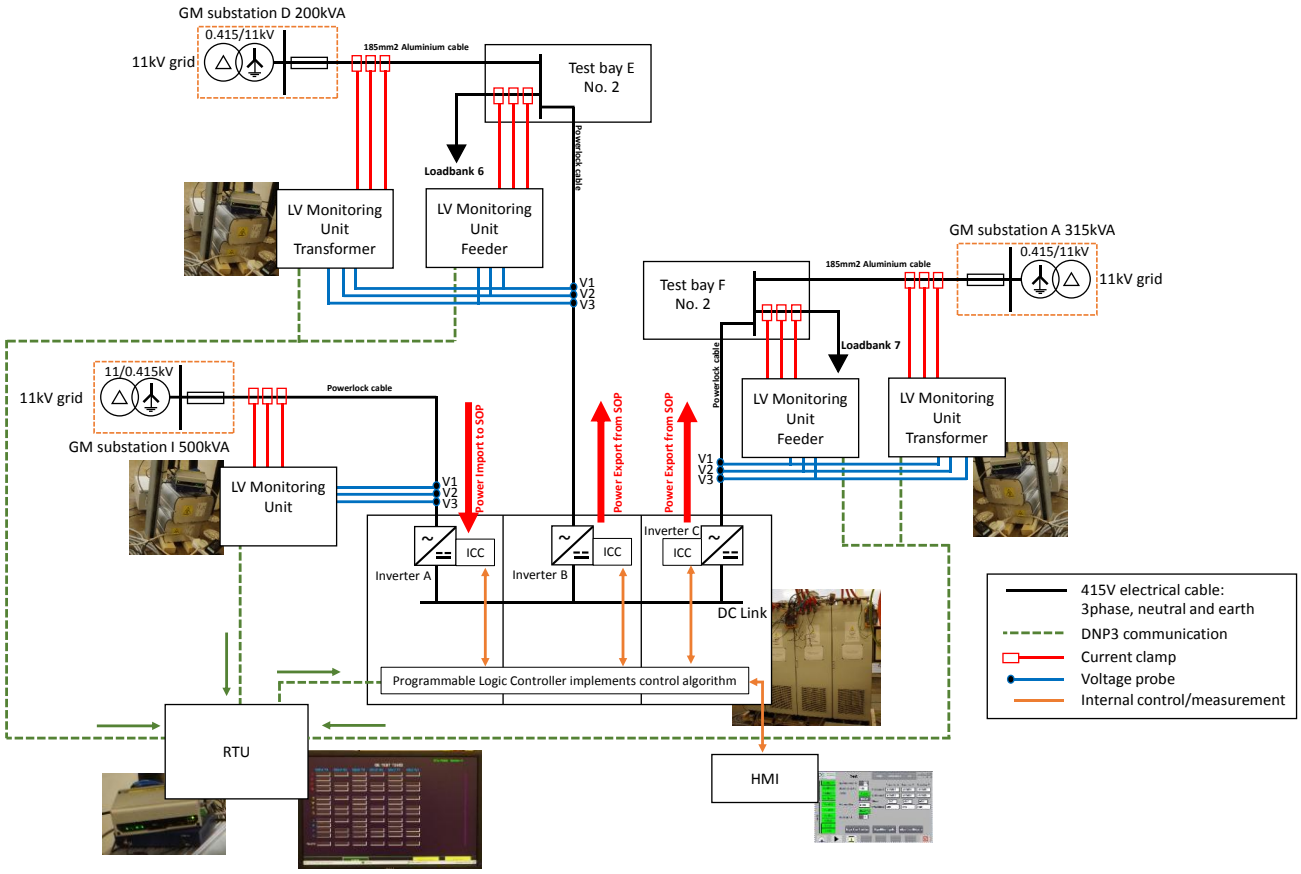


Figure 65: SOP configuration for the end to end test

For the purposes of the End to End test the parts of the algorithm relating to substation load support were enabled via the SOP HMI. Specifically this included:

- V1 voltage high
- V1 voltage low
- V2
- V0
- Feeder import high
- Feeder export high
- Transformer import high
- Transformer export high
- P mode
- Q mode

For a detailed explanation of the HMI screens and the algorithm controls (specifically the setting for this test) see Appendix A. The information contained within this appendix was prepared by Imperial College London. The thresholds within the algorithm relating to the feeder current on inverter B were lowered so that the algorithm would react when load bank 6 was increased. Originally the *transformer import trip* threshold was set to operate for a 50 A load and later in the test the threshold was increased to 100 A.

Please note, the *transformer import trip* threshold will be referred to as variable I_{set} and the *transformer import reset threshold* will be referred to as I_{reset} for the purposes of this test.

It should also be noted that the DNP3 communication was not fully operational for this test so inverter B was loaded, not inverter C as was originally intended in the testing plan. This did not influence the validity of the test as the DNP3 system and algorithm were both tested and it was demonstrated that both were operating. For reference, the issues surrounding the communication are listed below:

- Inverter A and inverter C readings on the mimic screen (displayed from the RTU) were reversed when referenced to the HMI
- Current readings of phase 3 on inverter B were correct on the mimic screen but wrong on the HMI however TPS confirmed that the correct phase 3 reading is going to the algorithm even though it's being displayed incorrectly on the HMI
- Phase A, 2 and 3 current readings on inverter C were correct on the mimic screen but wrong on the HMI (again TPS confirmed that the correct readings are going to the algorithm even though it's being displayed incorrectly on the HMI)
- The current readings for inverter A (substation I) on the mimic were wrong. This appears to be bad data caused by a faulty LV monitor (current clamps were changed to no effect)

4.9.2 Results and Analysis

Figure 66 shows the phase A current measured at the terminals of the SOP inverters during the first hour of the end to end test. At 09:00 in the graph the PNDC network has been energised and the SOP has been enabled (see introduction of section 3 for explanation of enable state).

At 09:05 the balanced three phase load on load bank 6 (connected to SOP inverter B) was increased from 0 kW (in 10 kW increments) up to 30 kW. At the 30 kW load step (43 A load current observed) the SOP began injecting current from inverter B. At this stage: (1) Inverter A began absorbing current to supply inverter B and (2) inverter C remained at its pre-load current of 23A. This is an expected operation from the SOP.

At 09:15 the load on load bank 6 was decreased from 30 kW in 10 kW increments to 0 kW. It can be observed from Figure 66 that inverter B continues injecting even when the load has been removed. This is an unexpected operation as the SOP should stop injecting current when the load falls below the 'reset' threshold (set to 40 A at this part of the test). At 09:30 the SOP was disabled.

At 09:52 the SOP was enabled. It was noted on the HMI Test screen that inverter A P_{demand} was -40 kW and inverter B P_{demand} was +40 kW and that the SOP immediately began injecting current from inverter B.

At 10:03 the SOP was disabled and the voltage support part of the algorithm was disabled to determine if this was causing the current injection ('*V1 voltage high*' and '*V1 voltage low*' to OFF for all inverters). It was observed that on the HMI screen Test Screen (see Appendix A) both inverter A and inverter P demands decreased to 0 kW.

At 10:05 the SOP was re-enabled and it was observed that the SOP was no longer injecting current beyond the 23 A per phase associated with the enabled state. This suggests that the voltage support algorithm may have been conflicting with the current support part of the algorithm (it can be observed from Figure 67 that the trip voltage of 250 V is not exceed on any inverter on any phase during this time period).

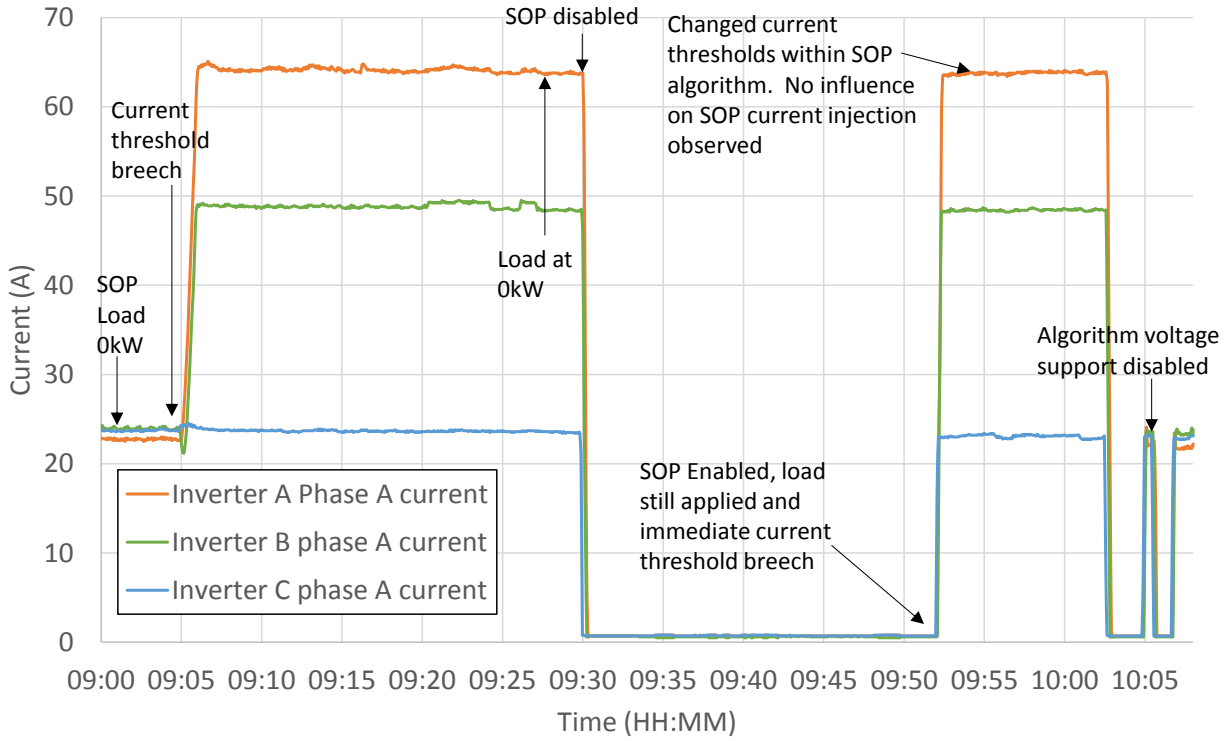


Figure 66: Phase A RMS current output from SOP inverters

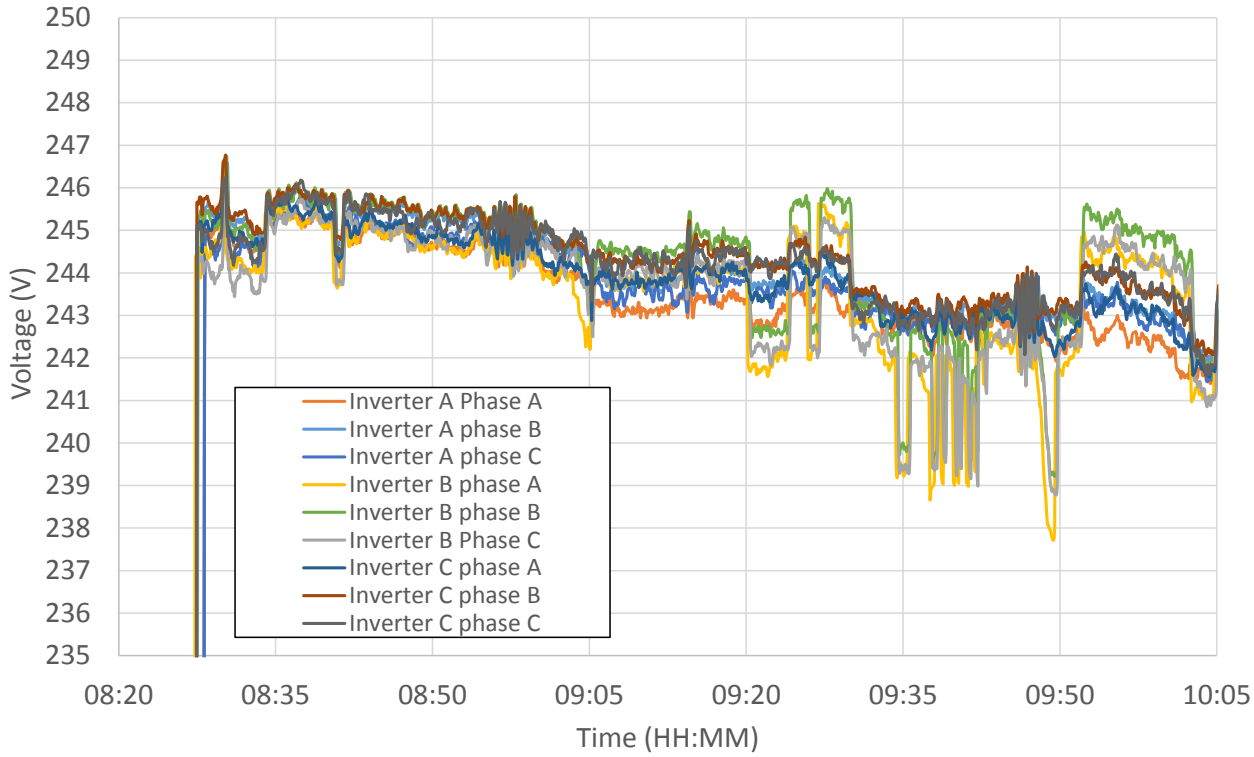


Figure 67: Voltage output from SOP inverters

After the voltage support part of the algorithm was disabled the SOP was re-enabled and load bank 6 was increased from 0 kW (in 10 kW increments) up to 30 kW. At the 30 kW load step (43 A load current observed) the SOP began injecting current from inverter B. This is the expected response from the SOP. However, instead of a constant magnitude of current, the current began oscillating as shown in the period marked as '1' in Figure 68.

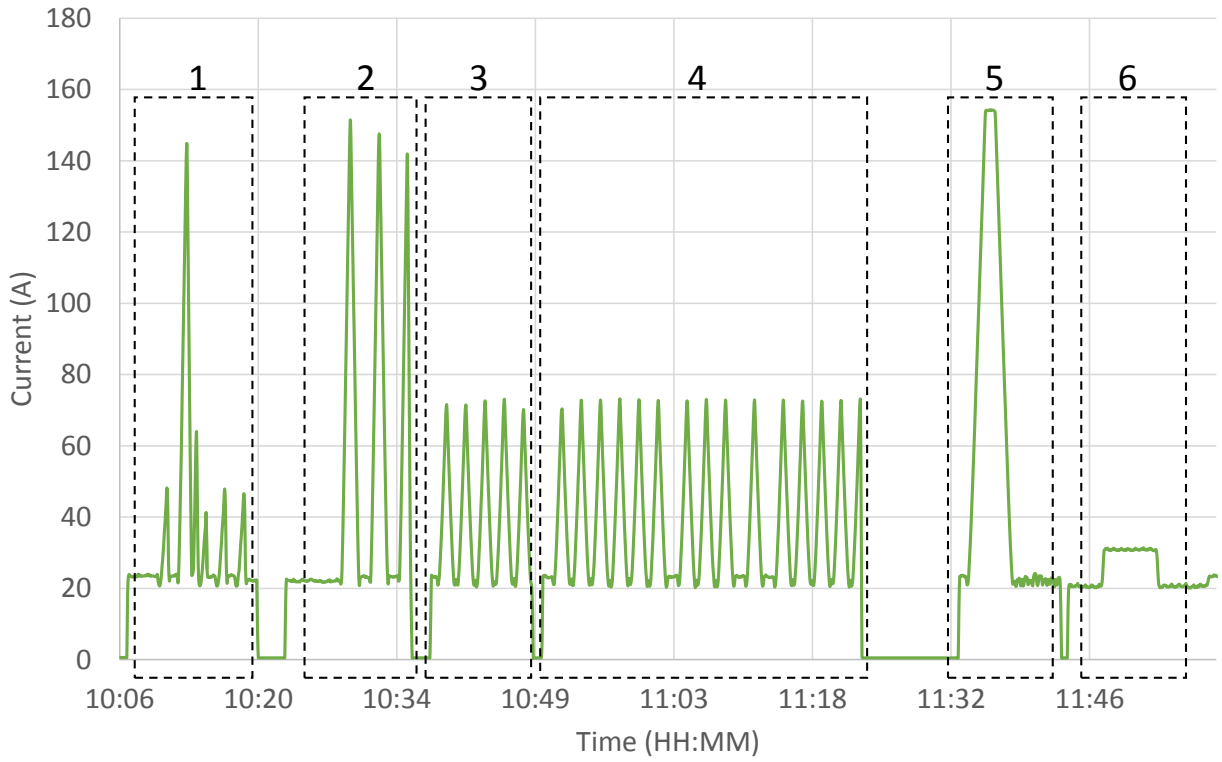


Figure 68: SOP inverter B – phase A RMS current

This current injection oscillation appears to be a result of a number of control settings however the principle of it can be explained with an example, as illustrated in Figure 69.

In this example the load at load bank 6 is increased to 55 A. The SOP is not injecting current therefore the load is supplied entirely from Substation D and therefore I_{SUB} (current from substation) and I_{Load} (current to load) are equal to 55 A.

The RTU updates every one minute so after a time delay (of maximum 1 min) it registers the change in I_{Load} and sends the data to the PLC within the SOP. The SOP algorithm running on the PLC registers that the I_{set} threshold (set to 50 A) has been exceeded and begins injecting current. Therefore I_{SOP} begins increasing, I_{SUB} begins decreasing and I_{Load} remains constant.

However, the RTU only updates every minute so regardless of the new I_{SUB} current the SOP will continue injecting larger amounts of current in an attempt to reduce I_{SUB} below the algorithms I_{set} threshold of 50 A. After one minute the RTU updates and sends the new I_{SUB} data to the PLC. The SOP algorithm registers that I_{SUB} is below the I_{reset} threshold (set to 50 A) and begins decreasing the current injection from the SOP. Therefore I_{SOP} begins decreasing, I_{SUB} begins increasing and I_{Load} remains constant.

At the next RTU update (two minutes into the scenario) the SOP algorithm running on the PLC registers that the I_{set} threshold (set to 50 A) has been exceeded again and begins increasing the current injection from the SOP. This results in the oscillating process repeating. The result of this process is an oscillating current that doesn't reach a stable level.

The parameters that influence the nature and stability of the oscillation are:

1. The RTU update rate
2. The I_{set} threshold
3. The I_{reset} threshold
4. Rate of current injection increase
5. Three phase load bank 6 load

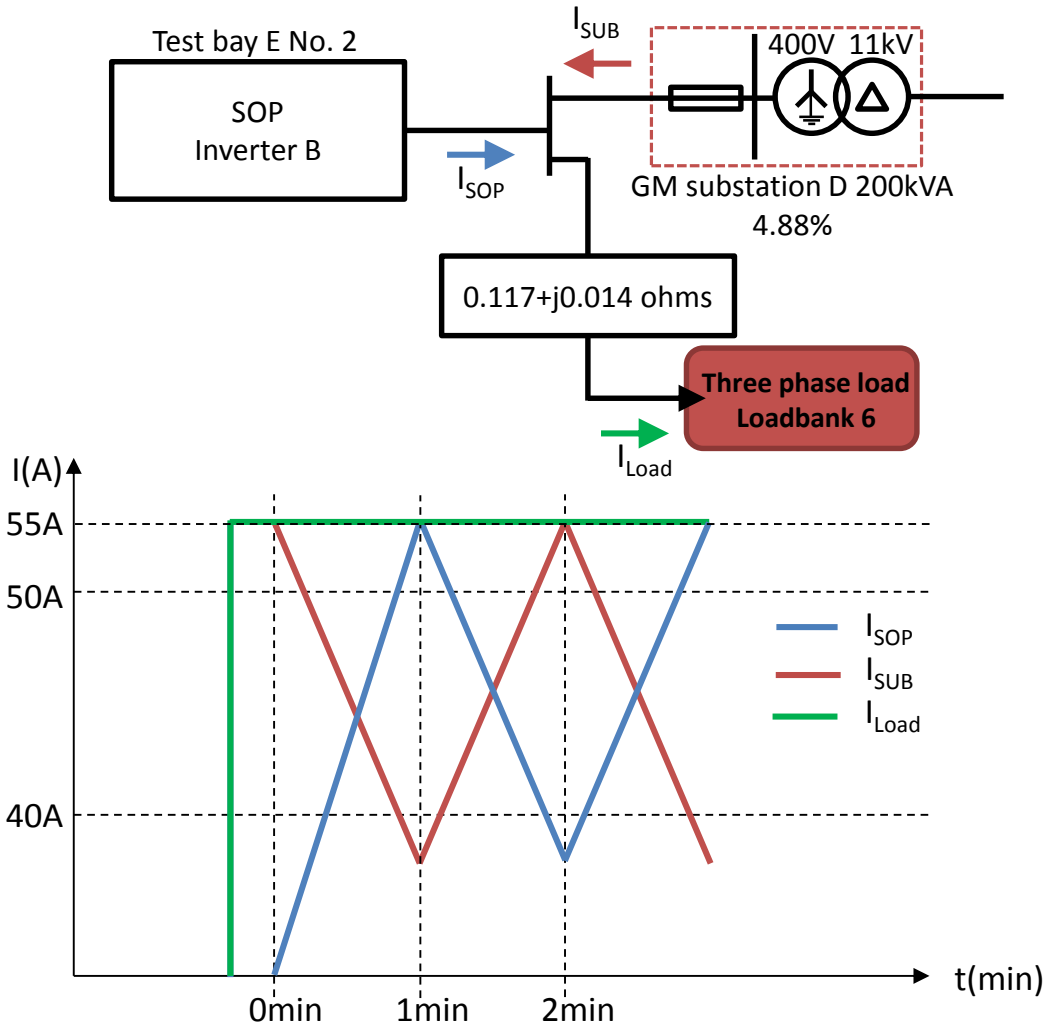


Figure 69: Example of current oscillation in end to end test

The next stage of this test involved modifying the above parameters to see if stable current injection could be achieved. Table 5 shows the different settings for each period (shown in Figure 68), within period 6 (approximately 11:46) stable current injection was achieved with the settings shown in Table 5. In periods 1-5 stable current injection was not achieved.

Table 5: Modified parameters for control of SOP oscillation

Period	RTU update (s)	I_{set} (A)	I_{reset} (A)	P_{rate} (kW/s)	Loadbank 6 (kW)
1	60	60	50	2	30
2	60	100	40	2	70
3	60	100	40	1	80
4	60	100	90	1	80
5	15	100	90	1	80
6	15	100	80	1	80

After stable current injection was achieved the load bank 6 was reduced from 80 kW in 10 kW increments to test the reset component of the algorithm. At 50 kW (I_{load} equal to 73 A) the SOP was observed to reduce current injection to the default enabled current injection value of approximately 20 A per phase (as shown in Figure 68), this is the expected response of the SOP to I_{load} falling below the reset threshold.

The next stage of the test was to repeat the same load test with a three phase inductive load, the inverter B phase A current output from this test is shown in Figure 70.

1. At 12:12 the SOP was enabled and load bank 6 was configured to apply a three phase inductive load from 0 kVAr to 100 kVAr in 10 kVAr steps.
2. At 12:16 when the load bank was increased from 50 kVAr to 60 kVAr (I_{load} of 82 A observed) the I_{set} indicator was observed on the HMI and the SOP began current injection. This is the expected response to the I_{set} threshold being exceed, however, the current injection again began oscillating.
3. At 12:18 the SOP was disabled and via the HMI enables screen the 'P mode' (active power support mode) was disabled and the 'Q mode' (reactive power support mode) was enabled to evaluate whether this was would impact the reactive power support functionality of the SOP algorithm.
4. At 12:23 the SOP was re-enabled and the load bank was increased from 50 kVAr to 60 kVAr (I_{load} of 82 A observed) the I_{set} indicator was observed on the HMI and the SOP began oscillating current injection.

Figure 71 shows the active power output from all three SOP inverters and Figure 72 shows the reactive power output from all three SOP inverters. In Figure 71 it can be seen that when the I_{set} threshold is exceed the SOP starts oscillating between export and import of active power, however in Figure 72 the reactive power input/output from the SOP does not change from the pre-set state other than a saw tooth 'wobble'. This response suggested that the reactive power support part of the algorithm was not operational and at this stage the test was stopped.

Figure 70: SOP inverter B – phase A RMS current

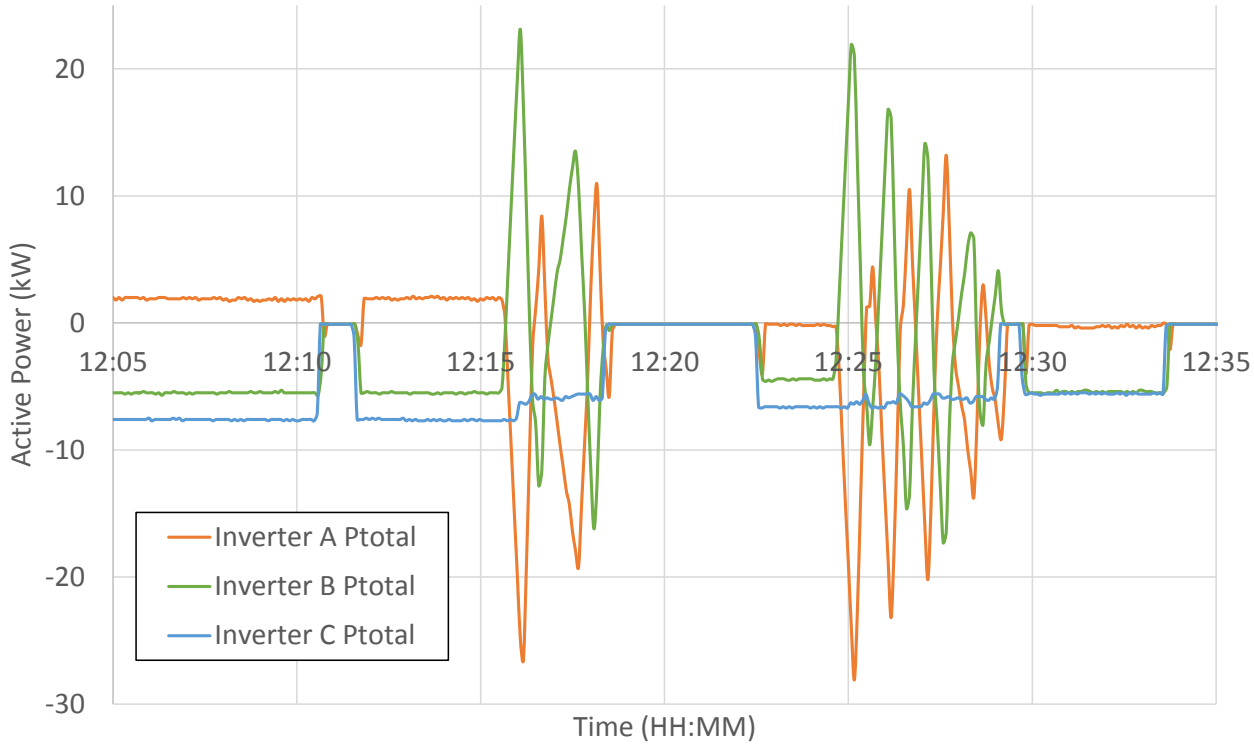


Figure 71: SOP inverters total three phase active power output

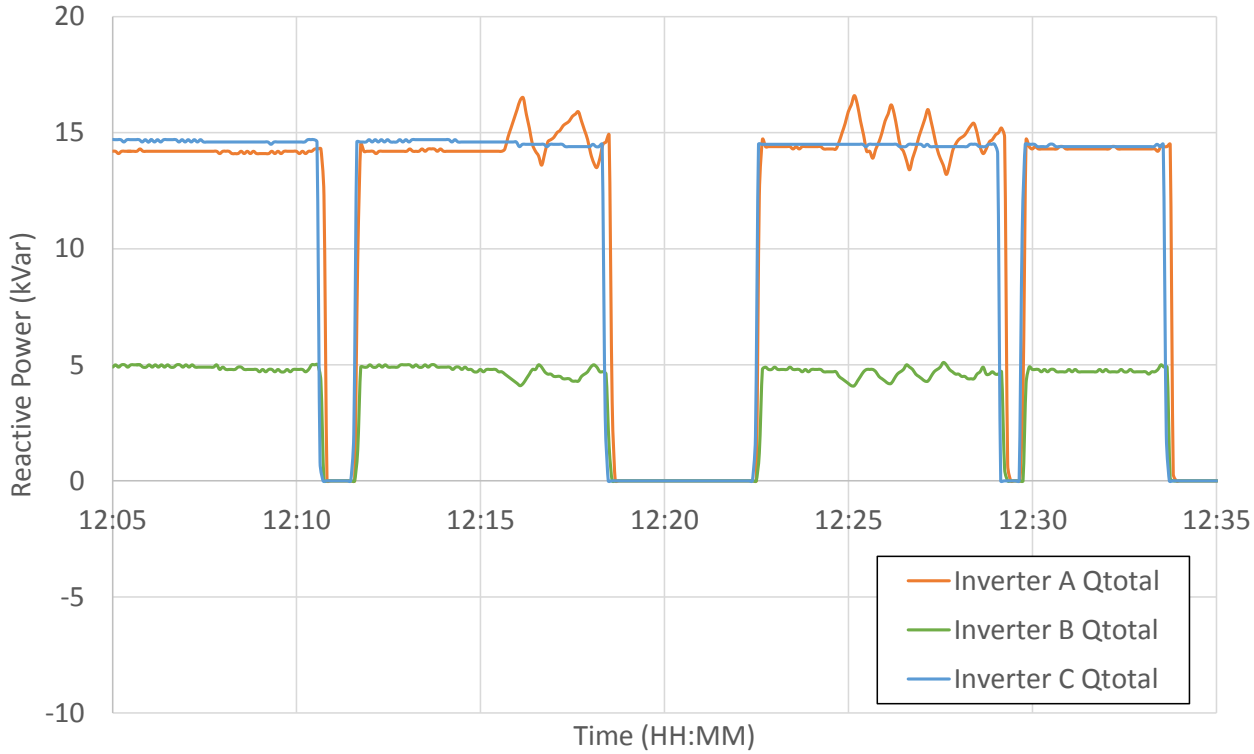


Figure 72: SOP inverters total three phase reactive power output

4.9.3 Conclusions

The test results demonstrate that the DNP3 communication system operates in conjunction with the SOP algorithm. This test results also demonstrate that the current support part of the algorithm operates to reduce

the load on the associated transformer. This was the expected outcome from this test, however, there are a number of areas where unexpected, or out-of-specification behaviour, was observed:

1. This test has shown that the current output from the SOP oscillates when the algorithm trip threshold is exceeded. Imperial College London have been responsible for the algorithm development and has advised that the next version of the algorithm (v1.3 was used for this test and v1.5 is the next iteration) will incorporate a 'predictive' element that will resolve this issue.
2. This test has also indicated that there may be a conflicting control issue between the algorithm voltage support and current support functionality.
3. The test also demonstrated that the SOP failed to operate as expected when supplying the inductive load.

4.10 Fault and frequency test

There are two parts to this test. The objective of the first part is to confirm the different over/under frequency protection limits are operational on the SOP. The objective of the second part is to confirm the SOP limits its output current when faults are applied close to its terminals. For this test three 400 V faults of different types (phase-earth, phase-phase and three phase) were applied close to the inverter B terminals and a phase-earth 11 kV fault was applied downstream of the feeder supplying substation A and D.

4.10.1 Method

The network configuration for this test is shown in Figure 73. The network frequency was controlled using the Motor Generator (MG) set and the faults were applied at Test bay E No. 1. The fault thrower is configurable so that a single phase to earth fault, a phase-phase fault or a three phase fault can be applied.

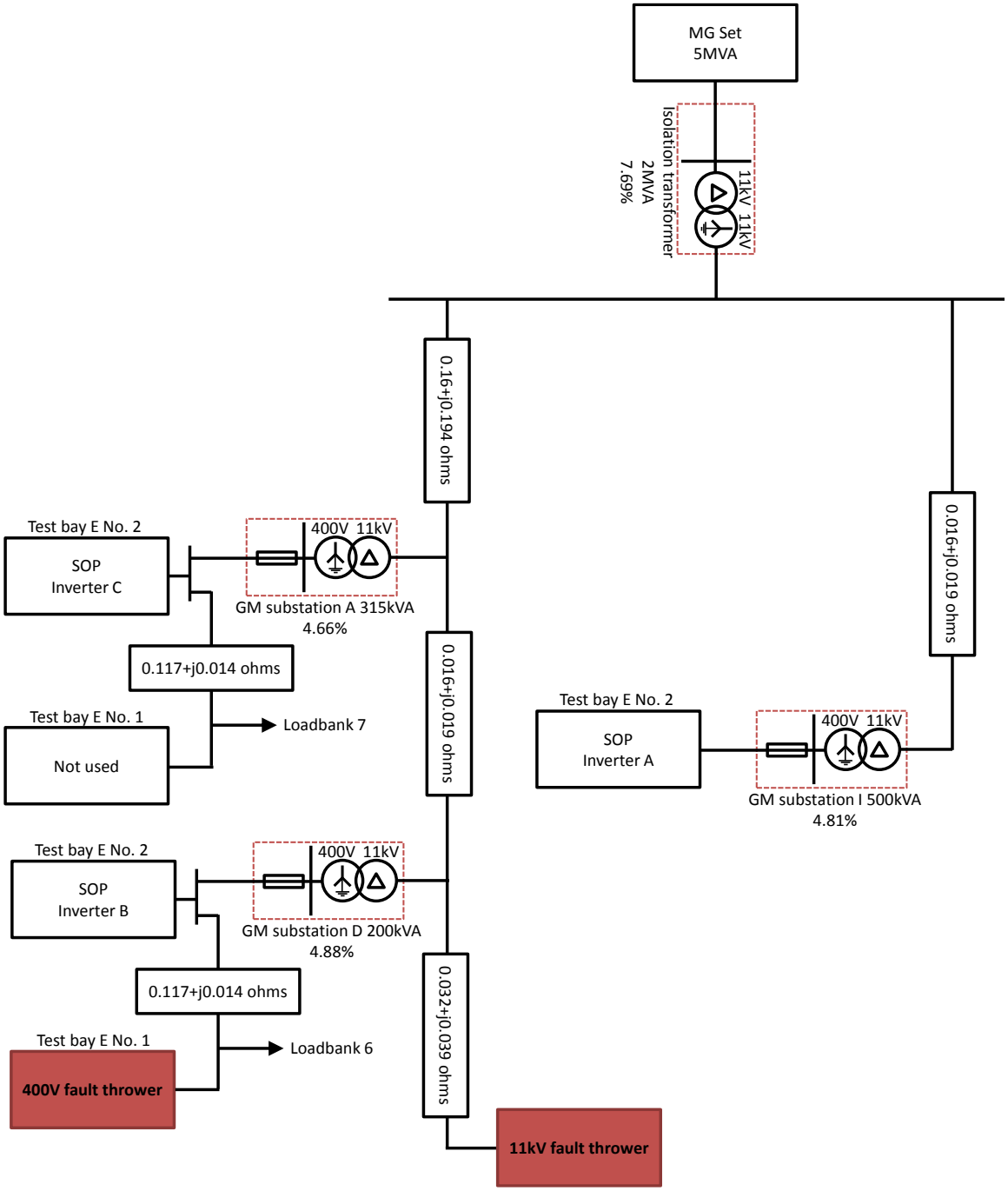


Figure 73: Network configuration for frequency, 400 V and 11kV fault test

TPS have advised that when the SOP leaves an 'allowed' frequency band it will enter an 'inhibited' mode and stop operation. When the SOP re-enters the 'allowed' frequency band it will begin normal operation without outside intervention. The inhibit mode is also indicated as a state '3' on the status tab of the SOP HMI (please note, this is a state indicator and is not related to the bands indicated in Table 6). In the test, an inhibit state is indicated by the recorded phase current decreasing to 0 A. TPS have advised on the frequency protection thresholds as shown in Table 6.

Table 6: Over/under frequency protection settings

Type of protection	Band	Frequency level (Hz)	Inhibit time delay
Over frequency	1	50.5Hz	1 minute
Under frequency	1	49.5Hz	1 minute
Over frequency	2	52Hz	10 ms
Under frequency	2	47.5Hz	10 ms

TPS have also advised that there is a 1 Hz hysteresis setting on the band 2 thresholds. This is clearer if explained in the context of an example: if the frequency exceeds 52 Hz continuously for 10 ms the SOP will enter the inhibit mode. If the frequency then falls to 51.5 Hz the SOP will remain in inhibit mode due to the 1 Hz hysteresis. If the frequency falls to 50.8 Hz within 1 min of breaching the 50.5 Hz band 1 threshold the SOP will not leave the inhibit state until the 1 minute time delay is complete. The SOP will then enter an inhibit state when the 1 min interval is over (band 1 protection). There is also a 5 s delay on the reset. So if the frequency then falls to 50.3 Hz (which is within the 'allowed' frequency band) there will be a 5 s delay before the SOP leaves the inhibit mode.

There are five protection elements within the fault test (numbered as shown in Figure 74):

1. The SOP has software based protection with the following settings (provided by TPS):
    a. Grid current protection:
        i. Long: 575 A rms for 8.1 s, 10 s reset when the fault has cleared.
        ii. Short: 957 A rms for 450 ms, 10 s reset when the fault has cleared.
        iii. Immediate: 1496 A rms for 5 ms, 10 s reset when the fault has cleared.
    b. Internal Inductor Protection – 650 A rms for 5 ms, 5 s reset when the fault has cleared.
    c. DC link Protection – 200 A, with a 1 ms trip and a 5 s reset.
2. The SOP also has CB protection (provided by TPS) – setting listed in Appendix B.
3. Substation D has 80 A J Type Fuse protection on all phases
4. The fault thrower has Schneider Electric NSX Micrologic trip CB protection with the following settings:
    a. Long time protection: $I_{pick\text{-}up}$=300 A and time setting=1 s.
    b. Short time protection: $I_{pick\text{-}up}$=2500 A and time settings=0 s (instantaneous).
    c. Instantaneous protection: $I_{pick\text{-}up}$=4800 A.
5. The fault thrower has a contactor with a time delay setting of 1 s. The contactor makes the fault connection and will automatically open after 1 s regardless of the fault being cleared.

The observed operation of the protection during the test (in order) was: (1) SOP software based protection operates to limit the fault current contribution of the SOP, (3) fuse protection operates to isolate substation D and (5) contactor opens to isolate the fault. Neither (2) SOP CB protection nor (4) fault thrower CB protection were observed to operate on overcurrent protection. Prior to each fault the inverter was controlled (via the HMI) to inject: (1) Inverter B export +32 kW and +24 kVAr and (2) Inverter C export +32 kW and +24 kVAr.

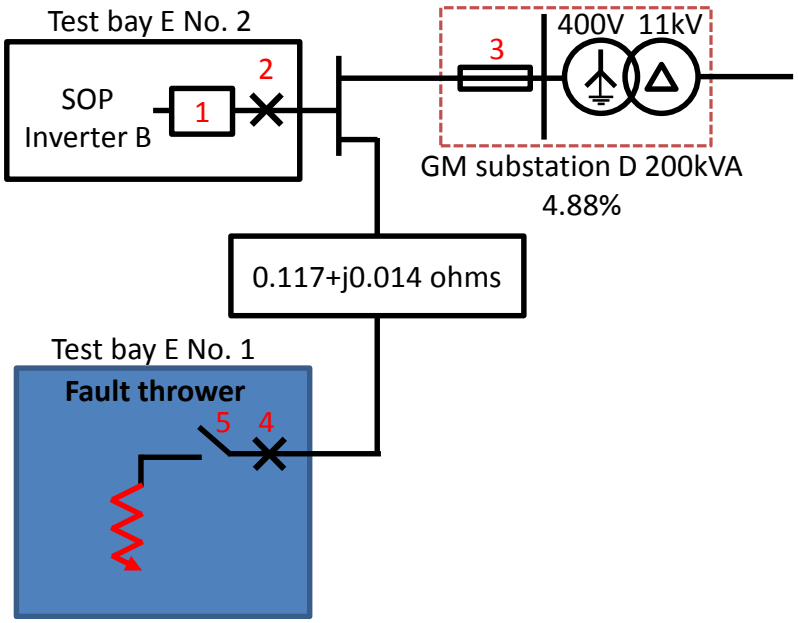


Figure 74: Fault thrower protection operation

4.10.2 Results and Analysis

4.10.2.1 Frequency test

Figure 75 shows test plan steps 1-3. The frequency is shown in the y-axis on the left hand side and inverter A phase A voltage and current are shown on the y-axis on the right hand side. The other phases have been omitted from the graph as the response is balanced across all three phases. The other inverter responses have also been omitted from the graph as they match the response of inverter A (the same frequency is applied to all inverters simultaneously during this test).

1. The SOP was enabled (see introduction of section 3 for explanation) and using the SOP HMI inverter B and inverter C were set to:
    a. Inverter B export +32 kW and +24kVAr (from 0 kW and 0kVAr in one step).
    b. Inverter C export +32 kW and +24kVAr (from 0 kW and 0kVAr in one step).
2. The frequency is then decreased to 49.7 Hz and the SOP was observed to not enter an inhibit state over a three minute period. This is expected behaviour from the SOP frequency protection.
3. The frequency is then decreased to 49.3 Hz and the SOP did not enter an inhibit state after one minute. This is unexpected behaviour, based on the frequency protection settings when the frequency is decreased below the 49.5 Hz threshold the SOP should enter an inhibit state after one minute of the threshold being breeched. In the graph, an inhibit state is indicated by the recorded phase current decreasing to 0 A.
4. In order to test the band 1 under frequency protection the frequency was then decreased further to 49Hz. After one minute (frequency decreased at 10:27:57 and inhibit state entered at 10:28:58), the SOP entered an inhibit state indicated by the current output decreasing to 0 A. This is the expected time delay from the frequency protection when the SOP falls below the band 1 threshold.
5. The frequency was then increased to 49.7 Hz and the SOP remained within the inhibit state for over 1 minute. This is unexpected behaviour, based on the frequency protection when the frequency increases beyond the 49.5 Hz threshold the SOP should leave the inhibit state after a 5 s delay.
6. In order to test the band 1 stage of the under frequency protection the frequency was then increased further to 50 Hz. After 25 s the SOP left the inhibit state as indicated by the current

output increasing from 0 A to 96 A. This is a slower response than expected, based on the frequency protection settings when the frequency increases beyond the 49.5Hz threshold the SOP should leave the inhibit state after a 5 s delay.

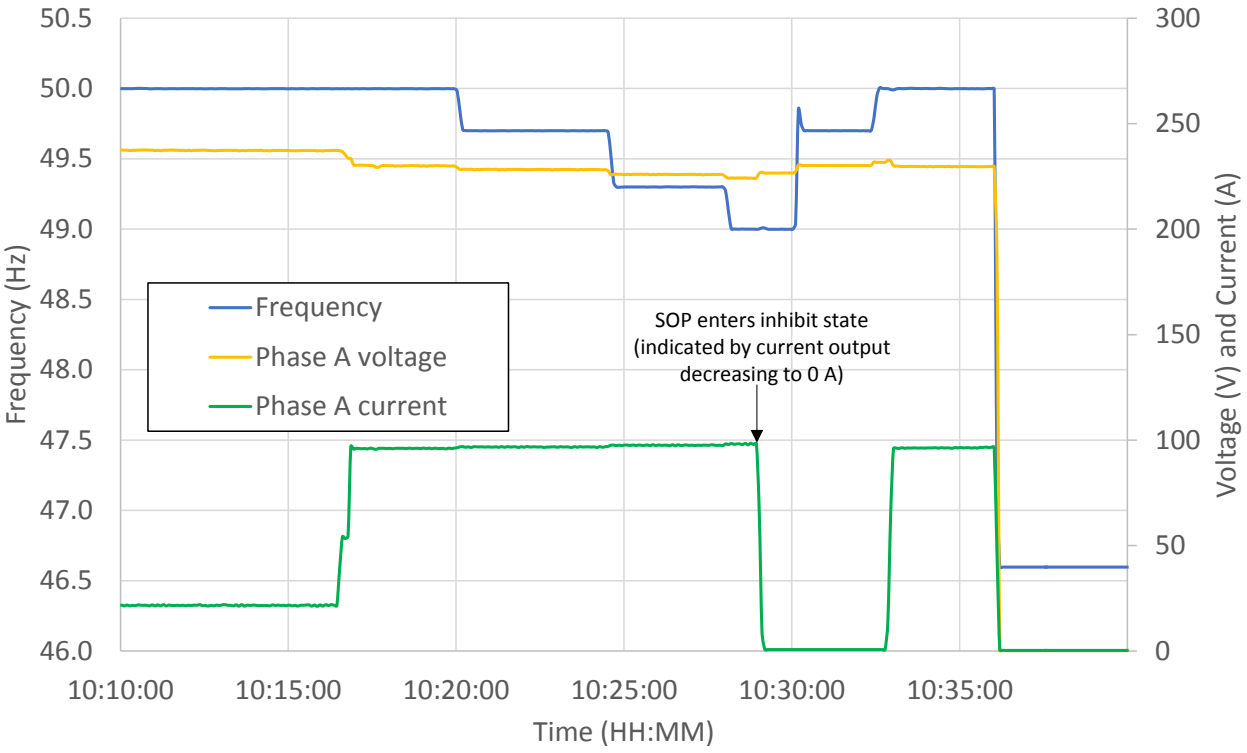


Figure 75: Frequency test part 1 - Inverter A phase A RMS current, phase A RMS voltage and network frequency

7. Figure 76 shows the remaining test plan steps. Please note each step is indicated on the graph with its corresponding number e.g. the step '8' is shown on the bottom of the graph as [8]. The next stage in this test was to evaluate the band 2 under frequency protection by decreasing the frequency to 47.3 Hz. When the frequency was reduced to this level it caused the undervoltage protection in the primary substation of the PNDC network to operate to isolate the network. To work around this protection setting the network voltage was increased from 230 V to 240 V.
8. The frequency was then decreased to 47.3 Hz and the SOP entered an inhibit state in less than 1 s. This is the expected operation and time delay for band 2 under frequency protection.
9. The frequency was then increased to 50 Hz and the SOP exited the inhibit state within approximately 30 s. Please note: the test plan specifies that for this step the network frequency should be increased to 49.7 Hz instead of 50 Hz but because of the error on the thresholds (observed in the earlier under frequency part of this test) the decision was made to increase the frequency to 50 Hz to observed the SOP exiting the inhibit state. Again, this is unexpected behaviour, based on the frequency protection when the frequency enters the allowed zone (i.e. greater than 49.5 Hz) the SOP should leave the inhibit state after a 5 s delay.
10. The next stage of the test was to evaluate the over frequency protection. The frequency was increased to 50.3 Hz and the SOP was observed to not enter an inhibit state over a three minute period. This is the expected response from the SOP over frequency protection.
11. The frequency was then increased to 50.7 Hz and the SOP was observed to not enter an inhibit state over a one minute period. This is unexpected behaviour, based on the frequency protection when the frequency increases above the 50.5 Hz threshold the SOP should enter an inhibit state after one minute of the threshold being exceeded.

12. In order to test the band 1 over frequency protection the frequency was then increased further to 51 Hz. After less than one minute (approximately 37 s), the SOP entered an inhibit state indicated by the current output decreasing to 0 A. This is the correction operation of the over frequency protection when the SOP exceeds the band 1 frequency protection threshold, however, the protection has operated faster than the 1 minute specified in the protection settings.
13. The frequency was then decreased to 50 Hz and the SOP was observed to exit the inhibit state within one minute (approximately 35 s). This is the expected response from the SOP over frequency protection, however, the time delay is longer than expected as the SOP should leave the inhibit state after a 5 s delay when the frequency enters the allowed zone (i.e. less than 50.5 Hz). Please note: the test plan specifies that for this step the network frequency should be decreased to 50.3 Hz instead of 50 Hz but because of the tolerance on the threshold (observed earlier in this test) the decision was made to decrease the frequency to 50 Hz to observe the SOP exiting the inhibit state.
14. The frequency was then increased to 51.9 Hz (with an overshoot of 52.3 Hz) and the SOP was observed to enter the inhibit state within 1 s. This is the expected response from the SOP over frequency protection when the band 2 over frequency threshold is exceeded.
15. To confirm that the SOP over frequency protection would operate for the increase of frequency to 51.9 Hz and the cause of the over frequency protection operation was not the 52.3 Hz overshoot the test was repeated with a ramped increase from 50 Hz to 51.9 Hz, again the SOP was observed to enter the inhibit state in less than 1 s.
16. Please note: test plan steps 13 and 14 were not tested. It was agreed with UKPN and TPS that there would be no useful learning achieved by repeating the band 2 over frequency test with a final higher frequency when it had already been established that the SOP would enter an inhibit state at 51.9 Hz.

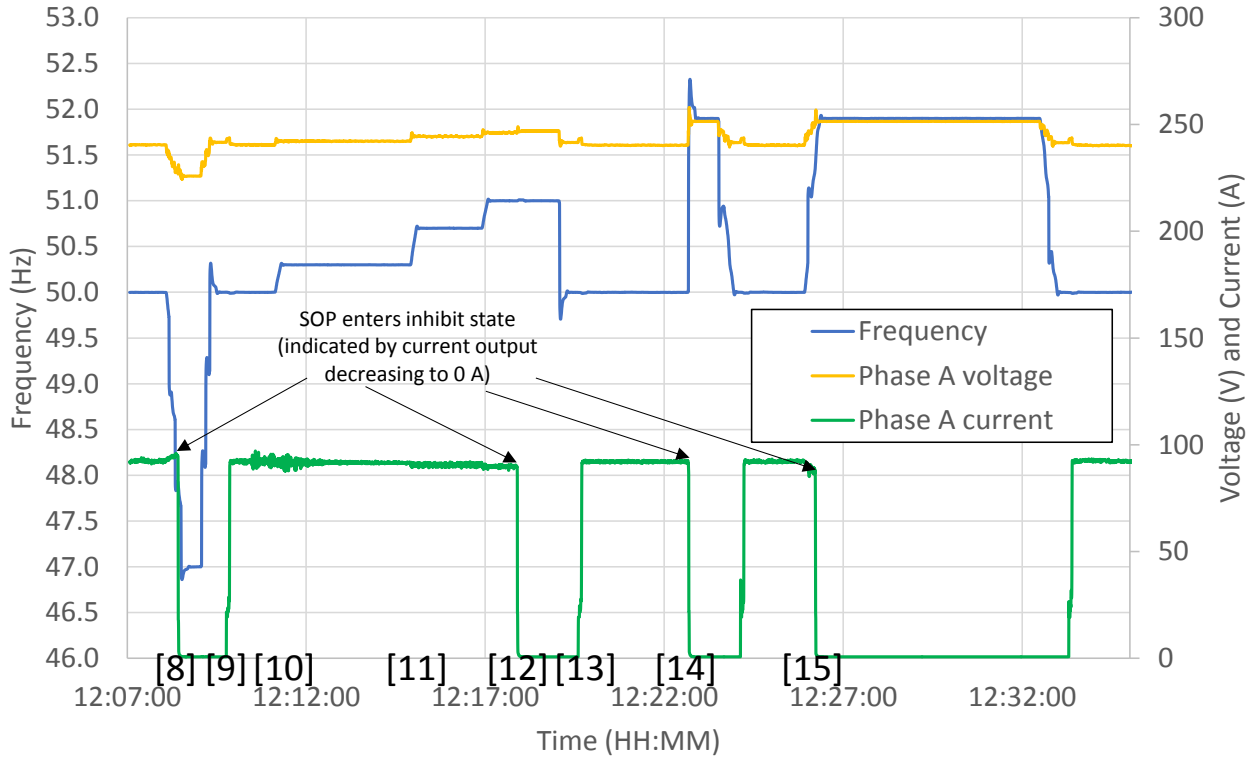


Figure 76: Frequency test part 2 - Inverter A phase A RMS current, phase A RMS voltage and network frequency

4.10.2.2 Single phase to earth fault

Prior to applying the fault, using the SOP HMI inverter B and inverter C were set to:

a) Inverter B export +32 kW and +24kVAr (from 0 kW and 0kVAr in one step).
b) Inverter C export +32 kW and +24kVAr (from 0 kW and 0kVAr in one step).

The voltage waveform recorded at inverter B during the Phase A to earth fault is shown in Figure 77 and the current waveform is shown in Figure 78. The fault is applied at approximately 13:15:53.551 and the SOP stops injecting current at 13:15:53.591. Within 40ms the SOP has detected the fault and limited its output current.

The phase A RMS voltage on inverter A and C during the fault is shown in Figure 79 and the phase A RMS current is shown in Figure 80. From Figure 79 the fault can be observed as a voltage spike. From Figure 80 it can be observed that the SOP stops injecting current on inverter A and inverter C when the fault is applied.

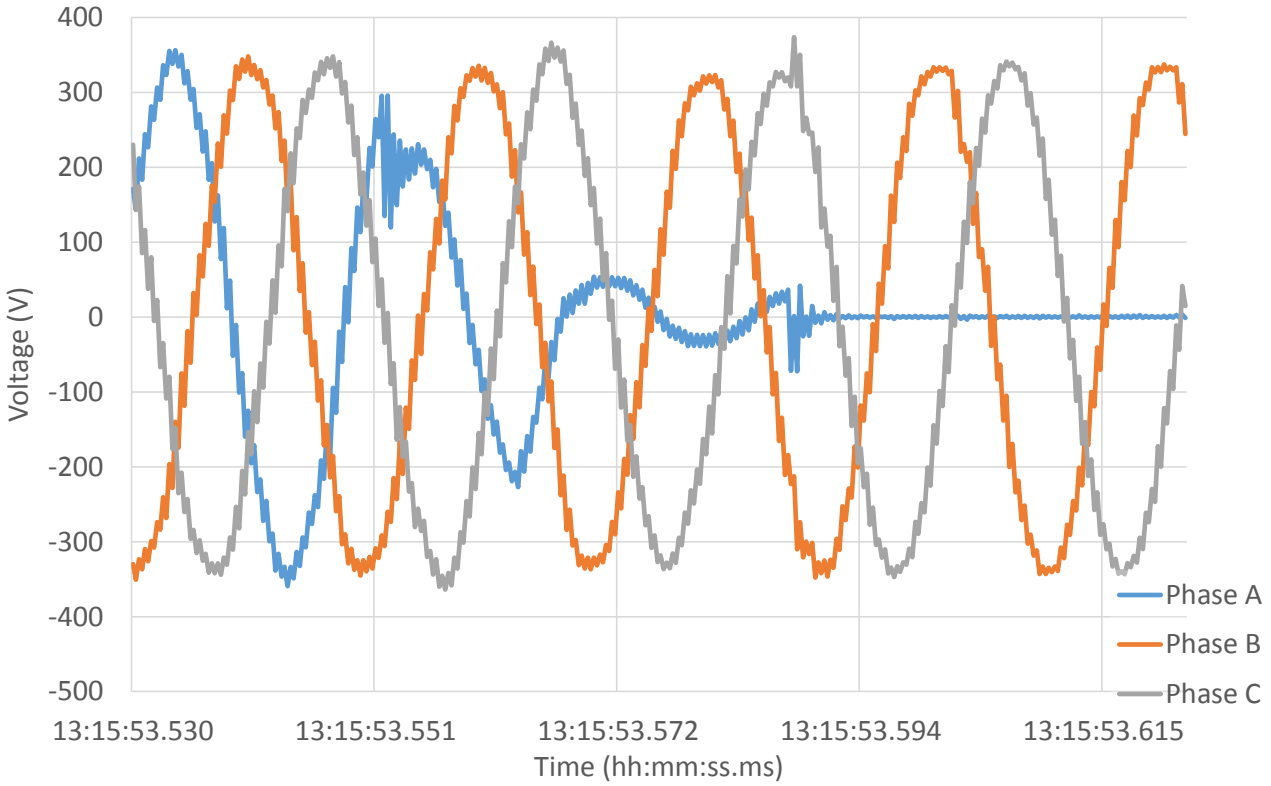


Figure 77: Phase A to Earth Fault – voltage measured at inverter B terminals

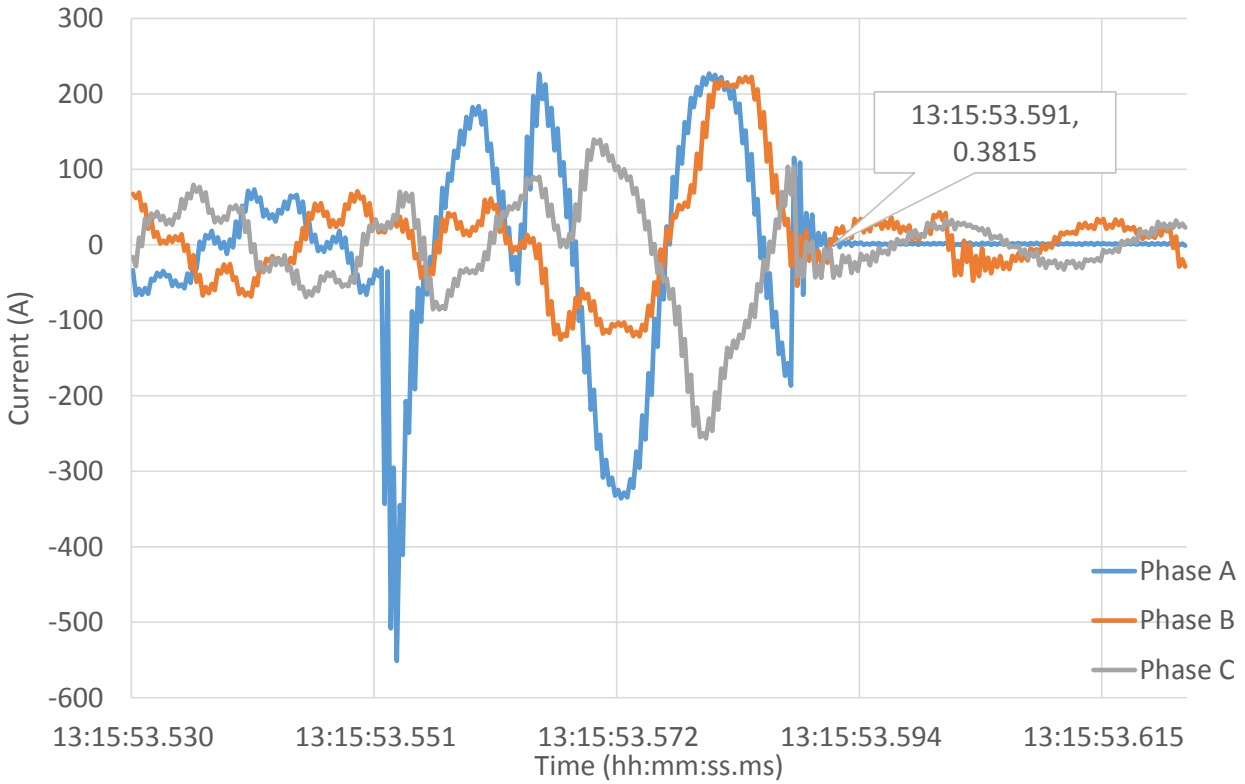


Figure 78: Phase A to Earth Fault – current measured at inverter B terminals

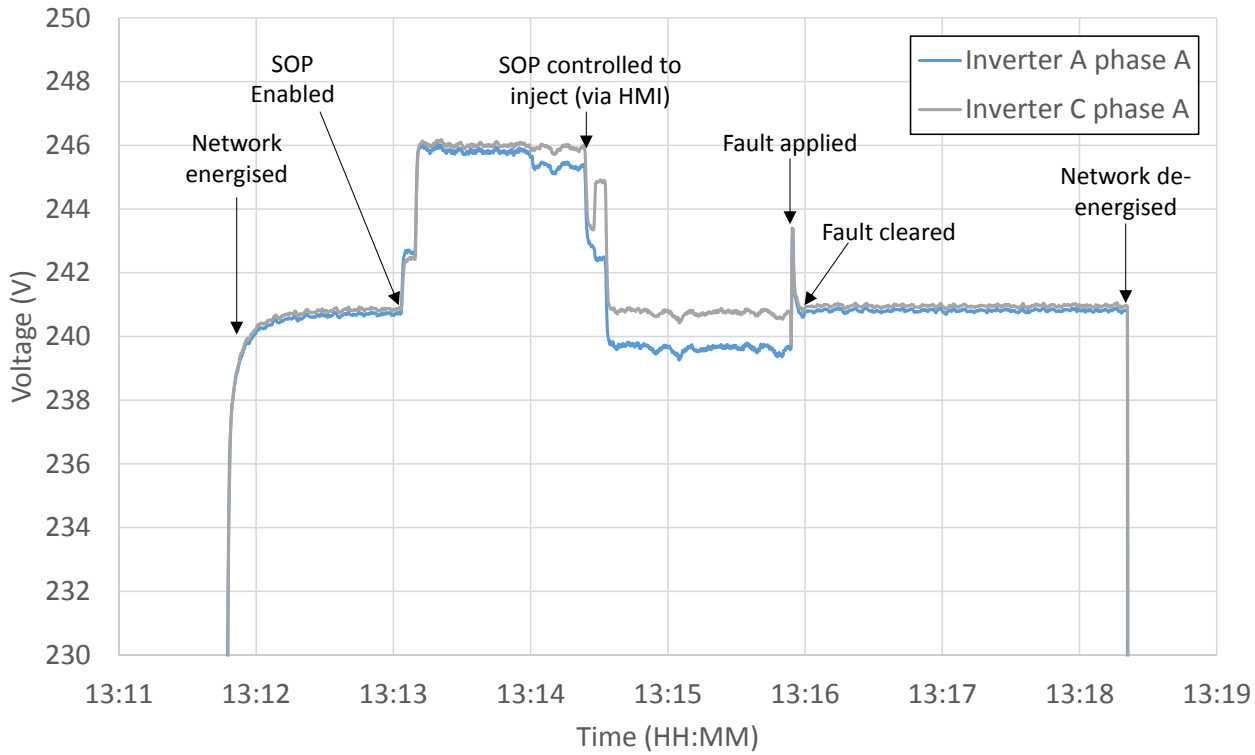


Figure 79: Phase A to earth fault – phase A RMS voltage measured at inverter A and inverter C terminals

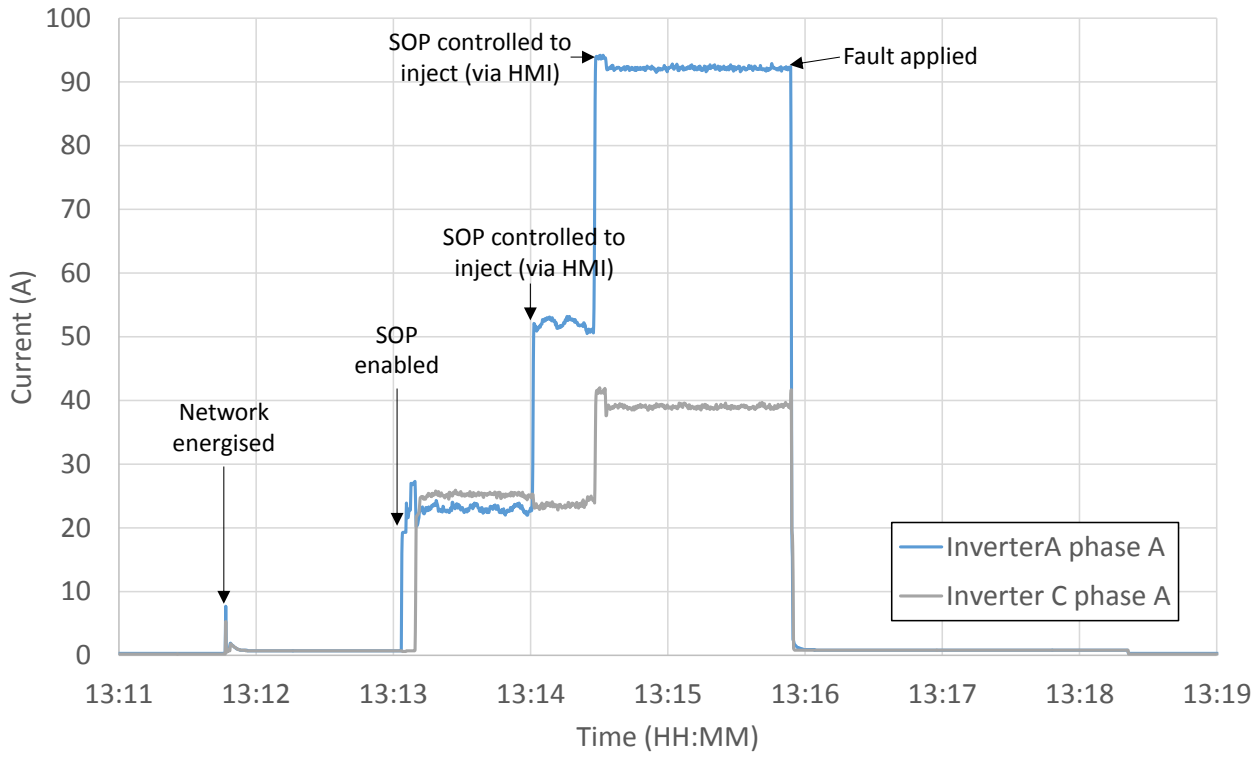


Figure 80: Phase A to Earth Fault – phase A RMS current measured at inverter A and inverter C terminals

4.10.2.3 Phase to phase fault

Prior to applying the fault, using the SOP HMI inverter B and inverter C were set to:

a) Inverter B export +32 kW and +24 kVAr (from 0 kW and 0 kVAr in one step).
b) Inverter C export +32 kW and +24 kVAr (from 0 kW and 0 kVAr in one step).

The voltage waveform recorded at inverter B during the phase A to phase 3 fault is shown in Figure 81 and the current waveform is shown in Figure 82. The fault is applied at approximately 13:43:37.980 and the SOP stops injecting current at 13:43:38.024. Within 44 ms the SOP has detected the fault and limited its output current.

The phase A RMS voltage on inverter A and C during the fault is shown in Figure 83 and the phase A RMS current is shown in Figure 84. As in the single phase to earth fault test the fault can be observed as a voltage spike in Figure 83. From Figure 84 it can be observed that the SOP stops injecting current on inverter A and inverter C when the fault is applied.

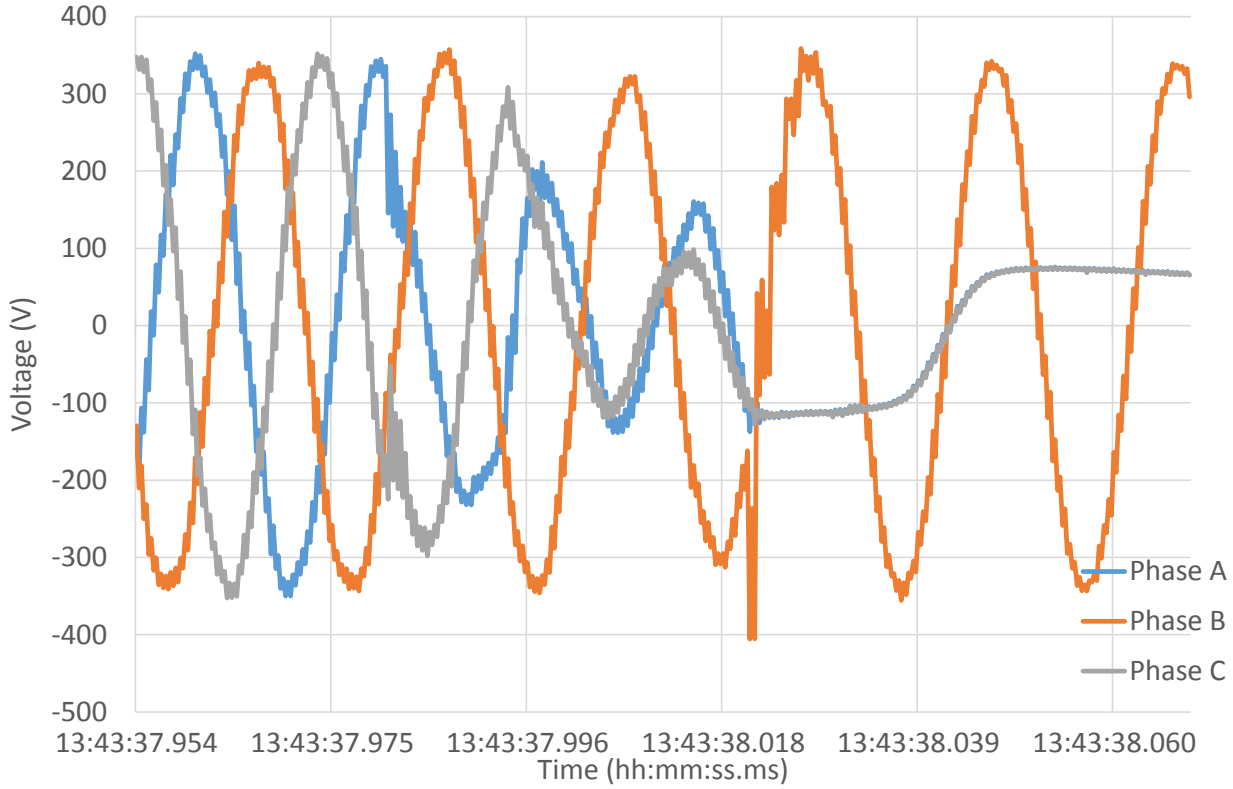


Figure 81: Phase A to Phase 3 fault – voltage measured at inverter B terminals

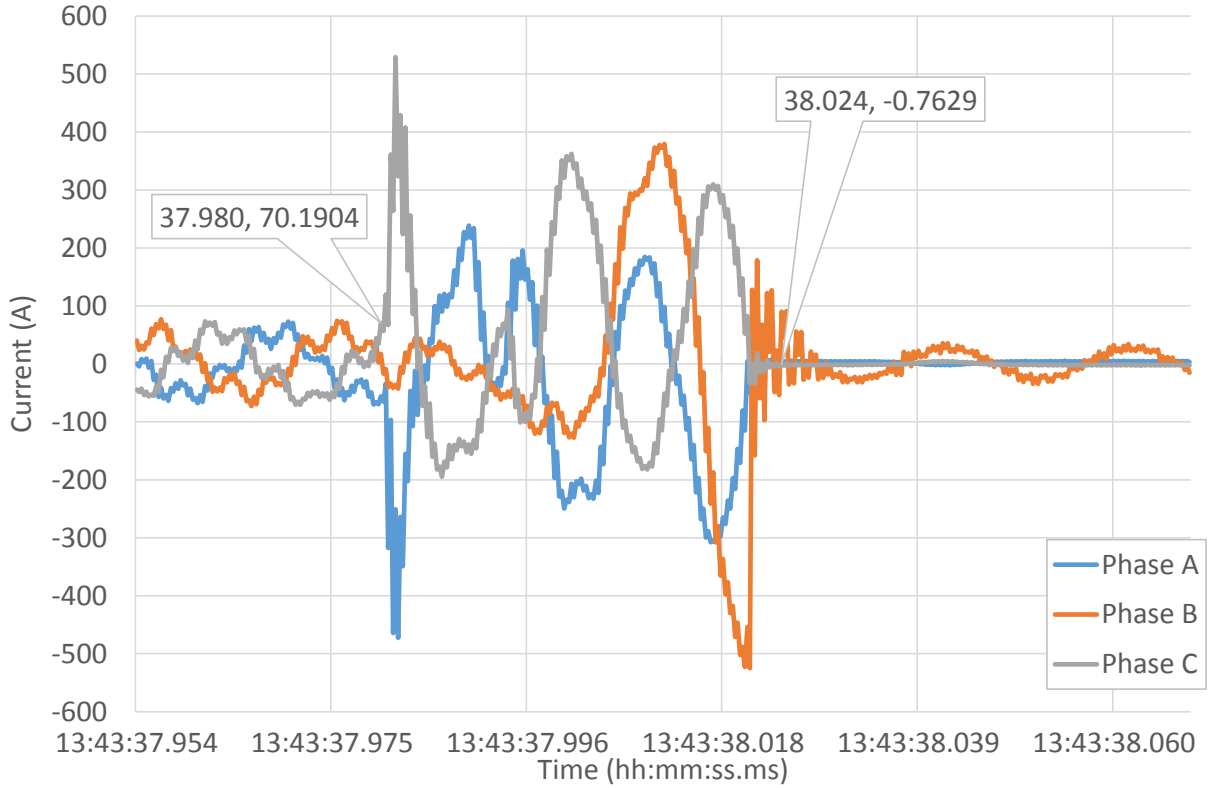


Figure 82: Phase A to Phase 3 fault – current measured at inverter B terminals

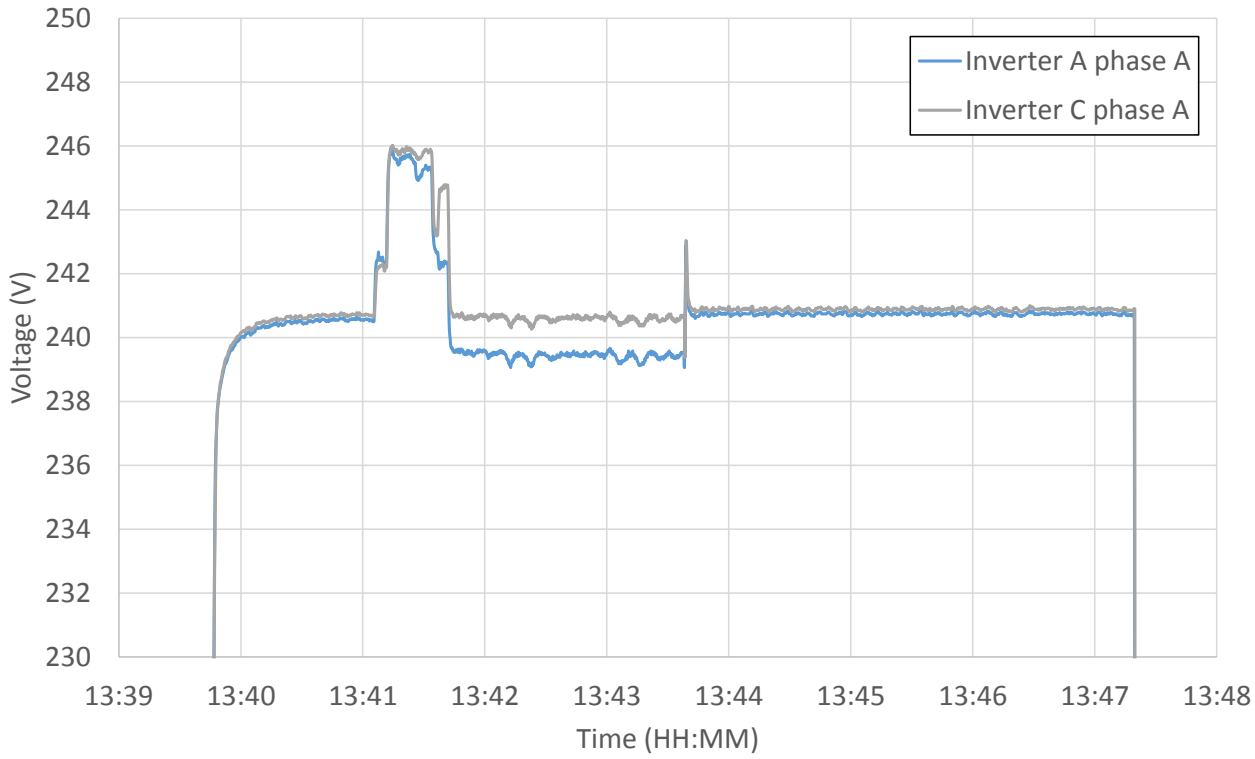


Figure 83: Phase A to Phase 3 fault – phase A RMS voltage measured at inverter A and inverter C terminals

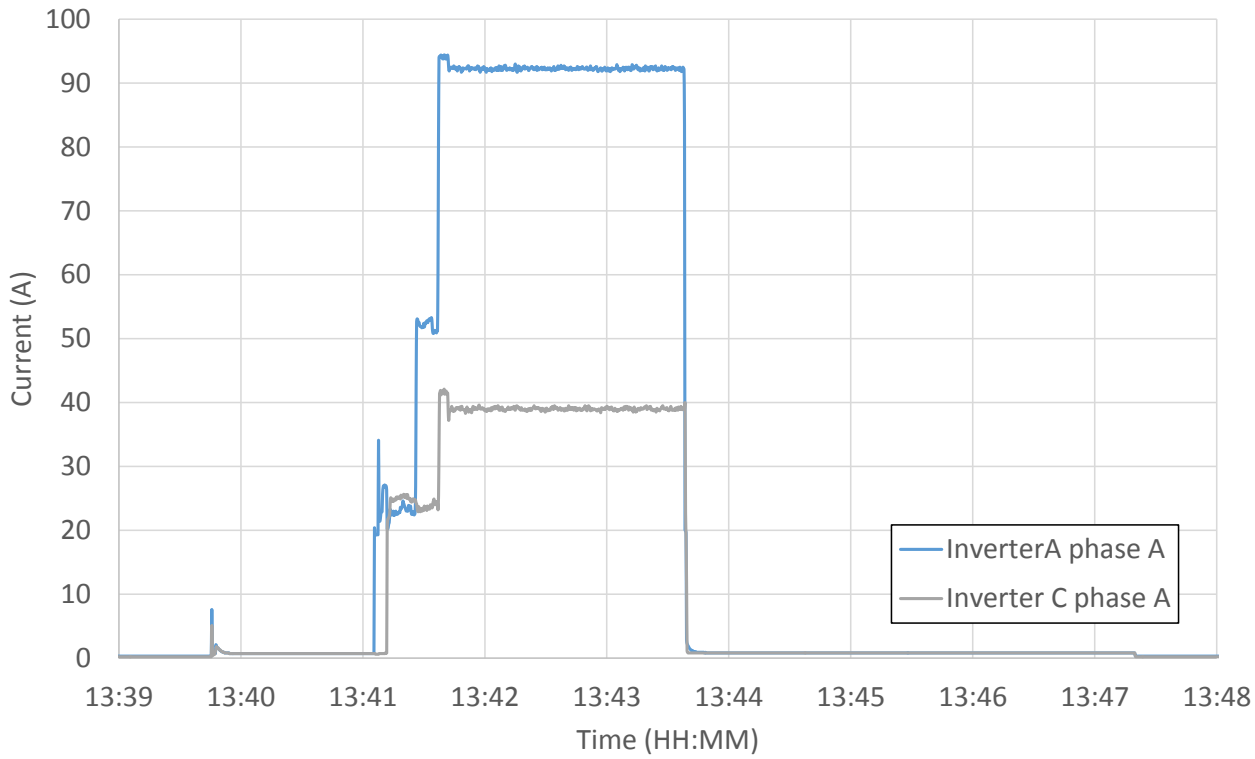


Figure 84: Phase A to Phase 3 fault – phase A current and voltage measured at inverter A and inverter C terminals

4.10.2.4 Three phase fault

Prior to applying the fault, using the SOP HMI inverter B and inverter C were set to:

a) Inverter B export +32 kW and +24kVAr (from 0 kW and 0 kVAr in one step).
b) Inverter C export +32 kW and +24kVAr (from 0 kW and 0 kVAr in one step).

The voltage waveform recorded at inverter B during the three phase fault is shown in Figure 85 and the current waveform is shown in Figure 86. The fault is applied at approximately 14:19:04.523 and the SOP stops injecting current at 14:19:04.541. Within 18ms the SOP has detected the fault and limited its output current.

The phase A RMS voltage on inverter A and C during the fault is shown in Figure 87 and the phase A RMS current is shown in Figure 88. As in the previous fault test the fault can be observed as a voltage spike in Figure 87. From Figure 84 it can be observed that the SOP stops injecting current on inverter A and inverter C when the fault is applied.

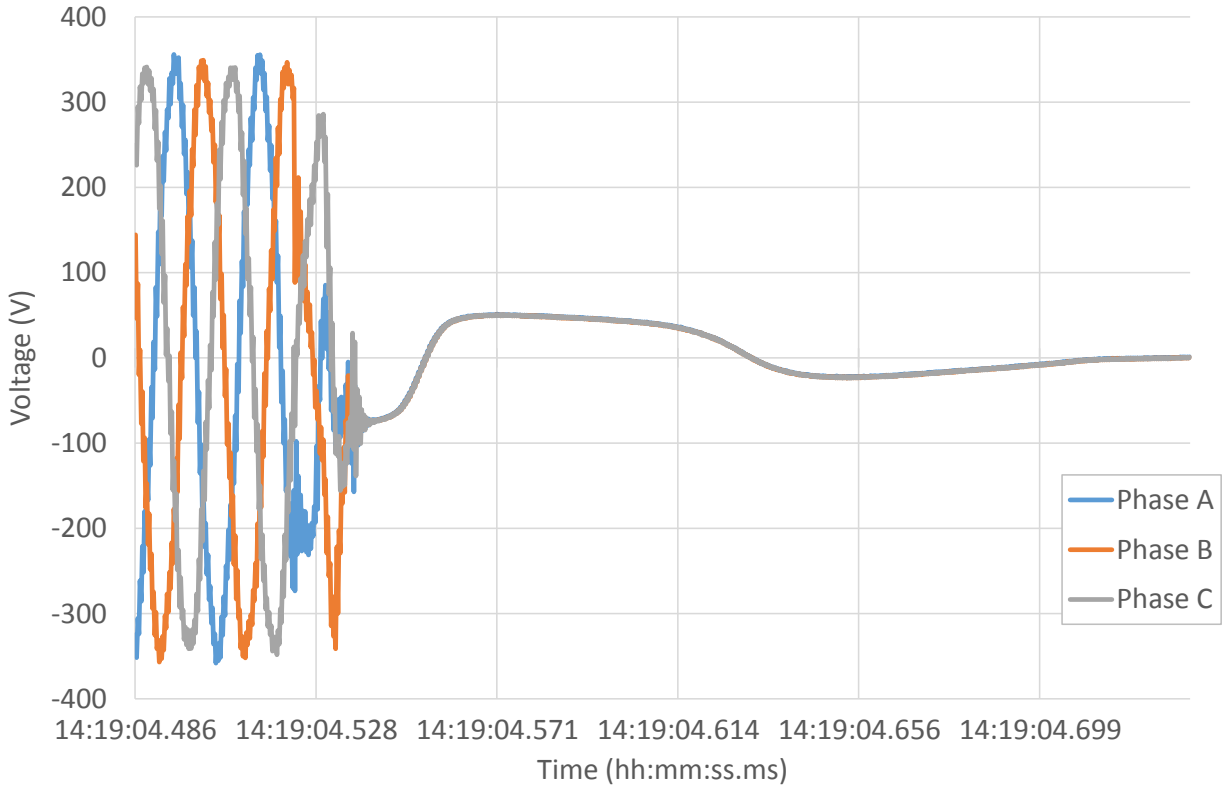


Figure 85: Three phase fault – voltage measured at inverter B terminals

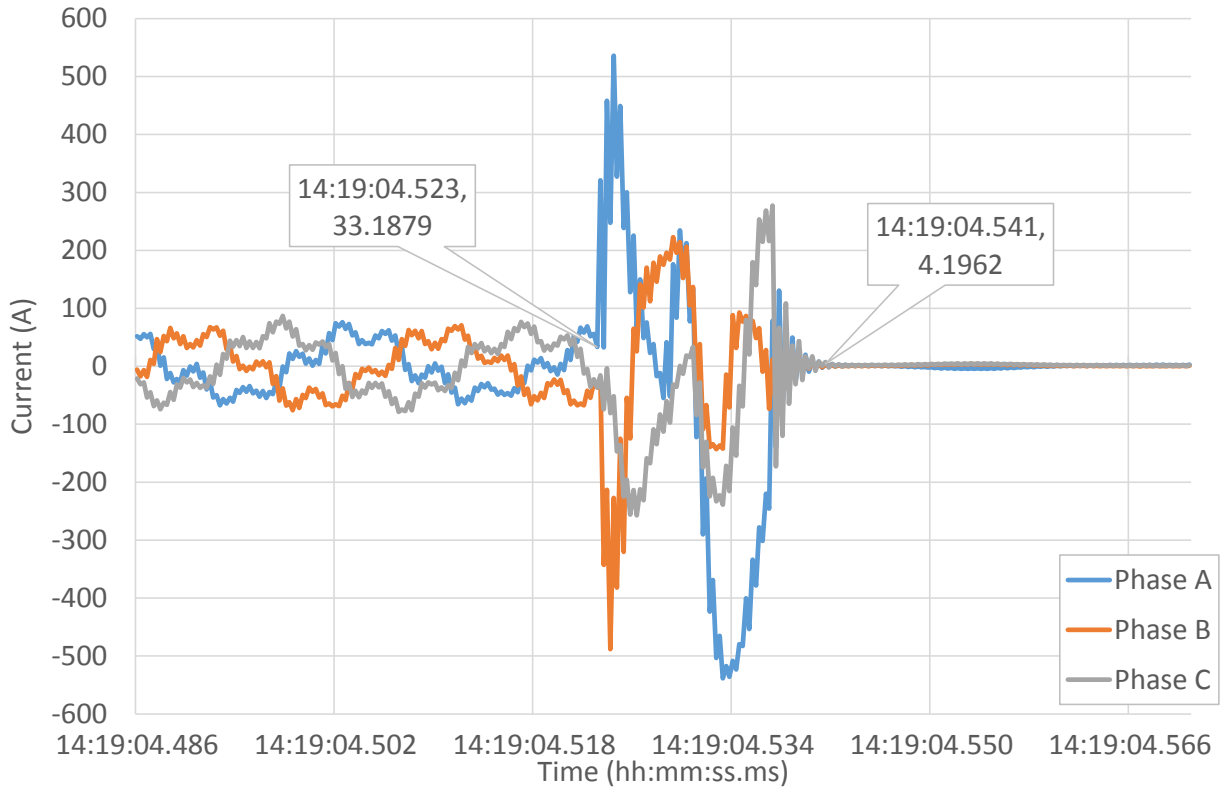


Figure 86: Three phase fault – current measured at inverter B terminals

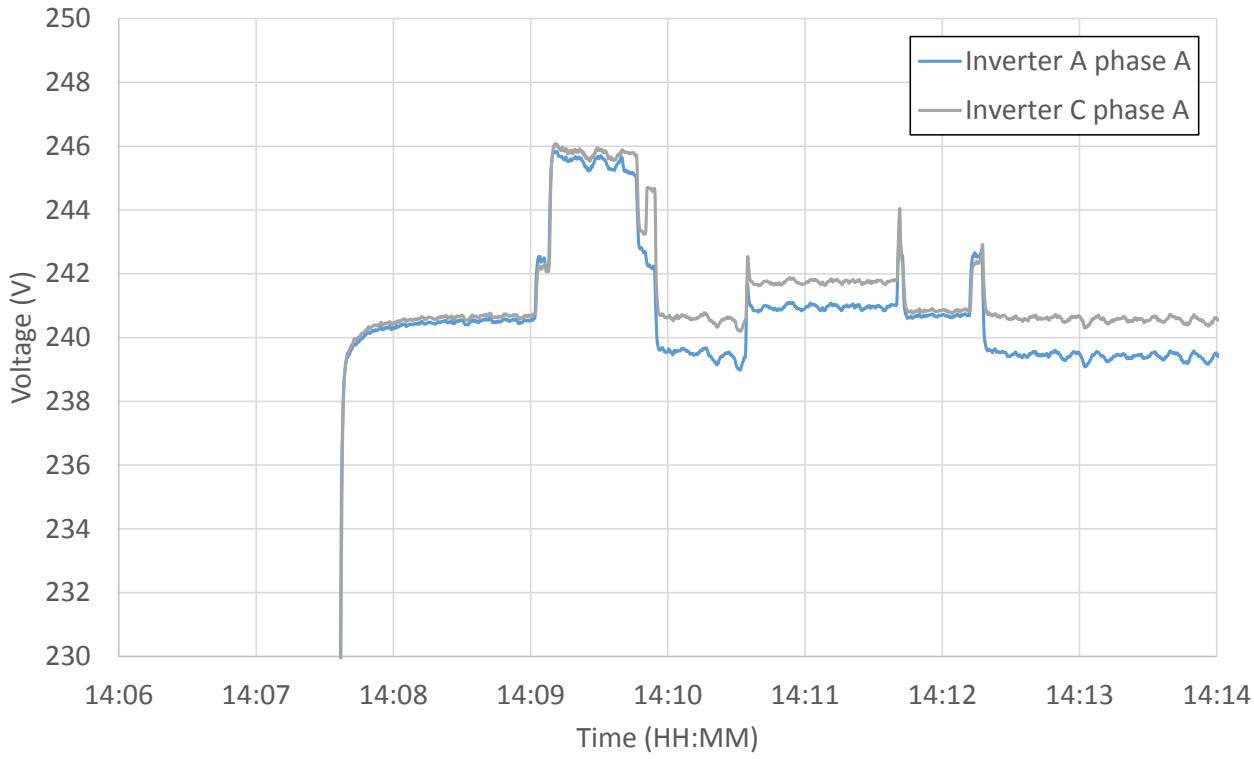


Figure 87: Three phase fault – phase A RMS voltage measured at inverter A and inverter C terminals

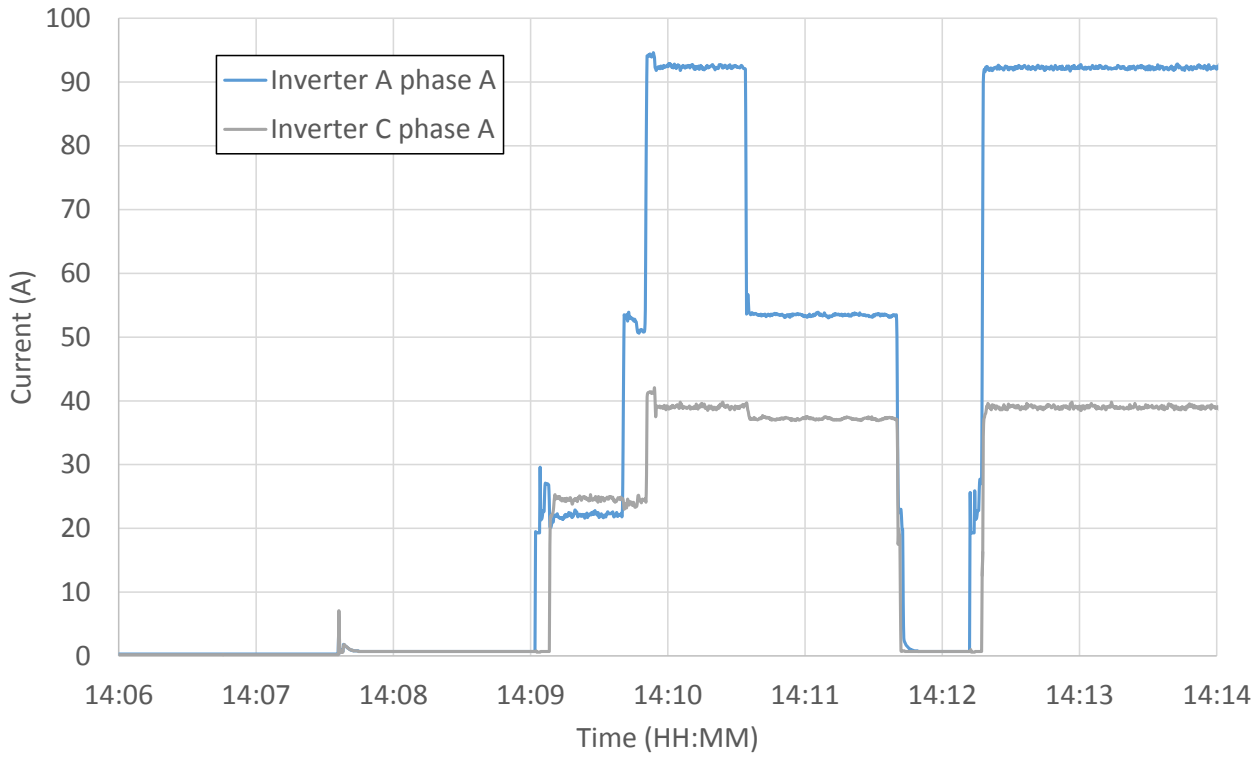


Figure 88: Three phase fault – phase A RMS voltage measured at inverter A and inverter C terminals

4.10.2.5 11 kV single phase to earth fault test

The final part of this test was to apply a single phase to earth fault on the 11 kV network and observe the fault response of the SOP. The voltage and current waveforms recorded at each of the SOP inverters is shown from Figure 89 to Figure 94. Please note the time difference between the different inverter plots is due to synchronisation error between the FLUKE Power Quality Analyser 435-II monitoring units.

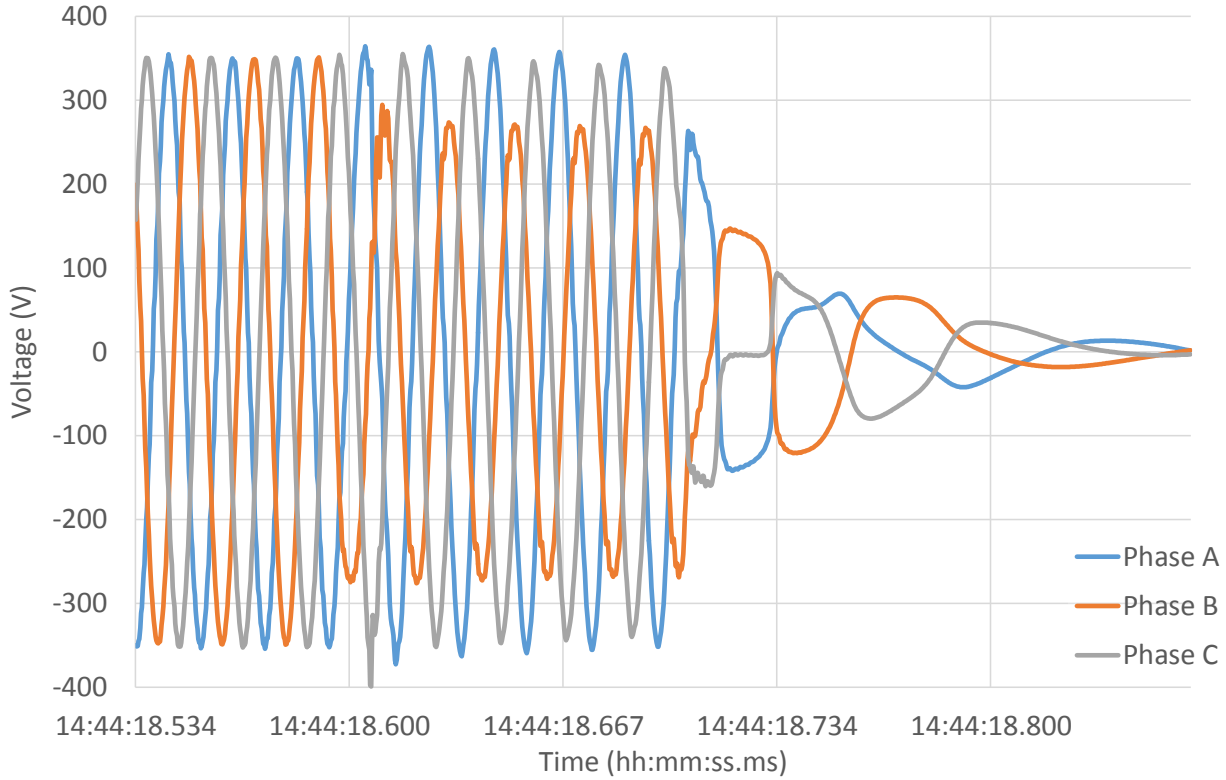


Figure 89: 11 kV phase A to Earth Fault – voltage measured at inverter A terminals

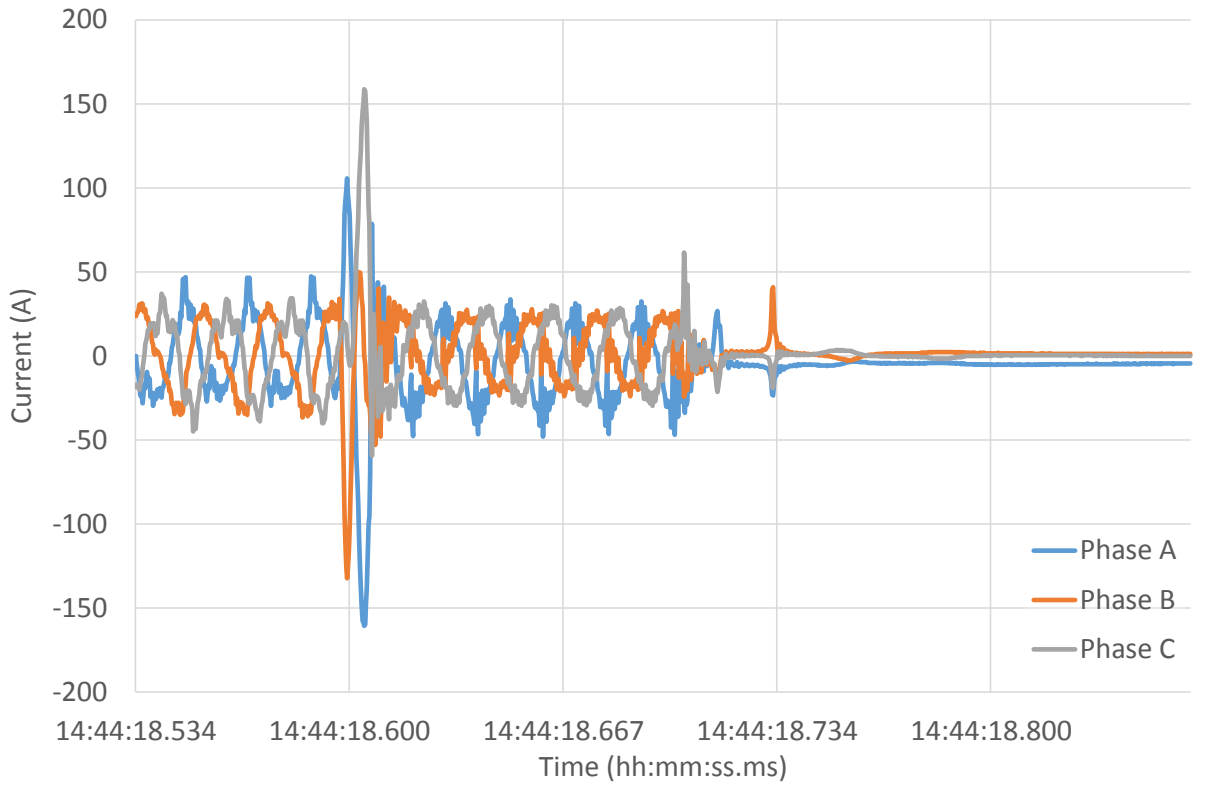


Figure 90: 11 kV phase A to Earth Fault – current measured at inverter A terminals

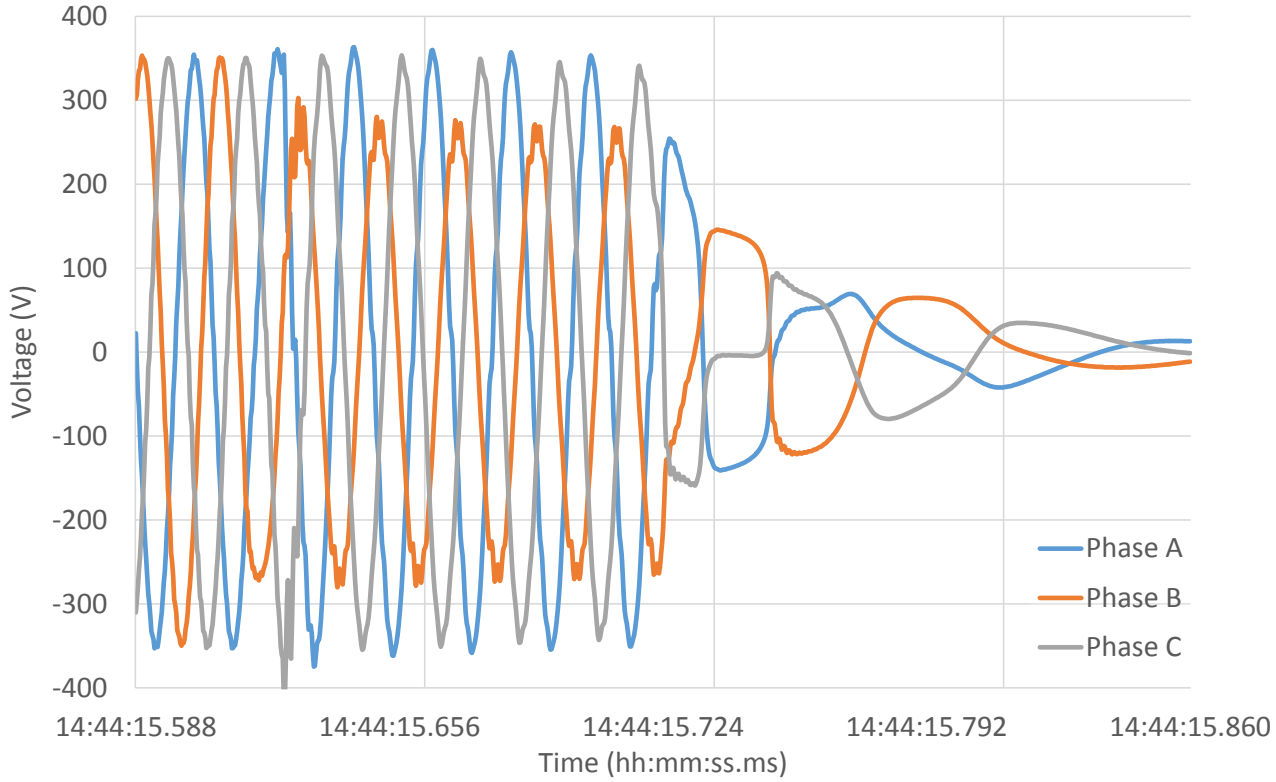


Figure 91: 11 kV phase A to Earth Fault – voltage measured at inverter B terminals

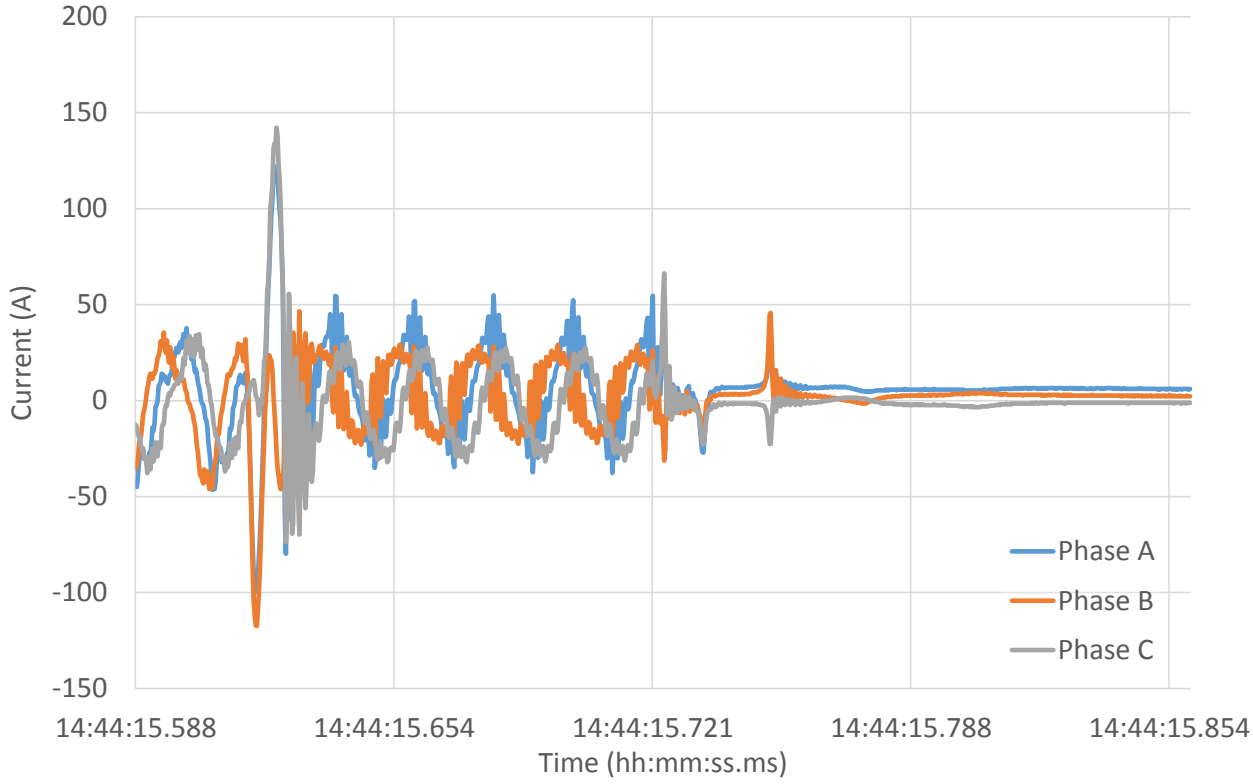


Figure 92: 11 kV phase A to Earth Fault – current measured at inverter B terminals

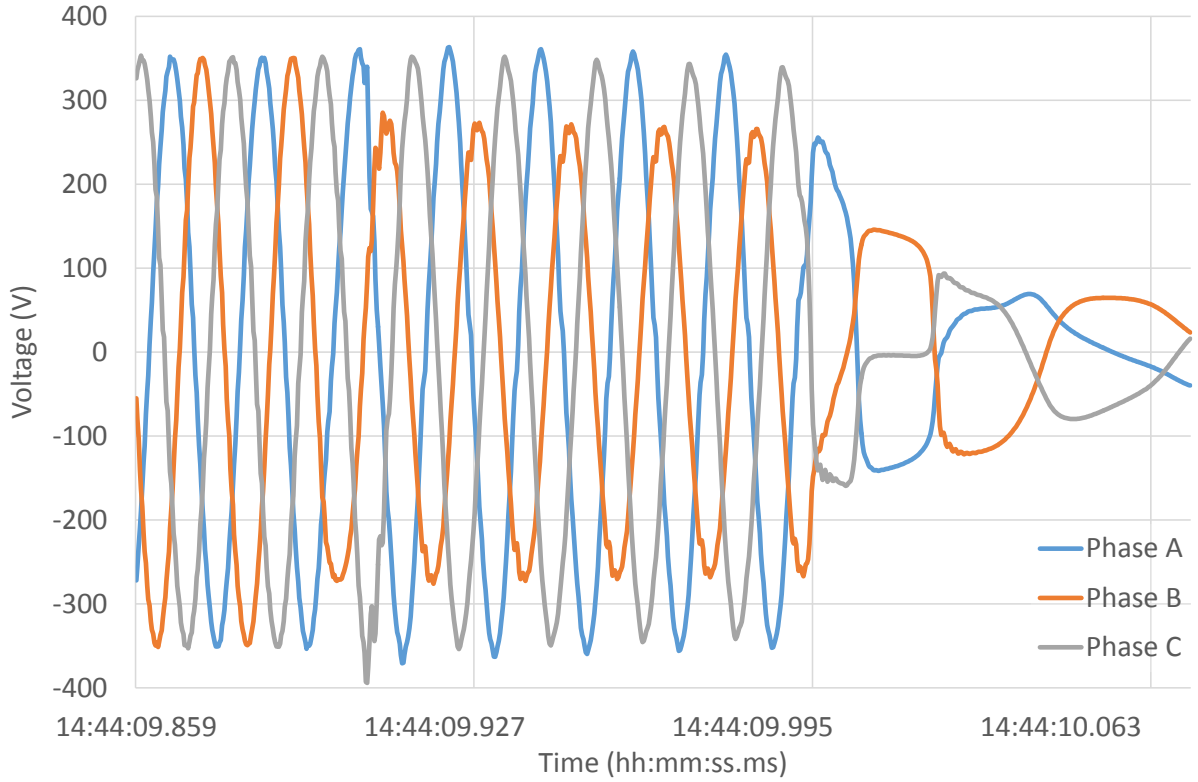


Figure 93: 11 kV phase A to Earth Fault – voltage measured at inverter C terminals

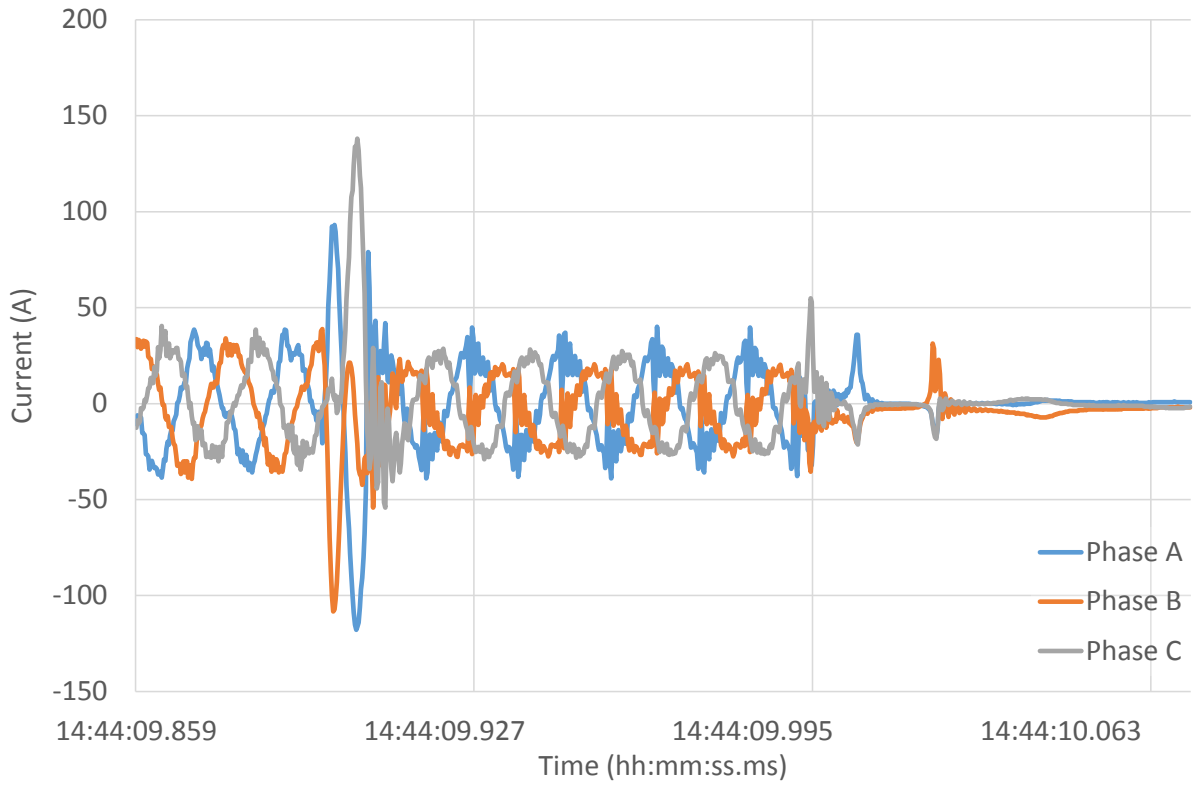


Figure 94: 11 kV phase A to Earth Fault – current measured at inverter C terminals

4.10.3 Conclusions

The frequency test has demonstrated that the SOP frequency protection will operate with a time delay when the frequency thresholds are breeched. It should be noted that the frequency thresholds at which the SOP

will operate do not match the frequency thresholds specified in the protection settings or in the test plan. It should also be noted that the time delay associated with the frequency thresholds specified in the protection settings do not match the time delays recorded in the test e.g. when the band 1 over frequency threshold was exceed the SOP should enter an inhibit state after 1 min delay but the SOP was recorded to operate after 37 s.

TPS have advised that the SOP phase locked loop (PLL) sample rate has been decreased since this test and it is probable that because of this change the SOP would operate closer to the frequency protection thresholds specified at the start of this section.

The fault test has demonstrated that when a fault is applied close to the terminals of the SOP the SOP reduces its output current on all inverters to approximately 0 A and for all of the faults tested (both at 400 V and 11 kV) the SOP did not output more than a 600 A per phase (instantaneous).

5 REPORT CONCLUSIONS AND SUMMARY

This exercise has shown that the SOP behaves as expected in much of the functional test cases. However, there are a number of areas where unexpected, or out-of-specification behaviour, was observed. The key areas where the SOP did not respond as expected are in the report summary table below. In many cases solutions have been proposed that could be incorporated into the next version of the SOP hardware or control algorithm.

Test dates	Report Section	Test Name	Pass	Significant observations	Comments on Pass status
12/02/2015	4.1	Balanced three phase load test	Y	1. Oscillations were observed in the power output from SOP. 2. Power import/export was recorded when the SOP was enabled (turned on) via the HMI. TPS have advised that this power transfer is related to the power requirements of the SOP to turn on and operate in a standby mode i.e. to supply power to the SOP LCL filters and power electronics without actively transferring power either due to manual (via HMI) or algorithm control.	This test evaluates the SOP's capability to transfer power from one terminal to another based on the HMI settings. The test results confirm that, when controlled to do so by the HMI, the SOP is capable of transferring three phase active power up to the limits tested.
13/02/2015	4.2	Load cycle test 1	Partial	1. As in the previous test, oscillations were observed in the power output from the SOP. 2. The SOP was observed to trip unexpectedly three times during the test.	This test evaluates the SOP's capability to supply there phase active power over an extended timescale. The SOP did supply power over the extended period however the SOP was noted to trip unexpectedly three times during the test. This test also evaluates the: audio noise generated by the SOP at different power outputs, the temperature the surface of the SOP reaches when supplying power over an extended period; and the EMF generated by the SOP at different power outputs. Temperature, audio noise and EMF were observed to comply with relevant standards and requirements.
16/02/2015	4.3	Load cycle test 2	Partial	1. The oscillations observed in the power output from the SOP in the previous test are no longer present. This is due to an update provided by TPS (voltage output limit on resonant controllers increased). 2. As in the previous test, the SOP was observed to trip unexpectedly four times during the test.	This test is a repeat of the previous load cycle test. Again, the SOP was observed to supply power over the extended period however the SOP was noted to trip unexpectedly four times during the test. Again, temperature, audio noise and EMF were observed to comply with relevant standards and requirements.

Test dates	Report Section	Test Name	Pass	Significant observations	Comments on Pass status
01/04/2015	4.4	Three phase reactive power support test	Y	1. Oscillations were observed in the power output from the SOP. The oscillation issue was later addressed via a further update from TPS to increase the upper limits on the resonant controllers and DC link voltage, both updates involved modifying the software on the SOP ICCs. 2. An offset between the HMI control setting and measured values was also observed.	This test evaluated the capability of the SOP to inject three phase reactive power. The test results confirm that the SOP is capable of injecting three phase reactive power up to +50 kVAr and -50 kVAr (while also exporting +126 kW) when controlled to do so via the HMI.
21/04/2015	4.5	Additional test: Repeat of EMF and audio measurements at increasing distances from SOP	Y	Audio noise exceeds limits specified by TPS.	Audio noise complies with Control of Noise at Work Regulations 2005 and EMF complies with 1998 ICNIRP exposure guidelines.

Test dates	Report Section	Test Name	Pass	Significant observations	Comments on Pass status
20/04/2015 and 21/04/2015	4.6	Phase unbalance improvement test	Y	1. The SOP was observed to trip unexpectedly when controlled to inject power at higher network voltages. 2. The SOP was observed to unexpectedly trip on neutral overcurrent protection during this test. 3. The SOP should have operated at a lower level of unbalance than it did in the test.	The first part of this test evaluated the SOP response after the TPS update. It was observed that with the update applied the SOP will operate at higher voltages without harmonics in the SOP power output (observed in earlier tests). However, the SOP was observed to trip out when the network phase voltage was set to 246 V and the SOP was controlled to inject active power. This is an area that may require further investigation as the SOP tripping out (as observed in this test) is likely to occur on networks where the voltage is being run in excess of 246 V. This second part of this test evaluated the SOP's ability to provide power to a single phase primarily resistive load. The SOP algorithm detects the unbalanced load by calculating the zero sequence voltage from the measured phase A, B and C voltages. If the zero sequence voltage exceeds a pre-set value (defined in the algorithm) the algorithm controls the SOP to transfer power to the load. The test results confirmed that the SOP will supply a single resistive phase load when the algorithm's zero sequence threshold is exceeded (which is interpreted as an unbalance load and therefore the SOP will try to address that by injecting current).
02/04/2015 and repeated 21/04/2015	4.7	Single phase reactive power support test	N	The SOP did not supply the single phase reactive load as expected in this test.	The SOP did not supply the single phase reactive load as expected in this test.

Test dates	Report Section	Test Name	Pass	Significant observations	Comments on Pass status
21/04/2015	4.8	Voltage support test	Partial	When the voltage was reduced from the upper limit (and the voltage fell below the reset value) the SOP did not stop exporting active power at the expected voltage 'reset' threshold.	The SOP achieved the objective of the test and exported active power to support the network voltage.
06/05/2015	4.9	End to end test	Partial	1. This test has shown that the current output from the SOP oscillates when the algorithm trip threshold is exceeded. Imperial College London have been responsible for the algorithm development and has advised that the next version of the algorithm (v1.3 was used for this test and v1.5 is the next iteration) will incorporate a 'predictive' element that will resolve this issue. 2. This test has also indicated that there may be a conflicting control issue between the algorithm voltage support and current support functionality. 3. The test also demonstrated that the SOP failed to operate as expected when supplying the inductive load.	This test evaluated the SOP communication systems ability to monitor the load current and transfer this information via the DNP3 communication system to the SOP algorithm. This test also evaluated the SOP algorithms response to this information. The test results demonstrate that the DNP3 communication system operates in conjunction with the SOP algorithm. This test results also demonstrate that the current support part of the algorithm operates to reduce the load on the associated transformer. This was the expected outcome from this test however, there are a number of areas where unexpected, or out-of-specification behaviour, was observed. Specifically relating to oscillating current output, conflicting control and failure to supply an inductive load.
15/04/2015 and 06/05/2015	4.10	Fault and frequency test	Y	The frequency thresholds at which the SOP will operate do not match the frequency thresholds specified in the protection settings or in the test plan. It should also be noted that the time delay associated with the frequency thresholds specified in the protection settings do not match the time delays recorded in the test e.g. when the band 1 over frequency threshold was exceed the SOP should enter an inhibit state after 1 min delay but the SOP was recorded to operate after 37 s.	The frequency test has demonstrated that the SOP frequency protection will operate with a time delay when the frequency thresholds are breeched. It should be noted that the thresholds and time delays do not match the thresholds and time delays specified by TPS. The fault test has demonstrated that when a fault is applied close to the terminals of the SOP the SOP reduces its output current on all inverters to approximately 0 A and for all of the faults tested (both at 400 V and 11 kV) the SOP did not output more than a 600 A per phase (instantaneous).

6 REFERENCES

[1] Interconnect Solutions, Cannon, VEAM, and BIW, “VEAM PowerLock and Snaplock High Current Power Connectors.”

[2] K. Jennett and F. Coffele, “Plan for Testing of ‘Soft Open Point’ Power Electronic Device at PNDC, PNDC/UKPN-001/TP-01H.” p. 11, 2015.

[3] “Health and Safety Executive, Noise, advice for employers.” [Online]. Available: http://www.hse.gov.uk/noise/advice.htm.

[4] “Sound Source: A- and C-Weighed Noise Meaurements.” [Online]. Available: http://www.hearforever.org/tools-to-learn/sound-source-a-and-c-weighted-noise-measurements. [Accessed: 01-Jun-2015].

[5] “NoiseNews: What are A, C & Z frequency weightings?” [Online]. Available: http://www.cirrusresearch.co.uk/blog/2011/08/what-are-a-c-z-frequency-weightings/. [Accessed: 01-Jun-2015].

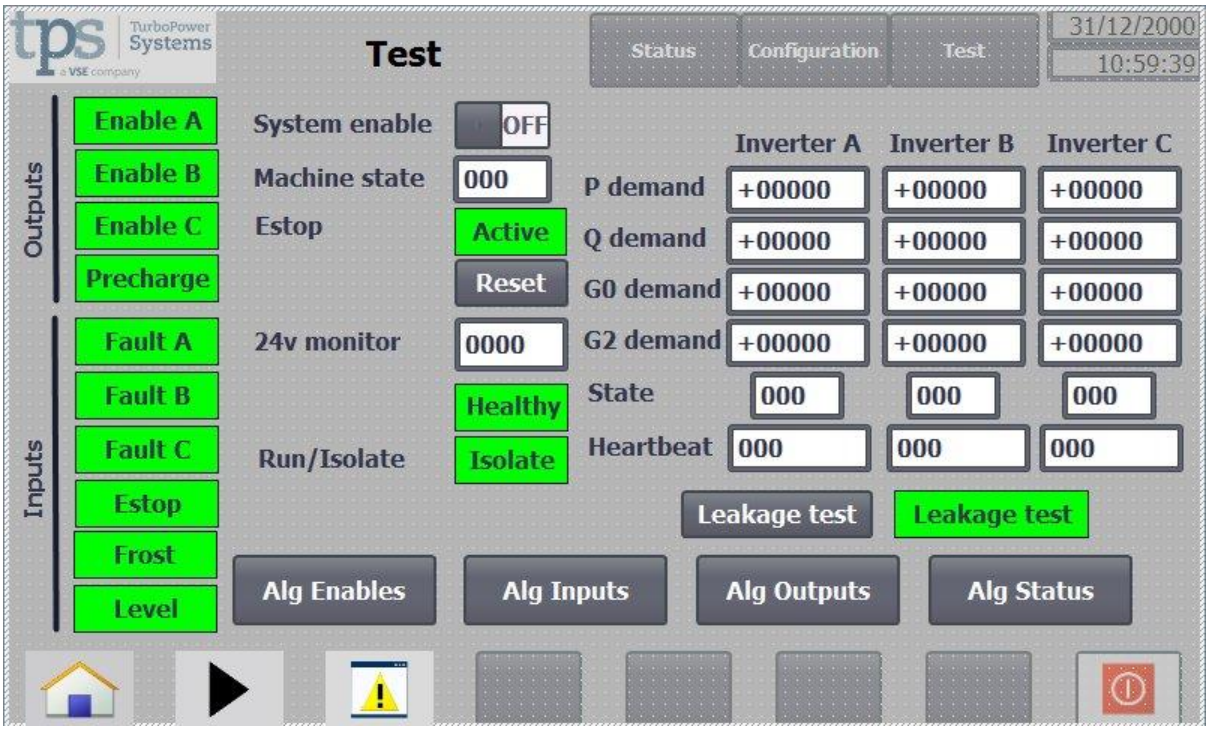
[6] “Health and Safety The Control of Noise at Work Regulations 2005.” Statutory Instruments, 2005.

[7] Amprobe, *Amprobe SM-10/SM-20 Sound Level Meters Users Manual*. .

[8] “ICNIRP Guidelines: For Limiting Exposure To Time Varying Electric, Magnetic and Electromagnetic Fields (Up To 300 Ghz).” International Commission On Non Ionizing Radiation Protection, Health Physics 74 (4):494|522; 1998.

7 APPENDIX A – HMI SETTINGS OVERVIEW

7.1 Test screen

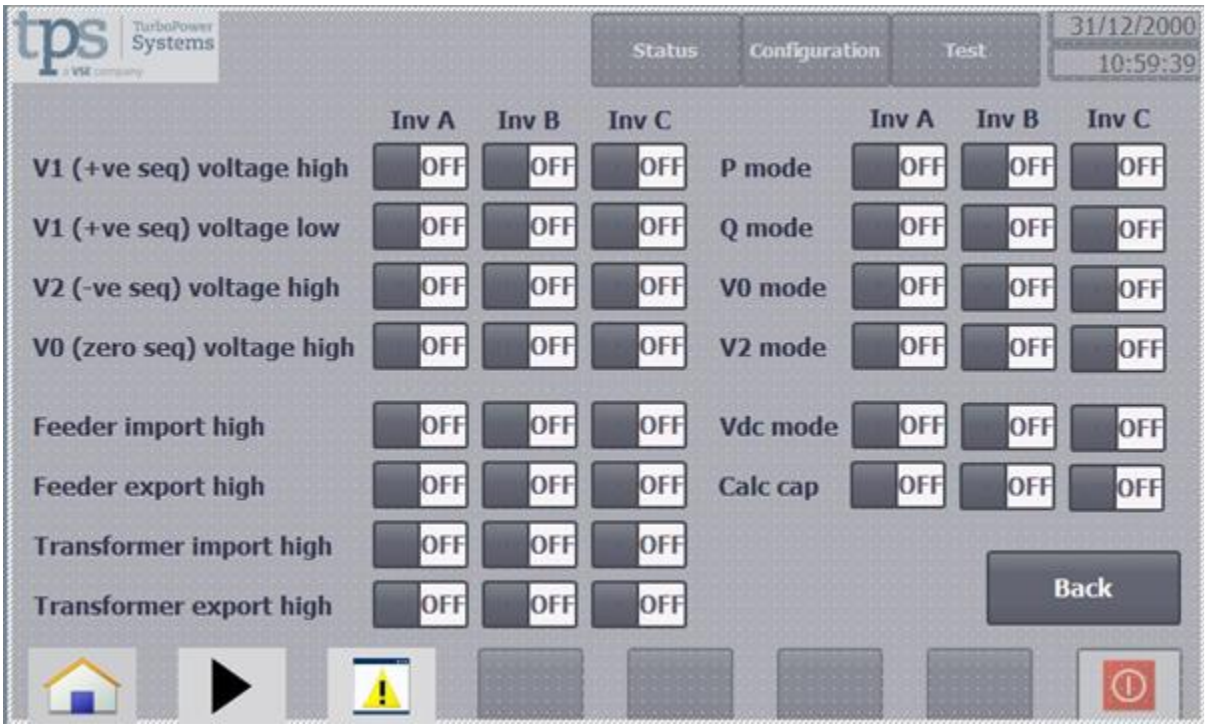


The state cell indicators are defined using the numerical referenced listed in the table below:

First digit (PLC status)		Second digit (Inverter status)	
Digit	**Meaning**	**Digit**	**Meaning**
0	Waiting for start	0	Power Up LAN
1	Assign DC Link Controller	1	Waiting for LAN
2	Pre-charge	2	Waiting for LAN Messages from PLC
3	Connect DC Link Controller	3	Waiting for Mode Assignment
4	Start Power Controllers	10	DC Link Controller, waiting for start command
5	Connect Power Controllers	11	DC Link Controller, Pre-charge dc link
6	Running	12	DC Link Controller, Connected
7	Shut Down Power Controllers	13	DC Link Controller, Inhibited
8	Shut Down DC Link Controller	14	DC Link Controller, Locked Out
		15	DC Link Controller, Emergency Stop
		20	Power Controller, waiting for operating conditions
		21	Power Controller, Synchronise with grid
		22	Power Controller, Connected
		23	Power Controller, Inhibited
		24	Power Controller, Locked Out
		25	Power Controller, Emergency Stop

7.2 Enables screen

Screen to switch on or off different support functions and modes of operation of the SOP.

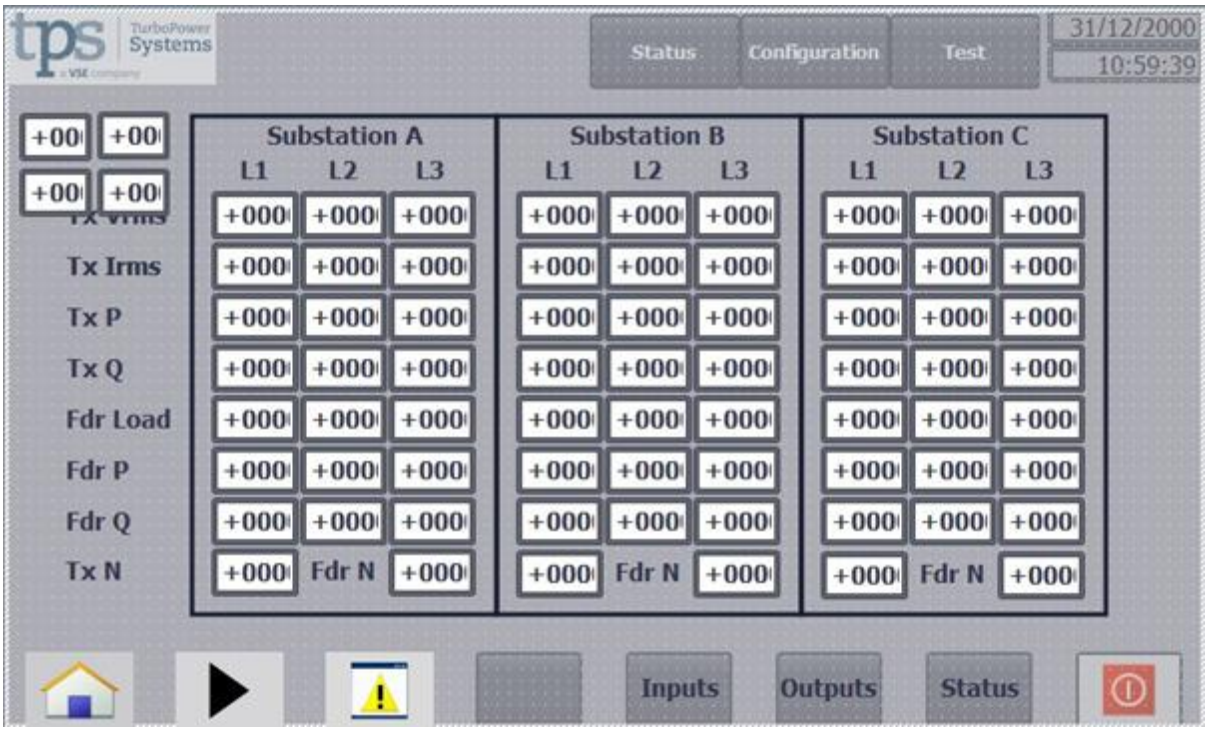


Field Name	Description	Support	Status
V1 voltage high	Enables support in a high voltage condition of the positive sequence voltage at the terminals of the SOP	This was switched on for the voltage support test	Enabled
V1 voltage low	Enables support in a low voltage condition of the positive sequence voltage at the terminals of the SOP	This was switched on for the voltage support test	Enabled
V2	Enables support in a high voltage condition of the negative sequence voltage at the terminals of the SOP	This was switched on for the unbalanced voltage support test (phase unbalance improvement test)	Disabled
V0	Enables support in a high voltage condition of the zero sequence voltage at the terminals of the SOP	This was switched on for the unbalanced voltage support test (phase unbalance improvement test)	Disabled
Feeder import high	Enables support in a high current import of the positive sequence current at the feeder		Enabled

	connection to the substation bus-bars		
Feeder export high	Enables support in a high current export of the positive sequence current at the feeder connection to the substation bus-bars		Enabled
Transformer import high	Enables support in a high current import of the positive sequence current at the secondary side of the substation transformer		Enabled
Transformer export high	Enables support in a high current export of the positive sequence current at the secondary side of the substation transformer		Enabled
P mode	Enables the SOP to operate in active power export or import mode	This should be enabled for voltage support, feeder support and transformer support to work	Enabled
Q mode	Enables the SOP to operate in reactive power export or import mode		Disabled
V0 mode	Enables to the SOP to operate in zero sequence support mode		Disabled
V2 mode	Enables to the SOP to operate in negative sequence support mode		Disabled

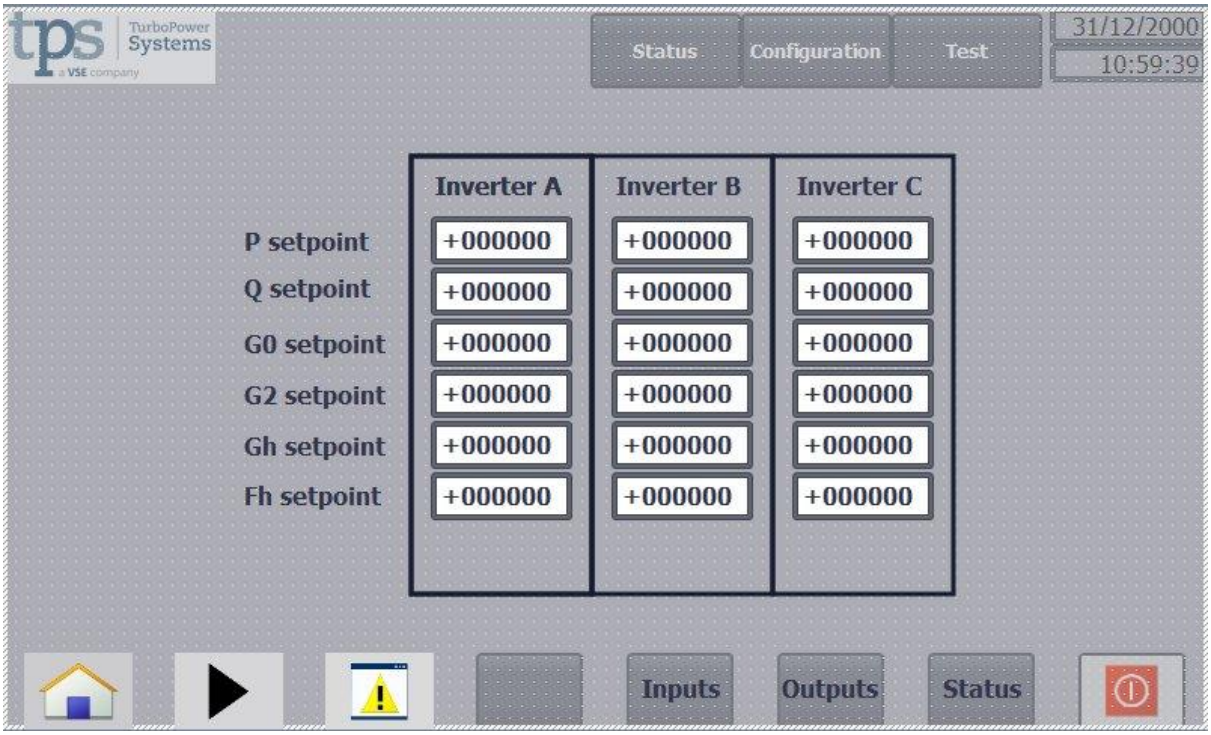
7.3 Algorithm inputs screen

Screen to show the status of the DNP3 communications.



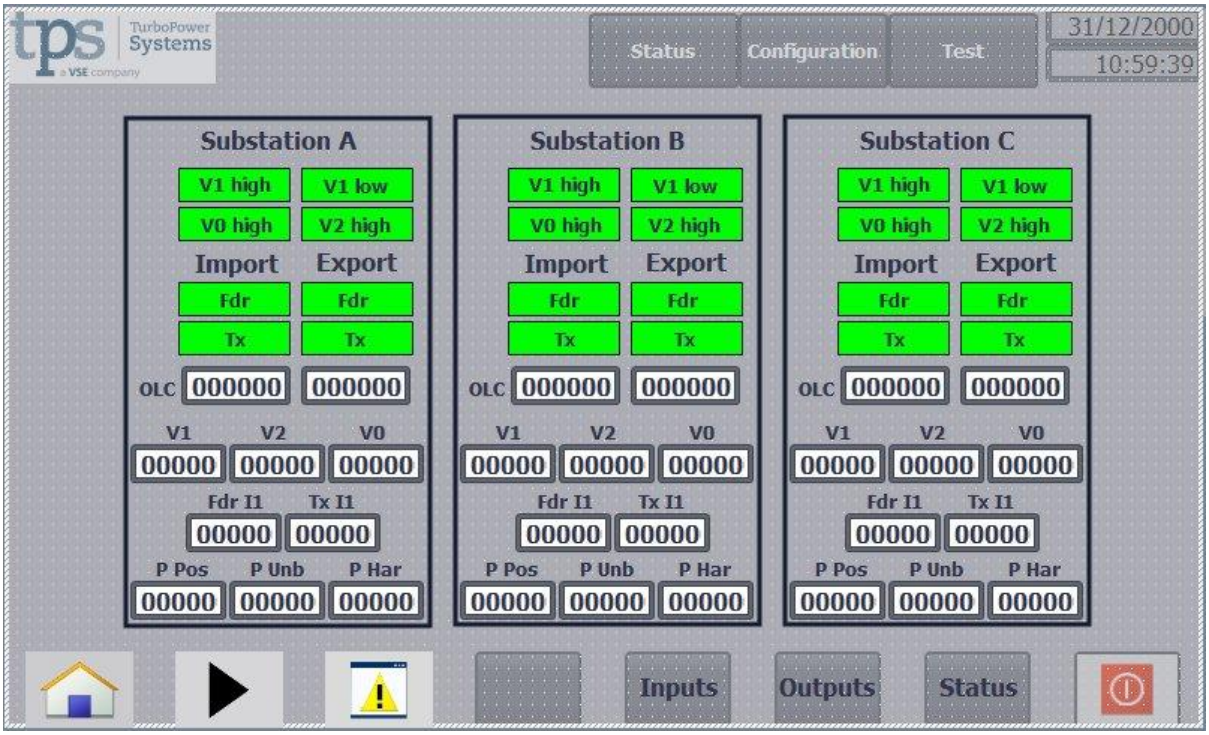
7.4 Algorithm outputs screen

This screen displays the sets points calculated by the algorithm and sent to the DSP control cards in order for the SOP to support the network.



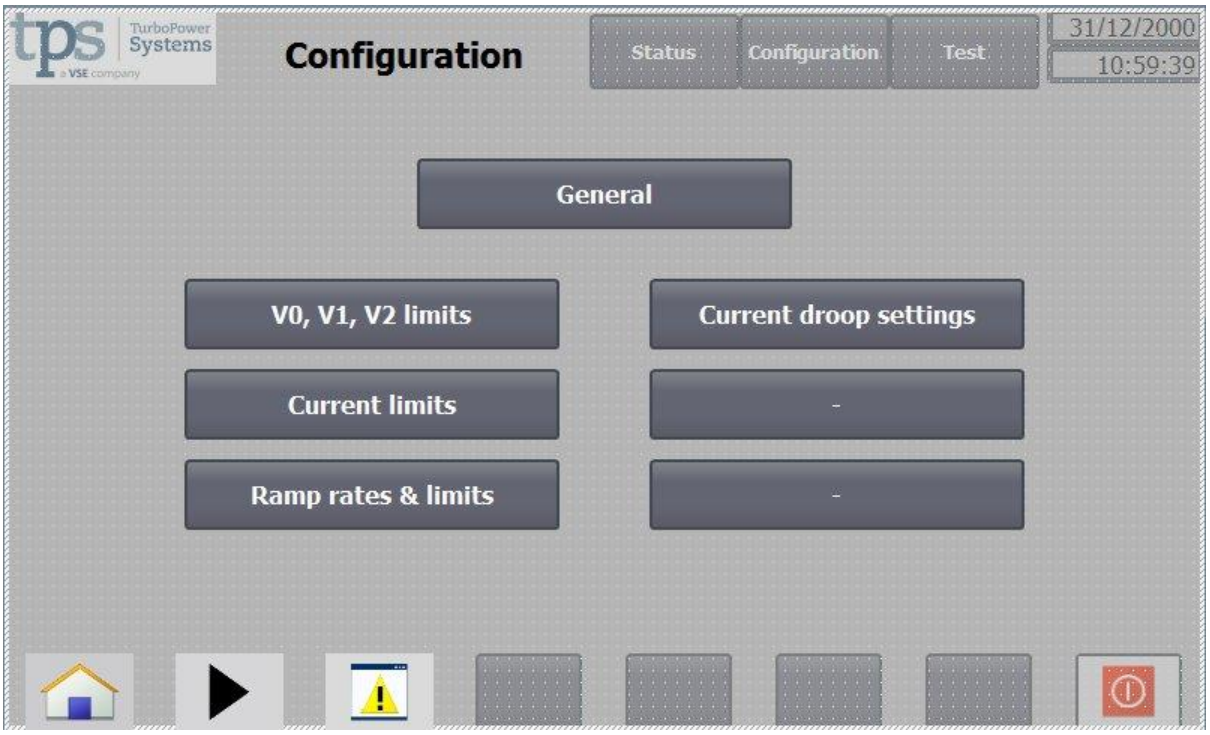
7.5 Algorithm status screen

This screen displays internal variables from the algorithm. If any of the support functions are above their thresholds, the relevant green box will turn red. The calculations form the sequence sets are displayed in the text boxes at the bottom of the screen.



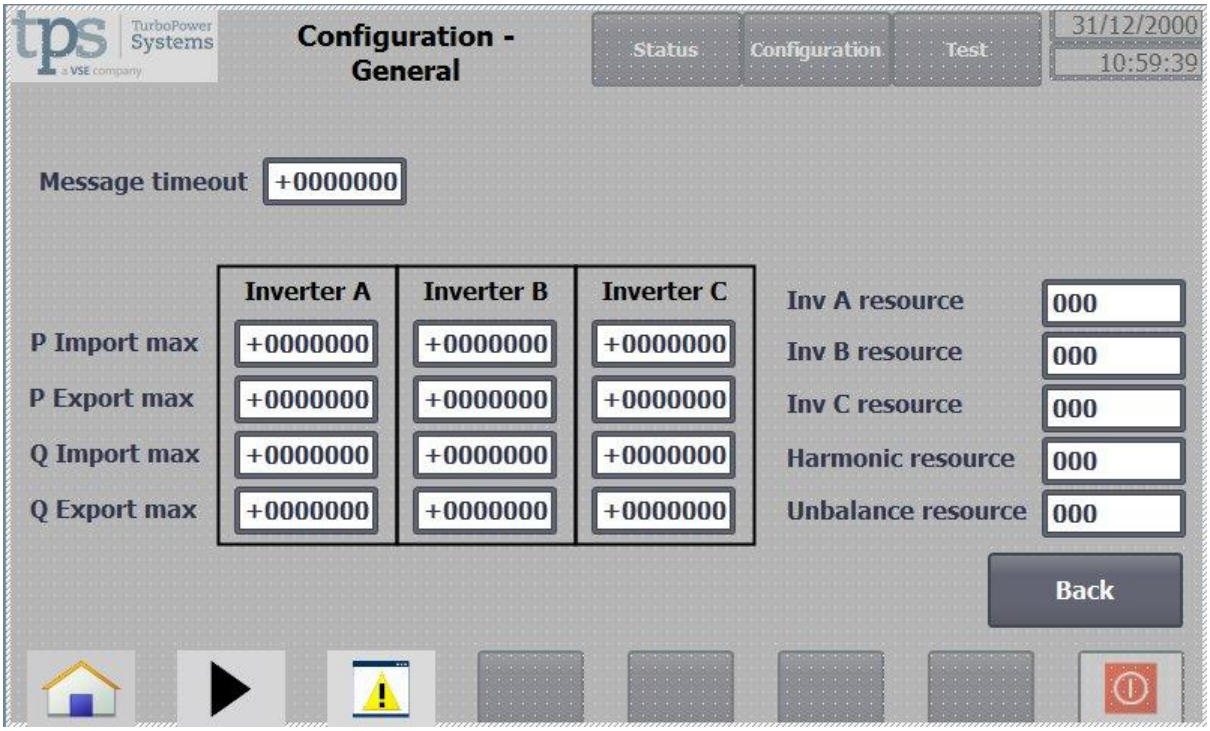
7.6 Configuration screen

Menu to select the screen for entering the set and reset limits for the different support functions of the SOP



7.7 Configuration general Screen

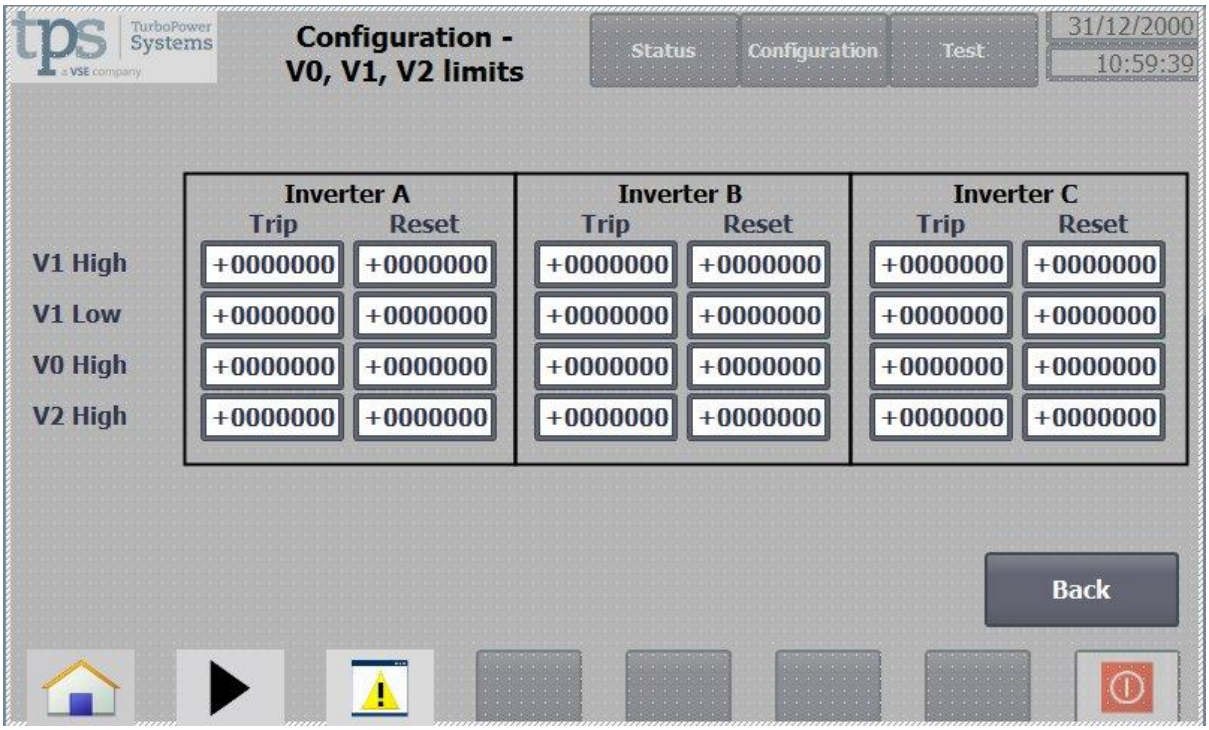
These are the values that the algorithm will limit the output for the SOP and should be set according to the cable or transformer rating limits. The algorithm will output power between zero and the maximum power / reactive power as set on this screen.



Field Name	Description	Status
P Import max	The maximum active power that the SOP may import on the corresponding port	The maximum power rating of the cable or transformer (maximum of 400 kW for substation I, 160 kW for substation D and 252 kW for substation A)
P Export max	The maximum active power that the SOP may export on the corresponding port	Maximum of 400 kW for substation I, 160 kW for substation D and 252 kW for substation A
Q Import max	The maximum reactive power that the SOP may import on the corresponding port	Maximum of 300 kVar for substation I, 120 kVA for substation D, 189 kVA for substation A
Q Export max	The maximum reactive power that the SOP may export on the corresponding port	Maximum of 300 kVar for substation I, 120 kVA for substation D, 189 kVA for substation A

7.8 Configuration voltage thresholds screen

This screen inputs the values for the set and reset thresholds for balanced and unbalanced voltage support.

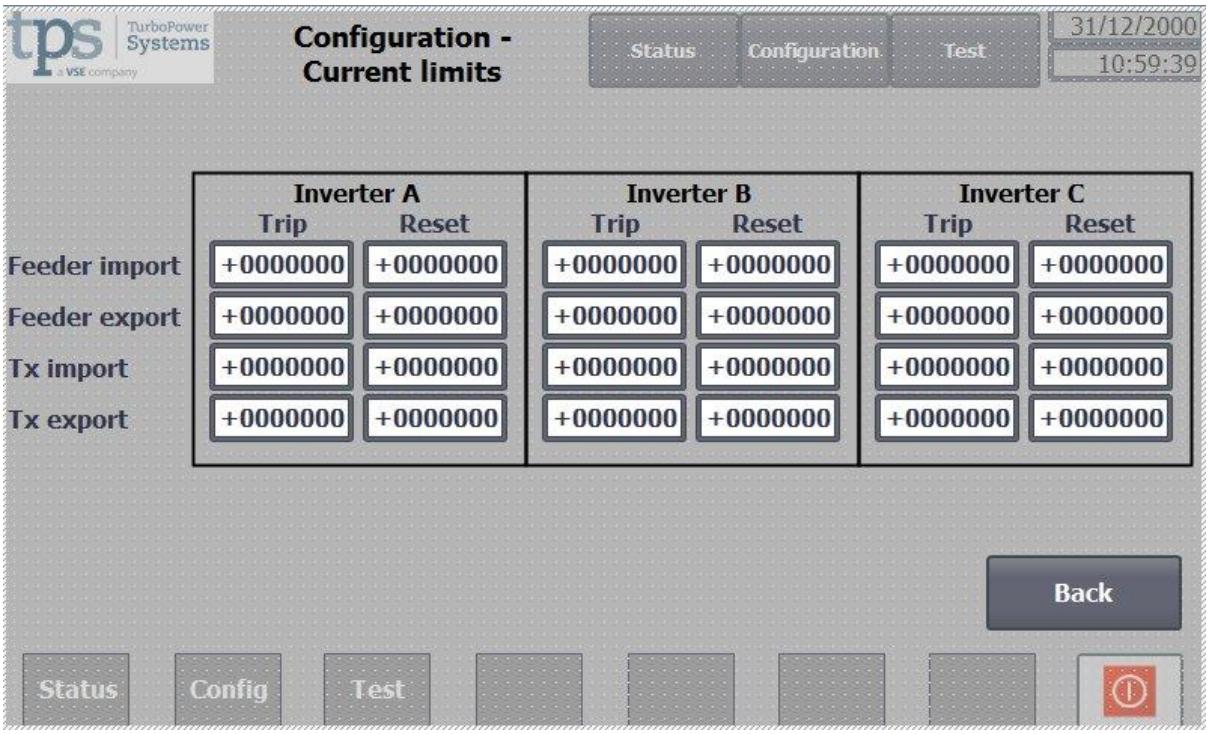


Field Name	Description	Support	Status
V1 upper set (V1 high)	The threshold set for a high voltage condition of the positive sequence voltage at the terminals of the SOP	Should be set to the value minus 1 to where the SOP needs to start supporting a high voltage	245 V
V1 upper reset (V1 high)	The threshold reset for a high voltage condition of the positive sequence voltage at the terminals of the SOP	Should be set to the value plus 1 to where the SOP needs to stop supporting a high voltage (although this failed in the test last week)	240 V
V1 lower set (V1 high)	The threshold set for a low voltage condition of the positive sequence voltage at the terminals of the SOP	Should be set to the value plus 1 to where the SOP needs to start supporting a low voltage	220 V
V1 lower reset (V1 high)	The threshold reset for a low voltage condition of the positive sequence voltage at the terminals of the SOP	Should be set to the value minus 1 to where the SOP needs to stop supporting a low voltage	230 V
V0 set (V0 high)	The threshold set for a high voltage condition of the zero sequence		2 V

	voltage at the terminals of the SOP		
V0 reset (V0 high)	The threshold reset for a high voltage condition of the zero sequence voltage at the terminals of the SOP		2 V
V2 set (V2 high)	The threshold set for a high voltage condition of the negative sequence voltage at the terminals of the SOP		2 V
V2 reset (V2 high)	The threshold reset for a high voltage condition of the negative sequence voltage at the terminals of the SOP		2 V

7.9 Limit trip screen

This screen sets the limits for the feeder and transformer support



If the test requires the SOP to support when the load is greater than, for example 100 A, then the trip limit should be set to 99 A. To ensure stability it is best to set the reset 10 A lower than the trip limit. Set the export setting to the same as the import settings. In Version 1 Issue 3 of the algorithm, the asset guarding uses the same values as the threshold set setting. If any of the ports have the threshold set to zero, then the algorithm will not use that port. This has been changed for the future releases of the algorithm and the asset guarding settings are different from the threshold settings.

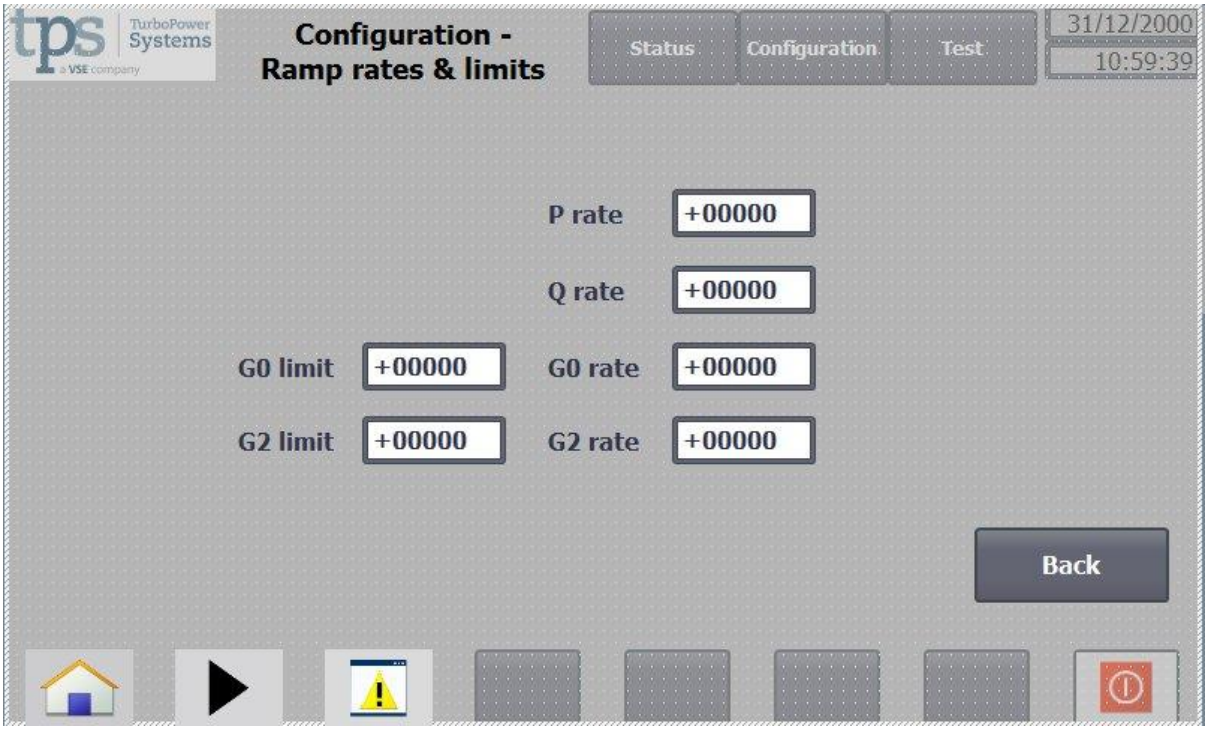
Field Name	Description	Status
Feeder import trip	The threshold trip for the import current condition of the positive sequence current at the feeder connection to the substation bus-bars	For the port that the load is connect to, set the trip to the value of current for which support is required. For the other ports set the trip to the current rating of the cable or transformer. I recommend the thresholds to be set to 500 A for substation I, 250 A for substation D and 50 A for substation A (if the SOP needs to start supporting at 50 A)
Feeder import reset	The threshold reset for the import current condition of the positive sequence current at the feeder connection to the substation bus-bars	Set the reset current to 10 A below the trip current
Feeder export trip	The threshold trip for the export current condition of the positive sequence current at the feeder	500 A for substation I, 250 A for substation D and 50 A for substation A (if the SOP needs to start supporting at 50 A)

	connection to the substation bus-bars	
Feeder export reset	The threshold reset for the export current condition of the positive sequence current at the feeder connection to the substation bus-bars	Set the reset current to 10 A below the trip current
Transformer import trip	The threshold trip for the import current condition of the positive sequence current at the secondary side of the transformer	500 A for substation I, 250 A for substation D and 50 A for substation A (if the SOP needs to start supporting at 50 A)
Transformer import reset	The threshold reset for the import current condition of the positive sequence current at the secondary side of the transformer	Set the reset current to 10 A below the trip current
Transformer export trip	The threshold trip for the export current condition of the positive sequence current at the secondary side of the transformer	500 A for substation I, 250 A for substation D and 50 A for substation A (if the SOP needs to start supporting at 50 A)
Transformer export reset	The threshold reset for the export current condition of the positive sequence current at the secondary side of the transformer	Set the reset current to 10 A below the trip current

If the rating of the cable is less than the current rating of the transformer then the thresholds should be set accordingly.

7.10 Ramp Rates

This screen sets the step the algorithm will make when the algorithm is operating to provide support to the network.



Field Name	Description	Support	Status
P rate	The increment of active power at the output of the SOP	If the SOP starts to hunt then reduce this value	2 kW/s
Q rate	The minimum increment of reactive power at the output of the SOP	If the SOP starts to hunt then reduce this value	2 kVar/s
G0 rate	The increment of Siemens at the output of the SOP scaled by 10 for the zero sequence conductance support		50 dS
G2 rate	The increment of Siemens at the output of the SOP scaled by 10 for the negative sequence conductance support		50 dS
G0 limit	The maximum Siemens that the SOP may set for solving negative sequence voltage		10 000 dS
G2 limit	The maximum Siemens that the SOP may set for		10 000 dS

	solving zero sequence voltage		

8 APPENDIX B – SOP CIRCUIT BREAKER PROTECT

The DIP switches are set for L,S,I,G

PR222DS/P, PR222DS/PD and PR223DS[1] - Protection functions and parameterisations

Protection functions		Trip threshold	Trip curves[2]	Excludability	Relation t = f(I)
L	Against overload with long inverse time delay trip and trip characteristic according to an inverse time curve (I^2t=k) according to IEC 60947-2 Standard	**Manual setting** I_1 = 0.40....1 x In step = 0.02 x In	**Manual setting** at 6 x I_1 t_1 = 3 - 6 - 9/12 - MAX[3]	-	$t = k/I^2$
		Electronic setting I_1= 0.40... 1 x In step 0.01 x In Trip between 1.1...1.3 x I_1	**Electronic setting** at 6 x I_1 t_1 = 3... 18s step 0.5s[4] Tolerance: ± 10%		
S	Against short-circuit with inverse short time delay trip and trip characteristic with inverse time (I^2t=k) or definite time	**Manual setting** I_2 = 0.6-1.2-1.8-2.4-3-3.6-4.2-5.8-6.4-7-7.6-8.2-8.8-9.4-10 x In[5]	**Manual setting** at 8 x In t_2 = 0.05 - 0.1 - 0.25 - 0.5s	■	$t = k/I^2$
		Electronic setting I_2 = 0.60...10 x In step 0.1 x In Tolerance: ± 10%	**Electronic setting** at 8 x In t_2 = 0.05...0.5s step 0.01s Tolerance: ± 10%[6]		
		Manual setting I_2 = 0.6-1.2-1.8-2.4-3-3.6-4.2-5.8-6.4-7-7.6-8.2-8.8-9.4-10 x In[5]	**Manual setting** t_2 = 0.05 - 0.1 - 0.25 - 0.5s	■	$t = k$
		Electronic setting I_2 = 0.60... 10 x In step 0.1 x In Tolerance: ± 10%	**Electronic setting** t_2 =0.05...0.5s step 0.01s Tolerance: ± 10%[6]		
I	Against short-circuit with instantaneous trip	**Manual setting** I_3 = 1.5-2.5-3-4-4.5-5-5.5-6.5-7-7.5-8-9-9.5-10.5-12 x In[5]	Instantaneous	■	$t = k$
		Electronic setting I_3 = 1.5... 12 x In[5] step 0.1 x In Tolerance: ± 10%			
G	Against earth fault with inverse short time delay trip and trip characteristic according to an inverse time curve (I^2t=k)	**Manual setting** I_4 = 0.2-0.25-0.45-0.55-0.75-0.8-1 x In	**Manual setting** up to 3.15 x I_4 up to 2.25 x I_4 up to 1.6 x I_4 up to 1.10 x I_4 t_4 = 0.1s t_4 = 0.25s t_4 = 0.4s t_4 = 0.8s	■	$t = k/I^2$[7]
		Electronic setting I_4 = 0.2...1 x In step 0.1 x In Tolerance: ± 10%	**Electronic setting** t_4 = 0.1...0.8s step 0.01s Tolerance: ± 15%		

[1] These tolerances hold in the following conditions:
- self-powered trip unit at full power and/or auxiliary supply
- two or three-phase power supply

In conditions other than those considered, the following tolerances hold:

	Trip threshold	Trip time
S	± 20%	± 20%
I	± 20%	≤ 50ms
G	± 20%	± 20%

[2] I_1 values for MAX setting:

CB	Electronic setting	Manual setting
T4 320	3...10.5s Step 0.5s	3-6-9-10.5
T5 630		
T6 1000		
T4 250	3...18s Step 0.5s	3-6-9-18
T5 400		
T5 800	3...18s Step 0.5s	3-6-9-18
T6 630	3...18s Step 0.5s	3-6-12-18

[3] For T4 In = 320 A and T5 In = 630 A, T6 In = 1000 A ⇨ I_1max = 9.5 x In and I_1max = 9.5 x In
For T6 In = 800 A ⇨ I_1max = 10.5 x In
[4] Tolerance: ± 10 ms
[5] The setting of the PR222DS trip unit is electronic only (local/remote).
The L protection can be set at I_1 = 0.16...1 x In. For I_1 < 0.4 x In the neutral setting must be at 100% of that of the phases
[6] t = k/I^2 up to the current value indicated, t = k (equating to the chosen setting) beyond the current value indicated

L	Against overload with **long** inverse time delay trip and trip characteristic according to an inverse time curve ($I^2t=k$) according to IEC 60947-2 Standard
S	Against short-circuit with inverse **short** time delay trip and trip characteristic with inverse time ($I^2t=k$) or definite time
I	Against short-circuit with **instantaneous** trip
G	Against **ground** fault with inverse short time delay trip and trip characteristic according to an inverse time curve ($I^2t=k$)

Nominal current **In** = 630 A.

L – Long (DIP switches can be added, e.g. 4,5 will provide **In** x 0.88 = 554 A)

I1 + 0.4				
DIP1 up	DIP2 up	DIP3 up	DIP4 up	DIP5 up
In x 0.02	**In** x 0.04	**In** x 0.08	**In** x 0.16	**In** x 0.32
DOWN	**DOWN**	**DOWN**	**UP**	**UP**

t1	
Down Down	3s
Down Up	6s
UP DOWN	9s
Up Up	Max

S – Short (DIP switches can be added, e.g. 1,2 will provide **In** x 1.8 = 1008A)

I2 + 0.0			
DIP1 up	DIP2 up	DIP3 up	DIP4 up
In x 0.6	**In** x 1.2	**In** x 2.4	**In** x 5.8
UP	**UP**	**DOWN**	**DOWN**

DIP 1 , 2	DIP 3	t2
Down Down	Down	0.05s when i > I2
Down Up	Down	0.1s when i > I2
Up Down	Down	0.25s when i > I2
UP UP	**DOWN**	0.5s when i > I2
Down Down	Up	0.05s when i > 8 x **In**
Down Up	Up	0.1s when i > 8 x **In**
Up Down	Up	0.25s when i > 8 x **In**
Up Up	Up	0.5s when i > 8 x **In**

I – Immediate (DIP switches can be added, e.g. 2 will provide **In** x 2.5 = 1575A)

I3 + 0.0			
DIP1 up	DIP2 up	DIP3 up	DIP4 up
In x 1.5	**In** x 2.5	**In** x 3	**In** x 5
DOWN	**UP**	**DOWN**	**DOWN**

Mode	
UP	Manual
Down	Electronic

Neutral	
Down Down	Off
Down Up	Off
UP DOWN	On at 50 % unbalanced > 50 % of phase
Up Up	On at 100 % unbalanced > 100 % of phase

G – Ground fault

(DIP switches can be added, e.g. 3 will provide **In** x 0.55 = 346A)

Ig + 0.0		
DIP1 up	DIP2 up	DIP3 up
In x 0.2	**In** x 0.25	**In** x 0.55
DOWN	**DOWN**	**UP**

I4	
DOWN DOWN	0.1s
Down Up	0.2s
Up Down	0.4s
Up Up	0.8s

9 APPENDIX C – SOP OPERATING MANUAL FOR TESTING AT THE PNDC

Unlock procedure within the SOP (TPS responsibility)

This procedure will be completed prior to the first test and after any subsequent work by TPS within the SOP. Prior to this procedure operational control will be given from the PNDC to TPS and after this procedure is completed TPS will return operational control to the PNDC.

1) With the unit isolated and no power to any of the equipment or auxiliary devices / test equipment, open the right three inverter cabinets using the key provided (the multimeter fitted to the end cabinet can be used to observe that the DC Link voltage within the cabinet is below a safe working voltage, however this is for indication only).
2) Test for dead using both a proving unit and voltmeter.
3) Unlock the circuit breakers (MCCB) within the cabinets by removing the padlocks.
4) The MCCB in each cabinet should then be placed in the automatic position. All MCCBs at this point should be in the off position. If the MCCB is not in the off position then set the MCCB to manual and place the MCCB in its off position by depressing the off button on the MCCB. Return the MCCB to automatic.
5) Close the 3 inverter cabinet doors.
6) Open the control cabinet door and close all the circuit breakers. Close the control cabinet door.

Make all external connections (PNDC responsibility)

1) With the power isolated and locked off at the test bay distribution boards, connect the three grid supplies to the connectors on the front of the inverter (SOP). NB Substation I will not be locked off but the incoming power cables are to be disconnected after the 11 KV grid has been powered down.

Connecting Power to the Cooling System (PNDC responsibility)

1) Plug in the cooling fan Power Supply Unit (PSU) (switched off at the mains socket)
2) Plug in hub power supplied (switched off at the mains socket)
3) Connect the 3 phase supply to the cooling pump (with the isolator in the off position).
4) Plug in the PLC's HMI to the external LAN connector (to 3T SOP) and connect the HMI PSU to the HMI (switched off).

Applying Power to the SOP (PNDC responsibility)

1) Ensure that the two outer valves on the cooling pipework are set to the on position.
2) Connect the mains power to the HMI and cooling fan (mains single phase).
3) Unlock the isolator to the cooling pump and place in the 'on' position, the pump will now engage.
4) Make the connection to Substation I.
5) Unlock the 2 incoming 3 phase grid mains power supplies and remove the isolation at the distribution board.
6) Engage the power to the 11 kV grid.
7) There is now mains power to the SOP and the dc link internal to the SOP will pre-charge to approximately 620 Vdc. Under no circumstances should the inverter cabinets or control cabinet be opened without following the isolation procedure for the SOP (including discharge of the dc link).
8) Once the PLC has connected to the 3 inverter control cards (ICC) it will be possible to control the SOP from the HMI interface (see figure 1) using the test page. You will be able to see the heartbeat indicators for each inverter cabinet increment when an LAN connection has been made from the PLC to the 3 ICCs.
9) An enable button is provided to turn on the SOP and connect it to the 3 incoming 3 phase grids in the correct sequence. Placing the enable button in the on position will start the start-up sequence.

10) Disabling the SOP is achieved by placing the enable button in the off position. The PLC will turn off the SOP in the correct sequence.
11) Numerical input blocks are provided for the control of power and reactive power for each of the 3 inverter cabinets. N.B. For the prototype the A inverter cabinet will provide control to maintain the DC link at 750 Vdc, as such it will ignore any real power demands placed on it.

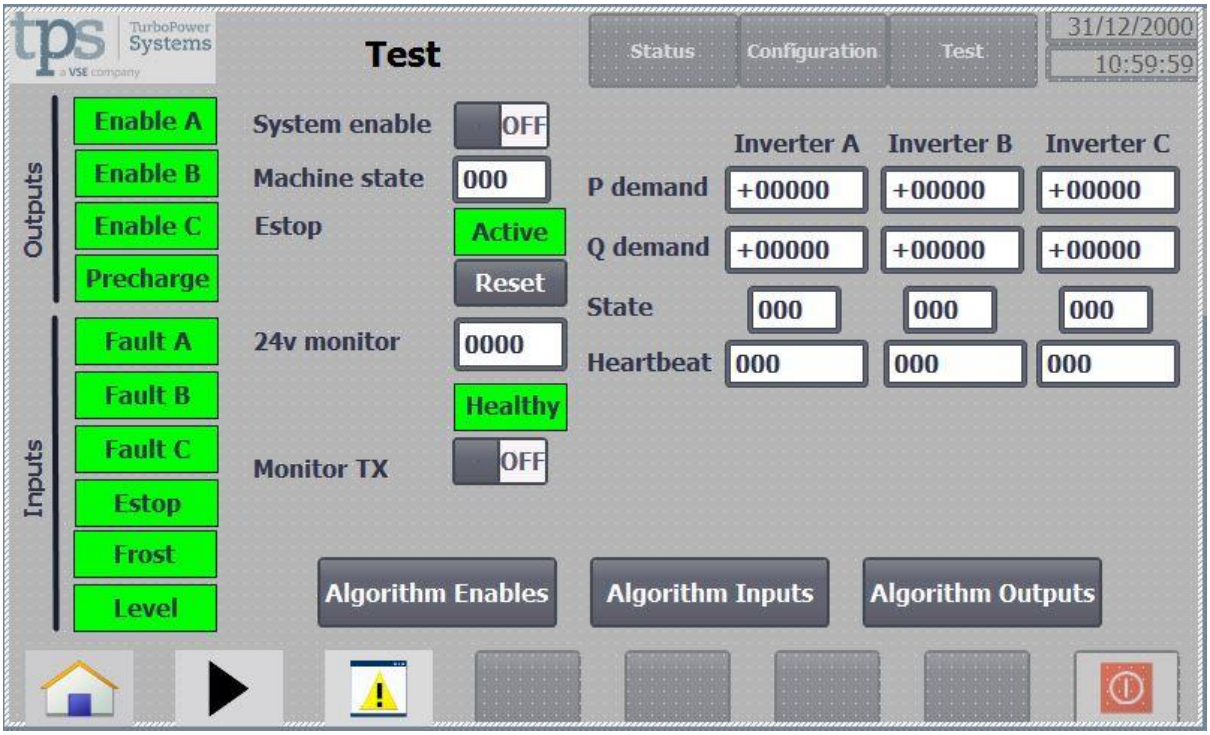


Figure 95: HMI Test Page

Turning off the SOP (PNDC responsibility)

1) Disable the SOP by placing the enable button in its 'off' position. The PLC will turn off the 3 inverter cabinets in sequence N.B. There will be motor noise generated by the MCCB as the closing is recharged.
2) Disconnect the 11 KV grid.
3) Wait 5mins
4) Isolate and lock off the 2 incoming 3 phase mains grid supplies.
5) Break the connection to Substation I.
6) Isolate and lock off the power to the 3 phase cooling pump.
7) Unplug hub power supplies (mains socket) to SOP
8) Disconnect the mains from the HMI and cooling fan.

Additional to turn off procedure for work within the SOP cabinets (TPS responsibility)

1) Wait for the DC Link to discharge. This will take a minimum of 5 minutes (the multimeter attached can be used to indicate the voltage level on the DC link) before opening the 3 inverter cabinet doors. Maximum allowable DC Link voltage is 35Vdc.
2) Test for dead in each cabinet using a proving unit and voltmeter.
3) Place the MCCBs in there locked position and lock off the MCCBs.

Emergency Stop Procedure

1) Press the remote emergency stop button connected to the SOP.
2) Press either of the emergency stop buttons within the test bay.

3) Disconnect the 11 KV Grid.
4) Break the connection to Substation I.
5) The inverter cabinets should not be opened before a 5 minute discharge period has been observed (the multimeter can be used to indicate the voltage level on the dc link, maximum dc link voltage is 35Vdc). As always there will be a need to test for dead once the cabinets have been opened to ensure that the unit is safe to work on.

Demonstration of Autonomous Power Transfer

SDRC 9.4

UK Power Networks
Delivering your electricity

Project Accreditations

Report written by Imperial College for the demonstration of autonomous power transfer between connected substations based on operational data. Data presented in this report was collected during testing at the Power Networks Demonstration Centre and at selected sites during the start of the SOP field trials.

Imperial College London

Contents

Abbreviations

AC	Alternating current
BAU	Business As Usual
DC	Direct current
DNO	Distribution Network Operator
DSP	Digital signal processor
FUN-LV	Flexible Urban Networks – Low Voltage
HV	High Voltage
LCNF	Low Carbon Networks Fund
LPN	London Power Networks
LV	Low Voltage
HMI	Human machine interface
NOP	Normal Open Point (for LV systems – either a Link box or LV distribution board)
PED	Power Electronics Device (interchangeable with SOP)
PNDC	Power Networks Demonstration Centre
RTU	Remote Telemetry Unit
P	Real power
PLC	Programmable Logic Controller
Q	Reactive power
SDRC	Successful Delivery Reward Criteria
SOP	Soft Open Point
SPN	South Eastern Power Networks
UKPN	UK Power Networks

1. Introduction

This report demonstrates autonomous power transfer between connected substations based on operational data for a three port SOP. The objective of the SOP is to transfer power between difference substations within the 400 V distribution network in order to solve network constraints. If one circuit is constrained because of high voltage or over current at the feeder or substation and is connected via the SOP to another circuit that is not constrained, the remaining capacity in the unconstrained circuit may be used to support the constrained circuit.

The SOP was tested at the Power Networks Demonstration Centre (PNDC) in Cumbernauld, Scotland. The PNDC is a venture between the University of Strathclyde, Scottish Enterprise, the Scottish Funding Council, Scottish Power and Scottish and Southern Energy aimed at accelerating the adoption of novel research and technologies into the electricity industry. The centre is equipped with multiple substations, cables and load banks. The three-port SOP was connected between different substations and different network constraints were simulated.

Four three-port and four two-port SOPs were connected to the interconnected network in Brighton. These devices are running an algorithm designed to share capacity and solve network constraints. The three-port SOPs were connected in substations and the two-port SOP were installed on the pavements. An algorithm was developed to autonomously transfer power to provide support to the network and solve the following constraints.

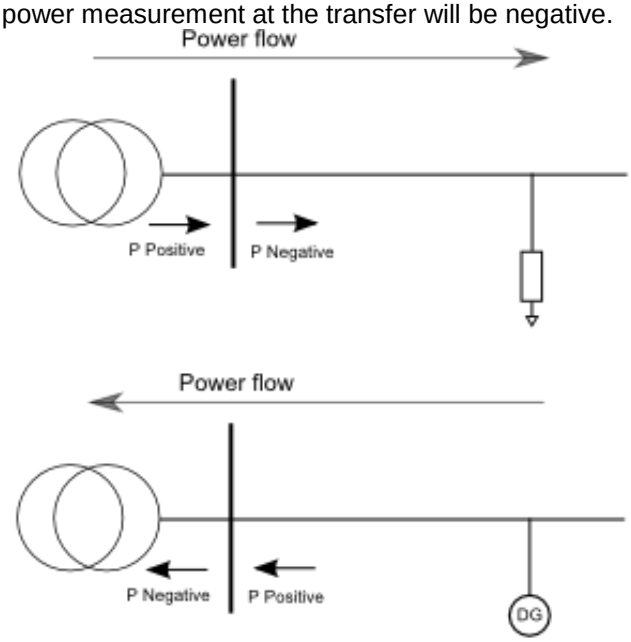
- Equalise the transformer loading or,
- Increase or reduce the voltage at the terminals of the SOP or,
- Support an overloaded feeder cable or,
- Support an overloaded transformer.

This report demonstrates autonomous power transfer between interconnected substations when one of the three substations experienced unbalanced transformers. Two cases are presented demonstrating the SOP registering that a constraint has occurred and transferring power until that constraint has been solved.

2. Definitions

SOP power convention

UK Power Networks use a convention where power flow towards the bus-bar is positive. The bus-bar is between the transformer and the feeder. Therefore, when the power flow is from the substation to the load the measurement will be positive for the transformer as the power flow is from the transformer towards the bus-bar. The measurement for the power at the feeder will be negative as the power flow will be away from the bus-bar. When the feeder has an excess of distributed generation and the power flow is from the cable to the transformer then the power measurement at the feeder will be positive and the power measurement at the transfer will be negative.

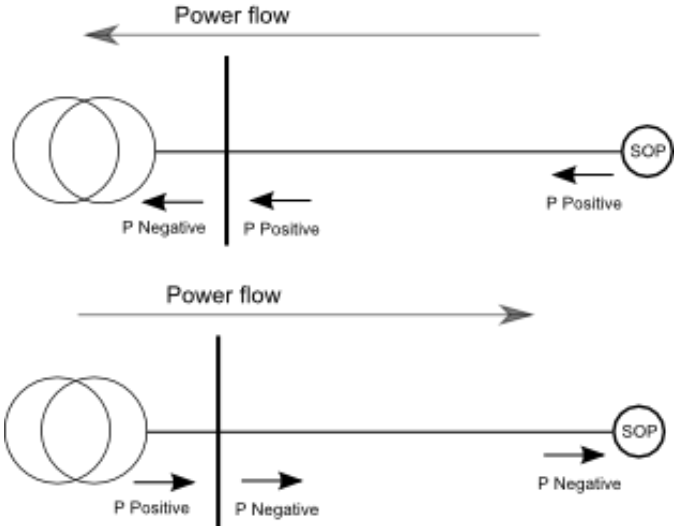


Feeder load / generation	Transformer P measurement	Feeder P measurement
Load only	Positive	Negative
Distributed generation only	Negative	Positive

Feeder capacitive / inductive	Transformer Q measurement	Feeder Q measurement
Capacitive	Negative	Positive
Inductive	Positive	Negative

The SOP will use a generator convention which defines positive power as the power generated or supplied from a source and negative power as the power consumed by a load. Reactive power is defined as positive for capacitive loads and negative for inductive loads. If the SOP is acting as a load where power is flowing from the 11 kV network,

through the transformer to the SOP, then the power will be negative. If power is being injected into the network from the SOP then the power reference will be positive.



Limit

A limit is being defined as a physical operating constraint. For example a 95 mm^2 cable is only able to carry 235 A of continuous current per phase. The maximum feeder current is limited by the thermal properties of the cable. If the cable is operated at over current continually then the cable will heat to a higher temperature and this could cause failure. However, the cable may be operated at an over current for a short period of time. This is known as the cyclic rating, which for 95 mm^2 cable is 290 A. For the SOP input parameters, the cyclic rating will be considered the limit.

Threshold

A threshold is a pre-defined value where, once reached, the SOP would decide if action is required.

Constraint function

A constraint function is a constraint on the network that the port is connected to. Each constraint function has an associated threshold. Constraint functions include the SOP terminal voltage, feeder current and transformer current.

Support function

A support function is an action that the SOP has available in order to support the constraint function.

Algorithm function

An algorithm function is a function or block within the algorithm. The SOP algorithm is partitioned into many algorithm functions.

Port

The SOP consists of three ports. Each port is connected to a common DC bus-bar and a different way on the AC LV distribution board.

Export

In this report, export power is defined as power flow from distributed generation sources to the network. When distributed generation is connected to the 400 V network, the power exported by the generation will flow from the source, through the cable and to the 400 V substations. If only distributed generation is connected to the feeder, then the feeder will export power from the feeder to the substation and the transformer will export power from the 400 V network to the 11 kV network.

Import

In this report, import power is defined as power flow from network to the load. When load is connected to the 400 V network, the power imported by the load will flow from the network, through the transformer and feeder. If only loads are connected to the feeder, then the feeder will import power from the substation and the transformer will import power from the 11 kV network to the 400 V network.

3. Network Configuration

The SOP at the PNDC was configured as follows.

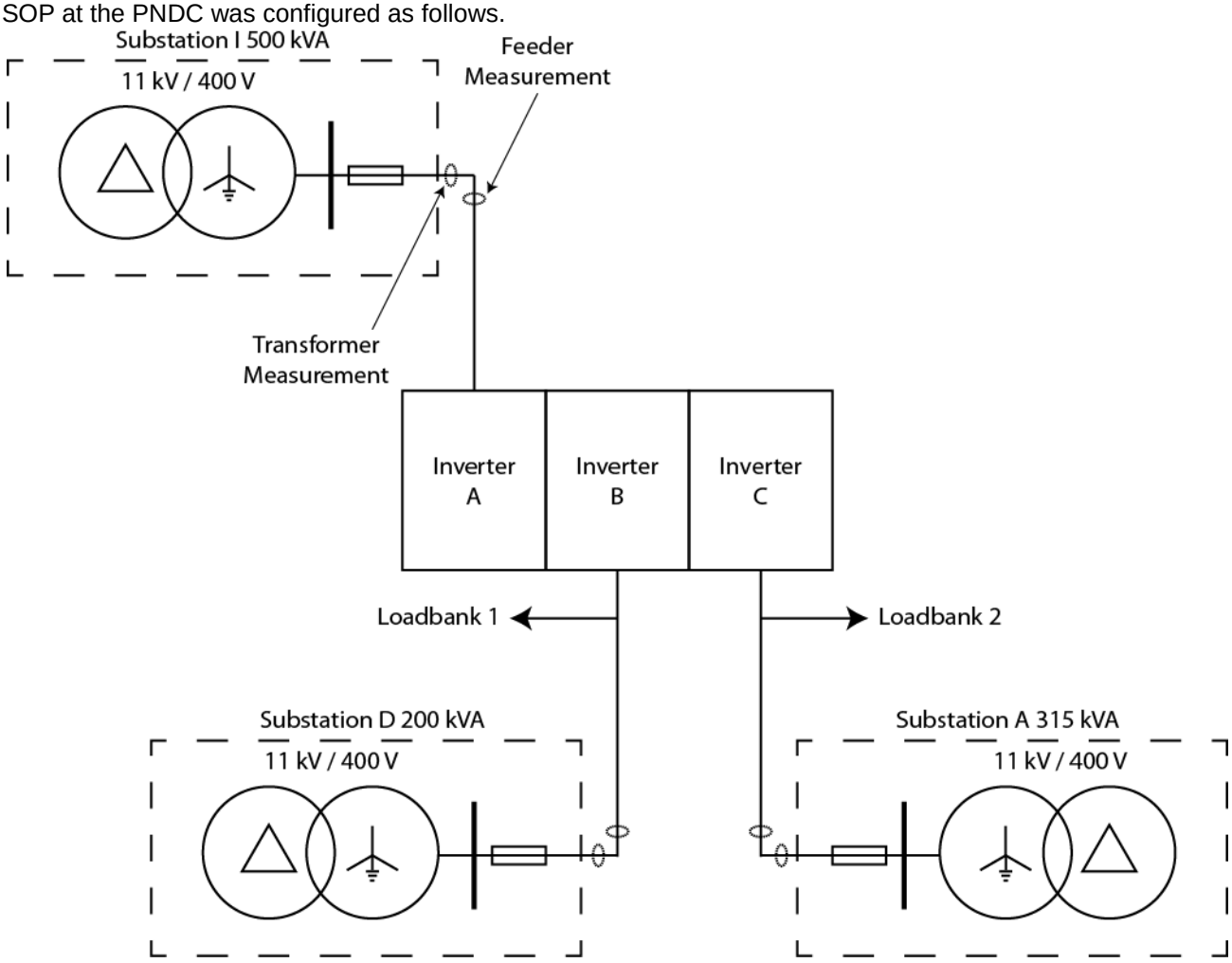


Figure 3.1: Diagram of the SOP connection at the PNDC

4. Voltage Constraint

Designed Operation

The output voltage of the SOP is measured using sensors internal to the hardware. The RMS voltage of each of the three phases is read as an input to the algorithm. The algorithm calculates the positive sequence set of the voltage and uses this calculated measurement to determine if support is required. When the voltage at a port is above the high threshold, the SOP will act as a load and absorb power to reduce the voltage. Once the voltage is less than the upper threshold set, the SOP will hold the amount of load. The load the SOP presents to the port will reduce once the voltage at that port is less than the upper voltage reset. When the voltage is less than the lower threshold set, the SOP will export power in an attempt to increase the voltage. Once the voltage is greater than the lower threshold set, the SOP will hold the amount of power export. The power export the SOP presents to the port will reduce once the voltage at that port is greater than the lower voltage reset. Table 4-1 shows the voltage level set at the PNDC.

Table 4-1: Voltage thresholds for the voltage at the terminal of the SOP

Threshold Name	Voltage (V)	Operation
Voltage positive sequence upper threshold set	> 250	When voltage is greater than threshold, SOP should initiate support function for high voltage
Voltage positive sequence upper threshold reset	< 240	When voltage is less than threshold, SOP should switch off support function for high voltage
Voltage positive sequence lower threshold reset	> 230	When voltage is greater than threshold, SOP should switch off support function for low voltage
Voltage positive sequence lower threshold set	< 220	When voltage is less than threshold, SOP should initiate support function for low voltage

When a set is triggered, the algorithm will ramp-up (integrate) the output in order to solve the constraint. When the set signal is released, the algorithm will stop the integrate function and hold the output. When the network constraint is no longer present, a reset signal will be triggered. Upon triggering of this reset signal, the SOP will reduce the output towards zero.

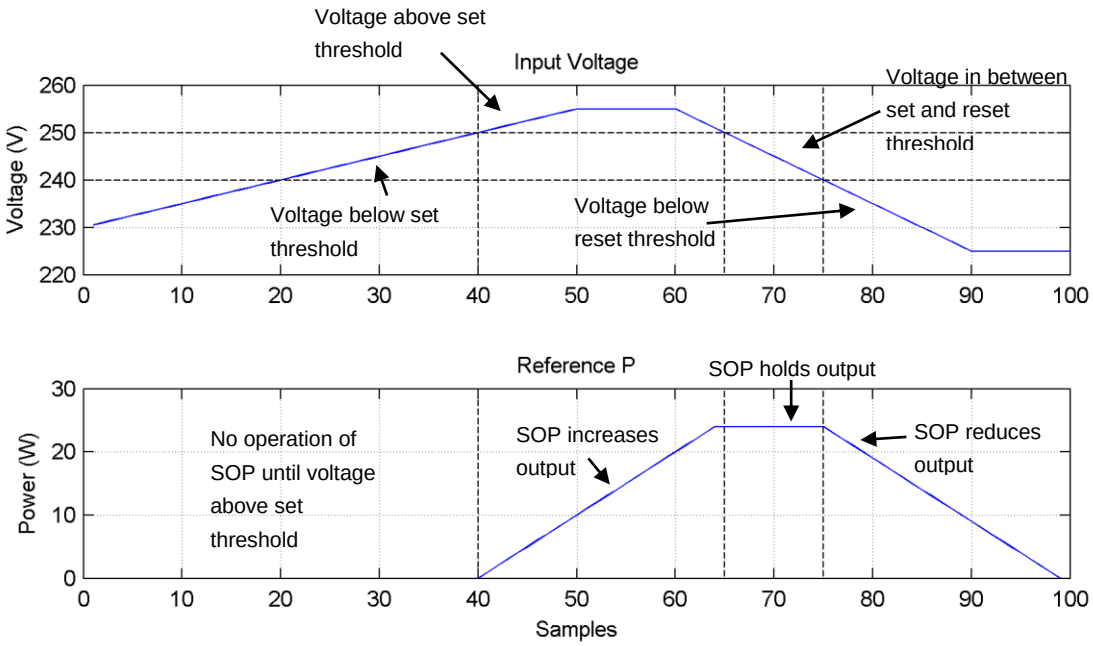


Figure 4.1: Graph showing a simplified operation of the controller

Figure 4.1 shows a simplified operation of the integral with hysteresis controller. The set threshold is set at 250 V and the reset threshold is set at 240 V. The measured voltage, which is an input to the controller, is shown in the top graph and the response of the controller, which is the power reference and output of the controller, is shown in the bottom graph. When the input voltage as measured by the controller is above 250 V (which is between samples 40 and 65), then the output of the controller increases as seen in the bottom graph. When the input voltage is between 240 V and 250 V then the output of the controller is held, as shown in samples 65 to 75. When the input voltage is below 240 V, then the output of the controller is decreased until the power reference is zero. This is shown between samples 75 and 100.

Operational Data

The voltage test was conducted at the PNDC at 15:12 and terminated at 17:04 on 21st April 2015. Initially the SOP and load banks were configured for the test. Once completed, the voltage at the substation that Inverter B was connected to was decreased from nominal by the use of taps at the secondary side of the substation transformer. The voltage was tapped down to the lowest tap (-11) then tapped up to the maximum tap (+16) before being tapped back to nominal (-4).

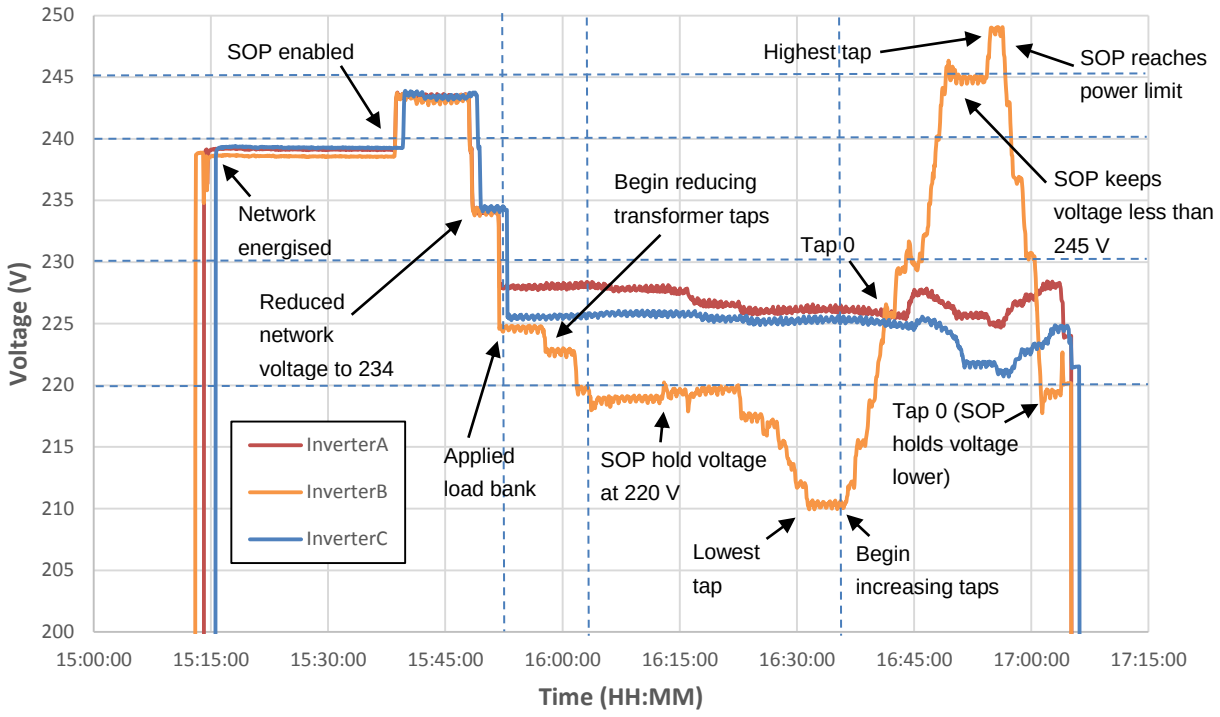


Figure 4.2: RMS voltage at the terminals of the SOP for the voltage constraint as measured by an external power analyser

Figure 4.2 shows the RMS voltage at the terminals of the SOP as measured by an external power analyser. The voltage was initially set to 240 V on all of the three ports at 15:15. The voltage was reduced at the secondary side of the transformer to 234 V at 15:50 and then a load of 80 kVA at 0.8 pf was applied to Inverter B and Inverter C. At 15:59 the voltage at Inverter B was reduced by 1 tap and 222 V was observed at the terminal of Inverter B. The voltage was continued to be tapped down by 1 tap every minute until -11 taps were reached at 16:36. The inverter started to support at 16:03 when the voltage at the terminal of the SOP was 218 V. This is 2 V less than the threshold setting of 220 V. Inverter B continues to support while the voltage at the secondary side of the substation was tapped down and maintained the voltage at the terminal of Inverter B between 218 V and 220 V. The SOP stopped supporting the voltage at 16:23 when the SOP reached the maximum power of 115 kW as set in the algorithm settings. The voltage at the terminal of the SOP reduced until 210 V was reached. The voltage was then tapped up at intervals of 2 taps until +14 taps was reached at the secondary side of the transformer. The voltage at the terminal of the SOP was 247 V and the SOP started to support the high voltage. The SOP maintained the voltage at the terminal between 247 V and 245 V until 16:50 where the voltage started to increase towards 250 V when the SOP again reached the maximum power of 115 kW as set in the algorithm settings. The voltage was then tapped down at 16:54 and the test was completed.

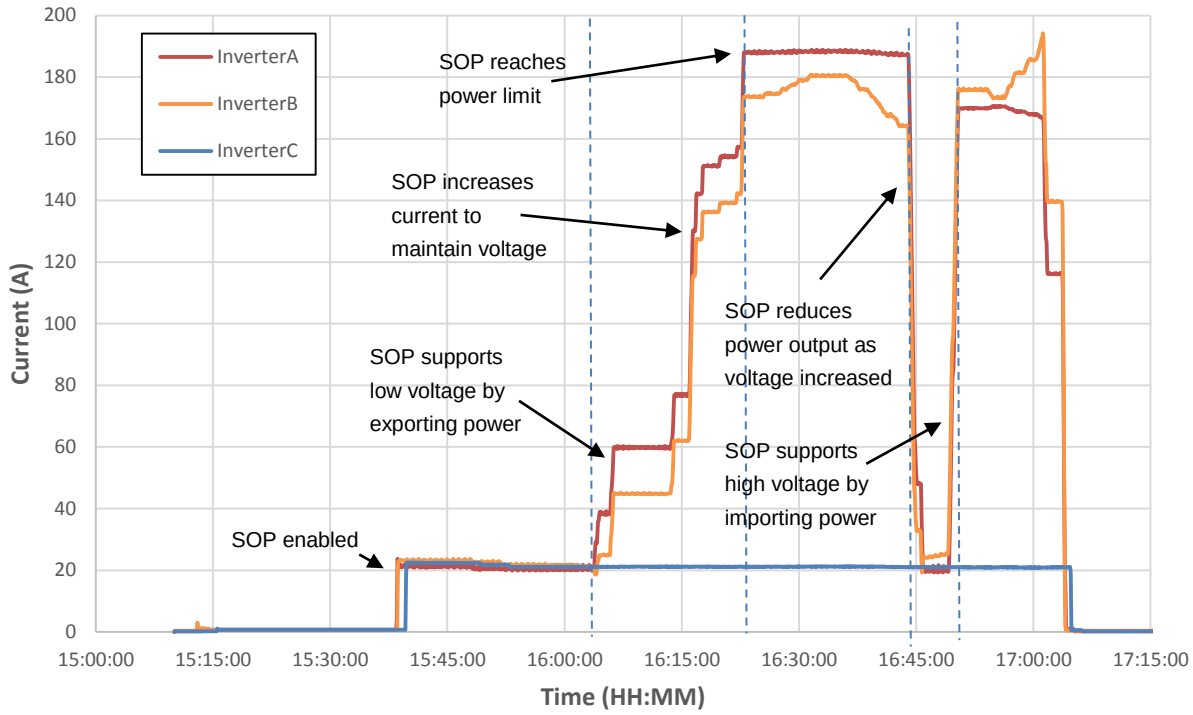


Figure 4.3: RMS current at the terminals of the SOP for the voltage constraint as measured by an external power analyser

Figure 4.3 shows the RMS current as measured by an external power analyser at the terminals of the SOP. It can be seen that both Inverter A and Inverter B have a similar current profile whereas Inverter C has a flat current profile. Version 1 of the algorithm does not utilise both ports when providing the opposite power flow for the port that is supporting unless a port providing reverse power flow reaches a limit. The feature of using two ports when no limits have been reached in order to provide reverse power for the other port which is supporting the constraint is a feature of Version 2. At 16:03 when the threshold of Inverter B is triggered, Inverter B starts to inject current into the network. Current injection increases until 16:23 when the current output at the terminal of the SOP is held constant. The current output is reduced at 16:44 and starts to increase again at 16:48 in order to support the high voltage.

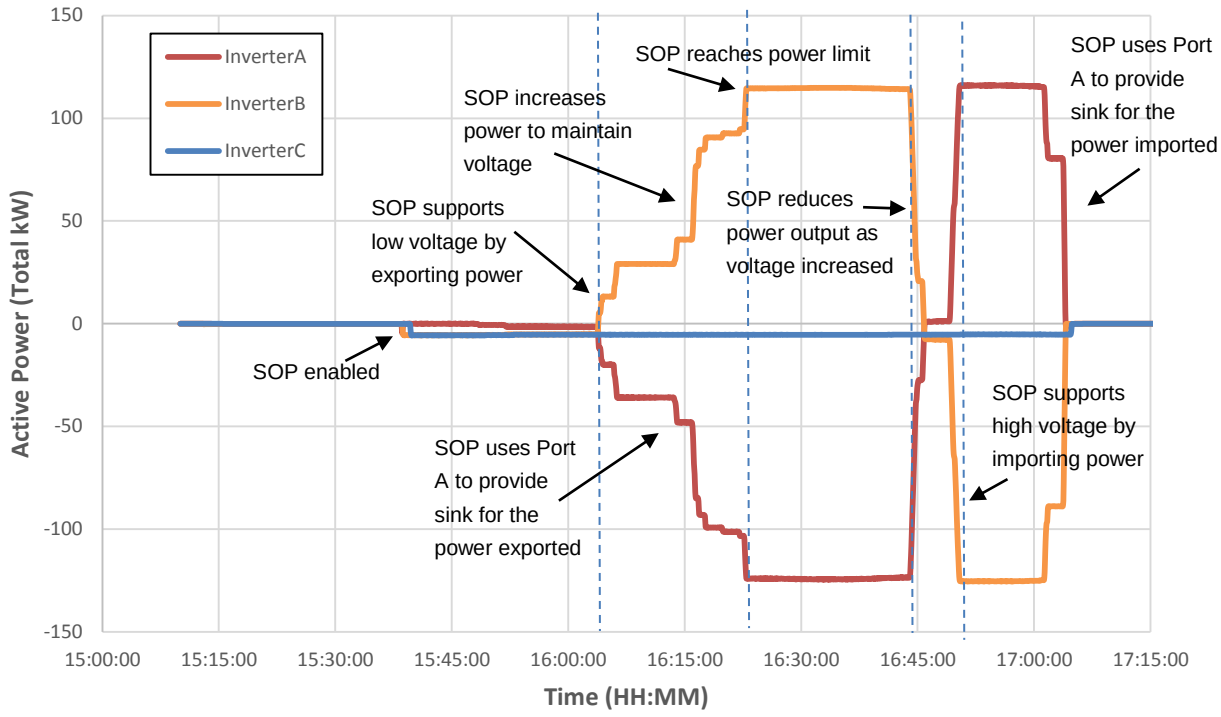


Figure 4.4: Power exported and imported at the terminal of the SOP as measured by an external power analyser, positive power is export and negative power is import

Figure 4.4 shows the active power export and import as measured by an external power analyser at the terminals of the SOP. Positive power is injection (generation) into the network and negative power is absorption (load). It can be seen that when Inverter B is injecting power, Inverter A is absorbing power and when Inverter B is absorbing power, Inverter A is injecting power. This demonstrates power transfer between the two substations that Inverter B and Inverter C interconnect.

At 16:30 when the threshold of Inverter B is set, Inverter B starts to inject power into the network in order to increase to voltage. Power injection increases until 16:23 when the power limit is reached and the algorithm is hold the power export constant. This demonstrates the algorithms ability to prevent the SOP exporting more power than set by the user. For example one port of the SOP may be connected to a smaller feeder or smaller transformer and the port will need to ensure it doesn't exceed the rating of the network assets. Power injection on Inverter B is reduced at 16:44 and Inverter B starts to absorb power at 16:48 in order to support the high voltage constraint.

Demonstration of power transfer

The SOP algorithm was programed to autonomously run and the algorithm determined the power set points. The points of interest from the test are as follows.

The inverter started to support at 16:03 when the voltage at the terminal of the SOP was 218 V. This was 2 V less than expected. The algorithm processes the voltage as a 16-bit integer and all voltage measured are rounded to the nearest integer. The rounding process causes a rounding error as 218.3 V will be interpreted as 218 V and 218.6 V will be interpreted as 219 V. The algorithm measures the three phase voltage and calculates the positive sequence voltage. The rounding of the voltages will mostly cause a rounding error for the result of the positive sequence voltage calculation. Another factor to consider is the threshold code. The threshold code uses a “less than” operator and not a “less than or equal to” operator for the lower voltage threshold. The user, through the HMI, programed the algorithm to support when the voltage was below 220 V. This use of the “less than” and not the “less than or equal to” operator will mean that the calculated positive sequence voltage will need to be less than 220 V. The next integer voltage less than 220 V is 219 V. It is expected that the algorithm should start operating when the voltage is less than or equal to 219 V. For these two reasons, a two volt difference was observed between the threshold setting and the measured voltage to when the SOP started to operate.

Between 16:03 and 16:23 the voltage is below the lower voltage threshold and between 16:48 and 16:51 the voltage above the upper voltage threshold. During these times the SOP algorithm operates autonomously to support the network voltage until the SOP power limit within the algorithm is reached. Once the SOP power limit is reached, the SOP is no longer able to maintain the voltage within the specified threshold settings.

5. Feeder Load Constraint

Designed Operation

The current of the secondary side of the transformer and connection of the feeder to the transformer was measured using external sensors (i.e. sensors that are external to the SOP, and not part of the SOP hardware). The external sensors were connected to the SOP via RTUs and communications using DNP3 via GPRS over the UK Power Network infrastructure. The RMS current of each of the three phases is read as an input to the algorithm. The algorithm calculates the positive sequence set of the current and uses this calculated measurement to determine if support is required. When the current at the transformer or feeder is in phase with the voltage (power is being imported) and is above the import current threshold set, the SOP will act as a source and inject power to reduce load on the transformer or feeder. This enables capacity to be shared between different transformers. Once the current is less than the import current threshold set, the SOP will hold the amount of export power. The power export (generation) the SOP presents to the port will reduce once the current at the substation or feeder is less than the import current reset. When the current is 180 degrees out-of-phase with the voltage (power is being exported) and if this is greater than the export current threshold set, the SOP will import power in an attempt to provide load to the feeder or transformer and reduce the generation fed back to the 11 kV network. This situation may occur on the network when there is a large amount of DG connected but only a small amount of load, for example noon on a day during summer. Once the current is less than the export current threshold set, the SOP will hold the amount of power import. The load the SOP presents to the port will reduce once the current at the feeder or transformer is less than the export current reset. Table 5-1 shows the current level set at the PNDC.

Table 5-1: Current thresholds for the current at the secondary side of the transformer and feeder connection to the transformer for successful operation of algorithm at PNDC after tuning the parameters

Threshold Name	Current (A)	Operation
Current import threshold set at feeder and transformer	> 100	When current import is greater than the threshold, SOP should initiate support function for import current
Current import threshold reset at feeder and transformer	< 80	When current import is less than the threshold, SOP should switch off support function for import current
Current export threshold set at feeder and transformer	> 100	When current export is greater than the threshold, SOP should initiate support function for export current
Current export threshold reset at feeder and transformer	< 80	When current export is less than the threshold, SOP should switch off support function for export current

When a set is triggered, the algorithm will ramp-up (integrate) the output in order to solve the constraint. When the set signal is released, the algorithm will stop the integrate function and hold the output. When the network constraint is no longer present, a reset signal will be triggered. Upon triggering of this reset signal, the SOP will reduce the output towards zero. This is shown in Figure 5.1.

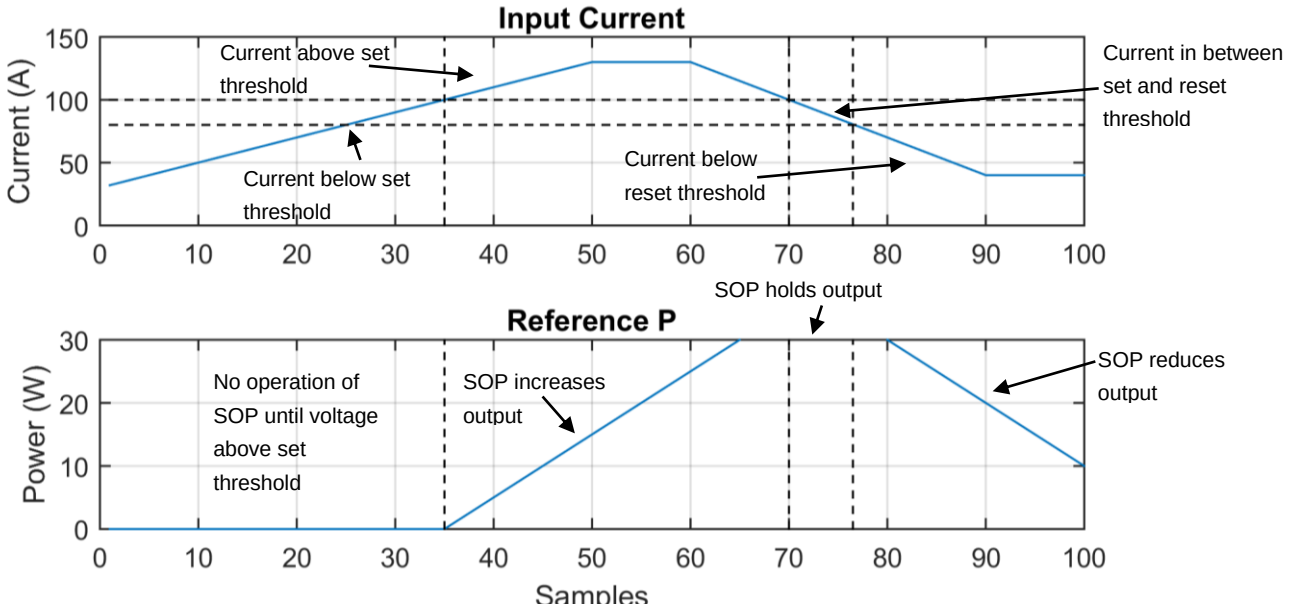


Figure 5.1: Graph showing a simplified operation of the controller for transformer and feeder load support

The load bank connected to the feeder that Inverter B was connected to was increased in steps of 10 kW increments from 0 kW to 80 kW. Two sets of remote sensors were placed at the transformer-end of the feeder to represent the measurements from the secondary side of the transformer and the feeder connection to the transformer. Thresholds in the algorithm were programmed to respond and support the feeder when the load was greater than 72 kW (100 A per phase at 240 V per phase) and to stop supporting the feeder when the load was less than 57.6 kW (10 A per phase at 240 V per phase). The data connection to the remote sensors was via the UK Power Network communication network to demonstrate the operation of the SOP in the field.

Operational Data

Figure 5.2 shows the current at the output of the SOP for the duration of the experiment as measured by an external power analyser. When the SOP was operating power was being transferred from Inverter A to Inverter B as shown by the profile of current from Inverter A matching the profile of current from Inverter B. The difference in current is a result of the losses for both the switching circuits, control electronics and cooling system.

At the beginning of the test (10:00 until 11:45), the parameters in the algorithm were not set correctly and the SOP experienced hunting. This lead to the algorithm ramping the power transfer up and down as can be seen by the ramping up and down of current. After 11:45, the correct parameters were entered in the algorithm and the SOP reached steady state. The load was increased to 80 kW and Inverter B transferred 30 A per phase to support the feeder such that the measurement was between 57.6 kW and 72 kW. Once stable operation was achieved the load was reduced and the SOP stopped transferring power as support was no longer required.

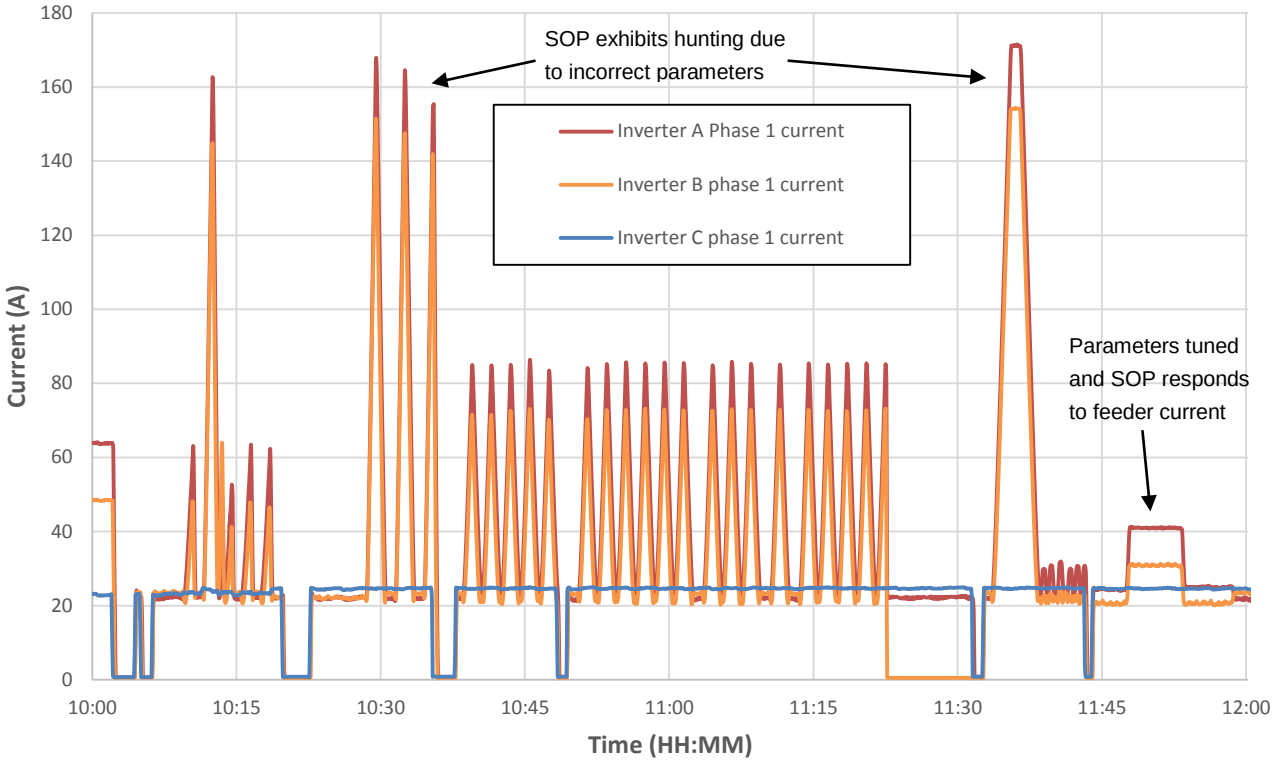


Figure 5.2: RMS current at the terminals of the SOP for the feeder load constraint as measured by an external power analyser

Figure 5.3 shows the power at the terminals of the SOP. It can be seen that when Inverter B requested power to support the feeder and transformer on port A, power transfer occurred from Inverter A to Inverter B. A load constraint was placed on the feeder and the algorithm responded by exporting power from Inverter B to reduce the load as seen by the remote sensors at the secondary-side of the transformer and as seen at the feeder connection to the

transformer. Between 11:45 and 12:00, the SOP transferred 20 kW of power from Inverter A to Inverter B to solve the load constraint.

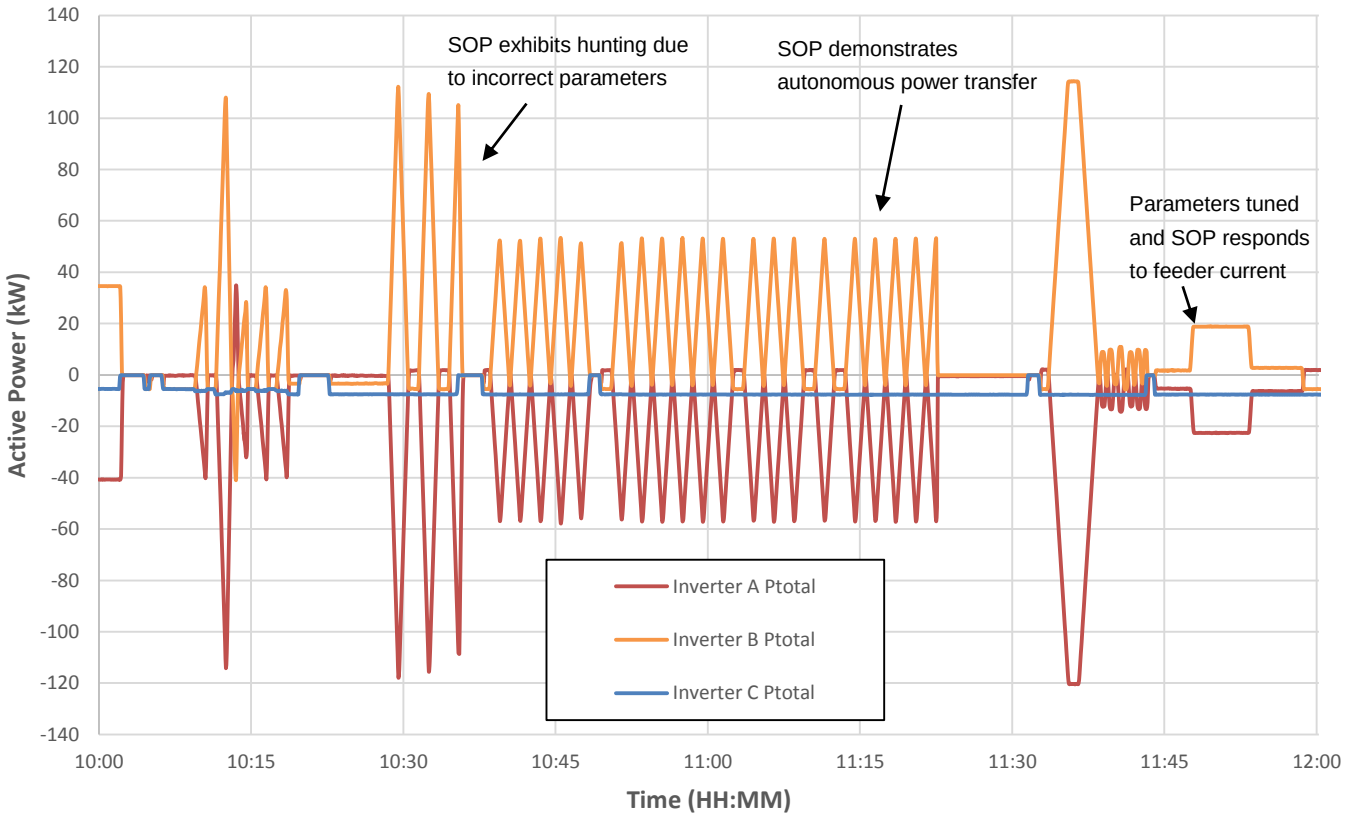


Figure 5.3: Power exported and imported at the terminal of the SOP as measured by an external power analyser, positive power is export and negative power is import

6. Network Configuration at Church Street

The SOP at the Church Street substation in Brighton was configured as shown in Figure 6.1.

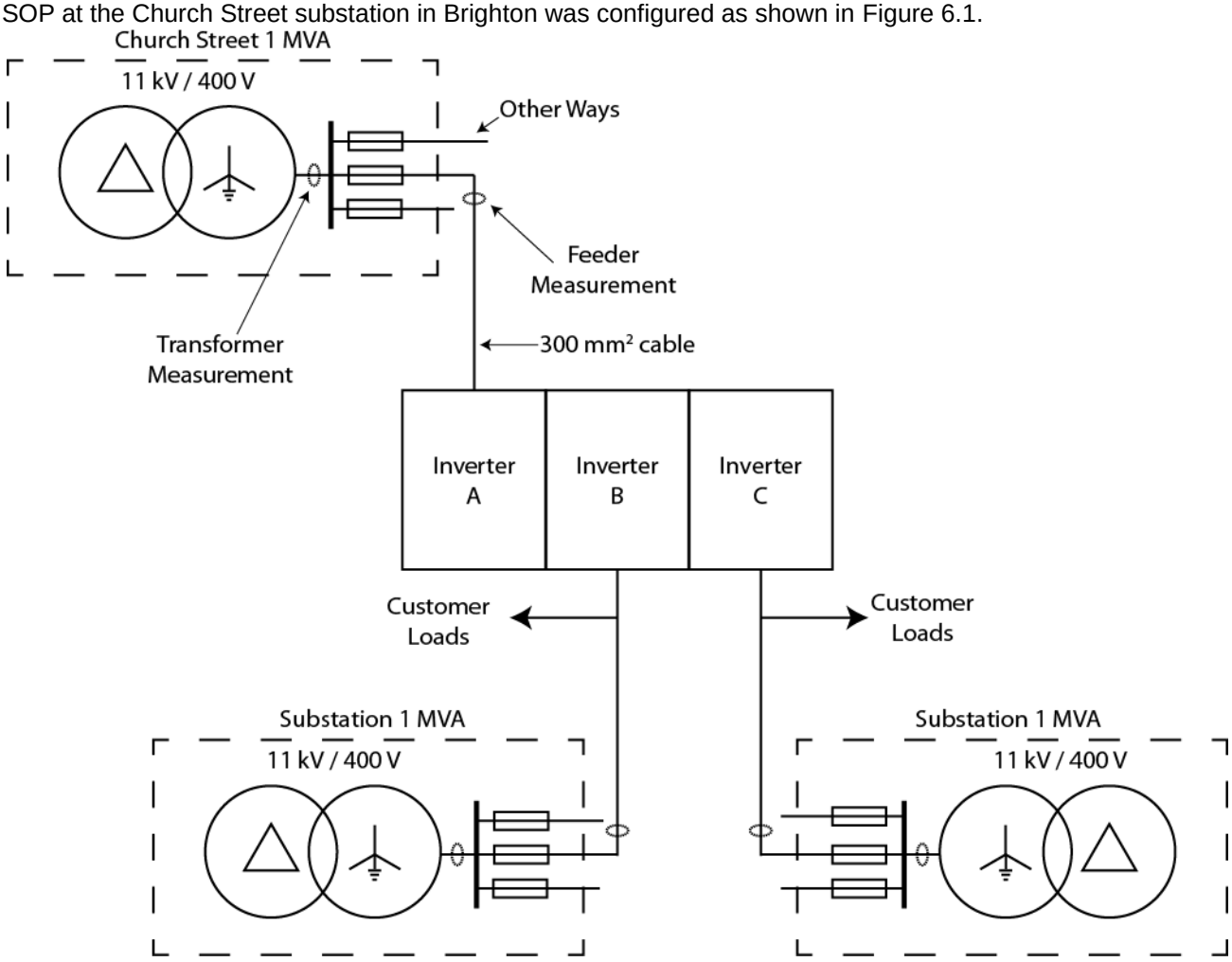


Figure 6.1: Diagram of the SOP connection at Church Street (one of the sites selected for the field trials)

7. Transformer Equalisation

Designed Operation

The aim of transformer equalisation is to balance the transformer load according to the capacity of the transformer. If there are two transformers in the network and transformer 1 is operating at 50 % utilisation and transformer 2 is operating at 100 % utilisation then the transformer equalisation algorithm will transfer load from transformer 2 to transformer 1 such that both transformers are operating at 75 % capacity.
Utilisation of the transformer is calculated as a percentage of the load with respect to the maximum power rating of the transformer. If the transformer is supporting a load of 600 kW and the rating of the transformer is 1000 kW then the utilisation of the transformer would be 60 %.

$$Transformer\ utilisation(\%) = \frac{Transformer\ load\ (W)}{Transformer\ rating\ (W)} \times 100$$

The utilisation of each transformer is compared to the average utilisation. Average utilisation is the summation of the utilisations from the transformer at each of the SOP ports, divided by the number of transformers connected to the SOP. If the utilisation of one of the transformers is less than the average utilisation then the transformer is under-utilised and greater loading is required. If the utilisation is greater than the average utilisation then the transformer is over utilised and less loading is required.
If the transformer has reverse power flow and the transformer is exporting power from the 400 V network to the 11 kV network, then the transformer is not loaded and the utilisation is considered to be zero. A future version of the algorithm may wish to consider when the transformer has reverse power flow.
This support function has two constraints

1. Transformer under-utilised
2. Transformer over-utilised

When the transformer is under-utilised more load is required and when the transformer is over-utilised then less load is required. The SOP will transfer power to either increase the loading by importing power from the network or decrease the loading on the transformer by exporting power into the network. The set and reset thresholds can be changed to increase or decrease the operational dead-band.

Field trial data (Event 1)

Figure 7.1 shows the response of the SOP from 13:10 until 14:00 on 12 August 2015. Real power, reactive power, RMS voltage and RMS current are shown for each of the three ports. The measurements from the three transformers are shown in Figure 7.2 and the status of the algorithm thresholds are shown in Figure 7.3. Real power transfer mode has been enabled and all other modes of operation have been disabled. This means the SOP will only solve feeder and transformer constraints. The thresholds related to voltage, reactive power and unbalance will be ignored and the SOP will operate until the voltage reaches either a minimum or a maximum of 216 V or 250 V respectively.

From Figure 7.3, it is possible to determine the function that the algorithm supports. At 13:10, the transformer connected to Port A has a smaller percentage of load with respect to the transformer capacity than the other

transformers. This is shown by the “set” signal for the graph “Tx Load Low” for Port A is high. For Port B, the transformer loading as a percentage of the transformer capacity is greater than the other transformers. The “set” signal for the graph “Tx Load Hi” is high. For Port C, none of the set signals are high. To equalise the transformers connected to Port A and Port B, the SOP must import power from Port A and inject power into Port B. Figure 7.1 at 13:10 shows the SOP importing power from Port A and exporting power to Port B. In the power graph of Figure 7.2 it can be seen that the load on Port A increases and the load on Port B decreases.

At 13:17, the graph “Tx Load Hi” in Figure 7.3 shows the SOP close to solving the transformer load and the “set” signal starts to change from a high state to a low state. Consequently, the SOP holds the output on Port B as can be seen by the power demand in Figure 7.1 for Port B not changing. While the condition on Port B has been solved, the requirement for Port A has not been solved. None of the real power transfer support functions for Port C are set and the algorithm starts to export power into Port C in order to increase the import from Port A. The export of power into Port C causes the voltage to slightly rise and the voltage asset guarding feature for high voltage then reduces the export power to zero. The increase and decrease of real power on Port C between 13:17 and 13:25 can be seen in Figure 7.1. When the algorithm is reducing the export power on Port C, it decides to increase the export power on Port B as opposed to decreasing the import port on Port A. While the SOP is solving the asset guarding requirement, the power output for Port A does not change.

Figure 7.3 shows that between 13:35 and 13:40, the transformer for Port A has increased the loading and has a greater load with respect to its capacity than the average loaded across the other transformers. It would be expected that the SOP should back off the power demand on Port A in order to reduce the loading on the transformer. However Figure 7.1 shows that the SOP continues to load the transformer until 13:34 where by the SOP starts to decrease the real power import from Port A. One explanation is that from 13:25 until 13:34, Port B requires more export to reduce the load on the Transformer connected to Port B since the “set” signal in Figure 7.3 is high. The increase in load on Port A causes the feeder current to trigger the “set” signal and this causes the SOP to reduce the load as seen in Figure 7.1. At 13:40, the feeder import current reduces below the limit and the load of the transformer is less than the average loading. The SOP should stop the decrease in import and increase the import to solve the transformer constraint. However, the SOP continues to decrease the output until the power output is zero. Once the port has reset, the SOP starts to increase the import for port A.

When the SOP is reducing the import for Port A, it decides to balance the SOP by reducing the export from Port C as this port is not supporting a network constraint. Once the export on Port C is zero, the SOP starts to import from Port C in order to leave Port B supporting the transformer load. No changes are made to Port B between 13:34 and 13:42. At 14:42, the transformer load on Port C goes above the average loading and the SOP hold the import on Port C and starts to reduce the export on Port B. The SOP continues to reduce the export on Port B until the import on Port A is zero at 13:52. From 13:52, the SOP starts to increase the loading on Port A and uses to Port B to increase the export. The loading on Port C also increases which it should not as the load on the transformer is already greater than the average. Further investigation is required to understand if this is an issue in the release of the algorithm currently in testing or if further modification is required to prevent this from happening.

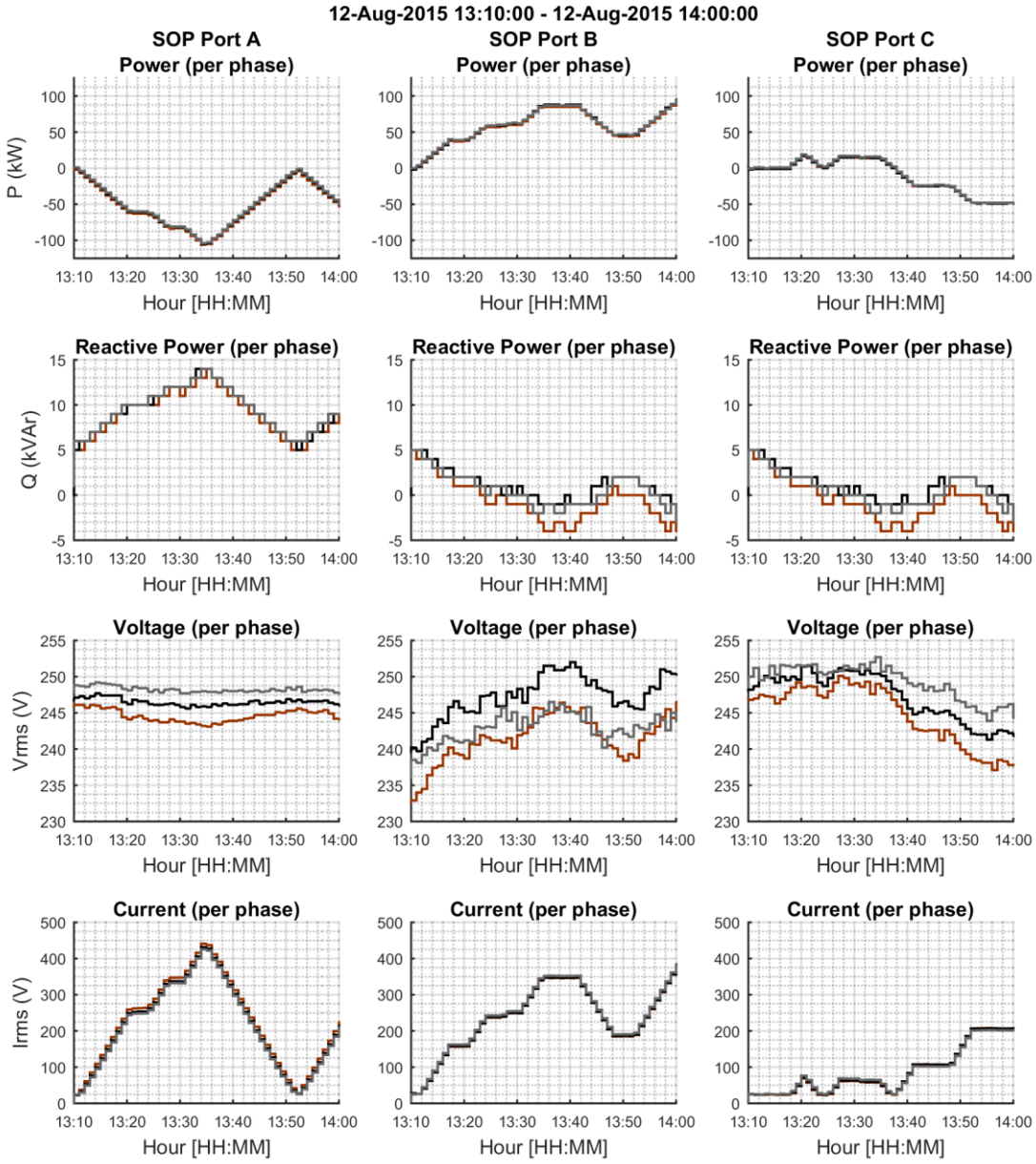


Figure 7.1: Event 1 of the SOP transferring real power to equalise the transformer loading

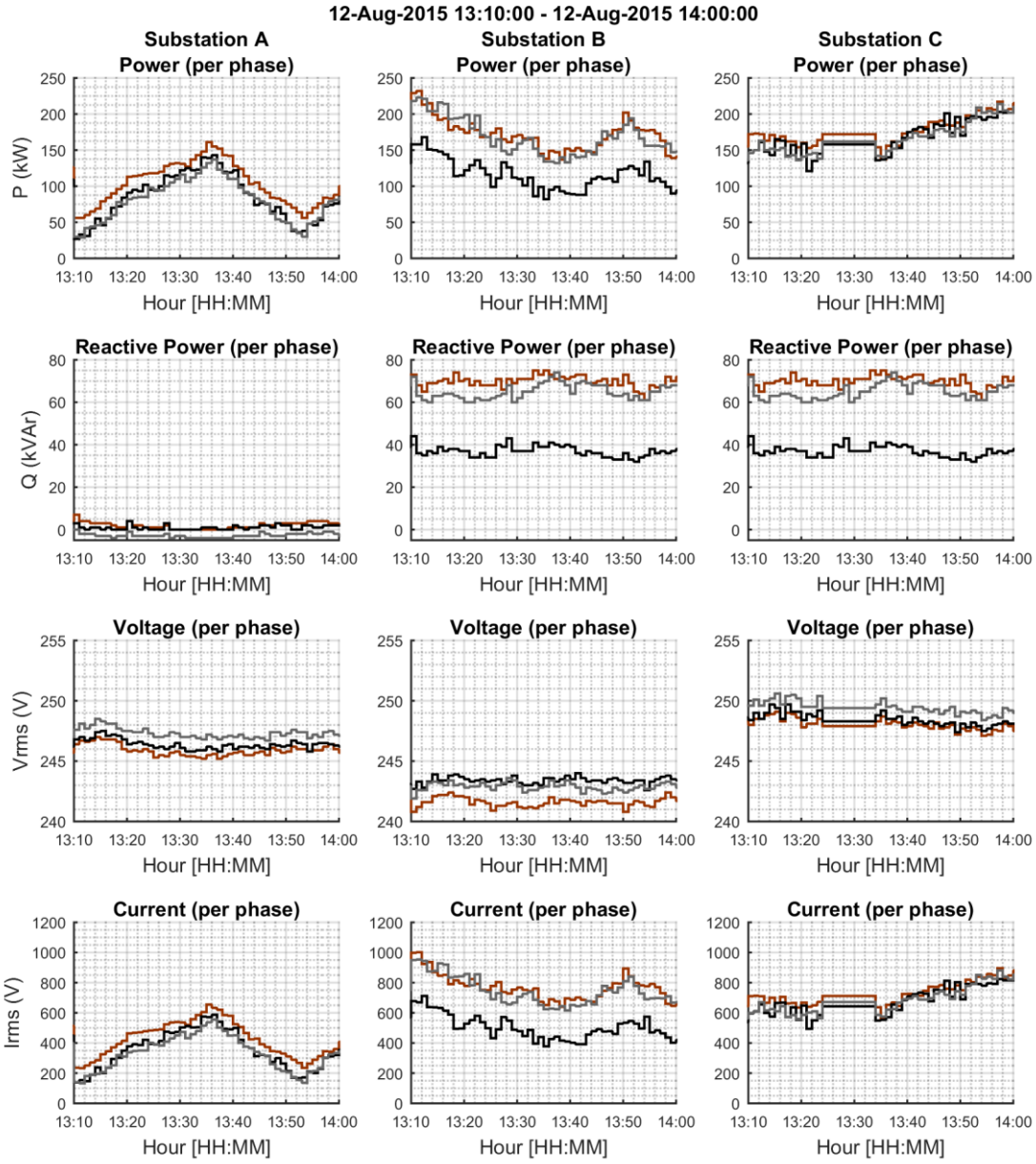


Figure 7.2: Measurements from the transformer during event 1

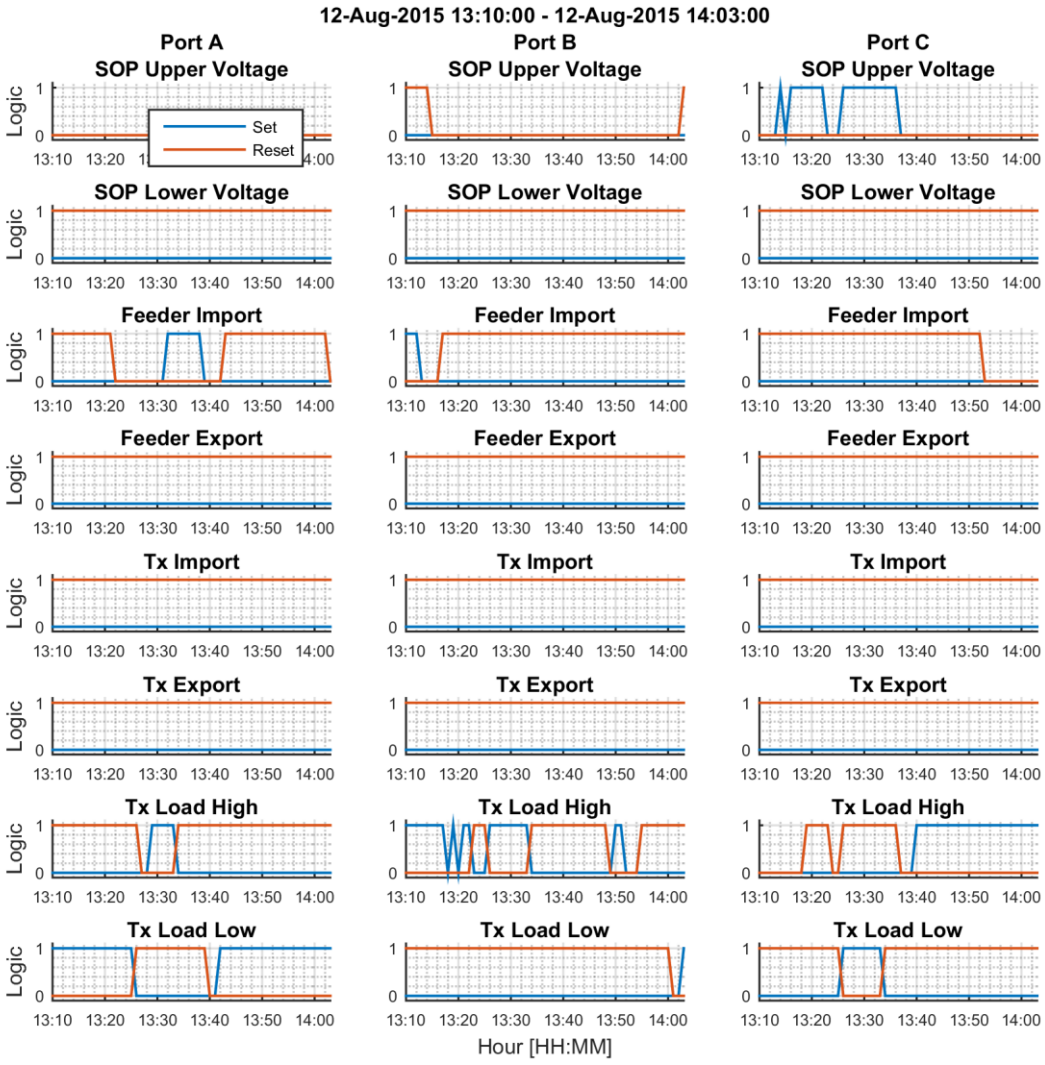


Figure 7.3: Status of the thresholds in the algorithm for event 1

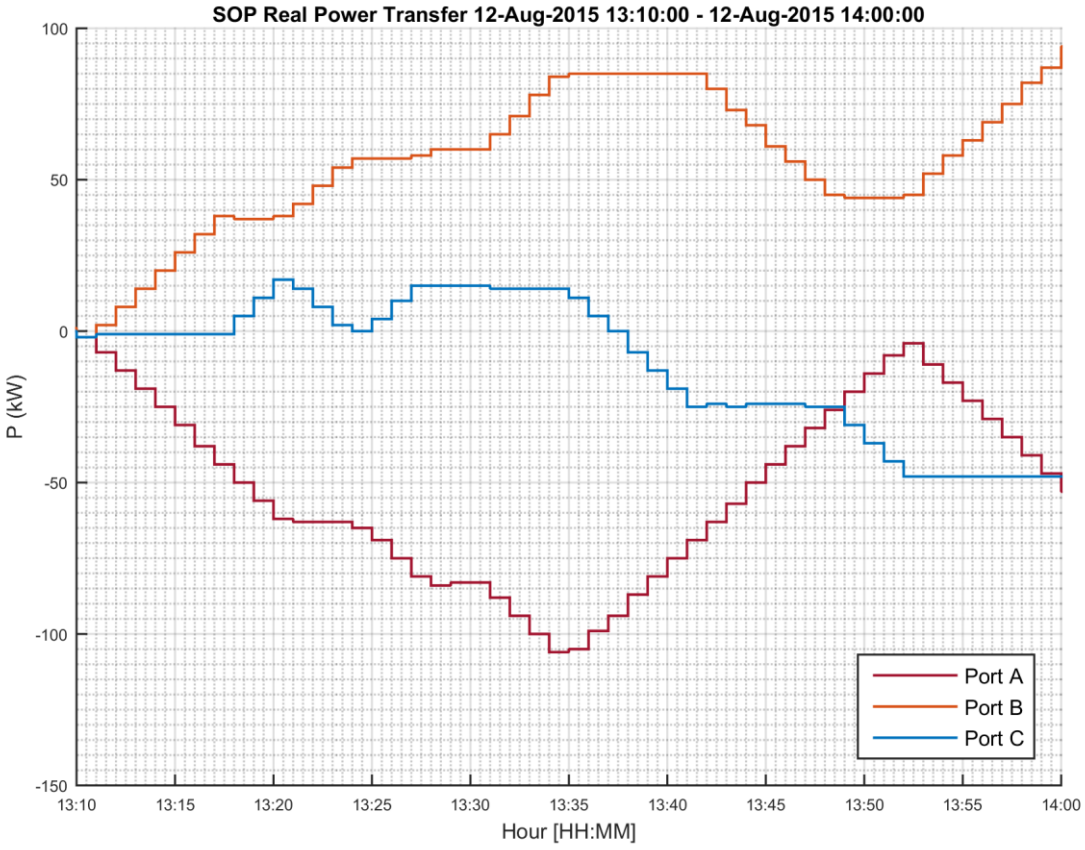


Figure 7.4: Comparison of the real power transfer for phase L1 of each of the three ports showing autonomous power transfer for event 1.

Field trial data (Event 2)

Figure 7.5 shows the response of the SOP, Figure 7.6 shows the measurements at the transformer and Figure 7.8 shows the threshold status for a second transformer equalisation event. From Figure 7.8, it can be seen that the transformer at Port A is under-utilised as the “set” signal for the graph called “Tx Load Low” is high. The transformer at Port B is over-utilised as the “set” signals for the graph called “Tx Load Hi” is high. For Port C, the reset signal for “Tx Load Hi” is low and this suggests that the load is within the dead-band but greater than the average utilisation. For the SOP to solve this constraint and equalise the transformer loadings, the SOP should import from Port A and export to Port B. There may be a small amount of export required for Port C as the average may change when the SOP operates. Since the volts are already high for Port C, the amount of export the SOP will be able to do is limited.

The SOP increases import on Port A and reaches a steady-state at 14:45 at a power import of 60 kW. The algorithm uses Port B to export the power and this reduces the loading on the transformer. A small amount of power is exported to Port C. Since there is a volatility in the load at the transformer, the SOP is constantly adjusting the power import and power export. The volatility is also visible in Figure 7.8 where the “set” signal for the graph “Tx Load Low” for port A, and the “reset” signal for the graph in “Tx Load Hi” for Port B is changing. This is expected and the dead-band between the “set” and “reset” setting is designed to prevent the SOP from ramping up and ramping down and to prevent the SOP form making transfers for only a small amount of equalisation.

The effect of the SOP on the transformer load is visible in Figure 7.6. The load on Port A can be seen to be increasing from 50 kW to 100 kW and being reduced from 200 kW to 150 kW for Port B. The load at Port C is already 150 kW and this does not need increasing or decreasing.

The autonomous power transfer for phase L1 of the SOP is shown in Figure 7.8 which is the same data as shown in Figure 7.5.

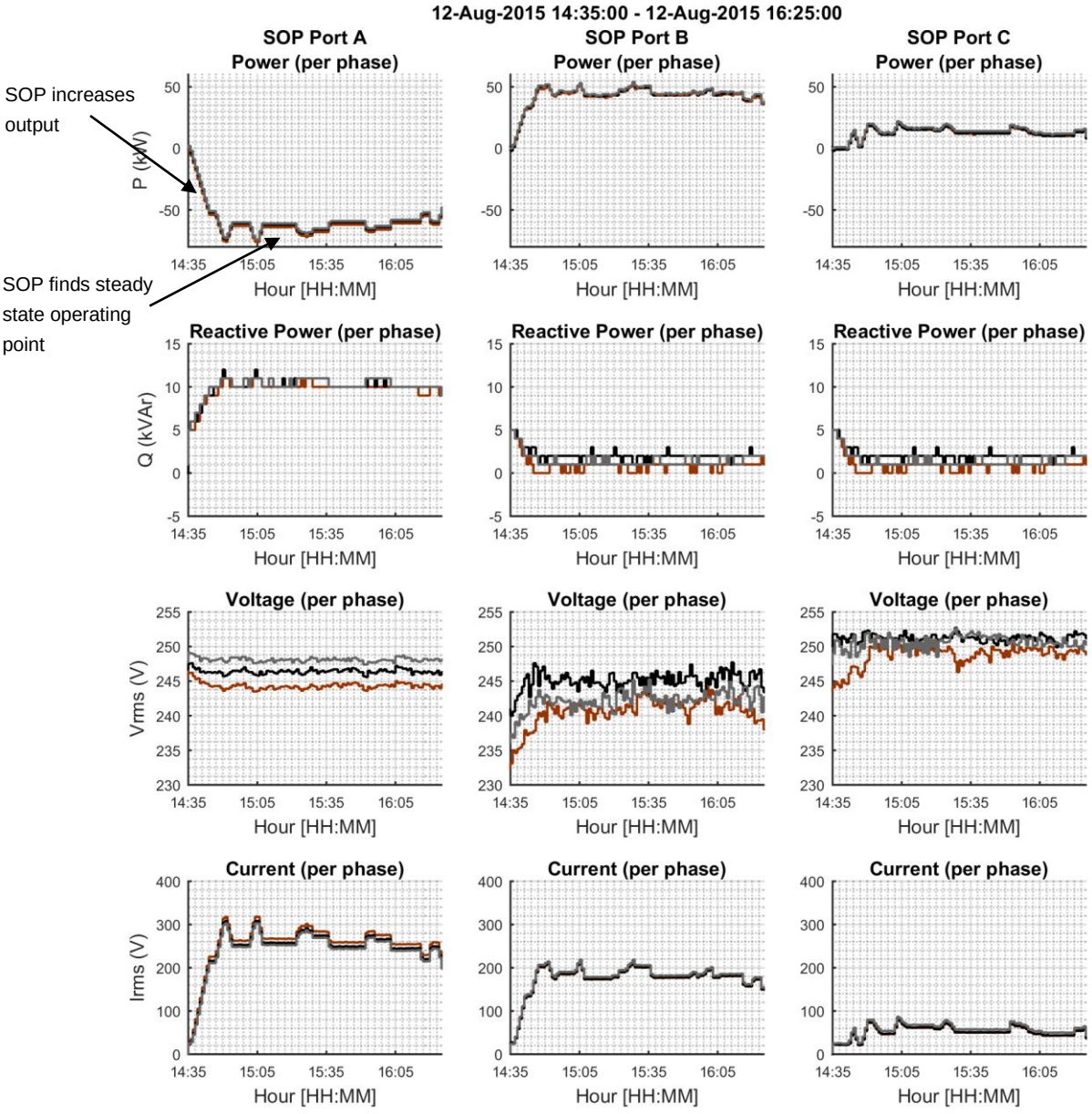


Figure 7.5: Event 2 of the SOP transferring real power to equalise the transformers

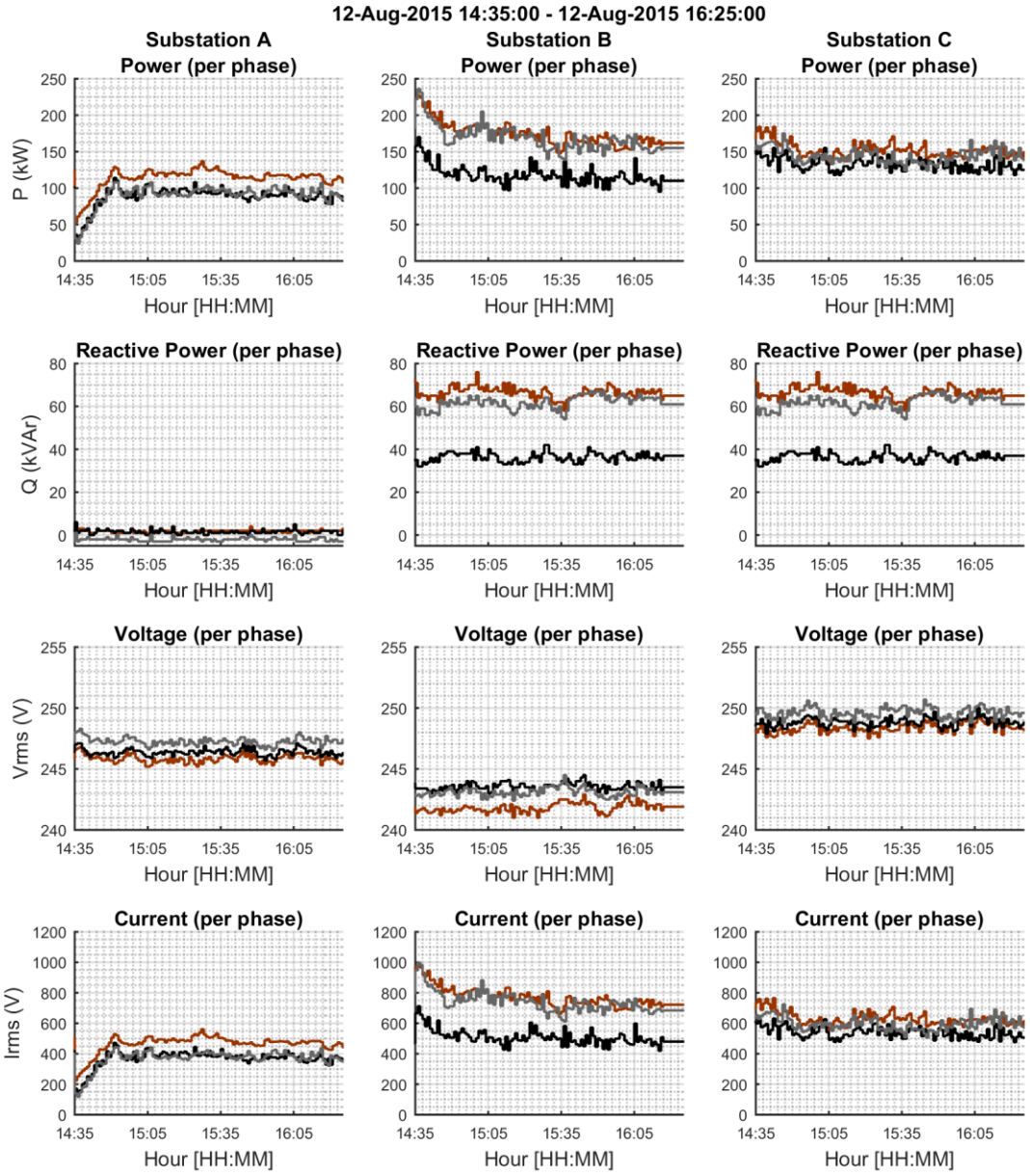


Figure 7.6: Measurements from the transformer during event 2

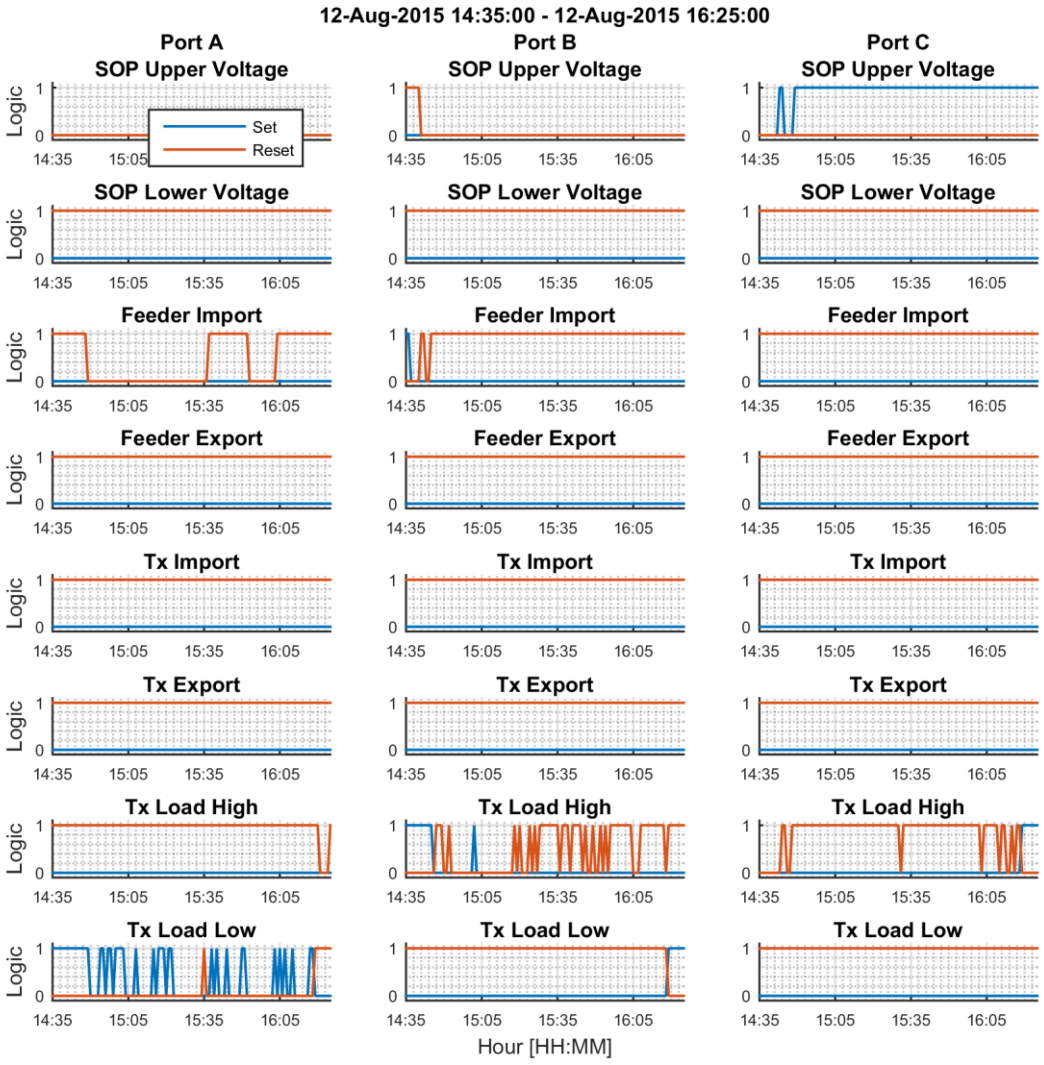


Figure 7.7: Status of the thresholds in the algorithm for event 2

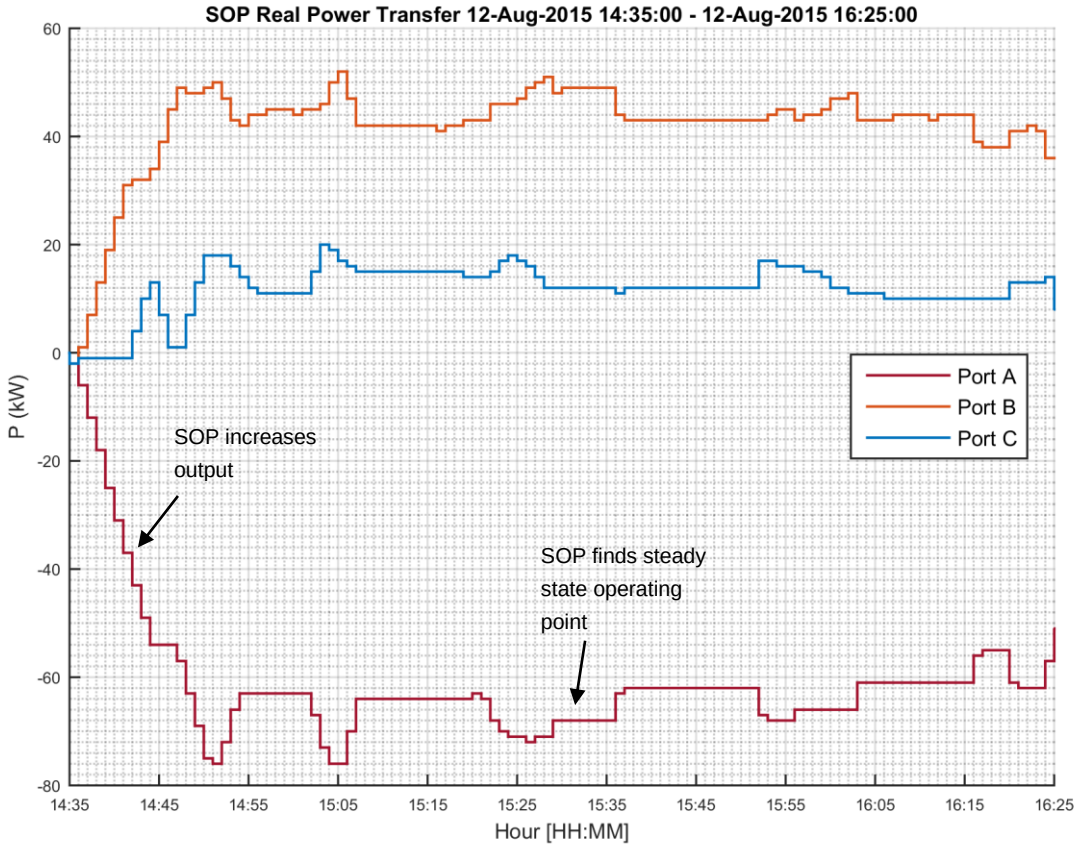


Figure 7.8: Comparison of the SOP power export on phase L1 for all three ports for event 2.

8. Conclusion

This report has demonstrated that the SOP and the SOP algorithm are able to autonomously transfer power from one feeder to another feeder in order to solve voltage and load constraints within the low-voltage network. This tests at PNDC highlighted that care should be taken when selecting the thresholds as incorrect settings can cause the SOP to ramp-up (to solve the constraint) and then immediately ramp down because during the ramp-up process the SOP has transferred more power than is required.

The algorithm was developed between the testing at PNDC and the field trials. The hunting issue identified from PNDC was solved. The field trial data emphasised that the SOP is able to autonomously transfer power between the three feeders in order to improve the load balance in the transformers. When balancing the transformers, the SOP needs to export to reduce the loading of the higher loaded transformer and import power to increase the loading of the lightly loaded transformers. When the SOP is exporting power, the voltage will rise, but since the voltage is already high, the SOP has limited success in exporting power.

From the field trial data it was notice that there were two sequences where the algorithm should behave differently. The first is when the algorithm reduced the output to zero when it only needed to reduce the output by a small amount when changing from reducing the feeder constraint to increasing the loading on the transformer. The second was when Port C increased its load but the port was not supporting an asset. A check should be included in the controller to prevent this from occurring. These will enable further development of the SOP algorithm.

Appendix A: Settings used for the SOP at Church Street

Table A-1: Threshold settings for the SOP

Threshold Name	Current (A)	Operation
Voltage positive sequence upper threshold set	≥ 250	When voltage is greater than threshold, SOP should initiate support function for high voltage on port A, B or C
Voltage positive sequence upper threshold reset	≤ 240	When voltage is less than threshold, SOP should reduce support function for high voltage on port A, B or C
Voltage positive sequence lower threshold reset	≥ 230	When voltage is greater than threshold, SOP should reduce support function for low voltage on port A, B or C
Voltage positive sequence lower threshold set	≤ 220	When voltage is less than threshold, SOP should initiate support function for low voltage on port A, B or C
Current import threshold set at feeder	≥ 350	When current import is greater than the threshold, SOP should initiate support function for import current on port A, B or C
Current import threshold reset at feeder	≤ 250	When current import is less than the threshold, SOP should reduce support function for import current on port A, B or C
Current export threshold set at feeder	≥ 350	When current export is greater than the threshold, SOP should initiate support function for export current on port A, B or C
Current export threshold reset at feeder	≤ 250	When current export is less than the threshold, SOP should reduce support function for export current on port A, B or C
Current import threshold set at	≥ 1120	When current import is greater than

transformer		the threshold, SOP should initiate support function for import current on port A, B or C
Current import threshold reset at transformer	≤ 900	When current import is less than the threshold, SOP should reduce support function for import current on port A, B or C
Current export threshold set at transformer	≥ 1120	When current export is greater than the threshold, SOP should initiate support function for export current on port A, B or C
Current export threshold reset at transformer	≤ 900	When current export is less than the threshold, SOP should reduce support function for export current on port A, B or C
Transformer equalisation high threshold set	≥ 20	When the different between the mean transformer utilisation and the transformer utilisation of the transformer on either port A, B or C, the SOP should export current.
Transformer equalisation high threshold reset	≤ 10	The threshold reset for the allowed different between the mean transformer utilisation and the transformer utilisation of the transformer on either port A, B or C the SOP should reduce export current.
Transformer equalisation low threshold set	≥ 20	The threshold set for the allowed different between the mean transformer utilisation and the transformer utilisation of the transformer on either port A, B or C, the SOP should import current.
Transformer equalisation low threshold reset	≤ 10	The threshold reset for the allowed different between the mean transformer utilisation and the transformer utilisation of the

		transformer on either port A, B or C, the SOP should reduce import current.