IOS-220
12-Bit High-Density Analog Output Board

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The I/O Server Module (IOS) Series IOS-220 module is a 12-bit, high-density, single-size IOS, analog output board with the capability to drive up to 16 analog voltage output channels. The IOS-220 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for many industrial control and scientific applications that require high-density, high-reliability, and high-performance at a low cost.

Important Note: The following IOS models are accessories to the IOS Server Models: IOS-7200, IOS-7200-WIN, IOS-7400, and IOS-7400-WIN; which are cULus Listed. This equipment is suitable for use in Class I, Division 2, Groups A, B, C, and D or non-hazardous locations only.

MODEL	# OUTPUTS	OPERATING TEMPERATURE RANGE
IOS-220-16	16	-40 to 85°C
IOS-220-8	8	-40 to 85°C

KEY IOS-220 FEATURES

- **High Channel Count** - Individual control of up to 16 analog voltage output channels is provided. Four units mounted on a carrier board provide up to 64 output channels in a single system slot.
- **12-Bit Accuracy** - Each channel contains its own 12-bit, Digital to Analog Converter (DAC) with an 11µS output settling time.
- **Bipolar Outputs** - Provides bipolar voltage range outputs: -10 to +10 Volts.
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration of the module.
- **Individual Output Control** - Output channels can be individually selected and updated with a single channel data write command when using the "transparent" output mode.
- **Simultaneous Output Control** - All output channels can be simultaneously updated with a single software trigger command when using the "simultaneous" output mode (DAC's are double-buffered which allows new data to be written to each channel before the simultaneous trigger updates the outputs).
- **Easy Mode Selection** - Selection of transparent and simultaneous output modes is easily done via software commands.
- **Reset is Failsafe** - Outputs reset to 0 volts following a power up or reset.
- **Conduction Cooled Module** - I/O modules employ advanced thermal technologies. A thermal pad and module cover wicks heat away from the module and transfers the energy to a heat spreading friction plate. Heat moves to the enclosure walls where it is dissipated by the external cooling fins.

I/O SERVER MODULE SOFTWARE LIBRARY

IOS MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows Embedded Standard applications interfacing with I/O Server Modules installed on Acromag Industrial I/O Server systems. This software (Model IOSSW-DEV-WIN) consists of a low-level driver and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic.NET, Borland C++ Builder and others. The DLL functions provide a high-level interface to the IOS carrier and modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IOS MODULE LINUX SOFTWARE

Acromag provides a software product (sold separately) consisting of Linux® software. This software (Model IOSSW-API-LNX) is composed of Linux libraries designed to support applications accessing I/O Server Modules installed on Acromag Industrial I/O Server systems. The software is implemented as a library of "C" functions which link with existing user code.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped. This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

The board may be configured differently, depending on the application.

Power should be removed from the board when installing IOS modules, cables, termination panels, and field wiring. Refer to your IOS module documentation for configuration and assembly instructions.

Default Hardware Configuration

A board is shipped from the factory configured as follows:

- Analog output range is -10 to +10 Volts and is not configurable.
- Programmable software register bits are undefined at reset, but the board defaults to 0 Volts on all analog outputs and the Simultaneous Channel Update Mode (see Section 3).

Programmable Register Configuration

Programmable registers are software configurable. That is, there are no hardware jumpers associated with them. Registers must be accessed to select the desired mode of operation and to update analog outputs (refer to Section 3 for details).

Analog Output Data Format

The bipolar output range (-10 to +10 Volts) is programmed with Bipolar Offset Binary (BOB) data to the Digital-to-Analog-Converter (DAC). The following table indicates the relationship between the data format and the ideal analog output voltage from the module.

Table 2.2: Bipolar Offset Binary (BOB) Output Data Format*

Analog Output Voltage (Volts)	BOB Data (Hex)
9.9951	FFF0
9.9902	FFE0
.	.
.	.
0.0049	8010
0.0000	8000
-0.0049	7FF0
.	.
.	.
-9.9951	0010
-10.0000	0000

* The BOB, 12-bit data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are shown as zero in the table, but actually it does not matter what is written to them.

CONNECTORS
IOS Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IOS modules to the carrier board. P2 is a 50-pin receptacle female header (Comm Con 8066-50G2 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity.

Table 2.3: IOS-220 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
+CH00	1	-CH12[1]	26
-CH00[1]	2	+CH13	27
+CH01	3	-CH13[1]	28
-CH01[1]	4	+CH14	29
+CH02	5	-CH14[1]	30
-CH02[1]	6	+CH15	31
+CH03	7	-CH15[1]	32
-CH03[1]	8	*RESERVED*	33
+CH04	9	*RESERVED*	34
-CH04[1]	10	*RESERVED*	35
+CH05	11	*RESERVED*	36
-CH05[1]	12	*RESERVED*	37
+CH06	13	*RESERVED*	38
-CH06[1]	14	*RESERVED*	39
+CH07	15	*RESERVED*	40
-CH07[1]	16	*RESERVED*	41
+CH08	17	*RESERVED*	42
-CH08[1]	18	COMMON[1]	43
+CH09	19	COMMON[1]	44
-CH09[1]	20	*RESERVED*	45
+CH10	21	*RESERVED*	46
-CH10[1]	22	NC[2]	47[2]
+CH11	23	*RESERVED*	48
-CH11[1]	24	NC[2]	49[2]
+CH12	25	COMMON[1]	50

Note: 1. The minus leads of all channels are connected to analog common on the module.
2. The ±12 volt analog power supplies are provided via the P1 connector by default. External power supply pins 47 and 49 can only be used if the IOS-220 is built at the factory for external analog power.

The field and logic side connectors are keyed to avoid incorrect assembly. P2 Pin assignments are unique to each IOS (see Table 2.3) and normally correspond to the pin numbers of the front panel, field I/O interface connector on the carrier board (you should verify this for your carrier board). In Table 2.3, channel designations are abbreviated to save space (i.e. channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively). Further, note the output signals all have the same ground reference ("-CH00" and the minus leads of all other channels are connected to analog common on the module).

Analog Output Noise and Grounding Considerations

All output channels are referenced to analog common on the module (See ANALOG OUTPUT CONNECTIONS for analog output connections), but each channel has a separate return (minus lead) to maintain accuracy and reduce noise. Still, the accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads $>$ 100KΩ) provide the best accuracy. For low impedance loads, the IOS-220 can source up to 5mA, but the effects of source and cabling resistance should be considered.

Output common is electrically connected to the IOS module ground. As such, the IOS-220 is non-isolated between the logic and field I/O grounds. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog outputs when a high level of accuracy/resolution is needed (e.g. 12-bits or more). Refer ANALOG OUTPUT CONNECTIONS for example output and grounding connections. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to provide isolated voltage or current outputs when used in conjunction with the IOS-220 output module.

3.0 PROGRAMMING INFORMATION

This board is addressable in the IOS module I/O space to control the level of analog outputs in the field and to read offset and gain calibration coefficients. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6. The IOS-220 uses this address space for enabling control signals for DAC functions and addressing offset and gain calibration coefficients used by the software to adjust the accuracy of the output range. The calibration coefficients are accessed via reads from EEPROM in the I/O space. The I/O space address map for the IOS-220 is shown in Table 3.1 below. Note the base addresses for the IOS module I/O space (see the I/O Server instruction manual) must be added to the addresses shown to properly access the I/O space.

ADDRESS MAPS

Table 3.1: IOS-220 I/O Space Address Memory Map

Base Addr + (Hex)	HIGH Byte D15 D08	LOW Byte D07 D00	Base Addr + (Hex)
01	(R/W) - DAC Channel 0		00
03	(R/W) - DAC Channel 1		02
05	(R/W) - DAC Channel 2		04
07	(R/W) - DAC Channel 3		06
09	(R/W) - DAC Channel 4		08
0B	(R/W) - DAC Channel 5		0A
0D	(R/W) - DAC Channel 6		0C
0F	(R/W) - DAC Channel 7		0E
11	(R/W) - DAC Channel 8[2]		10
13	(R/W) - DAC Channel 9[2]		12
15	(R/W) - DAC Channel 10[2]		14
17	(R/W) - DAC Channel 11[2]		16
19	(R/W) - DAC Channel 12[2]		18
1B	(R/W) - DAC Channel 13[2]		1A
1D	(R/W) - DAC Channel 14[2]		1C
1F	(R/W) - DAC Channel 15[2]		1E
21	(W) - Transparent Mode		20
23	(W)- Simultaneous Mode		22
25	(W) - Simultaneous Output Trigger		24
27	DAC Write Status Register		26
29		Control Register	28
2B	EEPROM Status	EEPROM Write Control	2A
2D ↓ 3F	NOT USED[1]		2C ↓ 3E
41		(R)-CH0 Offset Error	40
43		(R)-CH0 Gain Error	42
45		(R)-CH1 Offset Error	44
47		(R)-CH1 Gain Error	46
49		(R)-CH2 Offset Error	48
4B		(R)-CH2 Gain Error	4A
4D		(R)-CH3 Offset Error	4C
4F		(R)-CH3 Gain Error	4E
51		(R)-CH4 Offset Error	50
53		(R)-CH4 Gain Error	52
55		(R)-CH5 Offset Error	54
57		(R)-CH5 Gain Error	56
59		(R)-CH6 Offset Error	58
5B		(R)-CH6 Gain Error	5A
5D		(R)-CH7 Offset Error	5C
5F		(R)-CH7 Gain Error	5E
61		(R)-CH8 Offset Error[2]	60
63		(R)-CH8 Gain Error[2]	62
65		(R)-CH9 Offset Error[2]	64
67		(R)-CH9 Gain Error[2]	66
69		(R)-CH10 Offset Error[2]	68
6B		(R)-CH10 Gain Error[2]	6A
6D		(R)-CH11 Offset Error[2]	6C
6F		(R)-CH11 Gain Error[2]	6E
71		(R)-CH12 Offset Error[2]	70
73		(R)-CH12 Gain Error[2]	72
75		(R)-CH13 Offset Error[2]	74
77		(R)-CH13 Gain Error[2]	76
79		(R)-CH14 Offset Error[2]	78
7B		(R)-CH14 Gain Error[2]	7A
7D		(R)-CH15 Offset Error[2]	7C
7F		(R)-CH15 Gain Error[2]	7E

Notes (Table 3.1):

1. The IOS will respond to addresses that are "Not Used" with an active IOS module acknowledge ACK∗. Data read at “Not Used” addresses will be driven low.
2. Channels 8-15 are present in the IOS-220-16 Model, only.

The following sections give details on the function of each location in the I/O space noted above.

IOS Identification - (Read Only, 32 even-byte addresses)

Each IOS module contains an identification (ID) that resides in the IOS ID space.. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID. Fixed information includes the "IOS" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IOS-220 ID bytes are addressed using only the even addresses in a 64-byte block. The IOS-220 ID contents are shown in Table 3.2. Four signature bytes (220A), at offset 21 to 27 hex, permit software to discriminate between the original IOS-220 and new models IOS-220. Note that the base-address for the IOS module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID. Execution of an ID Read requires 0 wait states.

Table 3.2: IOS-220 ID Space Identification (ID)

Hex Offset From ID PROM Base Address	Numeric Value (Hex)	Field Description
00	49	
02	50	
04	41	
06	43	
08	A3	Acromag ID Code
0A	22 IOS-220-16 23 IOS-220-8	IOS Model Code
0C	00	Not Used (Revision)
0E	00	Reserved
10	00	Not Used
12	00	Not Used
14	0C	Total Number of ID PROM Bytes
16	55 IOS-220-16 34 IOS-220-8	CRC
18 to 1E	00	Not Used
20	32	Used to Identify the New IOS-220
22	32	
24	30	
26	41	
28 to 3E	00	Not Used

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DAC Channel Registers- (Read/Write, Base + 00H to 1EH)

The IOS-220 contains sixteen (16) DAC Channel Registers in the I/O space (see Table 3.1). Writing to the address of the specific register enables the DAC input buffer, to latch the data existing on the data bus.

Twelve bits of DAC data must be written to the DAC register left justified within the 16-bit word (D16). The four LSB's are undefined (typically passive pull-ups on the carrier board will cause undriven bits to be high). The data format is Bipolar Offset Binary (BOB, see Section 2 for details).

MSB											LSB				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
← DATA →												X	X	X	X

"X" means “Don’t Care” - the bit value does not matter.

The contents of the DAC Channel registers are transferred to their corresponding converter input buffer serially. This serial data transfer take 2µs. Thus, a new write of the same DAC register can be performed no sooner then 2µs after the previous write. A DAC Write Status register, at base address plus 26H, is available as a write operation busy status indicator. The channels Status bit will be set low upon initiation of a write operation and will remain low until the requested write operation has completed. New write accesses to the same DAC Channel register, should not be initiated unless its write busy status bit is set high. Read of the DAC Channel register should also wait 2µs after a write, to avoid read of the register as it is being serially shift out.

RESET CONDITION: All output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before a DAC output update by enabling the Transparent Mode, or enabling the Simultaneous Output Trigger. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

Execution of a DAC channel write or read command requires one wait state.

Transparent Mode - (Write, Base + 20H)

The Transparent Mode is a write-only register in the I/O space that is used to select and enable the transparent type of data transfer (it will not respond to reads). Once the Transparent Mode is selected, 12-bit digital data written to the address specific channel’s input latch will automatically be converted and transferred to the board’s field connector. The data is transferred from the input latch, through the DAC latch (transparent in this mode), to the analog output field connector until a reset, Simultaneous Mode, or Simultaneous Output Trigger is enabled. Execution of a Transparent Mode write command requires 1 wait state. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

D15...D00
X...X

"X" means “DON’T CARE” - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

In the Transparent Mode, the Simultaneous Mode can be activated by a write to the Simultaneous Output Trigger register.

Simultaneous Mode - (Write, Base + 22H)

The Simultaneous Mode is a write-only register (will not respond to reads) in the I/O space that is used to select the simultaneous type of data transfer. Once the Simultaneous Mode is selected, 12-bit digital data written to the address specific channel’s input latch will continue to be held until the Simultaneous Output Trigger register is written, before digital data is transferred to the output latch (and the updated analog output appears at the board’s field connector). The data, of all the channels, is simultaneously transferred, **once per simultaneous trigger,** from the DAC input latch to the output latch (and analog output updated) **only** when the Simultaneous Output Trigger register is enabled. Execution of a Simultaneous Mode Write command requires 1 wait state. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

D15...D00
X...X

"X" means “Don’t Care” - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

The Simultaneous Mode can also be activated while in Transparent Mode if a write occurs to the Simultaneous Output Trigger register.

Simultaneous Output Trigger - (Write, Base + 24H)

The Simultaneous Output Trigger is a write-only register (will not respond to reads) in the I/O space that produces the pulse needed to trigger the simultaneous type of data transfer. The Simultaneous Output Trigger register works in conjunction with the Simultaneous Mode register to simultaneously transfer all the channels’ digital data from the DAC input latch to the output latch (and update the analog output) at a specific time. The Simultaneous Mode register must be written to first. Then, writing to the Simultaneous Output Trigger register creates the trigger for digital data to be converted and transferred to the board’s field

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connector. The 12-bit digital data written to the address specific channel's input latch will continue to be held until the Simultaneous Output Trigger register is written.
This will trigger the transfer of digital data from the DAC input latch to the output latch and the digital to analog conversion producing the updated analog output. Execution of a Simultaneous Output Trigger Write command requires 1 wait state. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

D15...D00
X...X

"X" means "Don't Care" - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

The Simultaneous Mode can also be activated while in Transparent Mode if a write occurs to the Simultaneous Output Trigger register.

DAC Write Status Register - (Read, Base + 26H)

This DAC Write Status register can be read to monitor the busy status after a write to a DAC channel. New write of a DAC Channel register can be performed no sooner then 2µs after the previous DAC write command is executed.

The status of 16 DAC channels numbered 0 through 15 may be monitored via this register. Data bits 0 to 15 reflect the status of DAC channels 0 to 15. The channels corresponding status bit will be set low upon initiation of a write operation and will remain low until the requested write operation has completed. New write accesses to the DAC Channel register should not be initiated unless its write busy status bit is set high.

Control Register - (Read/Write, Base + 28H), Word address

This register is used to issue a software reset to the IOS-220. Setting bit-7 of this register to a logic high "1" will reset all analog output channels to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

This register is cleared (set to "0") following a reset. Reading or writing this register is possible via 16-bit or 8-bit data transfers.

EEPROM Write Control Register - (Read/Write, Base + 2AH)

Writes to the coefficient memory device require a special enable code. Writes to memory are normally only performed at the factory. The module should be returned to Acromag if the coefficients must be re-measured and stored to memory.

Write operations to coefficient memory are enable by setting bits 0 and 1 to logic high. Write operations to the coefficient memory at base address plus 40H to 7FH will take approximately 1m seconds.

Bit-15 of the EEPROM Status register serves as write operation busy status indicator. Status bit-15 will be set low upon initiation of a write operation and will remain low until the requested write operation has completed. New write accesses to the coefficient memory, should not be initiated unless the write busy status bit-15 is set high.

EEPROM Status Register - (Read, Base + 2BH)

This register is used to monitor the busy status after a write to the coefficient memory device. The DAC coefficients are measured and written at the factory . Reading bit-15 of this register can be used to detect the end of a coefficient memory write cycle. Bit-15 is actively pulled low "0" during the write cycle and is released to logic high "1" at completion of the write.

Channel Offset/Gain Error Coeff. - (Read, Base + 40 to 7FH)

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in a EEPROM. These coefficients can be retrieved (read-only) by accessing the last 32 low bytes (40H to 7EH) of the I/O space (D08 - or using the lower 8 bits for D16 accesses). The offset and gain calibration coefficients read from the EEPROM are stored with 1/4-LSB resolution. Thus, it is necessary to divide each coefficient by four to correctly use them when calibrating the bipolar outputs. Each is stored as a two's-complement (i.e. signed) eight-bit number. This number has a range of -128 to +127, which represents the offset or gain adjustments from -32 to +31.75 LSB's. Execution of a Channel Offset or Gain Error Read command requires 1 wait state.

HIGH BYTE							LOW BYTE							
							MSB							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							←——— DATA ———→							

PROGRAMMING CONSIDERATIONS FOR ANALOG OUTPUTS

The IOS-220 provides two methods of analog output programming for maximum flexibility with different applications. The following paragraphs describe the features of each and how to best use them.

Using the Transparent Mode

Use of the Transparent Mode provides the quickest method of updating the desired analog output. This method is geared for those applications that require maximum speed without the need for updating all channels simultaneously. In Transparent Mode, each

analog output channel is updated as soon as it is written to. Multiple channels may be written to separately, resulting in the analog outputs being updated one channel at a time. Functionally, the input latch is written to, and the DAC latch is automatically updated, providing more speed by eliminating a separate write instruction.

Transparent Mode Programming Example

1. Write to the Transparent Mode register to setup the transparent type of data transfer.
2. Read the EEPROM to acquire the channel's unique offset and gain calibration coefficient data. This data is necessary to adjust, by software, the accuracy of the involved channel's analog output. See USE OF CALIBRATION DATA.
3. Write the 16-bit (corrected 12-bit, left-justified) digital data to the desired DAC Channel Register.
4. (OPTIONAL) Observe or monitor that the specific DAC channel reflects the results of the digital data converted to an analog output voltage at the field connector.
5. Repeat steps 1-4 until all the desired channels reflect the updated analog output voltage at the field connector.

Using the Simultaneous Mode

Use of the Simultaneous Mode provides a method of distributing data simultaneously and synchronously to produce desired analog outputs. This method is useful for applications that require updating all the channels simultaneously and synchronously. Each channel is written to with the required 16-bit (12-bit, left-justified) data. When all the required channels contain the desired digital data, then a write to the Simultaneous Output Trigger register will produce a pulse to simultaneously trigger each channel's digital to analog converter. Thus, all the analog outputs are updated simultaneously. Functionally, each input latch is written to separately. When all input latches contain the desired digital data, then all channels are pulsed simultaneously and synchronously to convert to the updated analog output voltage.

Simultaneous Mode Programming Example

1. Write to the Simultaneous Mode register to setup the simultaneous type of data transfer.
2. Read the EEPROM to acquire the channel's unique offset and gain calibration coefficient data. This data is necessary to adjust, by software, the accuracy of the involved channel's analog output. See USE OF CALIBRATION DATA.
3. Write the 16-bit (corrected 12-bit, left-justified) digital data to the desired DAC Channel Register.
4. Repeat steps 2-3 to write new digital data to the DAC Channel Registers for all other channels requiring update.
5. Write to the Simultaneous Output Trigger register to produce a pulse to simultaneously trigger digital to analog conversions for all channels, resulting in updated analog output voltages at the field connector.
6. (OPTIONAL) Observe or monitor that DAC channels reflect the results of the digital data converted to an analog output voltage at the field connector.
7. Repeat steps 2-6 for continued simultaneous and synchronous triggered updates of all desired channels.

USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in the EEPROM. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Software calibration uses some fairly complex equations. Acromag provides software products (sold separately) to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). The maximum uncalibrated error is summarized as follows:

AD5570 @ 25^{O}C:

Linearity Error is +/- 0.003% maximum (i.e. 1/8 LSB).
Bipolar Offset Error is +/- 0.038% FSR (i.e. 20V SPAN) maximum.
Gain Error is +/- 0.038% FSR maximum.

Table 3.3 summarizes the maximum uncalibrated error combining the linearity, offset and gain errors:

Table 3.3: Maximum Overall Uncalibrated Error

Max. Linearity Error (%)	Max. Offset Error (%)	Max. Gain Error (%)	Max. Total Error* (%)
+/-0.003	+/-0.038	+/-0.038	+/-3.23 LSB (+/-0.079)

* This represents the worst case error with all errors summed. Typically, each error component is much less than its maximum and all error components do not reinforce each other. Thus, typical errors are much less than that shown in the table above.

Calibrated Performance

Accurate calibration of the IOS-220 can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in the PROM as 1/4 LSB's for each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage.

Table 3.4 summarizes the maximum calibrated error combining the linearity and adjusted offset and gain errors:

Table 3.4: Maximum Overall Calibrated Error

Max. Linearity Error LSB	Max. Offset Error LSB	Max. Gain Error LSB	Max. Total Error LSB (%)
+/-0.5	+/-0.25	+/-0.25	+/-1 LSB (+/-0.024)

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Thus, correcting the value programmed to the DAC Channel Register using the stored calibration coefficients provides the means to obtain excellent accuracy.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (ideal_count) written to the 12-bit DAC to achieve a specified voltage within the -10 to +10 Volt output range assuming Bipolar Offset Binary (BOB) data format (see Section 2 for details).

Ideal_Count = [(Count_Span / Ideal_Volt_Span) * Desired_Voltage] + Ideal_Zero_Count (1)

where,
Count_Span = 4096 (a 12-bit converter has 2^{12} possible levels)
Ideal_Volt_Span = 20 Volts (for the bipolar -10 to +10 Volt range)
Ideal_Zero_Count = 2048 (count for an ideal output of 0 Volts)

Equation (1) can be simplified using the above constants, since the range and DAC are fixed on the IOS-220. Equation (2) results:

Ideal_Count = [(4096 / 20) * Desired_Voltage] + 2048 (2)

Using equation (2), one can determine the ideal count for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts, equation (2) returns the result 3072 for Ideal_Count. If this value is used to program the DAC output (following conversion to Hex and left-justification), the output value will approach +5 Volts to within the uncalibrated error specified in Table 3.3. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal_Count into the Corrected_Count required to accurately produce the output voltage. This is illustrated in equation (3):

Corrected_Count = [(Ideal_Gain + Gain_Correction) * (Ideal_Count - Ideal_Zero_Count)] + (Ideal_Zero_Count + Offset_Correction) (3)

where,
Ideal_Gain = 1
Gain_Correction = PROM_Gain_Error / 4 / 4096 = PROM_Gain_Error / 16384
Offset_Correction = PROM_Offset_Error / (4)

Ideal_Count is determined from equation (2) and Ideal_Zero_Count remains 2048. PROM_Gain_Error and PROM_Offset_Error are obtained from the PROM on the IOS-220 on a per channel basis. Equation (3) can be written as (4) by making the listed substitutions:

Corrected_Count = [(1 + (PROM_Gain_Error / 16384)) * (Ideal_Count - 2048)] + (2048 + (PROM_Offset_Error / 4)) (4)

Using equation (4), you can determine the corrected count from the ideal count. For the previous example, equation (2) returned a result 3072 for the Ideal_Count to produce an output of +5 Volts. Assuming that a gain error of +13 and an offset error of -25 are read from the PROM on the IOS-220 for the desired channel, substitution into equation (4) yields:

Corrected_Count = [(1 + (13 / 16384)) * (3072 - 2048)] + (2048 + (-25 / 4)) = 3066.56

If this value (rounded to 3067) is used to program the DAC output (following conversion to Hex and left-justification), the output value will approach +5 Volts to within the calibrated error specified in Table 3.4 (+/-1 LSB). Note that the quantization error (up to 0.5 LSB) introduced by rounding to 3067 is not included in the overall accuracy specification.

Calibration Programming Example

The available bipolar range, centered around 0 Volts is -10 to +10 Volts. Assume it is necessary to program channel 0 with an output of -2.5 Volts.

1. Write to the Transparent Mode register @BASE + 20H with data of FFFFH to select the Transparent Mode. In this mode, data written to the Channel Register will be automatically transferred from the input latch to the output latch and converted to the desired output.
2. Read the PROM to retrieve the channel's unique offset calibration error data. For channel 0, read byte @BASE + 41H. An 8 bit two's compliment number is read (assume 20H). This corresponds to a PROM_Offset_Error of +32 decimal.
3. Read the PROM to retrieve the channel's unique gain calibration error data. For channel 0, read byte @BASE + 43H. An 8 bit two's compliment number is read (assume F1H). This corresponds to a PROM_Gain_Error of -15 decimal.
4. Calculate the Ideal_Count required to provide an uncorrected output of the desired value (-2.5 Volts) by using equation (2). **Ideal_Count =** [(4096 / 20) * -2.5] + 2048 = 1536.0
5. Calculate the Corrected_Count required to provide an accurate output of the desired value (-2.5 Volts) by using equation (4). **Corrected_Count =** [(1 + (-15 / 16384)) * (1536.0 - 2048)] + (2048 + (32 / 4)) = 1544.47
6. Write to the DAC Channel 0 Register @BASE + 00H with the desired data (6080H - data is determined by rounding 1544.47 decimal to 1544, then converting to Hex 608 and left justifying as 6080H).
7. (OPTIONAL) Observe or monitor that the specific DAC channel (0) reflects the results of the digital data converted to an analog output voltage at the field connector.
8. Repeat steps 2-7 to adjust the unique calibration characteristic and update each channel used, or repeat steps 4-7 to update the value of a single channel.

Error checking should be performed on the calculated count values to insure that calculated values below 0 or above 4095 decimal are restricted to those end points. Note that the software calibration cannot generate outputs near the endpoints of the range which are clipped off due to the uncalibrated hardware (i.e. the DAC).

4.0 THEORY OF OPERATION

This section describes the basic functionality of the IOS-220 circuitry. Review the IOS-220 Block Diagram as you study the following paragraphs.

ANALOG OUTPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). Field analog outputs are NON-ISOLATED. This means that the field return, output channel minus, and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops and excessive output loading (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to ANALOG OUTPUT

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CONNECTIONS for example analog output and grounding connections.

The fully populated board contains sixteen 12-bit DAC's (IOS-220-16), one per channel. This allows each channel to be independently programmed for maximum speed and accuracy and avoids the problems associated with designs using sample and hold amplifiers multiplexed to a single DAC. Each DAC may source up to 5mA of output current without requiring separate buffer amplifiers. DAC calibration is done via software to avoid the mechanical drawbacks of hardware potentiometers for each DAC channel. This also conserves board space and helps to achieve high channel density. Calibration parameters are stored in EEPROM on a per channel basis.

DAC inputs are double-buffered. This allows channels to be programmed by either of two modes (software register selectable). The Transparent Mode allows channels to be updated quickly on an individual basis, since data written to the input latch is immediately transferred to the output latch and converted to an updated analog output voltage. Selection of the Simultaneous Mode allows many or all channels to be updated at once. In this mode, the data for channels is written to their associated input latch, but does not get transferred to the output latch until a Simultaneous Trigger command is sent. All channels update synchronously and simultaneously upon receipt of the trigger command.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of the I/O Server to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Choose the "Support" hyperlink in our website's top navigation row then select "Embedded Board Products Support" or go to http://www.acromag.com/subb_support.cfm to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can be submitted from within the Knowledge Base or through the "Contact Us" hyperlink at the top of any web page.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration.....	Single I/O Server Module.
Length.....	4.030 in. (102.36 mm).
Width.....	1.930 in. (49.02 mm).
Board Thickness.....	0.062 in. (1.59 mm).
Height.....	0.500 in. (12.7 mm).

Power:

+5 Volts (±5%).....	33mA, Typical 45mA Maximum[1].
+12 Volts (±5%) from P1.....	150mA, Typical 200mA, Maximum[1]
-12 Volts (±5%) from P1.....	133mA, Typical 180mA, Maximum[1]

Notes

1. The maximum current draw assumes that the rated current of 5mA per channel is drawn. Current draw will be reduced proportionately for high impedance output loads.

Maximum Vcc Rise Time..... 100m seconds

ENVIRONMENTAL

Operating Temperature.....	-40°C to +85°C
Relative Humidity.....	5-95% Non-Condensing.
Storage Temperature.....	-55°C to +125°C.
Non-Isolated.....	Logic and field commons have a direct electrical connection.
Radiated Field Immunity (RFI).....	Complies with EN61000-4-3 (3 V/m, 80 to 1000MHz AM & 900MHz. Keyed) and European Norm EN50082-1 with no register upsets and analog output error is $< \pm$ 0.5% of a 20V
Conducted R F Immunity (CRFI)	Complies with EN61000-4-6 (3 V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets and analog output error is $< \pm$ 0.5% of a 20V.
Electromagnetic Interference Immunity (EMI).....	No register upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Surge Immunity.....	Not required for signal I/O per European Norm EN50082-1.

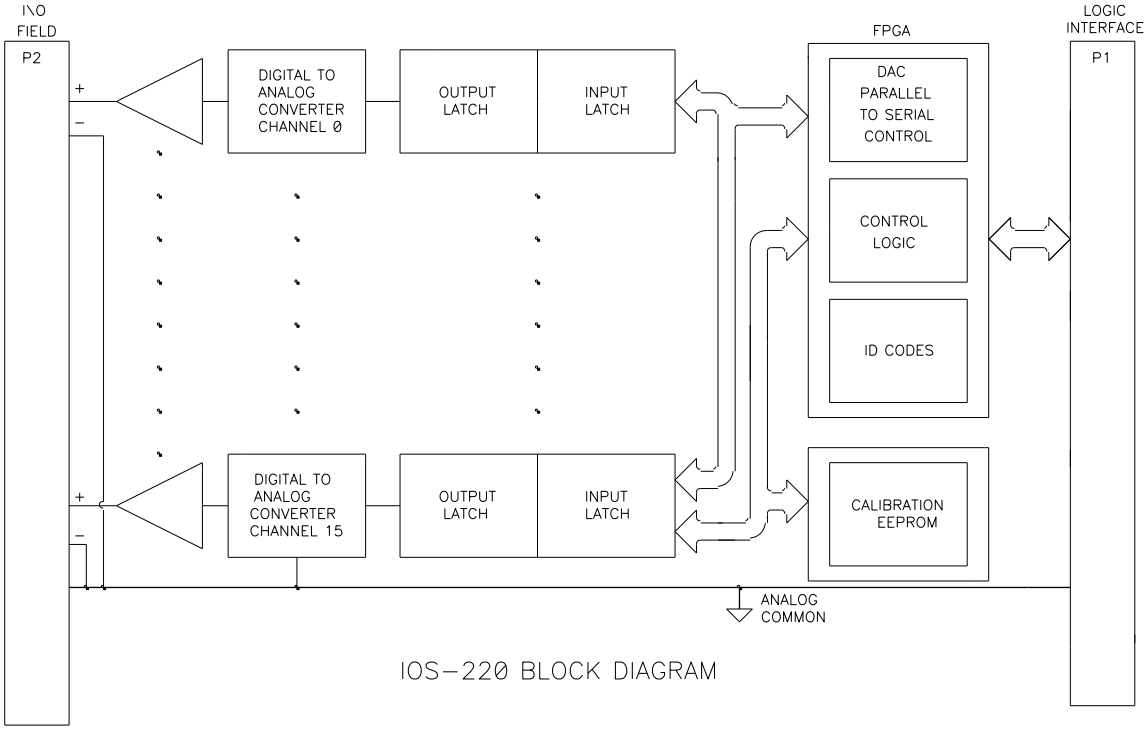
Electric Fast Transient (EFT) Immunity ……..……....	Complies with EN61000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.
Electrostatic Discharge (ESD) Immunity ……..……....	ESD conformance is only available on the IOS-231 model.
Radiated Emissions.....….....	Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

ANALOG OUTPUTS

Output Channels (Field Access).	IOS-220-16: 16 Single-Ended. IOS-220-8: 8 Single-Ended.
Output Type	Voltage (Non-isolated).
Output Range.....	Bipolar -10V to +10V (See Notes 2 & 3).
Output Current.....	-5mA to +5mA (Maximum); this corresponds to a minimum load resistance of 2KΩ with a 10V output (See Notes 2 & 3).
Data Format (left-justified).....	Bipolar Offset Binary (BOB).
DAC Programming.....	Immediate (transparently programmed to DAC output); Simultaneous (input latches of multiple DAC's are loaded with new data before simultaneously updating DAC outputs).
Resolution.....	12-bits.
Monotonicity over Temperature...	12-bits.
Linearity Error.....….....	±1/4 LSB (Maximum).
Differential Linearity Error.....	±1/8 LSB (Maximum).
System Accuracy.....	±0.025% of 20V SPAN Maximum corrected error (i.e. calibrated) at 25°C (See Note 4) with the output unloaded.
Settling Time.....….....	11µS to within 0.012% for a 20V step change (load of 5KΩ in parallel with 470 pf).
Output at Reset.....	Bipolar Zero Volts (See Note 5).
Output Noise.....	2.0mV rms in a 20MHz bandwidth, Typical.
Output Impedance.....	0.5Ω Maximum at 25°C (a load of 10KΩ will introduce 0.005% output error).
Short Circuit Current….....	25mA
Output Load Stability.....	Maximum recommended capacitive load is 500pf. Capacitive loads above 500pf can be tolerated, but with additional overshoot.
Gain Drift.....	±30ppm of 20V SPAN per °C Maximum.
Bipolar Zero Drift……..	±15ppm of 20V SPAN per °C Maximum.

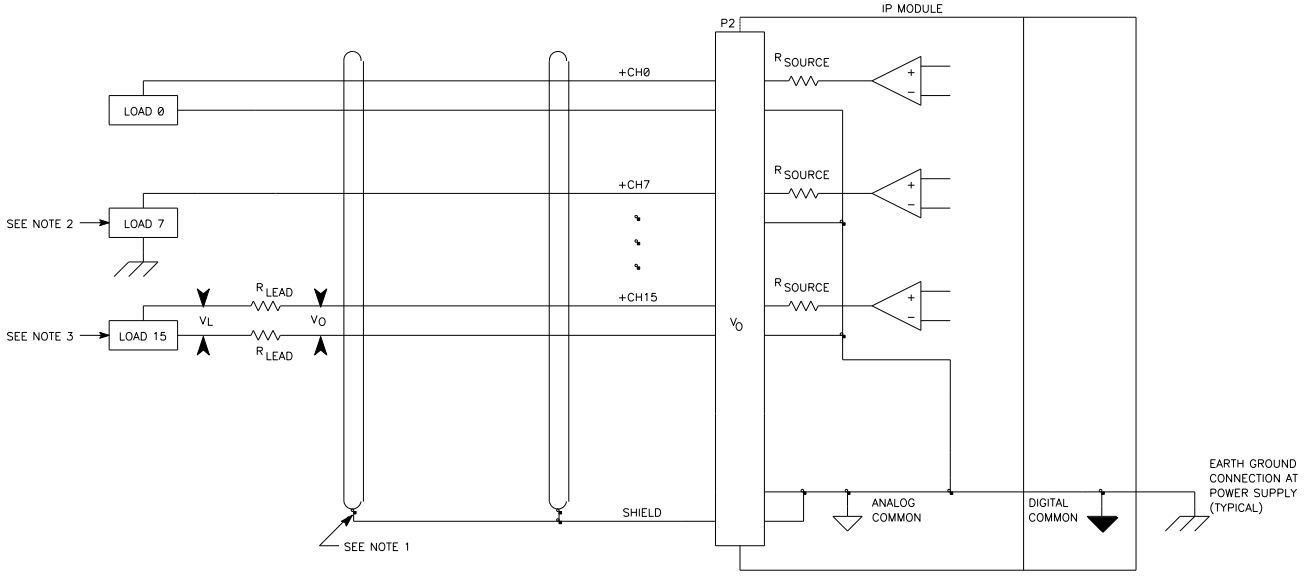
Notes (Analog Outputs):

2. Maximum output current (±5mA) can be achieved at the range endpoints using the internal ±12 volt power supplies sourced through P1. The internal supplies must not drop below ±12 volts to achieve maximum output current of ±5mA. A maximum output current of ±2mA is recommended for supplies at ±11.4 volts.
3. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.
4. Offset and gain calibration coefficients stored in the EEPROM must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error. Follow the output connection recommendations of Section 2, because non-ideal grounds can degrade overall system accuracy.
5. The reset function resets only the DAC (i.e. output) latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before a simultaneous DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch, producing an undesired analog output.



IOS–220 BLOCK DIAGRAM

NOTE: ALL 16 CHANNELS ARE REFERENCED TO ANALOG GROUND. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED LOADS TO THE NEGATIVE SIDE OF THE OUTPUT.



ANALOG OUTPUT CONNECTION DIAGRAM

NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONLY ONE END TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. ALL 16 CHANNELS ARE REFERENCED TO ANALOG COMMON AT THE IP MODULE. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED CHANNELS TO THE NEGATIVE SIDE OF THE OUTPUT.
3. VL < VO DUE TO VOLTAGE DROPS ACROSS THE LEAD RESISTANCE OF THE WIRE. IT IS RECOMMENDED THAT A HIGH RESISTANCE LOAD WITH A SHORT WIRE RUN BE CONNECTED AT THE OUTPUT TO REDUCE THE EFFECTS OF LEAD AND SOURCE RESISTANCE VOLTAGE DROPS IN THE WIRE.

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