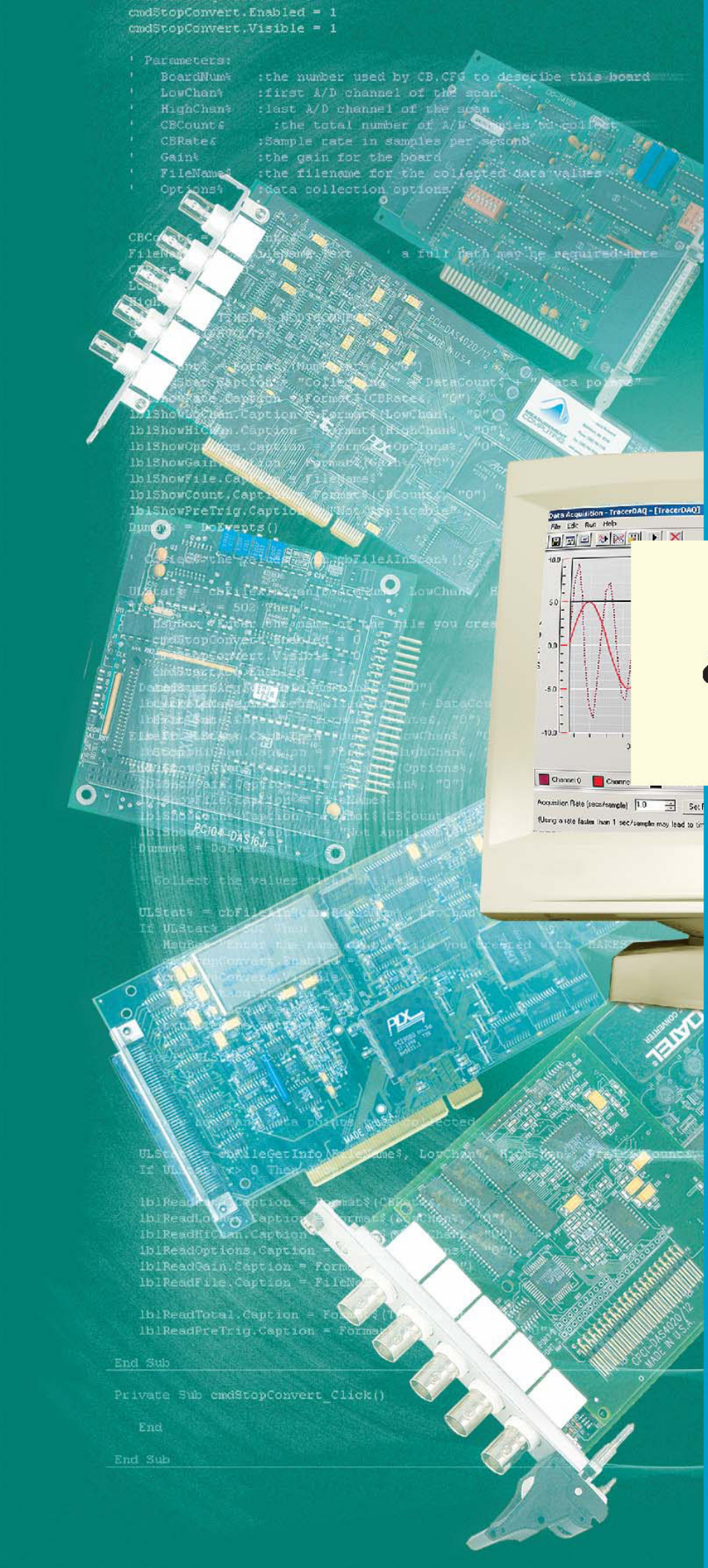


# User's Guide

# PCI-DAS6023 & PCI-DAS6025

Analog and Digital I/O Boards

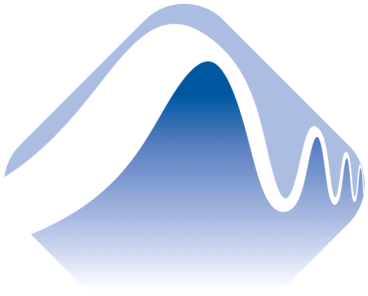
*Identical Specifications.*
*The Only Difference is the Price™*

MEASUREMENT COMPUTING™

# PCI-DAS6023 and PCI-DAS6025

**Analog and Digital I/O Boards**

## User's Guide



MEASUREMENT COMPUTING™

Document Revision 1, May, 2005

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# Table of Contents

# About this User's Guide

## What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS6023 and PCI-DAS6025 boards so that you get the most out of their analog, digital, and timing features.

This user's guide also refers you to related documents available on our web site, and to technical support resources that can also help you get the most out of these boards.

## Conventions in this user's guide

The following conventions are used in this manual to convey special information.

**For more information on …**

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

**Caution!** Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

*<#:#>* Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

**bold** text **Bold text** is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:

**1.** Insert the disk or CD and click the **OK** button.

*italic* text *Italic text* is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:

- The *Insta*Cal installation procedure is explained in the *Software Installation Manual*.
- *Never* touch the exposed pins or circuit connections on the board.

## Where to find more information

The following electronic documents provide helpful information relevant to the operation of the PCI-DAS6023 and PCI-DAS6025 board.

- MCC's *Specifications: PCI-DAS6023 and PCI-DAS6025* (the PDF version of Chapter 6 in this guide) is available on our web site at www.mccdaq.com/pdfs/PCI-DAS6025-23.pdf.
- MCC's *DAQ Software Quick Start* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *STC Register Map for the 6000 Series* is available on our web site at www.mccdaq.com/registermaps/RegMapSTC6000.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

This user's manual is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-DAS6023-25.pdf.

# Introducing the PCI-DAS6023 and PCI-DAS6025

## Overview: PCI-DAS6023 and PCI-DAS6025 features

This manual explains how to install and use the PCI-DAS6023 and PCI-DAS6025 boards. These boards can be used in a wide variety of measurement applications, including data logging, field testing and process control.

The PCI-DAS6025 provides 16 channels of 12-bit analog input, dual 12-bit analog outputs with a 10 kS/s per channel update rate, 32 digital I/O lines and two 16-bit counter timers.

The PCI-DAS6023 provides 16 channels of 12-bit analog input, 8 digital I/O lines and two 16-bit counter timers.

The analog inputs on each board can be configured as either eight differential or 16 single-ended channels. The input ranges are bipolar, in four ranges of ±10 V, ±5 V, ±500 mV, and ±50 mV. The ranges are software-selectable.

Each board provides nine user-configurable trigger/clock/gate pins that are available at a 100-pin I/O connector. Six of the pins are configurable as inputs and three pins are configurable as outputs.

Up to five PCI-DAS6000 series boards can be interconnected for I/O synchronization. Five trigger/strobes and a synchronizing clock are available on a 14-pin header connector. Interrupts can be generated by up to seven ADC sources and four DAC sources.

Both boards are equipped with an 82C54 counter chip that contains three 16-bit counters. Clock, gate, and output signals from two of the counters are available on the board's 100-pin I/O connector. The third counter is used internally.

## Software features

The following software ships with the PCI-DAS6023 and PCI-DAS6025 free of charge.

- *Insta*Cal installation, calibration, and test utility
- TracerDAQ™ suite of virtual instruments
- SoftWIRE® for Visual Studio® .NET graphical programming
- MCC DAQ Components for VS .NET (installed with SoftWIRE® for VS .NET)

For information on the features of *InstaCal*, TracerDAQ, and SoftWIRE, refer to the *DAQ Software Quick Start* booklet that shipped with the PCI-DAS6023 and PCI-DAS6025.

# Installing the PCI-DAS6023 or PCI-DAS6025

This section contains instructions on installing and configuring your PCI-DAS6023 or PCI-DAS6025 board, and includes description of compatible cables and accessory equipment.

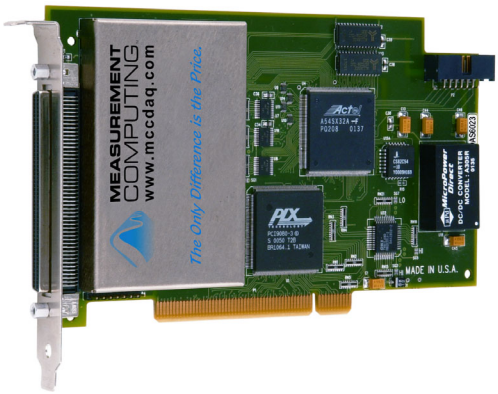
## What comes with your PCI-DAS6023 or PCI-DAS6025 shipment

As you unpack your board shipment, verify that the following components are included.

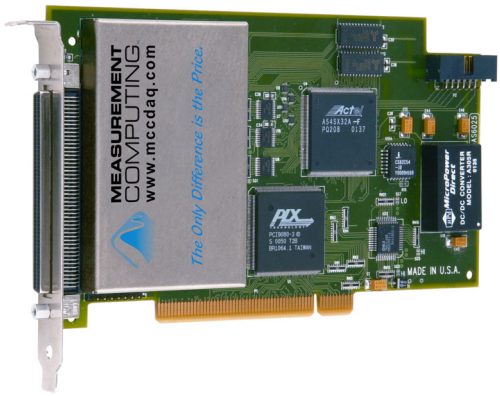
### Hardware

The following items should be included with your shipment:

- PCI-DAS6023 or PCI-DAS6025 board




PCI-DAS6023

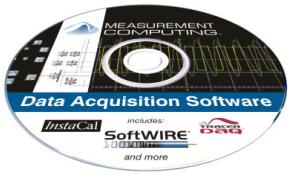



PCI-DAS6025

### Software

The *Measurement Computing Data Acquisition Software* CD contains the following software:

- *Insta*Cal installation, calibration, and test utility
- TracerDAQ suite of virtual instruments
- SoftWIRE for VS .NET
- SoftWIRE MCC DAQ Components for .NET




### Documentation

In addition to this hardware user's guide, you should also receive the *DAQ Software Quick Start* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). Please read this booklet completely before installing any software and hardware.

## Optional components

If you ordered any of the following products with your PCI-DAS6023 or PCI-DAS6025 board, they should be included with your shipment.

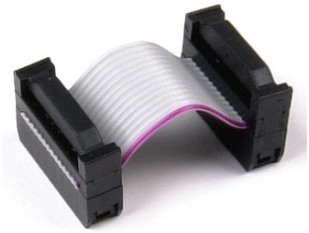
### Universal Library

- Universal Library™ Data Acquisition and Control Programming Tools (also includes the *Insta*Cal utility, the *Universal Library User's Guide*, and the *Universal Library Function Reference*)


### Cables

C100HD50-x

C100MMS-x



CDS-14-*x*

For more information on these MCC cables, refer to the "Connecting the board for I/O operations" section on page 2-9.

### Signal conditioning accessories

MCC provides signal termination products for use with the PCI-DAS6023 and PCI-DAS6025. Refer to the "Field wiring and signal termination accessories" section on page 2-9 for a complete list of compatible accessory products.

# Unpacking the board

Each PCI-DAS6023 and PCI-DAS6025 board is shipped in an antistatic container to prevent damage by an electrostatic discharge. To avoid such damage, perform the following procedure when unpacking and handling your board:

1. Before opening the antistatic container, ground yourself with a wrist-grounding strap or by holding onto a grounded object (such as the computer chassis).
2. Touch the antistatic container to the computer chassis before removing the board from the container.
3. Remove the board from the container. *Never* touch the exposed pins or circuit connections on the board.

If any items are missing or damaged, contact Measurement Computing Corp. by phone, fax, or e-mail. For international customers, contact your local distributor where you purchased the board.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@measurementcomputing.com

## Installing the software

Install the software included with your board *before* you install the hardware. Installing the software first ensures that the information required for proper board detection is installed and available at boot up.

Refer to the *DAQ Software Quick Start* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is shipped with the hardware, and is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

## Installing the hardware

PCI-DAS6023 and PCI-DAS6025 boards are completely plug-and-play. There are no switches or jumpers to set on these boards. Configuration is controlled by your system's BIOS. To install your board, follow the steps below:

**Install the MCC DAQ software before you install your board**

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *DAQ Software Quick Start* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box pops up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the *Measurement Computing Data Acquisition Software* CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *DAQ Software Quick Start* that came with your board for information on how to initially set up and load *Insta*Cal.
4. If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data. This warm-up period is required in order for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

## Configuring the hardware

All of the hardware configuration options on the PCI-DAS6025/6023 are software controlled. You may select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), the edge used for triggering when using an external pacer and the source for the two independent counters. Once selected, any program that uses the Universal Library will use these selections to initialize the hardware according to these selections.

Following is an overview of the available hardware configuration options for the PCI-DAS6023 and PCI-DAS6025 boards. For general information regarding signal connection and configuration, refer to the *Guide to Signal Connections*. This document is available on our web site at www.mccdaq.com/signals/signals.pdf.

## Differential input mode

When all channels are configured for differential input mode, eight analog input channels are available. In this mode, the input signal is measured with respect to the low input. The input signal is delivered through three wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The wire carrying the reference signal connects to CH# IN LO.
- The third wire is connected to LLGND.

Differential input mode is the preferred configuration for applications in noisy environments or when the signal source is referenced to a potential other than PC ground.

## Single-ended input mode

When all channels are configured for single-ended input mode, 16 analog input channels are available. In this mode, the input signal is referenced to the board's signal ground (LLGND). The input signal is delivered through two wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The second wire is connected to LLGND.

## Non-referenced single-ended input mode

This mode is a compromise between differential and single-ended modes. It offers some of the advantages of each mode. Using non-referenced single-ended mode, you can still get noise rejection but not the limitation in the number of channels resulting from a fully differential configuration. The possible downside is that the external reference input must be the same for every channel. It is equivalent to configuring the inputs for differential mode and then tying all of the low inputs together and using that node as the reference input.

When configured for non-referenced single-ended input mode, 16 analog input channels are available. In this mode, each input signal is not referenced to the board's ground, but to a common reference signal (AISENSE).

The input signal is delivered through three wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The wire carrying the reference signal connects to AISENSE.
- The third wire is connected to LLGND.

This mode is useful when the application calls for differential input mode but the limitation on channel count prevents it.

## DAQ-Sync configuration

You can interconnect multiple boards in the PCI-DAS6000 series to synchronize data acquisition or data output. To do this, order and install a CDS-14-*x* cable at the DAQ-Sync connectors (P2) between the boards to be synchronized. Each system can have one master and up to four slaves.

The "*x*" in the CDS-14-*x* part number specifies the number of connectors available on the cable, and therefore, the number of boards you can interconnect. Using a CDS-14-*2*, you can connect two PCI-DAS6000 series boards together for I/O synchronization. Using a CDS-14-*3*, you can synchronize three boards, and so on. You can connect up to five PCI-DAS6000 series boards. A CDS-14-3 cable is shown in Figure 2-3.

By default, all DAQ-Sync connectors are configured as inputs (slave mode). In order to be useful, use software to configure one board as the master and to define the signal sources of the slave boards. Refer to DAQ-Sync signals on page 4-2 for more information.

Detailed information regarding software configuration of these functions is available in the *STC Register Map for the PCI-DAS 6000 Series*. This document is available from our web site at www.mccdaq.com/registermaps/RegMapSTC6000.pdf.

# Connecting the board for I/O operations

## Connectors, cables – main I/O connector

Table 2-1 lists the board connectors, applicable cables, and compatible accessory products for the PCI-DAS6023 and PCI-DAS6025.

Table 2-1. Board connectors, cables, and accessory equipment

| | |
|---|---|
| Connector type | Shielded, SCSI 100-pin D-type |
| Compatible cables | C100HD50-*x* unshielded round cable. x = 3 or 6 feet. (Figure 2-1)<br>C100MMS-*x* shielded round cable. x = 1, 2, or 3 meters. (Figure 2-2) |
| Compatible accessory products with the C100HD50-*x* cable | ▪ ISO-RACK16/P<br>▪ ISO-DA02/P (PCI-DAS6025 only)<br>▪ BNC-16SE<br>▪ BNC-16DI<br>▪ CIO-MINI50<br>▪ CIO-TERM100<br>▪ SCB-50<br>▪ SSR-RACK24 (PCI-DAS6025 only. DADP-5037 adaptor required)<br>▪ CIO-ERB24 (PCI-DAS6025 only. DADP-5037 adaptor required)<br>▪ CIO-ERB08 (PCI-DAS6025 only. DADP-5037 adaptor required) |
| Compatible accessory products with the C100MMS-*x* cable | SCB-100 |

**Information on signal connections**

General information regarding signal connection and configuration is available in the *Guide to Signal Connections*. This document is available on our web site at http://www.measurementcomputing.com/signals/signals.pdf.

## Pin out – main I/O connector

Table 2-2. 8-channel differential mode pin out

| Signal Name | Pin | | Pin | Signal Name |
|---|---|---|---|---|
| LLGND | 1 | | 51 | FIRSTPORTA Bit 0 * |
| CH0 IN HI | 2 | | 52 | FIRSTPORTA Bit 1 * |
| CH0 IN LO | 3 | | 53 | FIRSTPORTA Bit 2 * |
| CH1 IN HI | 4 | | 54 | FIRSTPORTA Bit 3 * |
| CH1 IN LO | 5 | | 55 | FIRSTPORTA Bit 4 * |
| CH2 IN HI | 6 | | 56 | FIRSTPORTA Bit 5 * |
| CH2 IN LO | 7 | | 57 | FIRSTPORTA Bit 6 * |
| CH3 IN HI | 8 | | 58 | FIRSTPORTA Bit 7 * |
| CH3 IN LO | 9 | | 59 | FIRSTPORTB Bit 0 * |
| CH4 IN HI | 10 | | 60 | FIRSTPORTB Bit 1 * |
| CH4 IN LO | 11 | | 61 | FIRSTPORTB Bit 2 * |
| CH5 IN HI | 12 | | 62 | FIRSTPORTB Bit 3 * |
| CH5 IN LO | 13 | | 63 | FIRSTPORTB Bit 4 * |
| CH6 IN HI | 14 | | 64 | FIRSTPORTB Bit 5 * |
| CH6 IN LO | 15 | | 65 | FIRSTPORTB Bit 6 * |
| CH7 IN HI | 16 | | 66 | FIRSTPORTB Bit 7 * |
| CH7 IN LO | 17 | | 67 | FIRSTPORTC Bit 0 * |
| LLGND | 18 | | 68 | FIRSTPORTC Bit 1 * |
| n/c | 19 | | 69 | FIRSTPORTC Bit 2 * |
| n/c | 20 | | 70 | FIRSTPORTC Bit 3 * |
| n/c | 21 | | 71 | FIRSTPORTC Bit 4 * |
| n/c | 22 | | 72 | FIRSTPORTC Bit 5 * |
| n/c | 23 | | 73 | FIRSTPORTC Bit 6 * |
| n/c | 24 | | 74 | FIRSTPORTC Bit 7 * |
| n/c | 25 | | 75 | n/c |
| n/c | 26 | | 76 | n/c |
| n/c | 27 | | 77 | n/c |
| n/c | 28 | | 78 | n/c |
| n/c | 29 | | 79 | n/c |
| n/c | 30 | | 80 | n/c |
| n/c | 31 | | 81 | n/c |
| n/c | 32 | | 82 | n/c |
| n/c | 33 | | 83 | n/c |
| n/c | 34 | | 84 | n/c |
| AISENSE | 35 | | 85 | DIO0 |
| D/A OUT 0* | 36 | | 86 | DIO1 |
| D/A GND* | 37 | | 87 | DIO2 |
| D/A OUT1* | 38 | | 88 | DIO3 |
| PC +5 V | 39 | | 89 | DIO4 |
| AUXOUT0 / D/A PACER | 40 | | 90 | DIO5 |
| AUXOUT1 / A/D PACER | 41 | | 91 | DIO6 |
| AUXOUT2 / SCANCLK | 42 | | 92 | DIO7 |
| AUXIN0 / A/D CONVERT | 43 | | 93 | CTR1 CLK |
| n/c | 44 | | 94 | CTR1 GATE |
| AUXIN1 / A/D START | 45 | | 95 | CTR1 OUT |
| AUXIN2 / A/D STOP | 46 | | 96 | GND |
| AUXIN3 / D/A UPDATE | 47 | | 97 | CTR2 CLK |
| AUXIN4 / D/A START | 48 | | 98 | CTR2 GATE |
| AUXIN5 / A/D PACER | 49 | | 99 | CTR2 OUT |
| GND | 50 | | 100 | GND |
| | PCI slot ↓ | | | |

* Not connected on the PCI-DAS6023

Table 2-3. 16-channel single-ended mode pin out

| Signal Name | Pin | | Pin | Signal Name |
|---|---|---|---|---|
| LLGND | 1 | •• | 51 | FIRSTPORTA Bit 0 * |
| CH0 IN | 2 | •• | 52 | FIRSTPORTA Bit 1 * |
| CH8 IN | 3 | •• | 53 | FIRSTPORTA Bit 2 * |
| CH1 IN | 4 | •• | 54 | FIRSTPORTA Bit 3 * |
| CH9 IN | 5 | •• | 55 | FIRSTPORTA Bit 4 * |
| CH2 IN | 6 | •• | 56 | FIRSTPORTA Bit 5 * |
| CH10 IN | 7 | •• | 57 | FIRSTPORTA Bit 6 * |
| CH3 IN | 8 | •• | 58 | FIRSTPORTA Bit 7 * |
| CH11 IN | 9 | •• | 59 | FIRSTPORTB Bit 0 * |
| CH4 IN | 10 | •• | 60 | FIRSTPORTB Bit 1 * |
| CH12 IN | 11 | •• | 61 | FIRSTPORTB Bit 2 * |
| CH5 IN | 12 | •• | 62 | FIRSTPORTB Bit 3 * |
| CH13 IN | 13 | •• | 63 | FIRSTPORTB Bit 4 * |
| CH6 IN | 14 | •• | 64 | FIRSTPORTB Bit 5 * |
| CH14 IN | 15 | •• | 65 | FIRSTPORTB Bit 6 * |
| CH7 IN | 16 | •• | 66 | FIRSTPORTB Bit 7 * |
| CH15 IN | 17 | •• | 67 | FIRSTPORTC Bit 0 * |
| LLGND | 18 | •• | 68 | FIRSTPORTC Bit 1 * |
| n/c | 19 | •• | 69 | FIRSTPORTC Bit 2 * |
| n/c | 20 | •• | 70 | FIRSTPORTC Bit 3 * |
| n/c | 21 | •• | 71 | FIRSTPORTC Bit 4 * |
| n/c | 22 | •• | 72 | FIRSTPORTC Bit 5 * |
| n/c | 23 | •• | 73 | FIRSTPORTC Bit 6 * |
| n/c | 24 | •• | 74 | FIRSTPORTC Bit 7 * |
| n/c | 25 | •• | 75 | n/c |
| n/c | 26 | •• | 76 | n/c |
| n/c | 27 | •• | 77 | n/c |
| n/c | 28 | •• | 78 | n/c |
| n/c | 29 | •• | 79 | n/c |
| n/c | 30 | •• | 80 | n/c |
| n/c | 31 | •• | 81 | n/c |
| n/c | 32 | •• | 82 | n/c |
| n/c | 33 | •• | 83 | n/c |
| n/c | 34 | •• | 84 | n/c |
| AISENSE | 35 | •• | 85 | DIO0 |
| D/A OUT 0* | 36 | •• | 86 | DIO1 |
| D/A GND* | 37 | •• | 87 | DIO2 |
| D/A OUT1* | 38 | •• | 88 | DIO3 |
| PC +5 V | 39 | •• | 89 | DIO4 |
| AUXOUT0 / D/A PACER OUT | 40 | •• | 90 | DIO5 |
| AUXOUT1 / A/D PACER OUT | 41 | •• | 91 | DIO6 |
| AUXOUT2 / SCANCLK | 42 | •• | 92 | DIO7 |
| AUXIN0 / A/D CONVERT | 43 | •• | 93 | CTR1 CLK |
| n/c | 44 | •• | 94 | CTR1 GATE |
| AUXIN1 / A/D START | 45 | •• | 95 | CTR1 OUT |
| AUXIN2 / A/D STOP | 46 | •• | 96 | GND |
| AUXIN3 / D/A UPDATE | 47 | •• | 97 | CTR2 CLK |
| AUXIN4 / D/A START | 48 | •• | 98 | CTR2 GATE |
| AUXIN5 / A/D PACER GATE | 49 | •• | 99 | CTR2 OUT |
| GND | 50 | •• | 100 | GND |
| | PCI slot ↓ | | | |

* Not connected on the PCI-DAS6023

## Cabling

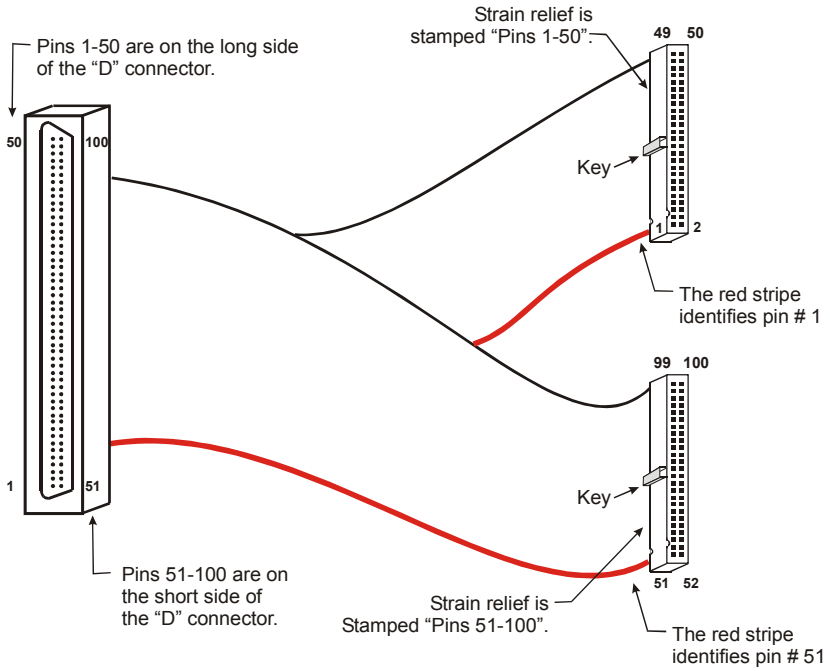



Figure 2-1. C100HD50-*x* Cable Connections

Details on the C100HD50-*x* cable are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=104&pf_id=1203.

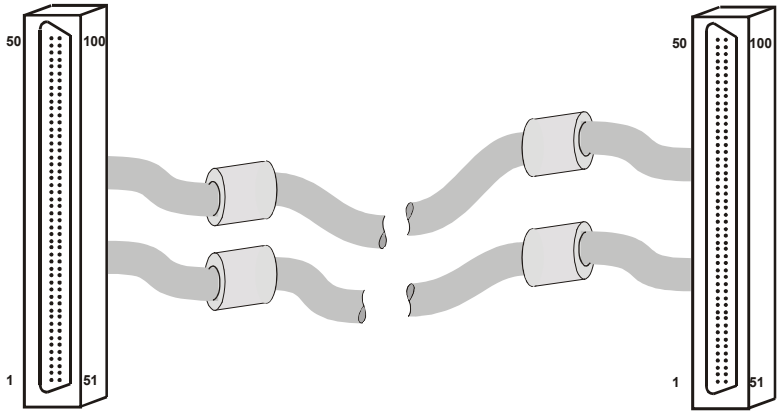



Figure 2-2. C100MMS-*x* Cable

Details on the C100MMS-*x* cable are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=104&pf_id=1514.

## DAQ-Sync connector and pinout

Table 2-4. DAQ-sync connector & cable types

| | |
|---|---|
| Connector type | 14-pin right-angle 100mil box header |
| Compatible cables | MCC p/n: CDS-14-*x*, 14 pin ribbon cable for board-to board DAQ-sync connection; *x* = number of boards (from 2 to 5 boards can be connected). See Figure 2-3. |

Table 2-5. DAQ-sync connector pinout (view from top)

| Signal Name | Pin | Pin | Signal Name |
|---|---|---|---|
| DS A/D START TRIGGER | 1 | 2 | GND |
| DS A/D STOP TRIGGER | 3 | 4 | GND |
| DS A/D CONVERT | 5 | 6 | GND |
| DS D/A UPDATE | 7 | 8 | GND |
| DS D/A START TRIGGER | 9 | 10 | GND |
| RESERVED | 11 | 12 | GND |
| SYNC CLK | 13 | 14 | GND |

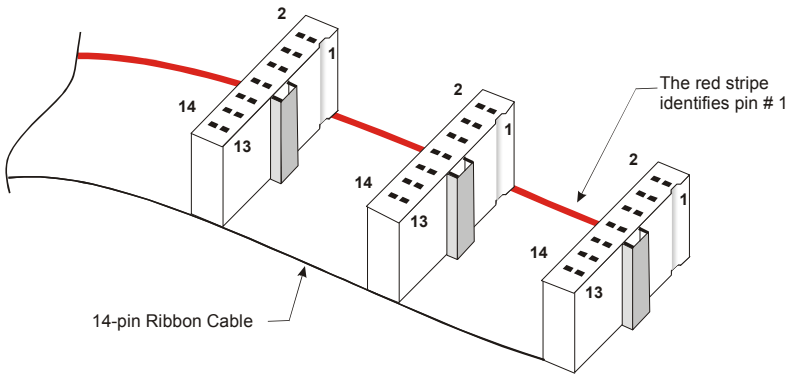



Figure 2-3. CDS-14-3 cable

## Field wiring and signal termination accessories

You can use the following BNC and screw terminal boards to terminate field signals and route them into the PCI-DAS6023 or PCI-DAS6025 using the C100HD50-*x* cable:

- BNC-16SE – Brings analog signals to standard BNC connectors. Designed for boards operating in single-ended mode. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=101&pf_id=713.
- BNC-16DI – Brings analog signals to standard BNC connectors. Designed for boards operating in differential mode. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=101&pf_id=714.
- CIO-MINI50 – 50-pin screw terminal board. Two boards are required. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=258.
- CIO-TERM100 – 100-pin screw terminal board (daisy-chained 50-pin IDC connectors). Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=281.
- SCB-50 – 50 conductor, shielded signal connection/screw terminal box provides two independent 50-pin connections. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1168.

You can use the following screw terminal box to terminate field signals and route them into the PCI-DAS6023 or PCI-DAS6025 board using the C100MMS-x cable:

- SCB-100 – 100 conductor, shielded signal connection/screw terminal box provides two independent 50-pin connections. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1169

### Analog signal conditioning

You can use the following analog signal conditioning products with the PCI-DAS6023 and PCI-DAS6025 using the C100HD50-*x* cable:

- ISO-RACK16/P – 16-channel, 5B module rack. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=127&pf_id=1111.
- ISO-DA02/P (PCI-DAS6025 only) – 2-channel, 5B module rack. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=128&pf_id=703.

### Digital signal conditioning (requires the DADP-5037 adaptor board)

The following digital signal conditioning products have 37-pin connectors. Use the DADP-5037 adaptor board for connections to the C100HD50-*x* cable's 50-pin connectors. Details on this adaptor board are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=103&pf_id=1381.

- SSR-RACK24 – 24-channel solid state I/O module rack. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=122&pf_id=1193.
- CIO-ERB24 – 24 Form C, 6A relays. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=123&pf_id=241.
- CIO-ERB08 – Eight Form C, 6A relays. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=123&pf_id=240.

# Programming and Software Applications

After following the installation instructions in Chapter 2, your board should now be installed and ready for use. Although the board is part of the larger DAS family, in general there may be no correspondence between registers[1]. Software written at the register level for other DAS models will not function correctly with your board.

## Programming Languages

Measurement Computing's Universal Library® provides access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic® or any other language, please refer to the *Universal Library User's Guide* (available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf).

## Packaged applications programs

Many packaged application programs, such as SoftWIRE®, Labtech Notebook™, and HP-VEE™, now have drivers for your board. If the package you own does not have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain drivers.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us by phone, fax or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@measurementcomputing.com

## Register-level programming

You should use the Universal Library or one of the packaged application programs mentioned above to control your board. Only experienced programmers should try register-level programming. If you need to program at the register level in your application, refer to the *STC Register Map for the PCI-DAS6000 Series.* This document is available on our website at www.mccdaq.com/registermaps/RegMapSTC6000.pdf.

[1] An exception to this is the DAQ Sync capability of these boards that permit synchronized data acquisition by multiple boards in this series

# Functional Details

## Basic architecture

Figure 4-1 shows a simplified block diagram of the PCI-DAS6023 and PCI-DAS6025. The PCI-DAS6025 provides all of the functional elements shown in the diagram. The PCI-DAS6023 does not provide D/A outputs, and has eight bits of TTL digital I/O rather than the 32 digital inputs/outputs provided by the PCI-DAS6025. The two boards are identical in all other respects.

The STC (System Timing and Control) is the logical center for all DAQ, DIO, and DAC (if applicable) operations. It communicates over two major busses, a local bus and a memory bus.

The local bus carries digital I/O data and software commands from the PCI Bus Master. Two Direct Memory Access (DMA) channels provide data transfers to the PC.

Primarily, the memory bus carries A/D and D/A (PCI-DAS6025 only) related data and commands. There are three buffer memories provided on the memory bus:

- The Queue Buffer is an 8K configuration memory. It can be used for storing programmed channel numbers, gains, and offsets.
- The ADC Buffer is an 8K FIFO (First In, First Out) for temporary storage of scanned and converted analog inputs.
- The DAC 16K Buffer can be used for storing data to be output as analog waveforms. (This function only applies to the PCI-DAS6025.)

### Auxiliary input and output interface

The board's 100-pin I/O connector provides six software-selectable inputs and three software-selectable outputs. The signals are user-configurable clocks, triggers and gates.

Refer to "DAQ signal timing" on page 4-3 for additional information and timing requirements for the signals.

Table 4-1 defines the possible and default signals that can be used on the nine pins.

**D/A signals**

The D/A signals are applicable to the PCI-DAS6025 only.

Table 4-1. Auxiliary I/O signals

| I/O type | Signal name | Function |
|---|---|---|
| AUXIN<5:0> sources (SW selectable) | A/D CONVERT | External ADC convert strobe (default) |
| | A/D EXT. TIMEBASE IN | External ADC pacer time base |
| | A/D START TRIGGER | ADC Start Trigger (default) |
| | A/D STOP TRIGGER | ADC Stop Trigger (default) |
| | A/D PACER GATE | External ADC gate (default) |
| | D/A START TRIGGER | DAC trigger/gate (default) (PCI-DAS6025 only) |
| | D/A UPDATE | DAC update strobe (default) (PCI-DAS6025 only) |
| | D/A EXT. TIMEBASE IN | External DAC pacer time base (PCI-DAS6025 only) |
| AUXOUT<2:0> sources (SW selectable) | STARTSCAN | A pulse indicating start of conversion |
| | SSH | Active signal that terminates at the start of the last conversion in a scan. |
| | A/D STOP | Indicates end of an acquisition sequence |
| | A/D CONVERT | ADC convert pulse (default) |
| | SCANCLK | Delayed version of ADC convert (default) |
| | CTR1 CLK | CTR1 clock source |
| | D/A UPDATE | D/A update pulse (default) (PCI-DAS6025 only) |
| | CTR2 CLK | CTR2 clock source |
| | A/D START TRIGGER | ADC Start Trigger Out |
| | A/D STOP TRIGGER | ADC Stop Trigger Out |
| | D/A START TRIGGER | DAC Start Trigger Out |
| Default selections summary | AUXIN0 | A/D CONVERT |
| | AUXIN1 | A/D START TRIGGER |
| | AUXIN2 | A/D STOP TRIGGER |
| | AUXIN3 | D/A UPDATE (PCI-DAS6025 only) |
| | AUXIN4 | D/A START TRIGGER (PCI-DAS6025 only) |
| | AUXIN5 | A/D PACER GATE |
| | AUXOUT0 | D/A UPDATE (PCI-DAS6025 only) |
| | AUXOUT1 | A/D CONVERT |
| | AUXOUT2 | SCANCLK |

## DAQ-Sync signals

The DAQ-Sync hardware provides the capability of triggering or clocking up to four slave boards from a master board to synchronize data input and / or output.

The PCI-DAS6023 and PCI-DAS6025 boards provide the capability of inter-board synchronization with other boards in the PCI-DAS6000 family. There are five trigger/strobes and a synchronizing clock provided on a 14-pin header connector. The available signals are:

- DS A/D START TRIGGER
- DS A/D STOP TRIGGER
- DS A/D CONVERT
- DS D/A UPDATE (PCI-DAS6025 only)
- DS D/A START TRIGGER (PCI-DAS6025 only)
- SYNC CLK

Except for the SYNC CLK signal, the DAQ-Sync timing and control signals are a subset of the AUXIO signals available at the 100-pin I/O connector. These versions of the signals are used for board-to-board synchronization and have the same timing specifications as their I/O connector counterparts. Refer to the "DAQ signal timing" section on page 4-3 for explanations of signals and timing.

Use the SYNC CLCK signal to determine the master/slave configuration of a DAQ-Sync-enabled system. Each system can have one master and up to three slaves. SYNC CLK is the 40 MHz time base used to derive all board timing and control. The master provides this clock to the slave boards so that all boards in the DAQ-sync-enabled system are timed from the same clock.

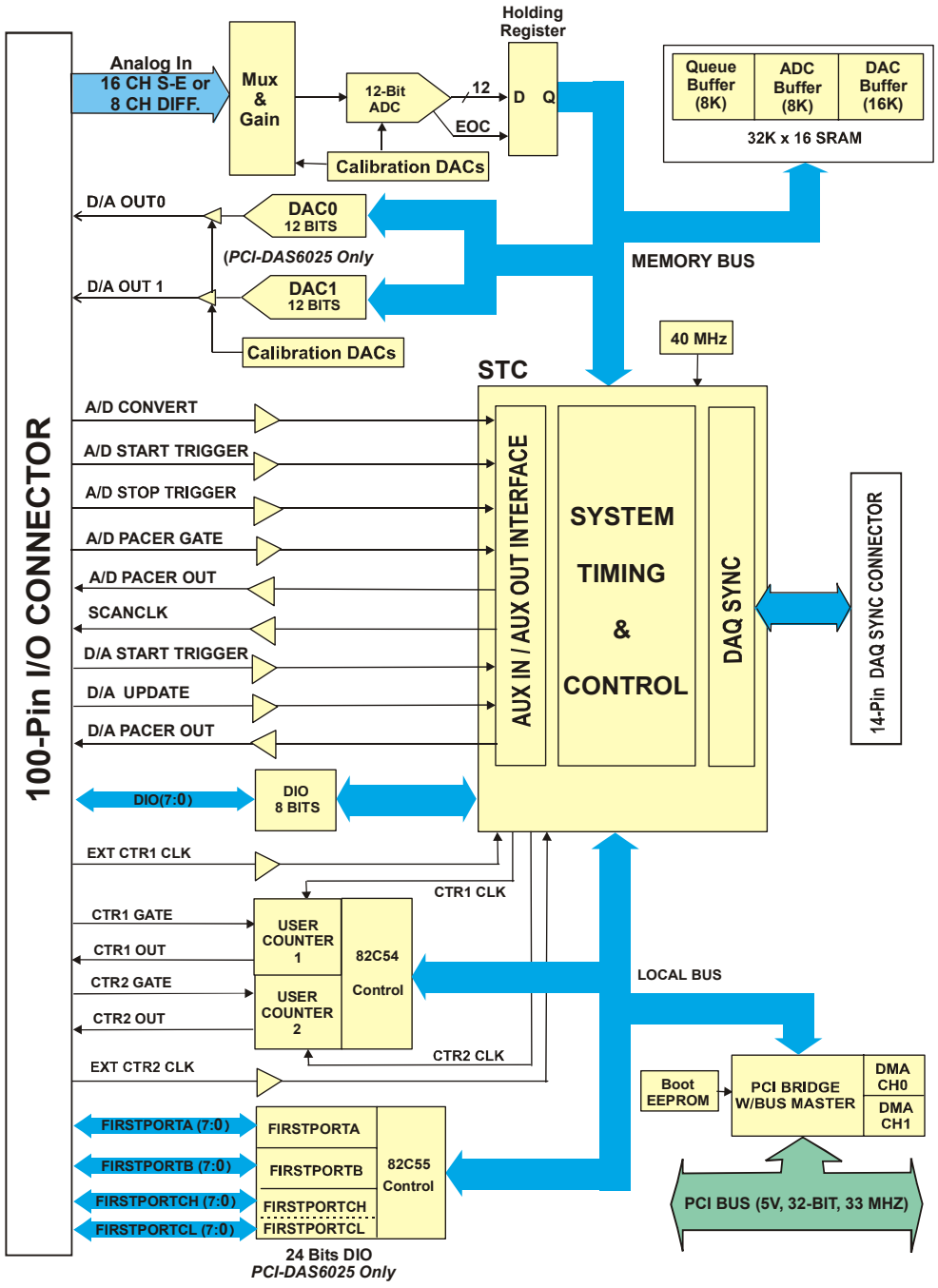



Figure 4-1. Block diagram – PCI-DAS6025 and PCI-DAS6023

## DAQ signal timing

The primary DAQ timing signals are:

- SCANCLK

- SSH
- A/D START TRIGGER
- A/D STOP TRIGGER
- STARTSCAN
- A/D CONVERT
- A/D PACER GATE

## SCANCLK signal

SCANCLK is an output signal that may be used for switching external multiplexers. It is a 400ns wide pulse that follows the CONVERT signal after a 50ns delay. This is adequate time for the analog input signal to be acquired so that the next signal may be switched in. The polarity of the SCANCLK signal is programmable. The default output pin for the SCANCLK signal is AUXOUT2, but any of the AUXOUT pins may be programmed as a SCANCLK output.

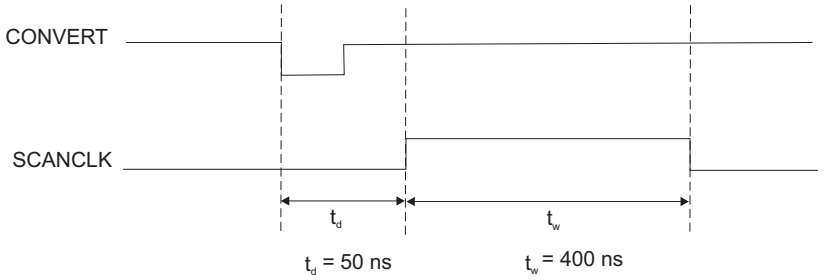



Figure 4-2. SCANCLK Signal Timing

## A/D START TRIGGER signal

The A/D START TRIGGER signal is used for conventional triggering, that is, when you only need to acquire data after a trigger event. Figure 4-3 shows the A/D START TRIGGER signal timing for a conventionally triggered acquisition.

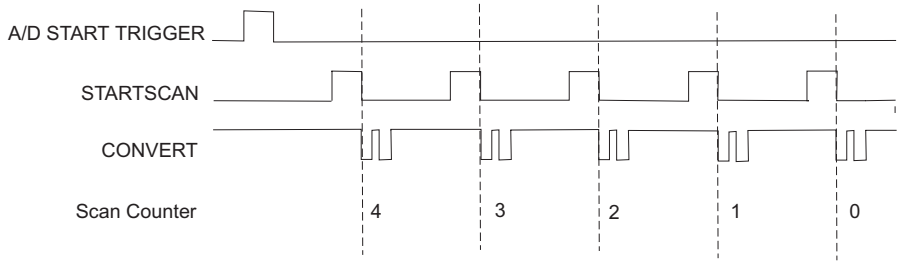



Figure 4-3. Data Acquisition Example for Conventional Triggering

The A/D START TRIGGER source is programmable and may be set to any of the AUXIN inputs or to the DAQ-Sync "DS A/D START TRIGGER" input. The polarity of this signal is also programmable to trigger acquisitions on either the positive or negative edge.

The A/D START TRIGGER signal is also available as an output and can be programmed to appear at any of the AUXOUT outputs.

See Figure 4-4 and Figure 4-5 for A/D START TRIGGER input and output timing requirements.

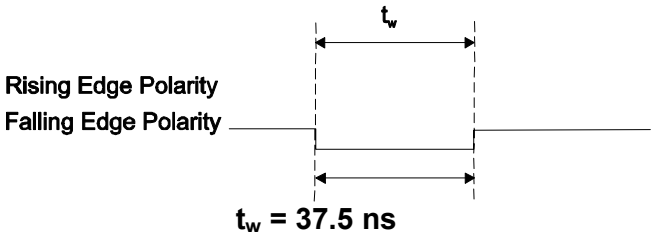



Figure 4-4. A/D START TRIGGER input signal timing

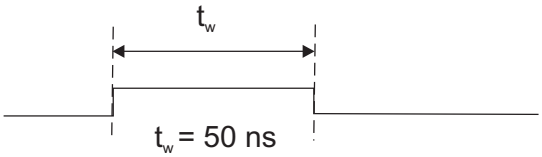



Figure 4-5. A/D START TRIGGER output signal timing

The A/D START TRIGGER signal is also used to initiate pre-triggered DAQ operations, that is, when you need to acquire data just previous to a trigger event. In most pre-triggered applications, the A/D START TRIGGER signal is generated by a software trigger. Descriptions of the use of A/D START TRIGGER and A/D STOP TRIGGER in pre-triggered DAQ applications follow.

## A/D STOP TRIGGER signal

Pre-triggered data acquisition continually acquires data into a circular buffer until a specified number of samples after the trigger event. Figure 4-6 illustrates a typical pre-triggered DAQ sequence.

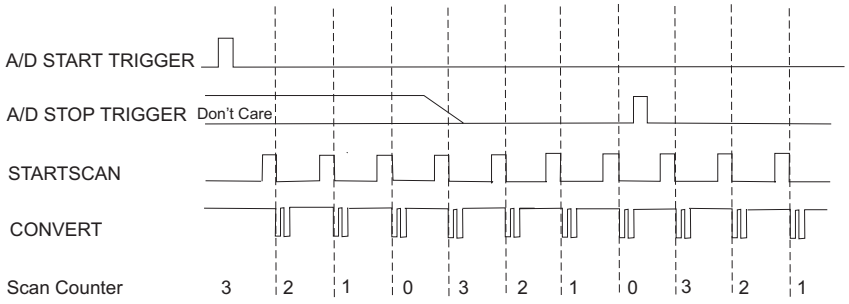



Figure 4-6. Pre-triggered data acquisition example

The A/D STOP TRIGGER signal signifies when the circular buffer should stop and when the specified number of post trigger samples should be acquired. It is available as an output and an input. By default, it is available at AUXIN2 as an input but may be programmed for access at any of the AUXIN pins or at the DAQ-Sync "DS A/D STOP TRIGGER" input. It may be programmed for access at any of the AUXOUT pins as an output.

When using the A/D STOP TRIGGER signal as an input, the polarity may be configured for either rising or falling edge. The selected edge of the A/D STOP TRIGGER signal initiates the post-triggered phase of a pre-triggered acquisition sequence.

As an output, the A/D STOP TRIGGER signal indicates the event separating the pre-trigger data from the post-trigger data. The output is an active high pulse with a pulse width of 50 ns. Figure 4-7 and Figure 4-8 show the input and output timing requirements for the A/D STOP TRIGGER signal.

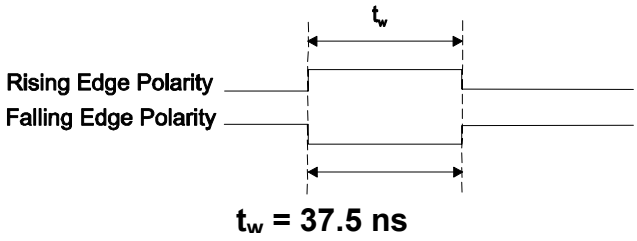



Figure 4-7. A/D STOP TRIGGER input signal timing

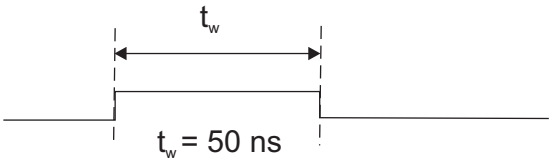



Figure 4-8. A/D STOP TRIGGER output signal timing

## STARTSCAN signal

The STARTSCAN output signal indicates when a scan of channels has been initiated. It may be programmed to be available at any of the AUXOUT pins. The STARTSCAN output signal is a 50ns wide pulse the leading edge of which indicates the start of a channel scan.

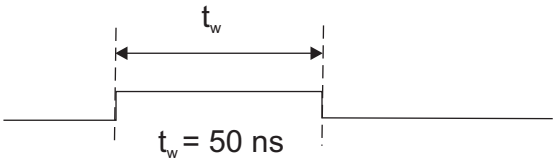



Figure 4-9. STARTSCAN start of scan timing

## SSH signal

The SSH signal can be used as a control signal for external sample/hold circuits. The SSH signal is programmable polarity pulse that is asserted throughout a channel scan. The state of this signal changes after the start of the last conversion in the scan. The SSH signal may be routed via software selection to any of the AUXOUT pins. Figure 4-10 shows the timing for the SSH signal.

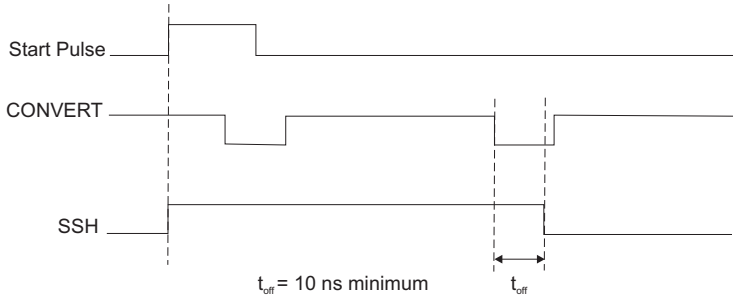



Figure 4-10. SSH signal timing

## A/D CONVERT signal

The A/D CONVERT signal indicates the start of an A/D conversion. It is available through software selection as an input to any of the AUXIN pins (defaulting to AUXIN0) or the DAQ-Sync "DS A/D CONVERT" input and as an output to any of the AUXOUT pins.

When used as an input, the polarity is software selectable. The A/D CONVERT signal starts an acquisition on the selected edge. The convert pulses must be separated by a minimum of 5 μs to remain within the 200 kS/s conversion rate specification.

Refer back to Figure 4-3 and Figure 4-6 for the relationship of A/D CONVERT to the DAQ sequence. Figure 4-11 and Figure 4-12 show the input and output pulse width requirements for the A/D CONVERT signal.

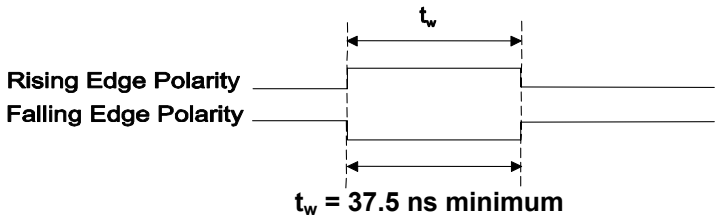



Figure 4-11. A/D CONVERT signal input timing requirement

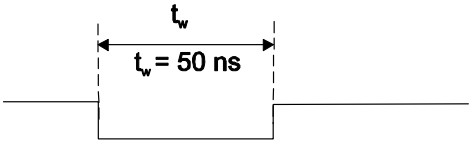



Figure 4-12. A/D CONVERT signal output timing requirement

The A/D CONVERT signal is generated by the on-board pacer circuit unless the external clock option is in use. This signal may be gated by external hardware (A/D PACER GATE) or internally via software.

## A/D PACER GATE signal

The A/D PACER GATE signal is used to disable scans temporarily. This signal may be programmed for input at any of the AUXIN pins.

If the A/D PACER GATE signal is active, no scans can occur. If the A/D PACER GATE signal becomes active during a scan in progress, the current scan is completed and scans are then held off until the gate is de-asserted.

## A/D EXTERNAL TIME BASE signal

The A/D EXTERNAL TIME BASE signal can serve as the source for the on-board pacer circuit rather than using the 40 MHz internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the A/D EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 4-13 shows the timing specifications for the A/D EXTERNAL TIME BASE signal.

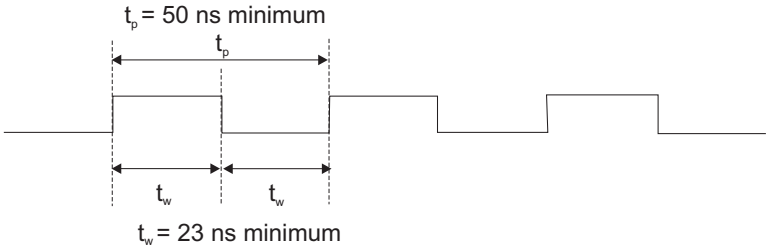



Figure 4-13. A/D EXTERNAL TIME BASE signal timing

### A/D STOP signal

The A/D STOP signal indicates a completed acquisition sequence. You can program this signal to be available at any of the AUXOUT pins. The A/D STOP output signal is a 50 ns wide pulse whose leading edge indicates a DAQ done condition.

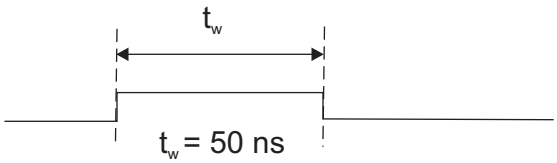



Figure 4-14. A/D STOP signal timing

## Waveform generation timing connections

There are three signals that control the timing for the analog output functions on the PCI-DAS6025. These are D/A START TRIGGER, D/A UPDATE, and D/A EXTERNAL TIME BASE signals.

### D/A START TRIGGER signal

The D/A START TRIGGER signal is used to hold off output scans until after a trigger event. The DAQ-Sync “DS D/A START TRIGGER” input or any AUXIN pin can be programmed to serve as the D/A START TRIGGER signal. It is also available as an output on any AUXOUT pin.

When used as an input, the D/A START TRIGGER signal may be software selected as either a positive or negative edge trigger. The selected edge of the D/A START TRIGGER signal causes the DACs to start generating the output waveform.

The D/A START TRIGGER signal can be used as an output to monitor the trigger that initiates waveform generation. The output is an active-high pulse having a width of 50 ns.

Figure 4-15 and Figure 4-16 show the input and output timing requirements for the D/A START TRIGGER signal.

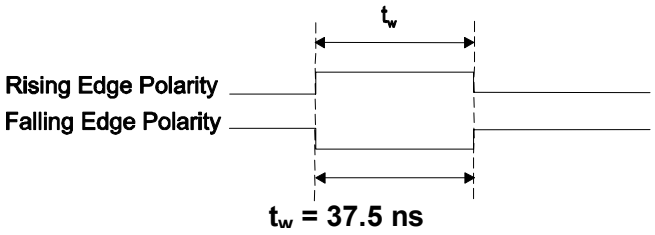



Figure 4-15. D/A START TRIGGER input signal timing

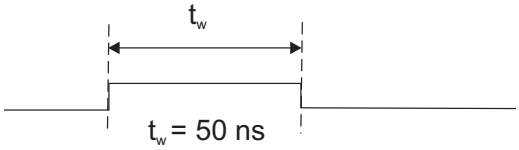



Figure 4-16. D/A START TRIGGER output signal timing

## D/A CONVERT signal

The D/A CONVERT signal causes a single output update on the D/A converters. The DAQ-Sync "DS D/A UPDATE" input or any AUXIN pin can programmed to accept the D/A CONVERT signal. It is also available as an output on any AUXOUT pin.

The D/A CONVERT input signal polarity is software selectable. DAC outputs will update within 100ns of the selected edge. The D/A CONVERT pulses should be no less than 100 μs apart.

When used as an output, the D/A CONVERT signal may be used to monitor the pacing of the output updates. The output has a pulse width of 225 ns with selectable polarity.

Figure 4-17 and Figure 4-18 show the input and output timing requirements for the D/A CONVERT signal.

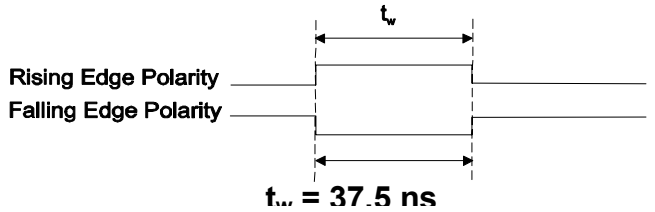



Figure 4-17. D/A CONVERT input signal timing

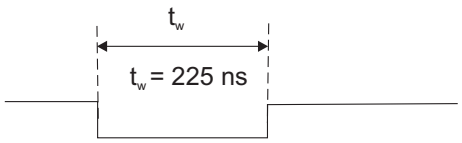



Figure 4-18. D/A CONVERT output signal timing

### D/A EXTERNAL TIME BASE signal

The D/A EXTERNAL TIME BASE signal can serve as the source for the on-board DAC pacer circuit rather than using the internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the D/A EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 4-19 shows the timing requirements for the D/A EXTERNAL TIME BASE signal.

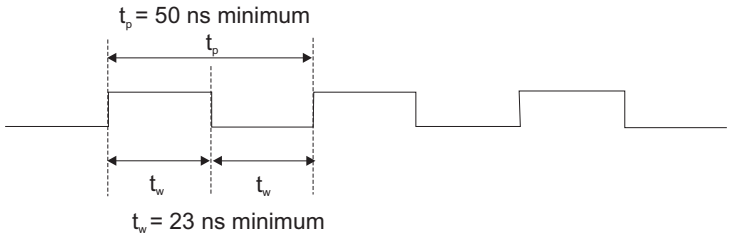



Figure 4-19. D/A EXTERNAL TIME BASE signal timing

## General-purpose counter signal timing

The general-purpose counter signals are:

- CTR1 CLK
- CTR1 GATE
- CTR1 OUT
- CTR2 CLK
- CTR2 GATE
- CTR2 OUT

### CTR1 CLK signal

The CTR1 CLK signal can serve as the clock source for independent user counter 1. It can be selected through software at the CTR1 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified. Figure 4-20 shows the timing requirements for the CTR1 CLK signal.

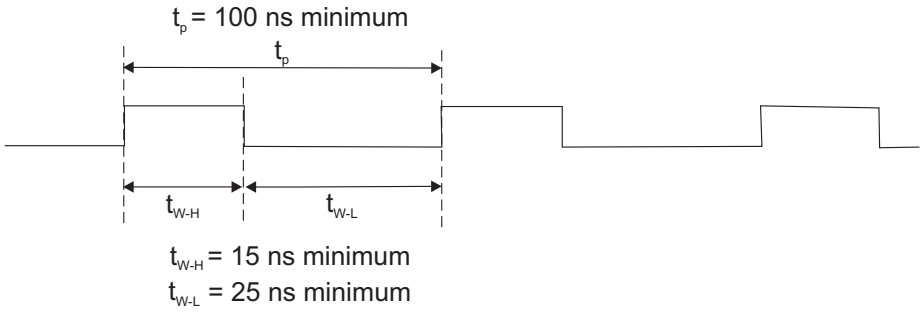



Figure 4-20. CTR1 CLK signal timing

## CTR1 GATE signal

You can use the CTR1 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR1 GATE pin. See Figure 4-21 for the minimum timing specification.

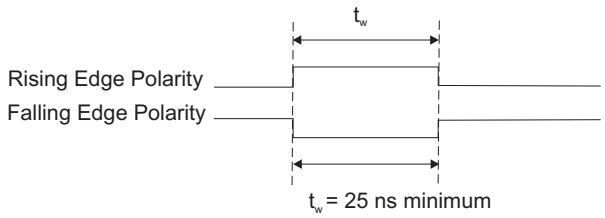



Figure 4-21. CTR1 GATE signal timing

## CTR1 OUT signal

This signal is present on the CTR1 OUT pin. The CTR1 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip. For detailed information on counter operations, refer to the 82C54 data sheet. This data sheet is available on our web site at www.mccdaq.com/PDFmanuals/82C54.pdf

Figure 4-22 shows the timing of the CTR1 OUT signal for counter mode 0 and mode 2.

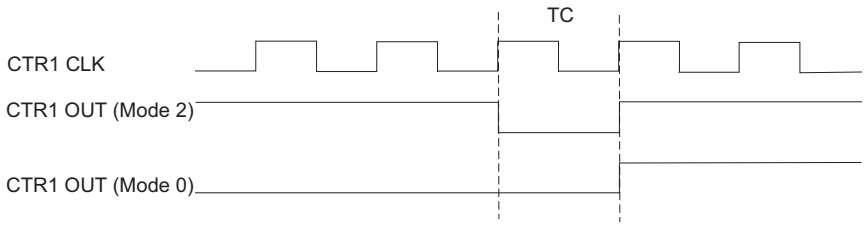



Figure 4-22. CTR1 OUT signal timing

## CTR2 CLK signal

The CTR2 CLK signal can serve as the clock source for independent user counter 2. It can be selected through software at the CTR2 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified. Figure 4-23 shows the timing requirements for the CTR2 CLK signal.

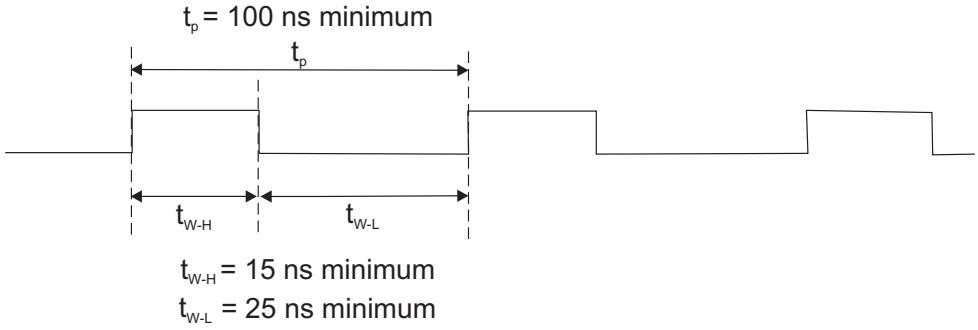



Figure 4-23. CTR2 CLK Signal Timing

## CTR2 GATE signal

You can use the CTR2 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR2 GATE pin. Figure 4-24 shows the timing requirements for the CTR2 GATE signal.

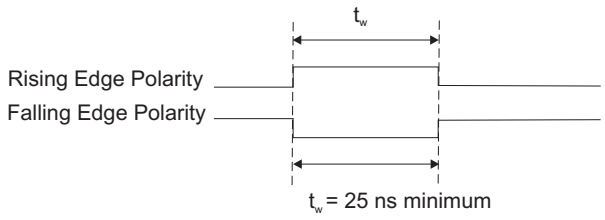



Figure 4-24. CTR2 GATE Signal Timing

## CTR2 OUT signal

This signal is present on the CTR2 OUT pin. The CTR2 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip. For detailed information on counter operations, refer to the 82C54 data sheet. This data sheet is available at www.mccdaq.com/PDFmanuals/82C54.pdf.

Figure 4-25 shows the timing of the CTR1 OUT signal for mode 0 and for mode 2.

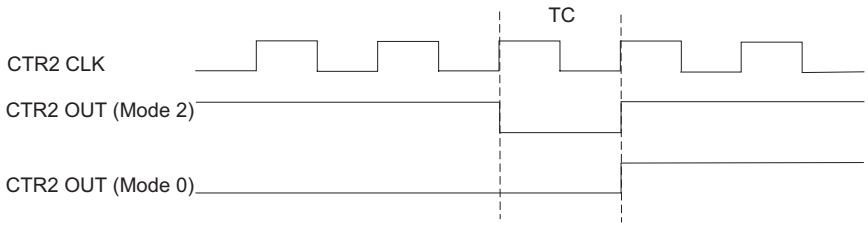



Figure 4-25. CTR2 OUT signal timing

# Calibrating the Board

## Introduction

We recommend that you calibrate the board using the *Insta*Cal utility after the board has fully warmed up. The recommended warm-up time is 15 minutes. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. Pre-measurement calibration insures that your board is operating at optimum calibration values.

## Calibration theory

Analog inputs are calibrated for offset and gain. Offset calibration for the analog inputs is performed directly on the input amplifier, with coarse and fine trim DACs acting on the amplifier.

For input gain calibration, a precision calibration reference is used in conjunction with coarse and fine trim DACs acting on the ADC. See Figure 5-1.

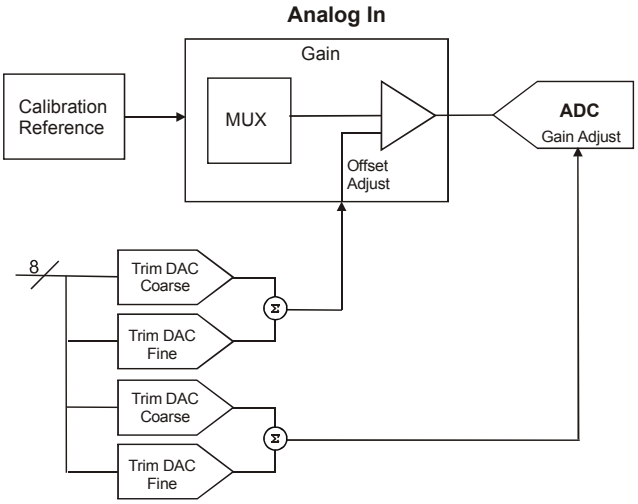



Figure 5-1. Analog input calibration

A similar method is used to calibrate the analog output components (PCI-DAS6025 only). A trim DAC is used to adjust the gain of the DAC. A separate DAC is used to adjust offset on the final output amplifier. The calibration circuits are duplicated for both analog outputs. See Figure 5-2.

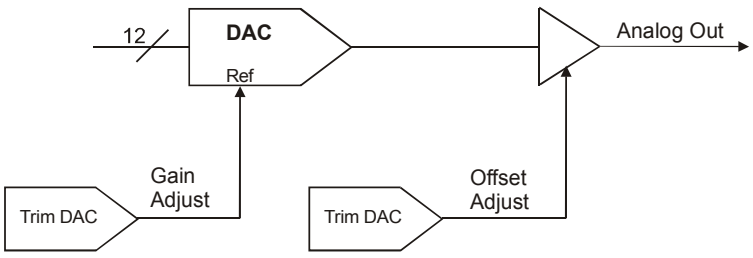



Figure 5-2. Analog output calibration

# Specifications

**Typical for 25 °C unless otherwise specified.**
**Specifications in *italic text* are guaranteed by design.**

## Analog input section

Table 6-1. Analog input specifications

| | |
|---|---|
| A/D converter type | Successive approximation type, min 200 kS/s conversion rate. |
| Resolution | 12 bits, 1-in-4096 |
| Number of channels | 16 single ended / 8 differential. Software selectable |
| Input ranges | ±10 V, ±5 V, ±500 mV, ±50 mV. Software selectable |
| A/D pacing (SW programmable) | Internal counter – ASIC. Software selectable time base:<br>▪ Internal 40 MHz, 50 ppm stability<br>External source via AUXIN<5:0>. Software selectable. |
| | External convert strobe: A/D CONVERT |
| | Software paced |
| Burst mode | Software selectable option, burst rate = 5 µS. |
| A/D gate sources | External digital: A/D GATE |
| A/D gating modes | External digital: Programmable, active high or active low, level or edge |
| A/D trigger sources | External digital: A/D START TRIGGER<br>A/D STOP TRIGGER |
| A/D triggering modes | External digital: Software-configurable for rising or falling edge. |
| | Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. |
| ADC pacer out | Available at user connector: A/D PACER OUT |
| RAM buffer size | 8 k samples |
| Data transfer | DMA |
| | Programmed I/O |
| DMA modes | Demand or Non-Demand using scatter gather. |
| Configuration memory | Up to 8 k elements. Programmable channel, gain, and offset |
| Streaming-to-disk rate | 200 kS/s, system dependent |

### Accuracy

200 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1 °C of internal calibration temperature, and ±10 °C of factory calibration temperature. Calculations for *Absolute Accuracy* are based on the average of 100 measurements performed at the max input voltage for a given range, measured after one year. Calibrator test source high side tied to Channel 0 High, and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 6-2. Absolute accuracy specifications

| Range | Absolute Accuracy |
|---|---|
| ±10 V | ±2.0 LSB |
| ±5 V | ±2.0 LSB |
| ±500 mV | ±3.0 LSB |
| ±50 mV | ±4.0 LSB |

Table 6-3. Absolute accuracy components - all values are (±)

| Range | % of Reading | Offset (mV) | Averaged Noise + Quantization (mV)[1] | Temp Drift (%/°C) | Absolute Accuracy at FS (mV) |
|---|---|---|---|---|---|
| ±10 V | 0.0558 | 2.930 | 1.262 | 0.0010 | 9.77 |
| ±5 V | 0.0563 | 1.460 | 0.605 | 0.0010 | 4.88 |
| ±500 mV | 0.1046 | 0.150 | 0.057 | 0.0010 | 0.73 |
| ±50 mV | 0.1340 | 0.024 | 0.007 | 0.0010 | 0.098 |

1. Averaged measurements assume dithering and averaging of 100 single-channel readings.

Table 6-4. Differential non-linearity specifications

| | | |
|---|---|---|
| All ranges | ±0.5 LSB typ | ±1.0 LSB max |

## System throughput

Table 6-5. System throughput specifications

| Condition | Calibration Coefficients | ADC Rate (max) |
|---|---|---|
| **2.** Single channel, single input range. | Per specified range | 200 kS/s |
| **3.** Multiple channel, single input range | Per specified range | 200 kS/s |
| **4.** Single channel, multiple input ranges. | Default to value for `cbAInScan()` range | 200 kS/s |

**Note:** For conditions 1-2 above, specified accuracy is maintained at rated throughput. Condition 3 applies a calibration coefficient which corresponds to the range value selected in `cbAInScan()`. This coefficient remains unchanged throughout the scan. Increased settling times may occur during gain-switching operations.

## Settling time

Settling time is defined here as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at a specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6-6. Settling time specifications

| Condition | Range | Accuracy | | |
|---|---|---|---|---|
| | | ±0.012% (±0.5 LSB) | ±0.024% (±1.0 LSB) | ±0.098% (±4.0 LSB) |
| Same range to same range | ±10 V | 5 µS typ | 5 µS max | 5 µS max |
| | ±5 V | 5 µS typ | 5 µS max | 5 µS max |
| | ±500 mV | 5 µS typ | 5 µS max | 5 µS max |
| | ±50 mV | 5 µS typ | 5 µS max | 5 µS max |
| Any range to any range | - | 25 µS typ | 20 µS typ | 15 µS typ |

## Parametrics

Table 6-7. Parametrics specifications

| | |
|---|---|
| Maximum working voltage (signal + common-mode) | Input must remain within ±11 V of ground |
| CMRR @ 60 Hz | ±10 V: 85 dB |
| | ±5 V: 85 dB |
| | ±500 mV:90 dB |
| | ±50 mV: 90 dB |
| *Small signal bandwidth, all ranges* | *500 kHz* |
| *Large signal bandwidth, all ranges* | *225 kHz* |
| *Input coupling* | *DC* |
| *Input impedance* | *100 GOhm in normal operation.* |
| | *Min 10 MOhm in powered off or overload condition.* |
| *Input bias current* | *±200 pA* |
| *Input offset current* | *±100 pA* |
| *Absolute maximum input voltage* | *–40 V to +55 V, power on or off. Protected inputs:*<br>▪ *CH<15:0> IN*<br>▪ *AISENSE* |
| Crosstalk | Adjacent channels: -60 dB |
| | All other channels: -80 dB |

## Noise performance

Table 6-8 summarizes the noise performance for the PCI-DAS6025, PCI-DAS6023. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 6-8. Analog input noise performance (not including quantization)

| Range | Typical Counts Dithered | LSBrms Dithered | Typical Counts Undithered | LSBrms Undithered |
|---|---|---|---|---|
| ±10 V | 4 | 0.6 | 2 | 0.1 |
| ±5 V | 4 | 0.6 | 2 | 0.1 |
| ±500 mV | 4 | 0.6 | 3 | 0.1 |
| ±50 mV | 7 | 0.8 | 4 | 0.7 |

# Analog output section (PCI-DAS6025 only)

Table 6-9. Analog output specifications (PCI-DAS6025)

| | |
|---|---|
| D/A converter type | Double-buffered, multiplying |
| Resolution | 12-bits, 1-in-4096 |
| Number of channels | 2 voltage output |
| Voltage range | ±10 V |
| *Monotonicity* | *12-bits, guaranteed monotonic* |
| *DNL* | *±1.0 LSB max* |
| Slew rate | 10V/µs min |
| Settling time | 20V step to 0.012% (0.5 LSB): 10 µs max |
| Noise | 200 µVrms, DC to 1 MHz BW |
| *Glitch energy* | *±24 mV @ 2 µs duration measured at mid-scale transition.* |
| Current drive | ±5 mA |
| *Output short-circuit duration* | *Indefinite @25 mA* |
| *Output coupling* | *DC* |
| Output impedance | 0.1 ohms max |
| Power up and reset | DACs cleared to 0 volts ±200 mV max |

Table 6-10. Absolute accuracy specifications

| **Range** | **Absolute Accuracy** |
|---|---|
| ±10 V | ±1.7 LSB |

Table 6-11. Absolute accuracy components

| **Range** | **% of Reading** | **Offset (mV)** | **Temp Drift (%/DegC)** | **Absolute Accuracy at FS (mV)** |
|---|---|---|---|---|
| ±10 V | ±0.0219 | ±5.93 | ±0.0005 | ±8.127 |

Each PCI-DAS6025 is tested at the factory to assure the board's overall error does not exceed ±1.7 LSB.

Table 6-12. Relative accuracy specifications

| **Range** | **Relative Accuracy** | |
|---|---|---|
| ±10 V | ±0.3 LSB, typical | ±0.5 LSB, max |

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

## Analog output pacing and triggering

Table 6-13. Analog output pacing and triggering specifications

| | |
|---|---|
| DAC pacing<br>(SW programmable) | Internal counter – ASIC. Selectable time base:<br>▪ Internal 40 MHz, 50 ppm stability.<br>▪ External Source via AUXIN<5:0>, SW selectable. |
| | External convert strobe: D/A UPDATE |
| | Software paced |
| DAC gate source<br>(SW programmable) | External digital: D/A START TRIGGER |
| | Software gated |
| DAC gating modes | External digital: Programmable, active high or active low, level or edge |
| DAC trigger sources | External digital: D/A START TRIGGER |
| | Software triggered |
| DAC triggering modes | External digital: Software-configurable for rising or falling edge. |
| DAC pacer out | Available at user connector: D/A PACER OUT |
| RAM buffer size | 16 K samples |
| Data transfer | DMA |
| | Programmed I/O |
| | Update DACs individually or simultaneously, software selectable. |
| DMA modes | Demand or non-demand using scatter gather. |
| Waveform generation throughput | 10 kS/s max per channel, 2 channels simultaneous |

## Analog input/output calibration

Table 6-14. Analog I/O calibration specifications

| | |
|---|---|
| Recommended warm-up time | 15 minutes |
| Calibration | Auto-calibration, calibration factors for each range stored on board in non-volatile RAM. |
| *Onboard calibration reference* | *DC Level: 10.000 V ± 5 mV. Actual measured values stored in EEPROM.* |
| | Tempco: 5 ppm/°C max, 2 ppm/°C typical |
| | Long-term stability: 15 ppm, T = 1000 hrs, non-cumulative |
| Calibration interval | 1 year |

# Digital input/output

## Discrete

Table 6-15. Discrete DIO specifications

| | |
|---|---|
| Digital type | Discrete, 5V/TTL compatible |
| Number of I/O | 8 |
| Configuration | 8 bits, independently programmable for input or output. All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground (factory configured option). |
| Input high voltage | 2.0 V min, 7.0 V absolute max |
| Input low voltage | 0.8 V max, –0.5 V absolute min |
| Output high voltage (IOH = -32 mA) | 3.80 V min, 4.20 V typ |
| Output low voltage (IOL = 32 mA) | 0.55 V max, 0.22 V typ |
| Data transfer | Programmed I/O |
| Power-up / reset state | Input mode (high impedance) |

### 82C55 (PCI-DAS6025 only)

Table 6-16. 82C55 specifications (PCI-DAS6025)

| | |
|---|---|
| Digital type | 82C55 |
| Number of I/O | 24 (FIRSTPORTA 0 through FIRSTPORTC 7) |
| Configuration | 2 banks of 8 and 2 banks of 4 or |
| | 3 banks of 8 or |
| | *2 banks of 8 with handshake* |
| Pull up/pull-down configuration | All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground (factory configured option). |
| *Input high voltage* | *2.0 V min, 5.5 V absolute max* |
| *Input low voltage* | *0.8 V max, –0.5 V absolute min* |
| *Output high voltage (IOH = -2.5 mA)* | *3.0 V min* |
| *Output low voltage (IOL = 2.5 mA)* | *0.4 V max* |
| Power-up / reset state | Input mode (high impedance) |

## Interrupt section

Table 6-17. Interrupt specifications

| | | |
|---|---|---|
| Interrupts | PCI INTA# - mapped to IRQn via PCI BIOS at boot-time | |
| Interrupt enable | Programmable through PLX9080 | |
| ADC Interrupt sources (SW programmable) | DAQ_ACTIVE: | Interrupt is generated when a DAQ sequence is active. |
| | DAQ_STOP: | Interrupt is generated when A/D Stop Trigger In is detected. |
| | DAQ_DONE: | Interrupt is generated when a DAQ sequence completes. |
| | DAQ_FIFO_1/4_FULL: | Interrupt is generated when ADC FIFO is ¼ full. |
| | DAQ_SINGLE: | Interrupt is generated after each conversion completes. |
| | DAQ_EOSCAN: | Interrupt is generated after the last channel is converted in multi-channel scans. |
| | DAQ_EOSEQ: | Interrupt is generated after each interval delay during multi-channel scans. |
| DAC Interrupt sources (SW programmable) | DAC_ACTIVE: | Interrupt is generated when DAC waveform circuitry is active. |
| | DAC_DONE: | Interrupt is generated when a DAC sequence completes. |
| | DAC_FIFO_1/4_EMPTY: | Interrupt is generated DAC FIFO is ¼ empty. |
| | DAC_HIGH_CHANNEL: | Interrupt is generated when the DAC high channel output is updated. |

## Counter section

Table 6-18. Counter specifications

| | |
|---|---|
| User counter type | 82C54 |
| Number of channels | 2 |
| Resolution | 16-bits |
| Compatibility | 5 V/TTL |
| CTRn base clock source (software selectable) | Internal 10 MHz, Internal 100 KHz or external connector (CTRn CLK) |
| Internal 10 MHz clock source stability | 50 ppm |
| Counter n gate | Available at connector (CTRn GATE). |
| Counter n output | Available at connector (CTRn OUT). |
| *Clock input frequency* | *10 MHz max* |
| *High pulse width (clock input)* | *15 ns min* |
| *Low pulse width (clock input)* | *25 ns min* |
| *Gate width high* | *25 ns min* |
| *Gate width low* | *25 ns min* |
| *Input low voltage* | *0.8 V max* |
| *Input high voltage* | *2.0 V min* |
| *Output low voltage* | *0.4 V max* |
| *Output high voltage* | *3.0 V min* |

## Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6025/6023 provides nine user-configurable Trigger/Clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

Table 6-19. Configurable AUXIN, AUXOUT, and external trigger/clocks

| | | |
|---|---|---|
| AUXIN<5:0> Sources (SW selectable) | A/D CONVERT: | External ADC convert strobe |
| | A/D TIMEBASE IN: | External ADC pacer time base |
| | A/D START TRIGGER: | ADC Start Trigger |
| | A/D STOP TRIGGER: | ADC Stop Trigger |
| | A/D PACER GATE: | External ADC gate |
| | D/A START TRIGGER | DAC trigger/gate |
| | D/A UPDATE: | DAC update strobe |
| | D/A TIMEBASE IN: | External DAC pacer time base |
| AUXOUT<2:0> Sources (SW selectable) | STARTSCAN: | A pulse indicating start of conversion |
| | SSH: | Active signal that terminates at the start of the last conversion in a scan. |
| | A/D STOP: | Indicates end of scan |
| | A/D CONVERT: | ADC convert pulse |
| | SCANCLK: | Delayed version of ADC convert |
| | CTR1 CLK: | CTR1 clock source |
| | D/A UPDATE: | D/A update pulse |
| | CTR2 CLK: | CTR2 clock source |
| | A/D START TRIGGER: | ADC Start Trigger Out |
| | A/D STOP TRIGGER: | ADC Stop Trigger Out |
| | D/A START TRIGGER: | DAC Start Trigger Out |
| Default selections: | AUXIN0: | A/D CONVERT |
| | AUXIN1: | A/D START TRIGGER |
| | AUXIN2: | A/D STOP TRIGGER |
| | AUXIN3: | D/A UPDATE |
| | AUXIN4: | D/A START TRIGGER |
| | AUXIN5: | A/D PACER GATE |
| | AUXOUT0: | D/A UPDATE |
| | AUXOUT1: | A/D CONVERT |
| | AUXOUT2: | SCANCLK |
| Compatibility | 5V/TTL | |
| Edge-sensitive polarity | Rising/falling, software selectable | |
| Level-sensitive polarity | Active high/active low, software selectable | |
| Minimum input pulse width | 37.5 ns | |

### DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 6-20. DAQ-Sync inter-board triggers/clock specifications

| | |
|---|---|
| DAQ-Sync signals: | DS A/D START TRIGGER |
| | DS A/D STOP TRIGGER |
| | DS A/D CONVERT |
| | DS D/A UPDATE |
| | DS D/A START TRIGGER |
| | SYNC CLK |

## Power consumption

Table 6-21. Power consumption specifications

| | |
|---|---|
| +5 V | PCI-DAS6025, PCI-DAS6023: 0.9 A typical, 1.1 A max. Does not include power consumed through the I/O connector. |
| +5 V available at I/O connector | 1 A max, protected with a resettable fuse |

## Environmental

Table 6-22. Environmental specifications

| | |
|---|---|
| Operating temperature range | 0 to 55 °C |
| Storage temperature range | -20 to 70 °C |
| Humidity | 0 to 90% non-condensing |

## Mechanical

Table 6-23. Mechanical specifications

| | |
|---|---|
| Card dimensions | PCI half card: 174.6 mm (L) x 106.9 mm (W) x 11.65 mm (H) |

## DAQ-Sync connector and pin out

Table 6-24. DAQ-Sync connector specifications

| | |
|---|---|
| Connector type | 14-pin right-angle 100 mil box header |
| Compatible cables | MCC p/n: CDS-14-x, 14-pin ribbon cable.<br>x = number of boards |

Table 6-25. DAQ-Sync connector pin out

| Pin | Signal Name |
|---|---|
| 1 | DS A/D START TRIGGER |
| 2 | GND |
| 3 | DS A/D STOP TRIGGER |
| 4 | GND |
| 5 | DS A/D CONVERT |
| 6 | GND |
| 7 | DS D/A UPDATE |
| 8 | GND |
| 9 | DS D/A START TRIGGER |
| 10 | GND |
| 11 | RESERVED |
| 12 | GND |
| 13 | SYNC CLK |
| 14 | GND |

# Main connector and pin out

Table 6-26. Main connector specifications

| | |
|---|---|
| Connector type | Shielded SCSI 100 D-Type |
| Compatible cables | C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet |
| | C100MMS-x, shielded round cable. x = 1, 2 or 3 meters |
| Compatible accessory products (with C100HD50-x cable) | ISO-RACK16/P<br>ISO-DA02/P (PCI-DAS6025 only)<br>BNC-16SE<br>BNC-16DI<br>CIO-MINI50<br>CIO-TERM100<br>SCB-50<br>SSR-RACK24 (PCI-DAS6025 only, with DADP-5037)<br>CIO-ERB24 (PCI-DAS6025 only, with DADP-5037)<br>CIO-ERB08 (PCI-DAS6025 only, with DADP-5037) |
| Compatible accessory products (with C100MMS-x cable) | SCB-100 |

Table 6-27. 8-channel differential mode pin out

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | LLGND | 51 | FIRSTPORTA Bit 0 * |
| 2 | CH0 IN HI | 52 | FIRSTPORTA Bit 1 * |
| 3 | CH0 IN LO | 53 | FIRSTPORTA Bit 2 * |
| 4 | CH1 IN HI | 54 | FIRSTPORTA Bit 3 * |
| 5 | CH1 IN LO | 55 | FIRSTPORTA Bit 4 * |
| 6 | CH2 IN HI | 56 | FIRSTPORTA Bit 5 * |
| 7 | CH2 IN LO | 57 | FIRSTPORTA Bit 6 * |
| 8 | CH3 IN HI | 58 | FIRSTPORTA Bit 7 * |
| 9 | CH3 IN LO | 59 | FIRSTPORTB Bit 0 * |
| 10 | CH4 IN HI | 60 | FIRSTPORTB Bit 1 * |
| 11 | CH4 IN LO | 61 | FIRSTPORTB Bit 2 * |
| 12 | CH5 IN HI | 62 | FIRSTPORTB Bit 3 * |
| 13 | CH5 IN LO | 63 | FIRSTPORTB Bit 4 * |
| 14 | CH6 IN HI | 64 | FIRSTPORTB Bit 5 * |
| 15 | CH6 IN LO | 65 | FIRSTPORTB Bit 6 * |
| 16 | CH7 IN HI | 66 | FIRSTPORTB Bit 7 * |
| 17 | CH7 IN LO | 67 | FIRSTPORTC Bit 0 * |
| 18 | LLGND | 68 | FIRSTPORTC Bit 1 * |
| 19 | n/c | 69 | FIRSTPORTC Bit 2 * |
| 20 | n/c | 70 | FIRSTPORTC Bit 3 * |
| 21 | n/c | 71 | FIRSTPORTC Bit 4 * |
| 22 | n/c | 72 | FIRSTPORTC Bit 5 * |
| 23 | n/c | 73 | FIRSTPORTC Bit 6 * |
| 24 | n/c | 74 | FIRSTPORTC Bit 7 * |
| 25 | n/c | 75 | n/c |
| 26 | n/c | 76 | n/c |
| 27 | n/c | 77 | n/c |
| 28 | n/c | 78 | n/c |
| 29 | n/c | 79 | n/c |
| 30 | n/c | 80 | n/c |
| 31 | n/c | 81 | n/c |
| 32 | n/c | 82 | n/c |
| 33 | n/c | 83 | n/c |
| 34 | n/c | 84 | n/c |
| 35 | AISENSE | 85 | DIO0 |
| 36 | D/A OUT 0* | 86 | DIO1 |
| 37 | D/A GND* | 87 | DIO2 |
| 38 | D/A OUT1* | 88 | DIO3 |
| 39 | PC +5 V | 89 | DIO4 |
| 40 | AUXOUT0 / D/A PACER OUT | 90 | DIO5 |
| 41 | AUXOUT1 / A/D PACER OUT | 91 | DIO6 |
| 42 | AUXOUT2 / SCANCLK | 92 | DIO7 |
| 43 | AUXIN0 / A/D CONVERT | 93 | CTR1 CLK |
| 44 | n/c | 94 | CTR1 GATE |
| 45 | AUXIN1 / A/D START TRIGGER | 95 | CTR1 OUT |
| 46 | AUXIN2 / A/D STOP TRIGGER | 96 | GND |
| 47 | AUXIN3 / D/A UPDATE | 97 | CTR2 CLK |
| 48 | AUXIN4 / D/A START TRIGGER | 98 | CTR2 GATE |
| 49 | AUXIN5 / A/D PACER GATE | 99 | CTR2 OUT |
| 50 | GND | 100 | GND |

* = N/C on PCI-DAS6023

Table 6-28. 16-channel single-ended mode pin out

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | LLGND | 51 | FIRSTPORTA Bit 0 * |
| 2 | CH0 IN | 52 | FIRSTPORTA Bit 1 * |
| 3 | CH8 IN | 53 | FIRSTPORTA Bit 2 * |
| 4 | CH1 IN | 54 | FIRSTPORTA Bit 3 * |
| 5 | CH9 IN | 55 | FIRSTPORTA Bit 4 * |
| 6 | CH2 IN | 56 | FIRSTPORTA Bit 5 * |
| 7 | CH10 IN | 57 | FIRSTPORTA Bit 6 * |
| 8 | CH3 IN | 58 | FIRSTPORTA Bit 7 * |
| 9 | CH11 IN | 59 | FIRSTPORTB Bit 0 * |
| 10 | CH4 IN | 60 | FIRSTPORTB Bit 1 * |
| 11 | CH12 IN | 61 | FIRSTPORTB Bit 2 * |
| 12 | CH5 IN | 62 | FIRSTPORTB Bit 3 * |
| 13 | CH13 IN | 63 | FIRSTPORTB Bit 4 * |
| 14 | CH6 IN | 64 | FIRSTPORTB Bit 5 * |
| 15 | CH14 IN | 65 | FIRSTPORTB Bit 6 * |
| 16 | CH7 IN | 66 | FIRSTPORTB Bit 7 * |
| 17 | CH15 IN | 67 | FIRSTPORTC Bit 0 * |
| 18 | LLGND | 68 | FIRSTPORTC Bit 1 * |
| 19 | n/c | 69 | FIRSTPORTC Bit 2 * |
| 20 | n/c | 70 | FIRSTPORTC Bit 3 * |
| 21 | n/c | 71 | FIRSTPORTC Bit 4 * |
| 22 | n/c | 72 | FIRSTPORTC Bit 5 * |
| 23 | n/c | 73 | FIRSTPORTC Bit 6 * |
| 24 | n/c | 74 | FIRSTPORTC Bit 7 * |
| 25 | n/c | 75 | n/c |
| 26 | n/c | 76 | n/c |
| 27 | n/c | 77 | n/c |
| 28 | n/c | 78 | n/c |
| 29 | n/c | 79 | n/c |
| 30 | n/c | 80 | n/c |
| 31 | n/c | 81 | n/c |
| 32 | n/c | 82 | n/c |
| 33 | n/c | 83 | n/c |
| 34 | n/c | 84 | n/c |
| 35 | AISENSE | 85 | DIO0 |
| 36 | D/A OUT 0* | 86 | DIO1 |
| 37 | D/A GND* | 87 | DIO2 |
| 38 | D/A OUT1* | 88 | DIO3 |
| 39 | PC +5 V | 89 | DIO4 |
| 40 | AUXOUT0 / D/A PACER OUT | 90 | DIO5 |
| 41 | AUXOUT1 / A/D PACER OUT | 91 | DIO6 |
| 42 | AUXOUT2 / SCANCLK | 92 | DIO7 |
| 43 | AUXIN0 / A/D CONVERT | 93 | CTR1 CLK |
| 44 | n/c | 94 | CTR1 GATE |
| 45 | AUXIN1 / A/D START TRIGGER | 95 | CTR1 OUT |
| 46 | AUXIN2 / A/D STOP TRIGGER | 96 | GND |
| 47 | AUXIN3 / D/A UPDATE | 97 | CTR2 CLK |
| 48 | AUXIN4 / D/A START TRIGGER | 98 | CTR2 GATE |
| 49 | AUXIN5 / A/D PACER GATE | 99 | CTR2 OUT |
| 50 | GND | 100 | GND |

* = N/C on PCI-DAS6023

# CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 16 Commerce Boulevard
Middleboro, MA 02346
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6023

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

**EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN 61326 (1997) Amendment 1 (1998)**

Emissions: Group 1, Class A

- EN 55011 (1998)/CISPR 11: Radiated and Conducted emissions.

Immunity: EN61326, Annex A

- EN 61000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- EN 61000-4-3 (1997): Radiated Electromagnetic Field immunity Criteria B.
- EN 61000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- EN 61000-4-5 (1995): Surge immunity Criteria A.
- EN 61000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- EN 61000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

Tests to EN61000-4-8 were not required. The PCI boards do not contain components that would be susceptible to magnetic fields.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in June, 2004. Test records are outlined in Chomerics Test Report #EMI3889.04.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Vice-President of Design Verification

# CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 16 Commerce Boulevard
Middleboro, MA 02346
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6025

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

**EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN 61326 (1997) Amendment 1 (1998)**

Emissions: Group 1, Class A

- EN 55011 (1998)/CISPR 11: Radiated and Conducted emissions.

Immunity: EN61326, Annex A

- EN 61000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- EN 61000-4-3 (1997): Radiated Electromagnetic Field immunity Criteria B.
- EN 61000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- EN 61000-4-5 (1995): Surge immunity Criteria A.
- EN 61000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- EN 61000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

Tests to EN61000-4-8 were not required. The PCI boards do not contain components that would be susceptible to magnetic fields.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in June, 2004. Test records are outlined in Chomerics Test Report #EMI3889.04.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Vice-President of Design Verification

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