To our customers,

Old Company Name in Catalogs and Other Documents

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RENESAS

User's Manual

Renesas Starter Kit for SH7124

User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
SuperH™RISC engine

Renesas Electronics
www.renesas.com

Rev.2.00 2006.11

Table of Contents

Chapter 1. Preface

Cautions

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Website: http://www.renesas.com/

Glossary

BRR	Baud Rate Register
ERR	Error Rate
HMON	Embedded Monitor
RTE	Renesas Technology Europe Ltd.
RSK	Renesas Starter Kit
RSO	Renesas Solutions Corp.

Chapter 2.Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The CPU board contains all the circuitry required for microcontroller operation.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Chapter 3.Power Supply

3.1.Requirements

This CPU board operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All CPU boards are supplied with an E8 debugger. This product is able to power the CPU board with up to 300mA. When the CPU board is connected to another system that system should supply power to the CPU board.

All CPU boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The CPU board is neither under not over voltage protected. Use a centre positive supply for this board.

3.2.Power – Up Behaviour

When the RSK is purchased the CPU board has the 'Release' or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. Switch 2 will cause the LEDs to flash at a rate controlled by the potentiometer.

Chapter 4.Board Layout

4.1.Component Layout

The following diagram shows top layer component layout of the board.

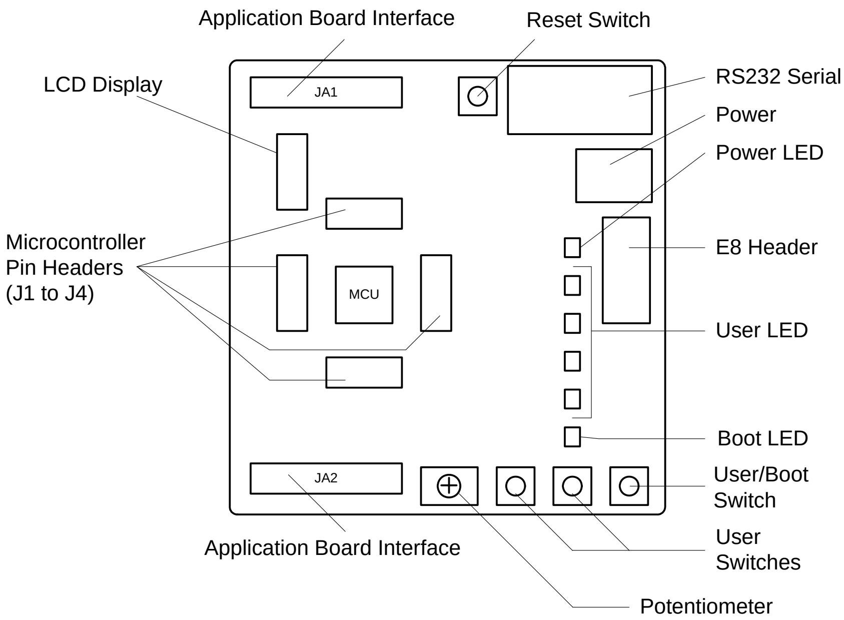

Figure 4-1: Board Layout

4.2.Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

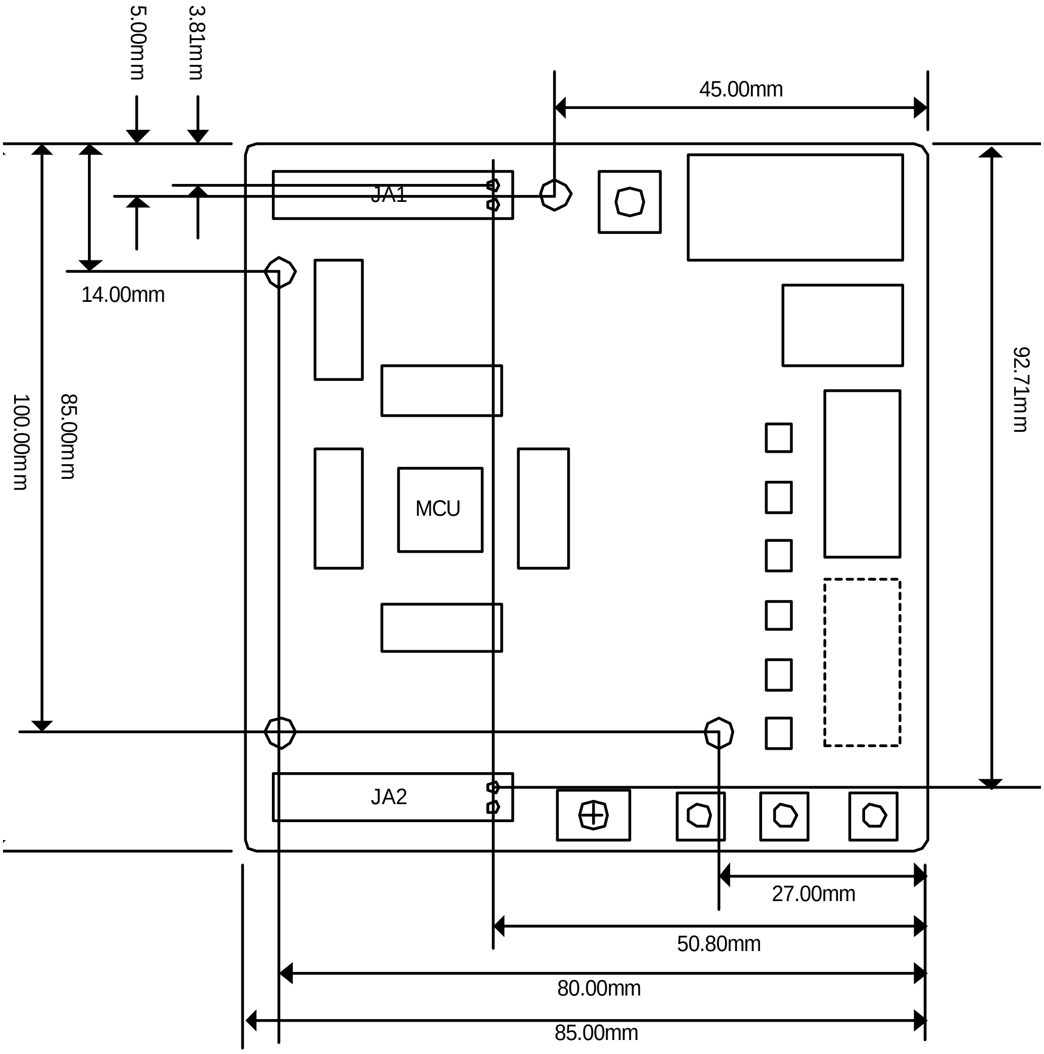

Figure 4-2 : Board Dimensions

Chapter 5.Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

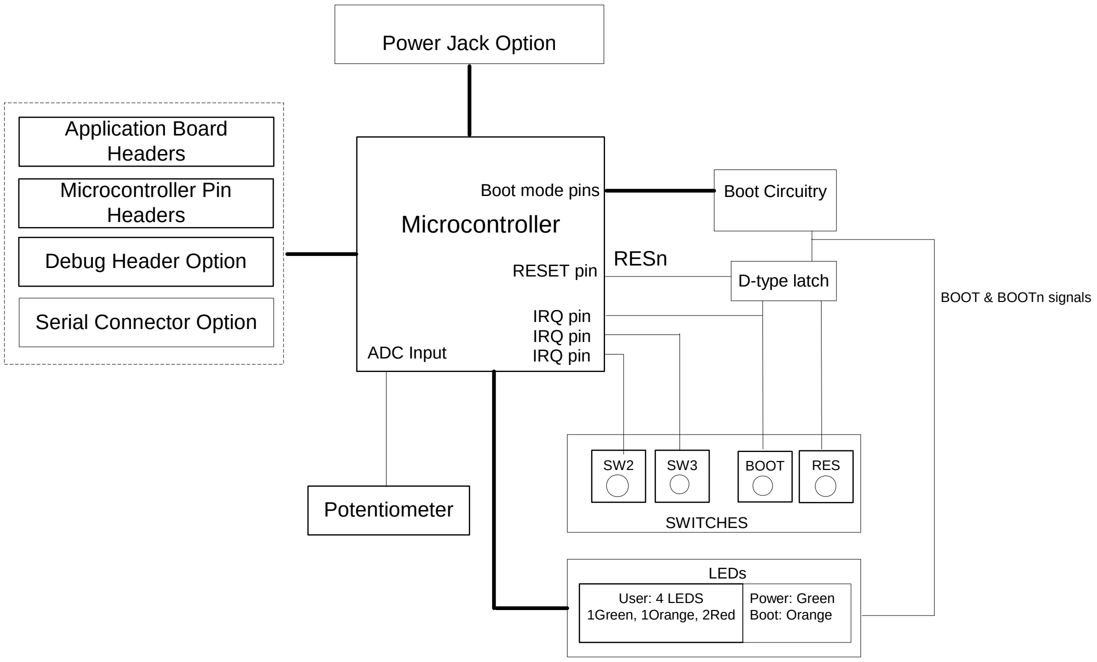

Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK.

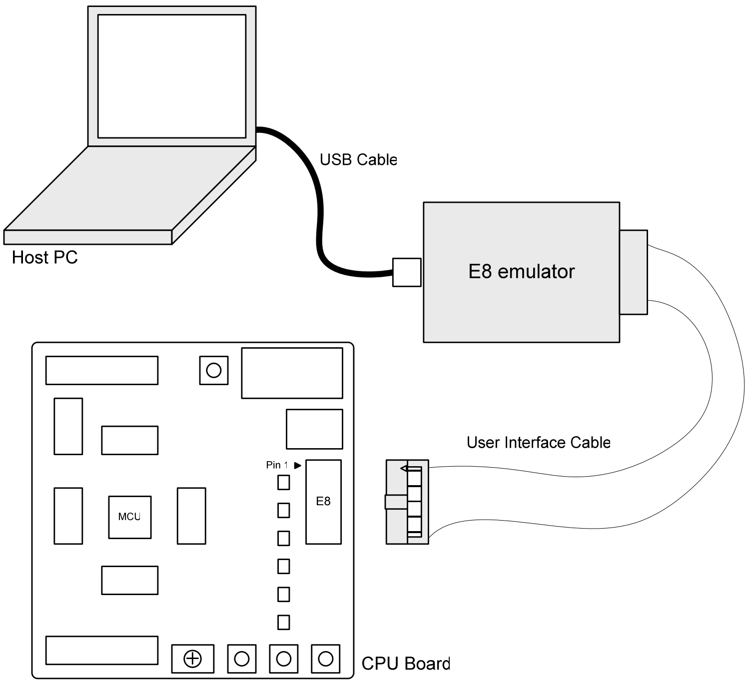

Figure 5-2 : RSK Connctions

Chapter 6.User Circuitry

6.1.Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1.

Switch	Function	Microcontroller
RES	When pressed; the CPU board microcontroller is reset.	RESn
SW1/BOOT*	Connects to an IRQ input for user controls. The switch is also used in conjunction with the RES switch to place the device in BOOT mode when not using the E8 debugger.	IRQ1, Pin 37 (Port B, pin 3)
SW2*	Connects to an IRQ line for user controls.	IRQ3 , Pin 36 (Port B, pin 5)
SW3*	Connects to the ADC analogue input.	AN3, Pin 44 (Port F, pin 3)

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

6.2.LEDs

There are six LEDs on the CPU board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

Table 6-2, below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Microcontroller Port Pin function	Microcontroller Pin Number	Polarity
LED0	Port E12	5	Active Low
LED1	Port E13	3	Active Low
LED2	Port E14	2	Active Low
LED3	Port E15	1	Active Low

Table 6-2:LED Port

6.3.Potentiometer

A single turn potentiometer is connected to AN2 of the microcontroller. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

6.4.Serial port

The microcontroller programming serial port (SCI) is connected to the E8 connector. This serial port can optionally be connected to the RS232 transceiver by fitting option resistors and the D connector in position J7. The connections to be fitted are listed in the following table.

Description	Function	Fit for RS232
TxD1	Programming Serial Port	R48
RxD1	Programming Serial Port	R49

Table 6-3:Serial Options Links

N.B. Do not connect an E8 if the RS232 port is used.

The board is designed to accept a straight through RS232 cable.

6.5.LCD Module

A LCD module can be connected to the connector J8. Any module that conforms to the pin connections and has a KS0066u compatible controller can be used with the tutorial code. The LCD module uses a 4bit interface to reduce the pin allocation. No contrast control is provided; this must be set on the display module.

Table 6-4 shows the pin allocation and signal names used on this connector.

The module supplied with the CPU board only supports 5V operation.

J13					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Ground	-	2	5V Only	-
3	No Connection	-	4	LCD_RS	26
5	R/W (Wired to Write only)	-	6	LCD_E	24
7	No Connection	-	8	No connection	-
9	No Connection	-	10		-
11	LCD_D4	11	12	LCD_D5	9
13	LCD_D6	10	14	LCD_D7	7

Table 6-4 LCD Module Connections

6.6.Option Links

Table 6-5 below describes the function of the option links contained on this CPU board. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R1	Oscillator	Feedback Resistor across X1	**No feedback**	
R2	Oscillator	**Connects X1 to Microcontroller**	Disconnects X1 from Microcontroller	R3, 4, 5
R3	Oscillator	**Connects X1 to Microcontroller**	Disconnects X1 from Microcontroller	R2, 4, 5
R4	Oscillator	Connects external clock to Microcontroller	**Disconnects external clock from Microcontroller**	R2, 3, 5
R5	Oscillator	Connects external clock to Microcontroller	**Disconnects external clock from Microcontroller**	R2, 3, 4
R10	Power	**Connect J5 to CON_5V**	Disconnect J5	
R11	Power	**UC_VCC Connected**	Disconnect to enable Microcontroller supply current to be measured.	
R12	Power	**Connect Board_VCC to CON_5V**	Disconnect Board_VCC from CON_5V	
R13	Power	**Connect AVCC to CON_5V**	Disconnect AVCC from CON_5V	
R14	Power	**Connect AVSS to GND**	Disconnect AVSS from GND	
R15	Power	**Connect AVSS to GND**	Disconnect AVSS from GND	
R47	RS232 Serial	Shutdown RS232 Transceiver	**Do not shutdown RS232 Transceiver**	
R48	RS232 Serial	Connect TTX to RS232 Serial port (E8 remains connected)	**Only E8 connected**	R49

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R49	RS232 Serial	Connect TRX to RS232 Serial port (E8 remains connected)	Only E8 connected	R48
R50	E8	E8 enabled	E8 disabled	
R51	E8	E8 connected to FWE	E8 not connected to FWE	
R54	Application Board Interface	Connect SCIaTX of application board interface to PA_9	Disconnect SCIaTX of application board interface	R55
R55	Application Board Interface	Connect TDO of application board interface to PA_9	Disconnect TDO of application board interface	R54
R56	Application Board Interface	Connect SCIaRX of application board interface to PA_8	Disconnect SCIaRX of application board interface	R57
R57	Application Board Interface	Connect TDI of application board interface to PA_8	Disconnect TDI of application board interface	R56
R58	Application Board Interface	Connect SCIaCK of application board interface to PA_7	Disconnect SCIaCK of application board interface	R59, 60
R59	Application Board Interface	Connect IO_3 of application board interface to PA_7	Disconnect IO_3 of application board interface	R58, 60
R60	Application Board Interface	Connect TCK of application board interface to PA_7	Disconnect TCK of application board interface	R58, 59
R61	Application Board Interface	Connect TMR1 of application board interface to PE_0	Disconnect TMR1 of application board interface	R62
R62	Application Board Interface	Connect IO_4 of application board interface to PE_0	Disconnect IO_4 of application board interface	R61
R63	Application Board Interface	Connect TRIGb of application board interface to PE_2	Disconnect TRIGb of application board interface	R64
R64	Application Board Interface	Connect IO_6 of application board interface to PE_2	Disconnect IO_6 of application board interface	R63
R65	Application Board Interface	Connect MO_UD of application board interface to PB_1	Disconnect MO_UD of application board interface	R66
R66	Application Board Interface	Connect TRISTn of application board interface to PB_1	Disconnect TRISTn of application board interface	R65
R68	LCD module	Connect LCD_E of application board interface to PA_1	Disconnect LCD_E	
R69	LCD module	Connect LCD_D5 of application board interface to PE_9	Disconnect LCD_D5	

Table 6-5 Option Links

6.7.Oscillator Sources

A crystal oscillator is fitted on the CPU board and used to supply the main clock input to the Renesas microcontroller. Table 6- details the oscillators that are fitted and alternative footprints provided on this CPU board:

Component					
		Value : Package	Manufacturer		
Crystal (X1)	Fitted	10Mhz	Approved	See www.renesas.com for details	
			CPU board		

Table 6-6: Oscillators / Resonators

Warning: When replacing the default oscillator with that of another frequency, the debugging monitor will not function unless the following are corrected:

- FDT programming kernels supplied are rebuilt for the new frequency
- The supplied HMON debugging monitor is updated for baud rate register settings.

The user is responsible for code written to support operating speeds other than the default. See the HMON User Manual for details of making the appropriate modifications in the code to accommodate different operating frequencies.

6.8.Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between Boot Mode, User Boot Mode and User mode. This circuit is not required on customers' boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the hardware manual for more information on the requirements of the reset circuit.

The reset circuit operates by latching the state of the boot switch on pressing the reset button. This control is subsequently used to modify the mode pin states as required.

The mode pins should change state only while the reset signal is active to avoid possible device damage.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7.Modes

The CPU board supports User Program mode and Boot mode. User Program mode may be used to run and debug user code, while Boot mode may only be used to program the Renesas microcontroller with program code. Both modes access the User MAT (the main area of 64Kbytes of Flash ROM on the device). Further details of programming the MAT are available in the SH7124 hardware manual.

When using the E8 debugger supplied with the RSK the mode transitions are executed automatically. The CPU board provides the capability of changing between User and Boot modes using a simple latch circuit. This is only to provide a simple mode control on this board when the E8 is not in use.

To manually enter boot mode, press and hold the SW1/BOOT. The mode pins are held in their boot states while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

More information on the operating modes can be found in the device hardware manual.

7.1.FDT Settings

In the following sections the tables identify the FDT settings required to connect to the board using the E8Direct debugger interface. The 'A' interface is inverted on the RSK board. This is to ensure the board can function in a known state when the E8 is connected but not powered. The E8 Debugger contains the following 'pull' resistors.

E8 Pin	Resistor
A	Pull Down (100k)
B	Pull Up (100k)

Table 7-1:E8 Mode Pin Drives

7.1.1.Boot mode

The boot mode settings for this CPU board are shown in Table 7-1 below:

FWE	MD1	LSI State after Reset End	FDT Settings	
			A	B
1	0	Boot Mode	0	1

Table 7-1: Mode pin settings

The following picture shows these settings made in the E8Direct configuration dialog from HEW.

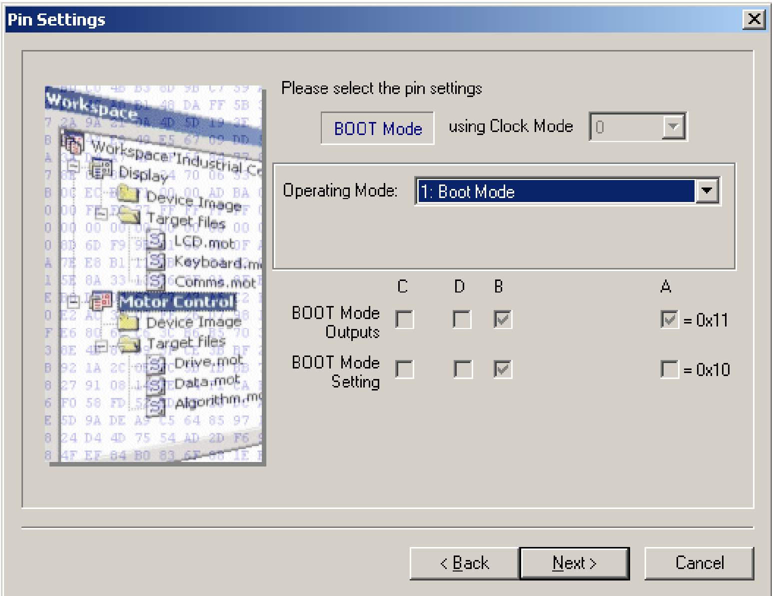

Figure 7-1: Boot Mode FDT configuration

7.1.2.User Mode

For the device to enter User Mode, reset must be held active while the microcontroller mode pins are held in states specified for User Mode operation. 100K pull up and pull down resistors are used to set the pin states during reset.

The SH7124 supports 4 user modes. The memory map in all of these modes is 16Mbyte in size. The default user mode for CPU board supporting SH7124 is 6.

FWE	MD1	LSI State after Reset End	FDT Settings	
			A	B
1	1	User Program Mode	1	1

Table 7-2: Mode pin settings

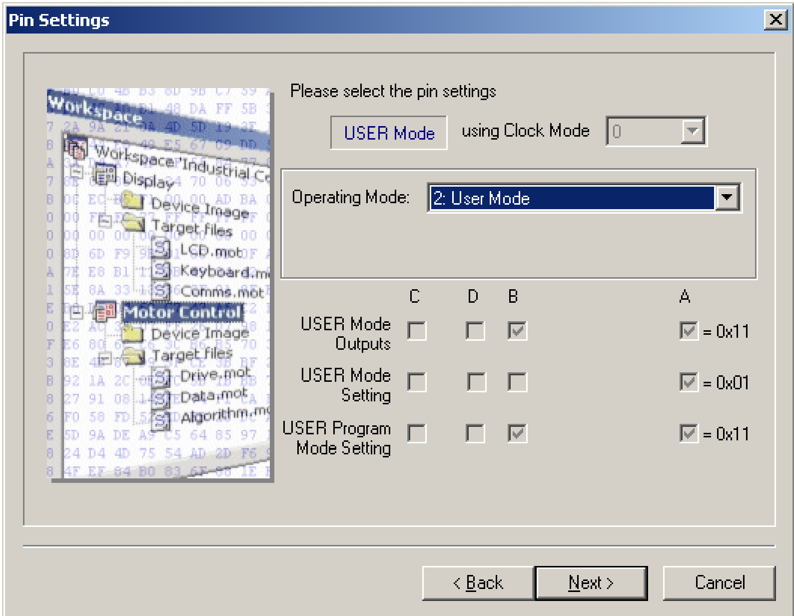

Figure 7-2: User mode FDT configuration

Chapter 8.Programming Methods

All of the Flash ROM on the device can be programmed when the device is in Boot mode. Once in boot mode, the boot-loader program pre-programmed into the microcontroller executes and attempts a connection with a host (for example a PC). On establishing a connection with the microcontroller, the host may then transmit program data to the microcontroller via the appropriate programming port.

Table 8-1 below shows the programming port for this Renesas Microcontroller and its associated pins

Programming Port Table – Programming port pins and their CPU board signal names		
SCI	TXD1, Pin 22	RXD1, PIN 23
CPU board Signal Name	E8_TTX/TMS	E8_TRX/TRST

Table 8-1: Serial Port Boot Channel

8.1.Serial Port Programming

This sequence is not required when debugging using the E8 supplied with the kit.

The microcontroller must enter boot mode for programming, and the programming port must be connected to a host for program download. To execute the boot transition, and allow programs to download to the microcontroller, the user must perform the following procedure:

Connect a 1:1 serial cable between the host PC and the CPU board

Depress the BOOT switch and keep this held down

Depress the RESET switch once, and release

Release the BOOT switch

The Flash Development Toolkit (FDT) is supplied to allow programs to be loaded directly on to the board using this method.

8.2.E10A Header

This device supports an optional E10A debugging interface. The E10A provides additional debugging features including hardware breakpoints and hardware trace capability. (Check with the website at www.renesas.com or your distributor for a full feature list).

Modifications to support E10A Debugger	
J9	Fit
J11	Fit: connect jumper between pins 2 & 3.
R51	Remove
R54	Remove
R55	Fit 0R Resistor
R56	Remove
R57	Fit 0R Resistor
R58	Remove
R59	Do not fit.
R60	Fit 0R Resistor

Table 8-2: E10A connections

Chapter 9.Headers

9.1.Microcontroller Headers

Table 9-1 to Table 9-4 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

J1					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	MO_Wn	1	2	MO_Vn	2
3	MO_Wp	3	4	UC_VCC	4, 17
5	MO_Vp	5	6	Ground	6, 19
7	MO_Un	7	8	NC	-
9	MO_Up	9	10	TRIGa	10
11	TMR0	11	12	IO_7	12

Table 9-1: J1

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	TRIGb/IO_6	13	2	IO_5	14
3	TMR1/IO_4	15	4	SCIaTx/TDO	16
5	UC_VCC	4, 17	6	SCIaRx/TDI	18
7	Ground	6, 19	8	SCIaCK/IO_3/TCK	20
9	IO_2	21	10	E8_TTX/TMS	22
11	E8_TRX/TRST	23	12	IO_1	24

Table 9-2: J2

J3					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	NC	-	2	IO_0	26
3	RESn	27	4	WDTOVF	28
5	CON_XTAL (via R5 when fitted)	29	6	CON_EXTAL (via R4 when fitted)	30
7	ASEMD0	31	8	NMI	32
9	FWE_E8B/ASEBRK	33	10	MD1_E8A	34
11	Ground	6, 19	12	IRQ3	36

Table 9-3: J3

J4					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	IRQ1	37	2	MO_UD/TRISTn	38
3	AVss	39	4	PF7	40
5	PF6	41	6	AD3	42
7	AD1	43	8	User_SW3	44
9	AD_POT	45	10	AD2	46
11	AD0	47	12	AVcc	48

Table 9-4: J4

9.2.Application Headers

Table 9-5 and Table 9-6 below show the standard application header connections.

JA1									
Pin	Generic Header Name		CPU board Signal Name	Device Pin	Pin	Header Name		CPU board Signal Name	Device Pin
1	Regulated Supply 1		5V		2	Regulated Supply 1		GROUND	
3	Regulated Supply2		NC	-	4	Regulated Supply 2		GROUND	
5	Analogue Supply		AVcc	48	6	Analogue Supply		AVss	39
7	Analogue Reference		NC	-	8	ADTRG		NC	-
9	ADC0	I0	AD0	47	10	ADC1	I1	AD1	43
11	ADC2	I2	AD2	46	12	ADC3	I3	AD3	42
13	DAC0		NC	-	14	DAC1		NC	-
15	IOPort		IO_0	26	16	IOPort		IO_1	24
17	IOPort		IO_2	21	18	IOPort		IO_3	20
19	IOPort		IO_4	15	20	IOPort		IO_5	14
21	IOPort		IO_6	13	22	IOPort		IO_7	12
23	Open drain	IRQAEC	IRQ3	36	24	I²C Bus - (3rd pin)		NC	-
25	I²C Bus		NC	-	26	I²C Bus		NC	-

Table 9-5: JA1 Standard Generic Header

JA2								
Pin	Generic Header Name		CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	Open drain		RESn	27	2	External Clock Input	CON_EXTAL	30*
3	Open drain		NMI	32	4	Regulated Supply 1	Vss1	6
5	Open drain output		WDTOVF	28	6	Serial Port	SCIaTX	16
7	Open drain	WUP	NC	-	8	Serial Port	SCIaRX	18
9	Open drain		IRQ1	37	10	Serial Port	SCIaCK	20
11	Up/down		MO_UD	38	12	Serial Port Handshake	NC	-
13	Motor control		MO_Up	9	14	Motor control	MO_Un	7
15	Motor control		MO_Vp	5	16	Motor control	MO_Vn	2
17	Motor control		MO_Wp	3	18	Motor control	MO_Wn	1
19	Output		TMR0	11	20	Output	TMR1	15
21	Input		TRIGa	10	22	Input	TRIGb	13
23	Open drain		NC	-	24	Tristate Control	TRISTn	38
25			PF6	41	26		PF7	40

Table 9-6: JA2 Standard Generic Header

Chapter 10.Code Development

10.1.Overview

Note: For all code debugging using Renesas software tools, the CPU board must either be connected to a PC serial port via a serial cable or a PC USB port via an E8. An E8 is supplied with the RSK product.

The HMON embedded monitor code is modified for each specific Renesas microcontroller. HMON enables the High-performance Embedded Workshop (HEW) development environment to establish a connection to the microcontroller and control code execution. Breakpoints may be set in memory to halt code execution at a specific point.

Unlike other embedded monitors, HMON is designed to be integrated with the user code. HMON is supplied as a library file and several configuration files. When debugging is no longer required, removing the monitor files and library from the code will leave the user's code operational.

The HMON embedded monitor code must be compiled with user software and downloaded to the CPU board, allowing the users' code to be debugged within HEW.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at www.renesas.com to check for the latest updates to the Compiler and Debugger manuals.

10.2.Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 256k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3.Mode Support

The HMON library is built to support 16Mbyte Advanced Mode only for the SH7124 family.

10.4.Breakpoint Support

The device does not include a user break controller. No breakpoints can be located in ROM code. However, code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM. To debug with breakpoints in ROM you need to purchase the E10A-USB on-chip debugger at additional cost.

10.5.Code located in RAM

Double clicking in the breakpoint column in the HEW code window sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them. (See the Tutorial Manual for more information on debugging with the HEW environment.)

10.6.HMON Code Size

HMON is built along with the user's code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Start-up of HMON	H' 0000 0000	0x0004
SCI_VECTORS	HMON Serial Port Vectors (Vector 220, 221, 222, 223)	H'0000 0370	0x0010
PHMON	HMON Code	H'0000 3000	0x20EA
CHMON	HMON Constant Data	H'0000 50EC	0x013C
BHMON	HMON Un-initialised data	Variable	0x0259
UGenU	FDT Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H'0000 1000	0x1004
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H'0000 0800	0x0004

Table 10-1: HMON Code size

10.7.Memory Map

The memory map shown in this section visually describes the locations of program code sections related to HMON, the FDT kernels and the supporting code within the ROM/RAM memory areas of the microcontroller.

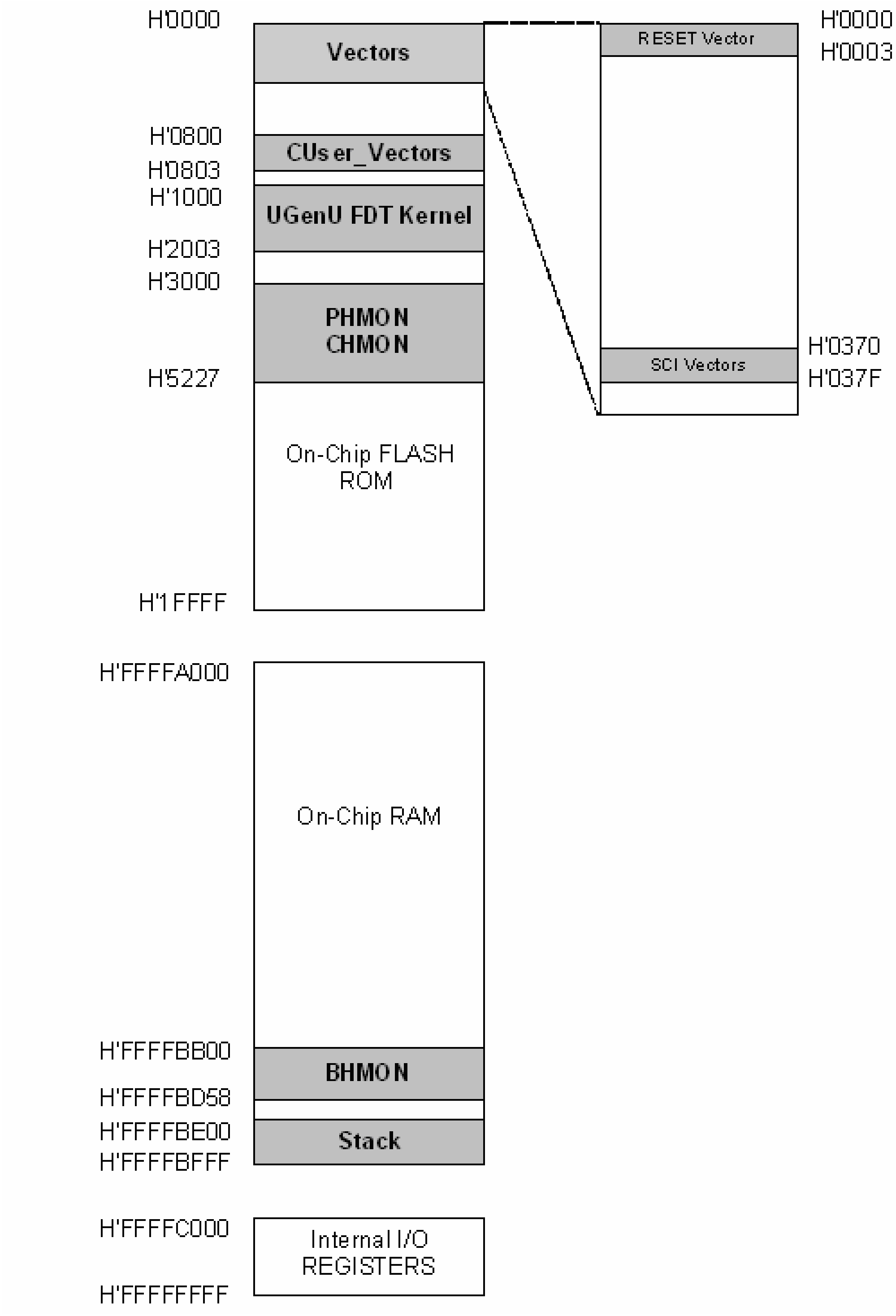

Figure 10-1: Memory Map

10.8.Baud Rate Setting

HMON is initially set to connect at 250000Baud. The value set in the baud rate register for the microcontroller must be altered if the user wishes to change either the serial communication baud rate of the serial port or the operating frequency of the microcontroller. This value is defined in the hmonserialconfiguser.h file, as SCI_CFG_BRR (see the Serial Port section for baud rate register setting values). The project must be re-built and the resulting code downloaded to the microcontroller once the BRR value is changed. Please refer to the HMON User Manual for further information.

10.9.Interrupt mask sections

HMON has an interrupt priority of 14. The serial port has an interrupt priority of 15. Modules using interrupts should be set to lower than this value (14 or below), so that serial communications and debugging capability is maintained.

Chapter 11. Component Placement

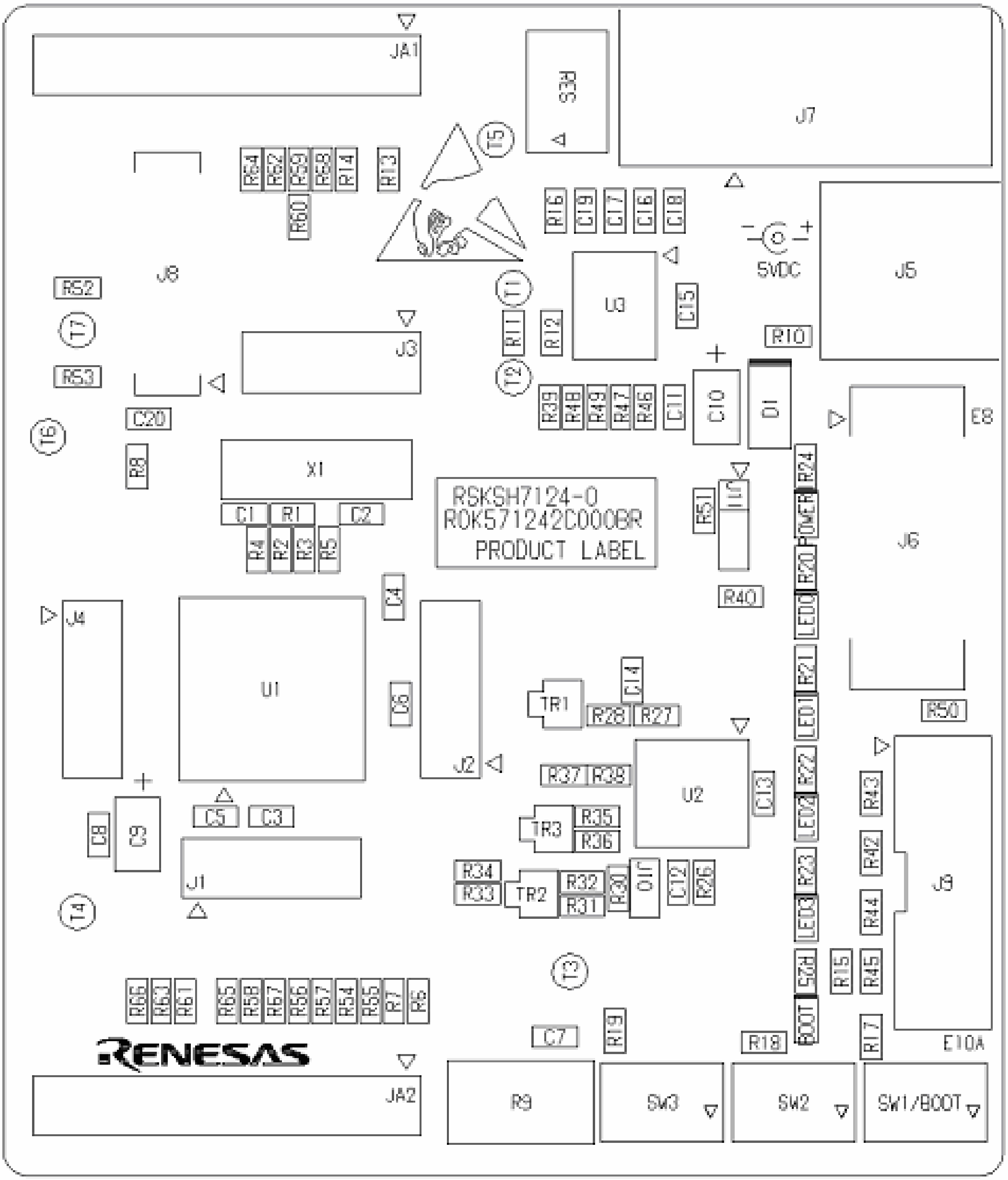

Figure 11-1: Component Placement

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the SH7124 series microcontrollers refer to the SH7125 Group, SH7124 Group *Hardware Manual*

For information about the SH7124 assembly language, refer to the SH *Series Programming Manual*

Online technical support and information is available at: http://www.renesas.com/rsk

Technical Contact Details

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Europe: tools.support.eu@renesas.com

Japan: csc@renesas.com

General information on Renesas Microcontrollers can be found on the Renesas website at: http://www.renesas.com/

Renesas Starter Kit for SH7124

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