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CPLD/FPGA BOARDS

Spartan 6 Tyro Kit

USER MANUAL

Contents

Introduction:

The board features:

- Xilinx Spartan 6 (XC6SLX9-TQG144) FPGA
- Xilinx Serial PROM (XCF04S)

External Peripherals Modules

- 128x64 G LCD with Contrast adjusts
- 16-Nos. General purpose point LEDs
- 16-Nos of Toggle switches (Digital inputs)
- 2-Nos. of Push Button
- 1-Nos. of Piezo Electric Buzzer
- 5V Relay with termination

Communication protocols

- Two Full Duplex UART (EIA RS232)

- SPI ADC and DAC interface

Other Features:

- 50 MHz crystal oscillator clock source
- Hard Reset Push Button

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1. Using Spartan-6 Tyro Kit

1.1 Package Contents

- Spartan-6 Tyro Kit
- Serial Port Cable

- JTAG Download Cable
- Printed User Manual
- 9V Power AC Adaptor
- LCD module (optional)
- GLCD module (optional)
- CD contains
    - Software
    - Example Programs
    - User Manual
    - Simple Projects

2. Learning Spartan-6 Tyro kit

The Spartan-6 Board comes with Xilinx Spartan-6(XC6SLX9) FPGA. It consist of several peripherals, power supply and supporting device circuitry systems. Spartan-6 Board provides a basic development platform for the FPGA device with all I/O available to the user. The device may be programmed in-circuit through the JTAG port from the PC. We meet all the basic specifications' standards with this product. One can experience the ease in the experimentation of Xilinx FPGA with many of the external peripherals.

2.1 Components placement

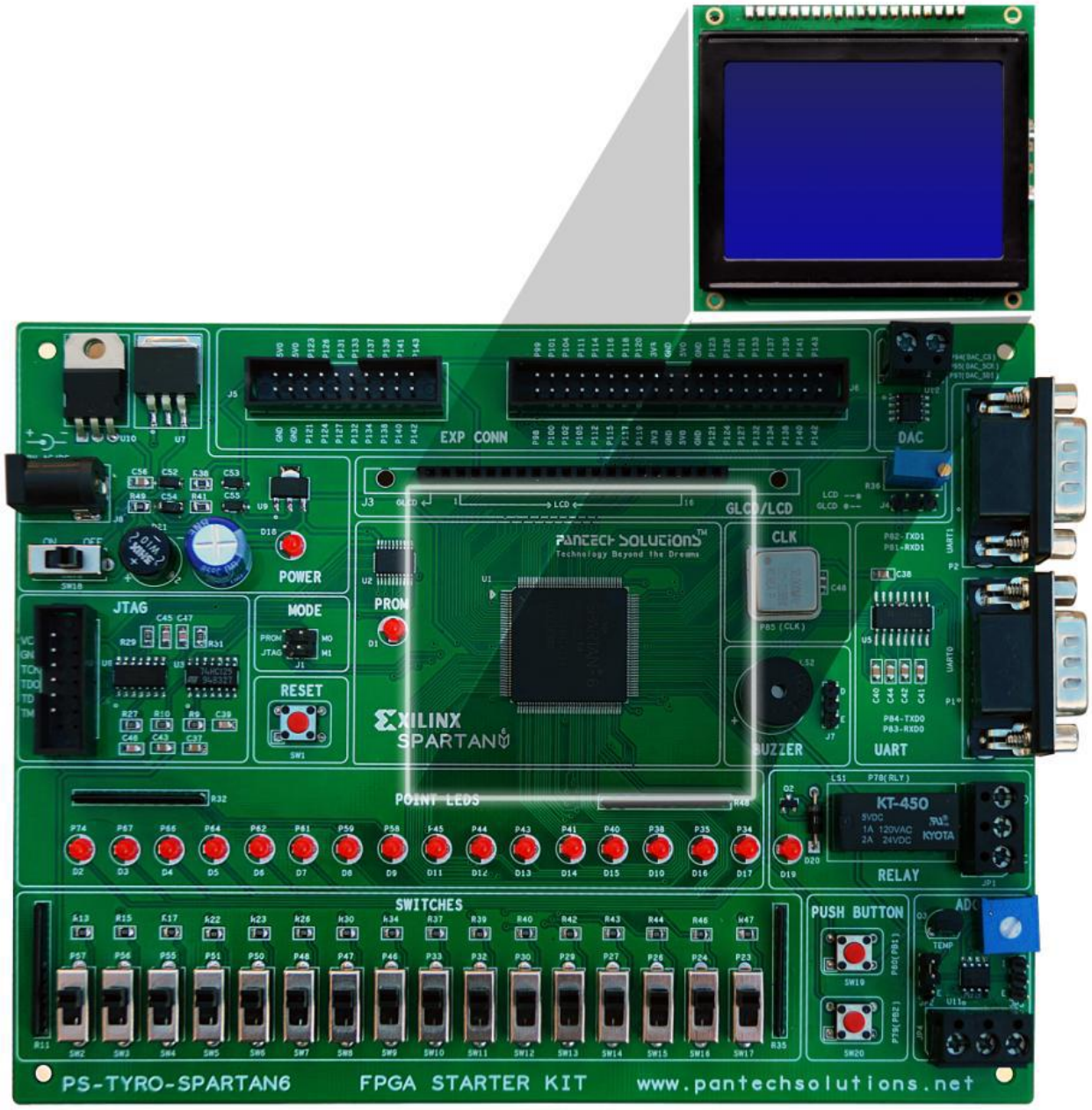


Figure 1.Spartan-6 Tyro Kit Components placement

2.2 Block Diagram

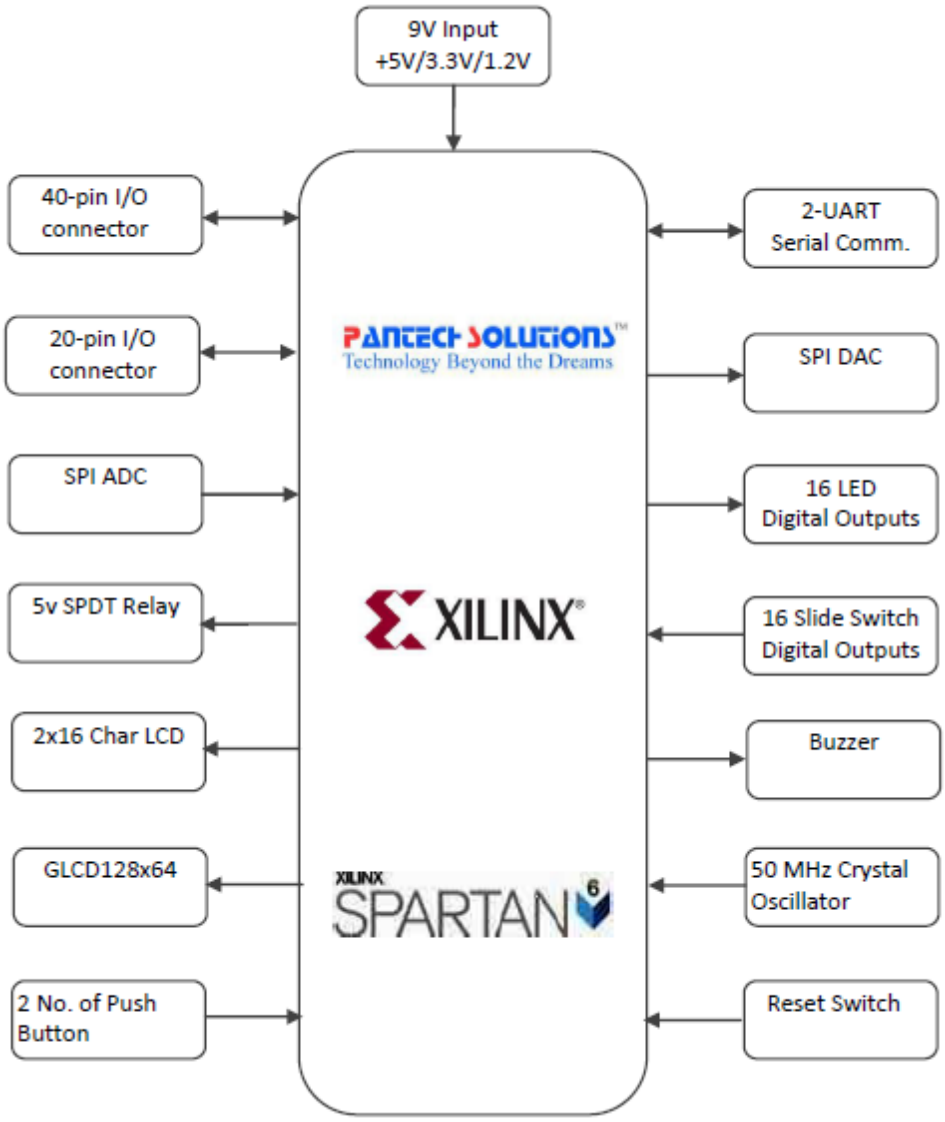


Figure 2 Spartan-6 Tyro Kit Block Diagram

2.3 Power Distribution

2.3.1AC Wall Adapter

The Spartan-6 Tyro Kit includes an AC wall adapter that produces a +9V DC output. Connect the AC wall adapter to the barrel connector along the left edge of the board, indicated as in **Error! Reference source not found.**. To disconnect power, switch off the power switch. The power indicator LED, lights up when power is properly applied to the board. The AC wall adapter operates from 100V to 240V AC input, at 50 or 60 Hz.

Voltage Regulators There are multiple voltages supplied on the Spartan-6 Tyro Kit Lab Kit: 5V, 3.3V and 1.2V regulators. The 3.3V regulator feeds all the VCCO voltage supply inputs to the FPGA's I/O banks and powers most of the components on the board. The 3.3V regulator supplies power to the FPGA's VCCAUX supply inputs. The VCCAUX voltage input supplies power to Digital Clock Managers (DCMs) within the FPGA and supplies some of the I/O structures. In specific, all of the FPGA's dedicated configuration pins, such as DONE, PROG_B, CCLK, and the FPGA's JTAG pins, are powered by VCCAUX. The FPGA configuration interface on the board is powered by 3.3V. Consequently, the 3.3V supply has a current shunt resistor to prevent reverse current. Finally, the 1.2V regulator supplies power to the FPGA's VCCINT voltage inputs, which power the FPGA's core logic. The board uses four discrete regulators to generate the necessary voltages. The 5V Regulator supplies power for Stepper Motor, DC Motor, Relays, GLCD and LCD.

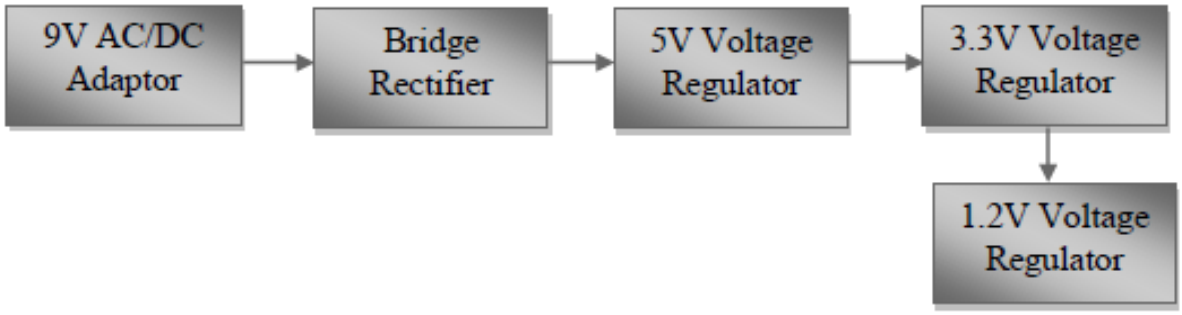


Figure 3 Spartan-6 Tyro Kit Power Supply

2.4 On-board Peripherals

The Spartan-6 Tyro Kit comes with many interfacing options

- 2 Nos. of Push Button
- 16-Nos. of Toggle switches (Digital Inputs)
- 16-Nos. of Point LED's (Digital Outputs)
- 2x16 Character LCD
- 128x64 G LCD with Contrast adjusts
- 5V Relay
- Two UART for serial port communication through PC

- Piezo Electric Buzzer
- SPI ADC
- SPI DAC
- Reset switch

2.5 Digital Inputs Toggle Switch

The Spartan-6 Tyro Kit has 16-slide switches, indicated as in Figure 44. The switches connect to an associated pin name, as shown in Table 1. A detailed schematic appears in Figure 4.

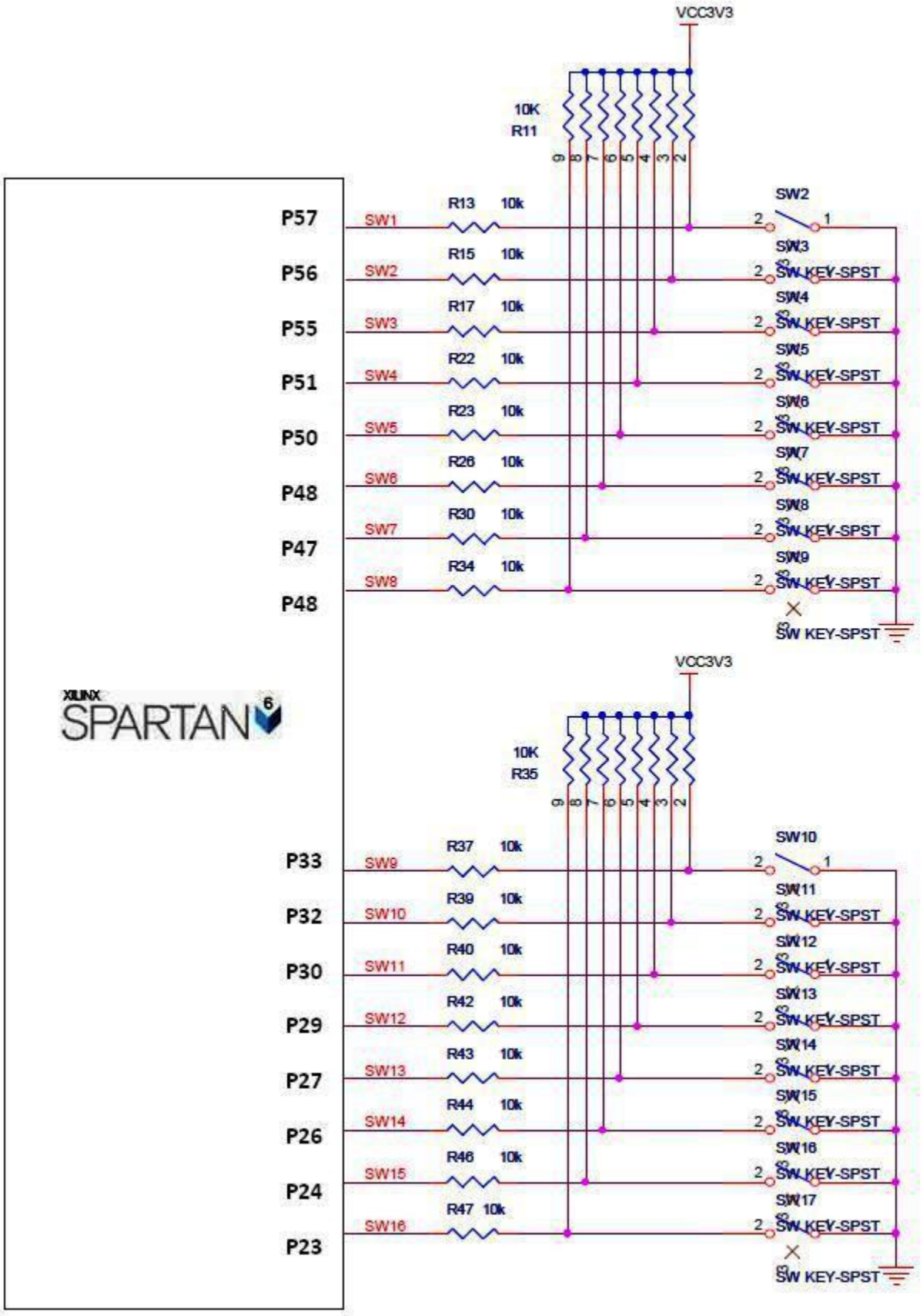


Table 1. Pin Connections to Slide Switches

SWITCH	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	Sw8	Sw9
Pin Name	P57	P56	P55	P51	P50	P48	P47	P46
SWITCH	Sw10	Sw11	Sw12	Sw13	Sw14	Sw15	Sw16	Sw17
Pin Name	P33	P32	P30	P29	P27	P26	P24	P23

When in the UP or ON position, a switch connects logic High. When DOWN or in the OFF position, the switch connects to ground, a logic Low. The switches typically exhibit about 2 ms of mechanical bounce and there is no active debouncing circuitry, although such circuitry could easily be added to the FPGA design programmed on the board. A 10KΩ series resistor provides nominal input protection.

Example Code

To see the demo result, click  inside Digital Input Switch folder of the CD.

2.6 Light Emitting Diodes

Light Emitting Diodes (LEDs) are the most commonly used components, usually for displaying pin's digital states. The Spartan-6 Tyro Kit has 16- LEDs located above the slide switches, indicated by in Figure5.

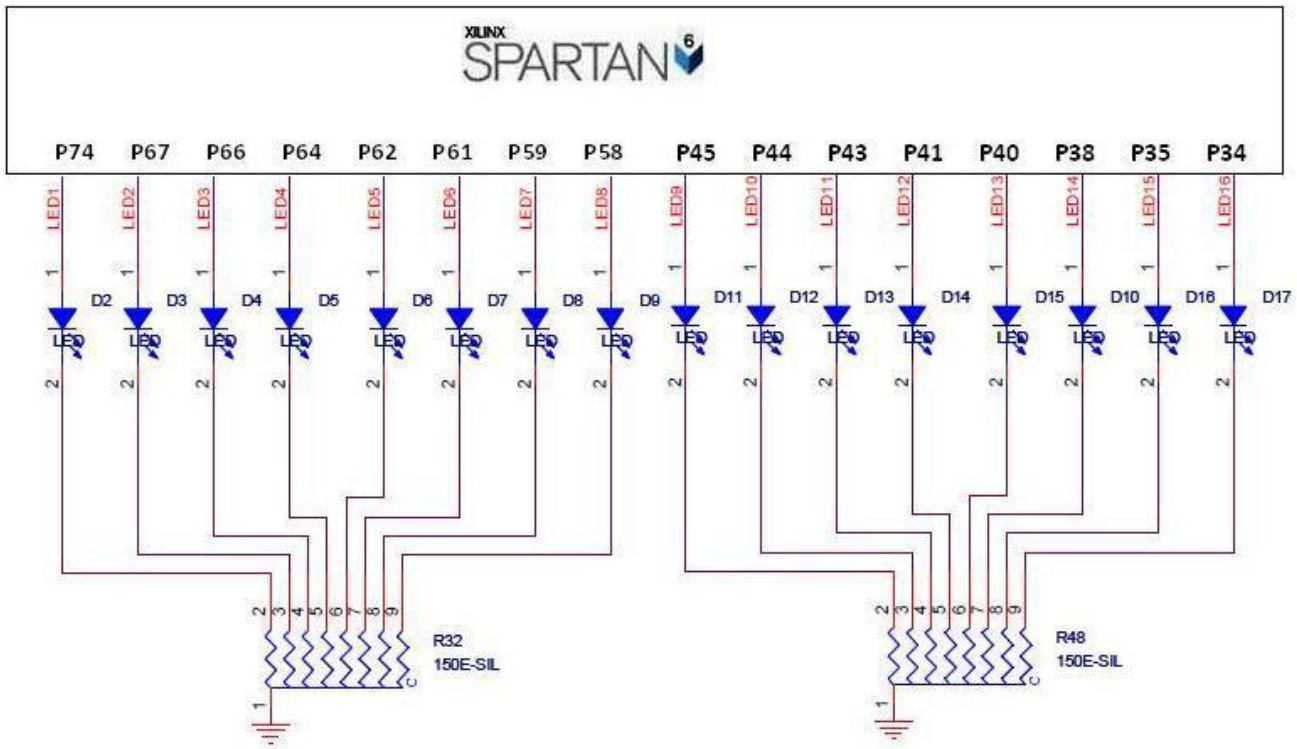


Figure 5.Point LED interface from Spartan-6 Tyro Kit

Table 2.Pin connections to the LEDs

ED	2	3	4	5	6	7	8	9
Pin Name	74	67	66	64	62	61	59	58
ED	10	11	12	13	14	15	16	17
Pin Name	45	44	43	41	40	38	35	34

The cathode of each LED connects to ground via a 220 ohm Ω resistor. To light an individual LED, drive the associated FPGA control signal High, which is the opposite polarity from lighting one of the 7-segment LEDs.

Example Code

To see the demo result, click  inside LED folder of the CD.

2.7 Character 2 x 16 LCD

The Spartan-6 Tyro Kit prominently features a 2-line by 16-character liquid crystal display (LCD). The Top board controls the LCD via

the 8-bit data interface shown in Figure. Although the LCD supports an 8-bit data interface..

2.7.1Voltage Compatibility

The character LCD is power by +5V. The FPGA I/O signals are powered by 3.3V. However, the FPGA's output levels are recognized as valid Low or High logic levels by the LCD. The LCD controller accepts 5V TTL signal levels and the 3.3V LVCMOS outputs provided by the FPGA to meet the 5V TTL voltage level requirements. The character LCD drives the data lines when LCD_RW is high. Most applications treat the LCD as a write-only peripheral and never read from the display.

Table 3.Pin Connection to LCD Interface

Signal	PIN Name
R/W	P10
RS	P8
E	P9
D0	P22
D1	P21
D2	P17
D3	P16
D4	P15

D5	P14
D6	P12
D7	P11

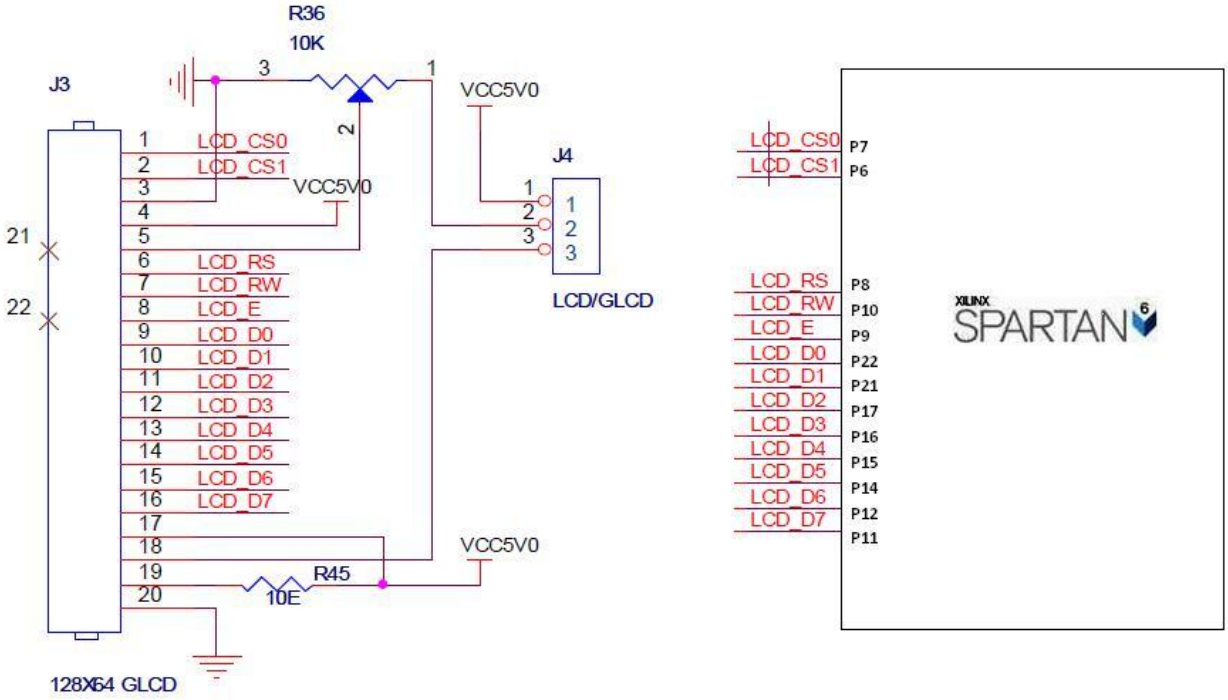


Figure 7.LCD connections from Spartan-6 Tyro Kit

Example Code

To see the demo result, click  inside LCD folder of the CD.

2.8 128 x 64 GLCD

The Spartan-6 Tyro Kit has 128x64 GLCD. 14 pins are needed to create 8-bit interface; 8 data bits (DB0-DB7), two chip select line (CS1) and (CS2), address bit (R/S), read/write bit (R/W) and control signal (E) and Reset (RST). The GLCD controller is a standard S6B0108 or equivalent, which is a very well-known interface for Graphical based LCDs.

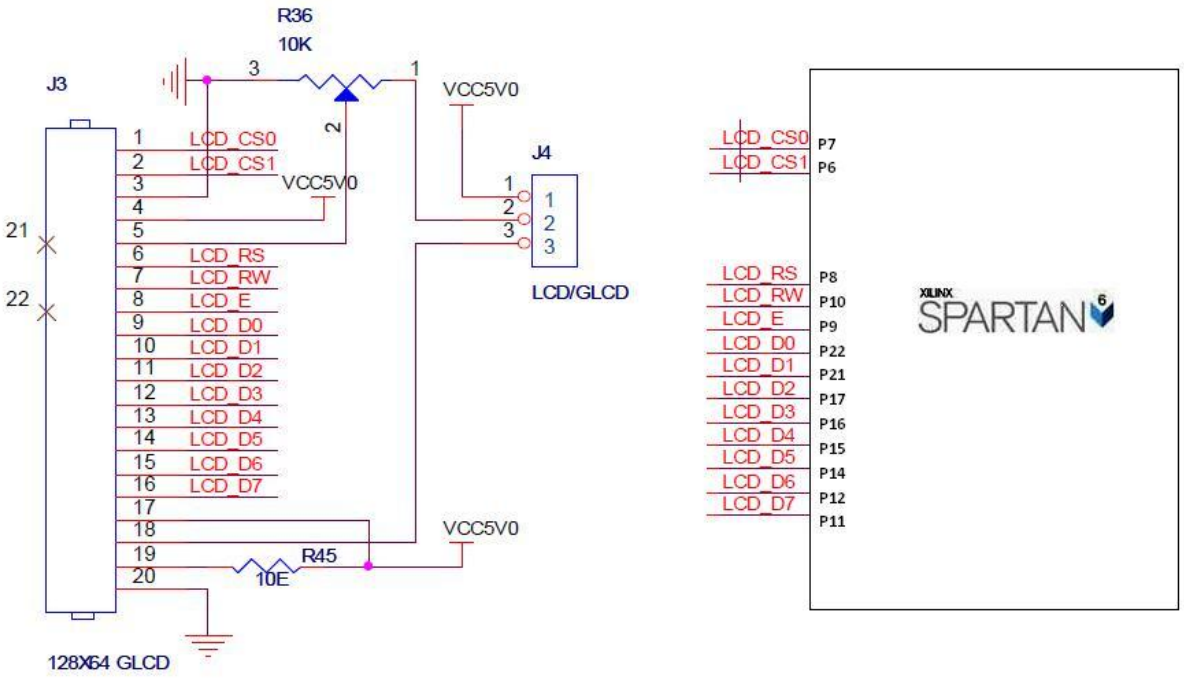


Figure 8.GLCD connections from Spartan-6 Tyro Kit

Table 4.Pin Connection to GLCD Interface

Signal	PIN Name
R/W	P10
RS	P8
E	P9
D0	P22
D1	P21
D2	P17
D3	P16
D4	P15
D5	P14
D6	P12
D7	P11
CS1	P7
CS2	P6

Example Code

To see the demo result, click  inside GLCD folder of the CD.

2.9 Relay Section

In Spartan-6 Tyro Kit , SPDT relay is used. TThe relays operate on 5V DC. The outputs of both the terminals of the relay are taken out on the connecter to connect the external circuitry.

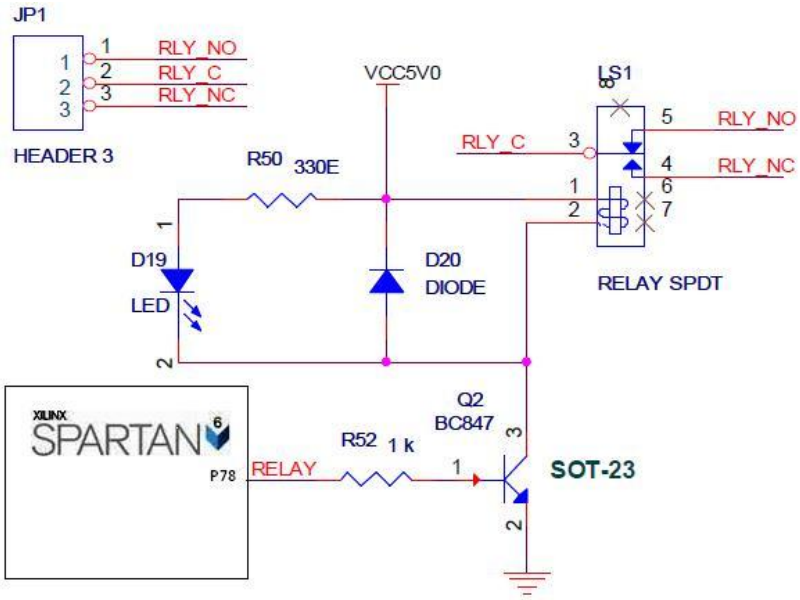


Figure 9.Schematic showing the relay connections

Table 5.Pin Connections to Relay/Driver

Signals	PIN NAME
Relay	P78

Example Code

To see the demo result, click  inside Relay Control folder of the CD.

2.10 RS-232 Serial Port

USART stands for Universal Synchronous Asynchronous Receiver Transmitter. Spartan-6 Tyro Kit supports both types of communication. The Spartan-6 Tyro Kit provides an RS232 port that can be driven by the top board FPGA. A subset of the RS232 signals is used on the Kit to implement this interface (RD and TD signals). The Spartan-6 Tyro Kit provides 2- female connector DB-9 connector, labeled P1 and P2. This board utilizes the Maxim Instruments MAX3232 RS232 driver for driving the RD and TD signals.

Table 6. RS232 signals and their pin assignments to the Spartan-3 FPGA

Connector Name	Signals	FPGA PIN
P1	TXD0	P84
	RXD0	P83
P2	TXD1	P82
	RXD1	P81

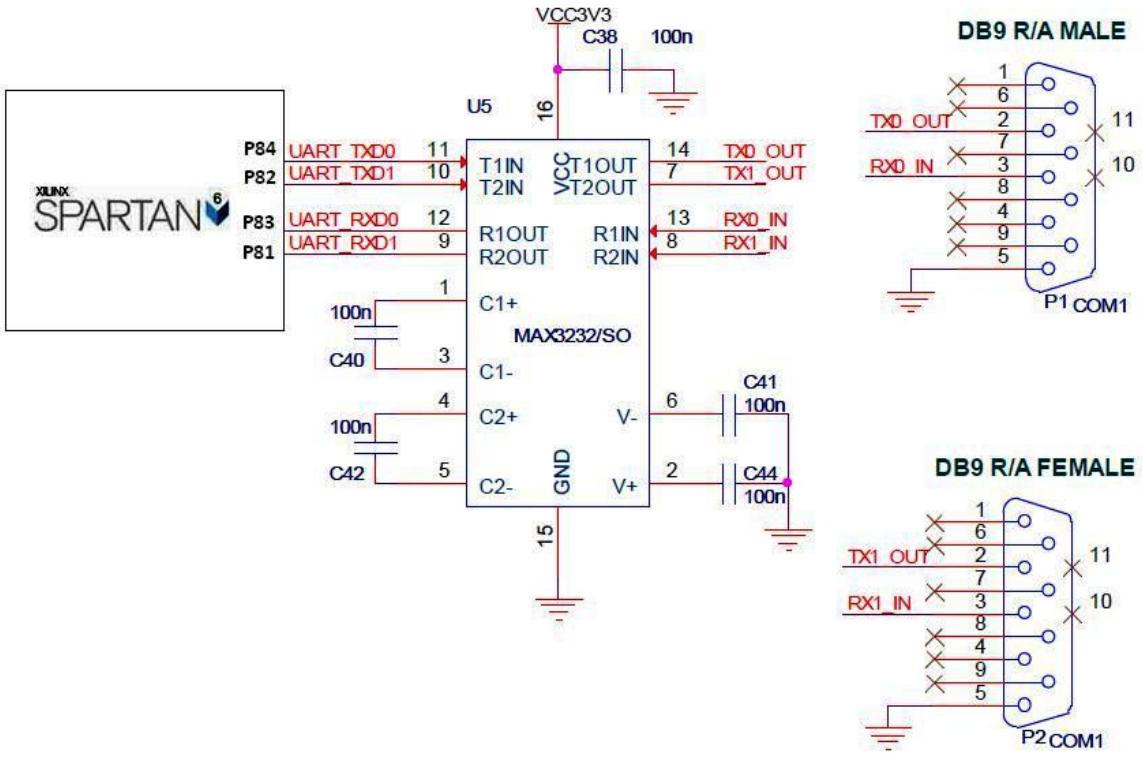


Figure 10.Detailed schematic of Spartan-6 Tyro Kit Interface with RS232

Example Code

To see the demo result, click  inside RS232 folder of the CD.

2.11 12 Bit ADC

These ADCs are SPI Bus based which is a serial bus. So the number of pins in IC is very low. Total of 4 lines are required to interface it with FPGA.

- MISO (Master In Slave Out)
- MOSI (Master Out Slave In)
- SCK (Serial Clock)
- CS (Chip Select)

Figure 11.SPI ADC Pin Diagram

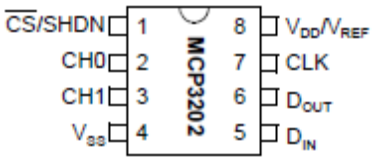
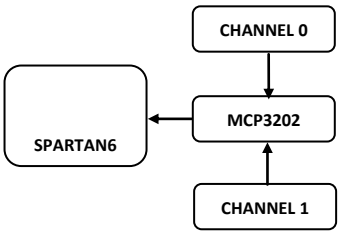


Table 7. ADC Pin Connection with Spartan-6 Tyro Kit

Connector Name	Signals	FPGA PIN
	DOUT	P93
	DIN	P92
	SCK	P88
	CS	P87

As you know in synchronous serial communication their is a clock line (SCK in case of SPI) which synchronizes the transfer.

The clock is always controlled by the MASTER. In our case the Spartan-6 is the MASTER and the MCP3202 is a slave on the bus. SPI is full duplex, which means data can be sent and received simultaneously.

SPI TRANSFER

A SPI transfer is initiated by the MASTER pulling the CS line low. The CS line sits at HIGH during idle state. Now master can write to the bus in 8bit (or 1 byte) chunks. One most important thing to note about SPI is that for every byte MASTER writes to SLAVE the MASTER receives one byte in return. So the only transaction possible is exchange of data. Their is no separate Read and Write commands their is only one command and that is Write.

Example Code

To see the demo result, click  inside ADC folder of the CD.

12 Bit SPI DAC

The controller designed coverts the digital data into analog, where the digital data is transferred using SPI Controller and DAC (MCP4921) converts the serial data into the analog. SPI Controller controls

the speed, data transmission, DAC selection etc. Based on the inputs from the SPI line, DAC (MCP4921) coverts the 12 bit data to analog.

Figure 12.SPI DAC Pin Diagram

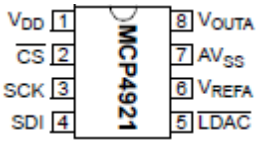
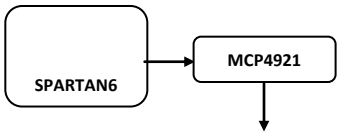


Table 8. DAC Pin Connection with Spartan-6 Tyro Kit

Connector Name	Signals	FPGA PIN
DAC SELECTION	CS	P97
	SCK	P95
	SDI	P94
ANALOG O/P		

Example Code

To see the demo result, click  inside DAC folder of the CD.

2.12 Push Button and Reset switch

It consist of two Push Buttons. It can be used to make an interrupt during application running. Reset switch forces the FPGA to reconfigure from the selected configuration memory source. Press and release this button to restart the FPGA configuration process at any time.

Table 9. Pin Connection with Spartan-6 Tyro Kit

Signals	PIN NAME
PushButton1	P80
PushButton2	P79
Reset	RST

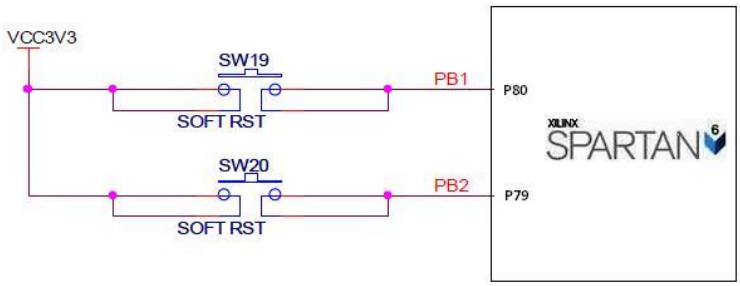


Figure 13.Push Button and Reset switch Interface with Spartan-6 Tyro Kit

2.13 Clock Source

The Spartan-6 Tyro Kit has a dedicated 50 MHz series clock oscillator source and an optional socket for another clock oscillator source. Figure provides a detailed schematic for the clock sources.

Table 10.Clock Oscillator Sources

Signals	PIN NAME
50MHZ	P85

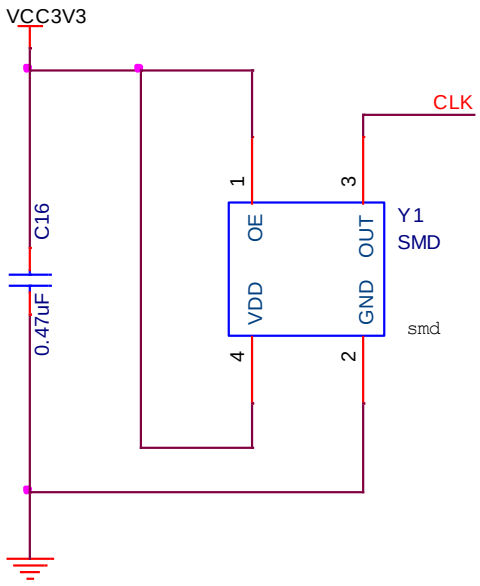


Figure 14. Clock source connections from Spartan-6 Tyro Kit

2.14 Expansion I/O Connectors

The Spartan-6 Tyro Kit consists of 20x2 pin connector and 2 no. of 10x2 pin connectors. Figure15 provides schematic for Expansion I/O connectors.

Table 11.Pin name for J9 and J11 10x2 pin Expansion Connector

Signals	10X2 EXP. CONNECTOR J5 PIN NAME
1	P143
2	P142
3	P141
4	P140
5	P139
6	P138
7	P137
8	P134
9	P133
10	P132
11	P131
12	P127
13	P126
14	P124
15	P123
16	P121

17	VCC
18	GND
19	VCC
20	GND

Table 12.Pin name for J6 20x2 pin Expansion Connector

Signals	20X2 EXP. CONNECTOR J6 PIN NAME	Signals	20X2 EXP. CONNECTOR J6 PIN NAME
1	P143	**21**	GND
2	P142	**22**	GND
3	P141	**23**	VCC 3V3
4	P140	**24**	VCC 3V3
5	P139	**25**	P120
6	P138	**26**	P119
7	P137	**27**	P118
8	P134	**28**	P117
9	P133	**29**	P116
10	P132	**30**	P115
11	P131	**31**	P114
12	P127	**32**	P112
13	P126	**33**	P111

14	P124	**34**	P105
15	P123	**35**	P104
16	P121	**36**	P102
17	GND	**37**	P101
18	GND	**38**	P100
19	VCC 5V	**39**	P99
20	VCC 5V	**40**	P98

2.15 Spartan-6 FPGA

Introduction

The purpose of this FPGA is to integrate all the necessary components for using a FPGA, but without being targeted on a special application. The board provides 102 I/O pins to the user, who can use them as inputs, outputs or both. The following figure elaborates the denotation.

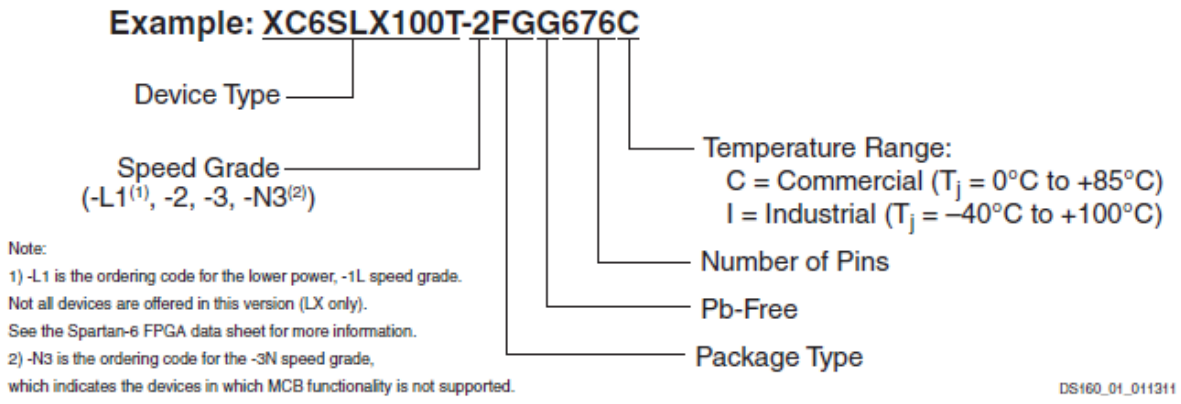


Figure 15.Spartan-6 FPGA ordering information

Device Part Marking

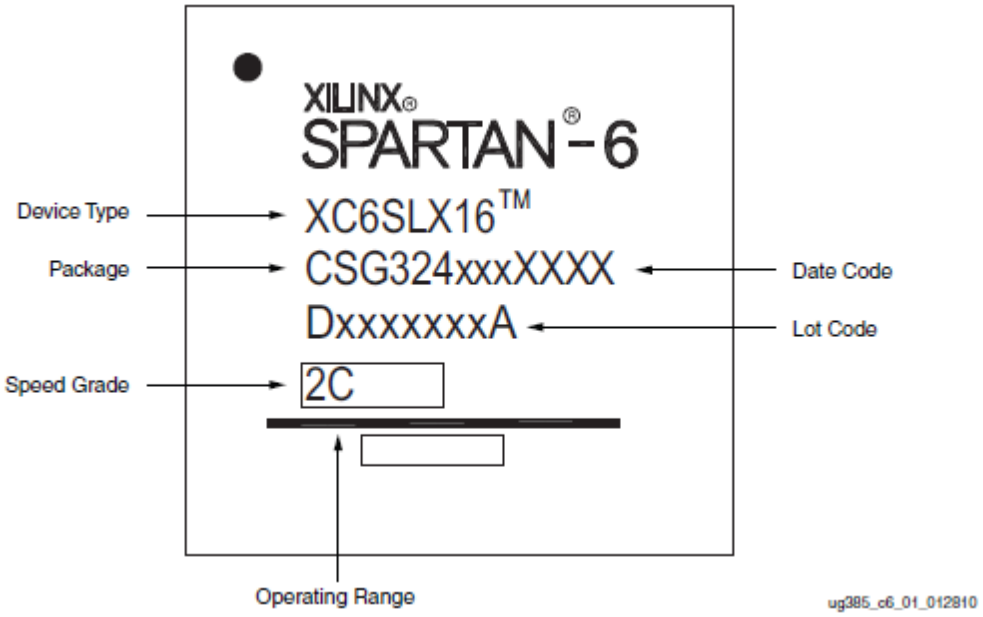


Figure 16.Spartan-6 FPGA Device Part Marking

The second important component on this board is the XCF04S-PROM, in which you can store a bit-file. The FPGA can be programmed directly from the PROM or through the JTAG connection. If the PROM-Boot option is enabled, the FPGA will be programmed out of the PROM when the power is turned on.

Also includes a JTAG programming and debugging chain.

A general overview of the FPGA architecture is presented in the following figure.

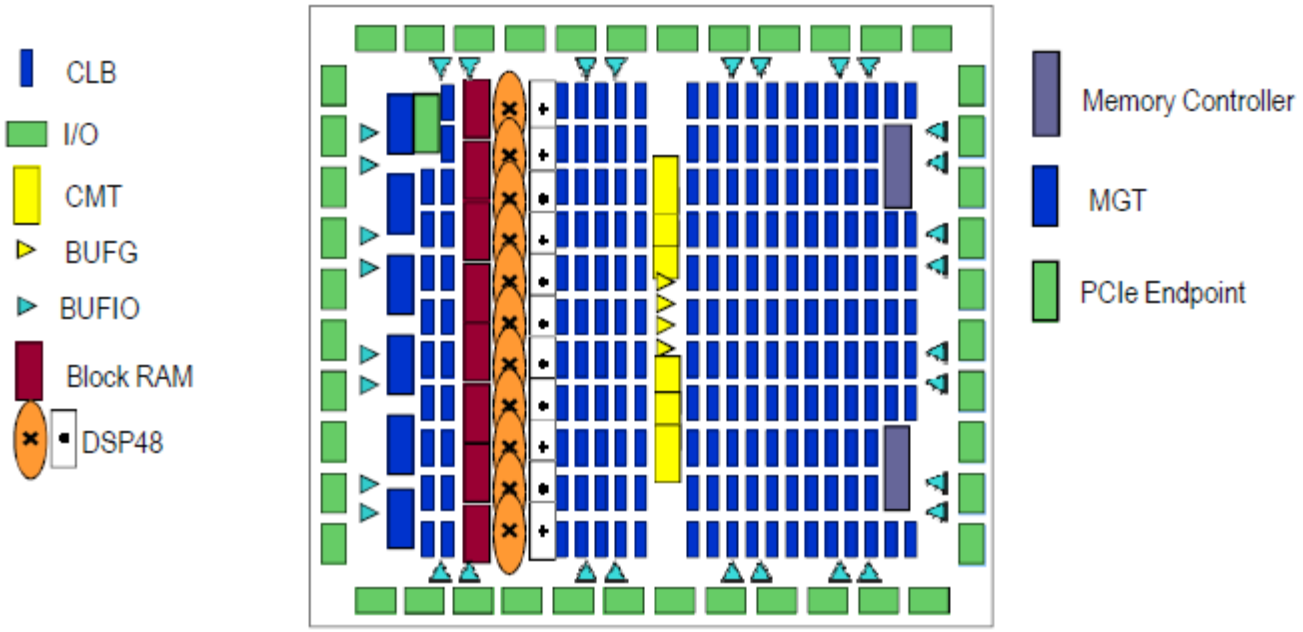


Figure 17.A general overview of the FPGA architecture

2.16 Configuration PROM

The Spartan-6 Tyro Kit has an XCF04S serial configuration Flash PROM to store FPGA configuration data and potentially additional non-volatile data, including Micro Blaze application code.

Table 13.Jumper setting description: XC6SLX9

Jumper Setting	Description
JTAG	The FPGA boots from Platform Flash. No additional data storage is available
PROM	The FPGA boots from Platform Flash, which is permanently enabled. The FPGA can read additional data from Platform Flash.

JTAG OPTION

For most applications, this is the default jumper setting. As shown in

, the Platform Flash is enabled only during configuration when the FPGA's DONE pin is Low. When the DONE pin goes high at the end of configuration, the Platform Flash is disabled and placed in low-power mode.

Table 14.Jumper setting

Jumper Setting	Description
M0 M1  	MODE0- JTAG Programming MODE1- Flash Programming

PROM READ OPTION

The Spartan-6 Tyro Kit includes a 4Mbit Platform Flash configuration PROM. The XC3S400 FPGA on the board only requires slightly less than 1Mbit for configuration data. The remainder of the Platform Flash is available to store other non-volatile data, such as revision codes, serial numbers and coefficients. To allow the FPGA to read from Platform Flash

after configuration, the jumper must be properly positioned as shown in Table 14. When the jumper is in this position, the Platform Flash is always enabled.

JTAG Programming/Debugging Ports

The Spartan-3 FPGA includes a JTAG programming and debugging chain. Additionally, there is JTAG headers for driving the JTAG signals from various supported JTAG download and debugging cables. A PANTECH JTAG3 low-cost parallel to JTAG cable is included as part of the kit and connects to the JTAG header. DB-25 parallel port connector connects to the 6-pin female header connector. The JTAG cable connects directly to the parallel port of a PC and to a standard 6-pin JTAG programming header in the kit that can program a devices that have a JTAG voltage of 1.8v or greater.

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