V850 Series Catalog 2000

32-bit Microcontrollers

NEC

Document No. (U14704EE1V0PF00)

February 2000

Dear NEC V850 Customer:

Welcome to the February 2000 edition of the V85x Series Development Tools Catalog. In this issue, we have included 19 new tools vendors and 47 products. NEC Electronics is continuing to make sure that you are provided with a broad and highly efficient tools environment. Our alliance with many of the most popular vendors has assured you of multiple options for compilers, real-time operating systems, reference boards, and software support, among others.

We know today that time-to-market pressures and “getting it right—the first time” can mean the difference in marketing a competitive product to specification and within ever-shrinking market windows. Our approach is to provide comprehensive solutions: a full range of feature-rich processors, companion chipsets, vertical market expertise, and a seamless development environment to aid your design programs.

Please review the leading-edge tools described in the following sections. Our tools partners have worked hard to anticipate your needs, not just for today but for well into the future, so that the power of the V85x 32-bit RISC family can help you achieve your product specifications and finally market success.

We would appreciate your suggestions as to how we may continue to improve our service to you and that of our tools partners.

Sincerely,

NEC Electronics Europe GmbH
Marketing Europe

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V85x-Series Microcontrollers

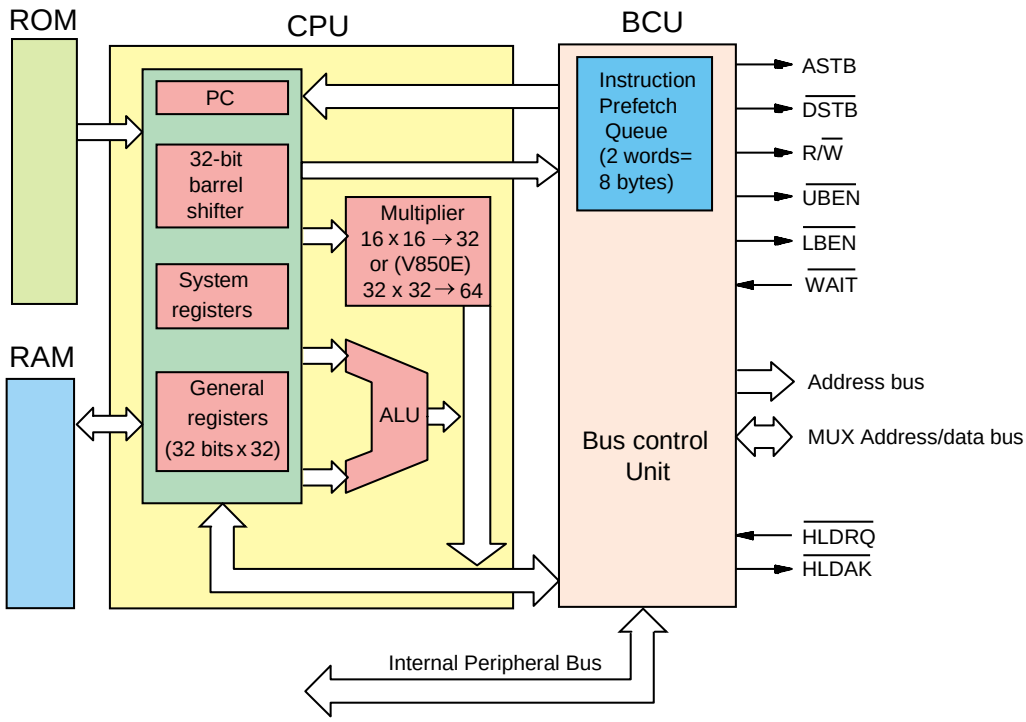
Small is beautiful

32-bit RISC Microcontrollers

V850 is the name of one of our microcontroller families.
These 32-bit RISC controllers are an ideal solution – even in areas where 16-bit CISC controllers are still being employed. 32-bit RISC controllers for the 16-bit CISC applications? You bet.

CPU Block Diagram

Harvard Architecture



Harvard architecture
The Harvard architecture has separate instruction and data paths which are accessed independently. Accessing one of the buses does not limit access to the other. In this way, a high execution speed can be achieved. This architecture is important especially for RISC microcontrollers that basically execute one instruction per clock.

Support of CISC-like instructions
The V850 Series supports CISC-like instructions such as bit manipulation instructions that are supported as standard by microcontrollers intended for embedded control applications. These instructions help enhance the object efficiency and facilitate programming in an assembly language. Moreover, addition instructions that can execute saturated processing, and a high-speed multiplier are also provided so that these can be used in combination for filter operations.

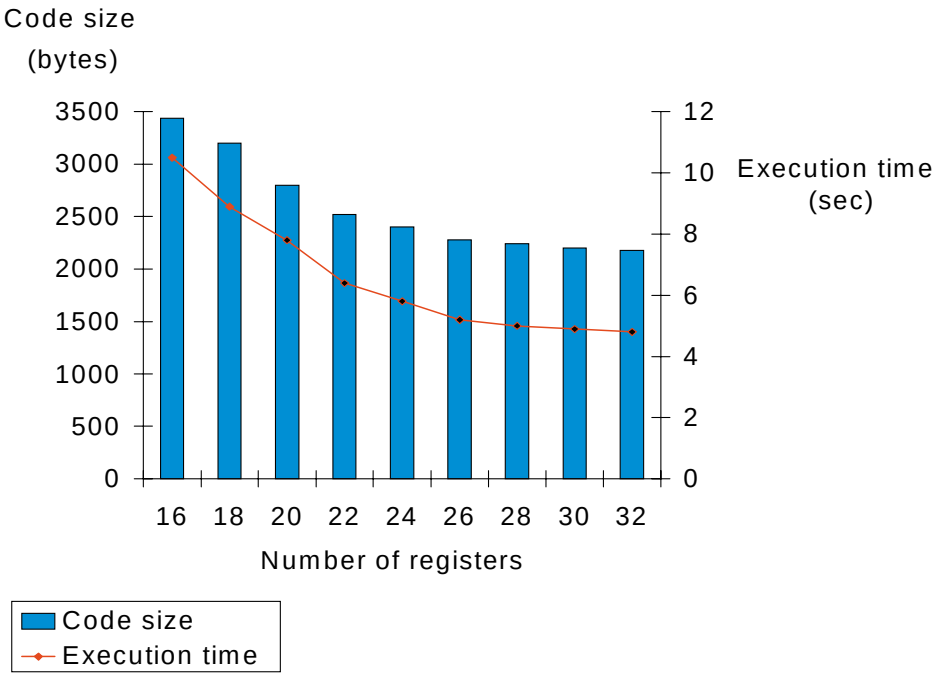
Quick interrupt response time
For applications with real-time requirements, the V850 has a programmable interrupt controller. Registers allow the processing of interrupts within 6-11 clock cycles (V850E). Maskable interrupts can be activated individually with programmable priority levels and external interrupts can be programmed to rising or falling signal edges. To improve software reliability, interrupts can also be generated by software traps or non-defined program codes.

Clock generation for extra-fast circuits
No problem for the V850. With a crystal or ceramic resonator, the user given frequency can be created via an integrated clock generator. Internal PLL decreases the external frequency. That brings down the price of the crystal and reduces EMI.

Static design
Ever more popular: operation at desired frequencies. There is no need for internal refresh. Power consumption is reduced by various modes down to turn off the clock completely.

32 general-purpose registers

The number of general-purpose registers available has a great influence on determining the object efficiency of a RISC-architecture microcontroller. As a result of evaluation by NEC, providing 24 to 26 registers is effective for enhancing the object efficiency (refer to Figure below). The V850 Series microcontrollers have 32 registers. This may be thought of as being excessive. However, these registers can be used as a soft register bank having two register sets when they are used with a C compiler capable of specifying mapping of general-purpose registers.



- Code size optimization and execution speed enhancement
- Example programme: servo control (compiled in C language)

The V850 concept

- High performance, including DSP functionality
- Easy system integration with standard peripherals and on-chip memory
- Working with low supply voltage and low power dissipation
- Simplified engineering through the support of excellent tools

V850 features

- Various memory configurations with on-chip RAM, ROM and Flash
- Hardware multiplier with saturation logic
- Many peripherals
- Software libraries for complex standardised functions
- Optimised instruction set for compact control applications
- Customer specific design and ASIC macros
- Latest CMOS production technology

V850E

Optimised V850 architecture for top performance:

- 7 additional intructions reduce code while maintaining full binary software compatibility
- Higher system performance and clock rates possible up to 100 MHz
- New interface peripheral for connecting different memory types without additional logic
- 32-bit x 32-bit multiplication with 64-bit results

V850S

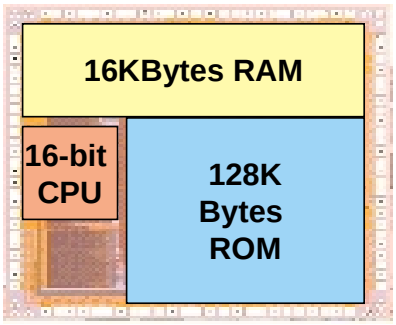
The concept for ultra-low power dissipation:

- Optimisation at limited clock frequency
- 51 mW at 20 MIPS
- Close to 400 MIPS/ Watt
- Low supply voltage, wide voltage range

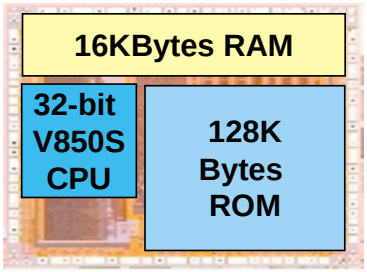
Small enough?

Using 32-bit cores instead of 16-bit can reduce Chipsize

20MIPS @ 40MHZ



20MIPS @17MHZ



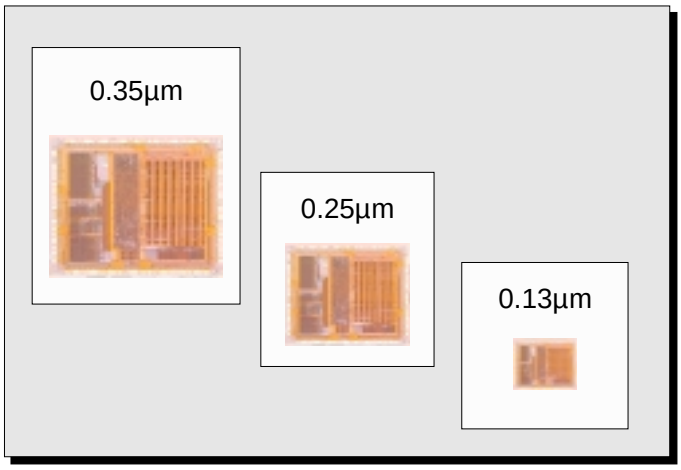
- On-chip memory (128KB and more) takes much more silicon space than the CPU core
- V850 is optimised for low clock frequencies which allows the use of very compact memory cells
- Finer geometries make core size differences insignificant
- 32-bit controller are likely to be the first candidates for newer process technologies
- There is no cost adder for switching from 8-bit (78K) to 32-bit (V850)

Because the RISC technology in the V850 line lets the processor core be simplified, making it smaller and more cost-effective than the most 16-bit cores.

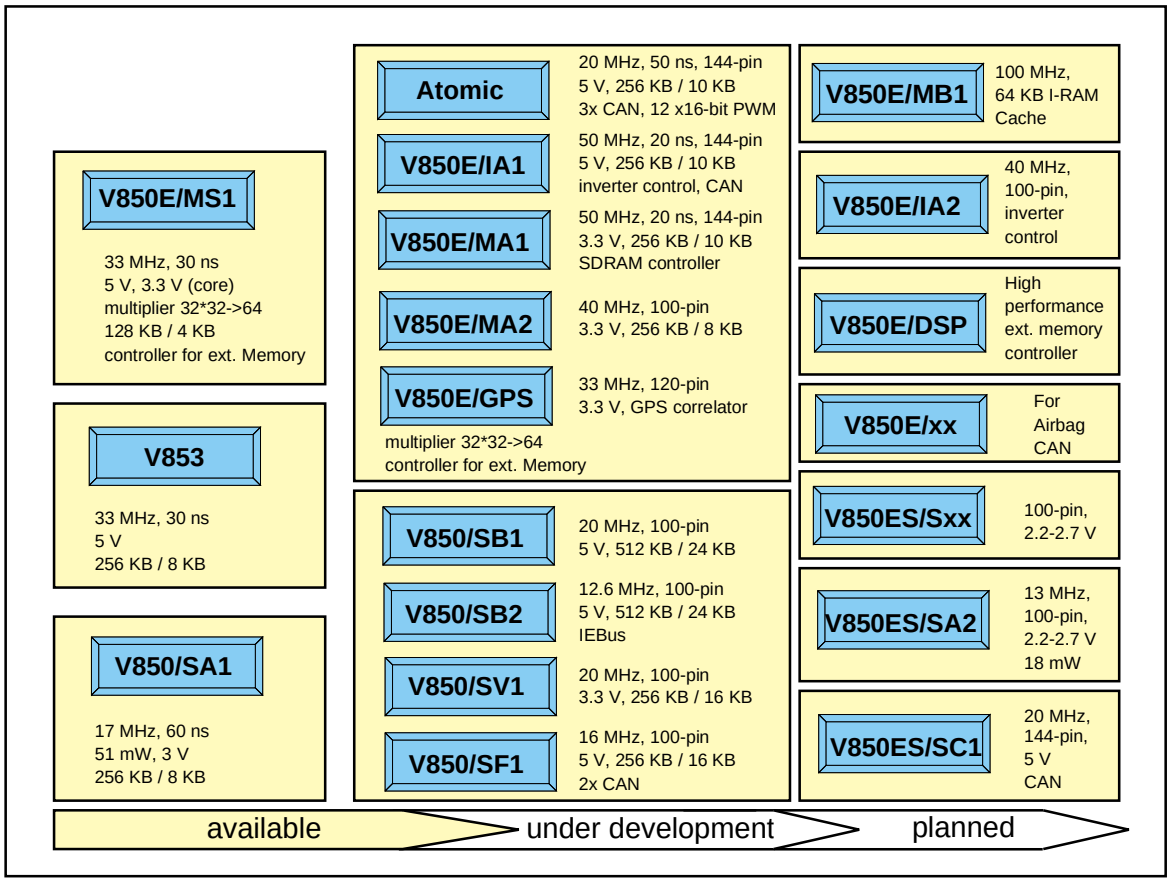
For instance, the 0,25 µm technology already in use has a core that's a tiny 1.3 mm^2. The V850 line has incorporated those instructions that, thorough investigation tells us, are used most often.

These are then processed by the hardware at extremely high speeds. Usually in one clock cycle. 32-bit V850 microcontrollers don't cause any software overhead, either. So differences in program size to 16-bit controllers are no cause for concern.

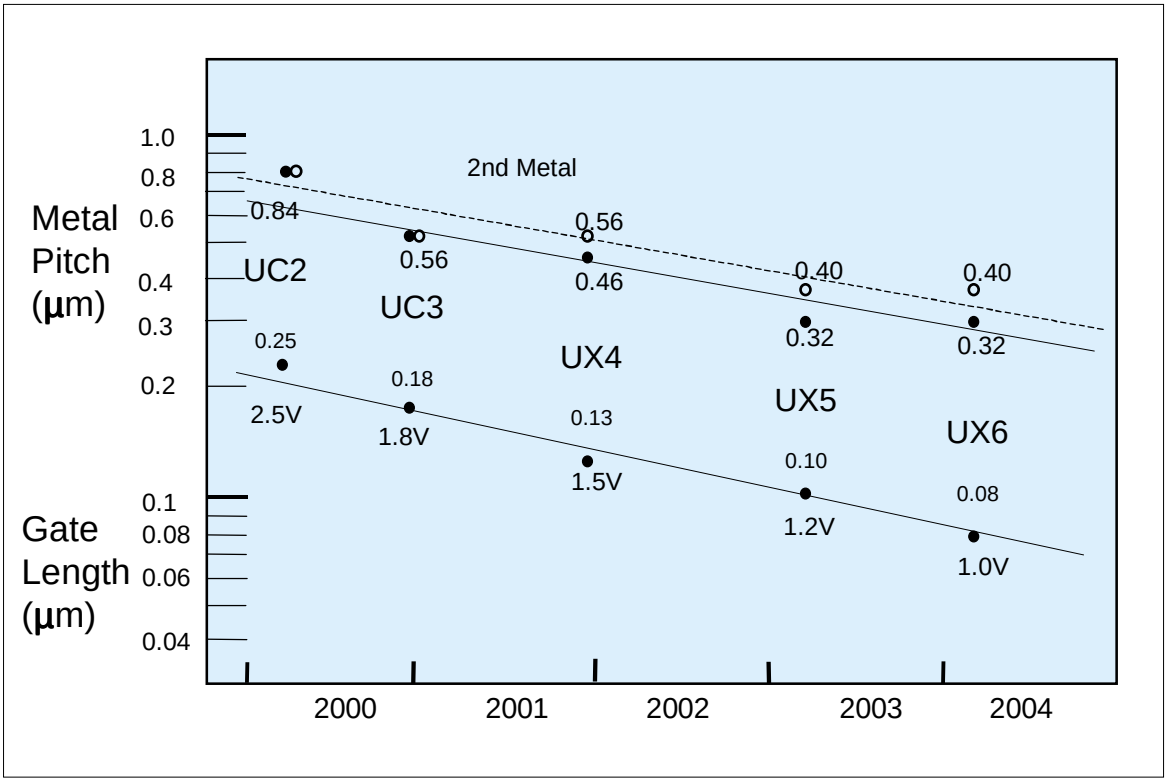
Impact of design process on chip size



V850 Line-up



Process Technology Roadmap



V853 32-bit RISC Microcontroller

Description

The single-chip V853 microcontroller is a member of NEC's 32-bit RISC V850 family. It integrates CPU, ROM, RAM and peripheral functions on chip. The internal bus is 32 bits wide, the external bus 16 bits wide. Controller memory options are listed in Table 1.

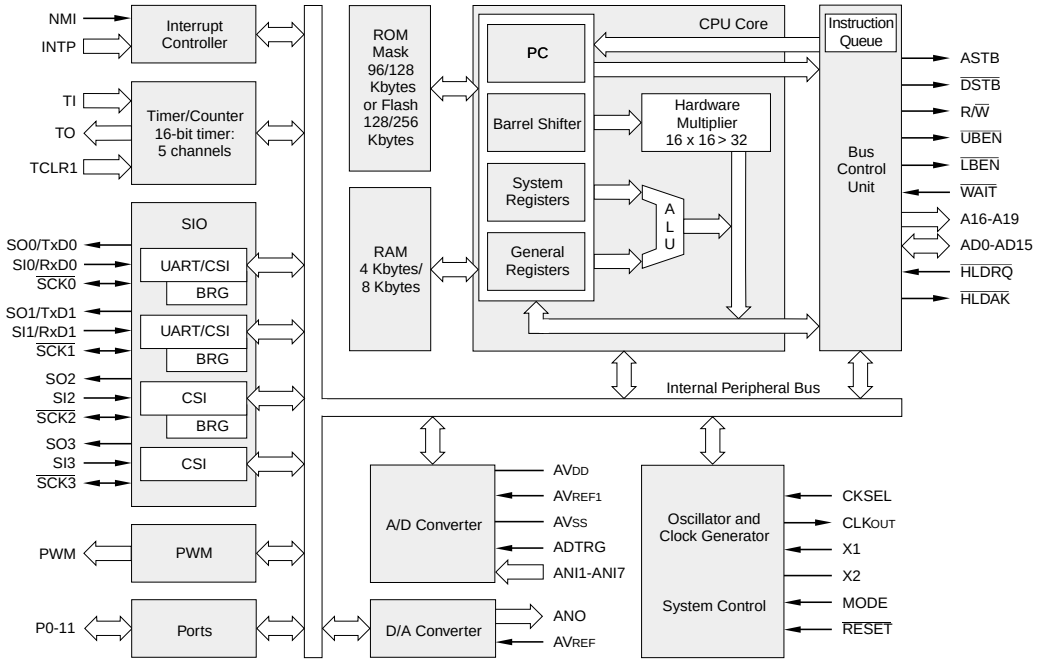
Applications

Like other V850 series controllers, the V853 device is used for real-time control applications, such as servo motor control in computer peripherals and machine tools, for engine management control, consumer electronics and multimedia. Flash memory, a variety of serial communication channels and AD/DA converters make it the perfect choice for compact communication terminals and complete control systems. Typical benefits of Flash memory are individually programmed devices in the final production process and field upgradability. With their low power consumption and power-saving modes, V853 devices are also ideal for portable applications.

Features

- Small 32-bit RISC CPU core
- 30 ns minimum instruction execution time (33 MHz max. clock)
- 16-Mbyte linear address space
- 1-Mbyte external address space
- 32 general-purpose registers
- 74 instructions optimized for embedded control
- DSP functionality with 16-bit multiplication and saturation logic in a single clock cycle
- Up to 8 Kbytes internal RAM
- Interrupt controller
- Real-time pulse unit/timers
- Serial interface with baud rate generator
- A/D and D/A converters
- PWM
- Clock generator
- Power save functions
- Mask ROM, Flash versions
- 100-pin LQFP package

Block Diagram V853



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Max. freq. (MHz)	ROM (Kbytes)	Flash (Kbytes)	RAM (Kbytes)
µPD703004AGC-25	25	96	-	4
µPD703004AGC-33	33	96	-	4
µPD703003AGC-25	25	128	-	4
µPD703003AGC-33	33	128	-	4
µPD70F3004AGC-25	25	-	128	4
µPD70F3004AGC-33	33	-	128	4
µPD70F30025AGC-25	25	-	256	8
µPD70F30025AGC-33	33	-	256	8
µPD7030025AGC-25	25	256	-	8
µPD7030025AGC-33	33	256	-	8

Documentation

Doc Number	Devices	Type
U13919EE2V0CD00	NEC Micro-Components	CD-ROM
U10243EJ6V0UM00	V850	Architecture Manual
U10913EJ5V0UM00	V853	User's Manual
U13188EJ2V1DS00	V853 Mask	Data Sheet
U13189EJ2V0DS00	V853 Flash	Data Sheet

Tools

Order Number	Devices	Description	Type
V850-IAR-Toolset	V850	ICE + C Compiler	Hardware & Software
IE-703003-MC-EM1	V853	Emulation Board	Hardware
CPDW95/NT-CDR-V800	V850	C/C++ Compiler (GHS)	Optional Software
FA100-GC	100-pin LQFP	Programming Adapter	Hardware
SC100SDN	V850	Emulation Probe Extension	Optional Hardware
StartWARE-GHS-V850/SA1	V850	Starter Kit	Hardware & Software
FlashMASTER	V850	Programmer	Hardware

For further information on NEC's V850 family or other NEC products visit our European website at **www.nec.de**

V850/SA1 32-bit RISC Microcontrollers

Description

The single-chip V850/SA1 microcontroller - a member of NEC's 32-bit RISC V850 family - is optimized for very low power consumption and high performance. The V850/SA1, with its peripherals, consumes only 30 mW at 17 MHz, giving a performance/power ratio of 700 Mips/W. Together with power saving modes, this makes the V850/SA1 an excellent choice for portable applications. The 16-bit external bus simplifies interfacing.

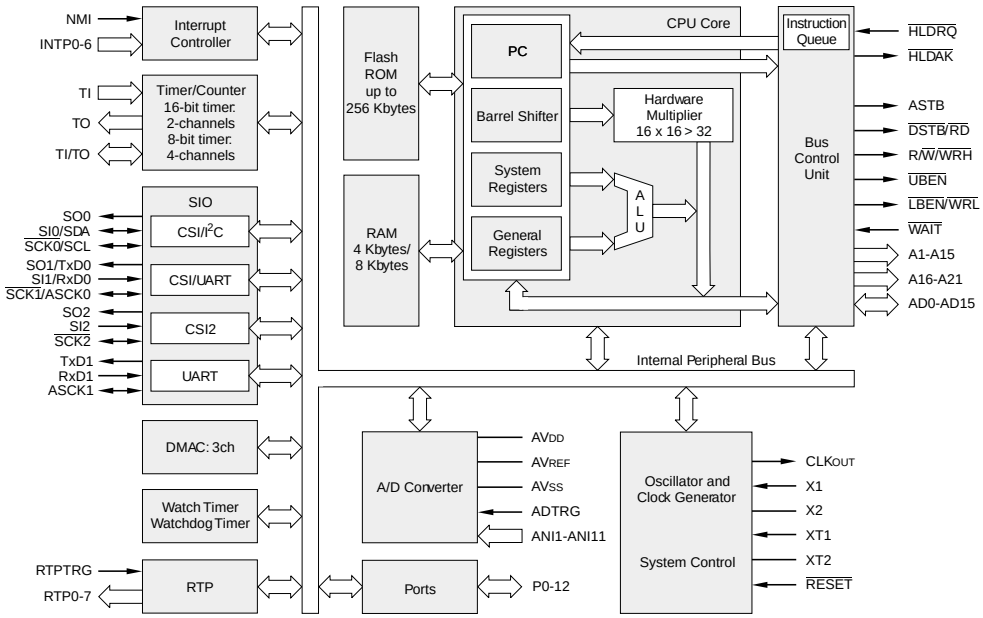
Applications

V850/SA1 devices are used primarily for applications in portable and battery-powered control, eg, communication terminals, test and measurement equipment, medical instruments.

Features

- 32-bit RISC CPU core
- Optimized for very low power consumption:
  30 mW at 17 MHz and 3 V (ROM)
  45 mW at 17 MHz and 3 V (Flash)
- 16-Mbyte linear address space, 4-Mbyte external access
- 59 ns minimum instruction execution time (at 17 MHz)
- 32 general-purpose registers
- Mask ROM version:
  up to 256 Kbytes ROM, 8 Kbytes RAM
- Flash ROM version:
  256 Kbytes ROM, 8 Kbytes RAM
- DSP functionality with 16-bit multiplication and saturation logic in a single clock cycle
- External 16-bit bus
- Real-time pulse unit (timers)
- Watch timer and watchdog timer
- Serial interface with baud rate generators
- I^2C option
- Peripheral set as 78K/4 16-bit controller family
- Clock generator with subclock operation
- Power save functions
- 100-pin LQFP and 121-pin FBGA packages

Block Diagram V850/SA1



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	I²C Bus	ROM (Kbytes)	Flash (Kbytes)	RAM (Kbytes)
µPD703014A	No	64	-	16
µPD703014AY	Yes	64	-	4
µPD703015A	No	128	-	4
µPD703015AY	Yes	128	-	4
µPD703017A	No	256	-	8
µPD703017AY	Yes	256	-	8
µPD70F3017A	No	-	256	8
µPD70F3017AY	Yes	-	256	8

Device orders must specify the package code: GC (100-pin LQFP), S1 (121-pin FBGA)

Documentation

Doc Number	Devices	Type
U13919EE2V0CD00	NEC Micro-Components	CD-ROM
U10243EJ6V0UM00	V850	Architecture Manual
U12768EJ2V0UM00*	V850/SA1	User's Manual
U13829EJ1V0DS00	µPD703015	Data Sheet
SUD-T-3607*	V850/SA1	Electrical Specification

*Preliminary Document

Tools

Order Number	Devices	Description	Type
V850-IAR-Toolset	V850	ICE + C Compiler	Hardware & Software
IE-703017-MC-EM1	V850SA1	Emulation Board	Hardware
CPDW95/NT-CDR-V800	V850	C/C++ Compiler (GHS)	Optional Software
FA100-GC	V850	Programming Adapter	Hardware
SC100SDN	V850	Emulation Probe Extension	Optional Hardware
StartWARE-GHS-V850/SA1	V850S	Starter Kit	Hardware & Software
FlashMASTER	V850	Programmer	Hardware

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V850/SB1 32-bit RISC Microcontrollers

Description

The single-chip V850/SB1 microcontroller - a member of NEC's 32-bit RISC V850 family - is optimized for very low power consumption and high performance. Based on the V850/SA1, the V850/SB1 has additional features, including 3-5 V I/O interface support and ROM correction. An optimized CPU together with power saving modes makes the V850/SB1 an excellent choice for portable applications. The 16-bit external bus simplifies interfacing.

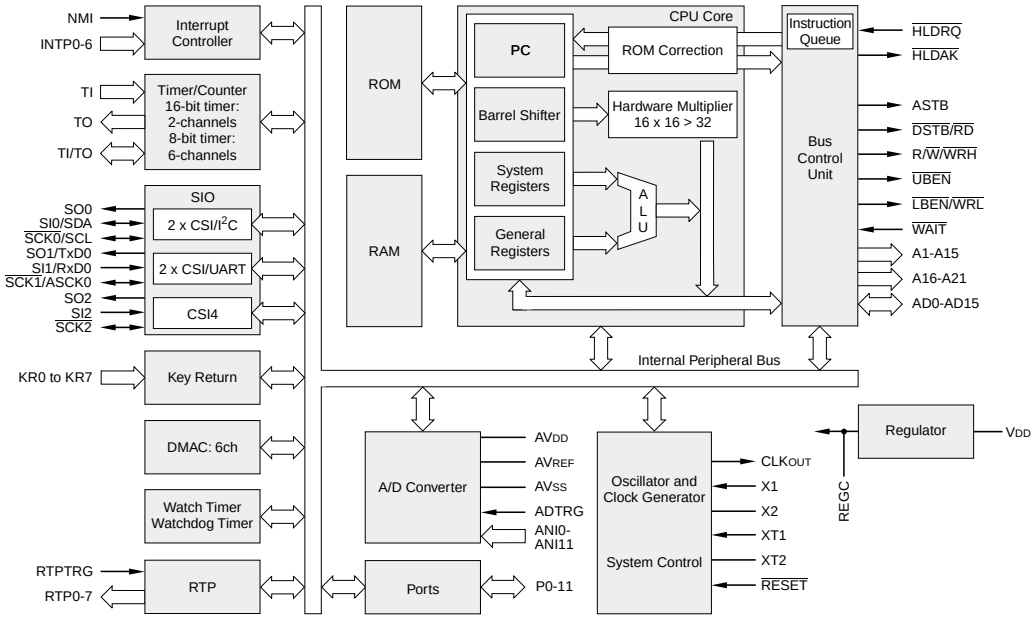
Applications

V850/SB1 devices are used primarily for applications in portable and battery-powered control, eg, communication terminals, test and measurement equipment, medical instruments. An excellent cost/performance ratio makes them an ideal choice for classical 16-bit applications.

Features

- 32-bit RISC CPU core
- Optimized for very low power consumption
- 50 ns minimum instruction execution time (at 20 MHz)
- 16-Mbyte linear address space, 4-Mbyte external access
- 32 general-purpose registers
- ROM: up to 512 Kbytes ROM or Flash
- ROM correction
- RAM: up to 24 Kbytes
- DSP functionality with 16-bit multiplication and saturation logic
- External 16-bit bus
- Timer: 8 channels, suitable for PWM output
- Serial interface with baud rate generator
- I^2C option
- 12-channel A/D converters with 10-bit resolution
- Key return function
- Peripheral set similar to 16-bit controller
- Clock generator with subclock operation
- Power save functions
- Voltage regulator: 5 V input → internal 3.3 V
- 100-pin LQFP package

Block Diagram V850/SB1



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Max. freq. (MHz)	ROM (Kbytes)	Flash (Kbytes)	RAM (Kbytes)
µPD703033A	20	256	-	16
µPD703033AY	20	256	-	16
µPD70F3033A	20	-	256	16
µPD70F3033AY	20	-	256	16
µPD703032A	20	512	-	24
µPD703032AY	20	512	-	24
µPD703030A	20	384	-	20
µPD703030AY	20	384	-	20
µPD70F3032A	20	-	512	24
µPD70F3032AY	20	-	512	24

Documentation

Doc Number	Devices	Type
U13919EE2V0CD00	NEC Micro-Components	CD-ROM
U10243EJ6V0UM00	V850	Architecture Manual
U13568EJ1V0UM00*	V850/SB1	User's Manual

*Preliminary Document

Tools

Order Number	Devices	Description	Type
V850-IAR-Toolset	V850	ICE + C Compiler	Hardware & Software
IE-703037-MC-EM1	V850	Emulation Board	Hardware
CPDW95/NT-CDR-V800	V850	C/C++ Compiler (GHS)	Optional Software
FA100-GC	V850GC	Programming Adapter	Hardware
SC100SDN	V850	Emulation Probe Extension	Optional Hardware
NEXB-100SD/RB	100-pin QFP	Adapter	Hardware
StartWARE-GHS-V850/SA1	V850S	Starter Kit	Hardware & Software
FlashMASTER	V850	Programmer	Hardware
FA100-GF	V850GF	Programming Adapter	Hardware

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V850/SF1 32-bit RISC Microcontrollers

Description

The V850/SF1 microcontroller subseries is a member of NEC's successful V850 family of 32-bit single-chip microcontrollers. It combines a high performance RISC CPU with a peripheral mix (including CAN Interfaces) optimized for automotive applications. A large choice of devices with different on-chip memory configurations is available allowing to use V850/SF1 as a platform for a variety of end products. A 16-bit external bus simplifies interfacing.

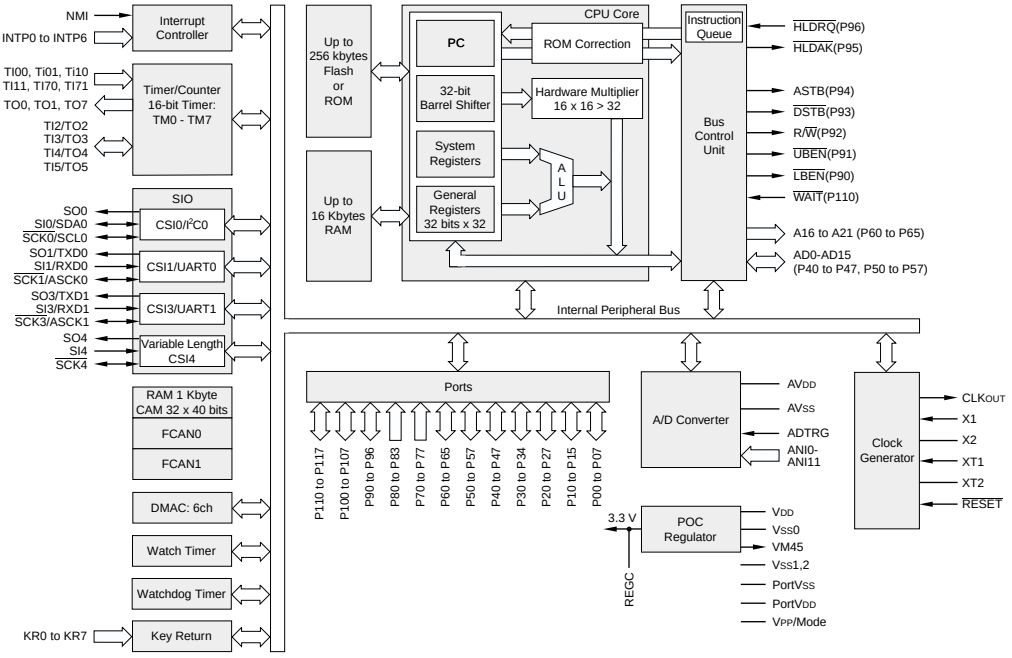
Applications

V850/SF1 devices are used in demanding automotive applications that require single or double CAN, up to 256 Kbytes ROM or Flash and high processing performance at very low EMI. Examples are car audio systems, dashboards, information terminals. An excellent cost/performance ratio makes V850SF1 devices the ideal choice for classical 16-bit applications.

Features

- 32-bit RISC CPU core
- Optimized for very low power consumption
- 62,5 ns minimum instruction execution time (at 16 MHz)
- 16-Mbyte linear address space, 4-Mbyte external access
- 32 general-purpose registers
- ROM: up to 256 Kbytes Mask or Flash
- ROM correction
- RAM: up to 16 Kbytes
- DSP functionality with 16-bit multiplication and saturation logic
- External 16-bit bus
- Timer: 8 channels, suitable for PWM output
- Serial interface with baud rate generator
- I^2C option
- 12-channel A/D converters with 10-bit resolution
- Key return function
- Peripheral set similar to 16-bit controller
- Clock generator with subclock operation
- Power save functions
- Voltage regulator: 5 V input → internal 3.3 V
- 100-pin LQFP and 100-pin QFP packages

Block Diagram V850/SF1



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Max. freq. (MHz)	Interfaces	ROM (Kbytes)	Flash (Kbytes)	RAM (Kbytes)
µPD703076Y	16	1ch CAN	128	-	10
µPD703077Y	16	2ch CAN	128	-	10
µPD703078Y	16	1ch CAN	256	-	16
µPD703079Y	16	2ch CAN	256	-	16
µPD70F3077Y	16	2ch CAN	-	128	10
µPD703077Y	16	2ch CAN	-	256	16

Device orders must specify the package code GC (100-pin LQFP), GF (100-pin QFP)

Documentation

Doc Number	Devices	Type
U13919EE2V0CD00	NEC Micro-Components	CD-ROM
U10243EJ6V0UM00	V850	Architecture Manual
U14665EJ1V0UM00*	V850/SF1	User's Manual

*Preliminary Document

Tools

Order Number	Devices	Description	Type
V850-IAR-Toolset	V850	ICE + C Compiler	Hardware & Software
IE-703079-MC-EM1	V850SF1	Emulation Board	Hardware
CPDW95/NT-CDR-V800	V850	C/C++ Compiler (GHS)	Optional Software
FA100-GC	V850GC	Programming Adapter	Hardware
SC100SDN	V850	Emulation Probe Extension	Optional Hardware
StartWARE-GHS-V850/SA1	V850S	Starter Kit	Hardware & Software
FlashMASTER	V850	Programmer	Hardware

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V850E/MS1 32-bit RISC Microcontrollers

Description

The single-chip V850E/MS1 microcontroller is a member of NEC's 32-bit RISC V850 family. The device is optimized for high speed and high performance. New instructions make for more compact code size while maintaining backward compatibility to V850 standard products.

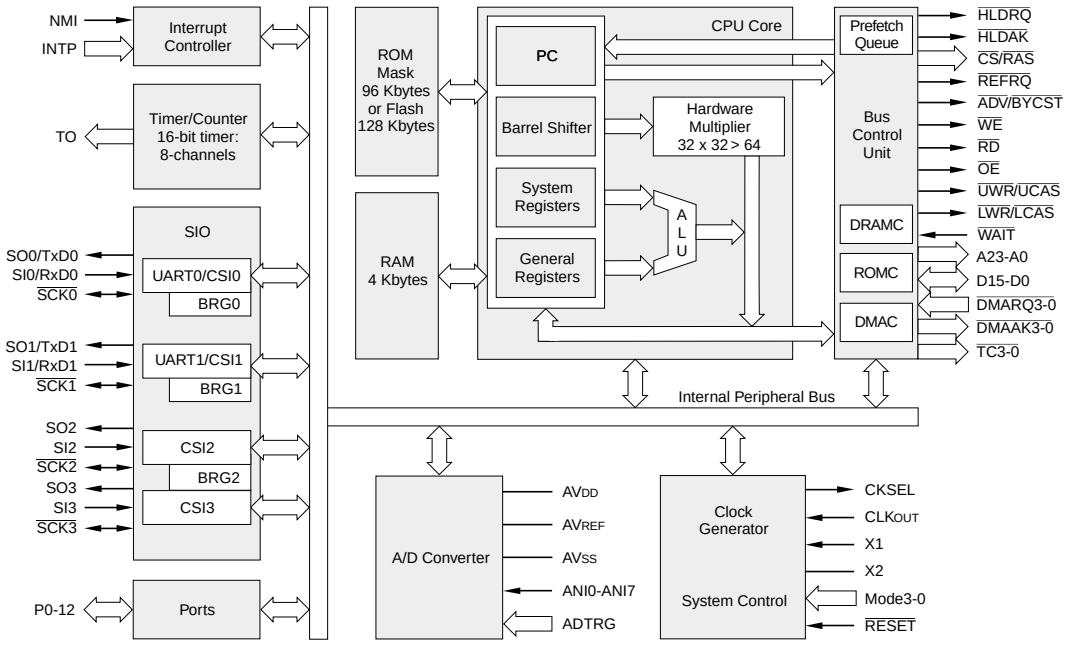
Applications

V850E/MS1 devices are used primarily for embedded multimedia consumer applications, such as communication terminals, printers and other computer peripherals. Other high-end embedded real-time control applications, such as servo motor control in computer peripherals and machine tools, and engine management control, are better served by the V850E. With their low power consumption and power-saving modes, V850E/MS1 devices are also ideal for portable applications.

Features

- Enhanced 32-bit RISC CPU core with additional instructions
- 64-Mbyte linear address space
- 32-Mbyte external address space
- 25 ns minimum instruction execution time (40 MHz max. clock)
- 32 general-purpose registers
- 4 Kbytes internal RAM
- ROMless, Mask ROM (96/128 Kbytes), Flash EPROM (128 Kbytes)
- DSP functionality with 32-bit multiplication and saturation logic in a single clock cycle
- Bus controller including memory controller
- DMA controller
- Real-time pulse unit/timers
- Serial interface with baud rate generator
- Clock generator with PLL
- Power save functions
- 144-pin QFP and 157-pin FPBGA packages

Block Diagram V850E/MS1



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Max. freq. (MHz)	Voltage core/peripherals	ROM (Kbytes)	Flash (Kbytes)	RAM (Kbytes)
µPD703100	40	3.3 V/5 V	-	-	4
µPD703100A	40	3.3 V/3.3 V	-	-	4
µPD703101	33	3.3 V/5 V	96	-	4
µPD703101A	33	3.3 V/3.3 V	96	-	4
µPD703102	33	3.3 V/5 V	128	-	4
µPD703102A	33	3.3 V/3.3 V	128	-	4
µPD70F3102	33	3.3 V/5 V	-	128	4
µPD70F3102A	33	3.3 V/3.3 V	-	128	4

Device orders must specify the package code GJ (144-pin FQFP), F1 (157-pin FPBGA)

Documentation

Doc Number	Devices	Type
U13919EE2V0CD00	NEC Micro-Components	CD-ROM
U12197EJ3V0UM00	V850E	Architecture Manual
U12688EJ3V0UM00	V850E/MS1	User's Manual
U14168EJ2V0DS00	µPD703100A, 703101A, 703102A, 70F3102A	Data Sheet
U13995EJ1V0DS00	µPD703100, 703101, 703102, 70F3102	Data Sheet

Tools

Order Number	Devices	Description	Type
IE-703102-MC-EM1 (-A)	V850E/MS1	Emulation Board	Hardware
CPDW95/NT-CDR-V800	V850	C/C++ Compiler (GHS)	Optional Software
FA144-GJ	V850E/MS1	Programming Adapter	Hardware
SC144SDN	V850E/MS1	Emulation Probe Extension	Optional Hardware
FlashMASTER	V850	Programmer	Hardware
IE-703102-MC	V850E/MS1	Emulator	Hardware
EWEMUL-N9X/NT-CR-85X	V850	C Compiler	Software
IE-70000PCI-IF-A	V850	PC-Interface Card	Hardware

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Atomic 32-bit RISC Microcontrollers

Description

Devices in the V850 RISC family match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable with standard 16-bit CPUs.
The 'Atomic' is a single-chip microcontroller in NEC's 32-bit RISC V850 family, designed to meet the requirements of tomorrow's automotive and industrial applications. It is based on NEC's enhanced V850E CPU core. The 'Atomic' combines CPU, ROM and RAM with powerful peripherals and 3 Full-CAN interfaces in one chip.

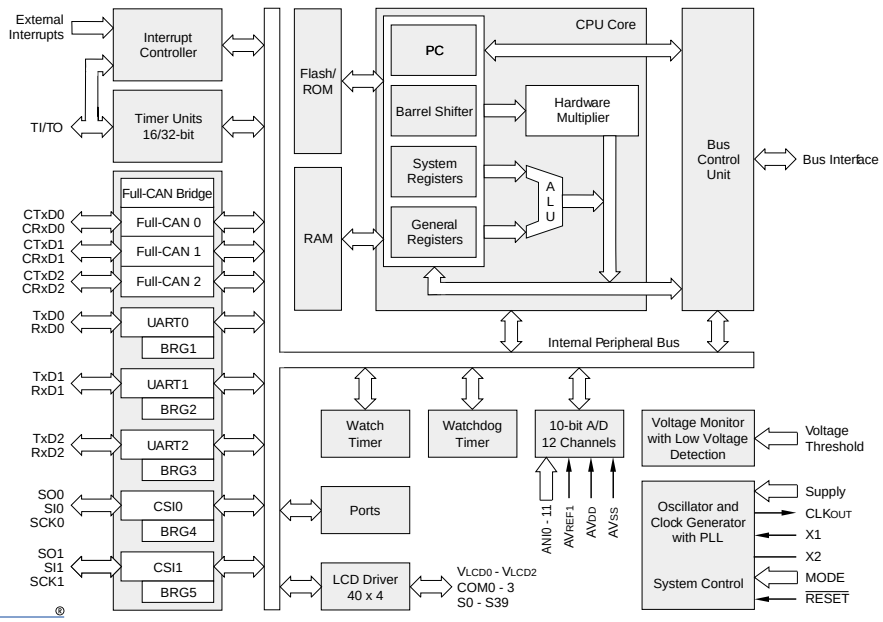
Applications

Basically intended for automotive applications, like body control or dashboard, the V850 'Atomic' is also an excellent choice for other applications where a combination of high performance, sophisticated peripheral functions and CAN network support is required. The V850's integrated power-saving modes allow power consumption to be managed effectively under varying conditions.

Features

- V850E CPU core,
  32-bit RISC Harvard Architecture
- 20 MHz @ 5 V, -40 to +85°C
- Memory options:
  256 Kbytes Flash/8 Kbytes RAM
  256 Kbytes ROM/8 Kbytes RAM
  128 Kbytes Flash/4 Kbytes RAM
- DSP functionality:
  hardware multiplier (32 x 32 => 64-bit)
  saturation logic, barrel shifter
- A/D converter: 12-channel 10-bit resolution
- 40 x 4 segment LCD controller/driver
- Interrupt controller
- Timer unit:
  16/32-bit multi-purpose timer x 3
  16-bit OS timer x 2
  watchdog timer x 1
  watch timer x 1
- Serial interfaces: 3 x UART, 2 x CSI
- Up to 3 Full-CAN modules
- FCAN bridge/gateway
- Clock generator with PLL
- External bus interface
- Power saving functions
- 144-pin QFP packages

Block Diagram Atomic



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Internal RAM (Kbytes)	Internal ROM (Kbytes)
µPD703121GJ-UEN	4	128 Mask
µPD703123GJ-UEN	8	256 Mask
µPD70F3123GJ-UEN	8	256 Flash

Documentation

Doc Number	Device	Type
U12197EJ2V0UM00	V850E Family	Architecture Manual

Software Tools

Order Number	Description	Platform
CPDW9X/NT-CDR-V85X	C/C++Compiler and Tools[1]	Windows 9X/NT
CPDHP-CDR-V85X	C/C++Compiler and Tools[1]	HP
CPDSUN/SOLARIS-CDR-V800	C/C++Compiler and Tools[2]	SUN/SOLARIS
EWEMUL-W9X/NT-CDR-V85X	C/C++Compiler and Tools[3]	Windows 9X/NT
EWSIM-W9X/NT-CDR-V85X	C/C++Compiler and Tools[4]	Windows 9X/NT
CSEMUL-W9X/NT-CDR-V85X	C/C++Compiler and Tools[5]	Windows 9X/NT

[1] Green Hills tools MULTI embedded development kit including ICE interface
[2] Green Hills tools MULTI embedded development kit
[3] IAR tools: Embedded Workbench for Emulator
[4] IAR tools: Embedded Workbench for Simulator
[5] IAR tools: Add-on to 4 - allows debugging on Emulator in addition to Simulator

A tool set (V850E-IAR-Toolset) is available comprising EWEMUL-W9X/NT-CDR-V85X plus in-circuit emulator hardware except emulation board

Hardware Tools

Order Number	Description
IE-V850E-MC	Emulator
EB-POWERFW7301/05	Power Supply
IE-70000-PCI-IF	PC Interface Card
IE-7000-CD-IF-A	PCMCIA Adapter
IE-70000-MC-SV3	Ethernet Adapter
SC144SDN	Emulation Probe
IE703123-MC-EM1	Emulation Board
FA-144GJ-UEN	Flash Programming Adapter

For further information on NEC's V850 CAN family or other NEC products visit our European website at **www.nec.de**

Compilers/Debuggers/Linkers

Nucleus DBUG+ Multitasking Debugger

Features

- Displays task information
- Displays queue information
- Displays resource information
- Displays event group information
- Displays memory partition information
- Modify/display memory capability
- Invoke all Nucleus PLUS services from command line
- Documented source code provided
- Integrated with popular source debuggers

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

Nucleus DBUG+ was developed to assist users of Nucleus PLUS in debugging their multitasking applications. It installs as a task in any Nucleus PLUS system and provides a number of features not normally available within traditional debugging environments.

Because Nucleus DBUG+ is installed as a task, it can freely interact with the rest of the tasking environment. Additionally, tasking information can be viewed in both overview and detailed form. All user interaction with Nucleus DBUG+ is performed through a command line prompt.

The user invokes Nucleus DBUG+ by either entering a status command or invoking Nucleus PLUS services by entering the C interface calls. Status commands have optional parameters which can indicate the specifics associated with the status (e.g., ts 1 -- displays status of task number 1). C interface calls are entered and the user is prompted for the appropriate parameters.

As well as being delivered with complete source code and without royalties, Nucleus PLUS is provided with six months free technical support. This includes phone, fax, email and new releases. For more information, contact Accelerated Technology today.

Accelerated Technology
INCORPORATED

Nucleus MNT Windows NT-based Prototyping Environment

Features

- Executes as a native Windows NT™ or Windows 95™ application
- Designed and developed with Microsoft's Visual C++™ tool set
- PC hosted development and run-time environments
- Prototype most C code that will be used in target system
- Provided with a pre-built project file

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

Nucleus MNT utilizes three modules ported to the Windows NT (or Windows 95) threads environment to perform initialization, scheduling, and timer management functions. The initialization module sets up interrupt vectors for the timer and the terminal interface. The scheduling module employs the Windows thread model to manage the switching of tasks, while the timer module processes a timer tick to facilitate the Nucleus PLUS task sleep, time-slicing, time-out, and timer-thread capabilities.

Development and Debugging:

Nucleus MNT was designed and developed to work with Microsoft's Visual C++ tool set. The complete Microsoft Visual C++ Integrated Development Environment is available, including the editor, make/project capabilities, compiler, librarian, assembler, linker, and debugger.

By using the project file supplied with Nucleus MNT, you can be up and running almost immediately. The release files shipped with Nucleus MNT are loaded into a directory. You add the project to your Microsoft Visual C++ environment and the "Build" menu selection is invoked to produce a Windows NT console application. The Executable contains a demonstration program that exercises almost all Nucleus PLUS capabilities. You can modify this program or replace it with tasks you create when you begin development of your project.

Because Nucleus MNT and the programs developed with it are true Windows NT applications, they can be debugged using the standard Microsoft Visual C++ debugger. Other debugging aids supplied with Microsoft Visual C++ (e.g., Spy) also can be used in the debugging process.

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Nucleus UDB
Portable Source Level Debugger

Features

- Automatic tracing feature
- Kernel aware debugging
- Configurable display windows for source, memory, variables, registers, etc
- Intuitive button bar interface provides a quick learning curve
- Complex breakpoints
- Console window capture-to-file capability
- Universal file viewer
- Stopwatch for timing functionality
- Improved source file tracking
- Advanced Dynamic Data Exchange
- Advanced DLL interface

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

The price/performance ratios among microprocessors are constantly changing. Processors appropriate for today's projects may not be suitable for tomorrow's application. For the embedded systems developer, this often means readjusting to a new set of development tools. To relieve some of the burden and speed development time, Nucleus UDB offers a consistence interface across various processor platforms. This enables developers to quickly adapt to new challenges and meet the demands of changing applications.

Nucleus UDB was designed from the ground up to take advantage of the facilities contained within the Windows operating system. Nucleus UDB offers an intuitive button driven interface, as well as an event driven sequencer system. In addition, UDB provides both task specific and general breakpoint capabilities to help accelerate embedded system development. Combined, these features offer faster performance, as well as the ability to run other applications while a debugging session is active.

Source Level Debugging:
Nucleus UDB is a powerful, GUI-based source-level debugger for embedded applications. Its three component configurations include the debugger front-end, host communications module, and target monitor. These components combine for a powerful and portable debugging environment. Since the front end is standard across all target CPU platforms, developers need learn only one debugging environment.

Accelerated Technology
INCORPORATED

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CodeTEST® Embedded Software Test and Analysis Tools

A Member of the CodeOPTIX™ Family of Embedded Software Visibility Tools

Features

- ◆ Performance Analysis
- Measures function and task execution times
- Counts call-pair linkages to identify thrashing
- Non-sampled measurements of 32,000 functions at one time
- ◆ Coverage Analysis
- Displays coverage at program, function, or source levels
- Plots coverage over time
- Completely interactive measurements simplify test creation and refinement

- ◆ Memory Allocation Analysis
- Dynamic display shows memory leaks in progress before the system crashes
- Pinpoints memory allocation and free errors to offending source line
- Measures true worse case allocation

- ◆ Trace Analysis
- Traces embedded programs at source, control-flow, or high level
- Deep trace captures over 100 thousand source lines of execution
- Powerful triggering and trace display options zero in on problems
- Designed for software engineers

NEC CPUs Supported

Call for supported processors

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

Designed especially for embedded developers, the CodeOPTIX family of test and analysis tools includes three NEW CodeTEST products: CodeTEST Native™, CodeTEST Software-In-Circuit™, and CodeTEST Hardware-In-Circuit™. Each represents a different phase in the embedded software development lifecycle: development, debugging, and testing.

CodeTEST Visibility Modules

Trace Analysis provides an unmatched depth of software execution trace, in three levels of detail, for processors with or without internal caches.

Performance Analysis boosts productivity by providing accurate visibility of code performance, making verification and performance problem area identification straightforward.

Memory Analysis saves time and money by proactively watching the memory usage of your application, often revealing memory leaks and other memory errors in embedded code.

Coverage Analysis improves product quality through identifying high-risk areas of code by showing exactly what functions, blocks, or statements have, or have not been executed.

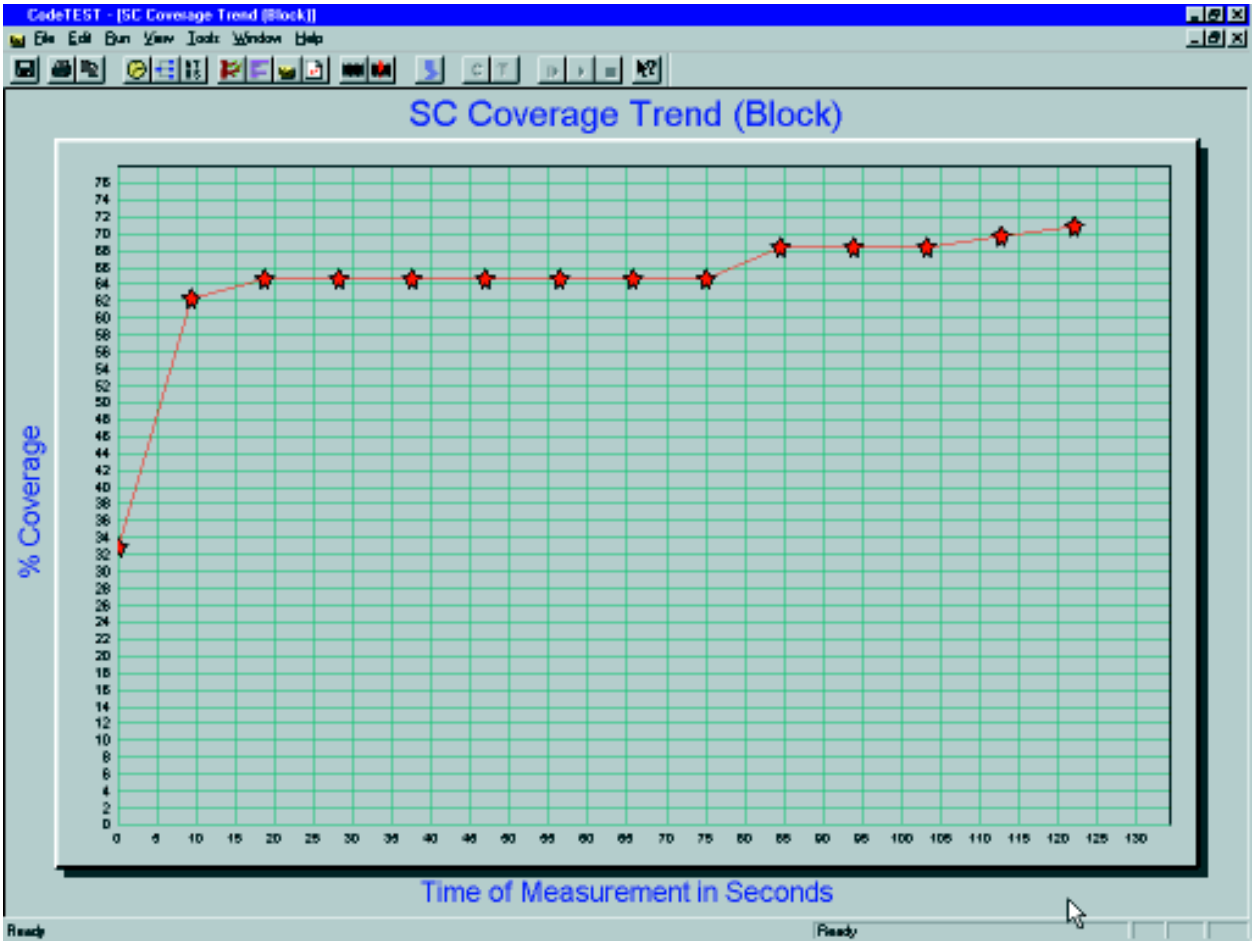
Advanced Coverage Tools (ACT) qualify for the highest of regulated test standards (such as RTCA/DO-178B, Level A) for measuring and documenting statement coverage (SC), decision coverage (DC), and modified condition decision coverage (MCDC).

CodeTEST Hardware

Universal Probe provides a flexible hardware interface adaptable to a wide variety of target systems. Even under difficult space constraints the Universal Probe can connect to headers, busses, processors, and other devices.

CodeTEST-VME gives you a variety of selectable views of code behavior. Instead of “surfing” the VME backplane hunting for specific events with a bus analyzer, you can drill down and focus on individual processor code. Or move up to a higher level of abstraction and monitor System Level Trace to see the interactions among the various subsystem CPU board activities

Applied Microsystems
CORPORATION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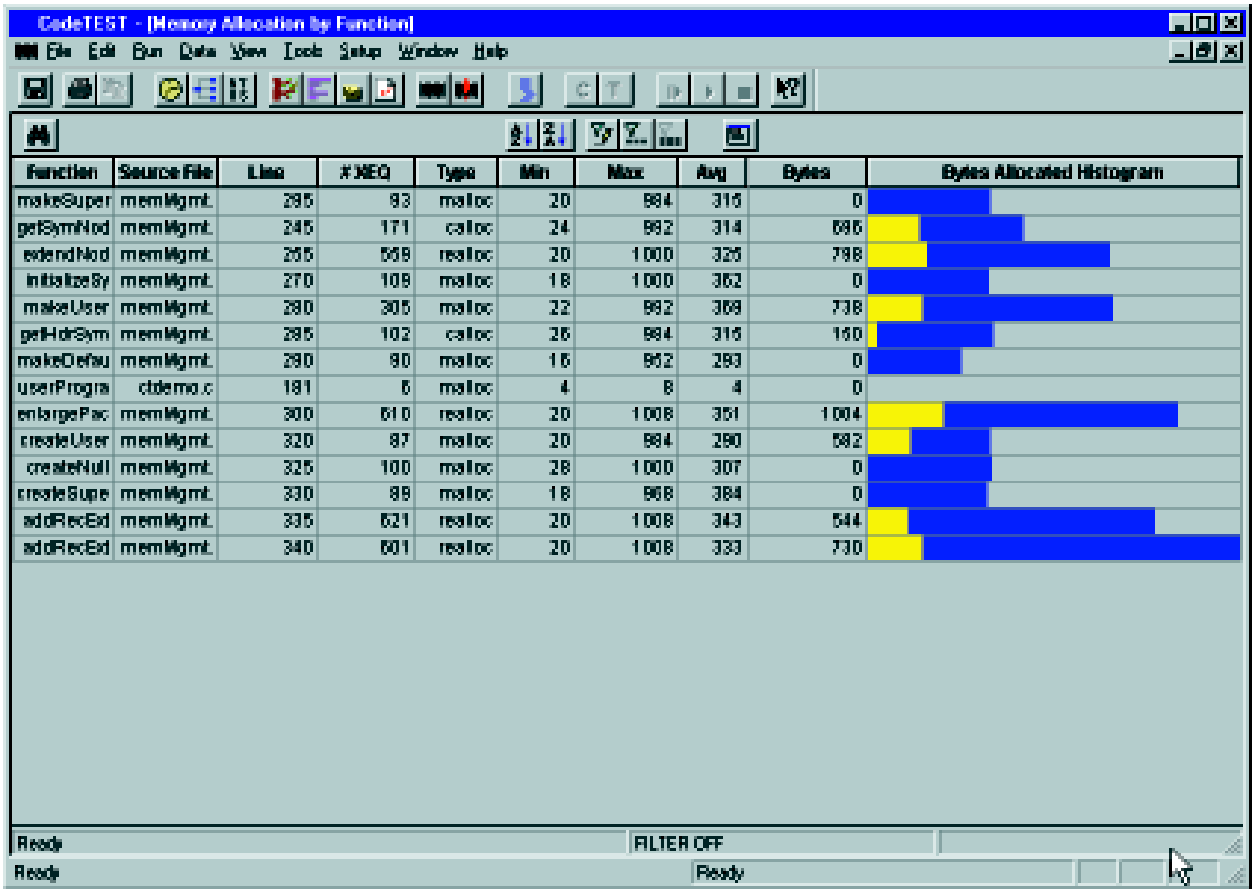
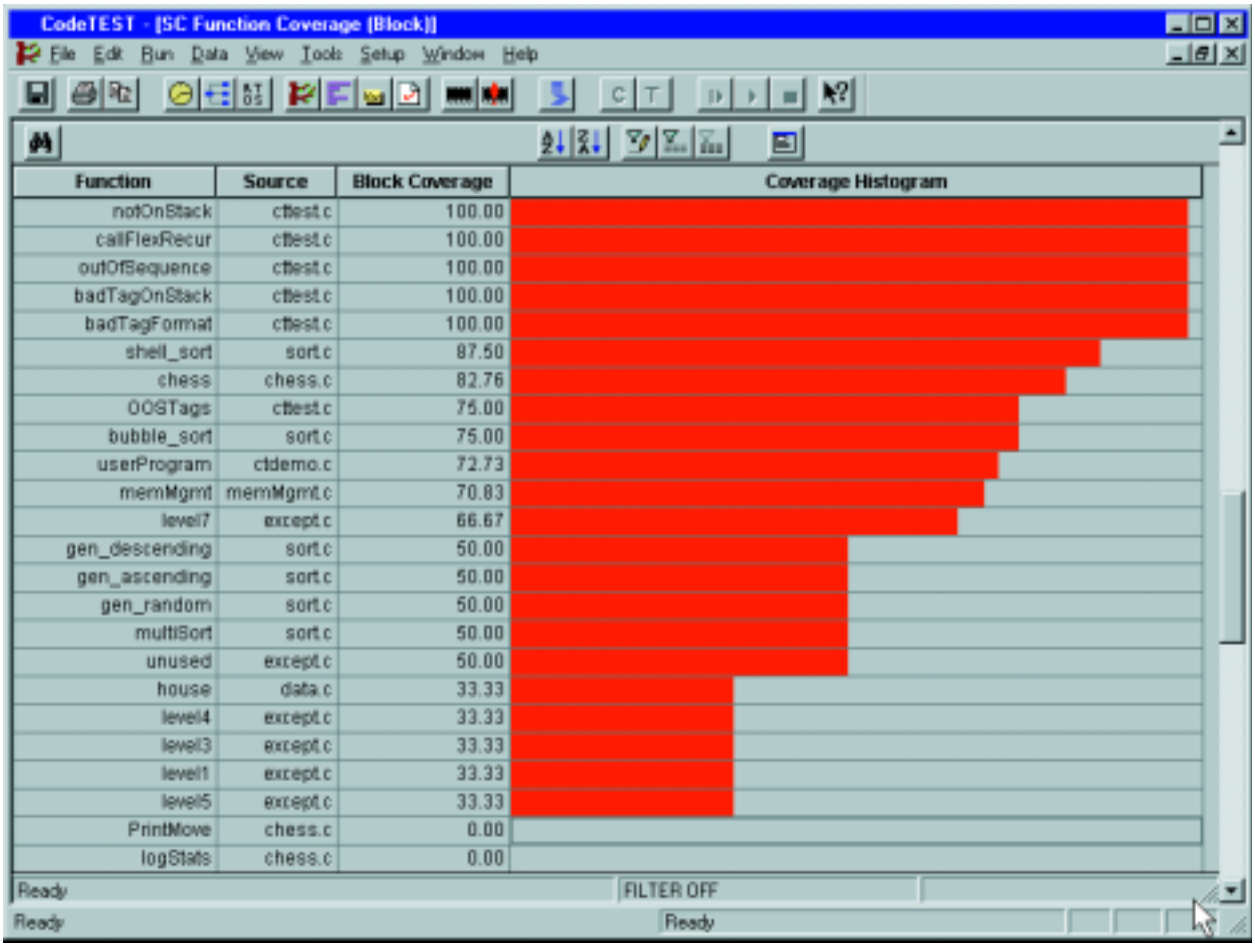
File Edit Run View Tools Window Help
SC Coverage Trend (Block)
% Coverage
Time of Measurement in Seconds
Ready
Ready


CodeTEST - [Memory Allocation by Function]
File Edit Run Data View Tools Setup Window Help
Function | Source File | Line | # XEQ | Type | Min | Max | Avg | Bytes | Bytes Allocated Histogram
makeSuper | memMgmt. | 295 | 93 | malloc | 20 | 984 | 316 | 0
getSymNod | memMgmt. | 245 | 171 | calloc | 24 | 992 | 314 | 686
extendNod | memMgmt. | 255 | 569 | realloc | 20 | 1000 | 325 | 798
initializeSy | memMgmt. | 270 | 109 | malloc | 18 | 1000 | 362 | 0
makeUser | memMgmt. | 280 | 305 | malloc | 22 | 992 | 369 | 738
getHdrSym | memMgmt. | 285 | 102 | calloc | 26 | 984 | 315 | 150
makeDefau | memMgmt. | 290 | 90 | malloc | 16 | 952 | 283 | 0
userProgra | ctdemo.c | 181 | 6 | malloc | 4 | 8 | 4 | 0
enlargePac | memMgmt. | 300 | 610 | realloc | 20 | 1008 | 351 | 1004
createUser | memMgmt. | 320 | 87 | malloc | 20 | 984 | 290 | 582
createNull | memMgmt. | 325 | 100 | malloc | 28 | 1000 | 307 | 0
createSupe | memMgmt. | 330 | 89 | malloc | 18 | 968 | 384 | 0
addRecExt | memMgmt. | 335 | 621 | realloc | 20 | 1008 | 343 | 544
addRecExt | memMgmt. | 340 | 601 | realloc | 20 | 1008 | 333 | 730
Ready
FILTER OFF
Ready
Ready



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NetROM

Features

◆ Target Communication
- High-speed Ethernet connection between target and host
- Rapid code download over Ethernet using standard protocols such as TFTP and TCP
- Four dual-port memory channels provide four LAN channels for multiple user sessions with NetROM or the target

◆ Target Control
- Eight user-asserted target command signals
- Eight status signals from the target that can be polled at will

◆ Memory Emulation
- Offers emulation memory of 1 or 4 MB
- Supports 8-, 16-, and 32-bit words
- Support for 64-bit words and over 4 MB emulation memory through multiple NetROM units
- Automatically supports both 5 V and 3.3 V memory devices

◆ Debugger Integration
- Integrated with industry-leading source-level debuggers
- Supports task-aware and system-level debugging
- Provides writeable memory for breakpoints in ROM space

◆ Cost-Effectiveness
- Reusable tool lowers development and debugging costs

NEC CPUs Supported

V85x

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

NetROM™ is a revolutionary product for embedded software developers. It provides a flexible debugging platform that combines high-speed target communication and debugging capabilties. NetROM requires almost no target resources and can be rapidly moved from project to project and from processor to processor.

NetROM supports a variety of debuggers and monitors from vendors including GreenHills, Integrated Systems Inc., Microtec Research, Microware, Software Development Systems, and WindRiver.

Linking your preferred debugger and target monitor, NetROM accelerates the development cycle through faster downloads and target communications, remote target control, and emulation of ROM memory devices. Using NetROM, developers can realize download and debug communications gains of approximately 20%. NetROM accomplishes this improvement by:
- Adding network connectivity to your target without requiring Ethernet hardware or software on the target;
- Eliminating the need to burn EPROMs or program FLASH devices;
- Replacing slow serial downloads with fast Ethernet downloads;
- Allowing target debugging to occur from any network host rather than a dedicated workstation;
- Reducing the time-penalty for software debug experiments.

NetROM offers emulation memory of 1 or 4 MB; supports 8-, 16-, 32-, and 64-bit words; and over 4 MB emulation memory through multiple NetROM units. Also automatically supports both 5 V and 3.3 V memory devices.

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DIAB-SDS

Optimizing C, C++, Java™ Compilers, Run-Time Analysis Tools, and SingleStep Debug Solutions

Features

- Highly optimizing compiler suites for C, C++, and Java™
- Fast, compact, high quality code for NEC V800 Series CPUs
- Application specific (profile-driven) optimizations for increased performance
- Run-Time Analysis tools, including Run-Time Error Checker and Profiler, for improved code quality, performance, memory usage
- FastJ™ compiles Java to native machine code for applications without a JVM
- Powerful SingleStep GUI debugger for advanced C, C++, Java and ASM debugging
- Task/kernel aware debug
- Exceptional flexibility and reliability for embedded applications
- Proven with leading RTOS and kernel packages

NEC CPUs Supported

V850, V850E

Host Platforms Supported

Windows 95/98/NT

Target Connections Supported

ROM monitors

Product Overview

DIAB-SDS is the embedded development tools leader and is widely known for its highly-optimizing compilers, award-winning Run-Time Analysis tools, and powerful SingleStep debug solutions. DIAB-SDS is a wholly owned, independent operating subsidiary of ISI.

Highly Optimizing Compilers

DIAB-SDS compiler suites are the expert's choice for demanding NEC V8xx-based designs. DIAB-SDS compilers feature the industry's most advanced compiler optimization techniques and offer superior performance, flexibility, and reliability. In addition to providing robust, standards compliant compilers for C, C++, and Java, DIAB-SDS tools offer many features specific to embedded development. These features include: generating ROMable code and data; ability to mix assembler with C/C++, and Java code; ROMable reentrant code and libraries; options to pack or byte swap structures to match existing data types; and complete control of code and data memory allocation and placement. For developers who want to program in Java but cannot afford the performance and size costs of a JVM, DIAB-SDS offers the FastJ compiler suite. FastJ compiles Java source code directly to native machine code and offers code size and performance comparable to C++. FastJ also supports mixed language programming so you can mix native C and ASM code with Java code. The SingleStep debugger features Java-specific capabilities that allow you to debug Java and mixed language applications. FastJ interfaces to an RTOS using Pthreads calls (a subset of POSIX). Check with DIAB-SDS to see if your RTOS/kernel is supported.

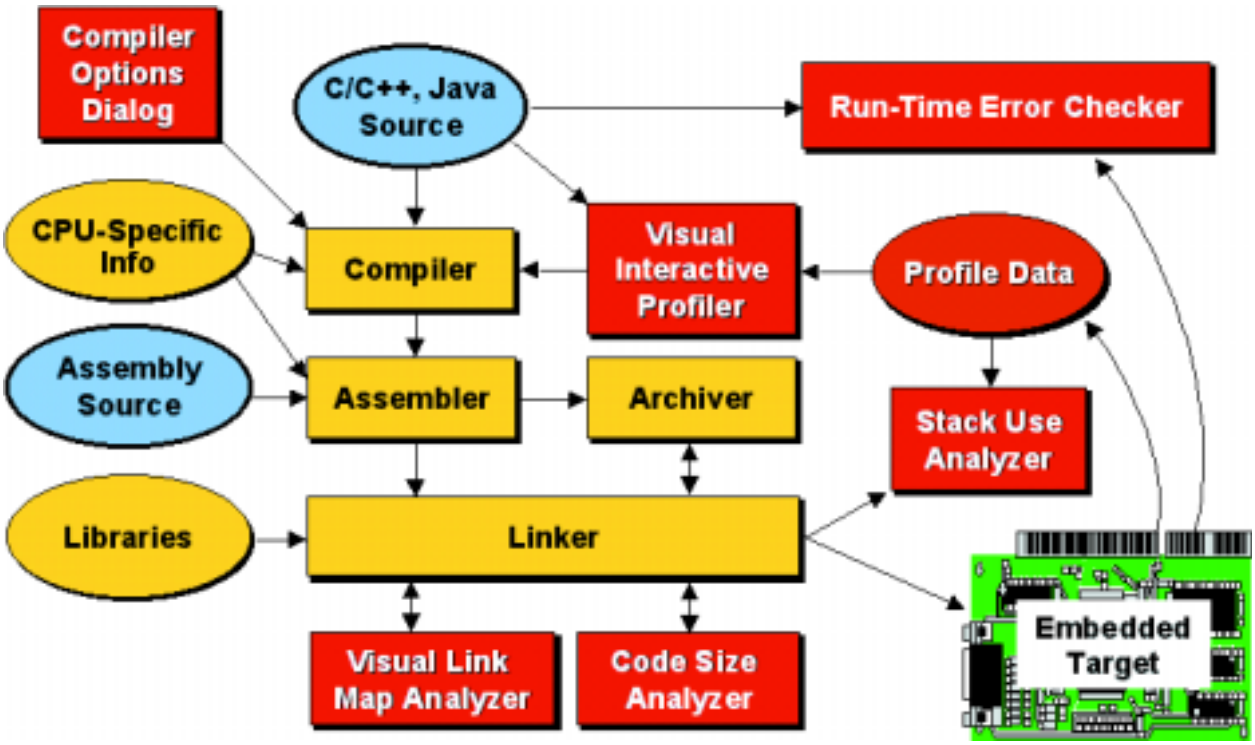
Run-Time Analysis (RTA) Tools

DIAB-SDS award-winning RTA Suite provides an integrated set of Run-Time Analysis tools to help you develop higher quality, higher performance code in less time. The RTA Suite includes a powerful Run-Time Error Checker, Visual Interactive Profiler, Stack Use Analyzer, Visual Link Map Analyzer, Code Size Analyzer and other tools to help you improve program reliability, performance and memory usage. In particular, the Run-Time Error Checker detects hard-to-find pointer errors and memory leaks while the profiler identifies true program hot spots for optimization purposes. DIAB-SDS compilers can also generate application specific optimizations based on run-time profile data.

diab·sds An ISI Company
The Embedded Tools Leader

SingleStep Debug Solutions
The SingleStep debugger is a powerful debug environment for embedded development. Graphical source-level and assembler-level debug features are combined with a wide array of tools to provide a rich environment for debugging and developing NEC V800 Series based designs. SingleStep also features advanced RTOS/kernel aware debug capabilities. These features allow you to debug applications in the context of your RTOS or kernel. Several leading RTOS packages are supported, including pSOSystem from ISI.

DIAB-SDS tools are available integrated with ISI's pRISM+ development environment and with other third party tools offerings. Contact your DIAB-SDS representative for more information.



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Green Hills Embedded Software Development Tools V800 Family

Features

Optimizing Compilers

- C, C++, Embedded C++
- Run-Time libraries

MULTI® Integrated Development Environment

- Source Level Debugger
- Graphical Project Builder
- Text Editor
- Version Control System
- Graphical Browser
- Performance Profiler
- Run-Time Error Checking
- Remote Target Connection

NEC CPUs Supported

V8xx

Host Platforms Supported

Windows 95/NT, SPARC/Solaris, PA-RISC/HP-UX

RTOSs Supported

ThreadX, VxWorks/Tornado, Nucleus PLUS, and custom RTOSs.

Target Systems Supported

Simulators, ROM Monitors, CPU Boards, In-Circuit Emulators, Processor Probes, OCD/BDM/JTAG

Product Overview

V800 Optimizing Compilers

The Green Hills Optimizing Compilers for V800 all utilize a common code generator with architecture-specific optimizations. Each supported V800 model has its own particular pipeline and instruction set characteristics. These are accommodated in the code generator to produce code best suited for the target processor. The following V800-specific features are supported:

- **Processor** - One option for each supported V800 model. This setting determines the instructions permitted, as well as the pipeline optimization strategy used.
- **V850 Tiny Data Area (TDA)**- Allocates a small area of TDA memory to hold small data objects and reference objects in that area.
- **Reserve r2 or r5 for the User** - The compiler reserves r2, r5, or both for the user.
- **Reserve r15-r24 (22 Register Mode)** - Generates code in 22 register mode.
- **Reserve r17-r22 for the User (26 Register Mode)** - Generates code in 26 register mode.
- **Constant value 255 in r20** - Size optimization for unsigned byte loads.
- **Constant value 255 in r20 and 65535 in r21**- Size optimization for unsigned byte and halfword loads.
- **Position Independent Code (PIC) and Data (PID)** - Allows executable files and data to be placed anywhere in memory and still run correctly.
- **Far Subroutine Calls** - Generates register-indirect calls for user functions.
- **Small Data Area (SDA)**- Allocates a SDA memory to hold small data objects and reference objects in that area.
- **Zero Data Area (ZDA)** - Allocates a ZDA memory to hold small data objects and reference objects in that area.
- **Small Prologue and Epilogue Code** (size optimization).
- **V850 Short Load/Store Size Optimization.**

Run-Time Libraries

A comprehensive suite of run-time libraries for C, C++, and EC++ are included in the corresponding compiler distributions for each language. Several different versions of the libraries are provided to accommodate different combinations of processor and memory models. The combinations include hardware vs. software floating point and CPU specific versions. Full featured start-up code and libraries include automatic copy of data from ROM to RAM and system call emulation. Source code to the run-time libraries is available so that users can customize routines according to the special needs of their applications.

The MULTI Integrated Development Environment

MULTI Software Development Environment is a complete integrated development environment for embedded applications using C, C++, and EC++ languages. MULTI provides a direct graphical interface with all Green Hills compilers, and supports multi-language development and debugging. MULTI contains all of the tools you need to complete a major programming project:

- Project Builder
- Source Level Debugger
- Performance Profiler
- Run-time Error Checking
- Graphical Browser
- Text Editor
- Version Control System

MULTI provides a host-based (Windows 95/98/NT PC or UNIX workstation) graphical environment for V800 target development. Host-target connectivity is provided through a variety of means, depending on the target environment. MULTI supports many V800 targets, including evaluation boards from NEC. These boards can be accessed with a variety of interfaces:

- **Bare Board Access (No RTOS or ROM Monitor)** - MULTI supports NEC's V850 In-Circuit Emulator through 850Eserv. MULTI provides a complete software package that enables programmers to debug code without need for operating systems, kernels, or even ROM monitors.

- **Commercial RTOS Support** - MULTI supports V800 boards running ThreadX and Accelerated Technology's Nucleus PLUS. MULTI provides multitask-aware debugging. Special commands allow tasks to be stopped upon system events such as task creation.

- **Custom RTOS Support** - MULTI can be interfaced with a custom RTOS through integration of the Green Hills INDRT API. INDRT provides all the debug information needed by MULTI, and is easily integrated into user code.

- **Instruction Set Simulator** - The *Sim800* and *Sim850* instruction set simulator interpretively executes V8xx programs on the host PC or workstation without the need for target hardware by simulating the execution of the target processor at the instruction level. *Sim800/Sim850* provides full debug features, host I/O, command window, and extended profiling. *Sim800/Sim850* also simulates target CPU cache for those processors which support it.

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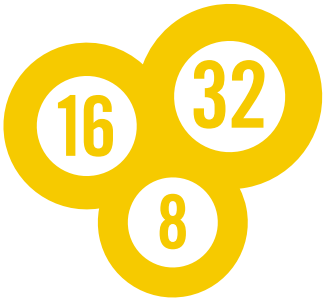
IAR Embedded Workbench™ for V85x family



Features

IAR Embedded Workbench for the V850

- Total integration of compiler, assembler, linker, librarian, and debugger
- Plug-in architecture for several IAR toolkits
- Hierarchical project presentation
- Integrated project manager and make facility
- Includes Source code and binary data editors
- Support for external tools (editors, version control systems)
- All tool options configurable from one dialog
- Extensive on-line help
- Runs under Windows 95/98/NT 4.0

IAR C Compiler for the V850

- Supports ANSI C as well as Embedded C++
- Supports the V850/V850S and V850E series
- 3 different memory models (tiny, small, and large)
- 3 code models (normal, large, and PIC code)
- Chip specific extensions to suit development for embedded applications
- Built-in V85x-specific optimizer.

IAR C-SPY™ Debugger for the V850

- C and assembler source level language debugger
- Powerful handling of complex breakpoints
- C-like macro language
- Powerful interrupt simulation
- C-structures browser
- Function level profiling
- Code coverage
- Trace

NEC CPUs Supported

V850/Sxx and V850E/xx

Host Platforms Supported

PC: Minimum 486, with Windows 9x, Windows NT 4.0
UNIX: SUN Solaris

Product Overview

IAR Embedded Workbench — The complete development tools for NEC V850

The IAR Embedded Workbench is a highly evolved development tool for programming embedded applications. The tool supports C and C++ for most V85x applications. The Embedded Workbench offers powerful and efficient optimization and ease of use. It gives the concept “user friendly” a whole new meaning for programming embedded applications. With its built-in chip-specific optimizer, the compiler generates very efficient, fast and reliable PROMable code. Furthermore, in addition to this solid technology, IAR also provides professional technical support, which is yet another reason why engineers adopt IAR C/C++ compilers.

C-SPY — More than just a high-level language debugger

The IAR V85x C-SPY is a high-level language debugger incorporating a complete C expression analyzer and full C/C++-type knowledge. C-SPY comes in three different flavors: Simulator, ROM-monitor and Emulator version. It combines the detailed control of code execution needed for embedded development debugging with the flexibility and power of the C/EC++ language. C-SPY shows the calling stack as well as tracing on both statement and assembler levels. The source window can display C/C++ source code and mix it with assembler. C-SPY has support for function level/ profiling and code coverage. There is also a ”locals” window showing the auto variables and parameters for the current function. CWV850 is user-friendly with customizable toolbars, drag and drop facility, and user-configurable shortcut keys for all commands.

IAR SYSTEMS

Support and Updates

IAR Systems V850 tool kit comes with the following benefits:

- 1 year warranty after purchase, including free technical support via: telephone, fax, and email, plus free upgrades.
- Extensive documentation including step-by-step tutorials.

Summary of available V850 Tools

- EWV850 Windows Embedded Workbench (including Compiler, Assembler & Linker)
- CWV850 Debugger/Simulator
- CWV850R Debugger/ROM-monitor version
- CWV850I Debugger/Emulator version for the NEC IE-703002-MC / IE-703102-MC series.

The V850 tools from IAR are compatible with most popular real-time kernels available on the market.

Consulting & Services

In times where the success of a new product is heavily dependent on time-to-market, outsourcing to specialists becomes one of the most momentous chances to lead a great idea into a big hit. Having the required V850 know-how in house, IAR Systems expanded their NEC V850 support from development tools to a complete service package, starting with pure consulting functions up to the development of „turn key“ solutions.

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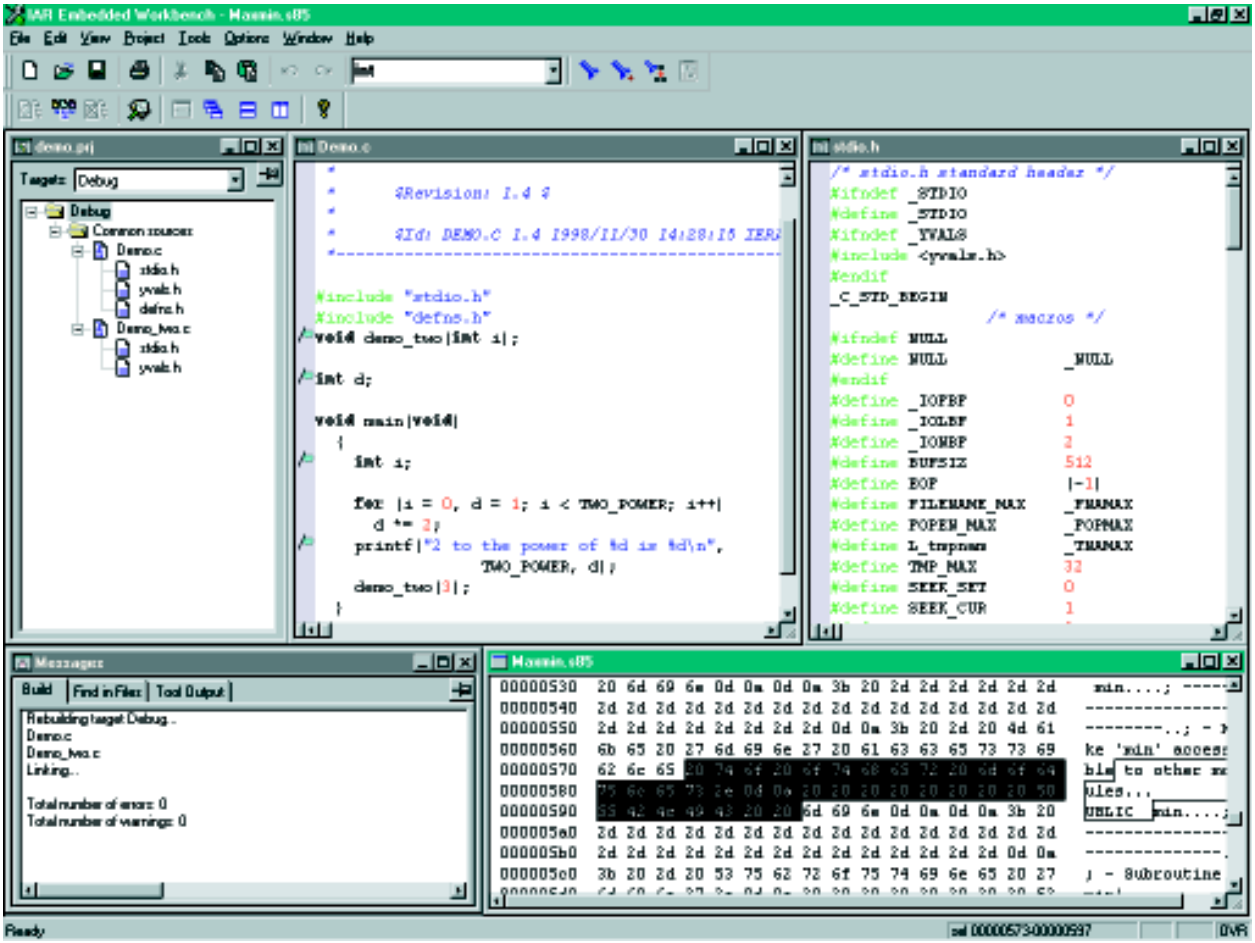


TRACE32-ICD
In-Circuit Debugger

Features

- ROM monitor based Debugger
- Software compatible with RISC Emulator TRACE32-FIRE for NEC V850
- Debugging via Eprom Simulator
- Source & Variable Windows
- Stack Frame Window
- Array and Structure Display
- Register and Peripheral Display
- Program and Spot Breakpoints
- Download Speed 100 kByte/sec
- Trigger Input and Output

NEC CPUs Supported

V851, V852, V853, V850/SA1, and V850/SB1

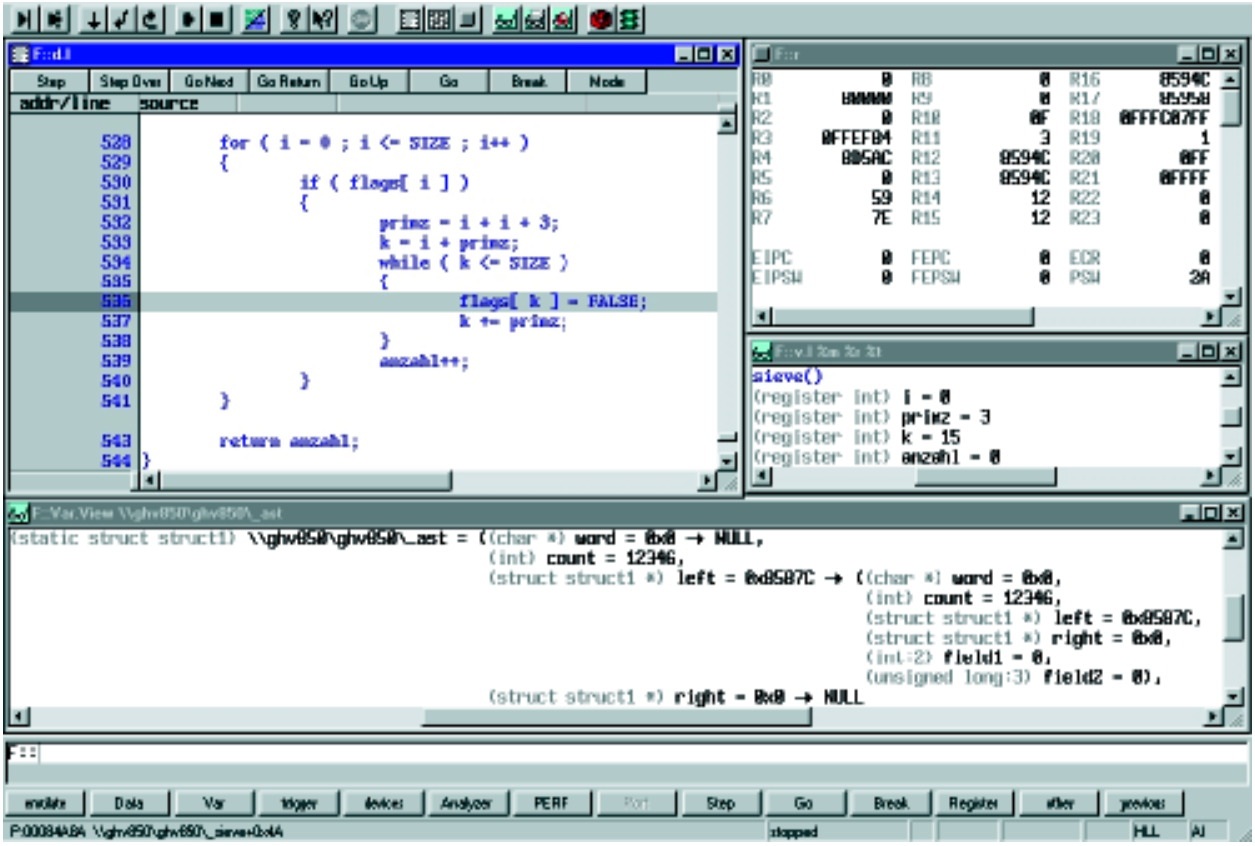
Host Platforms Supported

PC (Windows 3.11/95/NT), Linux, SCO-ODT, SUN3, SPARC, DEC-ULTRIX, VAX-VMS, ALPHA-OSF1, ALPHA-VMS, HP9000/300/400/700, AIX

Product Overview

The TRACE32 tool suite provides a complete set of development and testing tools. The advanced modularity of TRACE32 makes it very easy to upgrade the systems to future needs. TRACE32 works with the highest variety of host interfaces. TRACE32-ICD In-Circuit Debuggers are highly cost effective tools for debugging on high level language and assembler level. All major programming languages are supported from most compiler vendors. Real time systems support is also included for task and processor states.
The compatibility that exists between the TRACE32-ICD debuggers and Lauterbachs high end In-Circuit emulators TRACE32-ICE and TRACE32-FIRE opens up a wide range of application areas for these tools. In addition to the obvious application in starter and test system environments, ICD debuggers are more and more used in large projects for pure software development side by side with the high end tools. Moving from one tool to the other can be done seamlessly without having to learn a new user interface.
TRACE32-DEBUGGER - the highly intuitive software interface offers seamless integration with the entire range of TRACE32 hardware. It is completely configurable by the user, no other system offers more flexibility.

LAUTERBACH



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Real-Time Operating Systems

Nucleus PLUS
Real-Time Operating System

Features

- No royalties
- C source code provided
- Scaleable: 4 KB - 45 KB, depending on necessary functionality
- Written in ANSI C
- Deterministic, low interrupt latencies
- Extensible: make new services by combining existing services
- Configurable: easily exclude services not used
- Dynamic creation of all Nucleus PLUS tasks
- Intertask communication: mailboxes, variable queues, pipes
- Task synchronization: counting semaphores, events, UNIX-like signals
- One-shot and multiple-shot task timers
- Memory management: fixed partitions, variable length (malloc)
- Place any Nucleus PLUS component in any area of memory
- Advanced Interrupt Management Mechanism (AIMM)

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

Real-time services that are available in the basic Nucleus PLUS product are more full-featured and capable than virtually any real-time kernel on the market today. Accelerated Technology performed an evaluation of the most prominent real-time kernels currently on the market. From this analysis, Nucleus PLUS was developed. Nucleus PLUS has been developed with a "micro-kernel" structure in mind. That is, the essential services of the real-time, embedded environment are provided in such a way that additional operating-system-oriented features can be easily added.

Nucleus PLUS is a real-time, pre-emptive, multitasking kernel designed for time-critical embedded applications.
Nucleus PLUS is extremely portable and is currently available for use with most microprocessor families.

Accelerated Technology
INCORPORATED

Nucleus PC+ Prototyping Environment for Use with Windows 3.1/95

Features

- Interface Identical to Nucleus PLUS
- Test Software Using PC Software Tools (Borland C/C++™ and Microsoft C/C++™)
- Recompile With Intel i960 Dependent Files for Target System
- Use DOS Services for I/O
- Executes as a native Windows 3.1 or Windows 95 application

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

Nucleus PC+ is the version of Accelerated Technology's Nucleus PLUS kernel that can be used in an MS-DOS environment. This environment is ideal for embedded applications requiring the responsiveness of multitasking while taking advantage of low cost PC hardware. Further, all of your C code can be developed in the friendly PC environment.

Development Tools

The real mode version of Nucleus PC+ has been prepared for use with the Borland and Microsoft C compilers and assemblers. Accelerated Technology provides libraries that can be linked with your application to build a Nucleus PLUS-based application that is an MS-DOS executable. A special version of Borland's Turbo debugger that has been enhanced with Nucleus PLUS awareness has been developed by Paradigm Systems. This product, Paradigm DEBUG™, is ideal for debugging Nucleus PC+ applications that have been developed with either the Borland or Microsoft compilers.

For programs exceeding the 640 Kbyte boundary or those requiring the advantage of a 4 Gbyte address space, the protected mode version of Nucleus PC+ can be used. It's been prepared for use with the MetaWare High C™ and Watcom C™ compilers in combination with the PharLap DOS Extender™ and the PharLap™, Turbo™, or Microsoft assemblers.

Interrupt Management

Nucleus PC+ provides access to the PC's interrupt structure, allowing you to invoke a task thread from an interrupt. By doing this, executing threads can be preempted by an interrupt service routine. Nucleus PC+ also permits the processing of interrupts without kernel involvement. In this case, you perform the necessary register saving and restoring, or you can employ the INTERRUPT pragma.

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Nucleus C++ Object Oriented Real-Time Software

Features

- Object-oriented version of Nucleus PLUS
- Object-oriented approach to programming
- Objects can be statically or dynamically declared
- Service calls are handled as member functions
- Easy alternative to memory-sharing methods
- Full support for new and free operators
- Available for any C++ compiler

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

The power of C++ comes from its support for new ways of programming and thinking about programming problems. We at Accelerated Technology view this as being a significant breakthrough for the embedded industry. With C++, you can develop applications quickly by reusing components and efficiently designing applications using an object-oriented approach.

Nucleus C++ brings true object-oriented development to real-time systems. Objects can be statically or dynamically declared, while the creation and deletion of services become transparent to the user. Tasks, Task Communication, Task Synchronization, Timers, Memory Management, Interrupt Management, and I/O Drivers are all accessible as objects.

Service calls are handled as member functions specifically targeted to the object in question (e.g., task, queue, etc.). All Nucleus PLUS parameters use the data abstraction features of C++ automatically. Nucleus C++ Memory and Partition Pool objects allow an easy alternative to memory-sharing methods. Default parameters and typed objects, which simplify the application development cycle, make programming easier for C++ users.

Nucleus NET
TCP/IP Protocol Stack

Features

- TCP/IP Protocol stack
- Protocols supported: TCP, UDP, IP, BOOTP, IGMP, ICMP, ARP, RARP, DNS, DHCP
- Optional protocols: RIP/RIPII, PPP, POP3, and SMTP
- Socket User Interface
- Full Integration with Nucleus PLUS for optimal performance.
- Blocking and Non-Blocking Services Supported
- Standard Interface to Physical Layer Devices
- Send/receive ping requests
- Compact and scalable

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

Nucleus NET is a set of networking protocols to provide interoperability between Nucleus PLUS-based systems and other TCP/IP or UDP/IP based systems.

A socket interface is provided to maintain a similar programming environment to those familiar with the UNIX socket programming model.

Nucleus NET provides a well defined driver interface for user supplied drivers, and can support various MAC layer drivers. There is less wasted memory space, due to a more efficient packet-buffering scheme, and support is available for Raw IP, IP forwarding, IP reassembly, IP fragmentation, and IP multicasting, IGMP, and DHCP services. Network-centric applications, such as routers, switches, and bridges are also supported. Nucleus NET is also the foundation for ATI's latest Web-related products, including Nucleus WebServ.

As with all Accelerated Technology products, Nucleus NET is delivered in source code form and no royalties are charged for the inclusion of binary copies in a single product line. Nucleus is also provided with six months free technical support. This includes phone, fax, email and new releases. For more information, contact Accelerated Technology today.

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Nucleus VNET
Virtual Networking Support for Nucleus PLUS

Features

- Supports virtual networking between multiple Nucleus PLUS based TCP/IP, WinSock, and remote node applications
- Hosted on Windows NT or remote nodes on network
- Access to full Visual C++ features
- Depends on Nucleus MNT and Nucleus NET
- Can build and test multiple TCP/IP applications on same target
- Two levels of device driver support

NEC CPUs Supported

V850/SA1, V850E, V853

Host Platforms Supported

Windows 95/NT

Product Overview

TCP/IP services are provided for Windows NT™ in the Nucleus MNT environment through a virtual networking facility. Nucleus VNET is a version of Nucleus NET that has been ported to the Windows NT environment. Nucleus VNET allows Nucleus MNT processes to communicate with each other via a shared memory area. That means multiple versions of Nucleus MNT can be executed on an NT machine, each with its own IP address. Developers who use this technology have the ability to simulate a network on an NT machine. The same shared memory area can be used to communicate with Windows NT applications via a virtual NDIS driver and nodes on the physical network using Windows NT routing facilities.

Initialization

Nucleus VNET's Virtual NDIS driver, which is responsible for allocating the global memory area, is started when the NT workstation is booted. The VNET driver then is started manually by the user. This driver must be started after the NDIS driver because it depends on the NDIS to allocate and initialize the common memory. After both drivers have been started, one or more Nucleus MNT/Nucleus VNET applications can be executed.

Communication

Nucleus VNET applications communicate with the VNET driver via NT's Device I/O Control call. Because Nucleus VNET requires Windows NT device drivers, it will execute only on a Windows NT workstation.

Accelerated Technology
INCORPORATED

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OSE - the new Generation Real-Time Operating System

Features

- Design on a higher level
- Interprocess communication
- Automatic error detection
- OSE kernel high throughput
- Small size
- OSE is a fully pre-emptive real-time kernel
- Basic System Calls:
  - alloc
  - send
  - receive
  - receive_w_tmo
  - free_buf
  - delay
- OSE Illuminator high performance debugging

NEC CPUs Supported

V850, V850E

Host Platforms Supported

PC: Windows 95/NT

Product Overview

OSE is a powerful architecture for the design of real-time embedded systems. OSE offers a modern, high-level approach to the development of realtime systems that achieves significant time savings over development using a more conventional RTOS.

Design on a higher level
While OSE offers all the functionality of a conventional RTOS, most applications can be programmed using a powerful subset of system calls. This results in greater clarity during the design and code phases and much faster code development. Together with OSE's automatic error detection and built-in application level debugging, these features greatly enhance productivity.

Interprocess communication
OSE is based on a message-passing model that provides fast, asynchronous interprocess communication. Work performed by the application is divided into a number of communicating processes. Each process is a separate object with its own protected resources, which are entirely controlled by the kernel. For example, OSE message queues do not need to be set up by the application process. The kernel automatically creates all processes with a message queue of unlimited size that is initialized and ready to use. The system can easily be divided into logical parts, independently designed and coded. Messages provide a clean interface between the processes.

Automatic error detection
OSE has a very advanced, built-in error detection system. Unlike a conventional RTOS, OSE automatically invokes a user-defined error handler if an error is detected. This simple feature replaces the complex code and inconsistencies that often result when programmers handle errors differently throughout the application, if at all.

OSE Kernel
OSE for V850 is a multitasking, fully pre-emptive real-time operating system for the NEC V850 processor family including the V850E. OSE for V850 combines high functionality with excellent realtime performance since the kernel is entirely written in highly optimized assembler. In particular, signal handling is extremely efficient, resulting in very high data throughput rates, making it ideal for high performance communications applications. OSE for V850 is a deterministic real-time operating system and performance is independent of the size of the application. OSE is written in highly optimized assembler specially tuned for the V850 processor family. The code size of the kernel is only 8 kbytes. OSE is a fully pre-emptive real-time kernel. Processes can be interrupted and rescheduled between any CPU instruction, even within a system call. Through the use of a signal-based concept, a basic system call set of six calls is enough to write a majority of the application code, significantly simplifying the coding. For special functionality, some 30 additional system calls are available within OSE.

OSE Illuminator

OSE provides a system that is very straightforward to design. It also provides the unique capability to debug a system in the same way it was designed – at the application level of message passing and process swaps. Illuminator is an application level debugging tool which allows monitoring, tracing and breakpoints on interprocess communication and context switches – thus debugging on a higher level.

OSE Illuminator Functions

Breakpoints, system trace and monitoring on:

- Signal send
- Signal receive
- Process swap
- System error
- Time stamp on traced events
- Memory pool analysis
- System profiling
- Stack usage and analysis
- Process status with signals in queue
- System timing analysis
- System error reporting

High Performance Debugging

The OSE Illuminator can be connected over a serial line to the target system. For high performance debugging, Illuminator can also be connected via a special interface (E-Box) to the target system. The E-Box has ist own high-speed processor and performs most of the system level debugging functions separated from the kernel and the target system. As there is very little debug code left in the kernel, the target system can run at almost the full speed even with all debug functions enabled. As the debugger is separated from the target system, full runtime non-intrusive system level debugging is possible. This technique allows Illuminator to debug even crashed systems giving full post mortem debug possibilities.

C/C++ Compiler

The OSE for V850 Real-Time Operating System supports actually the C/C++ development environments from IAR Systems and Greenhills.

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ERCOS^{EK}
OSEK Real-Time Operating System

Features

- Reliability proved in several mass-production projects
- Sophisticated task- process concept
- Cooperative and preemptive multitasking within one application
- Fast scheduling of periodical tasks using the ERCOS^{EK} time- table
- Resource protection by the advanced priority ceiling protocol
- System time
- Deadlines
- Fully integrated in the ETAS tool chain

NEC CPUs Supported

V85x

Host Platforms Supported

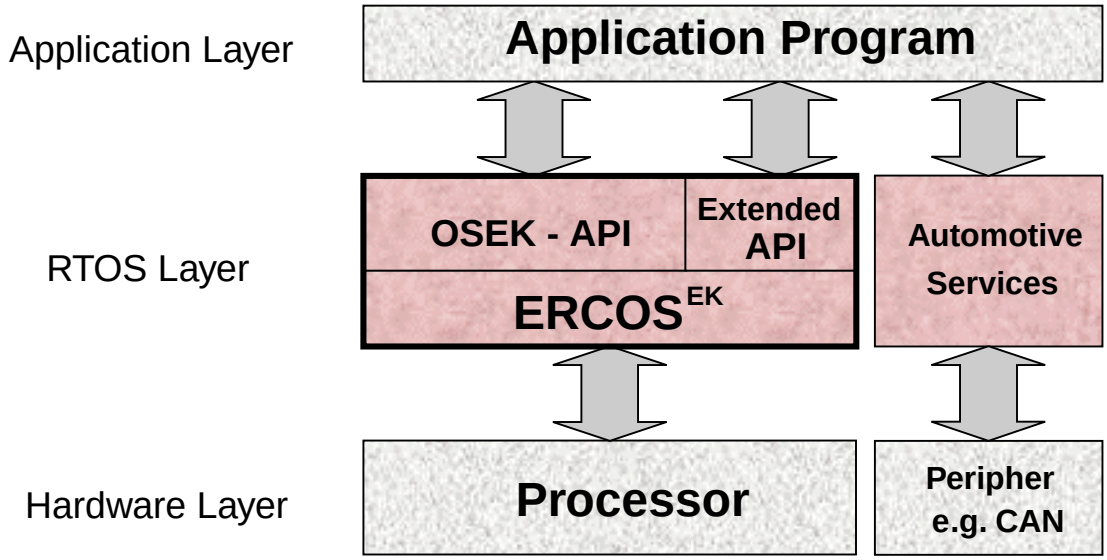
PC: Windows 95/98/NT

Product Overview

The extensive years of ETAS experience in the automotive sector, well thought-out embedding in the development process and the proverbial reliability are probably the decisive factors for the success of ERCOS^{EK}. This is reflected, for example, in the mass production of various ECUs based on ERCOS^{EK}.

ERCOS^{EK} corresponds to the international OSEK standard and communicates with the application via the interface defined in the OSEK standard, the OSEK API. Over and above this, ERCOS^{EK} offers an extended instruction set that the user can but doesn't have to use. These extensions have developed from practical experience and have proved their efficiency over the years.
Some of these extensions are also likely to become OSEK standards in the future; ETAS is ahead of its time.
The connection of the application to the hardware is perfect with the Automotive Services - reflecting the ETAS philosophy of a consistent and extensive tool chain. The Automotive Services can be seen as drivers and are available for the following functions: CAN, KWP2000, CCP, the OSEK COM transport layer and a gateway for protocol conversion.

ETAS
Engineering Tools



Applications based on ERCOSEK:

- Engine management, gasoline
- Engine management, diesel
- Control systems for diesel injection pumps
- Transmission control systems
- Electrical power steering
- Dashboard systems
- Adaptive Cruise Control
- Powertrain management
- Antiblock systems
- Traction slip control
- Driving dynamics control
- Control for electric-powered car

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pSOSystem
Real-Time Operating System

Features

- Field-proven in over 38 million embedded devices worldwide
- pRISM+ integrated development environment
- Industry leading networking, including Internet standards
- Scalable and customizable to fit individual application requirements
- Support for a wide variety of CPUs and drivers
- Fast, deterministic pSOS+ kernel
- Pre-emptive tasking environment
- Popular Board Support Packages supplied in source code format
- Multi-processor support, including NEC's v8xx processor family

NEC CPUs Supported

v8xx processor family

Host Platforms Supported

Windows 95/98/NT

Product Overview

pSOSystem™ is a modular, high-performance, real-time operating system (RTOS) designed specifically for embedded microprocessors. It provides a complete multi-tasking environment that offers performance, reliability, and ease-of-use on both custom and commercial hardware. pSOSystem is supported by ISI's pRISM+® integrated development environment, an integrated cross-development environment that speeds all phases of embedded application design, development and debugging. In addition, many third-party solution providers offer a variety of tools to support pSOSystem.

Along with all of ISI's embedded systems solutions, pSOSystem helps developers bring superior products to market faster than ever before. It uses a modular architecture, containing ISI's pSOS+® real-time multi-tasking kernel and a collection of companion software components and libraries. Each piece of pSOSystem is completely self-contained, allowing developers to scale OS functionality and memory to meet the exact requirements of each application. Developers can easily scale pSOSystem-based designs, from simple stand-alone devices to complex, networked, multi-processor systems.

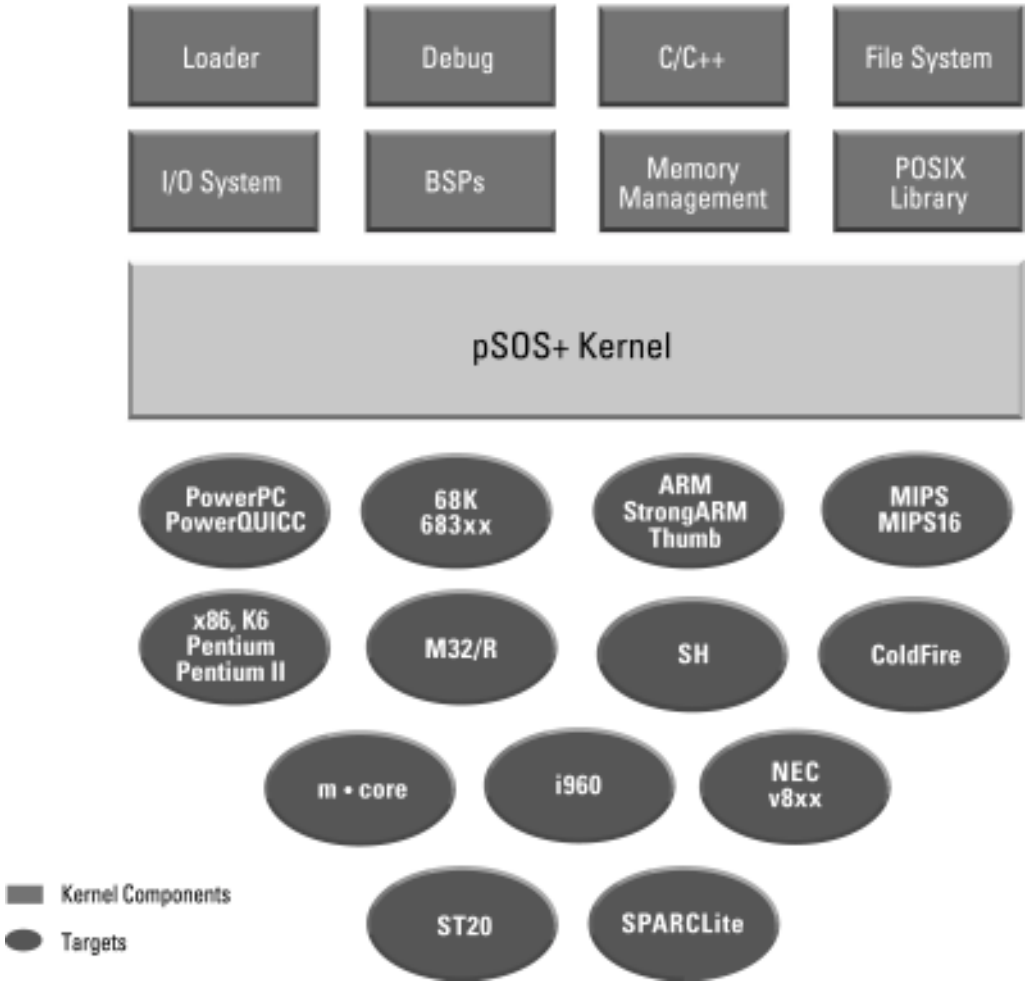
pSOSystem component technology is combined with a Board Support Package (BSP), which contains chip initialization and device drivers that isolate the pSOSystem components and the application from the underlying hardware, protecting the application development against processor and peripheral hardware obsolescence. New or upgraded hardware requires only simple modifications to device drivers in the BSP.

pSOSystem provides all of the layered applications required to complete designs quickly and easily, including file transfer and sharing capabilities, and embedded user interfaces.

Processor Support
pSOSystem supports the v8xx processor family.

Support, Service and Training
ISI's customers enjoy comprehensive training, product maintenance, online and telephone support, and field application engineering. In addition, they benefit from ISI's specialized engineering design service center, Doctor Design, Inc., which provides co-sourced technical consulting expertise to speed customers' project development and accelerate time-to-market.

ISI's Customer Education Services group helps customers make the most of their ISI investment with a variety of courses and training sessions. Classes are scheduled at numerous locations throughout the world and cover a variety of topics ranging from basic principles to advanced applications.



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embOS

Features

- Preemptive multitasking
- Fast & efficient
- Affordable, no royalties
- Small footprint
- Fully interruptible kernel
- Easy to use
- Versatile
- Support directly by developers

NEC CPUs Supported

V85x

Host Platforms Supported

PC: Windows 95/98, Windows NT, UNIX

Product Overview

A real-time operating system for embedded applications is designed to offer the benefits of a fully featured multitasking system even for hard real time applications using minimal resources.
The kernel is fully interruptible and so efficient that it can be used in very time critical applications. The memory footprint in both RAM and ROM is so small that it can be used with single-chip microcontrollers, leaving maximum room for the user-program.All functions of **embOS** have been placed in individual moduls to ensure that only the functions needed are actually linked into the application program. Despite its size and efficiency, it features the entire palette of communication mechanisms such as mailboxes, events and different kinds of semaphores.
All tasks and communication instances can be dynamically created, deleted and configured.
embOS is fully priority controlled: Of the tasks in READY-state, the one with the highest priority is active.
Tasks that have identical priorities are executed “quasi-simultaneously” in round robin. If no task is ready, **embOS** automatically puts the CPU in to a power-saving mode in the idle-task.

Debugging

is made easy: **embOS** is supplied in a release and debug version, where the debug version catches most programming faults like bad pointers, uninitialized data structures, even stack overflows.

emWin

A fully featured GUI is available for applications using graphical displays. It works seemslessly with **embOS** and any type of graphical LCD even under tough real time conditions.

Developing applications with embOS

embOS is available in source or object code form. Both come with libraries for all memory models, initialization of the controller in “C”-source, usable sample modules and a frame application in source code form. This frame program creates 2 tasks with little functionality. By modifying this frame application, the first steps are very easy (Experienced programmers have the first multitask program running in typically less than 1 hour). All parts that might have to be adopted to the application are provided in source code form.

Typical applications for embOS

Everything from battery-powered, single chip products to systems demanding ultra-fast response, flexibility and multiple processes :

- programmable machine controls
- printers
- telecommunication equipment
- battery powered instruments.

Technical Info

kernel size (ROM)	1100 - 1600 byte*
kernel RAM usage	18 - 48 byte *
kernel CPU usage	at 1 ms Tick with V850 lss than .3%
RAM usage mailbox	9 - 18 byte
RAM usage binary and counting semaphore	3 - 12 byte
RAM usage of resource semaphore	5 - 12 byte
RAM usage timer	9 - 16 byte
RAM usage event	0
Basic time unit (One Tick)	Default 1 ms, can be configured, Min. 100µs (V850)**
task activation time	independent of no. of tasks (e.g. max 12 µs V850)
interrupt latency time	very short, since kernel is fully interruptible
No. of tasks:	Unlimited (by available RAM only)
No. of mailboxes:	Unlimited (by available RAM only)
No. of semaphores:	Unlimited (by available RAM only)
No. of software timers:	Unlimited (by available RAM only)
Max. no. of priorities:	255
Max. no. of tasks with identical priotities	Unlimited

* Actual site depends on CPU, C-Compiler and memory
** Actual minimum depends on CPU, system clock, speed of bus interface etc.

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osCAN

Features

Products:

- OSEK/VDX conformant operating system
- Tool for CAN applications in the automotive field
- Tool for CAN applications in the automation field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V850

Host Platforms Supported

Windows 9x/NT

Product Overview

osCAN is a fully OSEK/VDX 2.0 compliant Real-time Multitasking system. Highly scalable and efficient, osCAN offers a set of networking modules for almost all CAN based applications. The OSEK kernel may be combined with the OSEK net management as well as with the CANopen or DeviceNet protocol stack.

Operating System: OSEK/VDX is a static operating system. All operating system objects may be defined with the easy-to-use graphical configuration tool from Vector Informatik. OSEK is dedicated to event driven applications, but comfortable timing functions are provided as well.

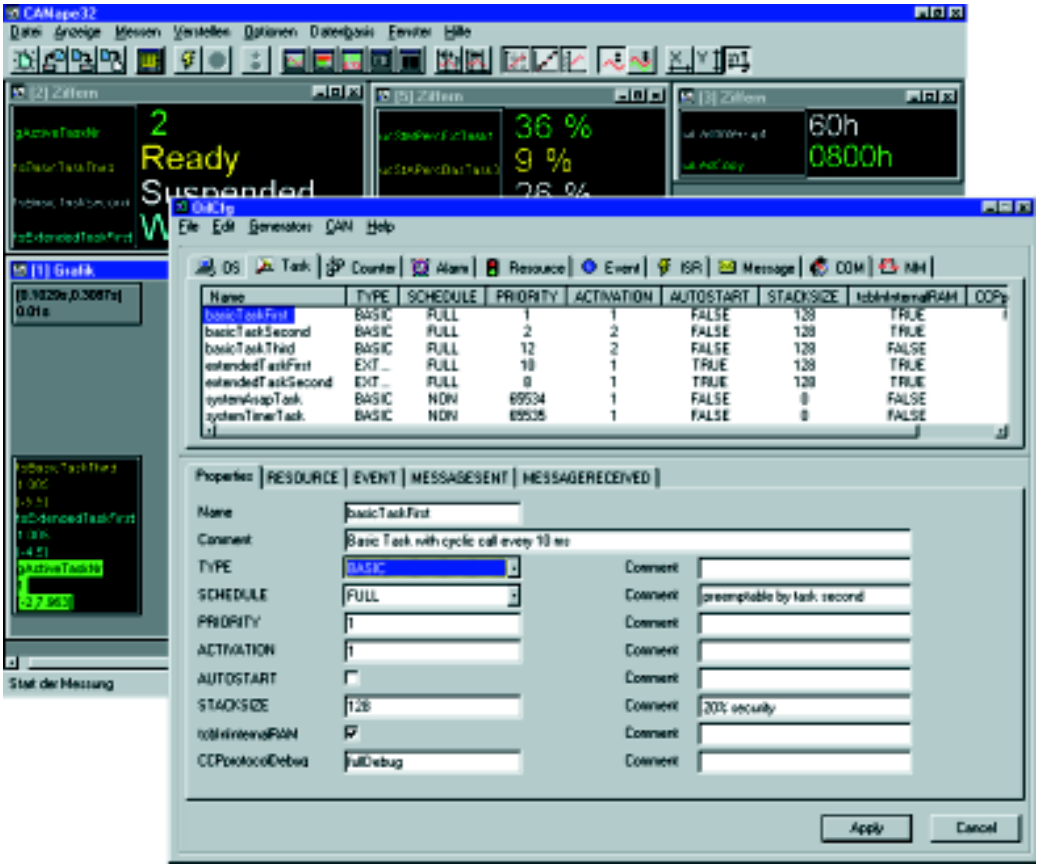
Network management: Within this OSEK-NM V2.5 compliant module standard node supervision and the transitions between operating and sleep mode are defined.

CAN driver: The widely used CAN driver offers logical handles for a strict separation of the universal driver code and the specific data structures. The identifier set up is comfortably accomplished using the CANdb editor, which is delivered together with the driver.

Simulation: With CANoe-OSEK a simulation tool is available from Vector Informatik. Designed for the support of system design and integration of CAN-networks CANoe offers the possibility to design the application according to the OSEK standard and simulate it on a PC.

Remote debugging: The diagnosis tool CANape from Vector Informatik allows monitoring of operating system objects under standard operating conditions, whenever a standard emulator is not applicable. Data access is done remotely via the CAN-bus, using the standard automotive CCP protocol. The necessary configuration of CANape is generated automatically.

Target Systems: NEC 78K0, NEC V850 and various platforms from other vendors.



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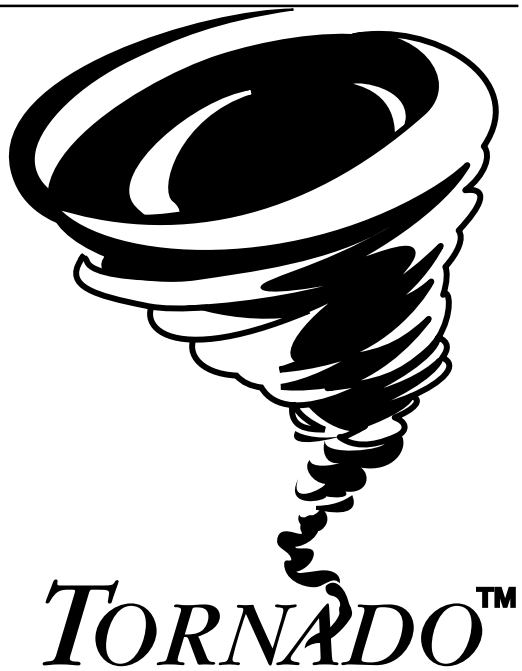
Tornado II™ Development Environment



Featuring the Industry-Leading VxWorks® RTOS

Features

- The superior development platform for the embedded developer
- A complete, intuitive and integrated tools suite
- Includes C/C++ compiler, editor, browser, powerful debugger and advanced command shell
- An open, extensible and customizable environment with published API supported by over 500 third Party Wind River Partners
- Additional run-times include fully featured networking, communications, graphics, Embedded Internet, Java, multi-processing and file systems.
- Powerful optional tools including source navigator, code coverage, dynamic memory analyser, dynamic C++ object visualisation, real-time data analysis and OS analyser.
- Open target connection strategy with tools independence including serial, ethernet, ROM emulator and in-circuit emulator
- GUI driven configurator for VxWorks® scalability across all real-time implementations
- Includes the proven, industry standard, high performance VxWorks® Operating System

NEC CPUs Supported

V85x

Host Platforms Supported

UNIX workstations, Windows 95/98/NT

WindRiver® SYSTEMS

An ISO 9001 Registered Company

Product Overview

Available for both UNIX- and Microsoft Windows-based hosts, the revolutionary Tornado development environment consists of the Tornado tools suite, the VxWorks RTOS, and a full range of communications options connecting host and target. All Tornado tools can be utilised at any stage of application development, with any level of target system resources. All are fully integrated and have sophisticated GUIs, and all are available regardless of target connection strategy (Ethernet, serial, ICE, ROM monitor or custom).

The Tornado APIs are published, from the GUI interfaces down to the debug agent interface, to facilitate customisation and third-party integration. In addition, developers can take advantage of a variety of productivity-enhancing WindPower Tools, including the VxSim simulator, the WindView system visualizer, Look! C++ dynamic visualisation debugger, CodeTest code coverage, CodeTest dynamic memory allocation analyser and the Stetho Scope data monitor.

VxWorks provides fast multitasking, preemptive scheduling (with optional round-robin scheduling for same-priority tasks) and fast interrupt response. To these microkernel features, VxWorks adds intertask communications and synchronisa-tion facilities, efficient memory management, multiprocessing support, a fast I/O system, IDE and SCSI support and MS-DOS, FLASH and RT-11-compatible file systems.

Tornado networking includes 4.4 BSD UNIX TCP/IP, sockets, SNMP, DHCP, NFS, RPC, ftp, rlogin, telnet and optional support for the X Window System. A wide range of integrated third-party networking products are available through WindRiver's WindNet Partners program, including ATM, OSI, SS7, Frame Relay, STREAMS, CORBA, ISDN, X.25, CMIP/GDMO, V.2, Iv6, XTP, Internet Protocols, and distributed network management.

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Evaluation Boards and Supported Hardware

*start*WARE – Starterkit for the V850/SA1 Microcontroller

Features

- Easy device evaluation capabilities
  *start*WARE contains elements to easily evaluate simple I/O functions such as serial interface, DIP-switches and 7-segment display.
- Debug monitor
  User application programs can be debugged using Green Hills MULTI Debugger.
- Internal flash memory
  V850/SA1 internal flash memory (256 kB) is available to use the *start*WARE as a standalone device or as a ready-to-use-system in user specific applications. The lower 128 kB contain a debug monitor and hardware test functions.
- external flash / RAM
  User application programs may be down-loaded into external flash memory or SRAM. 512 kB of external flash memory and 512 kB of external SRAM are available on *start*WARE.
- Flash programming support
  The monitor software contains self-programming support functions to program those areas of internal flash memory of the microcontroller that are not used by the monitor itself. Furthermore an external flash programmer can be connected for programming microcontroller internal flash memory.
- Zero wait-states
  Fast external memory is used to allow access to external RAM at 0-wait states. Access to external flash memory can be done at 1-wait state. If internal flash is used for program execution this is done with 0-wait using 32-bit memory access.
- Connectors for processor signals
  Almost all signals of the microcontroller are accessible via two 50-pin connector-pads. These can also be used for connecting *start*WARE to an external target board.

NEC CPUs Supported

V850/SA1

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

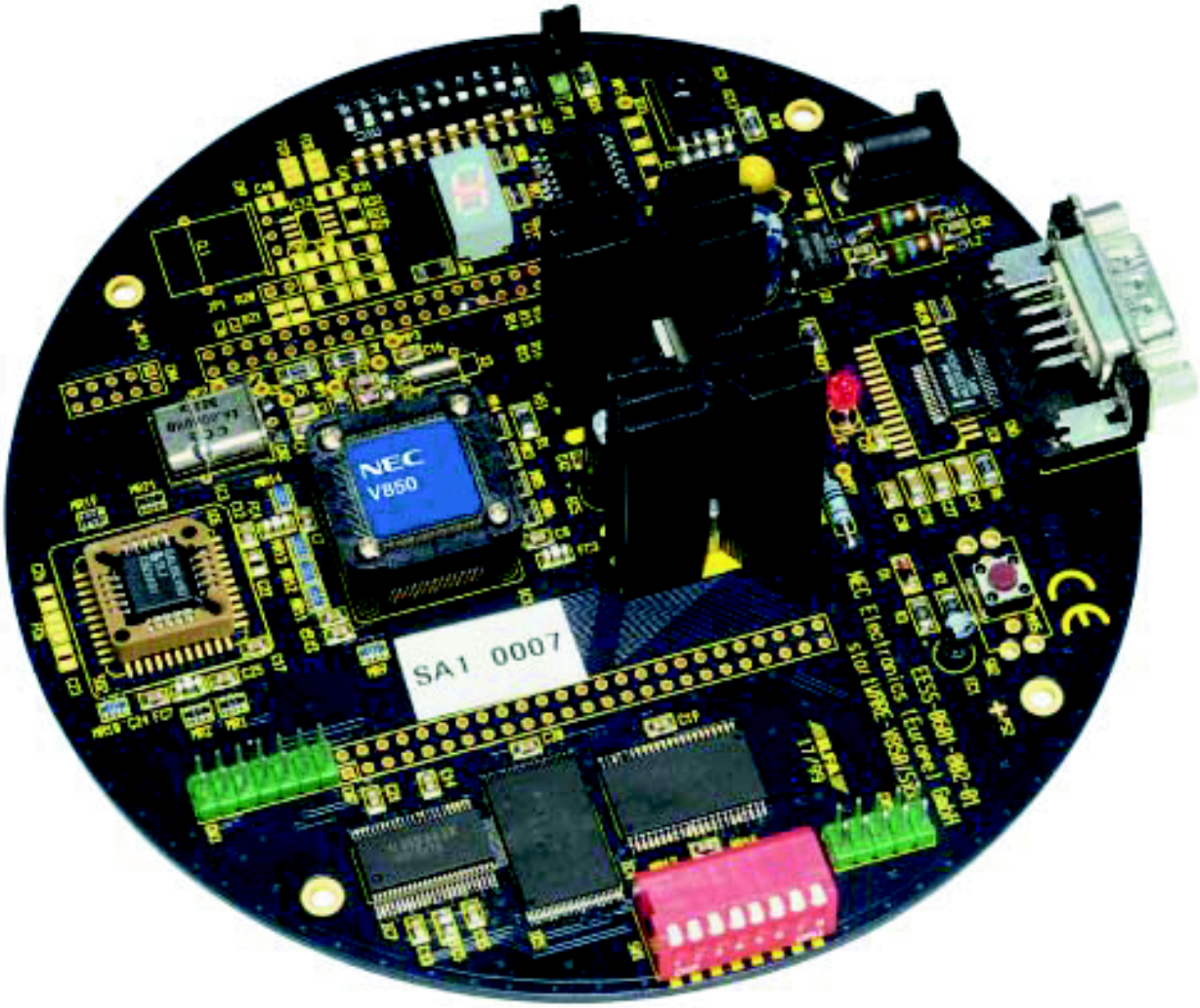
*start*WARE is a starterkit intended for evaluation of the V850 architecture using the V850/SA1 microcontroller. It allows easy evaluation of the V850/SA1 microcontroller by real time execution of application programs with and without connection to a host PC as well as connection to any kind of target hardware. It comes fully equipped with external RAM and flash-memory as well as a serial interface and parallel I/O for fast and easy first results. *start*WARE contains the Green Hills MULTI integrated development environment for comfortable development and debugging of user application programs.
Being compact and easy to set-up and use *start*WARE is the perfect tool to demonstrate and evaluate the key features of the V850 architecture in an all-in-one-concept.

RISC by NEC®: Know-how²

NEC

Ordering Information

Description	Order number
StartWARE Starterkit for V850/SA1	STARTWARE-GHS-V850-SA1



*flash*MASTER

Features

- Simple manipulation under Windows. The control SW runs under Windows 95/98/NT. Writing can thus be achieved through very simple handling.
- Interface with host via serial (RS-232C) or parallel centronics interface
  Serial transmission is possible from 9600 Baud to 38400 Baud.
- In system programming
  *flash*MASTER enables program writing without removing the CPU from the user system
- Data protection
  *flash*MASTER can write to flash ROM, but cannot read its contents. Its verification function can detect a verification error only in units; therefore data already in the CPU is protected
- Compatible data formats
  Intel - HEX-format
  Motorola S-Records
- EEPROM holds all programming parameters
- For factory programming an on-board Flash is implemented to store the program data
- Voltage supply
  flashMASTER provides supply voltage and programming voltage to the programming adapter
- Target Interface
  CSI
  UART
- Host Interface
  RS232
  Centronics

Host Platforms Supported

PC: Windows 95/98/NT

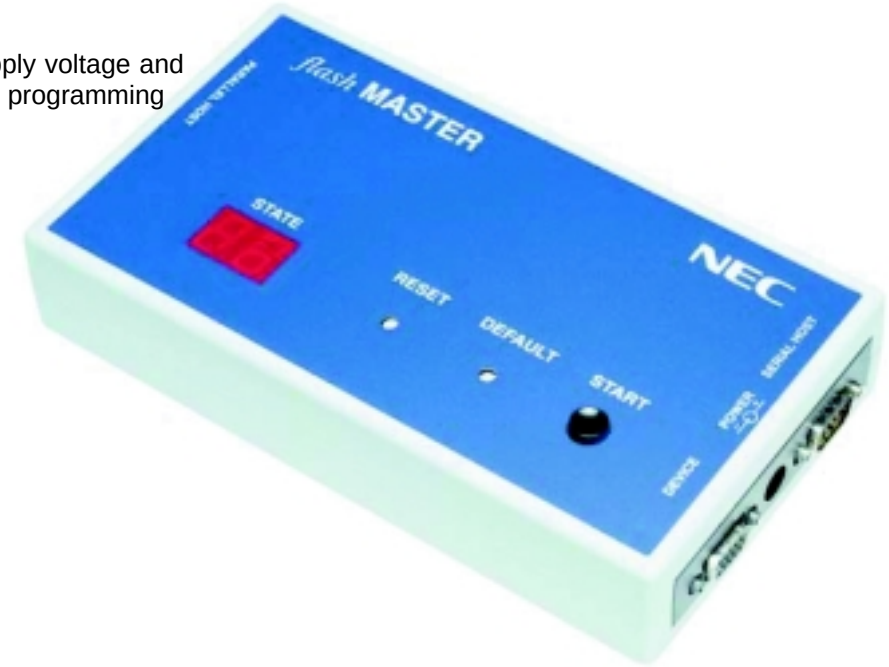
Product Overview

The flashMASTER is a dedicated flash writer for all NEC flash devices. A large on board flash memory allows Flash programming in standalone mode without host connection. The programmer contains two different cable connectors to the target system. The Flash master can erase, write and verify data up to 512 K.

Included in the package:
flashMASTER
Power Supply
Serial Interface cable to target
Serial Interface cable to host
Installation diskettes (3.5")
Manual.

Options:

Description	Order number
V85x Flash Programming adapter	FA-100GC



RISC by NEC: Know-how²

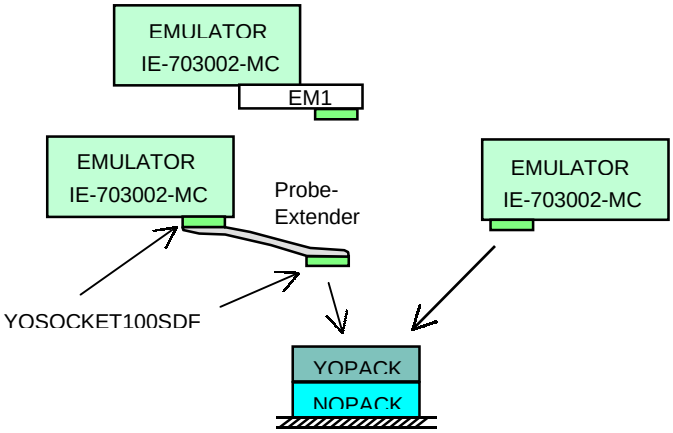
NEC

Programming adapters for flashmaster

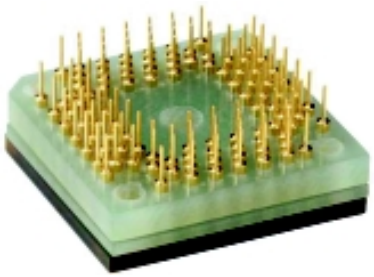
The following Programming adapters are used to program flash-devices of the V850 product family with the NEC flash programmer *flash*MASTER.

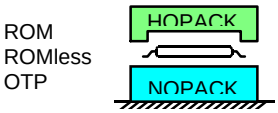
Order number	Package	Devices
FA-100GC	100-pin QFP (14 mm x 14 mm)	V853 V850/SA1 V850/SB1 V850/SF1
FA-100GF	100-pin QFP (14 mm x 20 mm)	V850/SB1 V850/SF1
FA-121FPBGA	121-pin fine pitch BGA (12 mm x 12 mm)	V850/SA1
FA-144GC	144-pin QFP (20 mm x 20 mm)	V850E/MS1 V850E/MA1 ATOMIC
FA-157FPBGA	157-pin fine pitch BGA (14 mm x 14 mm)	V850E/MS1

Sockets

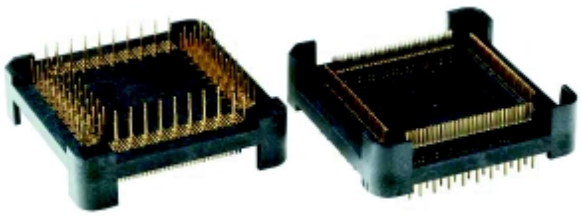


YQSOCKET100SD

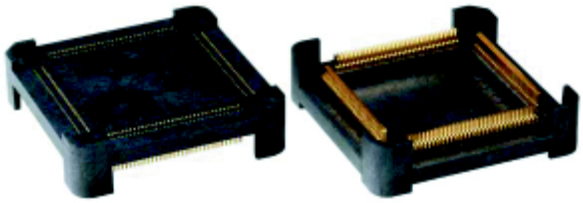




YQPACK144SD



HQPACK144SD



NQPACK144SD

Connector for 100-pin QFP target connection (14 mm x 14 mm, GC-package)

Description	Order number
Connector for target connection	NQPACK100SD
Cover for device installation	HQPACK100SD
Connector for emulator connection	YQPACK100SD
Socket for target connection	YQSOCKET100SDF
Socket for target connection	YQSOCKET100SDF-2

RISC by NEC®: Know-how²

NEC

Connector for 100-pin QFP target connection (14 mm x 20 mm, GF-package)

Description	Order number
Connector for target connection	NQPACK100RB
Cover for device installation	HQPACK100RB
Connector for emulator connection	YQPACK100RB
Footprint adapter (GF to GC)	NEXB-100SD/RB [Note]
Socket for target connection	YQSOCKET100SDF
Socket for target connection	YQSOCKET100SDF-2

Note: for V850/SB1 only

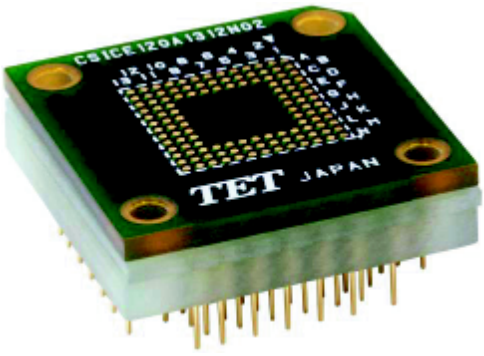
Connector for 144-pin QFP target connection

Description	Order number
Connector for target connection	NQPACK144SD
Cover for device installation	HQPACK144SD
Connector for emulator connection	YQPACK144SD
Socket for target connection	YQSOCKET144SDF
Socket for target connection	YQSOCKET144SDF-2

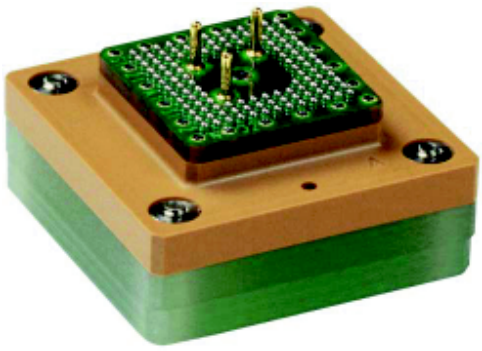
Connector for 121-pin FPBGA target connection

Description	Order number
Connector for target connection	CSPACK121A1312N02
Connector for emulator connection	CSICE121A1312N02

CSICE121A1312N02



CSPACK121A1312N02



Connector for 157-pin FPBGA target connection

Description	Order number
Connector for target connection	CSPACK157A1612N01
Connector for emulator connection	CSICE157A1614N01

Preprocessors/Logic Analyzers/Logic Scope

Personal Line - flexible Logic Analyzer Family for the Windows™ operating system

Features

- Disassemblers without the need of preprocessor hardware for reverse assembly of processor-code with detection and marking of jumps and non executed instructions.
- Easy-to-use graphical user interface operating under Microsoft Windows 3.1x, Windows 95 and NT
- High Level Language Manager for debugging on source code level and trigger on a source code line
- Software interface for user written control and data display programs
- Easy documentation through full compatibility to Windows programs like WinWord
- 32 to 192 channels with external clock rate of 100 MHz, configurable in 16 channel steps sharing either a single clock source or two time correlated clock sources
- 32K memory depth with full channel count, 64K at half the channels
- Internal clock rates up to 1 GHz for 72 channels or 144 channels with 500 MHz
- High impedance 16 channel active logic probes for easy adaptation and minimum loading
- Powerful 15 level trigger with physical trigger outputs to trigger external devices

NEC CPUs Supported

V85x planned

Host Platforms Supported

PC - Windows 3.1x, Windows 95/NT

Object Formats Supported

COFF, ELF/DWARF, IEEE695, Intel OMF386

Product Overview

The Personal Line (PL) Logic Analyzer Family features up to 192 channels per mainframe, a memory depth up to 32K, external clock rate up to 100 MHz, and internal clock rate up to 1GHz. A full range of triggering capability with interactive data stimulus allows the system to work as an ideal ATE system for user specific applications. The system can be stand alone or slaved to a PC running as an application under the popular MS Windows.

Capabilities include full time-correlated dual processor tracing (expandable to 16 processors), powerful Disassemblers and High Level Language Debugging, a Software Interface to control and operate the Personal Line from user written programs and a 10 ns Time Stamp for time correlation of all busses (processors) being monitored.

Personal Line - Analyzer Family

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proLine
Microsoft-Windows based
Real Time Debug Tool

Features

- Connects to any WindowsNT or Win95/98 PC
- Easy GUI with automatic SetUp
- Supports external bus speeds up to 180 MHz
- Supports Multi-Processor systems
- Raw-Data Bus-Disassemblers support State and Timing recordings without Pre-Processor Hardware
- High Level Language Manager for debugging on Source Code Level
- Link to Software Debuggers
- Rapid Support Service for new types of NEC based ASICs and processors
- Remote control from Unix and Windows workstations using VNC
- Records up to 4 Million Events in a single shot to find even the toughest problems
- Programmable Event Search finds the most complex events within the trace
- Flexible target connection technologies

NEC CPUs Supported

V85x, all Processors with external Address-Bus

Host Platforms Supported

PC - Microsoft Windows NT and Win95/98

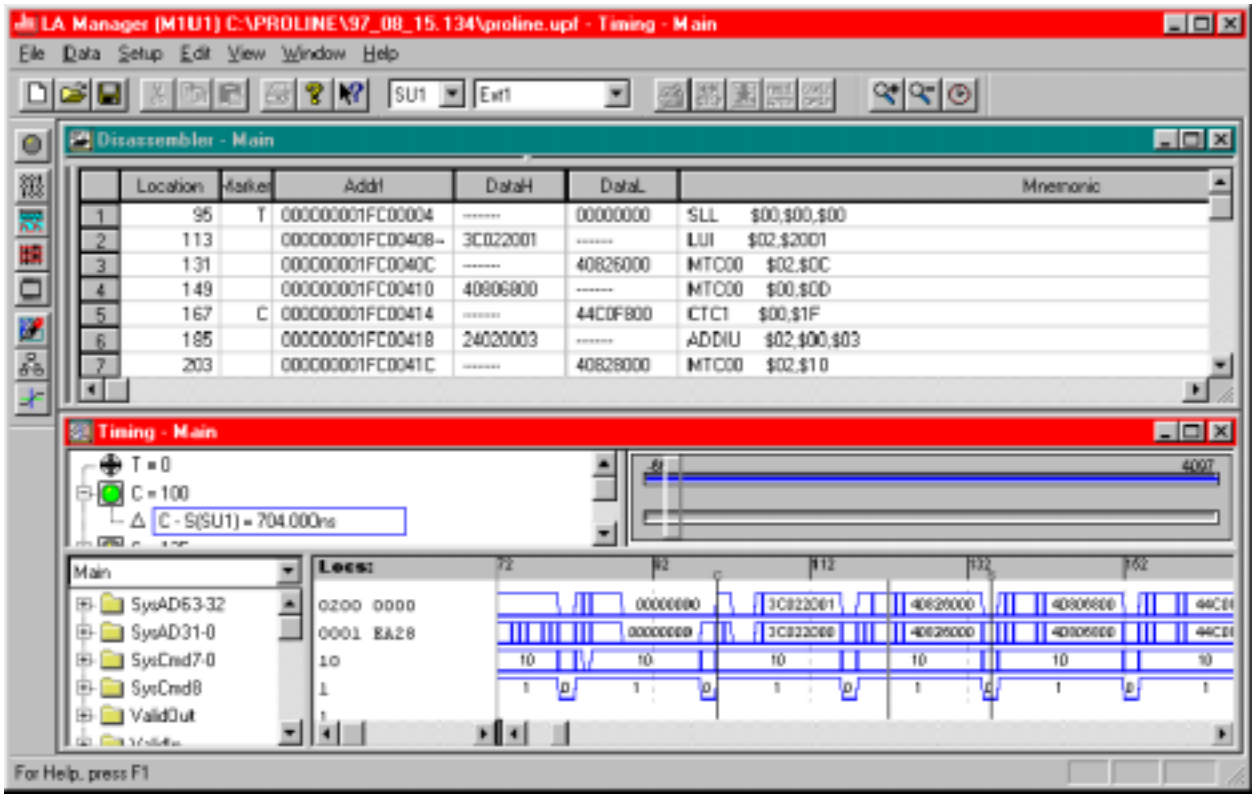
Object Formats Supported

COFF, ELF/DWARF1&2, IEEE695, UBROF

Product Overview

proLine is the latest of dli's Windows based high end logic analyzer systems.
The Hardware supports highest target speeds up to 180 MHz on the external bus, extremely deep memory for ultra long traces as well as most complex Trigger and Trace Conditions at all system speeds.
The Software allows easy handling of most complex situations, offers various time correlated data views, supports easy system SetUp and can be used on any PC even without the instrument connected (e.g. for documentation purposes).
VNC enables full remote accessibility via a local network or the Internet.
Intelligent High Level Language Support provides Source Code Debugging of application programs. including Break/Trigger-Points of the Logic Analyzer on a Source Code Line and correlating the real time trace with the Source-Code.

Member of Controlware Group



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The New TLA 700 Series for Hardware, Software and Integration

The TLA 720 is a benchtop mainframe solution with eleven-slot module expansion capability for high channel count applications.

Features

- Up to 16 Mbits per channel
- Microsoft Windows™ 98 operating system
- MagniVu ™ acquisition technology provides 2 GHz timing resolution on all channels
- 200 MHz state acquisition supports advanced processors and buses
- Simultaneous state and timing analysis through the same probes pinpoints elusive integration faults
- 500 ps timing on all channels
- Four Channel 1 GHz, 5 GS/s DSO provides high fidelity acquisition of analog signals
- Universal source code support for correlating high-level languages with real-time trace
- Performance analysis support for optimising target system performance
- Repetitive acquisition with memory comparison for automated testing
- Remote control using Microsoft COM/DCOM technology supports advanced data analysis

NEC CPUs Supported

V853, V850E

Host Platforms Supported

Windows 98/NT

Product Overview

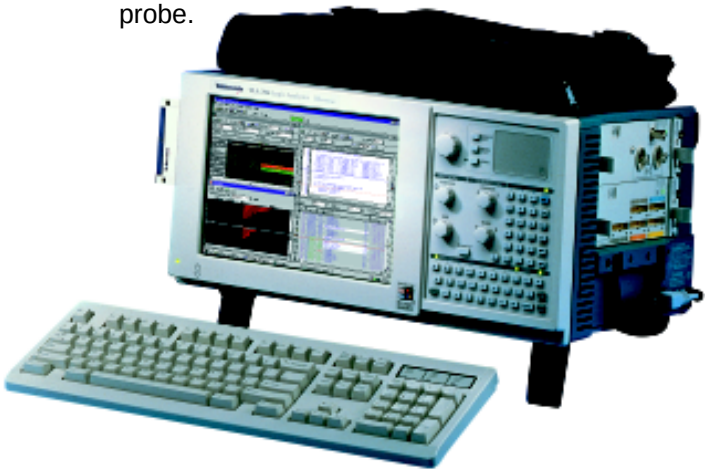
The TLA 700 Series is a new family of instruments developed specifically to address the fast-changing needs of today's digital design engineers. These products bring new technology to bear on the time and design pressures faced by digital system designers. The TLA 700 Series addresses the needs of the entire digital design team. HW developers, HW/SW integrators and embedded SW developers will all find the TLA 700 now provides solutions for those elusive problems that threaten their product development schedules ranging from analog signals to HLL source code. The family consists of portable and benchtop mainframes, logic analyzer modules, DSO modules, and a full line of complementary support products for popular microprocessors and buses.software real-time applications.

Open, industry-standard embedded PC

An open, embedded, Pentium-based PC ensures future expandability and compatibility with a wide range of PC hardware and software.

High Density Probing

The optional P6434 improves ease of connection for debugging today's high-speed microprocessor-based designs by connecting 34 channels with one probe. Both state and timing analysis, through the same probe.



TLA 714 Portable Logic Analyzer

Tektronix®

TLA 700 programmatic interface provides remote control with advanced data analysis
Extensive remote control command set based on Microsoft COM/DCOM technology interfaces seamlessly with Windows applications such as Excel or Visual Basic. Using the TLA 700 as a high-performance data acquisition device, perform advanced data analysis either directly on the TLA 700 or over the network on a remote computer.

Optional 5 GS/s, 1 GHz Digital Scope
Analog data is precisely correlated with digital data so you can see the quality of signals correlated to any problems they cause.

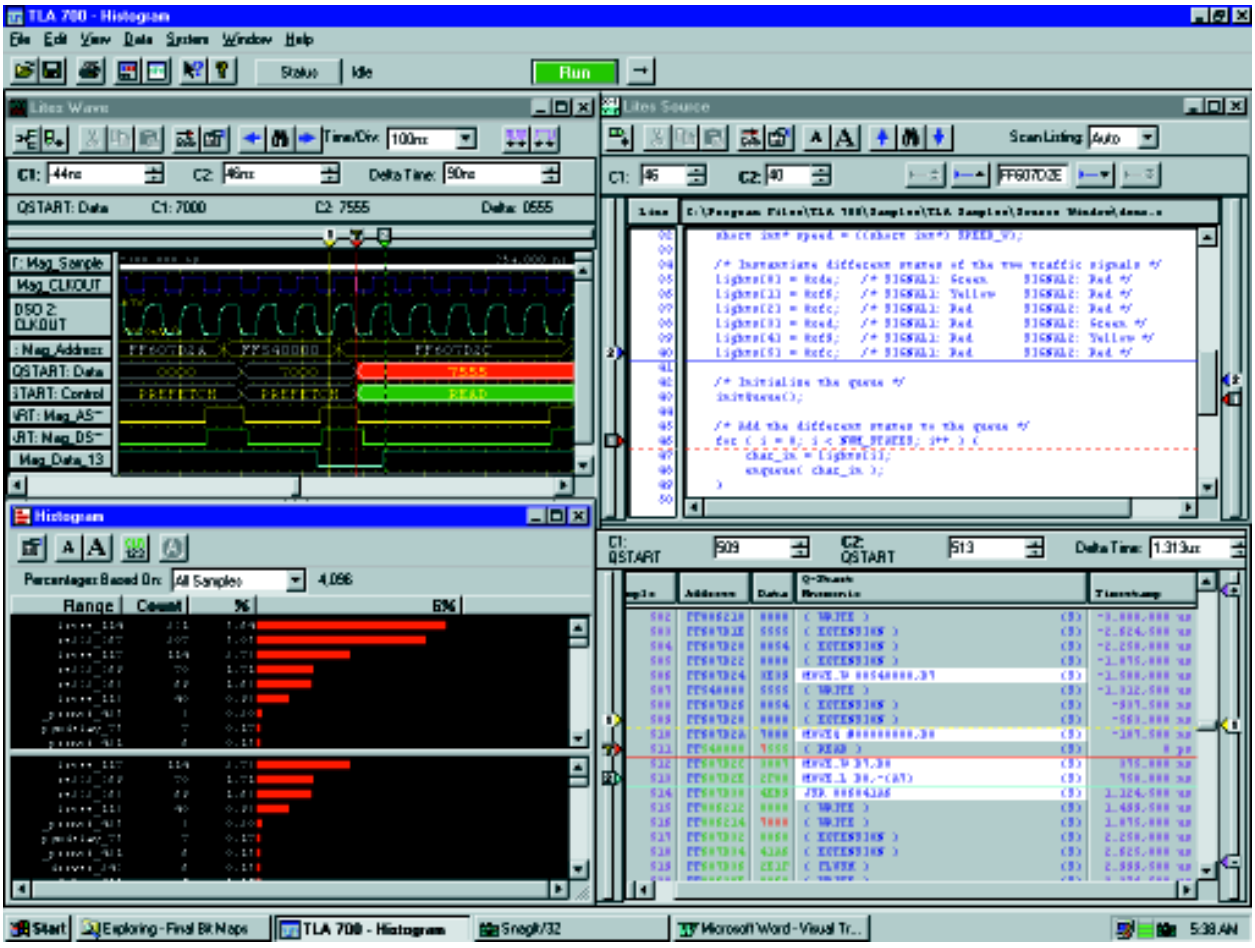
Find elusive problems quickly
Trigger directly on elusive setup/hold time violations over an entire bus. Quickly determine if the cause is intermittent timing violations.

Modular Connectivity
Both the portable and benchtop mainframe share the same modules, so moving instruments around the lab is simple.

Intuitive GUI
Based on Windows™ 98, an interface you already know how to use, so you are productive from the very first time you use the instrument.

State and timing simultaneously through the same probes
The first logic analyzer to offer both 2 GHz timing and 200 MHz state measurements at the same time, on all channels, through the same probes.

View high-level source code and processor mnemonics simultaneously
View processor trace data tightly time-correlated with high-level source code using the information in the object file from your software development environment.



Seeing the big picture from Analog signals to high-level source code:
View waveform, listing, source and histogram windows simultaneously in one large display.

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Logic Scope TLS 216

Features

- 2.5 pF, 1 megaohm Podlet Style FET Probes
- Display Modes: Analog, Timing Diagram and BusFormTM
- <±100 ps Timing Resolution
- 16 Input Channels
- 2 GS/s Simultaneous Sampling on All Channels
- 500 MHz Real-time Bandwidth
- Logic Family Presets for TTL, ECL and CMOS
- Sophisticated Time Qualified Triggering with Four Word Recognizers
- 3-Year Warranty
- Facilitates Hands-free Connection to SMTDevices
- Low Capacitance Probe for Non-intrusive Probing
- Powerful Triggering Reduces Time to Identify Problems
- Flexible Display Modes Simplify
- Recognition of Timing Faults
- High-speed Acquisitions on All Channels
- Facilitate Analysis of Complex System Interactions

NEC CPUs Supported

V853, V850E

Host Platforms Supported

Windows 95/NT

Product Overview

The TLS 216 Logic Scope is a new class of instrument designed to simplify the task of debugging digital hardware. The Logic Scope seamlessly combines in a single instrument the analog acquisition system of a high-speed digital storage oscilloscope (DSO) with the triggering and display systems of a logic analyzer. The 500 MHz bandwidth Logic Scope samples all channels simultaneously at 2 GS/s and has sophisticated time-qualified triggering, a high resolution color display, and an integrated MS-DOS compatible 3.5 inch floppy disk drive.

Sophisticated Triggering to Identify Complex Digital Problems

In addition to edge trigger, most digital signals can be easily captured using pulse, glitch and pattern triggers. The Logic Scope provides two new trigger resources that allow the instrument to directly trigger on common digital circuit behavior. The industry's first time-interval or sequence trigger type monitors the time between two events, allowing the instrument to easily trigger on setup time violations, hold-time violations, or unexpected propagation delay. The powerful "Time-out" trigger type can be used to capture incomplete handshake sequences or to trigger the instrument when the DUT "hangs". All of these trigger types let developers identify channel-to-channel relationships, including 16-Bit patterns and time-related/time-qualified system faults. The Logic Scope's external trigger-input can be used as a "Trigger Arm" to enhance cross-triggering between two instruments, simplifying the task of using a Logic Scope with other test equipment.

2.5 pF, Low-Mass FET Probes Ensure Non-Intrusive Connection

The Logic Scope includes a set of 16 specially designed probes that have extremely low probe-tip mass (1.5 grams) and input capacitance (2.5 pF). The low probe-tip mass ensures that connections made to surface mount and fine pitch ICs will be reliable. The low input capacitance, combined with the 1 mega-ohm input resistance, decreases the effect of the probe on the DUT's operation, allowing very accurate measurements to be made with confidence.
These characteristics are made possible by using a "podlet-style" probe-tip design instead of the "pencil-style" design of traditional oscilloscope probes. Employing the de facto industry standard of 0.1 inch spacing between the signal and ground inputs, each 0.1 inch thick podlet can directly attach to the hundreds of readily available IC adapters and clips.

Applications
Hardware Performance Verification
Multi-channel Data Acquisition
Mixed Signal Analysis
A/D and D/A Analysis
Hardware Timing Analysis

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To find out more information please look at our Test and Measurement website where you can request information to be sent to you by selecting the Contact Tektronix option.

Data Generator
DG2020A * P3410/P3420 * DG2030 * DG2040

Features

DG2000 SERIES (DG2020A, DG2030)

- Output Data Rate to 400 Mbits/s Maximum (200 Mbits/s DG2020A)
- Data Length to 256 K/channel (64 K/channel DG2020A)
- Multiple Output Channels:
  DG2030: 4 or 8
  DG2020A: 12, 24 or 36
- Independent Variable Delay Output:
  DG2030: 4/8, 100 ps res., -5 ns to 18 ns
  DG2020A: 4/8/12, 20 ps res., to 20 ns
- Variable Output Level:
  DG2030: -1.5 V to +3.5 V, 5 Vp-p (50 Ohm)
  DG2020A: P3410 (TTL), P3420
  (-2 V to +7 V,9 Vp-p (open))
- Variable Rise & Fall Time Control (independent) (DG2030)
- Flexible Sequence Control and Data Jump Tri-State Control
- Powerful and Easy-To-Use Data Built-in Editor
- Data Import from Various Instrument and Other Source
- DG-LINK S/W Supports ASCII/CSV Data Import

NEC CPUs Supported

V853, V850E

Host Platforms Supported

Windows 95/NT

Product Overview

DG2020A, DG2030 Data Generators
The Tektronix DG2020A and DG2030 digital data generators combine the high performance needed to test the latest technology devices with unprecedented ease of digital data creation and modification. The DG2020A and DG2030 are used to replicate valid, marginal and erroneous digital conditions that a design could encounter. What separates the DG2000 series from other digital pattern generators is its superior user interface combined with high performance. Everything needed to load, modify, and output vectors is built-in. Capabilities such as advanced sequencing (looping nest), built-in encoding schemes, and flexible editors make the DG2000 Series a powerful addition to your suite of test instruments.

DATA OUTPUT
The DG2020A offers the data rate up to 200 Mbps, 64 k data words length, up to 36 output channels in 12 channel increments and 100 ps timing delay control up to 20 ns function in the portable main frame.
P3410 output pod provides TTL level signal from a grouped pin-header connector. P3420 variable output pod provides 500 mV to 9 Vpp (-3 V to 7 V), 100 mV increment that covers ECL, TTL
CMOS logic level. Output connections consist of independent SMB connectors for each channel. The P3420 is capable of >30 mA of current sourcing, enough for your most demanding applications.
The DG2030 offers the data rate up to 400 Mbps, 256 k data words length, up to 8 output channels in 4 channel increments. Output voltage is from -1.5 V to +3.5 V (250 mVp-p to 5.0 Vp-p) into 50 Ohm that covers most popular technologies like CMOS, ECL/PECL, and TTL. Delay function supports from -5 ns to +18 ns with 20 ps increment. Tr/Tf is able to control independently from 500 ps to 8 ns.

Tektronix®

POWERFUL AND EASY-TO-USE DATA BUILT-IN EDITOR
The powerful built-in Data creation and editing capability allows you to create and modify your data streams quickly and easily. Data can be graphically created using the built-in functions including counters, shift registers, serial data and clocks.

EXTENDED FUNCTIONARY WITH SEQUENCING
Sequencing is a capability that extends the 256 k (DG2030), 64 k (DG2020A) record length and allows external events to control data flow. Each line in the sequencer can be controlled by an external event that can cause a jump to a different block of data. The DG2000 series can have up to (2000: DG2020A, 4000: DG2030) jumps (one per line) at the full clock rate and has specified latency that can be accounted for. External, Event and Inhibit, that can control the flow and impedance of the sequence.

IMPORT THE DATA FROM OTHER SOURCES
Getting data into the DG2000 Series is simple with multiple import options from several sources. Data can be imported from several Instruments including the Tektronix TLS216 logic scope, GPX logic analyzer, 2000 Series arbitrary waveform generators, and TDS Series scopes. To import data from other sources, a comma separated variable (CSV) format is supported. DG-Link application program for the PC (Windows* 95 environment) supports ASCII file format vector import such as TLA700 Logic analyzer or logic simulation software output vector, which can be converted to DG2000 Series file format and send via GPIB or floppy disk.

Applications
Replicate Vector Data from Simulator
Characterize a Device's Timing and Amplitude Margin
Replicate Data from Unavailable Part of the System
Inject Infrequent Faults to Test Fault Tolerance
Semiconductor (ASIC/FPGA/DAC)
Storage Media Write Data (HDD/FDD/MO/DVD)
CCD (Area, Liner) Image sensor
Printer, Copy (Color/Laser) Digital Graphic Data
LCD (STN/TFT/MIM) Display Device Drive/Control
Logic Board/Bus Simulation

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To find out more information please look at our Test and Measurement website where you can request information to be sent to you by selecting the Contact Tektronix option.

www.tek.com/Measurement/

In-Circuit Emulators

ADViCE real-time in-circuit emulators

Features

- Real-time, non-intrusive in-circuit emulation for 8 to 32 bit processors
- High performance, modular architecture offers emulation, debug, analysis and reporting for embedded systems development
- Supported on Windows PC and UNIX workstation hosts
- High speed serial, GPIB and ethernet connections
- Supports 256 KB to 4 MB emulation memory, fully emulates on chip memory
- Up to 64 pre-execution breakpoints
- 8 K trace with single continuous or multi trace mode
- Trace of code at bus, assembler or C-source level including external bus and time stamp
- 6 programmable trigger events as a combination of address, data, access type, external signal inputs can detect precise combinations of events
- Evants can be used for program break, trace trigger or performance analysis trigger
- Events can be cascaded sequentially or in a state machine mode to detect “if one then another” conditions
- C-source, assembler and mix mode program display in a powerful multi-window user environment
- Run, step, step-in, step-out, go to execution modes in C and assembler
- Powerful command language for macro and batch file execution
- User configurable function keys, short cut keys
- Profile analysis provides graphical and statistical information on processor overheads
- Performance analysis provides graphical and statistical information on function execution time
- Code coverage analysis provides graphical and statistical information on software test coverage
- Adaptor provides synchronisation of multi event sequencing to external device (eg storage scope)

NEC CPUs Supported

V850/SA1, V850/SB1,V850E/MS1,V850E/MA1,V853

Host Platforms Supported

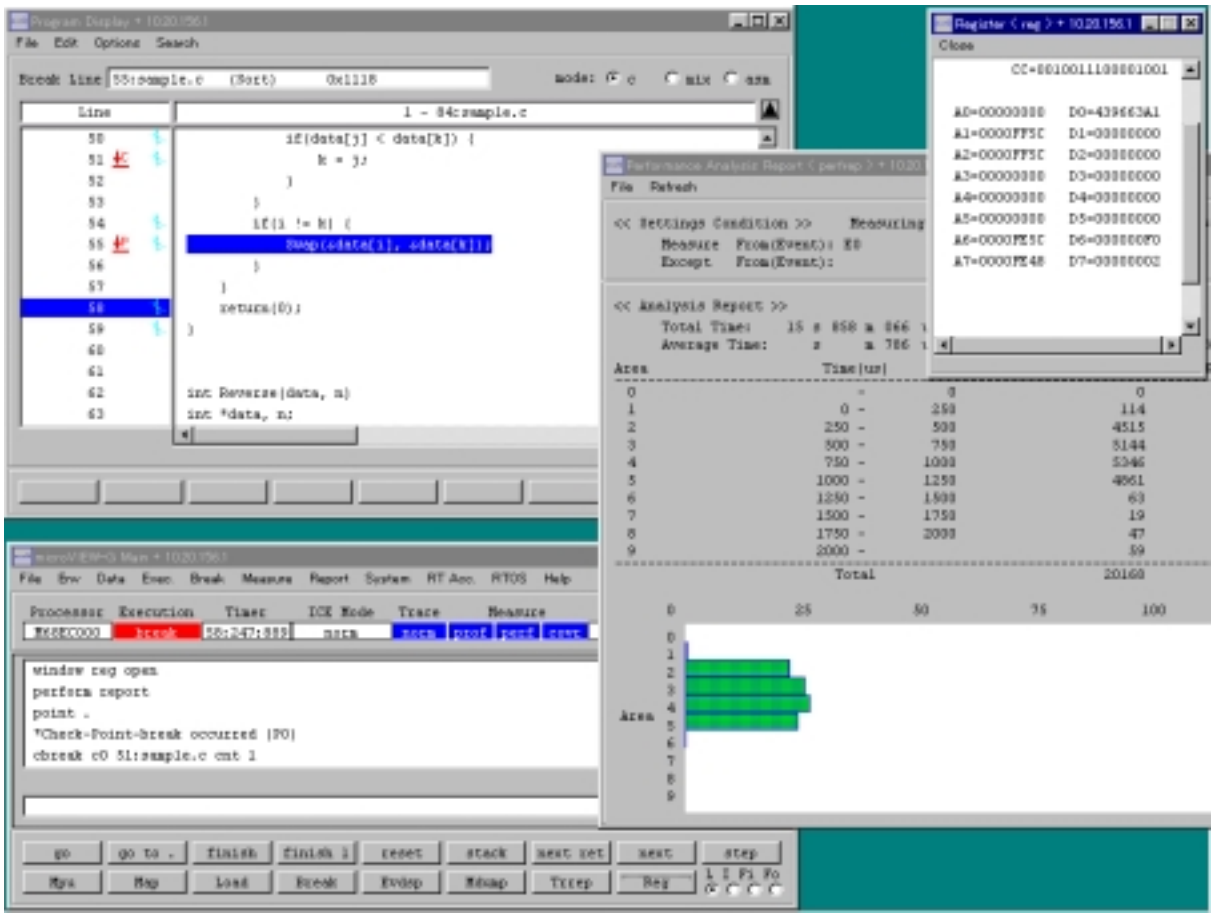
PC with 386 or higher, RS-232C, GPIB, Ethernet

Product Overview

The ADViCE In-Circuit emulator is manufactured by Yokogawa Digital Computer Corporation, Japan. Through close links with NEC, YDC have developed an emulation environment closely allied to their requirements.
The modular architecture allows the configuration for a specific processor to be changed with minimal impact to the overall system.

ASHLING
THE DEVELOPMENT SYSTEMS COMPANY

YOKOGAWA



Common across the range is the MicroView-G source level debugger and user interface

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http://www.ydc.co.jp/micom/index_E.htm
E-Mail:info@advice.ydc.co.jp

Distributors in Australia, Austria, Belgium, Hungary, Israel, Italy, Korea, Malaysia, Netherlands, Singapore, Spain, Sweden, Taiwan, Turkey

AF201 Flash Micro Programmer

Features

- Operates in stand alone mode or driven remotely via PC Windows application
- Read, Write, Modify to buffer memory, Blank Check, Erase, Program and Verify to flash
- Programs can be stored locally or on host PC
- High speed download/programming with optimised programming algorithms for maximum performance
- Simple cable connection to target system
- When operated stand alone programming can be a one step process
- When operated in remote mode control can be fully automated, included in an ATE environment for complete test, debug and programming
- Multiple AF201s can be controlled from one PC for high volume manufacturing environments

NEC CPUs Supported

V853, V850E

Host Platforms Supported

PC with 386 or higher, RS-232C, Ethernet

Product Overview

The AF201 from YDC has been developed to support in-target programming for microprocessors / microcontrollers with on-chip flash.

Designed to be modular and general purpose, the AF201 accepts a PCMCIA memory card which defines what processor configuration is to be supported and can also be used to store several program files. Connection to a target is via simple cable plug or clip on probes.

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Ashling Microsystems Ltd reserves the right to alter product specifications at any time and without notice.
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NetICE-R™
LAN-based ROM Emulator

Features

- Integrate the power of a local area network into the entire development process
- Add fast code download capability to your JTAG emulator via Ethernet
- Up to 8 Mbyte of ROM or RAM emulation
- Supports 8, 16, and 32 bit data bus widths
- Replaces the target Flash, EPROM, or RAM memory during debug. Simple and easy to use.
- Target processor independent
- Requires no hardware or software resources from target CPU
- Enable JTAG emulators and monitor programs to set software breakpoints in ROM space
- Retain ROM content after power is cycled to emulate real-time power-up target boot environment.
- Flash/EPROM emulation speed of up to 45 ns access time.
- Connect via standard ROM socket or via a special test connector
- Assortment of standard ROM cables available
- Supports standard (5 V) and low-voltage (3 V) targets
- ROMLoad utility software for direct hex file download over the network
- ROMLoad software supports Windows 95/98/NT, HP-UX, and Solaris
- ROM Function 'C' Library for ROM set-up and code download from remote applications

NEC CPUs Supported

V85x

Host Platforms Supported

Windows 95/98/NT

Product Overview

The NetICE-R is an easy to use ROM emulator that was designed to provide a means for fast download of ROM-based code over the Ethernet to the user's real-time/embedded target system.
The NetICE-R is a processor independent tool that can be used along with other development tools such as JTAG emulators, ROM monitor programs, embedded operating systems, etc. The NetICE-R adds fast download capabilities to inherently slow JTAG emulators, provides remote host to target connectivity, and eliminates the need to program Flash or EPROM devices every time that new target software is generated.
The target board is connected to the ROM emulator via a cable. A standard cable either plugs into the target ROM socket or a special cable is available that connects the address, data, and control signals of the target ROM device to the NetICE-R's 50-pin, SCSI-2-type connector.
Once connected to the target board, the user can download standard hex files quickly and easily over the Ethernet interface using the ROMLoad utility software that supports Windows 95/98/NT and UNIX host platforms.

ROMLoad Utility

The ROMLoad utility software is used for remotely setting-up the NetICE-R memory configuration and for downloading hex files from the PC to the NetICE-R memory. The software is provided with a graphical user interface for Windows 95/98/NT and as a command-line utility for HP-UX and Solaris. Motorola-S-Record format is a standard format for hex files and is generated by most software development tools such as 'C' compilers and assemblers. S-Record files are typically used when programming EPROM/Flash devices using a standard PROM programmer. The ROMLoad utility eliminates the need for EPROM/Flash device programming during the development phase of the project and enables the user to quickly and conveniently download new hex files to the emulation memory.

ROM Function Library

For users that want to develop their own host application and not use the provided ROMLoad utility, the NetICE-R is shipped with a ROM Function Library (RFL) Dynamic Link Library for use with 32-bit Windows program development. A summary of the RFL functions is provided below:

JTAG_Connect()
This function will connect the client application with the NetICE-R. The socket number of the connection is returned as an informational item.

CORELIS

JTAG_Disconnect()
This function will disconnect the client application from the NetICE-R.

ROM_Configure()
This function configures the ROM emulation module.

ROM_Control()
This function controls the enabling of the host and target interfaces.

ROM_Download_File()
This function downloads a file into the ROM emulation memory.

ROM_Fill()
This function takes one item and writes it to a specified number of sequential locations in the ROM emulation memory.

ROM_Pod_Info()
This function returns binary data describing the pod configuration of the detected ROM emulator boards.

ROM_Read()
This function reads data from ROM emulation memory.

ROM_RFL_Version()
This function returns a zero-terminated ASCII string, which provides the version number of the ROM Function Library DLL.

ROM_Version()
This function returns a zero-terminated ASCII string, which provides the version level of the ROM emulator.

ROM_Write()
This function writes data to ROM emulation memory.

LAN Standards
The NetICE-R fully supports the popular TCP/IP protocol. It is possible to connect the NetICE-R to various networks as long as the connection between the user's workstation and the NetICE-R uses the TCP/IP protocol.

Configurations
The NetICE-R is available in four different emulation memory configurations. The user has a choice of ordering either one or two built-in ROM emulation pods with pre-configured emulation memory of one or two mega-words. Bus width options are 8, 16, or 32 bit. Consult the factory for any other custom configurations.
Each emulation pod is designed to replace a particular target ROM (Flash/EPROM) device. The ROM emulation pod comes with pre-configured memory of either one or two mega-words deep and is software compatible to emulate either 8 or 16 bit wide memory.
The NetICE-R unit with two ROM emulation pods can replace two ROM devices in the target thereby providing ROM emulation of wider target memories.
In addition, the emulation memory can be write-protected from target write cycles and the NetICE firmware is in flash memory and is field upgradeable.

Specifications

Host Interface

Ethernet:
10-Base-T or 10-Base-2
Protocol:
TCP/IP
RS-232:
1200 thru 115.2 K baud

Emulation Memory I/O

Output Voltage Compatibility:
3.3 V or 5 V tolerant
Output Current (max.):
IOL = 24 mA
IOH = -24 mA
Input Voltage Compatibility:
3.3 V or 5 V tolerant
Input Current (max.):
IIL = -5 to 5 µA

Physical Size

5.57”Wx7.45”L x 1.52”H

Connectors

JTAG and Digital I/O Connectors:
50-pin SCSI II type connector
Parallel Port Connector:
DB-25
Serial Port Connector (unused):
DB-9
10-Base-T Connector:
RJ-45
10-Base-2 Connector:
BNC

Front Panel Indicators

POWER:
Green LED indicates that power is supplied to the card
READY:
Green LED indicates that power-up self-test passed

Back Panel Indicators

TX/RX:
Red LED indicates LAN data transmit/receive
LINK:
Red LED indicates that the 10-Base-T link is functional

Power Consumption
15 W, maximum

Operating Environment
Temperature:
0 °C to 55 °C
Relative Humidity:
10% to 90% non-condensing

Storage Environment
Temperature:
40 °C to 85 °C
Relative Humidity:
10% to 90% non-condensing

Supplied
- NetICE-R ROM Emulator
- ROMload Utility
- Emulation Function 'C' Library
- User's Manual
- Power Supply

Emulation Memory
1, 2, 4, or 8 MB

Option 1/1M – One pod, 1M x 16 or 1M x 8
Option 2/1M – Two pods, 1M x 16 or 1M x 8 each
Option 1/2M – One pod, 2M x 16 or 2M x 8
Option 2/2M – Two pods, 2M x 16 or 2M x 8 each

Target Access Speed
45 ns, minimum

Data Bus Width Support
8/16/32 bits

Supported ROMs
All popular 8 and 16 bit EPROMs and Flash devices

Electrical Interface Support
5 V/3.3 V

Available ROM Probe Support
24-pin DIP
28-pin DIP/PLCC
32-pin DIP/PLCC
40-pin DIP
44-pin PLCC
Others

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Fax: +(33) 1-60-11-98-09

TRACE32-FIRE
Fully Integrated RISC Emulator

Features

- Universal In-Circuit Emulator for 16, 32 and 64 Bit RISC Processors
- Bond-Out Technology
- Emulation of internal ROM
- Unlimited Hardware Breakpoints
- Up to 8 MByte dual-ported emulation memory
- Coverage Analysis (C0, M0 and Access)
- High-speed link via Ethernet or LPT
- 100 MHz Real Time Trace and Trigger
- Up to 400 Trace Channels
- Free programmable Trigger System (Bus and HLL)
- Integrated High-Level Language Debugger
- Integrated RTOS Debugger
- Performance Analysis and Statistic Functions
- Powerful graphical Analysis Functions
- Timing and Port-Analyzer

NEC CPUs Supported

V851, V852,V853, V850/SA1 and V850/SB1

Host Platforms Supported

PC (Windows 3.11/95/NT), SCO-ODT, SUN3, SPARC, DEC-ULTRIX, VAX-VMS, ALPHA-OSF1, ALPHA-VMS, HP9000/300/400/700, AIX

Product Overview

The TRACE32 tool suite provides a complete set of development and testing tools. The advanced modularity of TRACE32 makes it very easy to upgrade the systems to future needs. TRACE32 works with the highest variety of host interfaces.
TRACE32-FIRE Fully Integrated RISC Emulators are the leading edge tools that guarantee non-intrusive emulation at highest speeds. The concept of total integration guarantees the highest quality of support and system reliability. The TRACE32-FIRE PROBE can be used in stand-alone mode and can be upgraded with the more sophisticated TRACE32-FIRE Back End if and when it becomes necessary. The communication link to the host is done by a printer port or Ethernet allowing a high-speed transfer.
The compatibility that exists between the TRACE32-FIRE and Lauterbach´s TRACE32-ICD entry level debugger opens up a wide range of application areas for these tools. Moving from one tool to the other can be done seamlessly without having to learn a new user interface.
TRACE32-DEBUGGER - the highly intuitive software interface offers seamless integration with the entire range of TRACE32 hardware. It is completely configurable by the user, no other system offers more flexibility.

LAUTERBACH

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Mr. Phil Johnson

In-Circuit-Emulators for the V85x family

Features

- One emulator for the V85x family and one for the V850E family
- Extremely light in weight and compact
- 66 MHz (target)
- Emulator supply voltage of 5 V
- Operation voltage of target device 3 to 5 V
- Support for source level debugging
- Time measurement function
- Trace
  32 k frames x 150 bits trace buffer
  Time, system registers, opcode and memory accesses are traced
  Trace can be controlled by events (e.g. start/stop)
- Break
  Breakpoints can be set in source code or by events
  Forced break
- External logic probe for trace and break setting

Host Platforms Supported

PC: Windows 95/98/NT
SUN OS, Solaris, HP-UX

Product Overview

The NEC In-Circuit-Emulators are develpment tools that help the developer to efficiently debug hardware and software for microcontrollers of the V850 family. They incorporate functions such as break and trace using events, a code coverage function for program performance evaluation and a timer function.
Memory contents can be displayed and an external logic probe can be connected.
When debugging a V850-family system the dedicated option board for the V850 microcontroller that is used in the system has to be connected to the basis ICE. This set of basis ICE and option board is then connected to the target system for debugging.

Ordering information:

IE-703002-MC for V853, V850/SA1, V850/SB1 or V850/SF1
IE-703102-MC for V850E/MS1
IE-V850E-MC-A for V850E/MA1
IE-V850E-MC for Atomic

RISC by NEC: Know-how²

NEC

Required parts:

- **Power supply:**

Description	Order number
Power supply for emulator	EB-PowerFW7301/05

Generates the 5V voltage supply for the IE-703002-MC or IE-703100-MC

- **PC adapter:**

Description	Order number
PCI-bus PC adapter card for emulator	IE-70000-PCI-IF-C

Options:

- **Emulation boards:**

Description	Emulator used	Order number
Emulation board for V853	IE-703002-MC	IE-703003-MC-EM1
Emulation board for V850/SA1	IE-703002-MC	IE-703017-MC-EM1
Emulation board for V850/SB1	IE-703002-MC	IE-703037-MC-EM1
Emulation board for V850/SF1	IE-703002-MC	IE-703079-MC-EM1
Emulation board for V850E/MS1	IE-703102-MC	IE-703102-MC-EM1
Emulation board for V850E/MS1-	IE-703102-MC	IE-703102-MC-EM1-A
Emulation board for V850E/MA1	IE-V850E-MC-A	IE-703107-MC-EM1
Emulation board for Atomic	IE-V850E-MC	IE-703123-MC-EM1

The IE-7030xx-MC-EM1 are optional boards for the NEC In-Circuit-Emulators. By using the NEC In-Circuit-Emulators hardware and software can be debugged efficiently in system using the dedicated device.

- **Extension probe:**

Description	Order number
Extension probe (100-pin QFP) for V85x	SC-100SD
Extension probe (144-pin QFP) for V850E	SC-144SDN

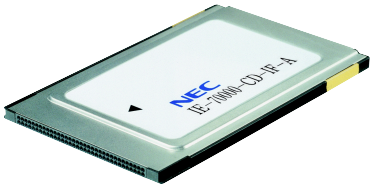
Used to connect emulator or emulation board to the target system via flex strip.

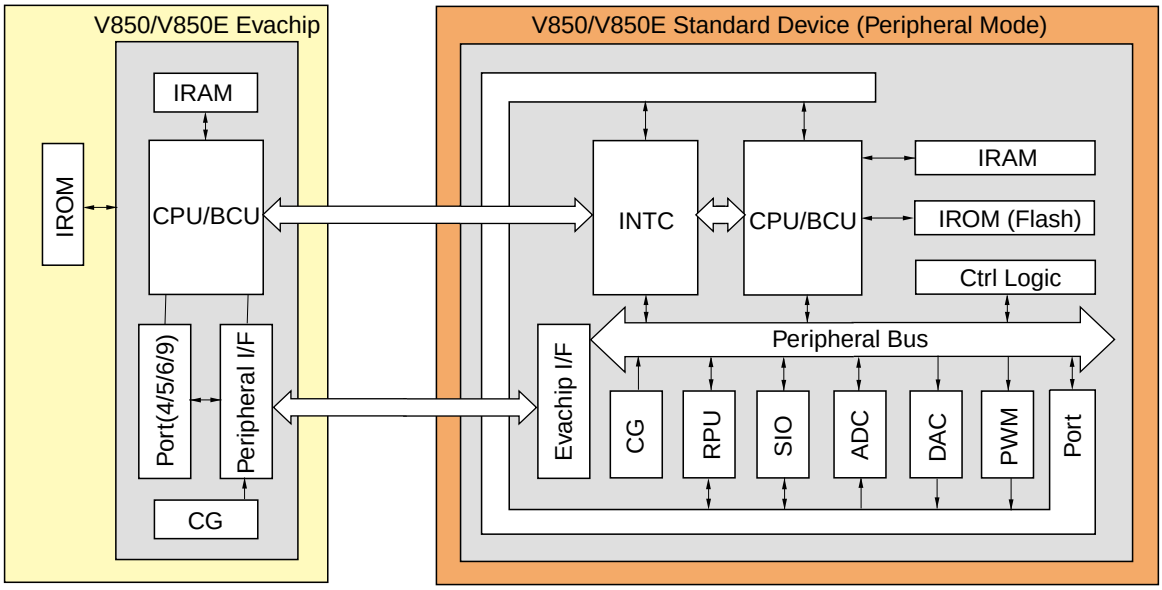
- **PCMCIA adapter:**

Description	Order number
PCMCIA adapter	IE-7000-CD-IF-A

The PCMCIA adapter offers the possibility to connect the V850 In-Circuit-Emulators to a Laptop computer that has got a PCMCIA slot.

PCMCIA adapter





In-Circuit-Emulator Schematic Overview

RTE-TP series
N-Wire interface Real Time Emulator

Features

- Processor On Board emulation function. Emulation is done by using real processor that has N-Wire/JTAG interface. Therefore execution of processor is stable and could provide high transparent emulation.
- Emulation Memory is supported. ROM emulation function is supported (MAX 4MB). Several types of ROM probe are prepared (option).
- Real time trace function is supported. Trace information conforming to N-Wire specification is recorded into memory.
- High speed download
- Various host interface are prepared. PCI interface, PCMCIA interface and LAN interface are supported.
- High level language debugger. High performance and high level language debugger, MULTI (GHS Debugger) is available to use.

NEC CPUs Supported

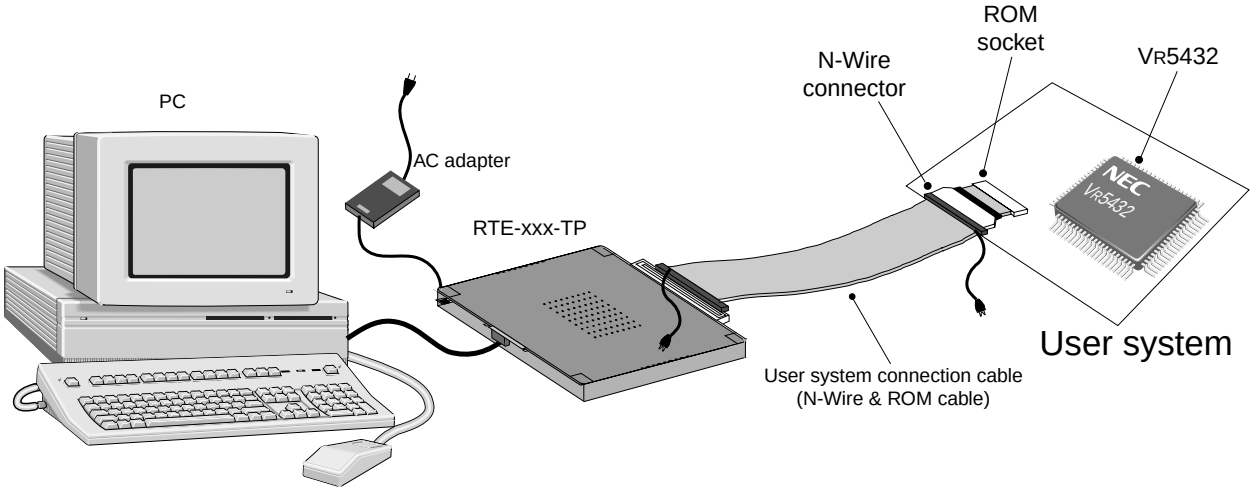
V850E

Host Platforms Supported

Windows95/98/NT

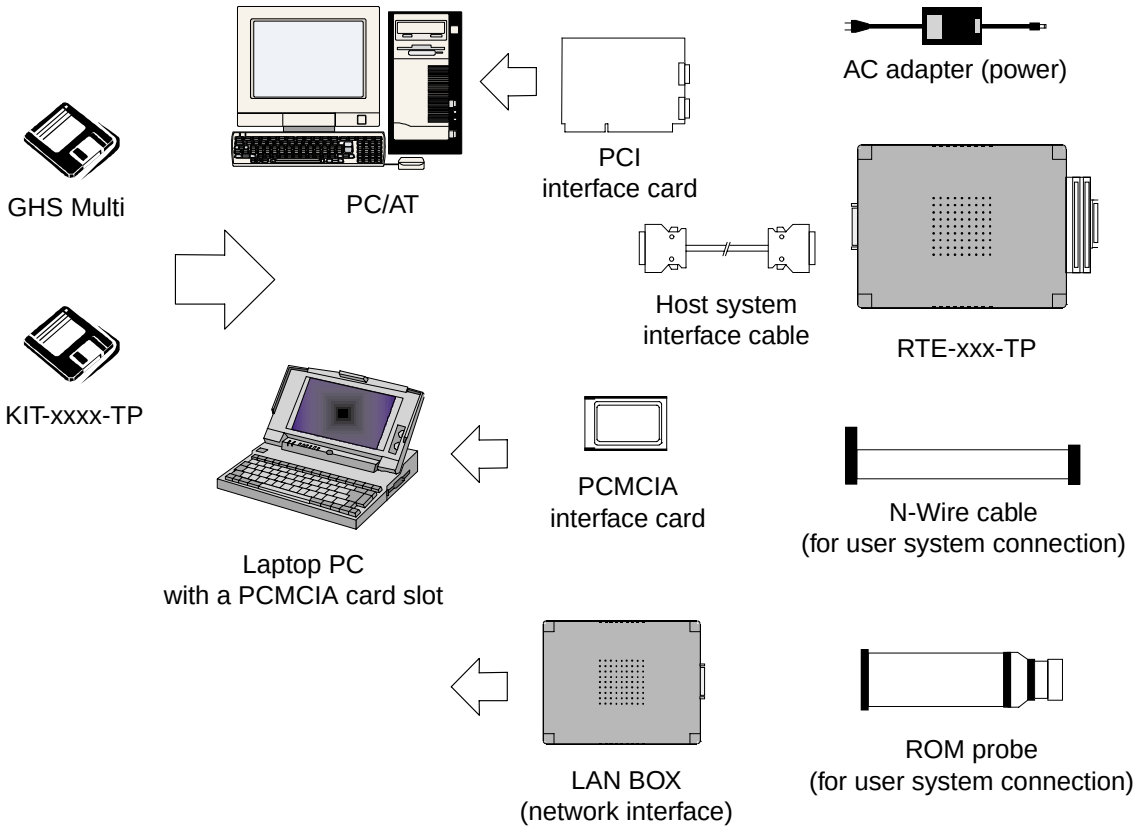
Product Overview

RTE-TP series is the emulator of NEC microcomputer which has DCU (Debug Control Unit) inside.



RISC by NEC: Know-how²

NEC



GHS Multi:	High level language debugger for RTE-xxxx-TP
KIT-xxxx-TP:	Control software for each software
PC/AT:	PC capable of running Windows95/98/NT
PCI interface card:	PCI bus interface card
PCMCIA interface card:	TYPEII card (version 2.1 of the PCMCIA specification or later
LAN BOX:	LAN supporting PC (10 base-T)
Host system: Interface cable:	Cable for connection RTE-xxx-TP to the host card
AC adapter:	Power supply
RTE-xxx-TP:	N-Wire ICE
N-Wire cable:	Cable for connection to the user system for debugging
ROM cable:	Probe for ROM emulation

EDA & Software Modeling Tools

Affirma™ HW/SW verifier

Features

- Tight integration with NC simulators for fast simulation
- Advanced capabilities for DSP/micro-processor convergent designs
- Efficient verification through links to system testbenches
- Open model and debugger APIs

Supports major Verilog Simulators

NEC CPUs Supported

V851, V853

Host Platforms Supported

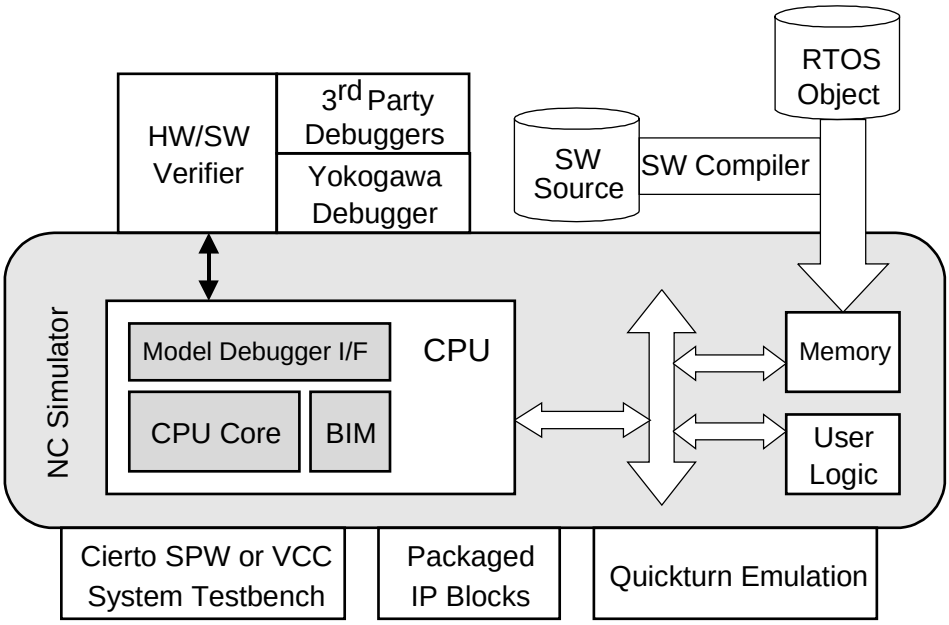
Sun Solaris 2.5.1, HP UX 10.2

Product Overview

The Affirma HW/SW verifier is a proven solution for HDL simulator integrated co-verification at over 40 companies. Its unique architecture positions the HDL simulator as the central control unit for co-verification. This simplifies the model integration task and opens the solution to the widest range of processor models.

Because of the tight integration, the HW/SW verifier can support up to eight processors in a single simulation process. It also uses the tight integration to access the SPW direct and OMI based links for system model integration and system testbench integration. The processor models are directly integrated to the simulator through PLI, OMI, or directly in HDL form. The API for model integration is available to customers and model developers and allows for the fastest model integration process.

HW/SW co-verification is focused on insuring that the functionality proven at the system level integrates correctly at the implementation level. As most of the integration issues involve signal timing or sequence, the HDL simulator focused Affirma HW/SW verifier provides the best solution to resolve these difficult integration problems.



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VirtualICE ™

The Proven Co-design and Co-verification Environment for System LSI and ASIC

Features

- Precise timing simulation of real CPU
- Applicable to multiple CPU/DSP System LSI
- Supports multi-vendor compilers including NEC's
- Supports major Verilog Simulators
- High simulation speed without sacrificing accuracy

NEC CPUs Supported

V850 family
V851, V853 (RTL, Behaviour)

V850 ASIC CORE family
Na851CA, NA853CA (Behaviour)

V850E ASIC CORE family
NB85E (RTL, Behaviour)
NB85EC (Behaviour)

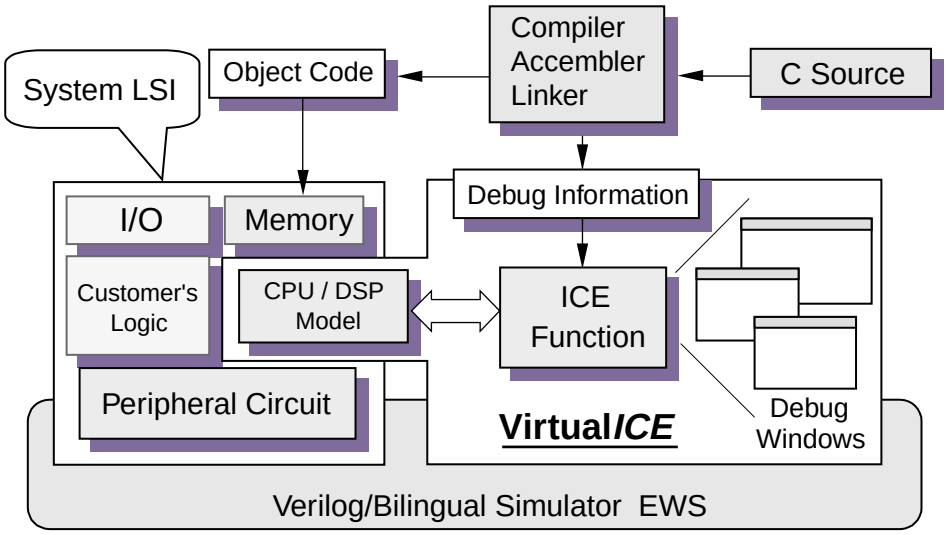
Host Platforms Supported

Sun Ultra Series or SPARC Station,
Solaris 2.5.1 or later

Verilog Simulator:
Verilog-XL, VCS,
ModelSim EE/PLUS,
NC-Verilog

Product Overview

VirtualICE offers design and Verification flexibility for system-on-a-chip design. The advent of deep sub-micron technologies and the resulting system-on-a-chip capabilities have engendered new design requirements. The ability to embed programmable computing elements within a chip mandates the simultaneous development of hardware and software. Time-to-market pressures and short product lifetimes demand efforts to reduce the development cycle while simultaneously minimizing the risk of an ASIC re-spin. Current design paradigms exacerbate the situation by separating the hardware and software development. Any method of hardware/software co-design should have the full capabilities of both hardware and software debug facilities, with full function compatibility and the ability to use real object code.
Yokogawa offers solutions for hardware and/software co-design. VirtualICE for Verilog simulators facilitates hardware/software validation in all phases of development. The CPU model of VirtualICE (written in Verilog HDL) merely simulates the behaviour of hardware with accuracy timing. The CPU model fetches and executes actual instructions from memory that is generated by the actual compiler. As a natural consequence, the result of the simulation is the same as if the software were running on the actual CPU with accuracy timing. It is very simple and the best way for hardware and software co-design. VirtualICE reduces the risk of new design by testing the hardware/software interfaces early in the development cycle.



Objective

Board level simulation
Function verification and test vector extracting in the design phase of ASICs
Targetless firmware debugging
Estimation of system performance
Development of system on silicon chip

Target system

Hard disc and DVD controllers
Printers
Multi-media equipment
Cellular phone and personal digital assistants (PDA)
Car navigation systems

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www.yokogawa.co.jp/Eda/index_e.html

Development Support Products

NEC Workshop Program 2000

Workshops '2000 NEC European Support Centre

NEC provides comprehensive workshops on a wide range of its Microproducts at the European Support Centre.

The 2-3 day courses provide participants with information on the CPU architecture of the device family, differences between family members and functionality of the on-chip peripherals.

Hands on sessions with development tools provide participants with practical experience. The workshops are targeted for technical/design engineers. All the workshops are held in English at our European Support Centre in Düsseldorf. Additional workshops at customer premises, or at local NEC sales offices, can be arranged on request.

For information on booking and detailed workshop agenda, please call +49(0)211-6503-216 or simply return the fax sheet, for further information.

Workshops	Date
75X/XL 4-bit Single Chip Microcontroller	On request
78K0 **78K0S** 8-bit Single Chip Microcontroller	15.02. 16.02.2000 09.05. 10.05.2000 12.09. 13.09.2000 05.12. 06.12.2000
78K4 16-bit Single Chip Microcontroller	28.03. 29.03.2000 05.09. 06.09.2000
V850 32-bit RISC Microcontroller	01.02. 02.02.2000 03.05. 04.05.2000 30.08. 31.08.2000 14.11. 15.11.2000
DSP/SPX	On request
VR Series 64-bit RISC Microprocessor	14.03. 16.03.2000 17.10. 19.10.2000

The latest update on our NEC Workshop can be found on our web site: **www.nec.de** in the "News" section.

RISC by NEC: Know-how²

NEC

Workshops '2000

Fax + 49(0) 211-6503-533

NEC Electronics (Europe) GmbH
Technical Product Support

Please send me further information on the following workshops:

- ☐ 75X & 75XL
  4-bit Single Chip Microcontroller
- ☐ 78K0 & 78K0S
  8-bit Single Chip Microcontroller
- ☐ 78K4
  16-bit Single Chip Microcontroller
- ☐ DSP & SPX
  Digital Signal Processor
- ☐ V850
  32-bit RISC Microcontroller
- ☐ VR Series
  64-bit RISC Microprocessor

Company .....

Name .....

Department .....

Street .....

PO box .....

City .....

ZIP code .....

Country .....

Date: ..... **Signature:** .....

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CANalyzer

Features

Products:

- Tool for development of CAN bus systems
- Tool for CAN applications in the automotive field
- Tool for CAN applications in the automation field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V85x

Host Platforms Supported

Windows 9x/NT

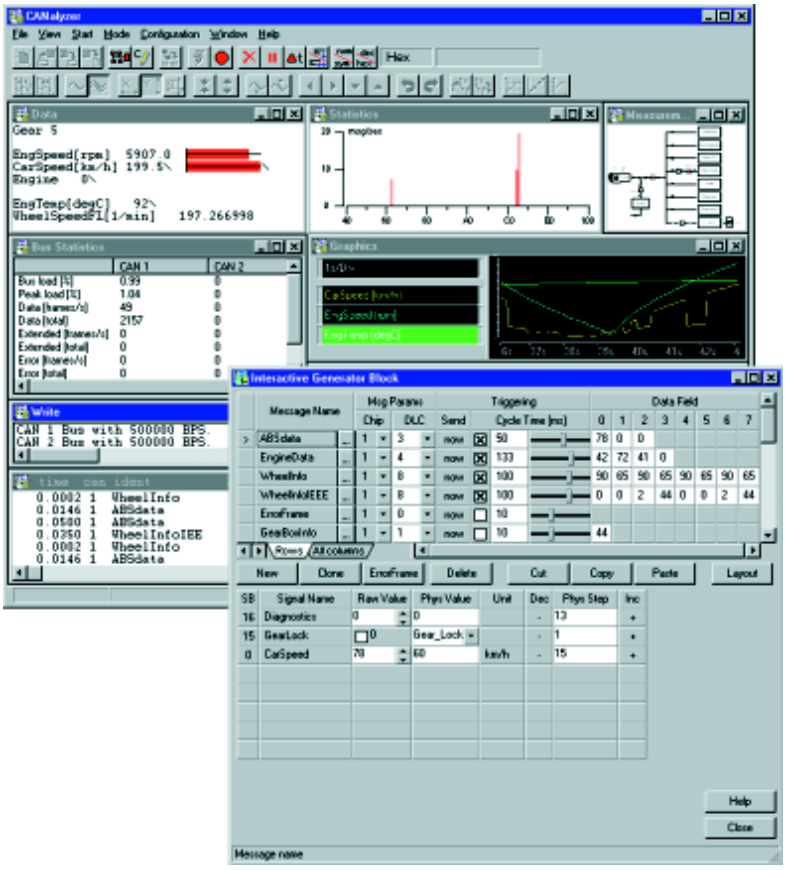
Product Overview

CANalyzer is a universal development tool for CAN bus systems, which assists in observing, analyzing and supplementing data traffic on the bus line. All requirements, from the first trial runs with CAN to error searches in complex problem situations, are covered by powerful functions and the free programmability. The CANalyzer is operated on the basis of a data flow chart, illustrating the data flow from the CAN bus over the PC-board to the various evaluation windows and to the logging file. To the highlights of the CANalyzer belongs - next to the simple and intuitive operation - the CAPL programmability and the possibility to place function blocks at any point in the data flow diagram.

The COM server allows the user to control CANalyzer remotely via the standard Windows communication port. As a result, it is easy to initiate a wide range of communications with CANalyzer by means of scripts, e.g. Java script or VBA, or compiled languages.

In the histogram function histogram data are acquired on the transmit intervals of individual messages. These data can be collected separately according to message and according to measurement sections defined by CAPL. Such histograms can be saved as combined tables in standard file formats, or they can be displayed directly by scripts, e.g. in Excel. Demo scripts are included with the product.

CANalyzer options are available for the industrial automation protocols CANopen, DeviceNet and Smart Distributed Systems as well as for the J1939 protocol.



vector Technische Informatik

CANoe

Features

Products:

- Comprehensive tool for CAN projects
- Tool for CAN applications in the automotive field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V85x

Host Platforms Supported

Windows 9x/NT

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Product Overview

CANoe, the CAN open environment, is a powerful tool that supports the entire development process of CAN networked systems based e. g. on NEC CAN controller.

The distribution of functions over network nodes, the necessary CAN messages, and the functional models of the individual network nodes are specified at the beginning of a development. In addition to the CAN data proper, so-called envi-ronment variables (e.g. switch settings, sensor signals, output signals) are needed to describe the functional models.

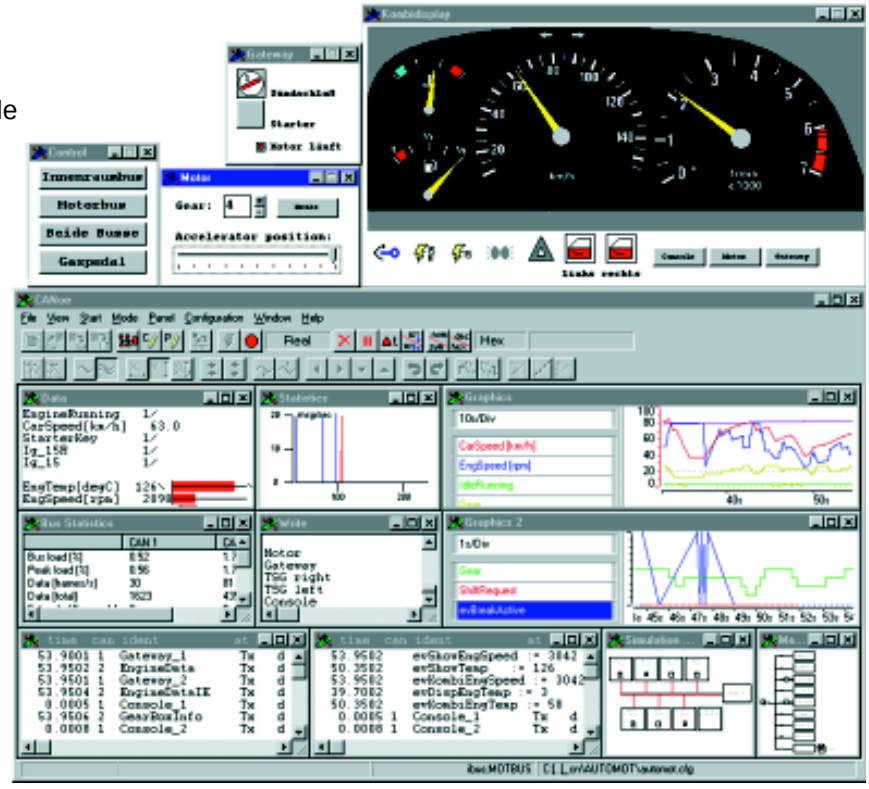
All information is stored in an extensive database. CANoe allows simulation and analysis of data communications between the individual network nodes and their environment. During the course of overall system realisation, the simulation of individual bus nodes can be substituted by real electronic control units.

These electronic control units can be operated either in their target environment or in a test environment with data specified and measured by CANoe.

CANoe has also extentions for modelling and analysis (Plug-Ins):
- OSEK Transport Protocol (OSEK-TP): Plug-in for modeling special applications, e.g. in the Man-Machine Interface area (MMI)

- OSEK Network Management (OSEK-NM)

- Other DLLs for proprietary protocols of individual motor vehicle manufacturers.



CANape

Features

Products:

- Tool for calibration of electronic control units via CAN
- Tool for CAN applications in the automotive field
- Tool for CAN applications in the automation field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V85x

Host Platforms Supported

Windows 9x/NT

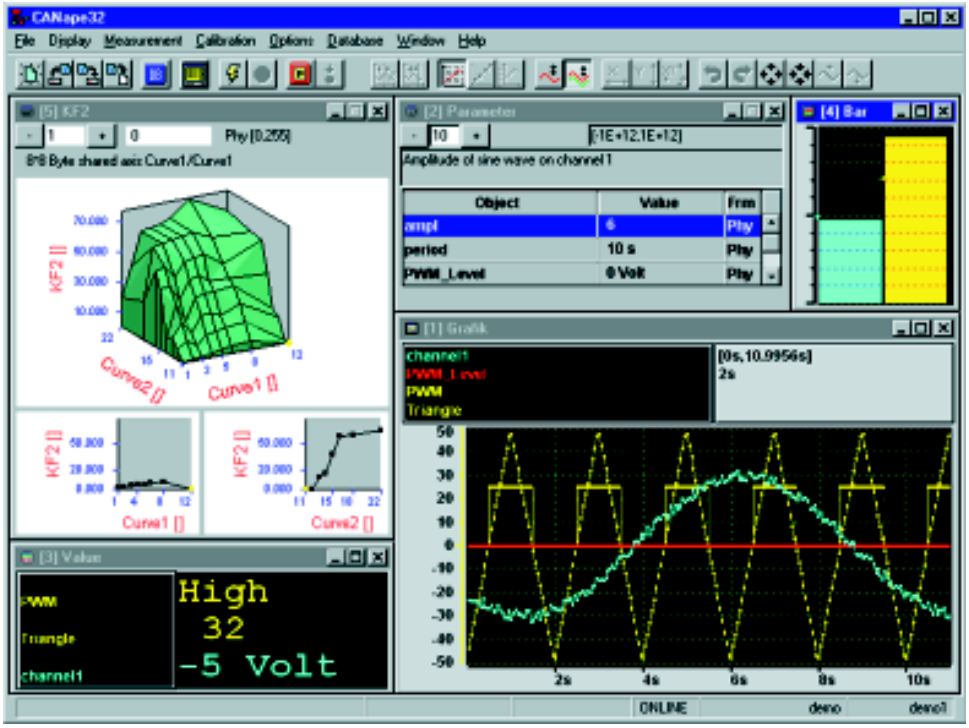
Product Overview

CANape is a PC-based development, testing and calibration tool for electronic controller units (ECU's). The primary target area for the use of CANape is the development and calibration of controllers which contain a CAN interface via CAN Calibration Protocol (CCP). By applying the standard interfaces developed in the ASAM initiative, CANape was created as a tool that is independent of the particular controller hardware and the development environment used.

With CANape, processes in the controller can be visualized in various formats by reading out and displaying internal process variables from the controller in real time (measurement data acquisition). In addition to process signals which are exchanged via CAN bus, specific measurement variables of the individual controller units can be queried, displayed and recorded in a time-correlated manner. Furthermore, characteristic variables, i.e. parameters that define the characteristics of the control or regulating algorithms in the controller (characteristic values, curves and maps) can be displayed and calibrated. The integrated database editor can be used to create a controller description file that is compatible with the ASAP2 standard.

The 'Flash programming' feature inside the data management unit, can be used to re-program the current contents of the calibration memory to the controller's flash memory - or any parameter set read from a parameter set file.

It is also possible to connect a controller via a K-Line using the KWP2000 protocol or to connect CANopen devices with the CANopen SDO protocol to CANape.



vector Technische Informatik

CANscope

Features

Products:

- Tool for measurement and display of CAN busline voltage
- Tool for CAN applications in the automotive field
- Tool for CAN applications in the automation field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V85x

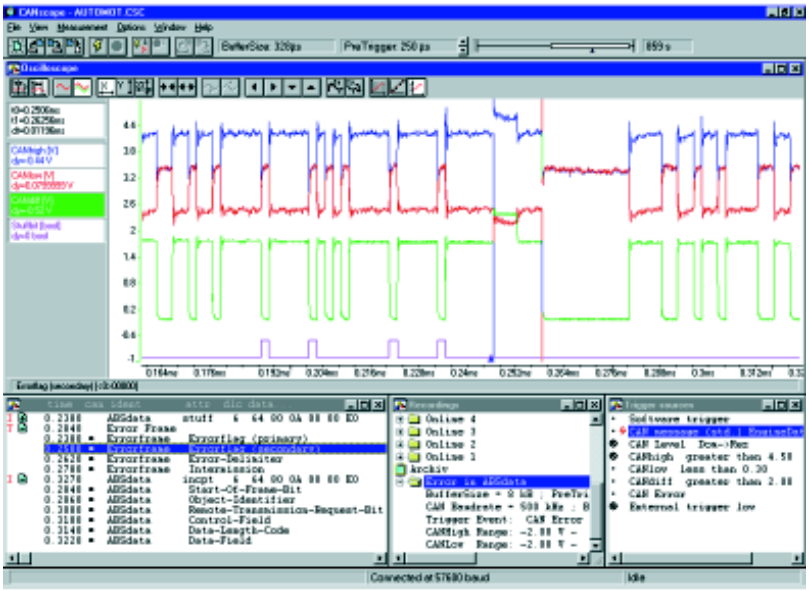
Host Platforms Supported

Windows 9x/NT

Product Overview

CANscope is a measuring instrument for logging and evaluating signal levels on the CAN bus. It consists of a robust logging module and easy-to-use evaluation software for Windows. The logging module is connected to the PC at a high baud rate via a RS232 port.

CANscope allows the developer to study the effects of various cable types, cable lengths, bus drivers, bus terminations and failure modes. Especially the micro controller developer can easily test his hardware.
A wide variety of trigger conditions are provided for selective error localization. For example, the trigger can be activated and the range around the trigger is completely recorded when a certain CAN message or Error frame occurs, or when the level exceeds an upper or lower limit.



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CANcardX

Features

Products:

- PC Card interface for CAN with a selection of bus drivers
- Tool for CAN applications in the automotive field
- Tool for CAN applications in the automation field

Service:

- Software development electronic networking
- Software development automotive electronic development- and application tools

NEC CPUs Supported

V85x

Host Platforms Supported

Windows 9x/NT

Product Overview

CANcardX the new CAN interface for mobile measurement tasks.

CANcardX is a PC card according to the PC-Card-standard (PCMCIA) with two new CAN controllers. This CAN controllers handles CAN messages with 11 bit as well as 29 bit identifiers.

Like the other CAN interfaces from Vector, CANcardX is able to detect and to generate error frames on the bus line.

CANcardX provides two completely independent CAN channels with two separate outlets. The transceivers are integrated into the connection cables - so called CANcabs. The user has the choice between several different transceivers: highspeed CANcabs according to ISO 11898 with or without optocoupler as well as several different CANcabs for body electronic busses of automotive industries.
Thus CANcardX covers all applications in the automation as well as in the automotive field.

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Integrated Systems, Inc.

Lauterbach Datentechnik GmbH

NEC Electronics Europe GmbH

SEGGER Microcontroller Systeme GmbH

Tektronix, Inc.

Vector Informatik GmbH

Appendix A

Wind River Systems, Inc.

Yokogawa Electric Corporation

Company Website Locators

Accelerated Technology, Inc . . . . . www.atinucleus.com

Applied Microsystems Corporation . . . . . www.amc.com

Ashling Microsystems Ltd. . . . . www.ashling.com

Cadence Design Systems. . . . . www.cadence.com

Corelis, Inc. . . . . www.corelis.com

DIAB-SDS. . . . . www.diabsds.com

Digital Logic Instruments GmbH. . . . . www.dli.de

Enea OSE Systems Inc. . . . . www.enea.com

ETAS GmbH & Co. KG. . . . . www.etas.de

Green Hills Software Inc. . . . . www.ghs.com

IAR Systems. . . . . www.iar.se

Integrated Systems, Inc. . . . . www.isi.com

Lauterbach Datentechnik GmbH. . . . . www.lauterbach.com

NEC Electronics Europe GmbH. . . . . www.nec.de

SEGGER Microcontroller Systeme GmbH . . . . . www.segger.com

Tektronix, Inc. . . . . www.tek.com/Measurement/

Vector Informatik GmbH. . . . . www.vector-informatik.de

Wind River Systems, Inc. . . . . www.windriver.com

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Document No. U14704EE1V0PF00

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