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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A125A/E	Rev.	1.00
Title	Notes on Using Ethernet Controller		Information Category	Technical Notification		
Applicable Product	RX64M Group RX71M Group	Lot No. All	Reference Document	RX64M Group User's Manual Hardware Rev 1.00 (R01UH0377EJ0100) RX71M Group User's Manual Hardware Rev 1.00 (R01UH0493EJ0100)		

(1) Notes。

If an erroneous frame is detected due to a corrupted frame or noise in the external circuit when the ETHERC and EPTPC are receiving data, subsequent normal frames may not be received properly.

(2) Measure

Reset the EDMAC, ETHERC, and EPTPC after an erroneous frame is detected. Then, wait for the required number of cycles before setting communications again.

■Detecting an erroneous frame

An erroneous frame can be detected by reading the INFABT flag in the SYNFP status register (SYSR) of EPTPCn.

The INFABT flag is provided for both EPTPC0 and EPTPC1, but the MINT interrupt is common to these channels. This requires each INFABT flag to be read in the MINT interrupt handler to confirm in which channel an erroneous frame is detected.

Even when the EPTPCn is not used but only the EDMACn and ETHERCn are used to receive and transmit standard Ethernet frames, also read the INFABT flag to detect an erroneous frame. (n = 0, 1)

■Resetting after detection of an erroneous frame

When the EPTPCn.SYSR.INFABT flag becomes 1, reset EPTPCn, EDMACn, and ETHERCn corresponding to the channel, and then wait for the required number of cycles before setting registers.

Even when the EPTPCn is not used but only the EDMACn and ETHERCn are used to receive and transmit standard Ethernet frames, also reset the EPTPCn and the registers. In this case, PTPEDMAC does not need to be reset. The following shows the resetting procedure. (n = 0, 1)

(1) Set the EPTPCn.PTRSTR.RESET bit to 1 (reset the EPTPCn by software)

(2) Set the EDMACn.EDMR.SWR bit to 1（reset the EDMACn and ETHERCn by software）

(3) Wait for at least 64 cycles of the peripheral module clock (PCLKA).

This step is necessary to initialize EDMACn and ETHERCn. Use a software loop or timer to wait for at least cycles of PCLKA.

(4) Set the EPTPCn.PTRSTR.RESET bit to 0 (release the EPTPCn reset)

(5) Reset communications

Set the registers of the EDMACn, ETHERCn, PTPEDMAC, and EPTPCn to enable communications.