phyCORE-MPC555

Hardware Manual

Edition July 2005

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

5th Edition: July 2005

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Preface

This phyCORE-MPC555 Hardware Manual describes the module's design and functions. Precise specifications for the Motorola MPC555 microcontroller series can be found in the enclosed MPC555 microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal. The MSB and LSB of the data and address busses shown in the circuit diagram are based on the conventions of Motorola. Accordingly, D31 and A31 represent the LSB, while D0 and A0 represent the MSB. These conventions are also valid for the parallel I/O signals.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC555

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC555 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC555 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC555 is a subminiature (72 x 57 mm) insert-ready Single Board Computer populated with Motorola's PowerPC MPC555 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0,635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC555 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC555.

The phyCORE-MPC555 offers the following features:

- Single Board Computer in subminiature form factor (72 x 57 mm) according to phyCORE specifications
- All applicable controller and other logic signals extend to two high-density 160-pin Molex connectors
- Processor: Motorola embedded PowerPC MPC555 (40 MHz clock)

- **Internal Features of the MPC555:**
  - 32-bit PowerPC core, 40MHz CPU speed
  - 64-bit Floating Point Unit
  - 26 kByte SRAM; capable of battery buffering
  - 448 kByte FLASH
  - Dual UART/SPI
  - Dual CAN 2.0B
  - Dual TPU with 16 channels each
  - Two 16-bit timer system
  - Eight channel 16-bit PWM system
  - Dual 10-bit ADC (7µs) with 32(41) channels (ext. MUX)
  - Multi-Purpose I/O signal
  - JTAG/BDM test/debug port

- **Memory Configuration[1]:**

  - SRAM: 128 kByte to 8 MB flow-through Synchronous Burst-RAM, 32-bit access, 0 wait states, 2-1-1-1 Burst mode
  - Flash-ROM: 0 / 512 kBytes/ 1 MB/ 2 MB/ 4 MB, 32-bit width
  - I^2C Memory: 4 kByte EEPROM (up to 32 kByte, alternatively I^2C FRAM, I^2C SRAM)

- I^2C Real-Time Clock with calendar and alarm function
- Power-down/wake-up support via RTC, decrementor, or external signal
- Dual UART/SPI port: RS-232 transceiver for both channels (RxD/TxD); also configurable as TTL
- Dual CAN port: CAN transceiver 82C251 for both channels; also configurable as TTL
- JTAG/BDM test/debug port
- Available in standard (0…+70°C) and industrial (-40…+85°C) temperature ranges

1: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

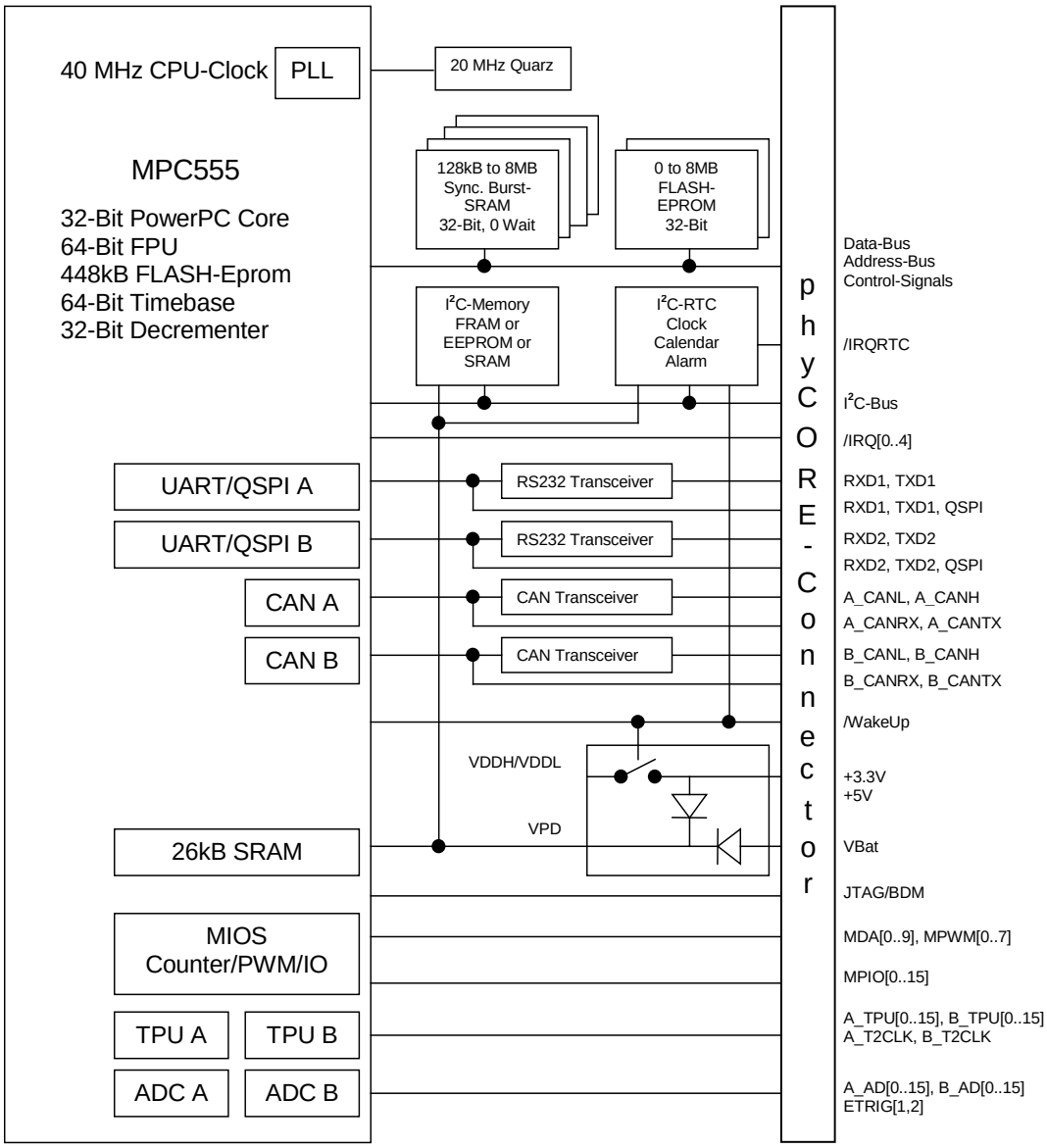


Figure 1: Block Diagram phyCORE-MPC555

1.2 View of the phyCORE-MPC555

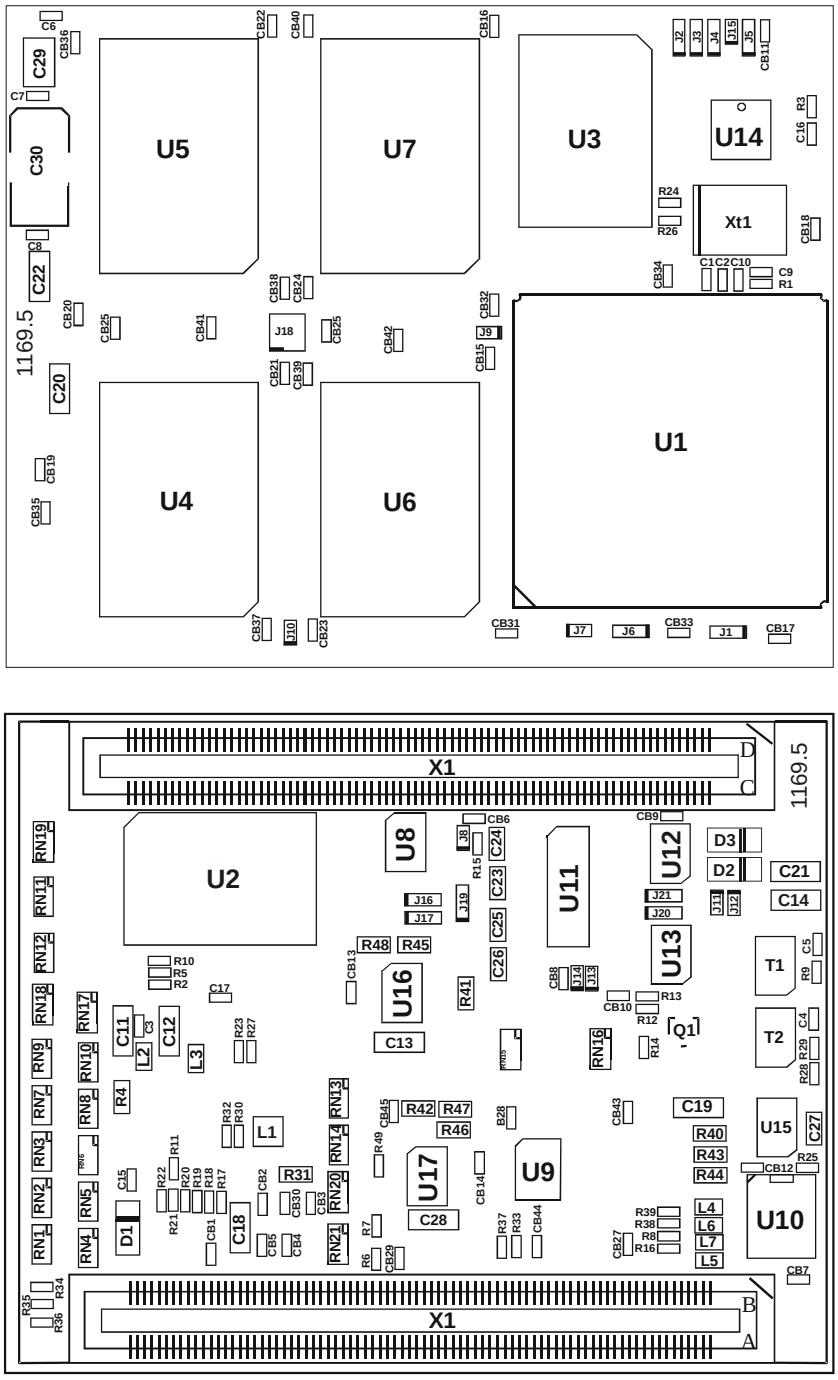


Figure 2: View of the phyCORE-MPC555

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to high density 0,635 mm SMT-plugs (refered to as phyCORE-Connector) lining two sides of the board (*refer to section 9*). This allows the phyCORE-MPC555 to be plugged into any target application like a "big chip".

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-Connector. *Please refer to the Motorola MPC555 User Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

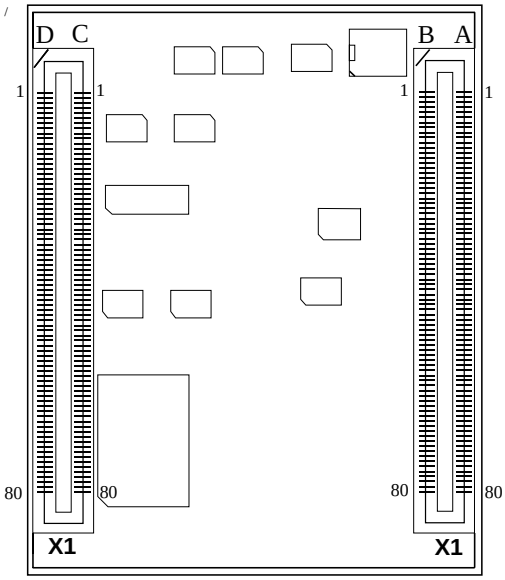


Figure 3: Pinout of the phyCORE-MPC555 (Bottom View)

Pin Number	Connection	I/O	Comments
Pin row X1A			
1A	EXTCLK	I	Optional external clock input of the MPC555
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	/IRQ3	I	/IRQ3 interrupt of the MPC555. Alternative: /KR, /RETRY, SGPIOC3 (I/O)
4A	/IRQ0	I	/IRQ0 interrupt of the MPC555. Alternative: SGPIOC0 (I/O)
5A	/CS2	O	Free /CS signal of the MPC555.
6A	/CS1	O	/CS signal of processor for control of synchronous SRAM U4-U7.
8A	/WE3	O	Write enable signal for the data lines D[24..31]. **Note** that D31 represents the LSB Alternative: AT3 (O) The alternative function may only be used if no on-board memory is populated.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	A30, A29, A27, A24, A22, A21, A19, A16, A14, A13, A11, A8	I/O	Address lines[1] Alternative: SGPIOA30, SGPIOA29, SGPIOA27, SGPIOA24, SGPIOA22, SGPIOA21, SGPIOA19, SGPIOA16, SGPIOA14, SGPIOA13, SGPIOA11, SGPIOA8 (I/O) For the use of the alternative function, note that the address lines are partially used for memory addressing.
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D30, D29, D27, D24, D22, D21, D19, D16, D14, D12, D11, D9, D6, D4, D3, D1	I/O	Data lines[1] Alternative: SGPIOD30, SGPIOD29, SGPIOD27, SGPIOD24, SGPIOD22, SGPIOD21, SGPIOD19, SGPIOD16, SGPIOD14, SGPIOD12, SGPIOD11, SGPIOD9, SGPIOD6, SGPIOD4, SGPIOD3, SGPIOD1 (I/O) For use of the alternative function, note that the data lines are used to connect the on-board memory devices.
34A	/TA	I/O	Transfer acknowledge signal of the MPC555.
35A	/TEA	I/O	Transfer error acknowledge signal of the MPC555.
36A	/BB	I/O	Bus busy signal of the MPC555. Alternative: VF2 (O), IWP3 (O)
51A	TSIZ0	I/O	Transfer size signal of the MPC555.

Pin Number	Connection	I/O	Comments
48A, 49A, 50A	NC	-	Not connected These contacts should remain unconnected on the target hardware side.
53A	/TS	I/O	Transfer start signal of the MPC555.
54A	RDNWR	I/O	Read/write (RD//WR) signal of the MPC555.
55A	/BDIP	I/O	Burst data in progress signal of the MPC555.
56A	/BURST	I/O	Burst indicator signal of the MPC555.
58A	/BI//STS	I/O	Burst inhibit signal of the MPC555. Alternative: special transfer start (O)
60A 61A 63A 64A 65A 66A 68A 69A	B_TPU15, B_TPU13, B_TPU11, B_TPU9, B_TPU7, B_TPU5, B_TPU3, B_TPU1	I/O	TPU I/O signals connected to the TPU B of the MPC555.
70A	B_T2CLK	I/O	Clock signal of the TPU B of the MPC555.
71A 73A 74A 75A 76A 78A 79A 80A	A_TPU15, A_TPU13, A_TPU11, A_TPU9, A_TPU7, A_TPU5, A_TPU3, A_TPU1	I/O	TPU I/O signals connected to the TPU A of the MPC555.
Pin row X1B			
1B	CLKOUT	O	Processor clock of the MPC555
2B	/IRQ1	I	/IRQ1 interrupt request of the MPC555 Alternative: /RSV (O), SGPIOC1 (I/O)
3B	/IRQ2	I	/IRQ2 interrupt request of the MPC555 Alternative: /CR (I), SGPIOC2 (I/O), /MTS (O) Per default, following a system reset, the /MTS function is pre-selected. The function can be configured in the register SIUMCR (Bits MTSC, MLRC).
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND		Ground 0 V

Pin Number	Connection	I/O	Comments
5B	/CS3	O	Free /CS signal of the MPC555
6B	/CS0	O	/CS signal[1] of the MPC555 used as control of the on-board Flash memory
7B	/OE	O	Output enable[1] signal of the MPC555
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	A31. A28, A26, A25, A23, A20, A18, A17, A15, A12, A10, A9	I/O	Address lines[1]: A31 is the LSB! Alternative: SGPIOA31, SGPIOA28, SGPIOA26, SGPIOA25, SGPIOA23, SGPIOA20, SGPIOA18, SGPIOA17, SGPIOA15, SGPIOA12, SGPIOA10, SGPIOA9 (I/O) For use of the alternative function, note that the address lines are partially used for memory addressing.
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D31, D28, D26, D25, D23, D20, D18, D17, D15, D13, D10, D8, D7, D5, D2, D0	I/O	Data lines[1]: D31 is the LSB and D0 is the MSB! Alternative: SGPIOD31, SGPIOD28, SGPIOD26, SGPIOD25, SGPIOD23, SGPIOD20, SGPIOD18, SGPIOD17, SGPIOD15, SGPIOD13, SGPIOD10, SGPIOD8, SGPIOD7, SGPIOD5, SGPIOD2, SGPIOD0 (I/O) For use of the alternative function, note that the address lines are partially used for memory addressing.
33B	/WE2	O	Write enable signal[1] for data lines D[16..23] Alternative: AT2 (O) The alternative function can only be used when no on-board memory is populated.
35B	/BG	I/O	Bus grant signal of the MPC555 Alternative: VF0 (O), LWP1 (O)
36B	/BR	I/O	Bus request signal of the MPC555 Alternative: VF1 (O), IWP2 (O)
47B, 48B, 50B	NC	-	Not connected These contacts should remain unconnected on the target hardware side.
51B	TSIZ1	I/O	Transfer size signal of the MPC555.
52B	/WE1	O	Write enable signal for data lines D[8..15] Alternative: AT1 (O) The alternative function can only be used when no on-board memory is populated.
53B	/WE0	O	Write enable signal for data lines D[0..7]. Note that D0 represents the MSB! Alternative AT0 (O) The alternative function can only be used when no on-board memory is populated.

Pin Number	Connection	I/O	Comments
55B	/IRQ4	I	/IRQ4 Interrupt request of the MPC555 Alternative: AT2 (O), SGPIOC4 (I/O)
56B	MODCK1	I	Mode clock select of the MPC555 MODCK1 is active only while /PORSET = low. Afterwards the alternative functions of this pin are available. Alternative: /IRQ5 (I), SGPIOC5 (I/O)
57B, 58B	MODCK2, MODCK3	I	Mode clock select of the MPC555 MODCK2 and MODCK3 are active only while /PORSET= low. Afterwards the alternative functions of these pins are available. Alternative: /IRQ6, /IRQ7 (I)
60B 61B 62B 63B 65B 66B 67B 68B	B_TPU14, B_TPU12, B_TPU10, B_TPU8, B_TPU6, B_TPU4, B_TPU2, B_TPU0	I/O	TPU I/O signals connected with the TPU B of the MPC555.
70B	A_T2CLK	I/O	Clock signal of the TPU A of the MPC555
71B 72B 73B 75B 76B 77B 78B 80B	A_TPU14, A_TPU12, A_TPU10, A_TPU8, A_TPU6, A_TPU4, A_TPU2, A_TPU0	I/O	TPU I/O signals connected with the TPU A of the MPC555.
Pin row X1C			
1C, 2C	+3V3	I	Supply Voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C	GND	-	Ground 0V
4C, 5C	+5V	I	Supply Voltage +5 VDC
6C	VBAT	I	Connection for external battery (+)2.4 - 3.3V
8C	+3V3GOOD	O	Indicator signal for a valid input voltage +3V3

Pin Number	Connection	I/O	Comments
9C	TEXP / /RSTCNF	I/O	While the /HRESET is active, the pin serves as an input and determines the source of the Hard Reset Configuration Word (HRCW). If a low level is applied, the HRCW is read from the data bus. Otherwise an internal HRCW is used that is derived from either the Flash (CMCFIG with /HC=0) or, in the case that /HC = 1, will be read as default value 0x00000000. Note that during /HRESET phase with /RSTCNF= high, the data bus must be held at tri-state. In normal operation / shut-down, the pin functions as an output and controls the power switch for VDDH and VDDL.
10C	/HRESET	I/O	Hard-reset signal[1] of the MPC555. An Open-Drain transceiver controls /HRESET.
11C	/PORSET	I/O	Power-on reset of the MPC555. An open drain transceiver controls the /PORESET. /PORESET monitors the input voltage +3V3 and VPD.
13C 14C 15C 16C 19C 24C 29C	MPIO15, MPIO13, MPIO11, MPIO9, MPIO7, MPIO6, MPIO5	I/O	MIOS GPIO signals of the MPC555.
18C	B_CANH	I/O	CANH output of the CAN transceiver of the second CAN interface.
20C	ECK	I	External baud clock input of both UARTs of the MPC555.
21C	RxD2	I	RxD input of the RS-232 transceiver of the second serial interface. J14 must be closed in order to use this interface.
23C	TxD2	O	TxD output of the RS-232 transceiver of the second serial interface.
25C	QGPIO5	I/O	General purpose input/output of the MPC555 Alternative: MOSI master out / slave in of the QSPI interfaces. (I/O)
26C, 28C	QGPIO3, QGPIO1	I/O	General purpose input/output of the MPC555 Alternative: PCS3, PCS1 peripheral /CS signal of the QSPI interfaces. (I/O)

Pin Number	Connection	I/O	Comments
30C, 38C	MPIO4, MPIO3	I/O	MIOS-GPIO signals of the MPC555 Alternative: VFLS1, VFLS0 (VFLS bit in MIOS1TCR) (A)
31C	SCL	I/O	I^2C Clock signal: The signal can be generated with SGPIOC7 via software or by using an external pin. SCL and SGPIOC7 are coupled via the 100R resistor at R38.
33C	DSDI	I	Development-Serial-Data-Input of the MPC555 BDM interface. Alternative: TDI Test-Data-In of the MPC555 JTAG port. The HRCW (D11) determines which function is active
34C	/TRST	I	Test-Reset input of the MPC555 JTAG port. /TRST is connected with /PORESET using a 10k resistor
35C	DSCK	I	Development-Serial-Clock of the MPC555 BDM port. Alternative: TCK Test-Clock of the MPC555 JTAG port The HRCW (D11) determines which function is active
36C	TMS	I	Test-Mode-Select of the MPC555 JTAG port
39C	MPIO1	I/O	MIOS-GPIO signals of the MPC555 Alternative: VF1- Visible-Instruction-Queue-Flash-Status (VF bit in MIOS1TPCR) (0)
40C, 41C, 43C	MDA9, MDA7, MDA5	I/O	Double-Action I/O MDA [31, 29, 27] of the MPC555-MIOS. These signals serve either as Input-Capture or Output-Compare
44C, 45C	MDA3 MDA1	I/O	Double-action I/O MDA[14, 12] of the MPC555-MIOS. These signals serve as either Input-Capture or Output-Compare. Alternatively these signals serve the external reload of the counter register within the counter modules.
46C 48C 49C 50C 51C	MPWM7, MPWM5, MPWM3, MPWM1, MPWM0	I/O	PWM output or I/O signals of the MPC555 MIOS (MPWM19, MPWM17, MPWM3, MPWM1, MPWM0)

Pin Number	Connection	I/O	Comments
53C	RXD2_TTL	I	Receive line of the second MPC555 UART. Alternative: QGPI2 general purpose input (I). When the alternative function is used, solder jumper J14 must be open in order to disconnect the receive output of the RS-232 transceiver.
54C	TXD2_TTL	O	Transmit line of the second MPC555 UART Alternative: QGPO2 general purpose output (O)
55C	/PWRON	O	/PWRON controls the FET switch of the +3V/VDDL and 5+V/VDDH supply voltages
56C	/WAKEUP	I/O	Low level at /WAKEUP completes a module shut down and prompts activation of the voltage supply. On the module, the RTC interrupt /IRTC can be connected to /WAKEUP using Jumper J15. /WAKEUP should have a wired-OR connection against GND.
58C 59C	ETRIG2, ETRIG1	I	Trigger inputs of the QADC modules A and B on the MPC555
60C, 61C	B_AD14, B_AD12	I/O	Analog input B_AN[58,56] of QADC module B on the MPC555 Alternative: B_PQA [6, 4] digital I/O
62C, 67C, 72C, 77C	GNDA	-	Ground 0V for analog signals. GNDA is connected to GND using the 0R resistor at R31.
63C 64C	B_AD10, B_AD8	I/O	Analog input B_AN [54,52] of QADC module B on the MPC555 Alternative: B_MA[2,0] (O) Alternative: B_PQA[2,0] digital I/O
65C 66C	B_AD6, B_AD4	I	Analog input B_AN[50,48] of QADC module B on the MPC555 Alternative: B_PQB[6,4] digital input (I)
68C 69C	B_AD2, B_AD0	I	Analog input B_AN[2,0] of QADC module B on the MPC555 Alternative: B_ANY, B_ANW (I) Alternative: B_PQB[2,0] digital input (I)
70C 71C	A_AD14, A_AD12	I/O	Analog input A_AN[58,56] of QADC module A on the MPC555 Alternative: A_PQA[6,4] digital I/O
73C 74C	A_AD10 A_AD8	I/O	Analog input A_AN[54,52] of QADC module A on the MPC555 Alternative: A_MA[2,0] (O) Alternative: A_PQA[2,0] digital I/O

Pin Number	Connection	I/O	Comments
75C 76C	A_AD6 A_AD4	I	Analog input A_AN[50,48] of QADC module A on the MPC555 Alternative: A_PQB[6,4] digital input
78C 79C	A_AD2 A_AD0	I	Analog input A_AN[2,0] of QADC module A on the MPC555 Alternative: A_ANY, A_ANW (I) Alternative: A_PQB[2,0] digital input (I)
80C	VDDA	O	Voltage supply +5 VDC for analog signals. VDDA is coupled with VDDH using a choke at L1.
Pin row X1D			
1D, 2D	+3V3	I	Supply Voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D	GND	-	Ground 0V
4D, 5D	NC	-	Not connected These contacts should remain unconnected on the target hardware side.
6D	VPD	O	Power-down supply voltage VPD, this is generated by VBAT or +3V3 using a diode switch. VPD serves as supply voltage for the MPC555 internal SRAM, the Real-Time Clock, and the serial EPROM.
7D	/PFI	I	Power-fail input is a TTL input that serves as a manual reset input for the /PORESET. /PORESET has a timeout of approximately 50 ms.
8D	/SRESET	I/O	Soft-reset of the MPC555
10D	/HRESIN	I	Hard-reset input controls the system reset /HRESET. /HRESET has a timeout of approximately 22 ms.
11D 12D 13D 15D	MPIO14, MPIO12, MPIO10, MPIO8	I/O	MIOS GPIO MPIO32B[14,12,10,8] signals of the MPC555
16D	RXD1_TTL	I	Receive line of the first MPC555 UART. Alternative: QGPI1 general purpose input If the alternative function is used, solder jumper J13 must be open in order to disconnect the receive output of the RS-232 transceiver.
17D	TXD1_TTL	O	Transmit line of the first MPC555 UART. Alternative: QGPO1 general purpose output

Pin Number	Connection	I/O	Comments
18D	B_CANL	I/O	CANL output of the CAN transceiver for the second CAN interface
20D	A_CANL	I/O	CANL output of the CAN transceiver for the first CAN interface
21D	A_CANH	I/O	CANH output of the CAN transceiver for the first CAN interface
22D	RxD1	I	RxD input of the RS-232 transceiver for the first serial interface. Jumper J13 must be closed to use this interface.
23D	TxD1	O	TxD output of the RS-232 transceiver for the first serial interface
25D	QGPIO6	I/O	General purpose input/output of the MPC555 Alternative: SCK clock of the QSPI interface (I/O)
26D	QGPIO4	I/O	General purpose input/output of the MPC555 Alternative: MISO Master In / Slave Out of the QSPI interface (I/O).
27D	QGPIO2	I/O	General purpose input/output of the MPC555 Alternative: PCS2, peripheral /CS signals of the QSPI interfaces (I/O)
28D	QGPIO0	I/O	General purpose input/output of the MPC555 Alternative: PCS0 peripheral /CS signals of the QSPI interfaces (I/O). SS: with the help of this bi-directional signal, the QSPI interface can switch into Slave Mode.
30D	SGPIOC7	I/O	General purpose input/output of the MPC555 SGPIOC7 is connected to the SCL signal of the I^2C bus via R38 and serves as the clock signal. Alternative: /IRQOUT interrupt output Alternative: LWP0- load/store watchpoint 0 After Reset, the LWP0 function is active.
31D	SGPIOC6	I/O	General purpose input/output of the MPC555 SGPIOC6 is connected to the SDA signal of the I^2C bus via R39 and serves as data signal. Alternative: FRZ- freeze (O) Alternative: /PTR- program trace (O) After reset, the /PTR function is active.

Pin Number	Connection	I/O	Comments
32D	SDA	I/O	Data line of the I^2C bus. SDA is connected to the MPC555 signal SGPIOC6 via R39.
33D	/IRTC	O	Interrupt output of the RTC. /IRTC can be connected to /WAKEUP using jumper J15.
35D	DSDO	O	Development serial data output of the MPC555 BDM port. Alternative: TDO test data out of the JTAG port (O). The HRCW (D11) determines the function.
36D, 37D	VFLS0, VFLS1	O	Visible history buffer flush status of the MPC555 BDM port. Alternative: IWP[0,1] instruction watchpoint (O). The HRCW (D9, D10) determines the function.
38D, 40D	MPIO2, MPIO0	I/O	MIOS GPIO signals of the MPC555 Alternative: VF2, VF0 visible instruction queue flush status (VF bit in MIOS1TPCR) (O)
41D, 42D,43D	MDA8, MDA6, MDA4	I/O	Double action I/O MDA[30,28,15] of the MPC555 MIOS. These signals serve either as input capture or output compare.
45D, 46D	MDA2, MDA0	I/O	Double action I/O MDA [13,11] of the MPC555 MIOS. These signals serve either as input capture or output compare. Alternatively these signals serve as clock input of the counter submodule (MDAO MMCSM6, MDA2 MMCCM22).
47D 48D 50D	MPWM6, MPWM4, MPWM2	I/O	PWM output or I/O signals of the MPC555 MIOS (MPWM[18, 16, 2])
51D	VDDGOOD	O	Indicator signal for valid supply voltages VDDH (+3.3 V) and VDDL (+5 V) after the FET switch. If the signal is high, the voltage is above the HRESET threshold.
52D	/VDDGOOD	O	Inverted VDDGOOD
53D	EPEE	I	EPEE switches the supply voltages of the on-chip Flash module on the MPC555 from VDDL (+3.3 V) to VDDH (+5 V). It also enables the erase/program function.
55D	B_CNTX0	O	CAN transmit line (TTL) of TouCAN module B on the MPC555
56D	B_CNRX0	I/O	CAN receive line (TTL) of TouCAN module B on the MPC555. With an activated CAN transceiver and Jumper J12 closed, the transceiver drives this pin.

Pin Number	Connection	I/O	Comments
57D	A_CNTX0	O	CAN transmit line (TTL) of TouCAN module A on theMPC555
58D	A_CNRX0	I/O	CAN receive line (TTL) of TouCAN module A on the MPC555. With an activated CAN transceiver and J11 closed, the transceiver drives this pin.
59D, 64D, 69D, 74D, 79D	GNDA	-	Ground 0V for analog signals. GNDA is connected to GND using the 0R resistor at R31.
60D 61D 62D	B_AD15, B_AD13, B_AD11	I/O	Analog input B_AN[59,57,55] of QADC module B on the MPC555. Alternative: B_PQA[7,5,3] digital I/O
63D	B_AD9	I/O	Analog input B_AN53 of QADC module B on the MPC555. Alternative: B_MA1 of B_QADC (O) Alternative: B_PQA1 of the digital I/O
65D 66D	B_AD7, B_AD5	I	Analog input B_AN[51,49] of QADC module B on the MPC555. Alternative: B_PQB[7,5] digital input (I)
67D 68D	B_AD3 B_AD1	I	Analog input B_AN[3,1] of QADC module B on the MPC555. Alternative: B_ANZ, B_ANX input (I) Alternative: B_PQB[3,1] digital input (I)
70D 71D 72D	A_AD15, A_AD13, A_AD11	I/O	Analog input A_AN[59,57,55] of QADC module A on the MPC555. Alternative: A_PQA[7,5,3] digital I/O
73D	A_AD9	I/O	Analog input A_AN53 of QADC module A on the MPC555. Alternative: A_MA1 of the A-QADC (O) Alternative: A_PQA1 digital I/O
75D, 76D	A_AD7, A_AD5	I	Analog input A_AN[51,49] of QADC module A on the MPC555 Alternative: A_PQB[7,5] digital input (I)
77D, 78D	A_AD3, A_AD1	I	Analog input A_AN[3,1] of QADC module A on the MPC555. Alternative: A_ANZ, A_ANX input (I) Alternative: A_PQB[3,1] digital input (I)
80D	VRH	O (I)	Reference voltage of the QADC module. If Jumper J7 is closed, VRH is connected with VDDA. J7 must be opened in order to use an external reference voltage.

Table 1: Pinout of the phyCORE-Connector X1

[1]: **Caution:**
Because of the LV-Flash devices used the signals A29..A9, D31..D0, /CS0, /OE, /WE0, /WE2 and /HRESET must have signal levels of max. 3.3 V +0.5 V.

3 Jumpers

For configuration purposes, the phyCORE-MPC555 has 21 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the jumper-pads, while *Figure 5* indicates the location of the jumpers on the board.

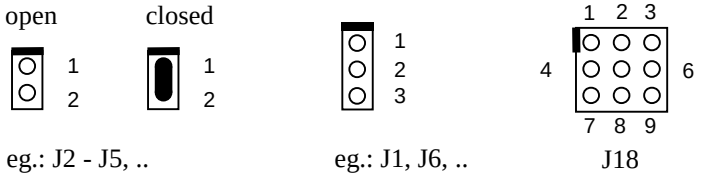


Figure 4: Numbering of the Jumper Pads

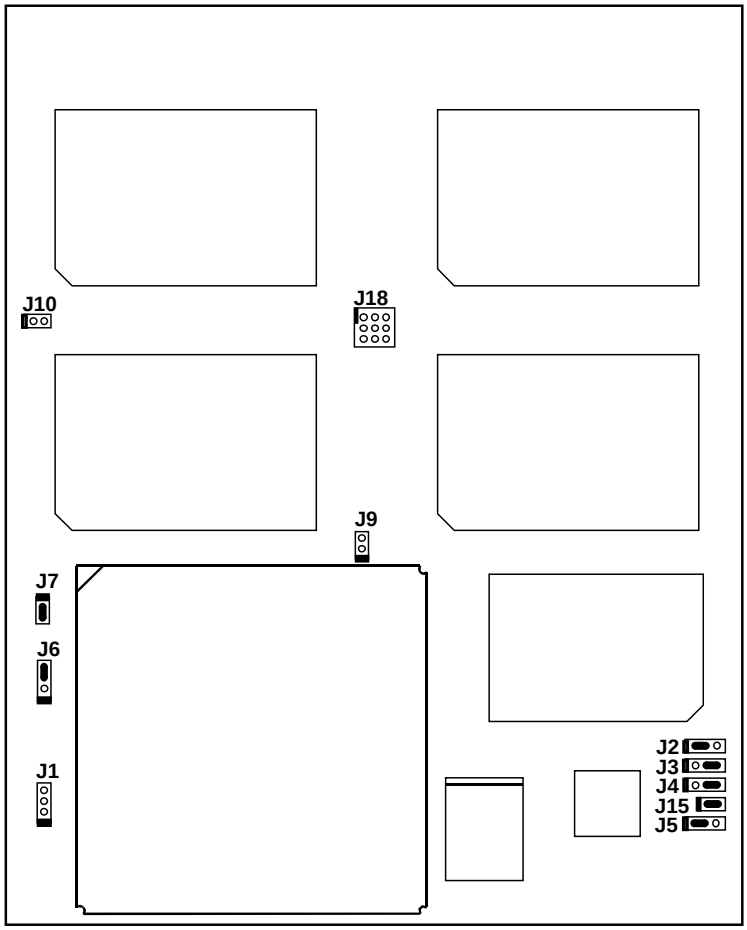


Figure 5: Location of the Jumpers (Controller Side) and Default Setting (Standard Version of the phyCORE-MPC555)[1]

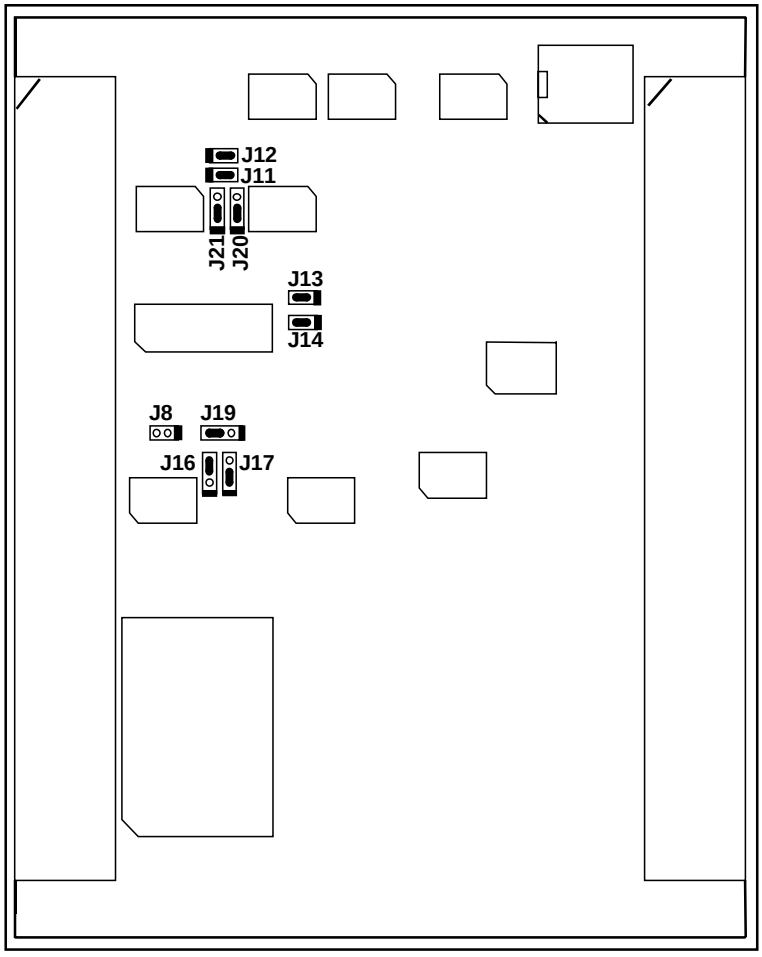


Figure 6: Location of the Jumpers (Connector Side) and Default Setting (Standard Version of the phyCORE-MPC555)[1]

[1]: Jumper J10 and J18 might vary because of different memory on the phyCORE-MPC555.

The jumpers (J = solder jumper) have the following functions:

Jumper	default	Comment
J1		Determines the memory for a program start after reset.
1+2		Internal (on-chip) Flash memory (D20 –> VDDL)
2+3		External (on-board) Flash memory (D20 –> GND)
open	X	D20 must be externally configured via a 4k7 resistor
Package Type		0R in SMD 0402
J2, J3, J4		These jumpers configure the clock mode of the MPC555. When /PORESET is active, the bit pattern connects to the MODCK [1..3] signals of the MPC555. Only the standard configurations using the MPC555's oscillator and quartz are shown below. The default configuration depends on the frequency of the external quartz populating the module. Configurations for use of an external clock source can be found in the MPC555 user's manual.
1+2, 2+3, 2+3	X	20 MHz Quartz, limp-mode activated (MODCK[1..3]=011)
1+2, 1+2, 2+3		20 MHz Quartz, limp-mode deactivated (MODCK[1..3]=001)
1+2, 2+3, 1+2	X	4MHz Quartz, limp-mode activated (MODCK[1..3]=010)
Package Type		0R in SMD 0402
J5		J5 determines the source of the Hard Reset Configuration Word (HRCW). During /HRESET, the HRCW configures the MPC555.
1+2	X	The HRCW is read via the data bus. Except D20 the data bus is supported by pull-down resistors and accordingly guarantees a valid data word. J1 configures D20 and determines the internal or external Flash memory as boot code source.
2+3		The internal default word is read as HRCW /HC = 0: the bit pattern (CMFCFIG) from the internal Flash is read /HC = 1: the internal default HRCW 0x00000000 is read
Package Type		0R in SMD 0402
J6		J6 selects the power supply for the internal SRAM of the MPC555.
1+2		The module input voltage +3V3 feeds the on-chip SRAM.
2+3	X	The power-down power supply (VPD) feeds the on-chip SRAM. In the event that there is no +3V3 module input supply, the VPD is provided by the battery input.
Package Type		0R in SMD 0402
J7		Selects the source for the positive reference voltage of the A/D converter modules of the MPC555.
open		The reference voltage VRH is derived from an external voltage source via phyCORE-Connector Pin X1D80.
closed	X	The reference voltage input is connected to the supply network VDDA (+5 V).
Package Type		0R in SMD 0402

Jumper	default	Comment
J8		J8 switches Pin 7 of the serial memory at U8 to high-level. On many memory devices, pin 7 enables the activation of a write protection function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC555 will have this write protection function. *Please refer to the corresponding memory data sheet for precise information*.
open	X	Write protection function is disabled.
closed		Write protection function is activated.
Package Type		0R in SMD 0402
J9		J9 switches the I/O signal MPIO0 to the power-down input of the synchronous BURST-SRAMs. This enables the external RAM banks to be switched to a power saving mode via software. During this state, the memory cannot be read or written to.
open	X	The signal MPIO0 is decoupled from the power-down inputs ZZ of the SRAMs and can be used for other functions. The ZZ inputs are connected to a pull-down resistor.
closed		The signal MPIO0 is connected to the power-down inputs ZZ of the SRAMs. A power-down is activated with high-level.
Package Type		0R in SMD 0402
J10[1]		J10 connects the memory bank address signal BA1 to the processor address line A9. This jumper must be closed in the case that the module is populated with synchronous BURST-SRAMs that have a capacity of 512k x 32/36 bit (2MB) or larger per device. In addition, Jumper J18 must be specifically set in accordance with the board's memory configuration. The factory default setting of J10 will be set according to the particular memory configuration of each individual module.
open		Synchronous BURST SRAM devices with a capacity smaller than 512k x 32/36 bit (2MB).
closed		Synchronous BURST SRAM devices with a capacity of 512k x 32/36 bit (2MB) or larger
Package Type		0R in SMD 0402
J11, J12		J11 and J12 disconnect the CAN receive lines of the MPC555 from the CAN transceivers at U12 and U13. This makes the controller's CAN TTL signals available at pins X1D58 (CAN_A) and X1D56 (CAN_B). This is useful for optically decoupling the CAN bus signals from the core logic.
open		The CAN receive signals A_CANRX0 and B_CANRX0 are disconnected from the CAN transceiver and are available at pin X1D58 (A_CANRX0) and X1D56 (B_CNRX0).
closed	X	The CAN receive signals A_CANRX0 and B_CANRX0 are connected to the CAN transceiver.
Package Type		0R in SMD 0402

Jumper	default	Comment
J13, J14		J13 and J14 connect the receive lines of both MPC555 UARTs to the RS-232 transceiver at U11. When left open the controller's RS-232 TTL signals are available at pins X1D16 (RXD1_TTL) and X1C53 (RXD2_TTL). This is useful for optically decoupling the RS-232 signals from the core logic.
open		The UART receive signals RXD1_TTL and RXD2_TTL are disconnected from the RS-232 transceiver. These signals are available at X1D16 (RXD1_TTL) and X1C53 (RXD2_TTL).
closed	X	The UART receive signals RXD1_TTL and RXD2_TTL are connected to the RS-232 transceiver.
Package Type		0R in SMD 0402
J15		Jumper J15 connects the alarm interrupt output of the Real-Time Clock (RTC) to the /WAKEUP signal of the power supply. Through programming of the RTC alarm functions, a precise wake up from a power-down can be executed.
open		The signal /IRTC is disconnected from the /WAKEUP input. /WAKEUP is tied to the potential of the supply voltage +3V3 via the pull-up resistor R24.
closed	X	The signal /IRTC is connected with the /WAKEUP input. The interrupt output of the RTC is of the open-drain type. /WAKEUP can further be used on the target hardware side (wired-OR against GND).
Package Type		0R in SMD 0402
J16, J17		J16 and J17 define the slave address (A2 and A1) of the serial memory on the I^2C bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to GND. It must be noted that the RTC at U10 is also connected to the I^2C bus. The RTC has the preconfigured address 0xA2 / 0xA3 that cannot be changed.
1+2, 2+3		A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1)
1+2, 1+2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2+3, 2+3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2+3, 1+2	X	A2= 1, A1= 1, A0=0 (0xAC / 0xAD) I^2C slave address 0xAC for write operations and 0xAD for read access.
Package Type		0R in SMD 0402

Jumper	default	Comment
J18[1]		J18 connects the memory bank address signals BA0 and BA1 to the corresponding address lines of the processor. The configuration of these jumpers is dependent on the memory size of the synchronous BURST-SRAM populating the module. The factory setting of J18 is in accordance with the memory configuration of each individual module. All four memory banks are typically equipped with the same devices. **Please note** that Jumper J10 must be specifically set in accordance with the board's memory configuration.. Jumper J10 is only closed when memory devices with a capacity of 512k x 32/36 bits or larger are used. In all other cases J10 remains open.
1+4, 2+3		32k x 32/36 bits per device, (J10 open)
3+6, 5+8		64k x 32/36 bits per device, (J10 open)
5+6, 7+8		128k x 32/36 bits per device, (J10 open)
4+7, 8+9		256k x 32/36 bits per device, (J10 open)
6+9		512k x 32/36 bits per device, (J10 closed)
Package Type		0R in SMD 0402
J19		J19 selects the supply voltage (VPD or VDDL) of the serial memory. VPD is used in the case that a serial SRAM, which requires buffering of its memory contents, populates the module. For EEPROM and FRAM memory VDDL is used as these memory devices are non-volatile
1+2		VPD is used to supply the serial memory at U8.
2+3	X	VDDL is used to supply the serial memory at U8.
Package Type		0R in SMD 0402
J20, J21		J20 and J21 serve to configure the CAN transceiver of both TouCAN channels on the MPC555. 82C250 (or compatible) devices are used as transceivers. The CAN signal rise time can be configured via a resistor tied to GND. With a 0R bridge against VDDH, the transceivers can be switched to stand-by mode.
1+2	X	0R resistor: minimal rise time
1+2		To reduce electromagnetic interference (EMI) a suitable size resistor can populate the module in support of lower CAN baud rates.
2+3		0R resistor: Stand-by
Package Type		SMD 0402

Table 2: Jumper Settings

[1]: Jumper J10 and J18 might vary because of different memory on the phyCORE-MPC555

4 Power System and Reset Behavior

The phyCORE-MPC555 must be supplied with two different supply voltages:

Supply Voltage 1: +3.3 V (VDDL)
Supply Voltage 2: +5 V (VDDH)

Caution:
Both supply voltages are necessary for the correct functioning of the phyCORE-MPC-555. Never attach a singel supply voltage to the phyCORE-MPC555. This might render the board inoperable.

The power supplies are connected to the module via two field effect transistors (FET). These FET switches can be switched off via software using the TEXPS bit found in the PLPRCR register. This supports the MPC555's "Power Down" power savings mode. *Figure 7* depicts the generation and the distribution of the supply voltages.

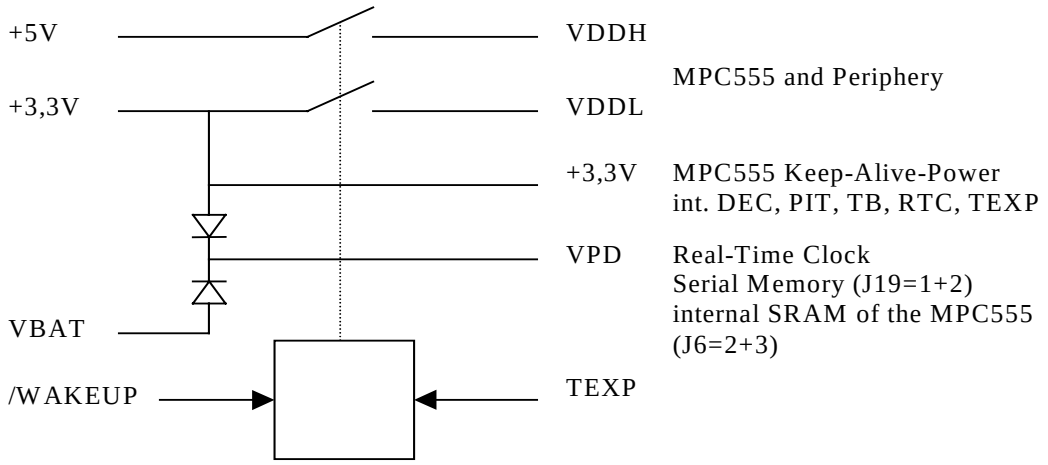


Figure 7: Power Concept

Power-On Behavior

When both supply voltages are attached to the corresponding ports of the module, a power-on reset (/PORESET) cycle will start. After successful completion of this cycle (/PORESET inactive), the hard-reset cycle is triggered. During the hard-reset cycle, the FET switch is automatically activated in order to set up the local supply voltages, VDDH and VDDL. The /HRESET cycle is fully completed when both local voltages have reached a valid level and the /HRESET timeout (ca. 25 ms) of the reset device has finished. The processor is now fully functional and will start program execution with the commands given at the reset exception (0x00000100 or 0xFFF00100).

Power-Off Behavior

If the power-down mode of the MPC555 has been programmed, the bit/signal TEXPS/TEXP will turn off the FET switches. The local supply voltages, VDDH and VDDL, will drop and the board will remain without current. Only the components in the MPC555 that control this mechanism are still supplied with power (direct from the +3.3 V input). The power consumption is reduced to a minimum. /PORESET and /HRESET remain inactive (high) during this state.

Wake-Up Behavior

After an event that negates the TEXP signal, the FET switch is activated again and the /HRESET cycle will start. Such an event can include a decrementor overflow, etc. A renewed /PORESET cycle will not run. Therefore the wake-up time of the processor depends only upon the /HRESET cycle. Events that do not originate from the MPC555 can also trigger a wake-up. Such events may include an alarm interrupt of the on-board Real-Time Clock (U10, RTC8563) or a low-level at the /WAKEUP port (pin X1C56 of the phyCORE-Connector). The alarm interrupt (/IRTC) must either be connected to the /WAKEUP signal of the board, via jumper J15, or brought back externally (pin X1D33 connected to pin X1C56). Even if the /IRTC is connected to /WAKEUP, additional input sources may be connected. For additional input sources, a wired-OR-connector (open-drain or open-collector transceiver) against GND is required.

5 Start-up System Configuration

The system configuration is done in multiple phases. This section describes the mechanism that is active up until execution of the initial software command.

Power-on Reset Phase
Hard-reset Phase
Initialization via software

5.1 Power-On Reset Phase

The processors clock generator is configured during the power-on reset phase. Solder jumpers J2, J3, and J4 are used to configure the clock mode. Depending on the desired clock source, a corresponding bit-pattern must be present at the processor lines MODCK[1..3] during the /PORESET phase. Because these signals are multiplexed with the interrupt inputs /IRQ5, /IRQ6, and /IRW7, no external hardware may interfere with these signals.

J2	J3	J4	Clock Mode
1 + 2	2 + 3	2 + 3	20 MHz quartz, limp mode activated (MODCK[1..3]=011)
1 + 2	1 + 2	2 + 3	20 MHz quartz, limp mode deactivated (MODCK[1..3]=001)
1 + 2	2 + 3	1 + 2	4 MHz quartz, limp mode activated (MODCK[1..3]=010)

Table 3: Clock Mode Configuration via Jumpers J2, J3 and J4

5.2 Hard Reset Configuration Word

The components of the MPC555 which are necessary for accessing and executing of the start-up code are initialized during the hard-reset phase. A data value, the hard-reset configuration word (HRCW), determines the initialization process. The HRCW can be supplied by various sources. Possible sources are the data bus, the internal (on-chip) Flash memory or an internal default data value.

The sources for the HRCW is determined by two conditions: setting of jumper J5 and the /HC bit in the internal Flash memory.

External HRCW

When the /HC bit in internal Flash memory is cleared (/HC=1) and J5 is closed at 1+2, the HRCW is read via the data bus. On the phyCORE, the data bus is connected with pull-down resistors (except D20). The signal level of D20 is configured to low or high via jumper J1. D20 determines the Flash memory that is active after reset (1+2 = internal Flash, 2+3 = external Flash).

Internal Default HRCW

If J5 is closed at 2+3 and /HC = 1 (Flash is cleared), then the internal default HRCW 0x00000000 is read.

Internal Flash HRCW (CMFCFIG)

If J5 is closed at pins 2+3 and /HC=0, the bit pattern (CMFCFIG) from the internal Flash is read.

6 System Memory

Two memory models can be distinuished when using the phyCORE-MPC555: the memory model that is active after reset and the runtime model. The runtime model is configurable by software.

6.1 Memory Model after Reset

The memory model after reset is defined through a special mechanism. While /HRESET is active, the memory model, as well as several other system configurations, are determined by the Hard Reset Configuration Word (HRCW).

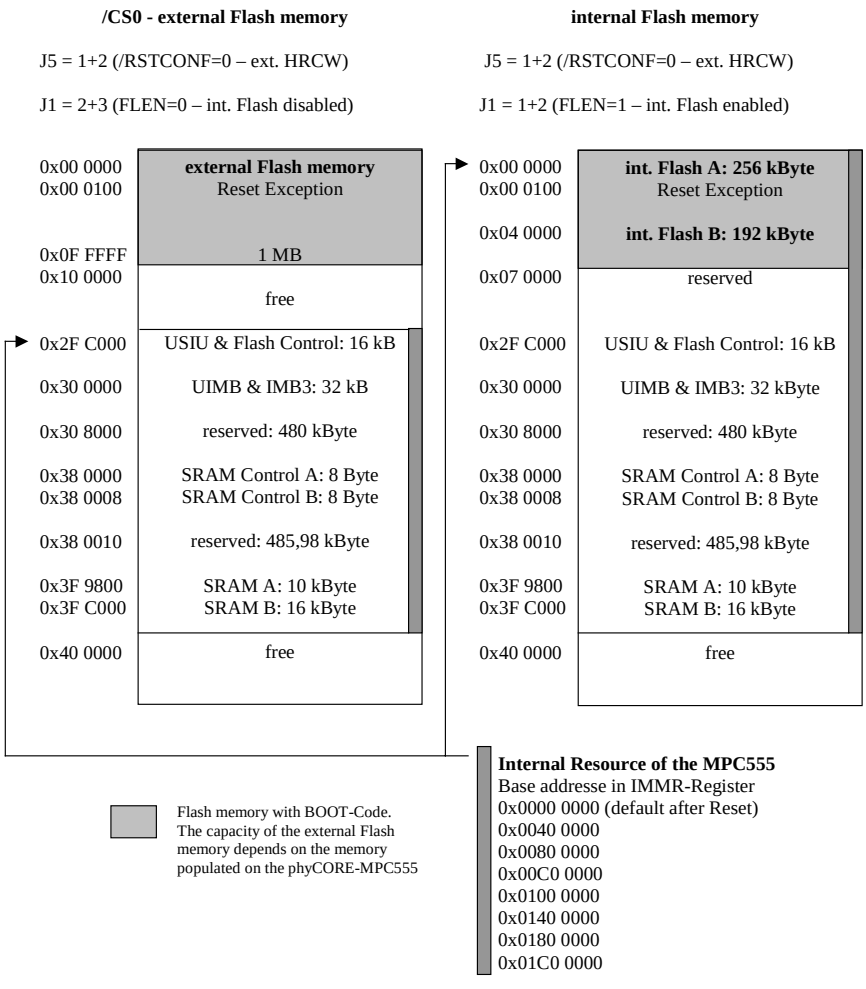


Figure 8: Default Memory Model after Hardware Reset

- Starting from external memory controlled by /CS0

  Configuration: J1=2+3 (FLEN bit in HRCW is zero)

After a reset, the address space for /CS0 is pre-initialized to 1 MB and begins from the absolute address 0x0000 0000. If the capacity of the external Flash memory exceeds 1 MB, the address mask in the OR0-register can be changed. Starting at address 0x002F 8000 the internal resources reside. The base address of the internal resources can be changed in the IMMR-register. There are seven configurations, as shown in *Figure 8.*

After reset the processor run code from the Reset Exception Location at address 0x0000 0100.

It is also possible to map the external Flash memory into a completely different address space. This is dependent on the application and is further determined by the runtime memory model.

- Starting from internal Flash memory

  Configuration: J1=1+2 (FLEN bit in HRCW is one)

After reset the internal Flash memory array is present from the absolute address 0x0000 0000. In this case Chip-Select channel 0 (/CS0) is disabled. During runtime, /CS0 can be re-enabled by software. The processor run code starting from the Reset Exception Location starting at 0x0000 0100.

6.2 Runtime Memory Model

The runtime memory model is configured by software in the internal register of the MPC555. A register set (BRx, ORx register) exists for each Chip-Select signal. In these registers, the base address, the size of the address space and the bus characteristic are configured.

/CS0 external on-board Flash memory
/CS1 external on-board synchronous BURST-SRAM
/CS2 free
/CS3 free

The runtime memory model is dependent on the application. *Table 4* shows example configurations.

Address Space	Space	Peripheral	MPC555 Register
0x0000 0000 0x0006 FFFF	448kByte	MPC555 on-chip Flash	IMMR[FLEN] = 1b IMMR[ISB]= 000b
0x002F C000 0x002F FFFF		MPC555 Periphery	IMMR[ISB]= 000b
0x0000 0000 0x007F 0000	8 MByte	/CS0 on-board Flash	IMMR[FLEN] = 0b BR0= 0x0000 0003 OR0= 0xFF80 0020
0x1000 0000 0x007F FFFF	8 MByte	/CS1 on-board SRAM	BR1= 0x1000 0001 OR1= 0xFF80 0000
0x2000 0000 0x20FF FFFF	16 MByte	/CS2 free	BR2= 0x2000 XXXX OR2= 0xFF00 XXXX
0x3000 0000 0x30FF FFFF	16 MByte	/CS3 free.	BR3= 0x3000 XXXX OR3= 0xFF00 XXXX

Table 4: Runtime Memory Map

The Flash memory space in *Table 4* is either external or internal dependent on the FLEN bit.
The register values for /CS2 and /CS3 depend on the connected peripherals. The places designated with an "X" determine the specific characteristics (bus-width, burst or non-burst, etc.) of the bus interface.

6.3 Flash Memory

6.3.1 Internal Flash Memory of the MPC555

To program the internal Flash memory of the MPC555, the on-chip Flash must first be unlocked with the EPEE signal. EPEE can be contacted via the pin X1D53 in the connector lining the edge of the module. EPEE is tied via a pull-down resistor to ground. This signal must be pulled to high for activation. Also EPEE controls switching of the internal Flash's supply voltage from VDDL to VDDH.

6.3.2 External Flash Memory (U2, U3)

Use of Flash as non-volatile memory provides the advantages of modern Flash technology. Various Flash devices can be used on the phyCORE-MPC555. The Flash memory devices used on the phyCORE-MPC555 operate in 16-bit mode and are organized in 32-bit with. The device at U2 connects to the low data bus while device U3 connects to the high data bus.

Type	Size	Manufacturer	Device Code	Manufacturer Code
29LV200T/B	256 kByte	AMD	223B/22BF	01
29LV200T/B	256 kByte	Fujitsu	223B/22BF	04
29LV200T/B	256 kByte	ST	0051/0057	20
29LV400T/B	512 kByte	AMD	22B9/22BA	01
29LV400T/B	512 kByte	Fujitsu	22B9/22BA	04
29LV400T/B	512 kByte	ST	00EE/00EF	20
29LV800T/B	1 MB	AMD	22DA/225B	01
29LV800T/B	1 MB	Fujitsu	22DA/225B	04
29LV800T/B	1 MB	ST	00D7/005B	20
29LV160T/B	2 MB	AMD	22C4/2249	01
29LV160T/B	2 MB	Fujitsu	22C4/2249	04
29LV160T/B	2 MB	ST	22C4/2249	20

Table 5: Flash Memory Device and Manufacturers Overview

Use of Flash memory enables in-circuit programming of the module. The Flash devices on the phyCORE-MPC555 are programmable at 3.3 VDC. Consequently, no dedicated programming voltage is required. As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

6.4 Synchronous BURST-SRAM (U4 – U7)

Use of synchronous flow-through BURST-SRAM supports the fastest MPC555 memory interface mode. The memory is organized in 32-bit width consisting of four banks. These banks appear to the processor as linear address spaces and do not require special activation. The SRAM is generally accessed via /CS1 without wait states.

The phyCORE-MPC555 can be populated with memory devices of various capacities. Generally, each memory bank can only be populated with memory devices of a consistent size. Configuration of the memory capacity is carried out by hardware using solder jumpers J10 and J18. *Table 6* shows all possible memory configurations.

Capacity	Type	Device	J18	J10
	-	-	-	-
128 kByte	32k x 32/36 bit	U4	1+4, 2+3	open
256 kByte	32k x 32/36 bit 64k x 32/36 bit	U4-5 U4	1+4, 2+3 3+6, 5+8	open open
384 kByte	32k x 32/36 bit	U4-6	1+4, 2+3	open
512 kByte	32k x 32/36 bit 64k x 32/36 bit 128k x 32/36 bit	U4-7 U4-5 U4	1+4, 2+3 3+6, 5+8 5+6, 7+8	open open open
768 kByte	64k x 32/36 bit	U4-6	3+6, 5+8	open
1 MB	64k x 32/36 bit 128k x 32/36 bit 256k x 32/36 bit	U4-7 U4-5 U4	3+6, 5+8 5+6, 7+8 4+7, 8+9	open open open
1.512 MB	128k x 32/36 bit	U4-6	5+6, 7+8	open
2 MB	128k x 32/36 bit 256k x 32/36 bit 512k x 32/36 bit	U4-7 U4-5 U4	5+6, 7+8 4+7, 8+9 6+9	open open closed
3 MB	256k x 32/36 bit	U4-6	4+7, 8+9	open
4 MB	256k x 32/36 bit 512k x 32/36 bit	U4-7 U4-5	4+7, 8+9 6+9	open closed
6 MB	512k x 32/36 Bit	U4-6	6+9	closed
8 MB	512k x32/36 bit	U4-7	6+9	closed

Table 6: Memory Options for the Synchronous BURST-SRAM

Caution:
The address space for the memory bank must always be configured to the maximum possible memory space. That means that if, for example, only one memory device with 256k x 32/36-bit capacity is populated, the address space has to be set to 4 MByte.

6.5 Serial Memory (U8)

The phyCORE-MPC555 is populated with a non-volatile memory device with a serial I^2C interface. This memory serves as storage for configuration data or parameters that must be protected in the event of a power failure. Various serial memory devices can be installed at U8, including EEPROM, FRAM, or SRAM. The capacity of these memory devices ranges from 512 Byte to 32 kByte.

When using SRAM at U8, solder jumper J19 must be connected at pins 1+2 to supply the memory device via VPD. Because the MPC555 has no I^2C interface, this protocol must be generated with software. The processor's port pins SGPIOC6 and SGPIOC7 are connected to SDA and SCL using resistors R39 and R38 per default. *Table 7* gives an overview of the possible devices for use at U8 as of the printing of this manual.

Type	**Size**	**I^2C Frequency**	**Address Pins**	**Write cycles**	**Life of Data**	**Device**	**Manufacturer**
EEPROM	256/512 Byte	400 kHz	A2, A1, A0	1 000 000	100 Years	CAT24WC02/04	CATALYST
	1/ 2 kByte	400 kHz	A2, A1, A0	1 000 000	100 Years	CAT24WC08/16	CATALYST
	4/8 kByte	400 kHz	A2, A1, A0	1 000 000	100 Years	CAT24WC32/64	CATALYST
	32 kByte	1 MHz	A1, A0	100 000	100 Years	CAT24WC256	CATALYST
FRAM	512 Byte	1 MHz	A2, A1	10 billion	10 Years	FM24CL04	RAMTRON
	8 kByte	1 MHz	A2, A1, A0	10 billion	10 Years	FM24CL64	RAMTRON
SRAM	256 Byte	100 kHz	A2, A1, A0	-	-	PCF8570	PHILIPS

Table 7: Memory Options for the Serial Memory U8

Note that the RTC is also connected to the I^2C bus. The RTC can operate with a bus frequency up to 400 kHz. It is advised not to allow higher bus frequency for the access to serial memory. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory can be configured via solder jumpers J16 (A1) and J17 (A2) in a manner that avoids signal collision. The address input A0 is hard-wired to GND.

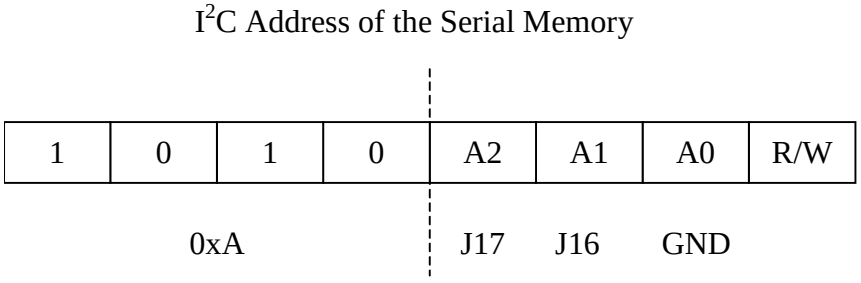


Figure 9: I²C Slave Address of the Serial Memory (U8)

Below are possible configurations:

I²C Address	**J16 A1**	**J17 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 8: I²C Address of the Serial Memory

When selecting the I²C slave address of the serial memory, please note that not all memory types make address pins A1 and A2 externally available to the user.

7 Serial Interfaces

7.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC555 at U11. This device adjusts the signal levels for the RXD1_TTL / RXD2_TTL and TXD1_TTL / TXD2_TTL lines. The RS-232 interface enables connection of the module to a COM-port on a host-PC. In this instance the RxD1 or RxD2 line (X1D22 / X1C21) of the transceiver are connected to the TxD line of the COM-port; while the TxD1 or TxD2 line (X1D23 / X1C23) are connected to the RxD line of the COM port. The ground circuitry of the phyCORE-MPC555 must also be connected to the applicable ground pin on the COM port.

The micrcontroller's on-chip UART does not support handshake signal communication. However, depending on user needs, hand shake communication can be replicated using port pins on the microcontroller. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the phyCORE module.

It is furthermore possible to externally use the TTL signals of both of the UART channels. These are located at X1C53, X1C54 (RXD2_TTL, TXD2_TTL) and X1D16, X1D15 (RXD1_TTL, TXD1_TTL) on the phyCORE-Connector. External connection of TTL signals is required for galvanic decoupling of the interface signals. Using solder jumpers J13 and J14, the TTL transceiver outputs of the on-board RS-232 devices can be disconnected from the receive lines RXD1_TTL and RXD2_TTL. This is required so that the external transceiver does not drive against the on-board transceiver. The transmit lines TXD1_TTL / TXD2_TTL can be connected parallel on the transceiver input without causing a collision.

7.2 CAN Interface

Two CAN transceivers (82C251 or 80C250) populate the phyCORE-MPC555 module at U12 / U13. These transceivers enable transmission and receipt of CAN signals via A_CNTx0 / A_CNRX0 and B_CNTx0 / B_CNRX0. The CAN transceivers support up to 1 Mbaud and up to 110 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). Additionally, the common mode voltage of both CAN transceivers must not exceed a certain threshold: -8V / +18V for the 82C250 and ±40V for the 82C251. If these thresholds cannot be adhered to, a galvanized decoupler must be installed. This is furthermore recommended for all large CAN networks. To decouple signals, the lines A_CANRX0 and B_CANRX0 must be disconected from the on-board transceiver ICs by means of jumpers J11 and J12. In order to ensure that the CAN transceivers do not use any unnecessary power, both can be switched to stand-by utilizing jumpers J20 and J21 (J20 / J21=2+3). The CAN TTL signals are routed to the pins of the phyCORE-Connector at X1D55, X1D56 (B_CNTX0, B_CNRX0) and X1D57, X1D58 (A_CNTX0, A_CNRX0)

A fast opto-coupler should be implemented to galvanically separate external CAN transceivers and the phyCORE-MPC555. It is recommended to use a Hewlett Packard HCPL06xx or a Toshiba TLP113 fast opto-coupler. Parameters for configuring a proper CAN-bus system are found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

In order to ensure proper message transmission via the CAN bus, a 120 Ohm terminating resistor must be connected to each end of the CAN bus between the pins delivering the CAN_H and CAN_L signals.

[1] CiA CAN in Automation -.Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

Configuration of the on-board transceiver:

Using jumpers J20 and J21, the transceivers at U12 and U13 can be switched to stand-by (2+3). Furthermore it is possible to configure the rise time using resistors to close both jumpers at 1+2 (leaving 2+3 open). With the usage of lower baud rates, this achieves a decrease of noise emissions on the CAN bus. Further information can be found in the data sheets for the Philips 82C250 / 82C251 transceiver chips.

7.3 BDM-Debug Interface

The MPC555 offers an on-chip Background Debug (BDM) interface. This interface allows external debug access to the controller without requiring any service software or firmware, such as a monitor program, on the chip. This internal debug interface furthermore contains hardware features supporting use with common cross development systems and debug environments, such as Metrowerks' CodeWarrior. For instance, the MPC555 features internal breakpoint registers enabling debugging in Flash-ROM memory.

The on-chip BDM interface extends from the MPC555 processor to the Molex connectors aligning the edges of the phyCORE module. External BDM signal converter circuitry, such as a Wiggler, enable connection of the MPC555 to a host-PC for purposes of debugging and code download. Please note that the Development Board for the phyCORE-MPC555 contains such BDM signal converter circuitry, through which decoded BDM signals are routed to a DB-25 connector at P1. This enables easy connection of the phyCORE-MPC555, as mounted on a Development Board, to a host-PC for start-up, download of user code and debugging.

In addition, the original BDM signals from the MPC555 processor are available on a 10-pin header connector at X4 on the phyCORE-MPC555 Development Board. Connection to other 3rd party BDM devices is possible using this BDM connector *(refer to Figure 10)*.

Figure 10 shows the pin assignment for the 10-pin BDM connector X4 on the phyCORE-MPC555 Development Board.

phyCORE Pin			**BDM Connector**				**phyCORE Pin**
X1D36	VFLS0	1	o	o	2	/SRESET	X1C10
X1C32	GND	3	o	o	4	DSCK	X1C35
X1D34	GND	5	o	o	6	VFLS1	X1D37
X1D10	/HRESET	7	o	o	8	DSDI	X1C33
X	VCC	9	o	o	10	DSDO	X1D35

Figure 10: 10-pin BDM Connector and Corresponding Pins of the phyCORE-Connector

X The supply voltage for the external BDM converter depends on the type used. *For additional information, please refer to the accompanying data sheet of the converter*.

8 Real-Time Clock RTC-8564 (U10)

The phyCORE-MPC555 is equipped with a Real-Time Clock. This RTC device provides the following features:

- Serial communication over the I^2C bus (address 0xA2) up to 400 kHz bus cycles
- Power consumption
  I^2C bus active (400 kHz): <1 mA
  I^2C bus inactive, CLKOUT pin inactive : <1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-MPC555 is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the I^2C bus (address 0xA2 / 0xA3) with the help of ports SGPIOC7 (SCL) and SGPIOC6 (SDA). In standard configuration, these processor port pins are connected to the I^2C bus using the 100 Ohm resistors R38 and R39. Since the MPC555 is not equipped with an internal I^2C controller, the protocol must be generated with software.

The Real-Time Clock also provides an interrupt output that is extended to the /WAKEUP signal via Jumper J15. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function the Real-Time Clock can be utilized in various applications. Closing Jumper J15 allows timed controlled wake-up of the phyCORE-MPC555, including start-up and operation out of power-down mode.

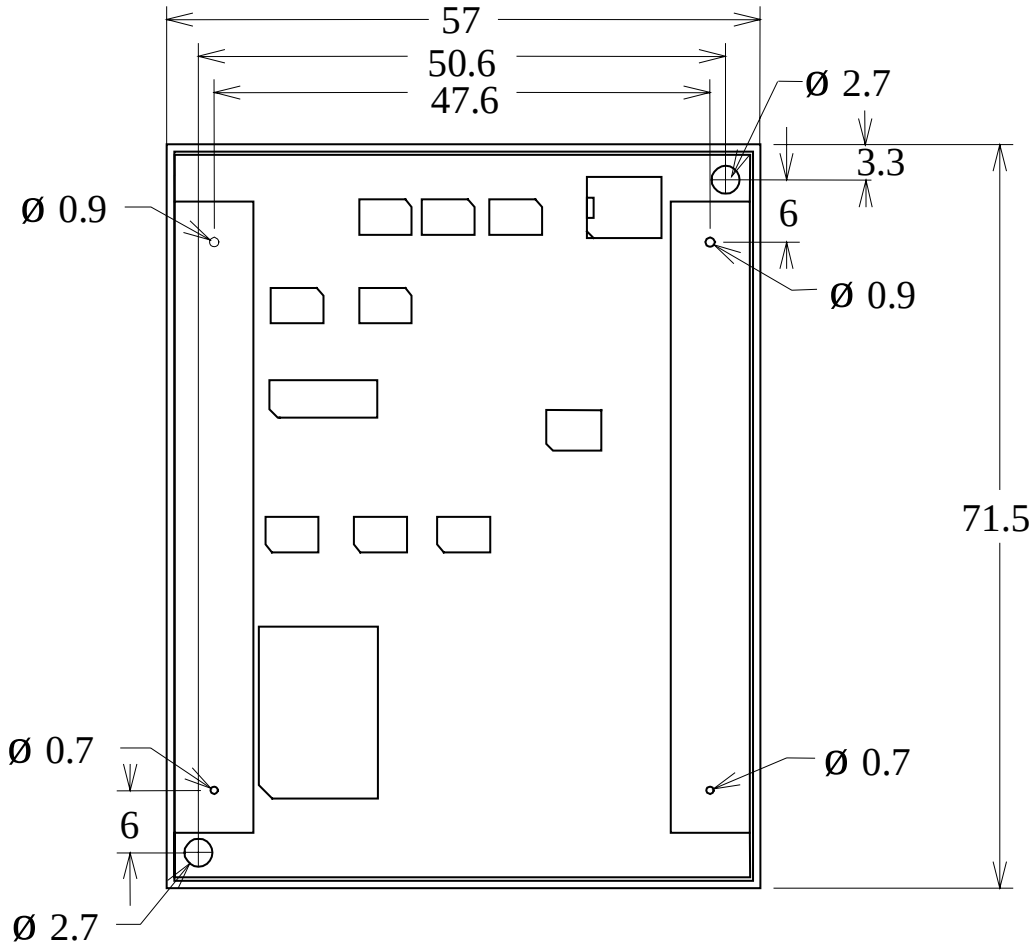
If the RTC interrupt should be used as a software interrupt which is connected to the corresponding interrupt input of the processor, the signal /IRTC must be externally connected with a processor interrupt input.

Additional information on the Real-Time Clock registers can be found in the accompanying RTC data sheet.

Caution:
After connection of the voltage supply or following a reset, the Real-Time Clock generates **no** interrupts, as the clock must first be initialized.

9 Technical Specifications

The physical dimensions of the phyCORE-MPC555 are represented in *Figure 11*.



Measurements are in mm

Figure 11: Physical Dimensions

The height of all components on the top side of the PCB is ca. 4.5 mm. The PCB itself is approximately 1.25 mm (+/- 10%) thick[1]. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 2 mm.

Additional Technical Data:

Parameter	Requirements	Characteristics
Dimensions		72 mm x 57 mm
Weight		ca. 25 g with max. memory
Humidity		max. 95 % r.F. not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range: Standard Extended		 0 °C to +70 °C -40 °C to +90 °C
Operating voltages: Voltage 3.3V Voltage 5V Battery		 3.3 V ± 5 % 5 V ± 5 % VBAT: 3 V-10 %
Operating Power Consumption: Voltage 3.3V Voltage 5V Voltage 3.3V Voltage 5V	40 MHz frequency 1 MByte SRAM 512 kByte Flash 4 MByte SRAM 4 MByte Flash	 Typ. 300 mA Typ. 40 mA[2] Typ. 620 mA Typ. 40 mA[2]
Battery power supply: RTC and internal SRAM in MPC555	VBAT = 3 V Voltage 5 V = 0 V Voltage 3.3 V = 0 V	Less than 10 µA

Table 9: Technical Data

These data apply to the standard configurations at the time of printing of this manual.

[1] : Applies to all PCBs 1169.2 and higher. PCB thickness for earlier PCB versions was 1.1 mm.
[2]: Without I/O access and load of MIOS, TPU, ADC etc.

Connectors on the phyCORE-MPC555:

Contact rows on the module:

Manufacturer:	Molex
Number of pins per contact rows:	160 (2 rows of 80)
Molex part number:	52760-1679 (lead free)
PHYTEC part number:	VM042

The Molex connectors mating with the ones populating the phyCORE-MPC555 are available in two different sizes. The mated height given describes the distance between the two PCBs they connect.

- Component height 5 mm, mated height 6 mm

Number of pins per contact row:	160 (2 rows of 80)
Molex part number:	55091-1679 (lead free)
PHYTEC part number:	VB082

- Component height 9 mm, mated height 10 mm

Number of pins per contact row	160 (2 rows of 80)
Molex type number	53553-1679 (lead free)
PHYTEC part number:	VB085

The corresponding mechanical diagrams of the contact elements can be found at www.molex.com.

In order to accurately calculate the free space available given the spacing over the PCB provided by the Molex connectors, the maximum height of the components on the underside of the phyCORE must be subtracted from the profile of the Molex connectors. For instance, a 10 mm high Molex connector yields 8 mm of space (10 mm less 2 mm) between the phyCORE-MPC555 and target circuitry into which it is integrated.

10 Hints for Handling the Module

Handling of the quartz on the phyCORE-MPC555

Removal of the standard quartz is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the boards as well as surrounding components and sockets remain undamaged while unsoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-MPC555 in Application Circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals that are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

11 Revision History

Date	Version numbers	Changes in this manual
11-Dec-2000	Manual L-523e_1 PCM-001 PCB# 1169.0 PCM-995 PCB# 1174.0	First edition.
01-Aug-2001	Manual L-523e_2 PCM-001 PCB# 1169.0 PCM-995 PCB# 1174.0	Minor revisions regarding spelling errors and conventions. Paragraph 4 in Appendix added.
30-Apr-2003	Manual L-523e_3 PCM-001 PCB# 1169.2 PCM-995 PCB# 1174.0	Description extended to PCB# 1169.2. Major revisions in sections *6.1* and *6.2*. Paragraph 2 and 3 in Appendix have been revised. This revision history table added.
12-Feb-2004	Manual L-523e_4 PCM-001 PCB# 1169.5 PCM-995 PCB# 1174.1	Top and bottom view to match PCB# 1169.5 inserted, section *1.2* Pinout *Table 1* adjusted to match PCB# 1169.5. Table 7 for serial memory (U8) and *Table 9* in Technical Specifications revised.
04-July-2005	Manual L-523e_5 PCM-001 PCB# 1169.5 PCM-995 PCB# 1174.1	*Section 9, "Technical Specifications"* PCB thickness corrected and Molex part numbers adjusted to lead free version.

Appendices A

A.1 Release Notes

The following section contains infomation about deviations to the description in this manual.

Changes in revision: PCB1169.0 through 1169.5

1. If the GAL P640 is installed , the function of Jumpers J2, J3, J4 and J5 is different to what's described in *section 3:*

J5, J3, J4		These jumpers configure the clock mode of the MPC555. During the active phase of /PORESET, the bit pattern available on the MODCK [1..3] pins is read by the MPC555 processor. Only the standard configurations using the MPC555's oscillator and quartz are shown below. The default configuration depends on the frequency of the external quartz populating the module. Configuration options for using an external clock source can be found in the MPC555 user's manual.
1+2, 2+3, 2+3	X	20 MHz Quartz, limp-mode activated (MODCK[1..3]=011)
1+2, 1+2, 2+3		20 MHz Quartz, limp-mode deactivated (MODCK[1..3]=001)
1+2, 2+3, 1+2		4MHz Quartz, limp-mode activated (MODCK[1..3]=010)
Package Type		0R in SMD 0402
J2		J2 determines the source of the Hard Reset Configuration Word (HRCW). During /HRESET, the HRCW configures the MPC555 processor.
1+2	X	The HRCW is read via the data bus. Except D20, the data bus is connected to pull-down resistors and accordingly guarantees a valid data word. J1 configures D20 and determines the internal or external Flash memory as boot code source.
2+3		The internal default word is read as HRCW
Package Type		0R in SMD 0402

2. The power-down feature is currently not supported due to a problem with the MPC555 processor.

3. None of the PCB revisions supports the ready/busy function on /IRQ5 (MODCK1). If the /IRQ5 is to be controlled externally using push button S5 of the Development Board PCM-995, then R37 must be removed.

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Document number: **L-523e_5, July 2005**

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Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by

PHYTEC

Ordering No. L-523e_5
Printed in Germany