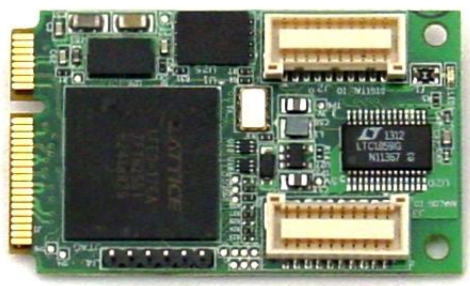
DS-MPE-DAQ0804

PCIe MiniCard Data Acquisition Port Module

Rev A.1 June 2015



Revision	Date	Comment
A.0	8/27/2014	Initial release
A.1	6/18/2015	Updated

FOR TECHNICAL SUPPORT PLEASE CONTACT:

support@diamondsystems.com

Diamond Systems Corporation
555 Ellis Street
Mountain View, CA 94043 USA
Tel 1-650-810-2500
Fax 1-650-810-2525
www.diamondsystems.com

CONTENTS

1. IMPORTANT SAFE HANDLING INFORMATION

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

This board contains a high density connector with many connections to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor’s) embedded computer boards.

ESD damage – This type of damage is usually almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board eventually simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced. To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply (i.e. almost all ICs). In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Overvoltage on digital I/O line – If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit

2. INTRODUCTION

2.1 Description

The DS-MPE-DAQ0804 is a rugged data acquisition PCIe MiniCard module with both analog and configurable digital I/O. It offers 8 single ended or 4 differential 16-bit analog inputs with an aggregate maximum sample rate of 100KHz, 2048 sample A/D FIFO, 4 16-bit analog outputs, and 14 configurable digital I/O lines. The buffered digital I/O lines can be optionally configured as either pulse width modulators or counter/timers. Diamond System' Universal Driver software provides driver support for all functions.

2.2 Features

- 8 single ended / 4 differential 16-bit analog inputs
- 100KHz maximum aggregate sample rate
- 2048 sample A/D FIFO with programmable threshold
- 4 analog input ranges: +/-10V, +/-5V, 0-10V, 0-5V
- 4 16-bit analog outputs
- 2 analog output ranges: 0-5V, 0-2.5V
- 14 digital I/O lines optionally configurable as:
  - 4 24-bit pulse width modulators
  - 8 32-bit counter/timers
- Latching connectors for increased ruggedness
- Universal Driver support for all functions

2.3 Operating System Support

- Linux 3.2.x
- Windows Embedded Standard 7, XP

2.4 Mechanical, Electrical, Environmental

- PCIe MiniCard full size format
- Dimensions: 50.95mm x 30mm (2" x 1.18")
- -40°C to +85°C ambient operating temperature
- Power input requirements: +3.3VDC +/- 5

2.5 Models

The DS-MPE-DAQ0804 product is available in two models as described below.

Product Number	Description
DS-MPE-DAQ0804	Analog I/O PCIe MiniCard Module with 8 A/D, 4 D/A & 14 DIO
DS-MPE-DAQ0800	Analog I/O PCIe MiniCard Module with 8 A/D & 14 DIO

3. PACKING LIST

The DS-MPE-DAQ0804 product comes with the PCIe MiniCard hardware assembly, a cable kit with one digital and one analog cable, and a hardware kit containing mounting screws.

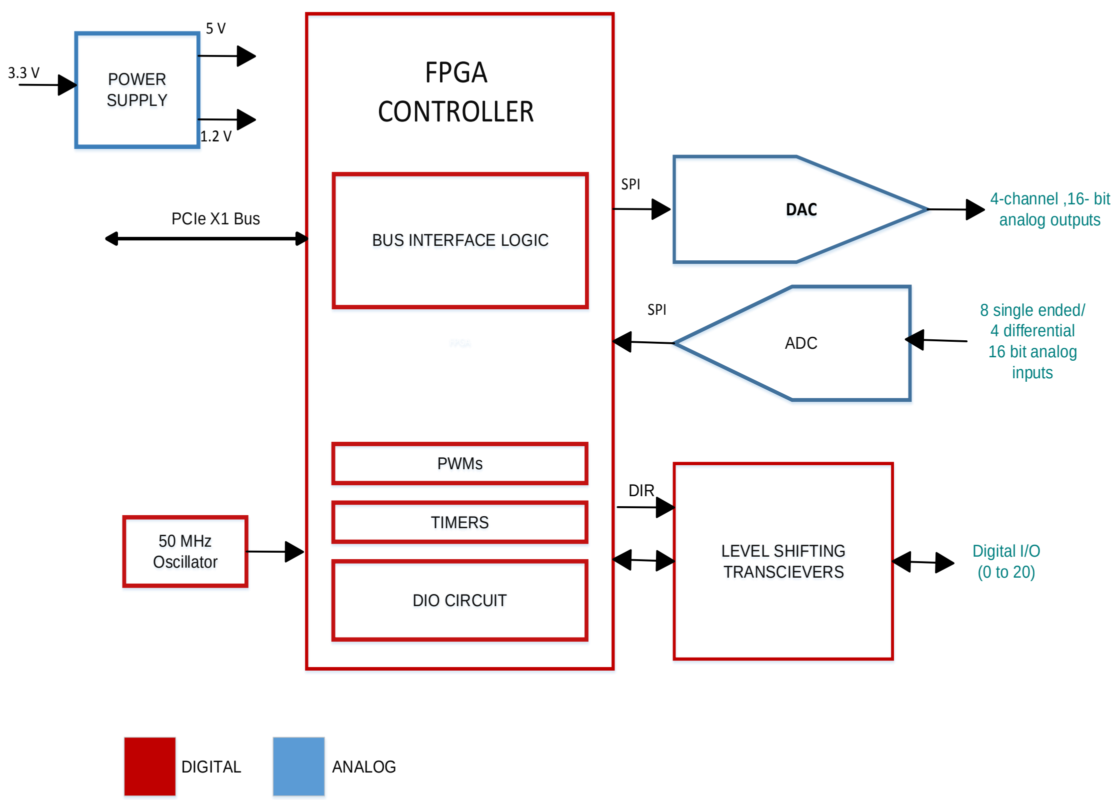
Quantity	Part Number	Description
1	915047x	DS-MPE-DAQ080x hardware assembly
1	6800502	Hardware Kit with mounting screws
1	CK-DAQ02	Cable Kit with analog and digital cables

4. FUNCTIONAL OVERVIEW

The DS-MPE-DAQ0804 is a PCIe MiniCard I/O module containing a combination of A/D, D/A, and DIO features using a PCIe interface. The A/D and D/A circuits are based on a high-integration A/D chip, LTC1859, with built-in single-ended/differential multiplexor and input range select circuit. A quad D/A chip AD5696 is used for the D/A features. Both analog components are powered by +5VDC and have their own integrated precision, low-drift voltage references.

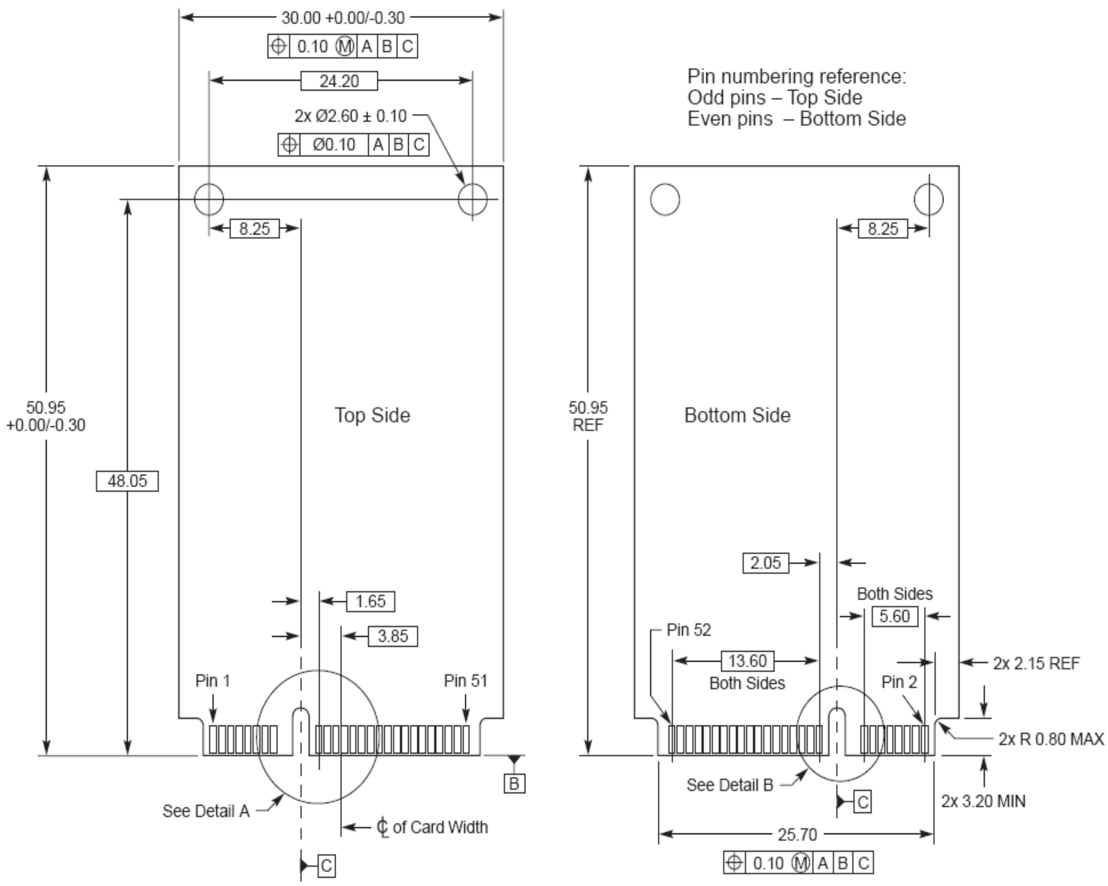
4.1 Functional Block Diagram

The DS-MPE-DAQ0804 block diagram is shown below.



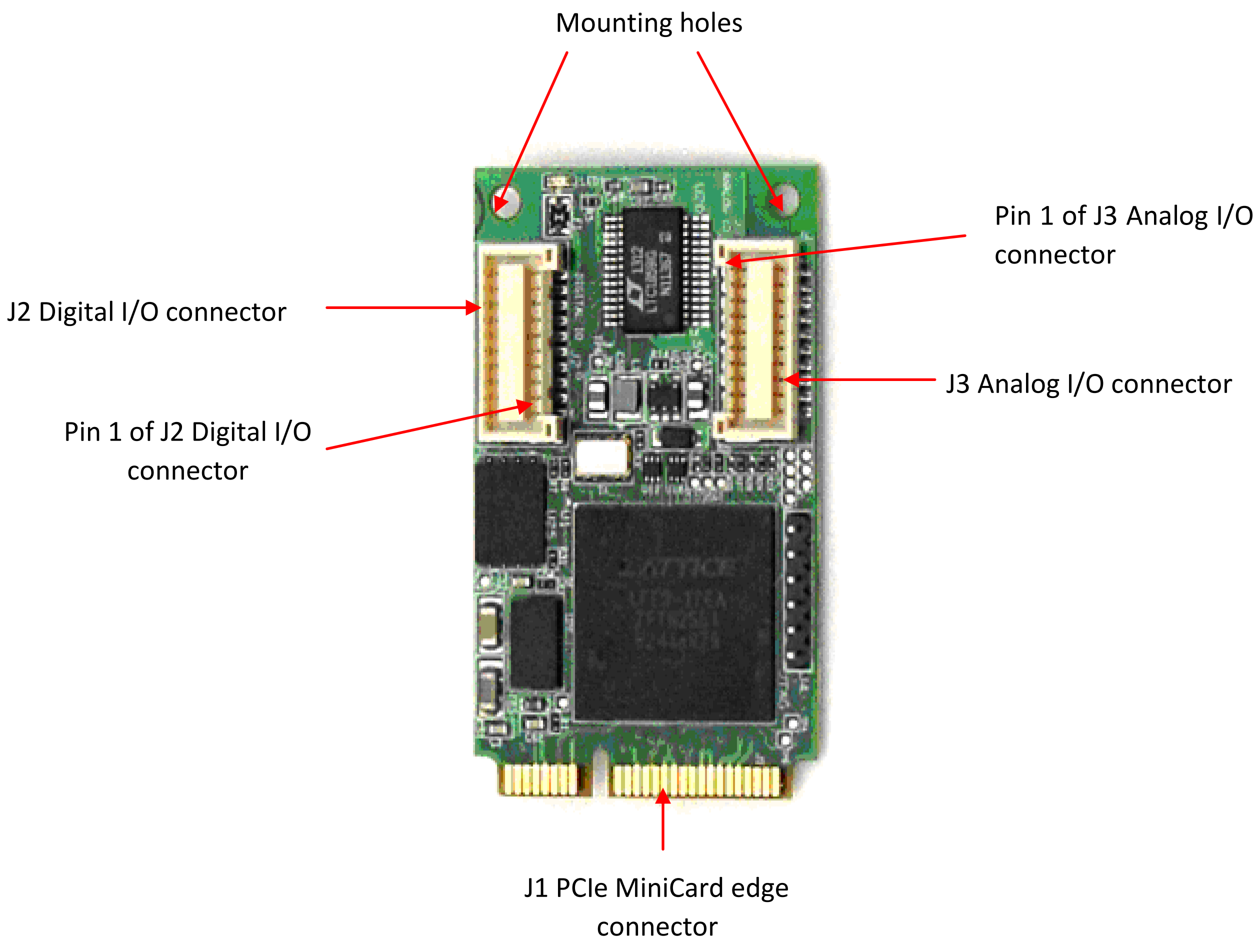
4.2 Mechanical Board Drawing

The DS-MPE-DAQ0804 conforms to the PCIe MiniCard electromechanical specification revision 1.2, full size format. Overall dimensions are 50.95mm L x 30.00mm W. The two mounting holes are isolated from the CPU ground and not connected to any ground lines.



5. INSTALLATION

The DS-MPE-DAQ0804 plugs in to any socket meeting the PCIe MiniCard specifications. It has two connectors, one for the analog I/O and one for the digital I/O, and a pair of mounting holes. To install the DS-MPE-DAQ0804, fully insert the board into a PCIe MiniCard connector and secure in place by inserting one screw from the hardware kit into each of the mounting holes, see the diagram below.



6. CONNECTOR PINOUT AND PIN DESCRIPTION

6.1 PCIe MiniCard Edge Connector (J1)

The DS-MPE-DAQ0804 module is compatible with the standard Mini PCIe socket pin out as shown below.

WAKE#	1	2	+3.3VAUX_3
COEX1	3	4	GND9
COEX2	5	6	+1.5V_1
CLKREQ#	7	8	UIM_PWR
GND1	9	10	UIM_DATA
REFCLK-	11	12	UIM_CLK
REFCLK+	13	14	UIM_RESET
GND2	15	16	UIM_VPP
	KEY		
RSVD(UIM_C8)	17	18	GND10
RSVD(UIM_C4)	19	20	W_DISABLE#
GND3	21	22	PERST#
PERN0	23	24	+3.3VAUX_4
PERP0	25	26	GND11
GND4	27	28	+1.5V_2
GND5	29	30	SMB_CLK
PETN0	31	32	SMB_DATA
PETP0	33	34	GND12
GND6	35	36	USB_D-
GND7	37	38	USB_D+
+3.3VAUX_1	39	40	GND13
+3.3VAUX_2	41	42	LED_WWAN#
GND8	43	44	LED_WLAN#
RSVD1	45	46	LED_WPAN#
RSVD2	47	48	+1.5V_3
RSVD3	49	50	GND14
RSVD4	51	52	+3.3VAUX_5

6.2 Digital I/O (J2)

The digital I/O signals are provided on a miniature 20-pin latching connector (J2).

DIO 0	1	2	DIO 1
DIO 2	3	4	DIO 3
DIO 4	5	6	DIO 5
CTR 0 I/O / DIO 6	7	8	DIO 7 / CTR 1 I/O
CTR 2 I/O / DIO 8	9	10	DIO 9 / CTR 3 I/O
CTR 4 I/O / DIO 10	11	12	DIO 11 / CTR 5 I/O
CTR 6 I/O / DIO 12	13	14	DIO 13 / CTR 7 I/O
PWM 0 Out / DIO 14	15	16	DIO 15 / PWM 1 Out
PWM 2 Out / DIO 16	17	18	DIO 17 / PWM 3 Out
+3.3V (fused)	19	20	Digital Ground

Connector Part Number / Description
JST BM20B-GHDS-G-TF 20-pin (2x10) 1.25mm pitch vertical SMT latching connector

6.3 Analog I/O (J3)

The analog I/O signals are provided on a miniature 20-pin latching connector (J3).

D/A 0	**1**	**2**	D/A 1
D/A 2	**3**	**4**	D/A 3
Analog Ground	**5**	**6**	Analog Ground
A/D 0	**7**	**8**	A/D 1
A/D 2	**9**	**10**	A/D 3
A/D 4	**11**	**12**	A/D 5
A/D 6	**13**	**14**	A/D 7
Analog Ground	**15**	**16**	Analog Ground
DIO 18	**17**	**18**	DIO 19 / A/D ext trigger
D/A ext trigger / DIO 20	**19**	**20**	Digital Ground

Connector Part Number / Description
JST BM20B-GHDS-G-TF 20-pin (2x10) 1.25mm pitch vertical SMT latching connector

7. ARCHITECTURE OVERVIEW

7.1 Bus Interface

The FPGA utilizes a PCI Express x1 bus interface. The design includes a PCIe core to implement the PCIe interface.

7.2 FPGA

The FPGA is a Lattice Semiconductor ECP3 family (LFE3) in BGA256 package. The FPGA includes an SPI core to gain access to the FPGA configuration flash memory. This allows the FPGA code to be updated in the field without requiring a JTAG cable or 3rd party software.

7.3 A/D Circuit

The module uses the Linear Technology LT1859 high-integration A/D converter chip for the A/D functionality and includes the following features:

- 16-bit A/D with 100KHz sampling rate
- 8 channel single ended / 4 channel differential multiplexor
- Input protection up to +/-25V
- Programmable input ranges: 0-10V, 0-5V, +/-10V, +/-5V
- Precision 2.5V low-drift reference voltage

7.4 D/A Circuit

The module uses the Analog Devices AD5686R D/A converter chip for the D/A functionality and includes the following features:

- 4 channel 16-bit D/A
- Single channel and simultaneous update modes
- Programmable output ranges: 0-2.5V, 0-5V
- Precision 2.5V low-drift reference voltage

7.5 Digital I/O

The 14 digital I/O lines are provided by the FPGA. They can operate in simple I/O mode in the form of 8-bit and 1-bit ports or in counter/timer and pulse width modulator modes. All bits have independent 1-bit drivers with independent direction control.

The digital I/O output voltage is +3.3V. The digital I/O lines can be software-configured for pull-up / down resistors. All lines are configured together for up or down.

7.6 Counter Timers and Clock Sources

The FPGA offers 8 32-bit counter/timers with programmable up/down counting, divide-by-n function, and square wave / pulse output. The Counters can be latched and read while counting.

7.7 Pulse Width Modulators

The FPGA includes 4 24-bit pulse-width modulator (PWM) circuits. Each circuit includes a period register as well as a duty cycle register. Both registers may be updated in real-time without stopping the PWM. Duty cycles from 0-100% inclusive are supported, as well as both positive and negative output polarity. The PWM clock may be selected from the on-board 50MHz clock or a 1MHz clock derived from the 50MHz clock. The PWM outputs are enabled on general purpose I/O pins with limited voltage and current capability. The user must determine whether these pins provide the appropriate voltage and current levels for the intended application or whether additional buffering or amplification is required.

.

7.8 Interrupt Circuit

Interrupts enable the board to request service independently of the program operation, typically in response to a user defined time interval or external event. The board supports interrupts from variety of sources including the digital I/O channels and counters/timers. The application is responsible for providing the interrupt service routine to respond to the interrupt request. An unserviced interrupt request may cause unpredictable 11ibble11. Diamond's Universal Driver software includes built-in interrupt handling routines that can link to user-defined code. This software lets you define the conditions that will generate an interrupt and then define the behavior of the system when an interrupt occurs.

8. ANALOG OUTPUT TECHNOLOGY OVERVIEW

8.1 D/A Circuit: Output Ranges and Resolution

The D/A circuit uses the Analog Devices AD5686R 4-channel 16-bit D/A converter. Pins P_DASCLK, P_DASDI, P_DASDO, P_DASYNC-, and P_DALDAC- control data transfer to the AD5686R. See the datasheet for timing requirements of these signals.

Name	Type	Reset	Description
P_DASCK	O	00	D/A serial clock
P_DASDI	O	0	D/A serial data in (from FPGA to DAC)
P_DASDO	I	Pulldown	D/A serial data out (from DAC to FPGA)
P_DASYNC-	O	1	D/A SPI interface synchronize signal
P_DALDAC-	O	1	D/A load command
P_DARANGE	O	0	D/A output range; 0 = 0-2.5V, 1 = 0-5V
P_DARESET-	O	1	D/A reset

Each output channel can be updated individually, or any number of channels can be updated simultaneously. Simultaneous update is useful when the application requires precise timing to avoid distortion or errors in the behavior of the controlled device.

The output range is the range of possible output values, from the smallest (lowest) value up to the highest (largest) value. The difference between the highest and lowest output value is called the span. For a +/-5V output range, the span is 10V.

The smallest change in output value, or resolution, is equal to 1/2n x the span, in which n = the number of bits (in this case 16). For a +/-5V output range, the resolution is 10V / 65535 = 153uV. This smallest change is commonly referred to as 1 LSB or the Least Significant Bit.

The DS-MPE-DAQ0804 uses straight binary coding for all output values; the range of output codes is 0-65535. The theoretical top value, 65536, requires 17 bits to be represented in binary form, which is unachievable in a 16-bit value. Therefore the top value of each output range is unavailable, and instead the maximum output value is 1 LSB less than the top value. Because the lowest output code is always 0, which is represented in binary form, the bottom value of each range is always equal to the exact nominal value of the range (within tolerance of the accuracy).

The conversion formula for analog outputs is the same for all ranges and is shown below.

Output V = (D/A code / 65536) x Span + Minimum output value

On power-up or when the board is reset, all pins are set to a tristate mode. Please refer to the D/A initialization sequence described later.

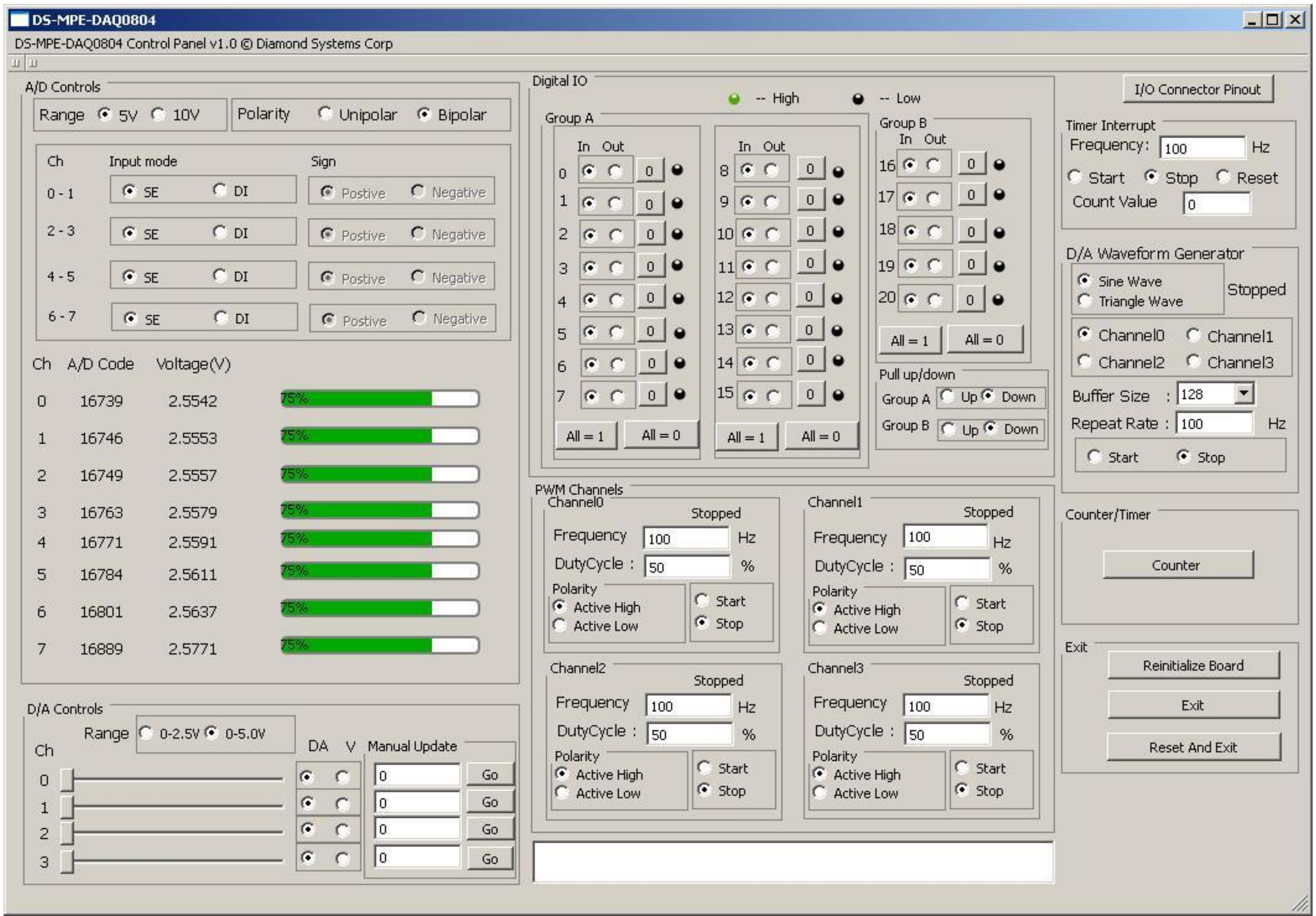
9. SOFTWARE DRIVER OVERVIEW

The DS-MPE-DAQ0804 module is configured by software. The board must first be initialized and then configured. These operations can be done either using Diamond's Universal Driver (version 7.0 or higher) or by an independent set of equivalent register operations. Please refer to the DS-MPE-DAQ0804 Control Panel Manual and DS-MPE-DAQ0804 Universal Driver Software User Manual for additional information.

9.1 Configuring Using Universal Driver

Diamond Systems' provides a device driver which will enable access to the board functionalities via an easy to use API set. This driver is called the Universal Driver and is available in Windows XP and Linux 2.6.xx operating systems. The details on the Universal driver can be found in the Universal Driver manual and can be accessed online at http://docs.diamondsystems.com/dscud/manual_Main+Page.html. The Universal Driver software comes on the Diamond System' Resource CD shipped with this product, or may be downloaded from the DS-MPE-DAQ webpage at http://www.diamondsystems.com/products/dsmpedaq0804.

The main screen of the graphical user interface is shown below.



9.2 Configuring Using Register Operations

The board can also be controlled using simple register read/write commands if you write your own driver. In typical modern operating systems, the user level applications cannot directly access the low level system information and don't have register level access. In order to communicate with any PCI device, a device driver is required.

The Universal Driver software can also be used to do register-level control, and a programmer can develop their own driver functionality that uses simple register read/write command after performing a PCI scan using the Universal Driver. Users of this type of access need to understand the board register map. This type of approach is suitable for someone who is very aware of the nature of low-level operations of hardware.

9.2.1 Interrupt level

Interrupts are used for hardware I/O operations that are independent of normal program flow. The DS-MPE-DAQ0804 can be set up to generate interrupts under several circumstances. The board can generate interrupts to transfer digital data into the board, as well as at regular intervals according to a programmable timer on the board. Individual control bits are used to enable each type of interrupt.

Since the DS-MPE-DAQ0804 board works on PCI Express bus architecture, the interrupt level is obtained as a result of a PCI scan performed by the device driver. To obtain the interrupt level used by the board, Diamond provides a default device driver, WinDriver, which can perform low level PCI commands and provide user level access to the board.

If you do not wish to use this driver and would like to develop your own driver, you need to be knowledgeable on the PCI / PCI express system architecture as well as the device driver model and architecture details for your chosen operating system.

10. SPECIFICATIONS

Analog inputs	8 16-bit single ended, 4 16-bit differential
Sample rate	100KHz maximum aggregate
Input ranges	+/-10V, +/-5V, 0-10V, 0-5V
A/D FIFO	2048 samples with programmable threshold
Input overvoltage protection	+/-25V
A/D clocking	Internal counter / timer, software command, or external clock
Analog input error	+/-28LSB (+/-0.04%) max zero scale error (no offset adjustment)
Analog outputs	4 16-bit
Output ranges	0-5V, 0-2.5V
Output updates	Simultaneous or individual channel
Output current	Up to 5mA per channel (1Kohm minimum load)
Output drift	Low drift 2ppm/^{o}C internal reference
Output error	+/-1.5mV (+/-0.03%) max zero scale error (no offset adjustment)
Analog calibration	Factory calibration for full-scale
Digital I/O	14 lines with 1-bit buffers for bit-by-bit individual direction control
DIO output voltage	+3.3V
DIO pull-up / pull-down	Software selectable
Pulse width modulators	4 24-bit, 0-100% duty cycle
Counter / timers	8 32-bit programmable
Input power	+3.3VDC +/-5%
Power consumption	0.462W @ 3.3V
Software drivers	Windows Embedded Standard 7, XP Linux 3.2.x
Universal Driver	Support for all functions
Operating temperature	-40°C to +85°C
Operating humidity	5% to 95% non-condensing
MTBF	xxx hours
Dimensions	50.95mm x 30mm (2” x 1.18”)
Weight	8.5g (0.3oz)
RoHS Compliant	Yes