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MC56F8346EVMUM/D
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# 56F8346 Evaluation Module

# User Manual

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# Preface

This reference manual describes in detail the hardware on the 56F8346 Evaluation Module.

**Note:** The 56F8346EVM board may have an obsolete part number, DSP56F836EVM.

## Audience

This document is intended for application developers who are creating software for devices using the Motorola 56F8346 part.

## Organization

This manual is organized into two chapters and two appendixes.

- Chapter 1,Introduction provides an overview of the EVM and its features.
- Chapter 2, Technical Summary - describes in detail the 56F8346 hardware.
- Appendix A, 56F8346EVM Schematics - contains the schematics of the 56F8346EVM.
- Appendix B, 56F8346EVM Bill of Material - provides a list of the materials used on the 56F8346EVM board.

## Suggested Reading

More documentation on the 56F8346 and the 56F8346EVM kit may be found at URL:

**www.motorola.com/semiconductors**

## Notation Conventions

This manual uses the following notational conventions:

| Term or Value | Symbol | Examples | Exceptions |
|---|---|---|---|
| Active High Signals (Logic One) | No special symbol attached to the signal name | A0<br>CLKO | |
| Active Low Signals (Logic Zero) | Noted with an overbar in text and in most figures | $\overline{WE}$<br>$\overline{OE}$ | In schematic drawings, Active Low Signals may be noted by a backslash: /WE |
| Hexadecimal Values | Begin with a "$" symbol | $0FF0<br>$80 | |
| Decimal Values | No special symbol attached to the number | 10<br>34 | |
| Binary Values | Begin with the letter "b" attached to the number | b1010<br>b0011 | |
| Numbers | Considered positive unless specifically noted as a negative value | 5<br>-10 | Voltage is often shown as positive: +3.3V |
| Blue Text | Linkable on-line | ...refer to Chapter 7, License | |
| Bold | Reference sources, paths, emphasis | ...see: **http://www.motorola.com/ semiconductors...** | |

## Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

| | |
|---|---|
| **A/D** | Analog-to-Digital; a method of converting Analog signals to Digital values |
| **ADC** | Analog-to-Digital Converter; a peripheral on the 56F8346 part |
| **CAN** | Controller Area Network; serial communications peripheral and method |
| **CiA** | CAN in Automation; an international CAN user's group that coordinates standards for CAN communications protocols |
| **D/A** | Digital-to-Analog; a method of converting Digital values to an Analog form |
| **DSP** | Digital Signal Processor or Digital Signal Processing |

| | |
|---|---|
| **56F8346** | Hybrid controller with motor control peripherals |
| **EOnCE** | Enhanced On-Chip Emulation; a debug bus and port created by Motorola to enable a designer to create a low-cost hardware interface for a professional quality debug environment |
| **EVM** | Evaluation Module; a hardware platform which allows a customer to evaluate the silicon and develop his application |
| **FlexCAN** | Flexable CAN Interface Module; a peripheral on the 56F8346 part |
| **GPIO** | General Purpose Input and Output port on Motorola's family of hybrid controllers; does not share pin functionallity with any other peripheral on the chip and can only be set as an input, output or level-sensitive interrupt input |
| **IC** | Integrated Circuit |
| **JTAG** | Joint Test Action Group; a bus protocol/interface used for test and debug |
| **LED** | Light Emitting Diode |
| **LQFP** | Low-profile Quad Flat Package |
| **MPIO** | Multi Purpose Input and Output port on Motorola's family of hybrid controllers; shares package pins with other peripherals on the chip and can function as a GPIO |
| **OnCE™** | On-Chip Emulation, a debug bus and port created by Motorola to allow a means for low-cost hardware to provide a professional-quality debug environment |
| **PCB** | Printed Circuit Board |
| **PLL** | Phase Locked Loop |
| **PWM** | Pulse Width Modulation |
| **QuadDec** | Quadrature Decoder; a peripheral on the 56F8346 part |
| **RAM** | Random Access Memory |
| **R/C** | Resistor/Capacitor Network |
| **ROM** | Read-Only Memory |
| **SCI** | Serial Communications Interface; a peripherial on Motorola's family of hybrid controllers |
| **SPI** | Serial Peripheral Interface; a peripheral on Motorola's family of hybrid controllers |
| **SRAM** | Static Random Access Memory |
| **UART** | Universal Asynchronous Receiver/Transmitter |
| **WS** | Wait State |

# References

The following sources were referenced to produce this manual:


[1] *DSP56800E Reference Manual*, DSP56800ERM/D; Motorola

[2] *56F8300 Peripheral User Manual*, MC56F8300UM/D; Motorola

[3] *56F8346 Technical Data*, MC56F8346/D; Motorola

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

# Chapter 1
# Introduction

The 56F8346EVM is used to demonstrate the abilities of the 56F8346 and to provide a hardware tool allowing the development of applications that use the 56F8346.

The 56F8346EVM is an evaluation module board that includes a 56F8346 part, peripheral expansion connectors, a CAN interface, 512KB of external memory and a pair of daughter card connectors. The daughter card expansion connectors are for signal monitoring and user feature expandability.

The 56F8346EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800E architecture. The tools and examples provided with the 56F8346EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The breakpoint features of the EOnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full speed until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory and peripherals through the EOnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the hybrid controller's peripherals. The EOnCE port's unobtrusive design means that all memory on the board and on the chip is available to the user.

## 1.1 56F8346EVM Architecture

The 56F8346EVM facilitates the evaluation of various features present in the 56F8346 part. The 56F8346EVM can be used to develop real-time software and hardware products based on the 56F8346. The 56F8346EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the user's application-specific device(s). The 56F8346EVM is flexible enough to allow a user to fully exploit the 56F8346's features to optimize the performance of his product, as shown in **Figure 1-1**.

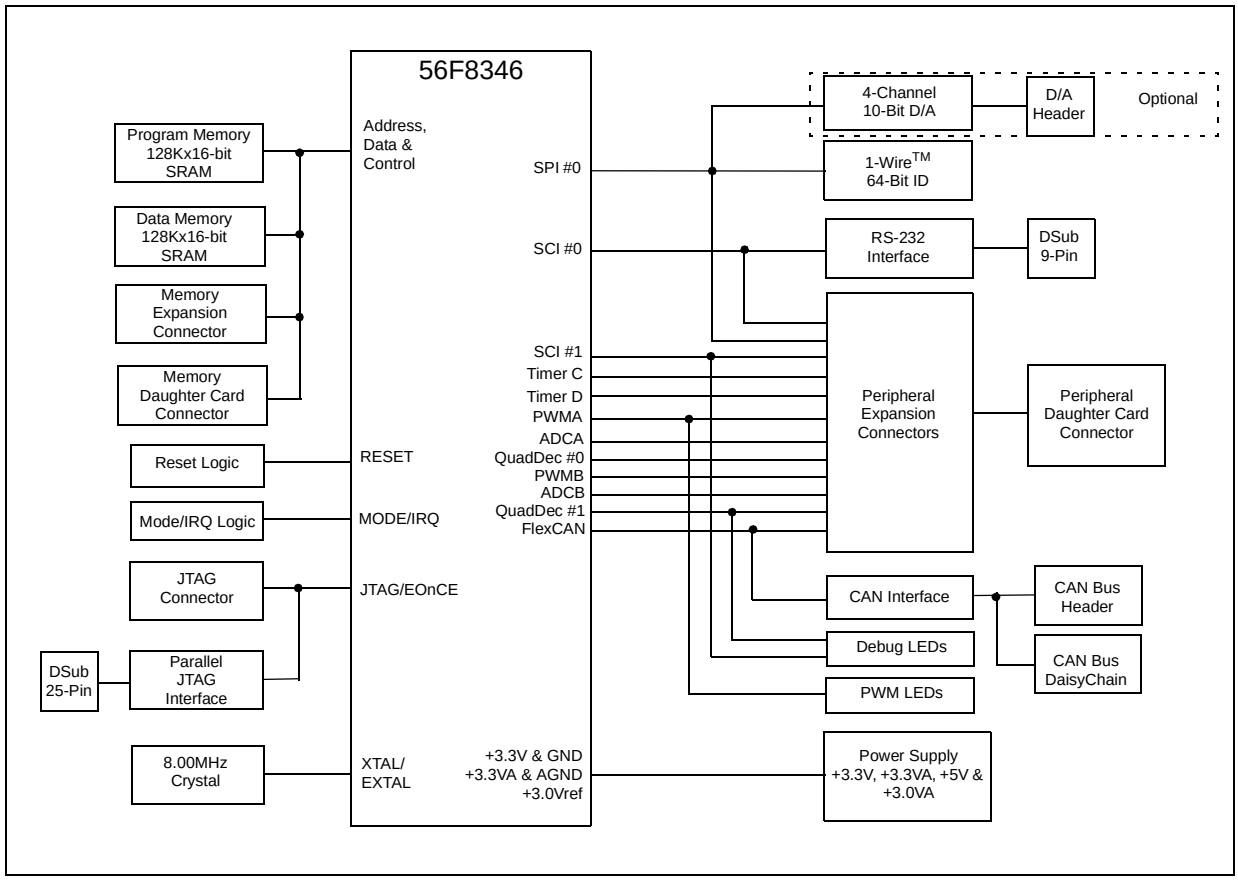


**Figure 1-1. Block Diagram of the 56F8346EVM**

## 1.2 56F8346EVM Configuration Jumpers

Sixteen jumper groups, (JG1-JG16), shown in **Figure 1-2**, are used to configure various features on the 56F8346EVM board. **Table 1-1** describes the default jumper group settings.

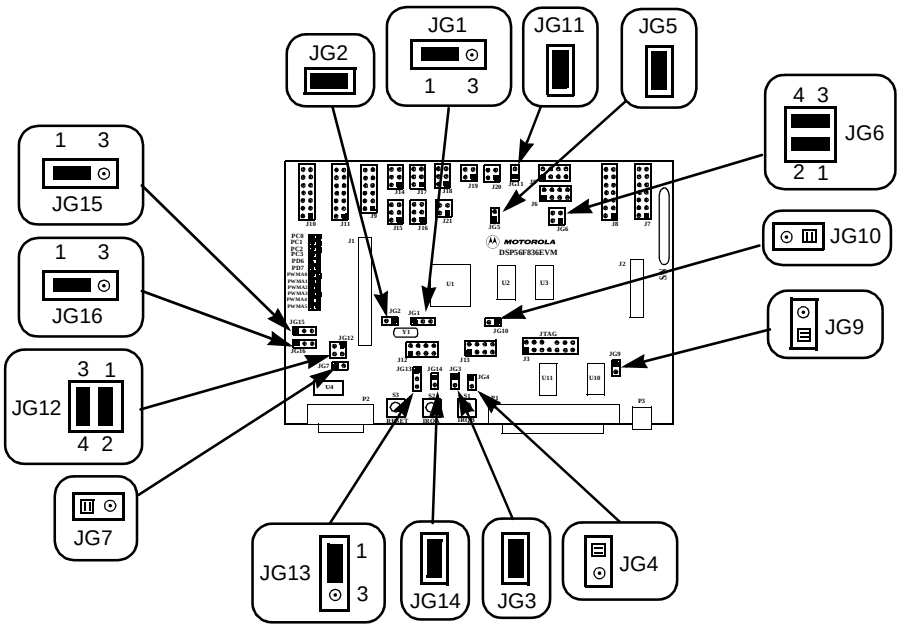


**Figure 1-2. 56F8346EVM Jumper Reference**

**Table 1-1. 56F8346EVM Default Jumper Options**

| Jumper Group | Comment | Jumpers Connections |
|---|---|---|
| JG1 | Use on-board EXTAL crystal input for the device's oscillator | 1–2 |
| JG2 | Use on-board XTAL crystal input for the device's oscillator | 1–2 |
| JG3 | Enable Internal Boot Mode | 1–2 |
| JG4 | Enable A0 - A19 for external memory accesses | NC |
| JG5 | Enable SRAM Memory Bank 0 (use CS0) | 1–2 |
| JG6 | Enable SRAM Memory Bank 1 (use CS1 & CS2) | 1–2 & 3–4 |
| JG7 | Enable RS-232 output | NC |
| JG8 | SPI #0 Daisy Chain (Optional--not populated on board by default) | NC |
| JG9 | Enable on-board Parallel JTAG Host/Target Interface | NC |
| JG10 | Connect Analog Ground to Digital Ground | NC |
| JG11 | CAN termination selected | 1–2 |
| JG12 | Pass RXD0 & TXD0 to RS-232 level converter | 1–2 & 3–4 |
| JG13 | Enable Crystal Mode | 1–2 |
| JG14 | Pass Temperature Diode to ANA7 | 1–2 |
| JG15 | User Jumper #0 | 1–2 |
| JG16 | User Jumper #1 | 1–2 |

## 1.3 56F8346EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12.0V DC/AC power supply to the 56F8346EVM board.

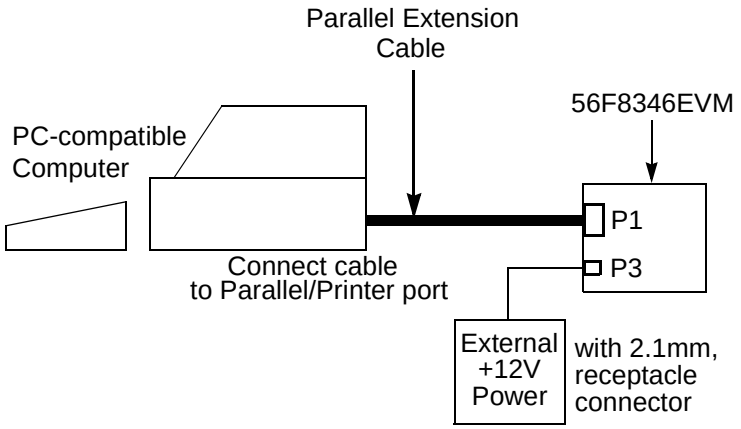


**Figure 1-3. Connecting the 56F8346EVM Cables**

Perform the following steps to connect the 56F8346EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F8346EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 1.2A power supply is not plugged into a +120V AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P3, shown in **Figure 1-3**, on the 56F8346EVM board.
5. Apply power to the external power supply. The green Power-ON LED, LED13, will illuminate when power is correctly applied.

# Chapter 2
# Technical Summary

The 56F8346EVM is designed as a versatile hybrid controller development card for developing real-time software and hardware products to support a new generation of applications in servo and motor control, digital and wireless messaging, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F8346, combined with the on-board 128K × 16-bit external program/data static RAM (SRAM), 128K × 16-bit external data/program SRAM, RS-232 interface, CAN interface, Daughter Card Expansion interface and parallel JTAG interface, makes the 56F8346EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F8346 processor.

The main features of the 56F8346EVM, with board and schematic reference designators include:

- 56F8346FV60, a 16-bit +3.3V/+2.5V Digital Signal Processor operating at 60MHz [U1]
- External fast static RAM (FSRAM) memory, configured as:
  - 128K×16-bit of memory [U2] with 0 wait state at 60MHz via CS0
  - 128K×16-bit of memory [U3] with 0 wait state at 60MHz via CS1/CS2
- 1-Wire Serial 64-Bit Unique ID [U6]
- Optional 4-Channel 10-bit Serial D/A, SPI for real-time user data display [U5]
- 8.00MHz crystal oscillator for hybrid controller frequency generation [Y1]
- Optional external oscillator frequency input connectors [JG1 and JG2]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J3]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1], including a disable jumper [JG9]
- RS-232 interface for easy connection to a host processor [U4 and P2], with a disable jumper [JG7]
- CAN interface for high speed, 1.0Mbps, FlexCAN communications [U16 and J5]

- CAN bypass and bus termination [J6 and JG11]
- Peripheral Daughter Card Expansion Connector, to allow the user to connect his own SCI, SPI or GPIO compatible peripheral to the hybrid controller[J1]
- Memory Daughter Card Expansion Connector, to allow the user to connect his own memory or memory device to the hybrid controller [J2]
- Connector to allow the user to connect his own SCI #0 / MPIO-compatible peripheral [J16]
- Connector to allow the user to connect his own SCI #1 / MPIO-compatible peripheral [J17]
- Connector to allow the user to connect his own SPI #0 / MPIO-compatible peripheral [J14]
- Connector to allow the user to connect his own SPI #1 / MPIO-compatible peripheral [J15]
- Connector to allow the user to connect his own PWMA-compatible peripheral [J10]
- Connector to allow the user to connect his own PWMB-compatible peripheral [J11]
- Connector to allow the user to connect his own CAN physical layer peripheral [J21]
- Connector to allow the user to connect his own Timer A / Encoder #0-compatible peripheral [J18]
- Connector to allow the user to connect his own Timer C-compatible peripheral [J19]
- Connector to allow the user to connect his own Timer D-compatible peripheral [J20]
- Connector to allow the user to attach his own A/D port A-compatible peripheral [J12]
- Connector to allow the user to attach his own A/D port B-compatible peripheral [J13]
- On-board power regulation from an external +12V DC-supplied power input [P3]
- Light Emitting Diode (LED) power indicator [LED13]
- Six on-board real-time user debugging LEDs [LED1-6]
- Six on-board Port A PWM monitoring LEDs [LED7-12]
- Internal/External (EXTBOOT) Boot MODE selector [JG3]
- Address Range (EMI_MODE) Boot MODE selector [JG4]

- Clock MODE (CLKMODE) Boot selector [JG13]
- Temperature Sense Diode to ANA7 selector [JG14]
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]
- General purpose jumper on GPIO PE4 [JG15]
- General purpose jumper on GPIO PE7 [JG16]

## 2.1 56F8346

The 56F8346EVM uses a Motorola DSP56F836FV60 part, designated as U1 on the board and in the schematics. This part will operate at a maximum external bus speed of 60MHz. A full description of the 56F8346, including functionality and user information, is provided in these documents:

- *56F8346 Technical Data Sheet*, (56F8346/D)**:** Electrical and timing specifications, pin descriptions, device specific peripheral information and package descriptions (this document)
- *56F8300 Peripheral User Manual*, (MC56F8300UM/AD): Detailed description of peripherals of the 56F8300 family of devices
- *DSP56800E Reference Manual*, (DSP56800ERM/D): Detailed description of the 56800E family architecture, 16-bit core processor, and the instruction set

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

**www.motorola.com/semiconductors**

## 2.2 Program and Data Memory

The 56F8346EVM contains two 128Kx16-bit Fast Static RAM banks. SRAM bank 0 is controlled by CS0 and SRAM bank 1 is controlled by CS1 and CS2. This provides a total of 256Kx16-bit of external memory.

### 2.2.1 SRAM Bank 0

SRAM bank 0, which is controlled by CS0, uses a 128K×16-bit Fast Static RAM (GSI GS72116, labeled U2) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-1**. CS0 can be configured to use this memory bank as 16-bit program memory, data memory, or both. Additionally, CS0 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with zero wait state access while the 56F8346 is running at 60MHz and can be disabled by removing the jumper at JG5.

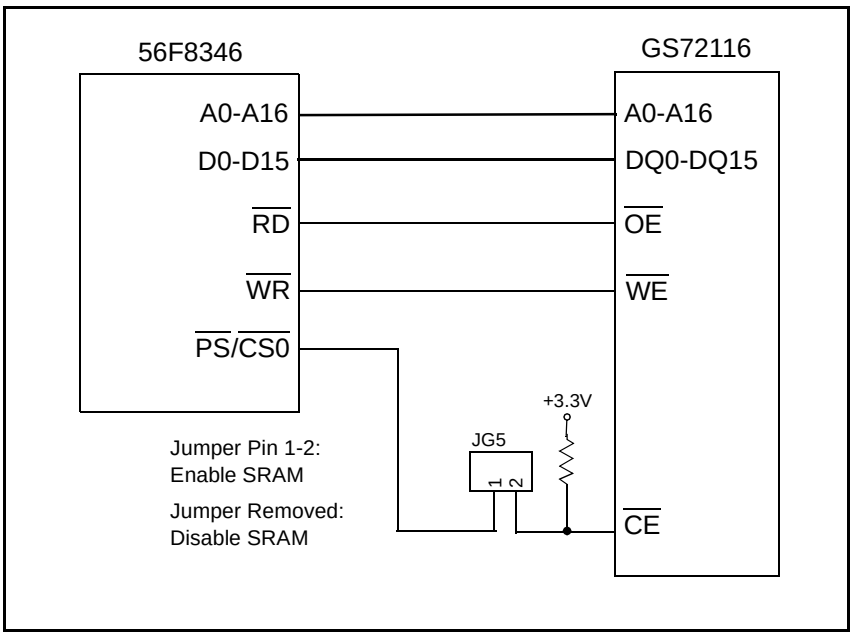


**Figure 2-1. Schematic Diagram of the External CS0 Memory Interface**

### 2.2.2 SRAM Bank 1

SRAM bank 1, which is controlled by CS1 and CS2, uses a 128K×16-bit Fast Static RAM (GSI GS72116, labeled U3) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-2**. Using CS1 and CS2, this memory bank can be configured as byte (8-bit) or word (16-bit) accessable program memory, data memory, or both. Additionally, CS1 and CS2 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with zero wait state access while the 56F8346 is running at 60MHz and can be disabled by removing the jumpers at JG6.

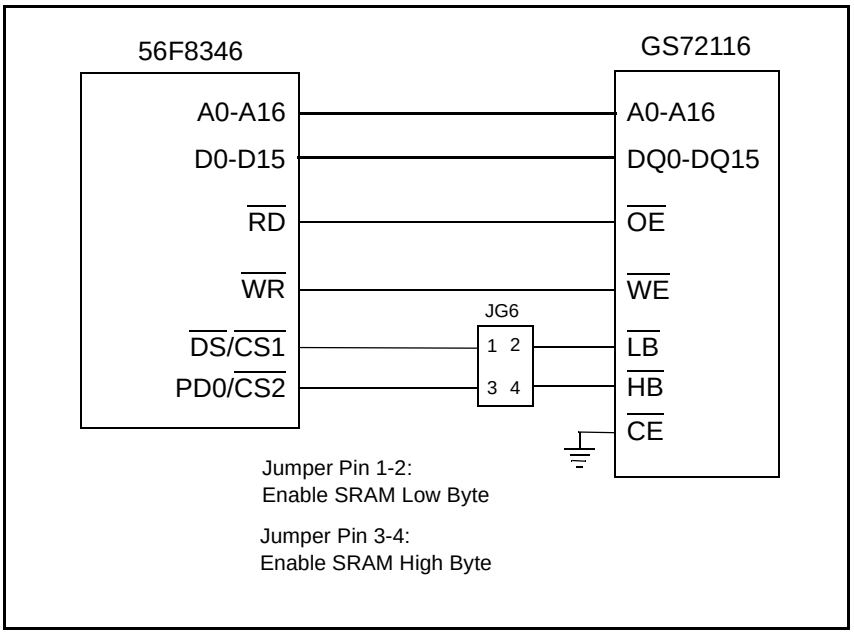


**Figure 2-2. Schematic Diagram of the External CS1/CS2 Memory Interface**

## 2.3 1-Wire 64-Bit ID

A unique ID for each 56F8346EVM board is provided by the use of a 64-bit 1-Wire ID device, Dallas Semiconductor DS2401P, designated as U6; see **Figure 2-3**. The device's 1-Wire interface connects to GPIO Port E 6 (PE6) through a zero ohm resistor. The 64-Bit ID in the 1-Wire part can be used to uniquely identify the 56F8346EVM board via software to external devices. Since the SPI #0 port and GPIO Port E are multiplexed on the 56F8346, the GPIO Port bit 7 must be selected in software and the data bit-banged on the 1-Wire interface. The 1-Wire ID port can be isolated from the hybrid controller, via the MISO0 signal, by removing R84.

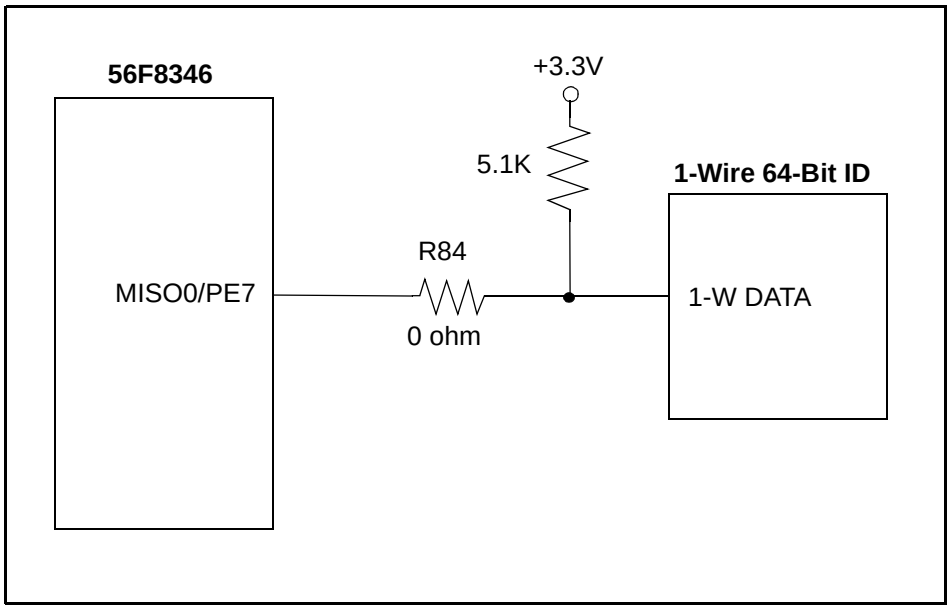


**Figure 2-3. 1-Wire 64-Bit ID Block Diagram**

## 2.4 RS-232 Serial Communications

The 56F8346EVM provides an RS-232 interface by the use of an RS-232 level converter, Maxim MAX3245EEAI, designated as U4. Refer to the RS-232 schematic diagram in **Figure 2-4**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232-compatible signal levels and connects to the host's serial port via connector P2. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The SCI0 port signals can be isolated from the RS-232 level converter by removing the jumpers in JG12, reference **Table 2-1**. The pinout of connector P2 is listed in **Table 2-3**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG7.

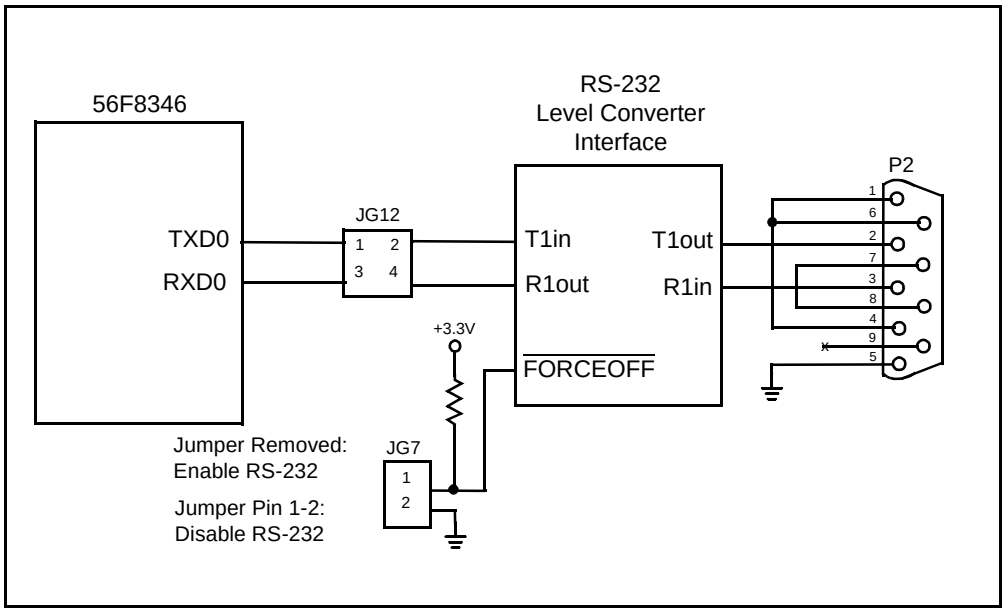


**Figure 2-4. Schematic Diagram of the RS-232 Interface**

**Table 2-1. SPI0 Jumper Options**

| JG12 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD0 | 2 | RS-232 TXD |
| 3 | RXD0 | 4 | RS-232 RXD |

**Table 2-2. RS-232 Serial Connector Description**

| P2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | Jumper to 6 & 4 | 6 | Jumper to 1 & 4 |
| 2 | TXD | 7 | Jumper to 8 |
| 3 | RXD | 8 | Jumper to 7 |
| 4 | Jumper to 1 & 6 | 9 | N/C |
| 5 | GND | | |

## 2.5 Clock Source

The 56F8346EVM uses an 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. To achieve its 120MHz maximum internal operating frequency, the 56F8346 uses its internal PLL to multiply the input frequency by 15. An external oscillator source can be connected to the hybrid controller by using the oscillator bypass connectors, JG1 and JG2; see **Figure 2-5**. If the input frequency is above 8MHz, then the EXTAL input should be jumpered to ground by adding a jumper between JG1 pins 2 and 3. The input frequency would then be injected on JG2's pin 2. If the input frequency is below 4MHz, then the input frequency can be injected on JG1's pin 2.

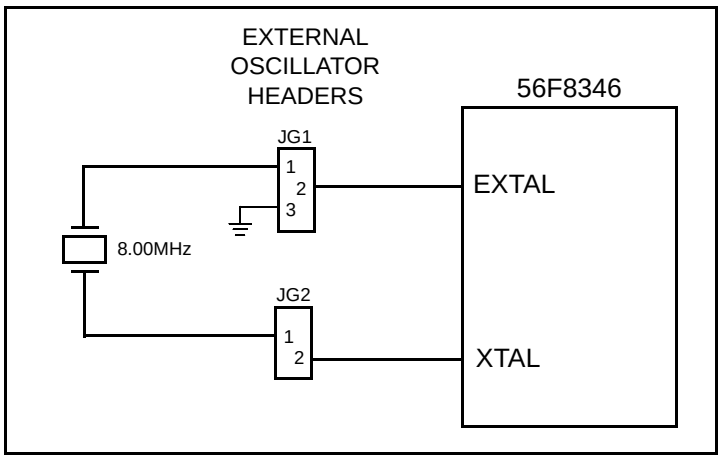


**Figure 2-5. Schematic Diagram of the Clock Interface**

## 2.6 Operating Mode

The 56F8346EVM provides three BOOT MODE selection jumpers, EXTBOOT, EMI_MODE and CLKMODE, to provide boot-up MODE options.

### 2.6.1 EXTBOOT

The 56F8346EVM provides an External/Internal Boot Mode jumper, JG3. This jumper is used to select the internal or external memory operation of the hybrid controller as it exits RESET. Refer to the **56F8300 Peripheral User Manual** and the **56F8346 Technical Data** sheet for a complete description of the chip's operating modes. **Table 2-3** shows the two External Boot operation modes available on the 56F8346.

**Table 2-3. EXTBOOT Operating Mode Selection**

| Operating Mode | JG3 | Comment |
|---|---|---|
| 0 | 1–2 | Bootstrap from internal memory (GND) |
| 3 | No Jumper | Bootstrap from external memory (+3.3V) |

### 2.6.2 EMI_MODE

The 56F8346EVM provides an EMI Boot Mode jumper, JG4. This jumper is used to select the external memory addressing range operating mode of the hybrid controller as it exits RESET. The user can select between a 64K address space or a 1M address space. Refer to the **56F8300 Peripheral User Manual** and the **56F8346 Technical Data** sheet for a complete description of the chip's operating modes. **Table 2-4** shows the two EMI operation modes available on the 56F8346.

**Table 2-4. EMI Operating Mode Selection**

| Operating Mode | JG4 | Comment |
|---|---|---|
| V1 | 1–2 | A0 - A15 (64K) available for external memory bus (GND) |
| V2 | No Jumper | A0 - A19 (1M) available for external memory bus (+3.3V) |

### 2.6.3 CLKMODE

The 56F8346EVM provides an Clock Boot Mode jumper, JG13. This jumper is used to select the type of clock source being provided to the hybrid controller as it exits RESET. The user can select between the use of a crystal or an oscillator as the clock source for the hybrid controller. Refer to the **56F8300 Peripheral User Manual** and the **56F8346 Technical Data** sheet for a complete description of the chip's operating modes. **Table 2-5** shows the two CLKMODE operation modes available on the 56F8346.

**Table 2-5. EMI Operating Mode Selection**

| Operating Mode | JG13 | Comment |
|---|---|---|
| Crystal | 1–2 | Enable the external clock drive logic so an external crystal can be used as the input clock source. (GND) |
| Oscillator | No Jumper | Disable the external clock drive logic. Use oscillator input on XTAL and Ground on EXTAL. (3.3V) |

## 2.7 Debug LEDs

Six on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-6**. **Table 2-6** describes the control of each LED.

**Table 2-6. LED Control**

| | Controlled by | |
|---|---|---|
| **User LED** | **Color** | **Signal** |
| LED1 | RED | Port C Bit-0 |
| LED2 | YELLOW | Port C Bit-1 |
| LED3 | GREEN | Port C Bit-2 |
| LED4 | RED | Port C Bit-3 |
| LED5 | YELLOW | Port D Bit-6 |
| LED6 | GREEN | Port D Bit-7 |

Setting PC0, PC1, PC2, PC3, PD6 or PD7 to a Logic One value will turn on the associated LED.

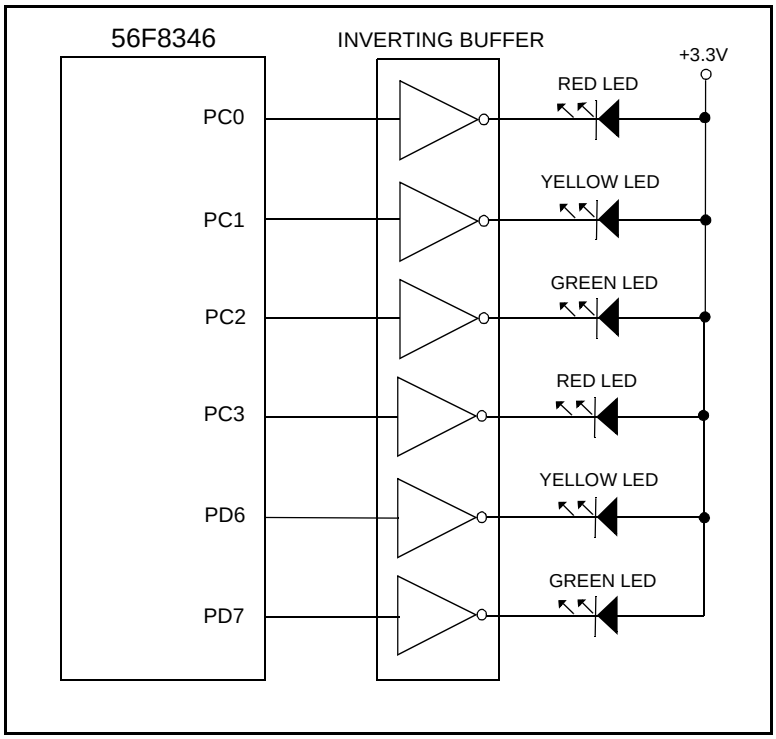


**Figure 2-6. Schematic Diagram of the Debug LED Interface**

## 2.8 Debug Support

The 56F8346EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

### 2.8.1 JTAG Connector

The JTAG connector on the 56F8346EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F8346's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-7** shows the pin-out for this connector.

**Table 2-7. JTAG Connector Description**

| J3 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TDI | 2 | GND |
| 3 | TDO | 4 | GND |
| 5 | TCK | 6 | GND |
| 7 | NC | 8 | KEY |
| 9 | $\overline{\text{RESET}}$ | 10 | TMS |
| 11 | +3.3V | 12 | NC |
| 13 | $\overline{\text{DE}}$ | 14 | $\overline{\text{TRST}}$ |

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG9. Reference **Table 2-8** for this jumper's selection options.

**Table 2-8. Parallel JTAG Interface Disable Jumper Selection**

| JG9 | Comment |
|---|---|
| No jumpers | Enable On-board Parallel JTAG Interface |
| 1–2 | Disable on-board Parallel JTAG Interface |

### 2.8.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the 56F8346 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-7**. Using this connector, the user can download programs and work with the 56F8346's registers. **Table 2-9** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG9 should be removed, as shown in **Table 2-8**.

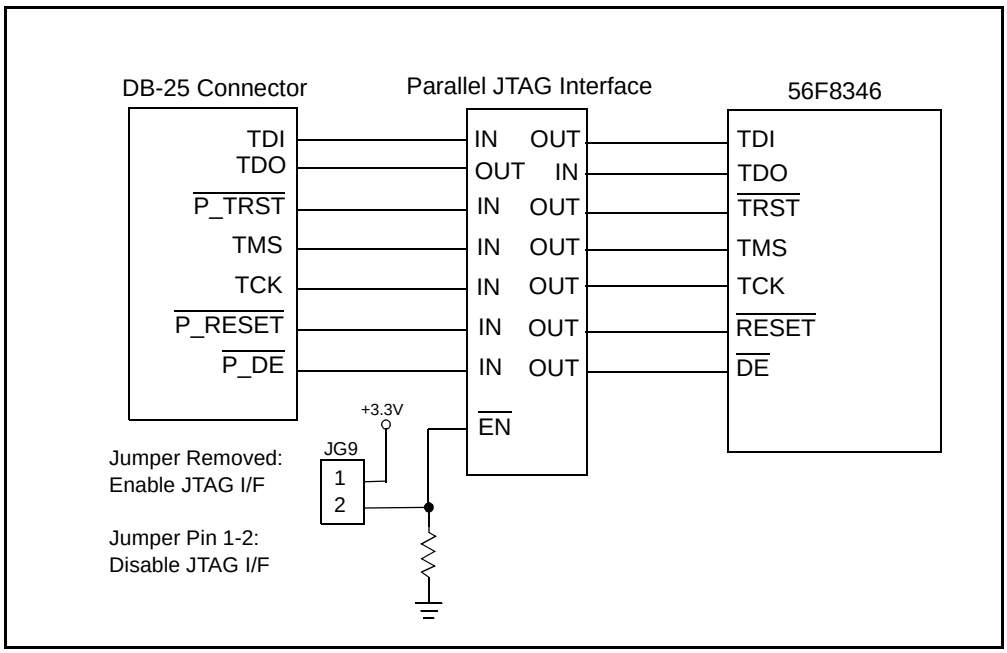


**Figure 2-7. Block Diagram of the Parallel JTAG Interface**

**Table 2-9. Parallel JTAG Interface Connector Description**

| P1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | NC | 14 | NC |
| 2 | PORT_RESET | 15 | PORT_IDENT |
| 3 | PORT_TMS | 16 | NC |
| 4 | PORT_TCK | 17 | NC |
| 5 | PORT_TDI | 18 | GND |
| 6 | $\overline{\text{PORT\_TRST}}$ | 19 | GND |
| 7 | $\overline{\text{PORT\_DE}}$ | 20 | GND |
| 8 | PORT_IDENT | 21 | GND |
| 9 | PORT_VCC | 22 | GND |
| 10 | NC | 23 | GND |
| 11 | PORT_TDO | 24 | GND |
| 12 | NC | 25 | GND |
| 13 | PORT_CONNECT | | |

## 2.9 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in **Figure 2-8**. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. S3 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

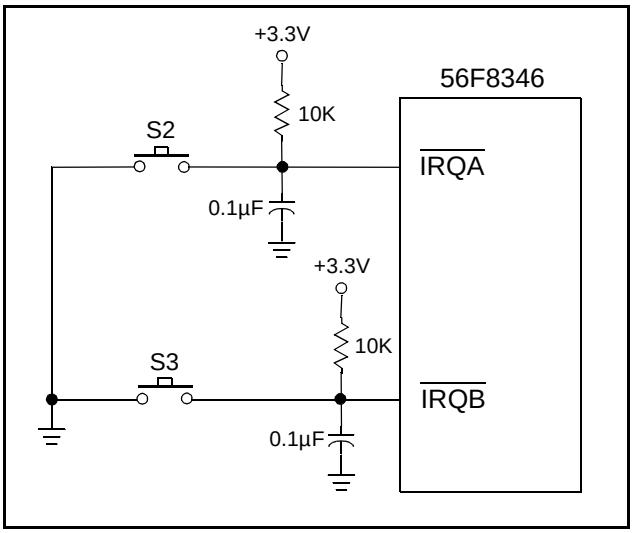


**Figure 2-8. Schematic Diagram of the User Interrupt Interface**

## 2.10 Reset

Logic is provided on the 56F8346 to generate an internal Power-On RESET. Additional reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button, S1; refer to **Figure 2-9**.

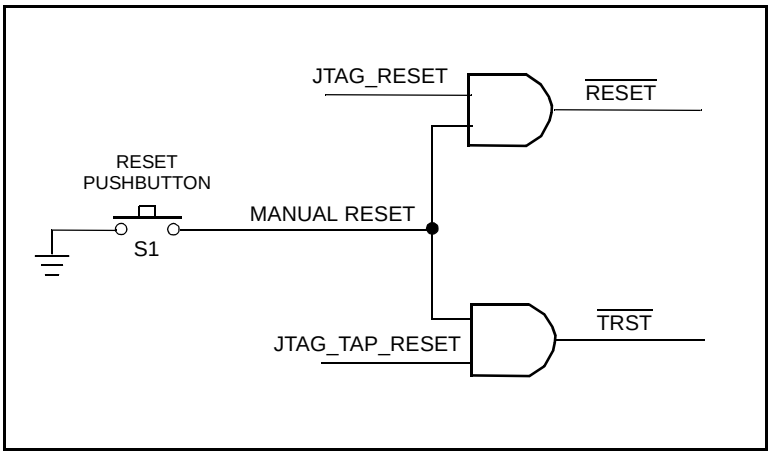


**Figure 2-9. Schematic Diagram of the RESET Interface**

## 2.11 Power Supply

The main power input to the 56F8346EVM, +12V DC at 1.2A, is through a 2.1mm coax power jack. This input power is rectified to provide a DC supply input. This allows a user the option to use a +12V AC power supply. A 1.2Amp power supply is provided with the 56F8346EVM; however, less than 500mA is required by the EVM. The remaining current is available for custom control applications when connected to the Daughter Card connectors. The 56F8346EVM provides +5.0V DC regulation for the CAN interface and additional regulators. The 56F8346EVM provides +3.3V DC voltage regulation for the hybrid controller, memory, D/A, ADC, parallel JTAG interface and supporting logic; refer to **Figure 2-11**. Additional voltage regulation logic provides a low noise +3.0V DC voltage reference to the hybrid controller's A/D $V_{REFH}$. Optionally, the device's A/D $V_{REFH}$ voltage can be provided by the +3.3V A supply on the board by removing U15 and adding a 10 ohm resistor at R83. A jumper, JG10, and resistor, R2, is provided to allow the analog and digital grounds to be isolated on the 56F8346EVM board. This allows the analog ground reference point to be provided on a custom board attached to the 56F8346EVM's Daughter Card connectors. By removing R2, the AGND reference is disconnected from the 56F8346EVM's digital ground. By placing a jumper in JG10, the AGND is reconnected to the 56F8346EVM's digital ground. Power applied to the 56F8346EVM is indicated with a Power-ON LED, referenced as LED13. Optionally, the user can provide the +2.5 DC voltage needed by the hybrid controller's core on connector J22 and disable the on-chip CORE voltage regulator by moving the resistor at R97 to R96. Additonally, four zero ohm resistors or shorting wires must be added at R92, R93, R94 and R95 to allow the external +2.5V DC to pass to the 56F8346.

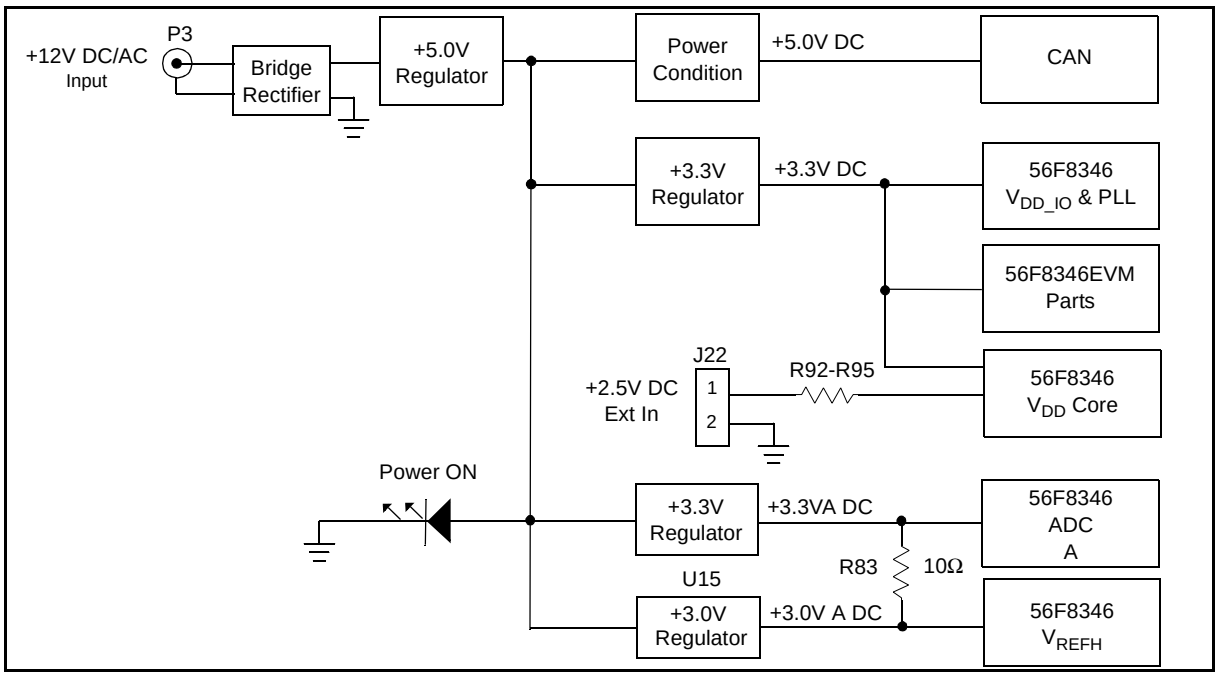


**Figure 2-10. Schematic Diagram of the Power Supply**

## 2.12 Daughter Card Connectors

The EVM board contains two daughter card expansion connectors. One connector, J1, contains the device's peripheral port signals. The second connector, J2, contains the hybrid controller's external memory bus signals.

### 2.12.1 Peripheral Daughter Card Expansion Connector

The device's peripheral port signals are connected to the Peripheral Daughter Card Expansion connector, J1. The Peripheral Daughter Card connector is used to connect a hybrid controller's daughter card or a user-specific daughter card to the device's peripheral port signals. The Peripheral Port Daughter Card connector is a 100-pin high-density connector with signals for the IRQs, RESET, SPI, SCI, PWM, ADC and Quad Timer ports. **Table 2-10** shows the Peripheral Daughter Card connector's signal-to-pin assignments.

**Table 2-10. Peripheral Daughter Card Connector Description**

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | +12V | 2 | +12V |
| 3 | GND | 4 | GND |
| 5 | +5.0V | 6 | +5.0V |
| 7 | GND | 8 | GND |
| 9 | +3.3V | 10 | +3.3V |
| 11 | GND | 12 | GND |
| 13 | PHASEA0/TA0 | | PHASEB0/TA1 |
| 15 | INDEX0/TA2 | 16 | HOME0/TA3 |
| 17 | GND | 18 | GND |
| 19 | PHASEA1/PC0/TB0/SCLK1 | 20 | PHASEB1/PC1/TB1/MOSI1 |
| 21 | INDEX1/PC2/TB2/MISO1 | 22 | HOME1/PC3/TB3/$\overline{SS1}$ |
| 23 | TXD0/PE0 | 24 | TXD1/PD6 |
| 25 | TXD0/PE0 | 26 | TXD1/PD6 |
| 27 | RXD0/PE1 | 28 | RXD1/PD7 |
| 29 | $\overline{IRQA}$ | 30 | $\overline{IRQB}$ |

**Table 2-10. Peripheral Daughter Card Connector Description (Continued)**

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 31 | RXD0/PE1 | 32 | RXD1/PD7 |
| 33 | PWMB0 | 34 | PWMB1 |
| 35 | PWMB2 | 36 | PWMB3 |
| 37 | PWMB4 | 38 | PWMB5 |
| 39 | GND | 40 | GND |
| 41 | ISB0 | 42 | ISB1 |
| 43 | ISB2 | 44 | GND |
| 45 | FAULTB1 | 46 | FAULTB0 |
| 47 | FAULTB3 | 48 | FAULTB2 |
| 49 | GND | 50 | GND |
| 51 | PWMA0 | 52 | PWMA1 |
| 53 | PWMA2 | 54 | PWMA3 |
| 55 | PWMA4 | 56 | PWMA5 |
| 57 | GND | 58 | GND |
| 59 | FAULTA0 | 60 | FAULTA1 |
| 61 | FAULTA2 | 62 | MISO0/PE6 |
| 63 | ISA0 | 64 | ISA1 |
| 65 | ISA2 | 66 | $\overline{\text{RSTO}}$ |
| 67 | MOSI0/PE5 | 68 | $\overline{\text{SS0}}$/PE7 |
| 69 | TD0 | 70 | TD1 |
| 71 | SCLK0/PE7 | 72 | TC0 |
| 73 | CAN_TX | 74 | CAN_RX |
| 75 | MOSI0/PE5 | 76 | MISO0/PE6 |
| 77 | SCLK0/PE4 | 78 | $\overline{\text{SS0}}$/PE7 |
| 79 | GND | 80 | GND |
| 81 | +VREFH | 82 | +VREFH |
| 83 | GNDA | 84 | GNDA |
| 85 | AN0 | 86 | AN1 |

**Table 2-10. Peripheral Daughter Card Connector Description (Continued)**

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 87 | AN2 | 88 | AN3 |
| 89 | AN4 | 90 | AN5 |
| 91 | AN6 | 92 | AN7 |
| 93 | AN8 | 94 | AN9 |
| 95 | AN10 | 96 | AN11 |
| 97 | AN12 | 98 | AN13 |
| 99 | AN14 | 100 | AN15 |

## 2.12.2 Memory Daughter Card Expansion Connector

The hybrid controller's external memory bus signals are connected to the Memory Daughter Card Expansion connector, J2. **Table 2-11** shows the port signal-to-pin assignments.

**Table 2-11. Memory Daughter Card Connector Description**

| J2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | A4 | 2 | A5 |
| 3 | A3 | 4 | A6/PE2 |
| 5 | A2 | 6 | A7/PE3 |
| 7 | A1 | 8 | $\overline{RD}$ |
| 9 | GND | 10 | GND |
| 11 | A0 | 12 | $\overline{DS}/\overline{CS1}$ |
| 13 | $\overline{PS}/\overline{CS0}$ | 14 | PD0/$\overline{CS2}$ |
| 15 | D0 | 16 | D15 |
| 17 | D1 | 18 | D14/PF7 |
| 19 | GND | 20 | GND |
| 21 | GND | 22 | GND |
| 23 | D2 | 24 | D13/PF6 |

**Table 2-11. Memory Daughter Card Connector Description (Continued)**

| J2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 25 | D3 | 26 | D12/PF5 |
| 27 | D4 | 28 | D11/PF4 |
| 29 | D5 | 30 | D10/PF3 |
| 31 | GND | 32 | GND |
| 33 | GND | 34 | GND |
| 35 | D6 | 36 | D9/PF2 |
| 37 | D7/PF0 | 38 | D8/PF1 |
| 39 | $\overline{WR}$ | 40 | PD1/$\overline{CS3}$ |
| 41 | A15/PA7 | 42 | A8/PA0 |
| 43 | GND | 44 | GND |
| 45 | A14/PA6 | 46 | A9/PA1 |
| 47 | A13/PA5 | 48 | A10/PA2 |
| 49 | A12/PA4 | 50 | A11/PA3 |
| 51 | PB0/A16 | 52 | GND |
| 53 | GND | 54 | GND |
| 55 | +3.3V | 56 | +3.3V |
| 57 | GND | 58 | GND |
| 59 | +5.0V | 60 | +5.0V |

## 2.13 Serial 10-bit 4-channel D/A Converter (Optional)

The 56F8346EVM board contains the provions for a user to provide a serial 10-bit, 4-channel D/A converter connected to the 56F8346's SPI #0 port. The output pins are uncommitted and are connected to a 4X2 header, J4, to allow easy user connections. Refer to **Figure 2-11** for the D/A connections and **Table 2-12** for the header's pin out. The D/A's output full-scale range value can be set to a value from +0.0V to +2.4V by a trimpot, R37. If this trimpot is preset to +2.05V, it would provide approximately +2mV per step. If another device must be used with SPI #0's MISO signal and with the D/A converter on the board, the daisy-chain jumper, JG8, can be used to extend or isolate the serial chain.

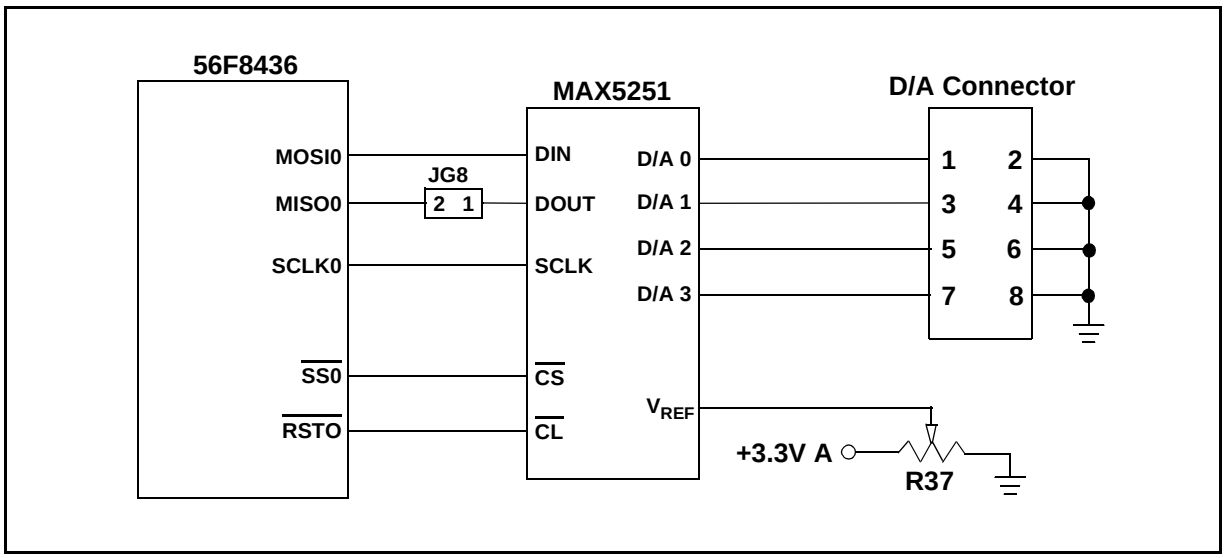


**Figure 2-11. Serial 10-bit, 4-Channel D/A Converter**

**Table 2-12. D/A Header Description**

| J4 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | D/A Channel 0 | 2 | AGND |
| 3 | D/A Channel 1 | 4 | AGND |
| 5 | D/A Channel 2 | 6 | AGND |
| 7 | D/A Channel 3 | 8 | AGND |

## 2.14 Motor Control PWM Signals and LEDs

The 56F8346 has two independent groups of dedicated PWM units. Each unit contains six PWM and three Phase Current sense inputs. One PWM unit has four Fault input lines, while the other has three Fault input lines. PWM group A's PWM lines are connected to a set of six PWM LEDs via inverting buffers. The buffers are used to isolate and drive the device's PWM group A's outputs to the PWM LEDs. The PWM LEDs indicate the status of PWM group A signals; refer to **Figure 2-12**. PWM Group A and B signals are routed out to headers, J10 and J11 respectively, and to the peripheral daughter card connector for easy use by the end user.

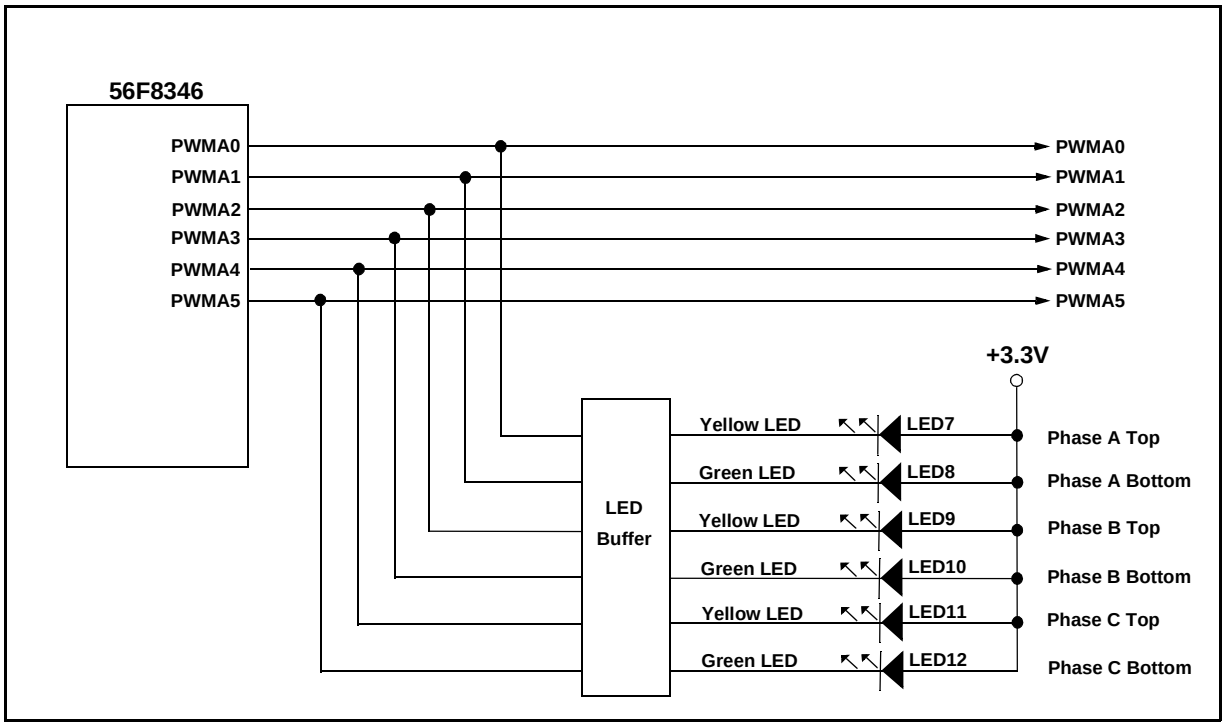


**Figure 2-12. PWM Group A Interface and LEDs**

## 2.15 CAN Interface

The 56F8346EVM board contains a CAN physical-layer interface chip that is attached to the FlexCAN port's CAN_RX and CAN_TX pins on the 56F8346EVM. The EVM board uses a Philips high-speed, 1.0Mbps, physical layer interface chip,PCA82C250. Due to the +5.0V operating voltage of the CAN interface chip, a pull-up to +5.0V is required to level shift the Transmit Data output line from the 56F8346. The CANH and CANL signals pass through inductors before attaching to the CAN bus connectors. A primary, J5, and daisy-chain, J6, CAN connector are provided to allow easy daisy-chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG11. Refer to **Table 2-13** for the CAN connector signals and **Figure 2-13** for a connection diagram.

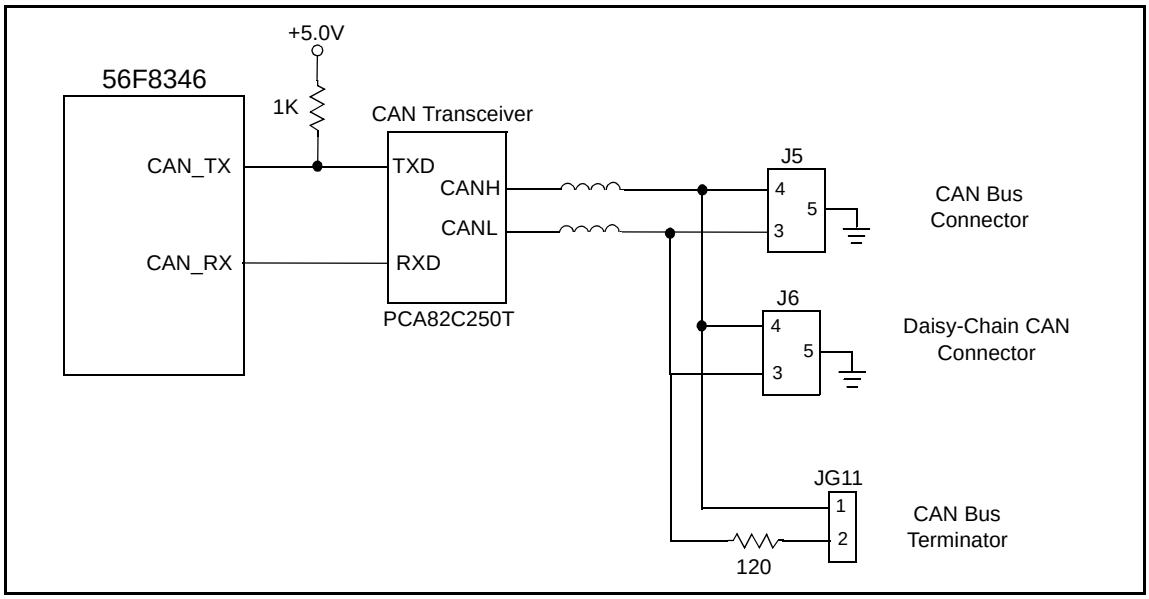


**Figure 2-13. CAN Interface**

**Table 2-13. CAN Header Description**

| J5 and J6 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | NC | 2 | NC |
| 3 | CANL | 4 | CANH |
| 5 | GND | 6 | NC |
| 7 | NC | 8 | NC |
| 9 | NC | 10 | NC |

## 2.16 Software Feature Jumpers

The 56F8346EVM board contains two software feature jumpers that allow the user to select “User-Defined” software features. Two GPIO port pins, PE4 and PE7, are pulled high or low with 10K ohm resistors on JG16 and JG17. Attaching a jumper between pins 1 and 2 will place a high or 1 on the port pin. Attaching a jumper between pins 2 and 3 will place a low or 0 on the port pin; see **Figure 2-14**.

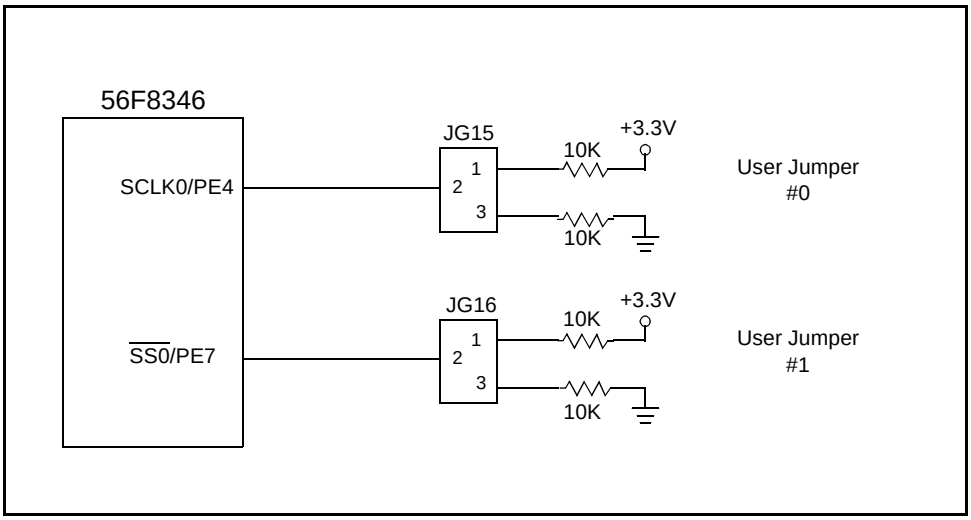


**Figure 2-14. Software Feature Jumpers**

## 2.17 Peripheral Expansion Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F8346. The following signal groups have Expansion Connectors:

- External Memory Address Bus/General Purpose Port A (bits 0-7)/General Purpose Port E (bits2&3)/General Purpose Port B (bit 0)
- External Memory Data Bus/General Purpose Port F (bits 0-7)
- External Memory Control/General Purpose Port D (bits 0 and 1)
- Encoder #0/Timer Channel A
- Encoder #1/Serial Peripheral Interface Port #1/Timer Channel B/General Purpose Port C (bits 0-3)
- Timer Channel C
- Timer Channel D
- A/D Input Port A
- A/D Input Port B
- Serial Communications Port 0/General Purpose Port E (bits 0 and 1)
- Serial Communications Port 1/General Purpose Port D (bits 6 and 7)
- Serial Peripheral Interface Port #0/General Purpose Port E (bits 4-7)
- PWM Port A
- PWM Port B

### 2.17.1 Address Bus Expansion Connector

The Address bus expansion connector contains the 56F8346's 17 external memory address signal lines. Address lines A6 & A7 can also be used as GPIO Port E lines (bits 2 and 3). Address lines A8 - A15, can also be used as GPIO Port A lines (bits 0-7). Address line A16 is an MPIO signal, which can be configured as A16 or GPIO Port B bit 0. Refer to **Table 2-14** for the Address bus connector information.

**Table 2-14. External Memory Address Bus Connector Description**

| J7 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | A0 | 2 | A1 |

**Table 2-14. External Memory Address Bus Connector Description**

| J7 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 3 | A2 | 4 | A3 |
| 5 | A4 | 6 | A5 |
| 7 | A6 / PE2 | 8 | A7 / PE3 |
| 9 | A8 / PA0 | 10 | A9 / PA1 |
| 11 | A10 / PA2 | 12 | A11 / PA3 |
| 13 | A12 / PA4 | 14 | A13 / PA5 |
| 15 | A14 / PA6 | 16 | A15 / PA7 |
| 17 | PB0 / A16 | 18 | NC |
| 19 | GND | 20 | +3.3V |

## 2.17.2 Data Bus Expansion Connector

The Data bus expansion connector contains the 56F8346's 16 external memory data signal lines. Refer to **Table 2-15** for the Data bus connector information. Data lines D7 - D14, can also be used as GPIO Port F lines (bits 0-7).

**Table 2-15. External Memory Address Bus Connector Description**

| J8 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | D0 | 2 | D1 |
| 3 | D2 | 4 | D3 |
| 5 | D4 | 6 | D5 |
| 7 | D6 | 8 | D7 / PF0 |
| 9 | D8 / PF1 | 10 | D9 / PF2 |
| 11 | D10 / PF3 | 12 | D11 / PF4 |
| 13 | D12 / PF5 | 14 | D13 / PF6 |
| 15 | D14 / PF7 | 16 | D15 |
| 17 | GND | 18 | +3.3V |

### 2.17.3 External Memory Control Signal Expansion Connector

The External Memory Control Signal connector contains 56F836's external memory control signal lines. CS2 and CS3 are MPIO signals, which can be configured as GPIO Port D lines (bits 0 & 1). Refer to **Table 2-16** for the names of these signals.

**Table 2-16. External Memory Control Signal Connector Description**

| J9 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | $\overline{RD}$ | 2 | $\overline{IRQA}$ |
| 3 | $\overline{WR}$ | 4 | $\overline{IRQB}$ |
| 5 | $\overline{PS}/\overline{CS0}$ | 6 | $\overline{DS}/\overline{CS1}$ |
| 7 | PD0/$\overline{CS2}$ | 8 | PD1/$\overline{CS3}$ |
| 9 | CLKO | 10 | $\overline{RESET}$ |
| 11 | GND | 12 | $\overline{RSTO}$ |

### 2.17.4 Encoder #0 / Quad Timer Channel A Expansion Connector

The Encoder #0 / Quad Timer Channel A port is an MPIO port attached to the Timer A expansion connector. This port can be configured as a Quadrature Decoder interface port or as a Quad Timer port. Refer to **Table 2-17** for the signals attached to the connector.

**Table 2-17. Timer A Signal Connector Description**

| J18 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PHASEA0/TA0 | 2 | PHASEB0/TA1 |
| 3 | INDEX0/TA2 | 4 | HOME0/TA3 |
| 5 | GND | 6 | +3.3V |

### 2.17.5 Encoder #1 / SPI #1 Expansion Connector

The Encoder #1 / SPI #1 port is an MPIO port attached to the SPI #1 expansion connector. This port can be configured as a Quadrature Decoder interface port, a Serial Peripherial Interface, Quad Timer port or General Purpose I/O port. Refer to **Table 2-18** for the signals attached to the connector.

**Table 2-18. SPI #1 Signal Connector Description**

| J15 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PHASEB1/MOSI1/TB1/PC1 | 2 | INDEX1/MISO1/TB2/PC2 |
| 3 | PHASEA1/SCLK1/TB0/PC0 | 4 | HOME1/$\overline{SS1}$/TB3/PC3 |
| 5 | GND | 6 | +3.3V |

## 2.17.6 Timer Channel C Expansion Connector

The Timer Channel C port is a Quad Timer port attached to the Timer C expansion connector. Refer to **Table 2-19** for the signals attached to the connector.

**Table 2-19. Timer Channel C Connector Description**

| J19 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TC0 | 2 | NC |
| 3 | GND | 4 | +3.3V |

## 2.17.7 Timer Channel D Expansion Connector

The Timer Channel D port is a Quad Timer attached to the Timer D expansion connector. Refer to **Table 2-20** for the signals attached to the connector.

**Table 2-20. Timer Channel D Connector Description**

| J20 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TD0 | 2 | TD1 |
| 3 | GND | 4 | +3.3V |

## 2.17.8 A/D Port A Expansion Connector

The 8-channel Analog to Digital conversion port A is attached to this connector. Refer to **Table 2-21** for connection information. There is an RC network on each of the Analog Port A input signals; reference**Figure 2-15**.

**Table 2-21. A/D Port A Connector Description**

| J12 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | AN0 | 2 | AN1 |
| 3 | AN2 | 4 | AN3 |
| 5 | AN4 | 6 | AN5 |
| 7 | AN6 | 8 | AN7 |
| 9 | GNDA | 10 | +VREFH |

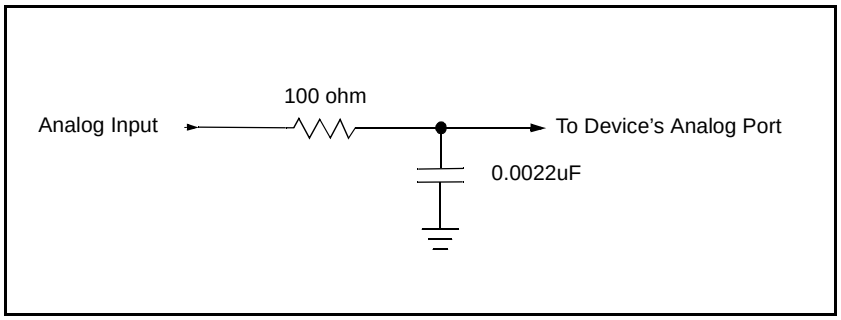


**Figure 2-15. Typical Analog Input RC Filter**

### 2.17.9 A/D Port B Expansion Connector

The 8-channel Analog-to-Digital conversion port B is attached to this connector. Refer to **Table 2-22** for connection information. There is an RC network on each of the Analog Port A input signals; see **Figure 2-15**.

**Table 2-22. A/D Port B Connector Description**

| J13 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | AN8 | 2 | AN9 |
| 3 | AN10 | 4 | AN11 |
| 5 | AN12 | 6 | AN13 |
| 7 | AN14 | 8 | AN15 |
| 9 | GNDA | 10 | +VREFH |

### 2.17.10 Serial Communications Port #0 Expansion Connector

The Serial Communications Port #0 is an MPIO port attached to the SCI #0 expansion connector. This port can be configured as a Serial Communications Interface or as a General Purpose I/O port. Refer to **Table 2-23** for connection information.

**Table 2-23. SCI #0 Connector Description**

| J16 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD0/PE0 | 2 | RXD0/PE1 |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +5.0V |

### 2.17.11 Serial Communications Port #1 Expansion Connector

The Serial Communications Port #1 is an MPIO port attached to the SCI #1 expansion connector. This port can be configured as a Serial Communications Interface or as a General Purpose I/O port. Refer to **Table 2-24** for connection information.

**Table 2-24. SCI #1 Connector Description**

| J17 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD1/PD6 | 2 | RXD1/PD7 |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +5.0V |

## 2.17.12 Serial Peripheral Interface #0 Expansion Connector

The Serial Peripheral Interface #0 is an MPIO port attached to this connector. This port can be configured as a Serial Peripheral Interface or as a General Purpose I/O port. Refer to **Table 2-25** for the connection information.

**Table 2-25. SPI #0 Connector Description**

| J14 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | MOSI0/PE5 | 2 | MISO0/PE6 |
| 3 | SCLK0/PE4 | 4 | $\overline{SS0}$/PE7 |
| 5 | GND | 6 | +3.3V |

## 2.17.13 FlexCAN Expansion Connector

The FlexCAN port is attached to this connector. Refer to **Table 2-26** for connection information.

**Table 2-26. CAN Connector Description**

| J21 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | CAN_TX | 2 | GND |
| 3 | CAN_RX | 4 | GND |

### 2.17.14 PWM Port A Expansion Connector

The PWM port A is attached to this connector. Refer to **Table 2-27** for connection information.

**Table 2-27. PWM Port A Connector Description**

| J10 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PWMA0 | 2 | PWMA1 |
| 3 | PWMA2 | 4 | PWMA3 |
| 5 | PWMA4 | 6 | PWMA5 |
| 7 | FAULTA0 | 8 | FAULTA1 |
| 9 | FAULTA2 | 10 | NC |
| 11 | ISA0 | 12 | ISA1 |
| 13 | ISA2 | 14 | GND |

### 2.17.15 PWM Port B Expansion Connector

The PWM port B is attached to this connector. Refer to **Table 2-28** for connection information.

**Table 2-28. PWM Port B Connector Description**

| J11 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PWMB0 | 2 | PWMB1 |
| 3 | PWMB2 | 4 | PWMB3 |
| 5 | PWMB4 | 6 | PWMB5 |
| 7 | FAULTB0 | 8 | FAULTB1 |
| 9 | FAULTB2 | 10 | FAULTB3 |
| 11 | ISB0 | 12 | ISB1 |
| 13 | ISB2 | 14 | GND |

## 2.18 Test Points

The 56F8346EVM board has a total of seven test points:

- Analog Ground (AGND)
- Three Digital Grounds (GND)
- +3.3
- +3.3VA
- +5.0V

# Appendix A
# 56F8346EVM Schematics

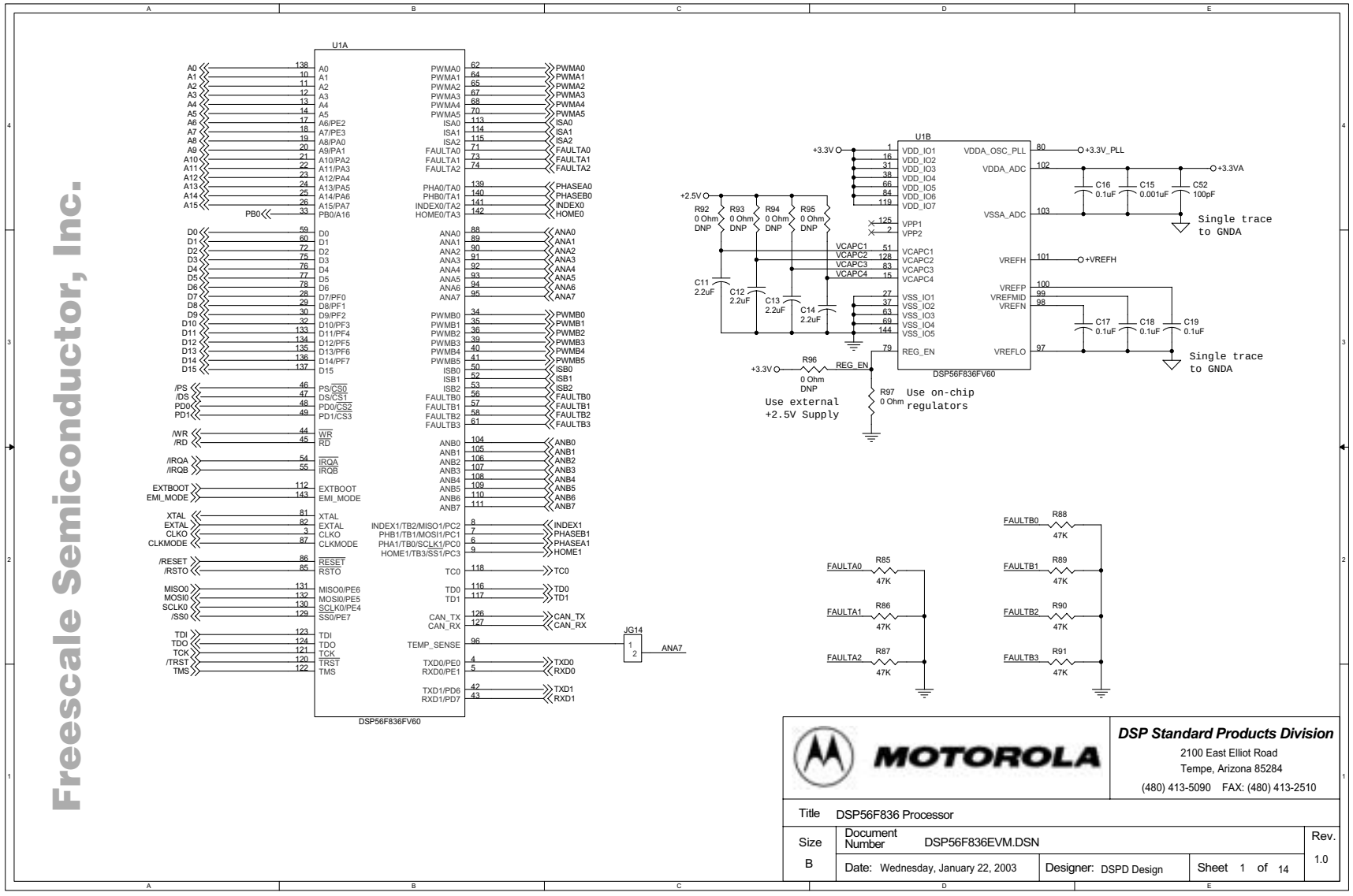


**Figure A-1. 56F8346 Processor**

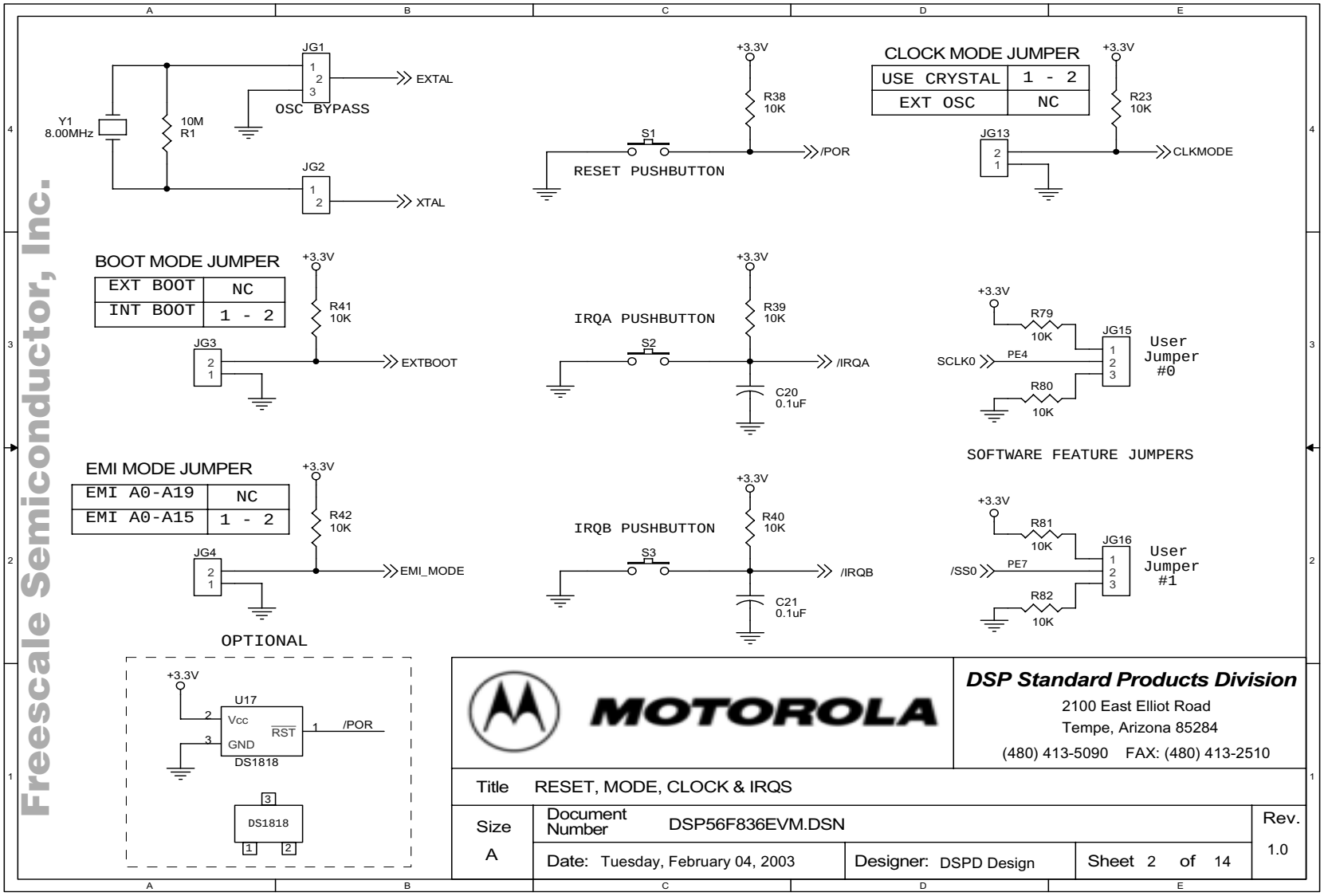


**Figure A-2. RESET, CLOCK, BOOT MODES & IRQs**

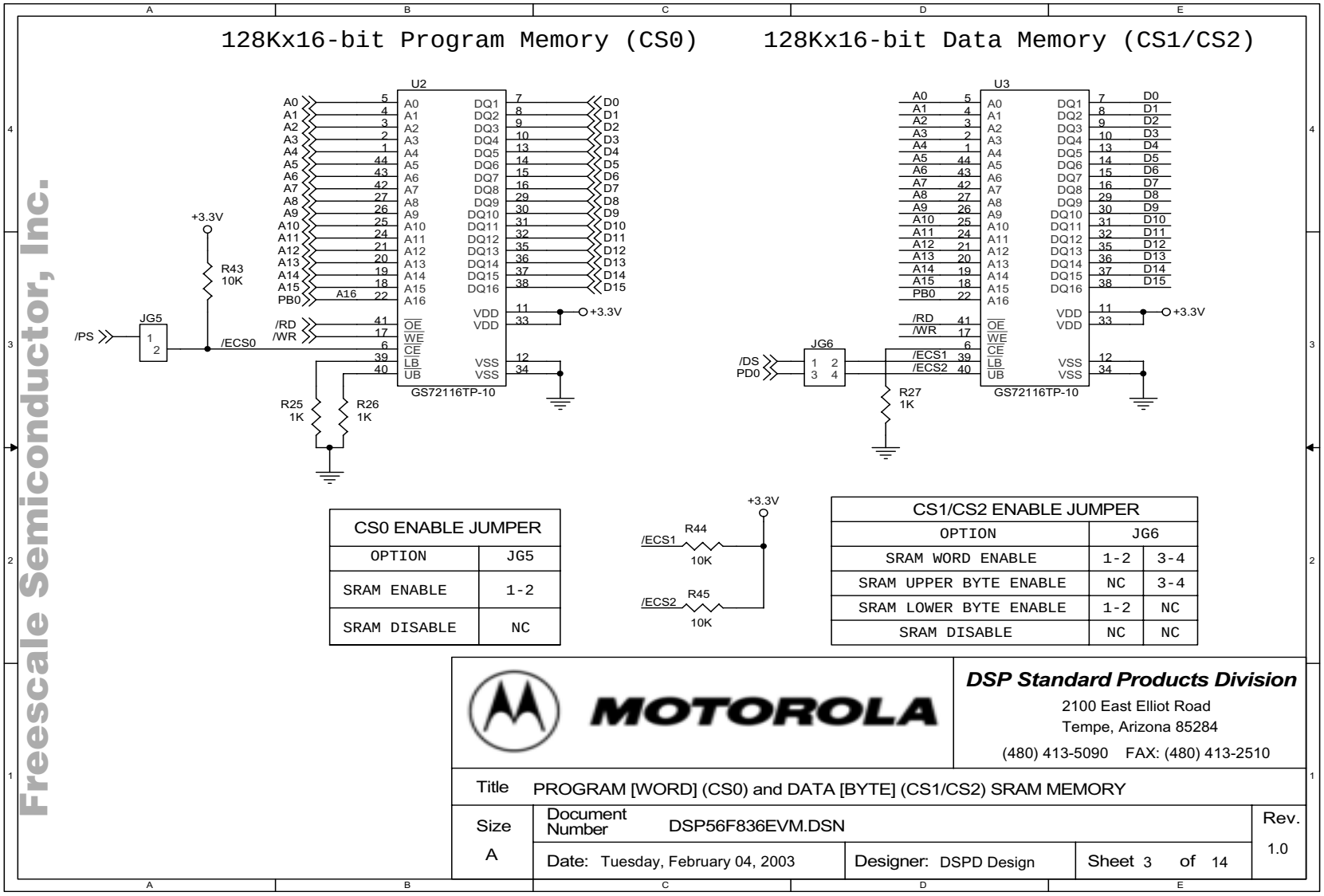


**Figure A-3. Program [Word] (CS0) & Data [Byte] (CS1/CS2) SRAM Memory**

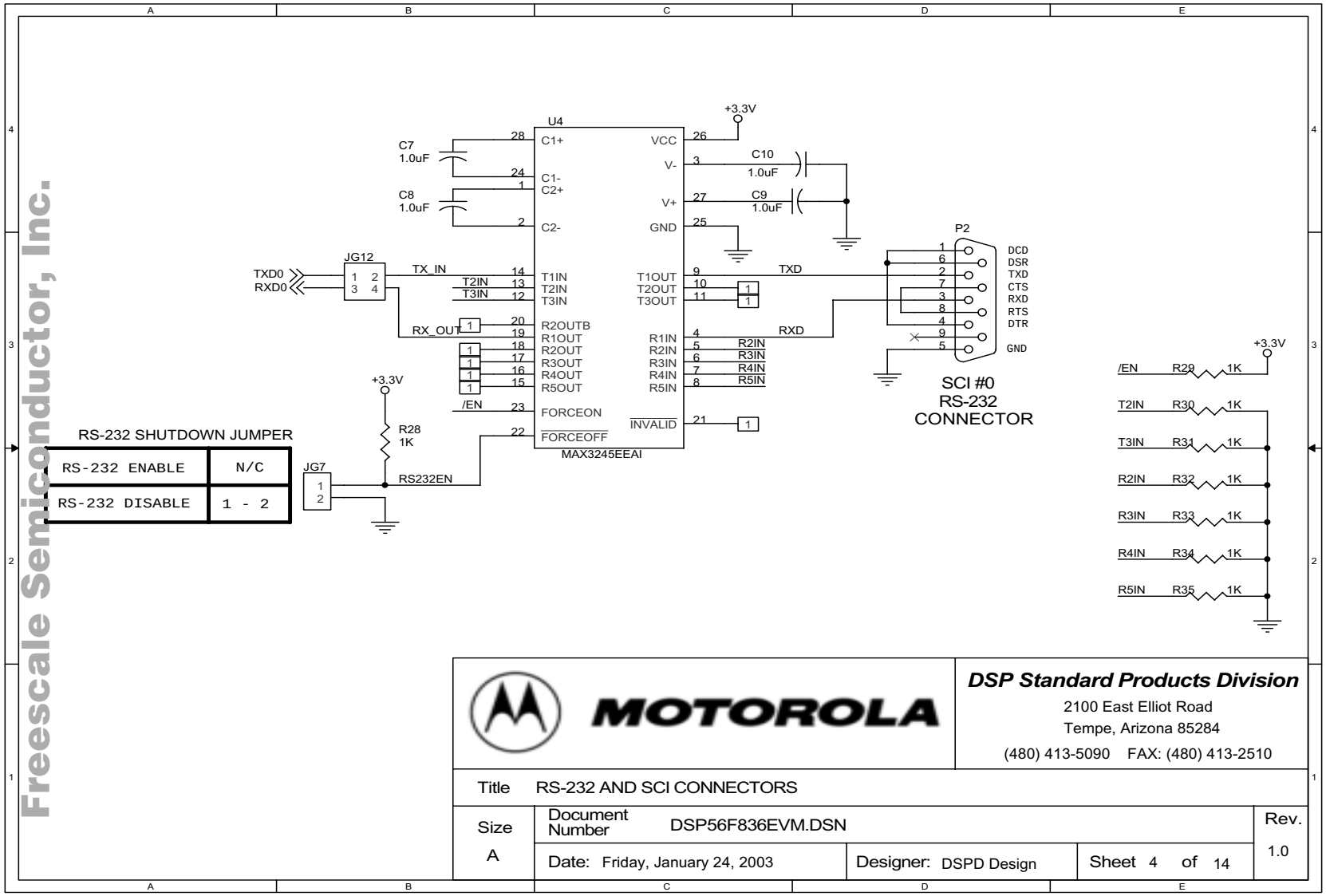


**Figure A-4. RS-232 and SCI Connectors**

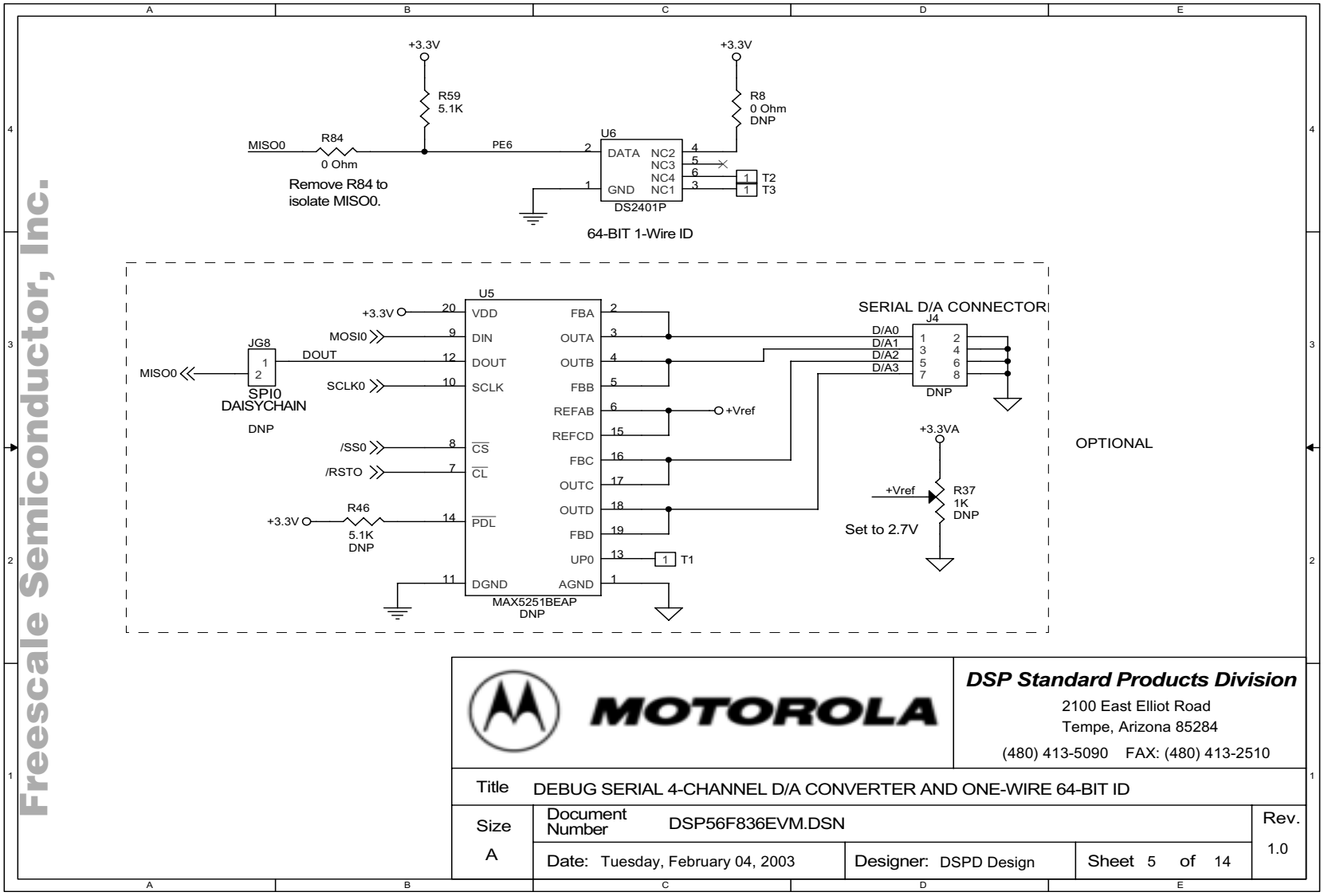


**Figure A-5. Debug Serial 4-Channel D/A Converter and One-Wire 64-Bit ID**

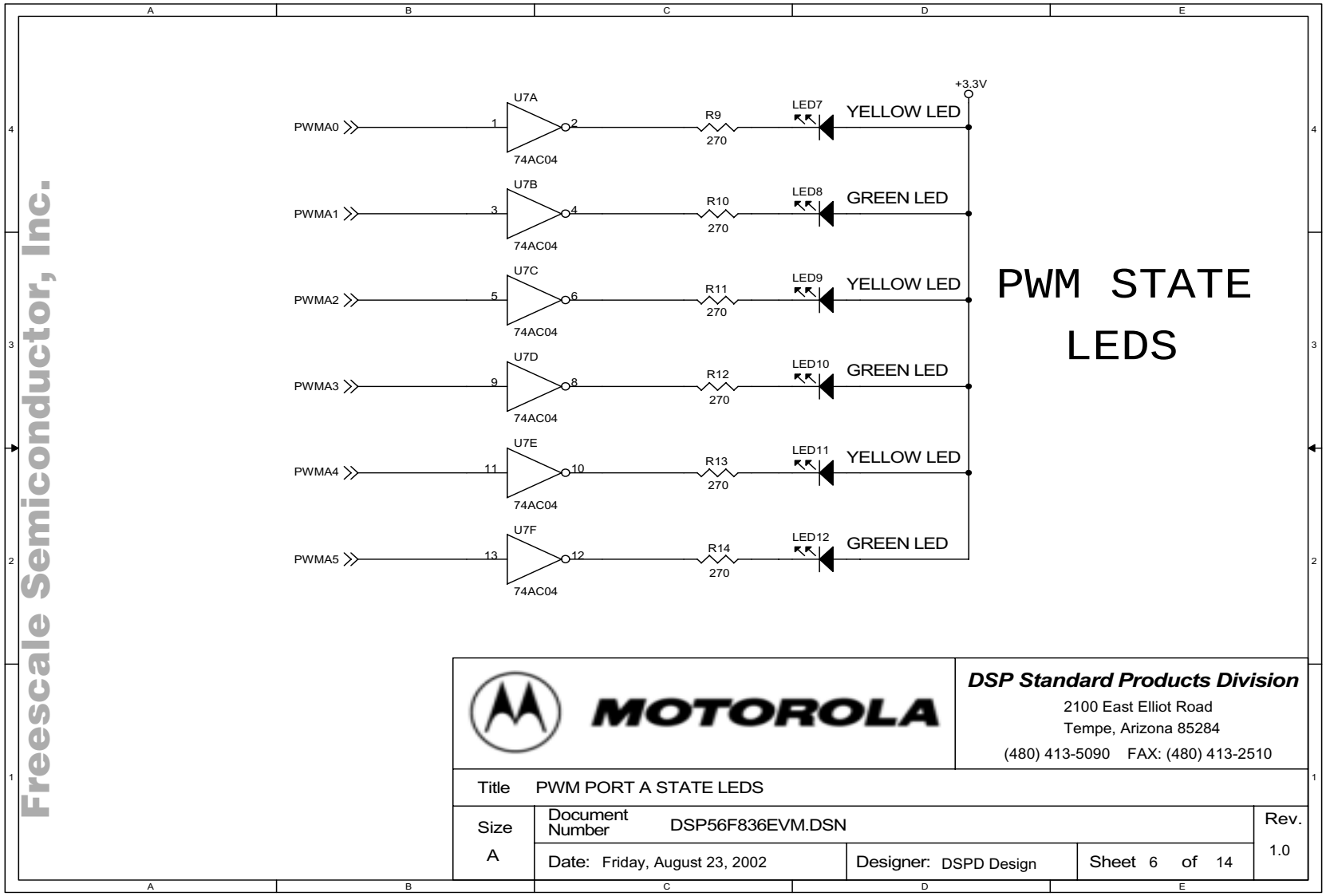


**Figure A-6. PWM Port A State LEDs**

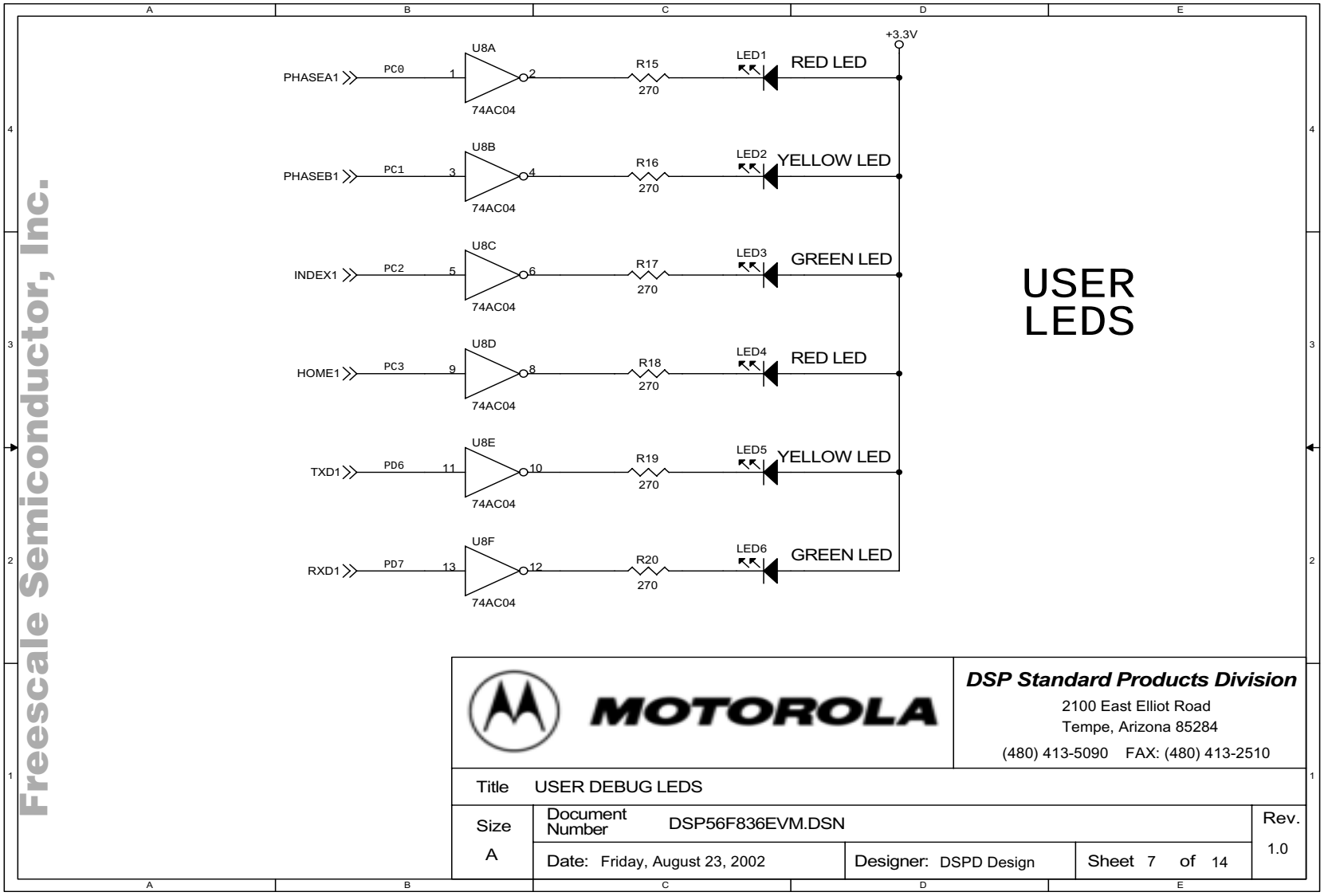


**Figure A-7. User Debug LEDs**

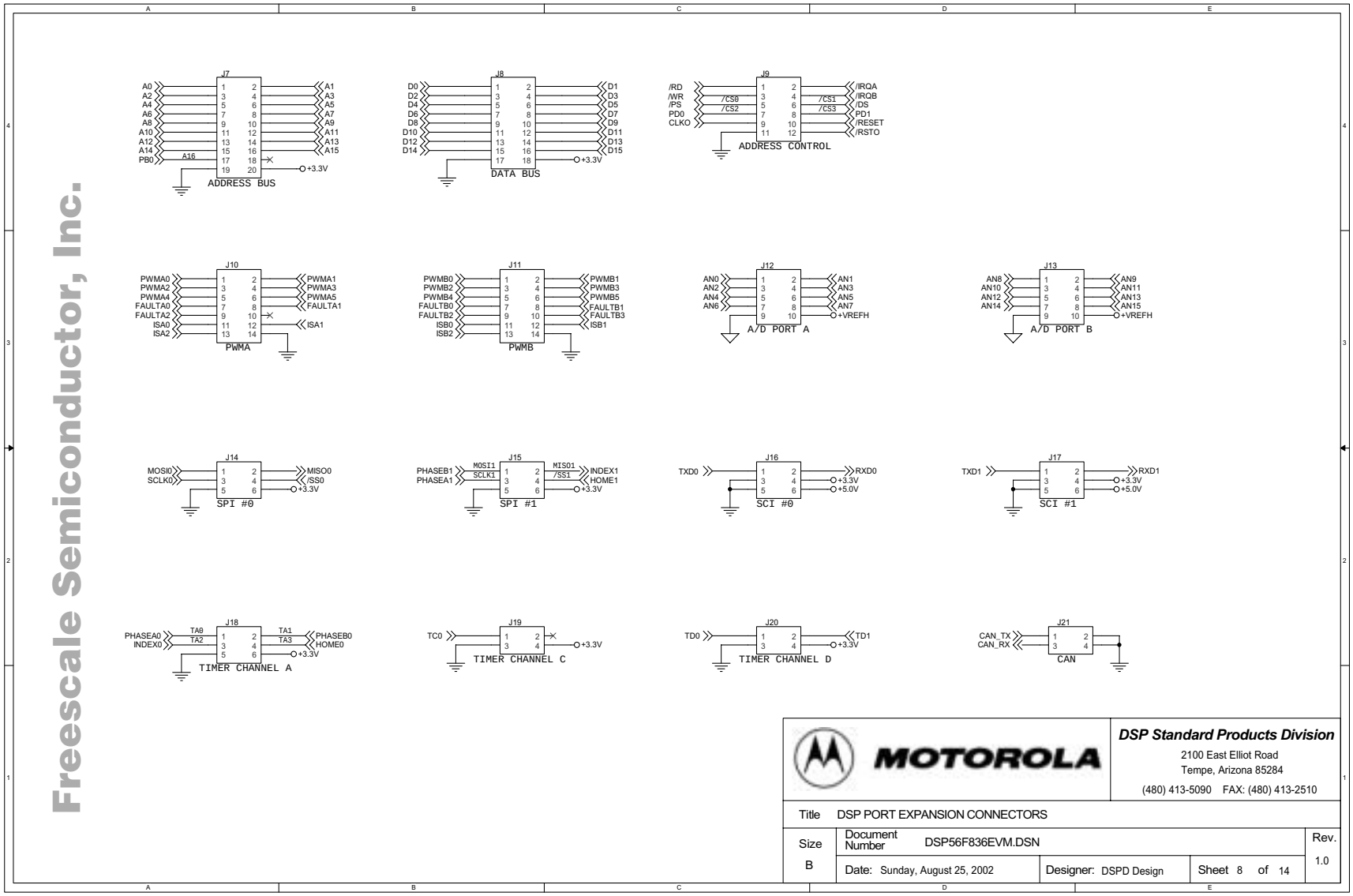


**Figure A-8. Port Expansion Connectors**

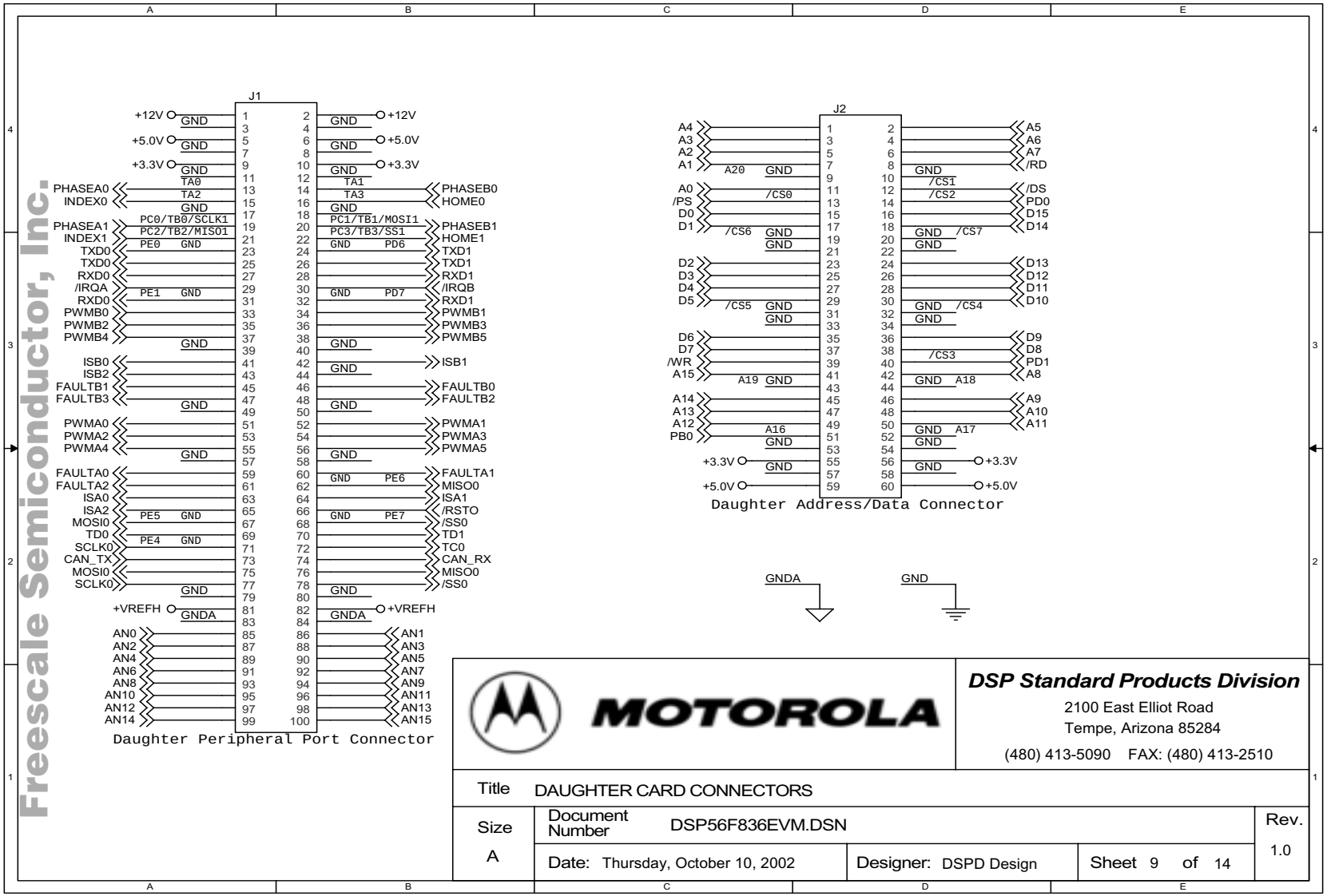


**Figure A-9. Daughter Card Connectors**

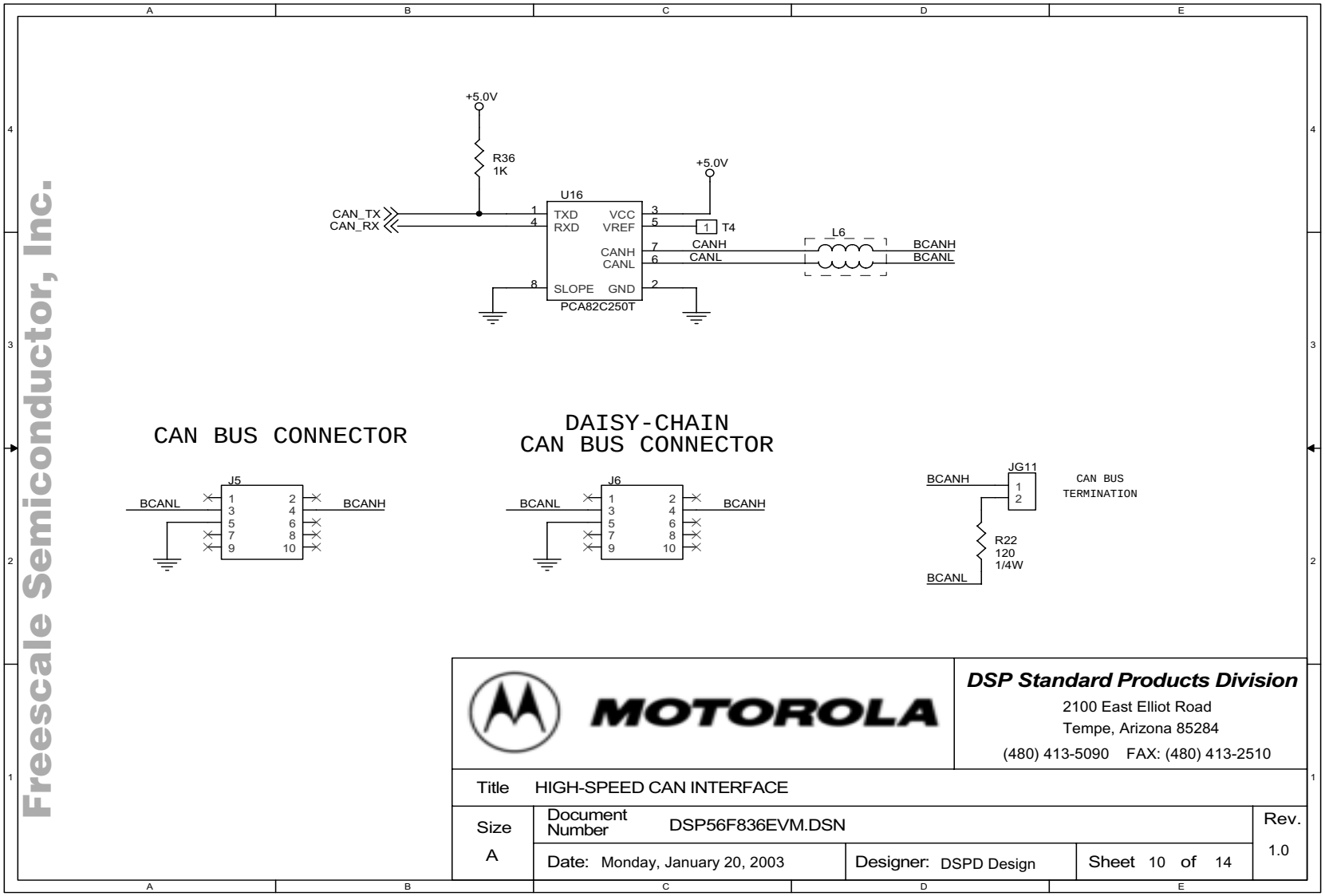


**Figure A-10. High-Speed CAN Interface**

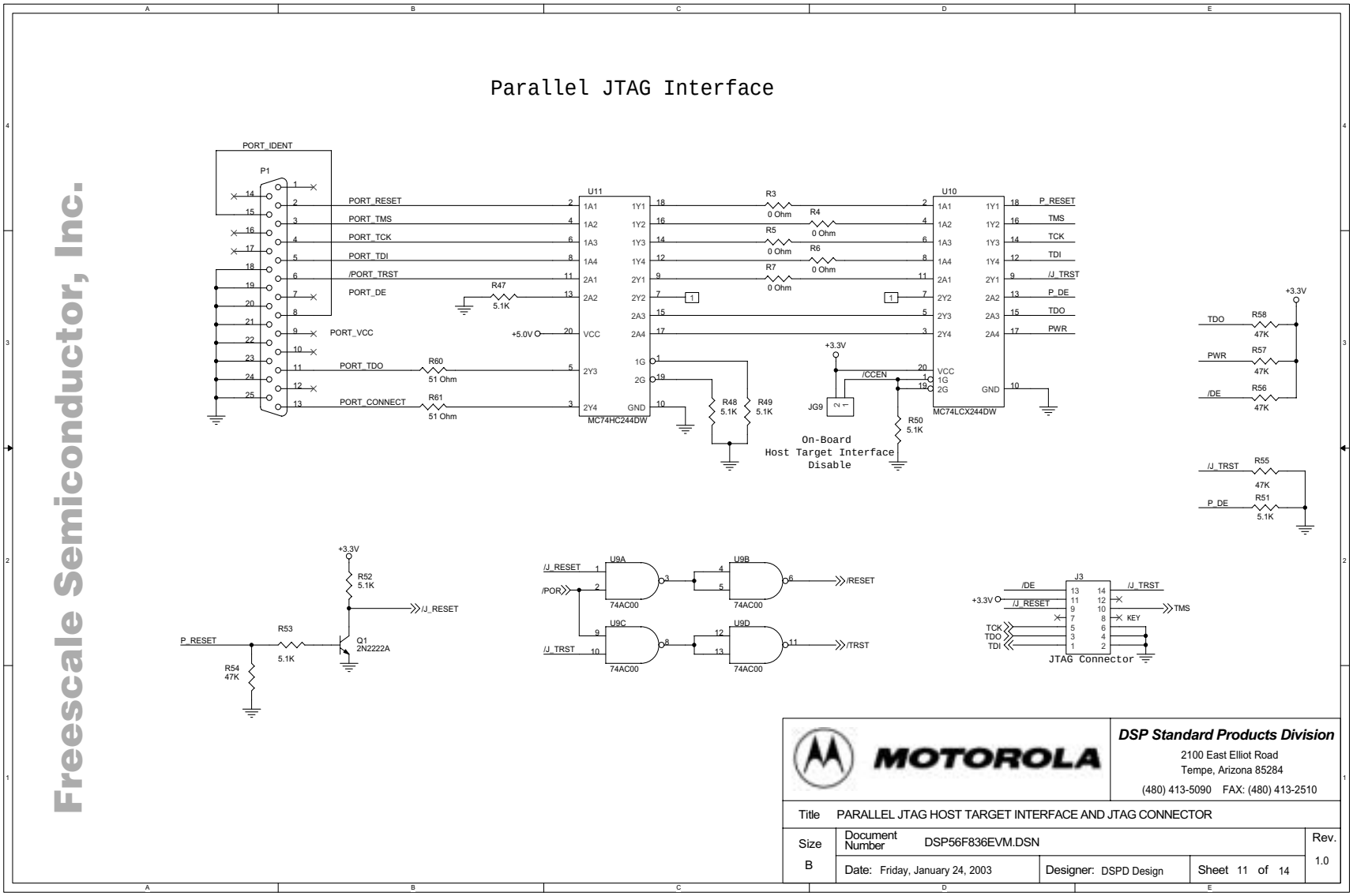


**Figure A-11. Parallel JTAG Host Target Interface and JTAG Connector**

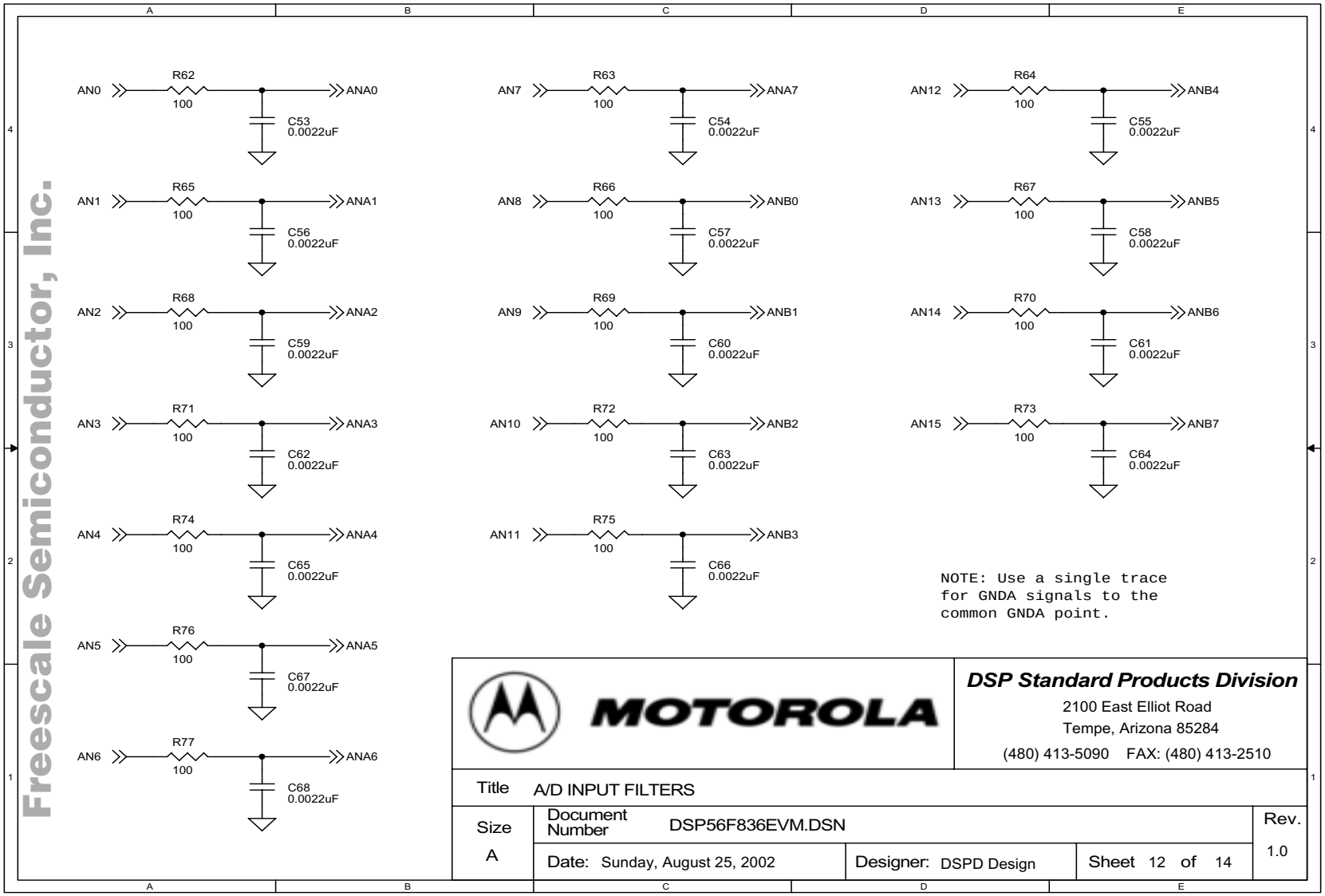


**Figure A-12. A/D Input Filters**

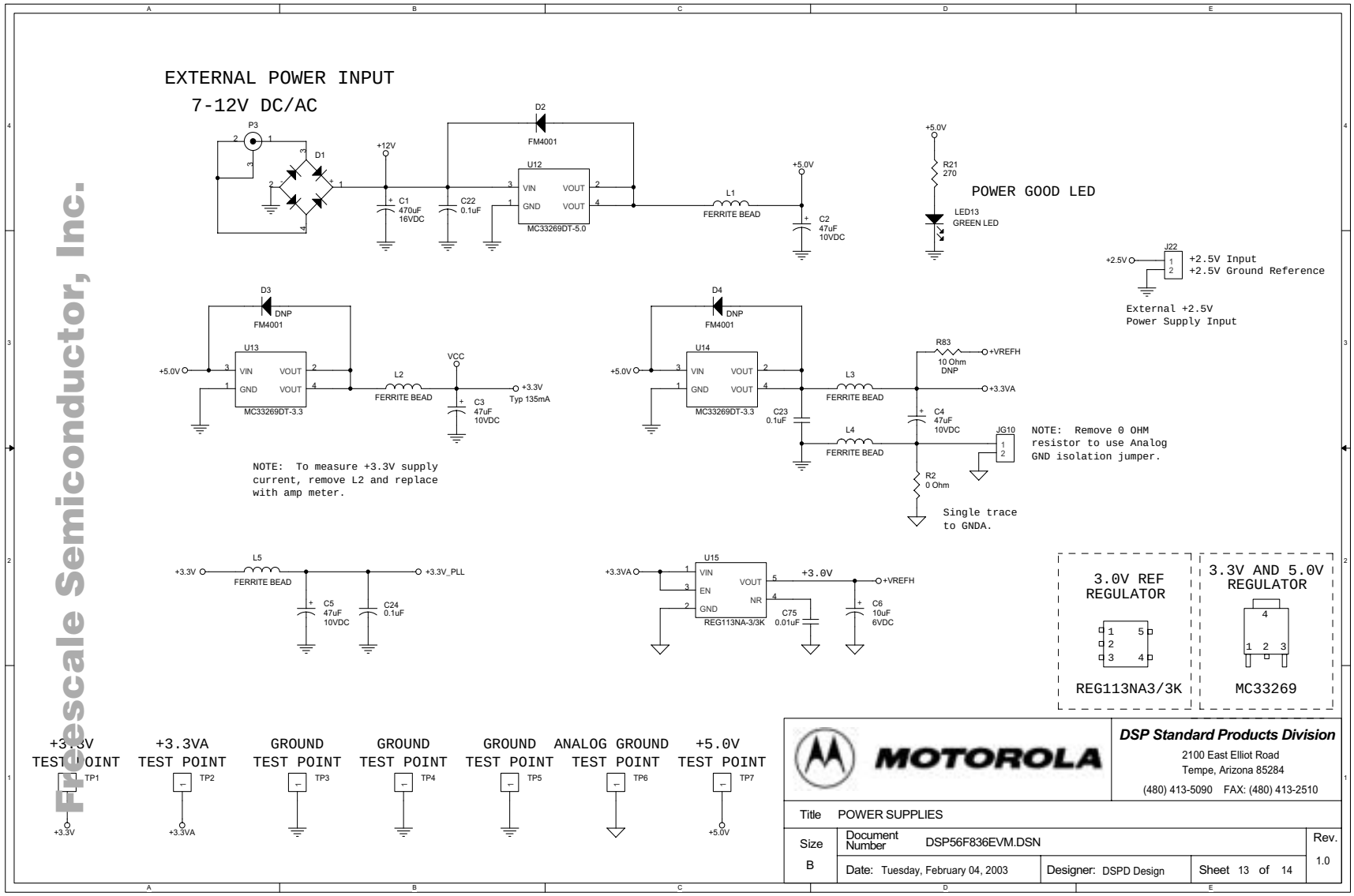




**Figure A-13. Power Supplies**

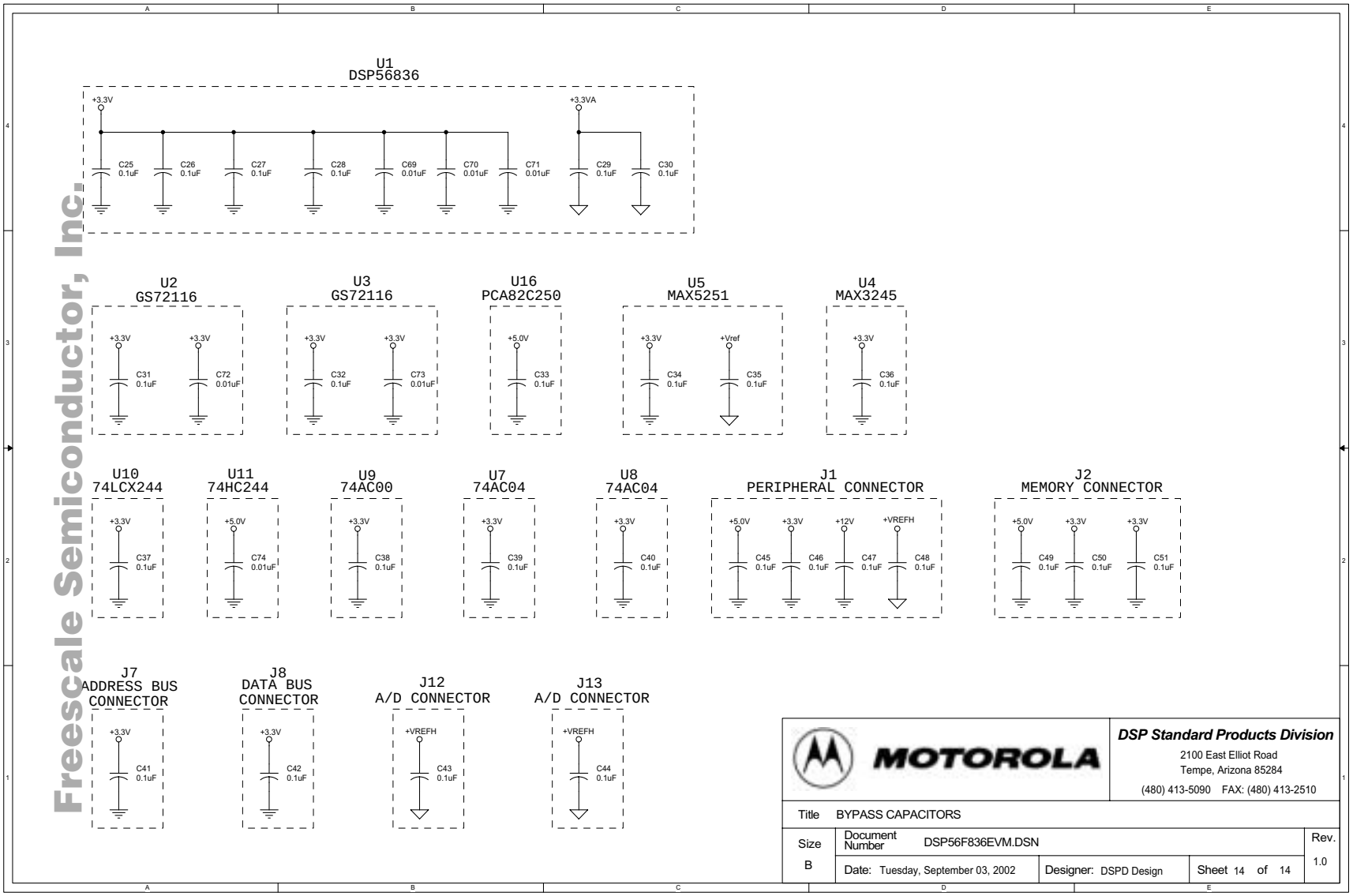


**Figure A-14. Bypass Capacitors**

# Appendix B
# 56F8346EVM Bill of Material

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Integrated Circuits** | | | |
| 1 | 56F8346 | U1 | Motorola, DSP56F8346FV60 |
| 2 | 128Kx16-Bit SRAM | U2, U3 | GSI, GS72116ATP-10 |
| 1 | RS-232 Transceiver | U4 | Maxim, MAX3245EEAI |
| 0 | SPI 4-Channel D/A | U5 (Optional) | Maxim, MAX5251BEAP |
| 1 | 64-Bit 1-Wire ID | U6 | Dallas Semiconductor, DS2401P |
| 2 | 74AC04 | U7, U8 | ON Semiconductor, MC74AC04AD |
| 1 | 74AC00 | U9 | Fairchild, 74AC00SC |
| 1 | 74LCX244 | U10 | ON Semiconductor, MC74LCX244ADW |
| 1 | 74HC244 | U11 | ON Semiconductor, MC74LHC44AADW |
| 1 | +5.0V Voltage Regulator | U12 | ON Semiconductor, MC33269DT-5 |
| 2 | +3.3V Voltage Regulator | U13, U14 | ON Semiconductor, MC33269DT-3.3 |
| 1 | +3.0V Voltage Regulator | U15 | Burr-Brown, REG113NA-3/3K |
| 1 | CAN Transceiver | U16 | Philips Semiconductor, PCA82C250T |
| 0 | Power-ON Reset | U17 (Optional) | Dallas Semiconductor, DS1818 |
| **Resistors** | | | |
| 1 | 10M Ω | R1 | SMEC, RC73L2A106OHMJT |
| 8 | 0 Ω | R2–R7, R84, R97 | SMEC, RC73JP2A |
| 0 | 0 Ω | R8, R92–R96 (Optional) | SMEC, RC73JP2A |
| 13 | 270 Ω | R9 - R21 | SMEC, RC73L2A271OHMJT |
| 1 | 120 Ω, 1/4W | R22 | YAGEO, CFR 120QBK |
| 13 | 10K Ω | R23, R38–R45, R79–R82 | SMEC, RC73L2A103OHMJT |

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| 12 | 1K Ω | R25–R36 | SMEC, RC73L2A103OHMJT |
| 0 | 5.1K Ω | R46 (Optional) | SMEC, RC73L2A512OHMJT |
| 8 | 5.1K Ω | R47–R53, R59 | SMEC, RC73L2A512OHMJT |
| 12 | 47K Ω | R54–R58, R85–R91 | SMEC, RC73L2A473OHMJT |
| 2 | 51 Ω | R60, R61 | SMEC, RC73L2A51OHMJT |
| 16 | 100 Ω | R62–R77 | SMEC, RC73L2A101OHMJT |
| 0 | 10 Ω | R83 (Optional) | SMEC, RC73L2A100OHMJT |
| **Potentioneters** | | | |
| 0 | 1K Ω | R37 (Optional) | BC/MEPCOPAL, ST4B102CT |
| **Inductors** | | | |
| 5 | 1.0mH FERRITE BEAD | L1–L5 | Panasonic, EXC-ELSA35V |
| 1 | CAN Bus Filter | L6 | EPCOS, B82790-S0513-N201 |
| **LEDs** | | | |
| 2 | Red LED | LED1, LED4 | Hewlett-Packard, HSMS-C650 |
| 5 | Yellow LED | LED2, LED5, LED7, LED9, LED11 | Hewlett-Packard, HSMY-C650 |
| 6 | Green LED | LED3, LED6, LED8, LED10, LED12, LED13 | Hewlett-Packard, HSMG-C650 |
| **Diode** | | | |
| 1 | +50V 1A BRIDGE RECT | D1 | DIODES, DF02S |
| 1 | S2B-FM401 | D2 | Vishay, DL4001DICT |
| 0 | S2B-FM401 | D3 & D4 (Optional) | Vishay, DL4001DICT |

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Capacitors** | | | |
| 1 | 470µF, +16V DC | C1 | ELMA, RV-16V471MH10R |
| 4 | 47µF, +16V DC | C2–C5 | ELMA, RV2-16V470M-R |
| 1 | 10µF, +10V DC | C6 | KEMET, T494B106M010AS |
| 4 | 1.0µF, +25V DC | C7–C10 | SMEC, MCCE105K3NR-T1 |
| 4 | 2.2µF, +25V DC (Low ESR) | C11–C14 | TAIYO YUDEN, CELMK212BJ225MG-T |
| 1 | 0.001µF | C15 | SMEC, MCCE102K2NR-T1 |
| 36 | 0.1µF | C16–C51 | SMEC, MCCE104K2NR-T1 |
| 1 | 100pF | C52 | SMEC, MCCE101K2NR-T1 |
| 16 | 0.0022µF | C53–C68 | SMEC, MCCE222K2NR-T1 |
| 7 | 0.01µF | C69–C75 | SMEC, MCCE103K2NR-T1 |

| | | | |
|---|---|---|---|
| **Jumpers** | | | |
| 3 | 3 × 1 Bergstick | JG1, JG15, JG16 | SAMTEC, TSW-103-07-S-S |
| 10 | 1 × 2 Bergstick | JG2–JG5, JG7, JG9–JG11, JG13, JG14 | SAMTEC, TSW-102-07-S-S |
| 2 | 2 × 2 Bergstick | JG6, JG12 | SAMTEC, TSW-102-07-S-D |
| 0 | 1 × 2 Bergstick | JG8 (Optional) | SAMTEC, TSW-102-07-S-S |
| **Test Points** | | | |
| 1 | +3.3V Test Point | TP1 | KEYSTONE, 5000 |
| 1 | +3.3VA Test Point | TP2 | KEYSTONE, 5004 |
| 3 | GND Test Point | TP3, TP4, TP5 | KEYSTONE, 5001 |
| 1 | GNDA Test Point | TP6 | KEYSTONE, 5002 |
| 1 | +5.0V Test Point | TP7 | KEYSTONE, 5003 |
| 0 | 1 × 1 Bergstick | T1–T3 (Optional) | Samtec, TSW-101-06-S-S |

| | | | |
|---|---|---|---|
| **Crystals** | | | |
| 1 | 8.00MHz Crystal | Y1 | CTS, ATS08ASM-T |
| **Connectors** | | | |
| 1 | DB25M Connector | P1 | AMPHENOL, 617-C025P-AJ121 |
| 1 | DE9S Connector | P2 | AMPHENOL, 617-C009S-AJ120 |
| 1 | 2.1mm coax Power Connector | P3 | Switchcraft, RAPC-722 |
| 1 | Peripheral Daughter Card Connector | J1 | HRS, FX6-100P-0.8SV2 |
| 1 | Memory Bus Daughter Card Connector | J2 | HRS, FX6-60P-0.8SV2 |
| 1 | 7x2 JTAG Header | J3 | SAMTEC, TSW-107-07-S-D |
| 1 | 4x2 Header | J4 | SAMTEC, TSW-106-04-S-D |
| 4 | 5x2 Header | J5, J6, J12, J13 | SAMTEC, TSW-106-05-S-D |
| 1 | 10x2 Header | J7 | SAMTEC, TSW-106-10-S-D |
| 1 | 9x2 Header | J8 | SAMTEC, TSW-106-09-S-D |
| 1 | 6x2 Header | J9 | SAMTEC, TSW-106-06-S-D |
| 2 | 7x2 Header | J10, J11 | SAMTEC, TSW-106-07-S-D |
| 5 | 3x2 Header | J14–J18 | SAMTEC, TSW-106-03-S-D |
| 3 | 2x2 Header | J19–J21 | SAMTEC, TSW-106-02-S-D |
| 1 | 1x2 Header | J22 | SAMTEC, TSW-106-02-S-S |
| **Switches** | | | |
| 3 | SPST Pushbutton | S1–S3 | Panasonic, EVQ-PAD05R |
| **Transistors** | | | |
| 1 | 2N2222A | Q1 | ZETEX, FMMT2222ACT |
| **Miscellaneous** | | | |
| 13 | Shunt | SH1–SH13 | Samtec, SNT-100-BL-T |
| 4 | Rubber Feet | RF1–RF4 | 3M, SJ5018BLKC |

# Index

## Numerics



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