IP-Unidig-E-48

48 Line Input/Output with LineSafe™ ESD Protection IndustryPack®

User's Manual

Manual Revision: 3 7/28/99 Hardware Revision: B

IP-Unidig-E-48

(415) 327-3808 FAX

48 Line Input/Output
with LineSafe™ ESD Protection
IndustryPack®

GreenSpring Computers
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200

This document contains information of proprietary interest to GreenSpring Computers. It has been supplied in confidence and the recipient, by accepting this material, agrees that the subject matter will not be copied or reproduced, in whole or in part, nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

GreenSpring Computers has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, GreenSpring Computers assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

This product has been designed to operate with IndustryPack carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Table of Contents

List of Figures

Product Description

The IP-Unidig-E-48 is part of the IndustryPack™ family of modular I/O components. It provides 48 lines of digital I/O, each with GreenSpring's unique LineSafe™ electrostatic discharge (ESD) protection circuit for increased ruggedness. Each line may be dynamically and individually configured for either input or output. Outputs may be double buffered, making it possible to synchronize multiple IPs. Both internal read back and direct read registers are provided for ease of software development. 16-bit word and 8-bit byte operations are supported.

The IP-Unidig-E-48 conforms to the IndustryPack Interface Specification. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module with final system implementation on a different one.

The IP-Unidig-E-48 is a member of the Unified Digital family of I/O. It is the only member with 48 outputs which are organized as two 24 bit registers. Other members of the family include a 24 I/O version with ESD protected I/O, buffered TTL I/O, differential I/O, optically isolated I/O, and high voltage I/O. Functions implemented within each output type include double buffered I/O, I/O with interrupts on all input lines, and four independent timers.

The software interface to the IP-Unidig-E-48 is simple and straight forward. Writing a one to any line turns off the output driver, allowing a passive pull up resistor to set the line to a logic high. Writing a zero to any line turns on the driver, driving the line to a logic low. For input use, a one is written to the corresponding line - this is the power up default. For output use, the binary value desired is written to the corresponding line.

Input and output lines may be double buffered by setting a bit in the Control Register. When this bit is set, the user must provide an external clock of up to 1 MHz. Another bit in the Control Register selects the polarity of this clock, allowing inputs and outputs to be latched on either the rising or falling clock edge. The IP-Unidig-T is ideally suited for generating this clock, though most TTL compatible clock sources may be used.

Two separate locations in I/O space are provided for each signal line. The first location is used to set the output state and also to read back the written value at the internal latch. This read back function is valuable to support bit operations (which are implemented by processors as read-modify-write cycles). It is also useful in debugging, making it possible to observe directly the last value written to the port. The second location is the direct read port, which is always used for reading input values. This register may also be used to verify the correct logic signal is actually on the interface cable.

Figure 1 shows a block diagram of the IP-Unidig-E-48.

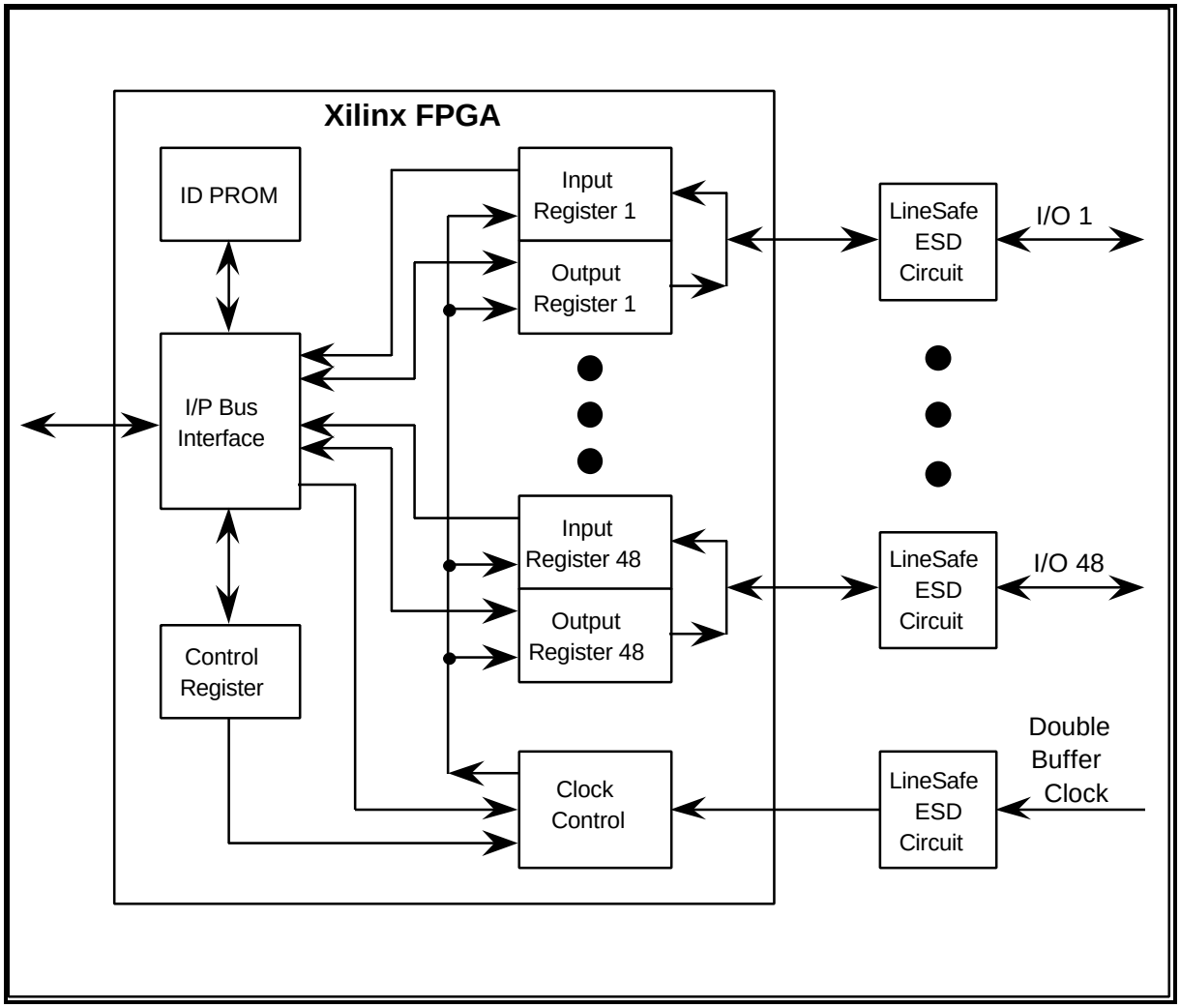

Figure 1 IP-Unidig-E-48 Block Diagram

VMEbus Addressing

IP-Unidig-E-48 normally is accessed one word at a time in the host's I/O space. Alternatively, byte or long word accesses may be used. If long words are used, the host (or support module) must map 32-bit long words into two 16-bit cycles. This is common for 68020 and 68030 implementation of the I/O space.

Standard Word Access, I/O Space

base + 0x0	word	write	Output lines 1– 16
base + 0x2	word	write	Output lines 17– 24
base + 0x0	word	read	Read back lines 1– 16
base + 0x2	word	read	Read back lines 17– 24
base + 0x4	word	read	Direct read lines 1– 16
base + 0x6	word	read	Direct read lines 17– 24
base + $C	word	read/write	Control Register
base + 0x40	word	write	Output lines 25– 40
base + 0x42	word	write	Output lines 41– 48
base + 0x40	word	read	Read backlines 25– 40
base + 0x42	word	read	Read backlines 41– 48
base + 0x44	word	read	Direct read lines 25– 40
base + 0x46	word	read	Direct read lines 41– 48

Figure 2 Word Access VME Address Map

Bit map of words at base + $0 and base + $6

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2 and base + $8

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Bit map of words at base + $40 and base + $44

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

Bit map of words at base + $42 and base + $46

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	48	47	46	45	44	43	42	41

Bit map of word at base + $C

Data Bit #	[15:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Alternate Byte Access, I/O Space

base + 0x0	byte	write	Output lines 9– 16
base + 0x1	byte	write	Output lines 1– 8
base + 0x3	byte	write	Output lines 17– 24
base + 0x0	byte	read	Read Back lines 9– 16
base + 0x1	byte	read	Read Back lines 1– 8
base + 0x3	byte	read	Read Back lines 17– 24
base + 0x4	byte	read	Direct Read lines 9– 16
base + 0x5	byte	read	Direct Read lines 1– 8
base + 0x6	byte	read	Direct Read lines 17– 24
base + $D	byte	read/write	Control Register
base + 0x40	byte	write	Output lines 33– 40
base + 0x41	byte	write	Output lines 25– 32
base + 0x43	byte	write	Output lines 41– 48
base + 0x40	byte	read	Read Back lines 33– 40
base + 0x41	byte	read	Read Back lines 25– 32
base + 0x43	byte	read	Read Back lines 41– 48
base + 0x44	byte	read	Direct Read lines 33– 40
base + 0x45	byte	read	Direct Read lines 25– 32
base + 0x47	byte	read	Direct Read lines 41– 48

Figure 3 Byte Access VME Address Map

Bit map of bytes at base + $0 and base + $4

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $1 and base + $5

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $3 and base + $7

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of bytes at base + $40 and base + $44

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	40	39	38	37	36	35	34	33

Bit map of bytes at base + $41 and base + $45

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	32	31	30	29	28	27	26	25

Bit map of bytes at base + $43 and base + $47

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	48	47	46	45	44	43	42	41

Bit map of byte at base + $D

Data Bit #	[7:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Alternate Long Word Access, I/O Space

base + $0	long	write	Output lines 1– 24
base + $0	long	read	Read Back lines 1– 24
base + $4	long	read	Direct Read lines 1– 24
base + $C	long	read/write	Control Register
base + $40	long	write	Output lines 25– 48
base + $40	long	read	Read Back lines 25– 48
base + $44	long	read	Direct Read lines 25– 48

Figure 4 Long Word Access VME Address Map

Bit map of long words at base + $0 and base + $4

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Bit map of long words at base + $40 and base + $44

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Line:	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	48	47	46	45	44	43	42	41

Bit map of long word at base + $C

Data Bit #	[31:18]	17	16	[15:0]
Write:	-	Clock Polarity	Dbl. Buffer En.	-
Read:	0	Clock Polarity	Dbl. Buffer En.	0

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

ISA (IBM PC-AT) Addressing

IP-Unidig-E-48 normally is accessed one word at a time in the host's I/O space. Alternatively, byte accesses may be used. The actual application will depend on the carrier board. See the carrier board manual for details.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1– 16
base + $2	word	write	Output lines 17– 24
base + $0	word	read	Read Back lines 1– 16
base + $2	word	read	Read Back lines 17– 24
base + $4	word	read	Direct Read lines 1– 16
base + $6	word	read	Direct Read lines 17– 24
base + $C	word	read/write	Control Register
base + $40	word	write	Output lines 25– 40
base + $42	word	write	Output lines 41– 48
base + $40	word	read	Read Back lines 25– 40
base + $42	word	write	Read Back lines 41– 48
base + $44	word	read	Direct Read lines 25– 40
base + $46	word	read	Direct Read lines 41– 48

Figure 5 Word Access ISA Address Map

Bit map of words at base + $0 and base + $4

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2 and base + $6

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Bit map of words at base + $40 and base + $44

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

Bit map of words at base + $42 and base + $46

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	48	47	46	45	44	43	42	41

Bit map of word at base + $C

Data Bit #	[15:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Alternative Byte Access, I/O Space

base + $0	byte	write	Output lines 1– 8
base + $1	byte	write	Output lines 9– 16
base + $2	byte	write	Output lines 17– 24
base + $0	byte	read	Read-back lines 1– 8
base + $1	byte	read	Read-back lines 9– 16
base + $2	byte	read	Read-back lines 17– 24
base + $4	byte	read	Direct Read lines 1– 8
base + $5	byte	read	Direct Read lines 9– 16
base + $6	byte	read	Direct Read lines 17– 24
base + $C	byte	read	Control Register
base + $40	byte	write	Output lines 25– 32
base + $41	byte	write	Output lines 33– 40
base + $42	byte	write	Output lines 41– 48
base + $40	byte	read	Read-back lines 25– 32
base + $41	byte	read	Read-back lines 33– 40
base + $42	byte	read	Read-back lines 41– 48
base + $44	byte	read	Direct Read lines 25– 32
base + $45	byte	read	Direct Read lines 33– 40
base + $46	byte	read	Direct Read lines 41– 48

Figure 6 Byte Access ISA Address Map

Bit map of bytes at base + $0 and base + $4

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $1 and base + $5

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $2 and base + $6

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of bytes at base + $40 and base + $44

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	32	31	30	29	28	27	26	25

Bit map of bytes at base + $41 and base + $45

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	40	39	38	37	36	35	34	33

Bit map of bytes at base + $42 and base + $46

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	48	47	46	45	44	43	42	41

Bit map of byte at base + $C

Data Bit #	[7:4]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

I/O Pin Wiring

This section gives the pin assignments and wiring recommendations for IP-Unidig-E-48.

The pin numbers given in Figure 2 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O 1	1	I/O 2	2
I/O 3	3	I/O 4	4
I/O 5	5	I/O 6	6
I/O 7	7	I/O 8	8
I/O 9	9	I/O 10	10
I/O 11	11	I/O 12	12
I/O 13	13	I/O 14	14
I/O 15	15	I/O 16	16
I/O 17	17	I/O 18	18
I/O 19	19	I/O 20	20
I/O 21	21	I/O 22	22
I/O 23	23	I/O 24	24
I/O 25	25	I/O 26	26
I/O 27	27	I/O 28	28
I/O 29	29	I/O 30	30
I/O 31	31	I/O 32	32
I/O 33	33	I/O 34	34
I/O 35	35	I/O 36	36
I/O 37	37	I/O 38	38
I/O 39	39	I/O 40	40
I/O 41	41	I/O 42	42
I/O 43	43	I/O 44	44
I/O 45	45	I/O 46	46
I/O 47	47	I/O 48	48
Double Buffer Clk	49	GND	50

Figure 7 I/O Pin Assignment

IndustryPack Logic Interface Pin Assignment

Figure 3 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Unidig-E-48. Pins marked n/c below are defined by the specification, but are not used on IP-Unidig-E-48. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1		26	
CLK	+5V		2		27
Reset*	R/W*	3		28	
D0	IDSel*		4		29
D1	n/c	5		30	
D2	n/c		6		31
D3	n/c	7		32	
D4	n/c		8		33
D5	n/c	9		34	
D6	IOSel*		10		35
D7	n/c	11		36	
D8	A1		12		37
D9	n/c	13		38	
D10	A2		14		39
D11	n/c	15		40	
D12	A3		16		41
D13	n/c	17		42	
D14	A4		18		43
D15	n/c	19		44	
BS0*	A5		20		45
BS1*	n/c	21		46	
–12V	A6		22		47
+12V	Ack*	23		48	
+5V	n/c		24		49
GND	GND	25		50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 8 Logic Interface Pin Assignment

Programming

Programming the IP requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This document refers to this address as "base".

After power on reset or VME system reset, the IP requires a minimum delay of 300 milliseconds before any accesses are made by the host system. This is to allow the Xilinx FPGA to configured itself. Any accesses during this time will result in a bus error. Reset sets all lines to be inputs and clears all bits in the Control Register.

Each of the 48 bits may be individually set as input or output. To set a bit to be input, write a "1" to the I/O bit location. This is the default.

To write a zero on the I/O signal line, write a "0" to the I/O bit location. To write a one on the I/O signal line, write a "1" to the I/O bit location. Writing a one and setting the signal line to input mode is the same. Passive pull-up resistors are used with tri-state drivers to implement the interface.

Using word access, up to 16 bits may be programmed at once. The IP implements a read back register at the same address used for writing to the signal line I/O bits. This permits "set bit" and "clear bit" instructions to be used in programming, which are implemented by the host hardware as read-modify-write cycles. Thus, single bits at well as bit fields may be accessed. The IP is organized into two 24 bit registers to maintain software compatibility with the Unidig family memory map.

The IP may also be accessed using byte or long word accesses. If long word accesses are used from a 68020, 68030, or 68040 host, the I/O space must be mapped into "D16". 68000 and 68010 hosts internally map all long word accesses into 16 bits, so no special precaution is necessary. Long word accesses use two separate IP cycles.

The IP uses a Control Register to enable double buffering and control the polarity of the Double Buffer Clock. I

Bit #	Definition	Access
0	Double Buffer Enable	Read/Write
1	Double Buffer Clock Polarity Select	Read/Write
2— 7	Reserved	Read as "0"

Figure 9 Control Register Bit Definitions

Control Register Bit Definitions:

Bit [0] = D0 LSB Double Buffer Enable
Double Buffer Enable bit. This bit enables double buffering. If this bit is set to a "1", the user must provide a clock on the Double Buffer Clock, pin 49. This clock may be up to 1 MHz and must have an edge rate faster than 60 ns. Writing a "0" disables double buffering. This is the default.

Bit [1] = D1 Double Buffer Clock Polarity Select

Double Buffer Clock Polarity Select bit. This bit controls the Double Buffer Clock polarity. Writing a "1" will cause output data to be latched out of the IP and input data to be latched into the IP on the falling edge of the Double Buffer Clock. Writing a "0" will cause data to be latched on the rising edge of the Double Buffer Clock. This is the default.

Bit [7..2] = D7..D2

These bits are reserved for future use and will be read as "0".

Double Buffering

Double buffering is a feature which allows all the inputs and outputs to be latched at the same time, whether on a single IP or a system with multiple IPs. This is useful for systems which require many inputs and outputs to be updated simultaneously. To use double buffering, an external TTL or CMOS level clock with an edge rate faster than 60 ns must be provided on Pin 49, the Double Buffer Clock Input pin and the Double Buffer Enable bit, Bit [0], in the Control Register must be set. The Double Buffer Clock polarity is programmable via the Double Buffer Clock Polarity bit, Bit [1], in the Control Register. Setting this bit to a "0" will cause the input and outputs to be latched on the rising edge of the Double Buffer Clock, while setting the bit to "1" will latch the inputs and outputs on the falling edge.

ID PROM

Every IP contains an IP PROM, whose size is at least 12 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-Unidig-E-48 is shown in Figure 10 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers, Inc.. The ID PROM on the IP-Unidig-E-48 is implemented in the Xilinx FPGA device.

The location of the ID PROM in the host's address space is dependent on the carrier board used. For most VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 5 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC for bytes used	(84)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(A2)
0B	Model No IP-Unidig-E-48	(65)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII “C”	(43)
05	ASCII “A”	(41)
03	ASCII “P”	(50)
01	ASCII “I”	(49)

Figure 10 ID PROM Data (hex)

Theory of Operation

IndustryPack Standards

The IP-Unidig-E-48 is part of the IndustryPack™ family of modular I/O products. It meets the IndustryPack Logic Specification. (Contact GreenSpring Computers, Inc. for a copy of this Specification.) It is assumed the reader is at least casually familiar with both this document and 68000 processor architecture.

Control Logic

All control logic is contained within a single Xilinx FPGA. It is clocked by the 8 MHz IP Logic clock from the Support Module. The IP responds to I/O and ID selects. It does not respond to memory selects, however the MEMSel* line is routed to the FPGA, enabling easy modification for special needs.

The IP does not require wait states for either read or write cycles. Thus, the FPGA generates Ack* on the clock cycle following either I/O or ID Select. Hold cycles (from the Support Module) are supported for both read and write cycles by extending Ack* as required. If no hold cycles are requested by the Support Module, the IP is capable of supporting the full 8 MByte per second data transfer rate of the IP Logic Interface Specification.

I/O Data Lines

All input and output latches and buffers are contained within the Xilinx FPGA. Each I/O line has GreenSpring's unique LineSafe™ ESD protection circuit for added ruggedness. This circuit uses a 33 Ohm resistor in series and an AVX TransGuard® ESD filter with the equivalent of a 1100 pF capacitor to ground on each I/O line. Standard ESD handling precautions should still be used as the IP Logic Interface lines are unprotected. Additionally, external voltage should not be applied when the IP is unpowered. This will damage the Xilinx FPGA. Turning on and off all power supplies at the same time will eliminate this problem.

Outputs use active low tri-state buffers which are controlled by the individual output lines. In this manner, they implement an open drain connection, being enabled when the output is low and disabled when the output is high. Three surface mount 10 K Ohm resistor networks pull up the I/O lines to +5V when the outputs are disabled.

Data Output

Each output has two latches associated with it. If double buffering is enabled, the Double Buffer Latch is clocked by the Double Buffer Clock. Without double buffering, this latch is clocked by the IP Clock. Figure 6 shows a block diagram. Outputs from the Double Buffer Latch directly drive the I/O output lines. Data is latched into the internal latch on the rising edge of the IP Clock after the IOSel* line is driven low.

Double buffering is enabled by setting the Double Buffer Enable Bit (bit [0]) in the Control Register to a "1". A TTL compatible signal must be provided on the External Clock, pin 49. This signal must have an edge rate faster than 60 ns. If double buffering is enabled, the Double Buffer Clock Polarity Bit (bit [1]) in the Control Register is used to set the Double Buffer Clock polarity. Setting the Double Buffer Clock Polarity Bit to a "0" will latch data on the rising edge and setting it to a "1" will latch data on the falling edge. The power up default is "0" for both these bits.

Data Input

The data may be read from two sets of address locations. The first set of locations, base + $0, base + $2 and base + $40 and base + $42 for word operations, function as the Internal Read Back Register. The data latched in the Internal Output Latch is read from these addresses. They support processor bit operations implemented as read-modify-write cycles, and are also useful for debugging purposes.

The second set of locations, base + $4, base + $6 and base + $44 and base + $46 for word operations, is the Direct Read Register. Data is latched into Input Register with the same clock which latches the Double Buffer Latch. Figure 11 shows a block diagram.

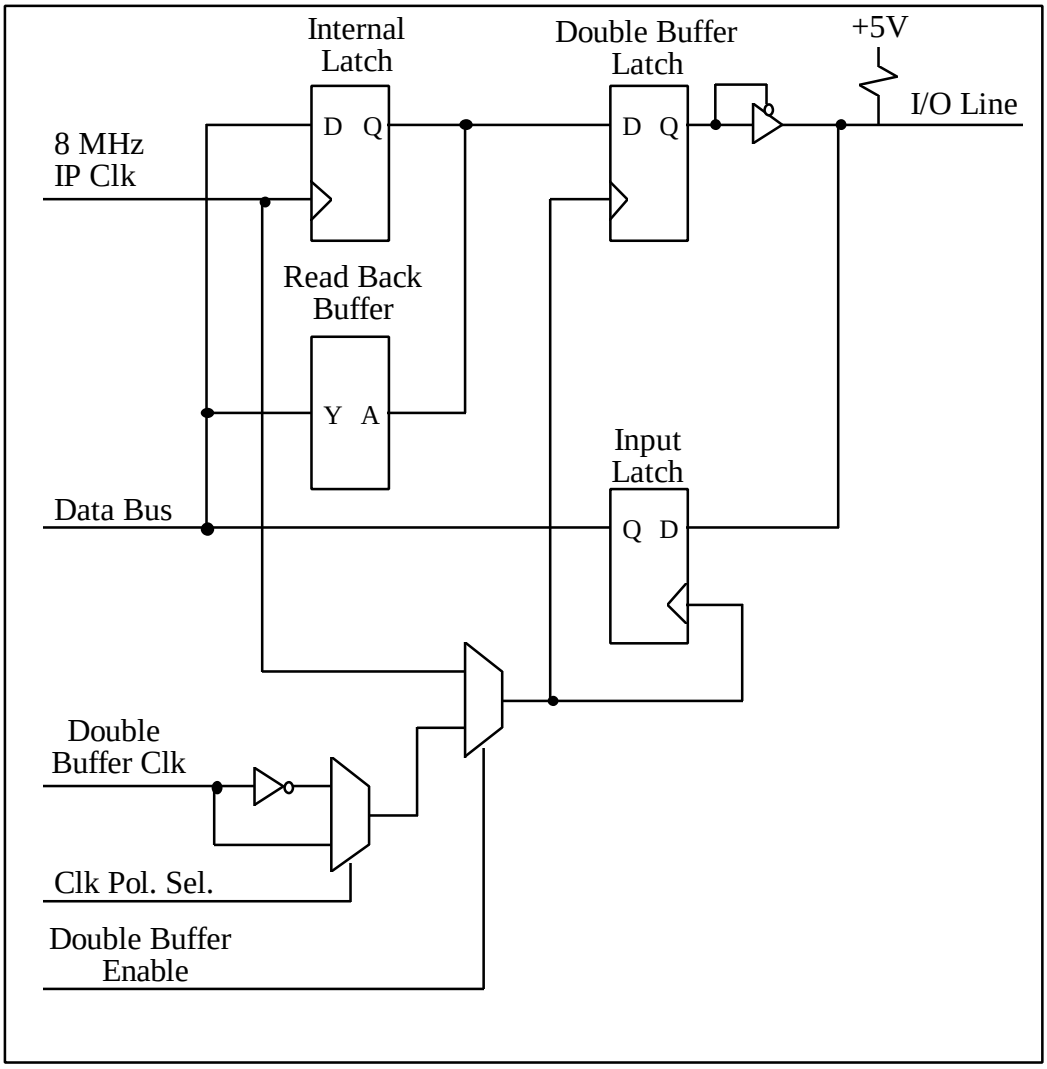

Figure 11 I/O Line Block Diagram

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-UniDig-E is constructed out of 0.062 inch thick FR4 V0 material. The four copper layers consist of two signal layers on the top and bottom, and two internal power and ground plane layers.

Through hole and surface mounting of components are used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and have gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four M2 metric stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, then the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. GreenSpring Computers disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

Specifications

Logic Interface	IndustryPack Logic Interface.
Digital Interface	48 digital signal lines with double buffered outputs and latched inputs. Each line is either an input or an output.
Interface Level	TTL Tri-state with 10 K Ohm pull up resistor standard. 4 mA current sink.
Software Interface	The 48 I/O lines are read and written to with either word or byte accesses. There is an 8-bit Control register.
Initialization	300 millisecond delay from reset. Forces all lines to be inputs. Disables double buffering.
Access Mode	Byte or word in I/O Space. Byte or word in ID Space.
Wait States	Zero.
Transfer Rate	8 Mbytes/second maximum, continuous.
Onboard Options	All options are software programmable.
Dimensions	Standard Single High IndustryPack width and length. 1.8 x 3.9 inches.
Construction	Conformal Coated FR4 4 layer Printed Circuit. Surface mounted components.
Temperature Coefficient	0.89 W/°C for uniform heat across IP.
Power Requirements	+5.0 VDC, 50mA typical.