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Zefeer

Hardware Manual

Zefeer Hardware Manual

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Contents

Common Technical Data

CPU	ARM9 (920T core) @166 (model DZA) or 200 MHz (DZB, DZG, DZN, and DZQ) with MMU
CPU supervision	
PSU supervisors	Core and I/O power supply separate supervision
Watchdog	1
DMA	12 internal
Digital ID	unique 32 bit
Memory	
Cache	16K cache for instructions +16K cache for data
SDRAM	from 16MBytes to 128MBytes (16-bit access in DZA and DZB only)
Flash NOR	4 MBytes (2M x 16bit) to 64 MBytes (32M x 16bit) ; access is at 16-bit;
EEPROM	internal 16 kbit
Interfaces (to the connector)	
Ethernet PHY	1/10/100Mbps ready for magnetics
UART	16550 compatible; IrDA on UART nr.2, HDLC on UART nr. 3 when existing
SPI	1 channel
AC97	2 channels
I^2S	6 channels
Timers	two general purpose 16-bit, one general purpose 32-bit, one 40-bit debug timer
External Bus	8/16-bit byte - 29 Address Bits -5 direct Chip Select
I/O Controller	yes (see model specs)
Debug	JTAG IEEE 1149.1 Test Access Port
Interrupts	up to 54
Other features	
RTC & Watchdog (Optional)	Dallas DS1374U-33+ On-board, I2C RTC device, pin for battery backup available on connector)
Mechanical	
Phisical	68,58 x 50,80 x 1,00 mm^3 (2,7"x 2,0"), with fixing holes
Connectors	2 x 140 pins 0.6mm pitch, gold-plated contacts
Compatibility	Hirose FX8C-140S-SV
PCB	6 (DZA/B) to 8 layers
Material	FR4
Technology	double-sided SMT
Temperature	0÷70 °C (-40÷85 °C available) operational temperature
PSU	
Single 3.3V± 5%	Through connector; 1.8V regulated on-board
Consumption	Around 0.5A worst case
Software	
RTOS	eCos (Order Code **ZECK**)
Multitasking OS	Linux 2.6.XX (Order Code **ZELK**)
Multitasking OS	Windows CE.net (Order Code **ZWCK**)
Agency approvals	
CE Mark	CE Mark (EN 55022, EN 61000-4-3, EN 61000-4-4, EN 61000-4-6)

1 - Introduction

ATTENTION! FOR ALL USER IN POSSES OF Zefeer Embedded Linux kit:

Zefeer Embedded Linux Kit 1.5.0 supports two new modules (DZQ3610x3 or DZQ3610x4). It is strongly recommended the reading of "AN-ZELK-009 Migrating to ZELK 1.5.0" that details the differences with respect to the previous modules.

ATTENTION! Starting from Zefeer-hm version 1.2.0, new zefeer modules are available. Such models have new features: RTC/WDT device integrated, new type of flash memories as P30, etc. It's stronlgy recommended to read the following section:5.2, 5.5, 9,10.

Zefeer is a General Purpose microprocessor CPU board powered by EP93XX ARM920T family processors from Cirrus Logic. Its compact form factor and easy-of-use concept make them suitable for uses in Industrial Controls, Digital Media Servers, Home Media Gateways, Digital Audio Jukeboxes, Streaming Audio Players, Set-Top Boxes, Point-of-Sale Terminals, Kiosks, Biometric Security Systems, GPS Systems, Consumer Electronic Applications.

Zefeer modules come with all essential features needed in order to quickly set up a customized system based on this processor. All Zefeer modules are provided with SDRAM, Flash, CPU supervisor and Ethernet MAC+PHY on board. External bus interface at 16/32 bits (depending on models), AC97, I2S, SPI, JTAG, timers, UARTs, USBs, IrDA and GPIOs are common to all Zefeer family as explained in the Technical Data.

All interface signals are passed through two 140 pin 0.6mm pitch stacking connectors, therefore users should complete hardware interfaces and connectors when they want to use them through the host board.
A full overview of the board is given, both from mechanical and electrical point of view. Nevertheless, for detailed information, user should refer to components manufacturer's data sheet.

Zefeer linecard supports both Linux and WindowsCE.net OS as well as eCos. Other related documents are the Zefeer Embedded Linux Kit (ZELK), Zefeer eCos Kit (ZELK), Zefeer Windows CE Kit (ZWCK) and Zefeer EVB Evaluation Board User Manual (see chapter 14 for references).
Table below summarizes main characteristics of off-the-shelf modules.

In order to know the specific features and optionals of your Zefeer module, or for order codes please, refer to Order Codes Section 10, page 44.

	Module name (Standard models)				
	DZA 4100C(x)	DZB 4100C(x)	DZG 8600C(y)	DZN 3600C(y)	DZQ 3600C(y)
CPU	EP9301	EP9302	EP9307	EP9312	EP9315
CPU frequency[MHz]	166	200	200	200	200
Bus frequency [MHz]	66	100	100	100	100
Flash [MB]	4	4	8	32	32
SDRAM [MB]	16*	16*	64	64	64
UARTs (max)	2	2	3	3	3
Audio engine and floating point coprocessor		Y	Y	Y	Y
PCMCIA					Y
IDE controller				Y	Y
USB host ports	2	2	3	3	3
LCD controller			Y	Y	Y
Graphic engine			Y		Y
Touch screen or ADC	5 ADC	5 ADC	8 wire	8 wire	8 wire
RTC&WDG DS1374 onboard	-	-	Only for y=4	Only for y=4	Only for y=4

* access to the SDRAM is performed at 16 bit.

- Extended temperature range is also available. Customizations and adaptations are also possible. Informations are subject to change. Informations may be not complete due to the need to condensate many informations in one table. In order to have a detailed information about each module, please contact sales department.

2 - Specifications

These specifications refer to available models. Some of them are considered part of the “standard” production. For customizations and details, please contact your distributor and see also Chapter 10.

CPU	Cirrus Logic EP93xx
Speed	166 (model DZA), or 200 MHz
Flash	4/8/16/32 MBytes
RAM	16/32/64/128 MBytes
EEPROM	16Kbit
Reset	External and CPU supervisor with Master Reset input
Power supply	3.3V and 1.8V supply regulated on board
Power consumption	typical < 1.7 W
Weight	20 g
Dimensions	67.5 x 50.8 mm^2 [2.7 x 2.0 inches]
Connectors	Hirose FX8C-140S-SV
Mating connectors	Hirose FX8C-140P-SV (5 mm board-to-board height) Hirose FX8C-140P-SV1 (6 mm board-to-board height) Hirose FX8C-140P-SV2 (7 mm board-to-board height) Hirose FX8C-140P-SV4 (9 mm board-to-board height) Hirose FX8C-140P-SV6 (11 mm board-to-board height)

3 - Board layout and Physical

Zefeer has been designed to fit on a 68.5 x 50.8 mm^2 (2 x 2.7 inches) module.

All Zefeer modules have the same footprint. Some DZA models (see Section 10, page 44) may have just one connector and a hole for fixing. Ask support for further informations.

Users should consider that mechanical tolerances are within $\pm$ 0.10 mm.

In Fig. 1 (**BOTTOM VIEW**) the pin 1 of J1 and J2 is marked by an arrow.

Others Mechanical drawings are available on request.

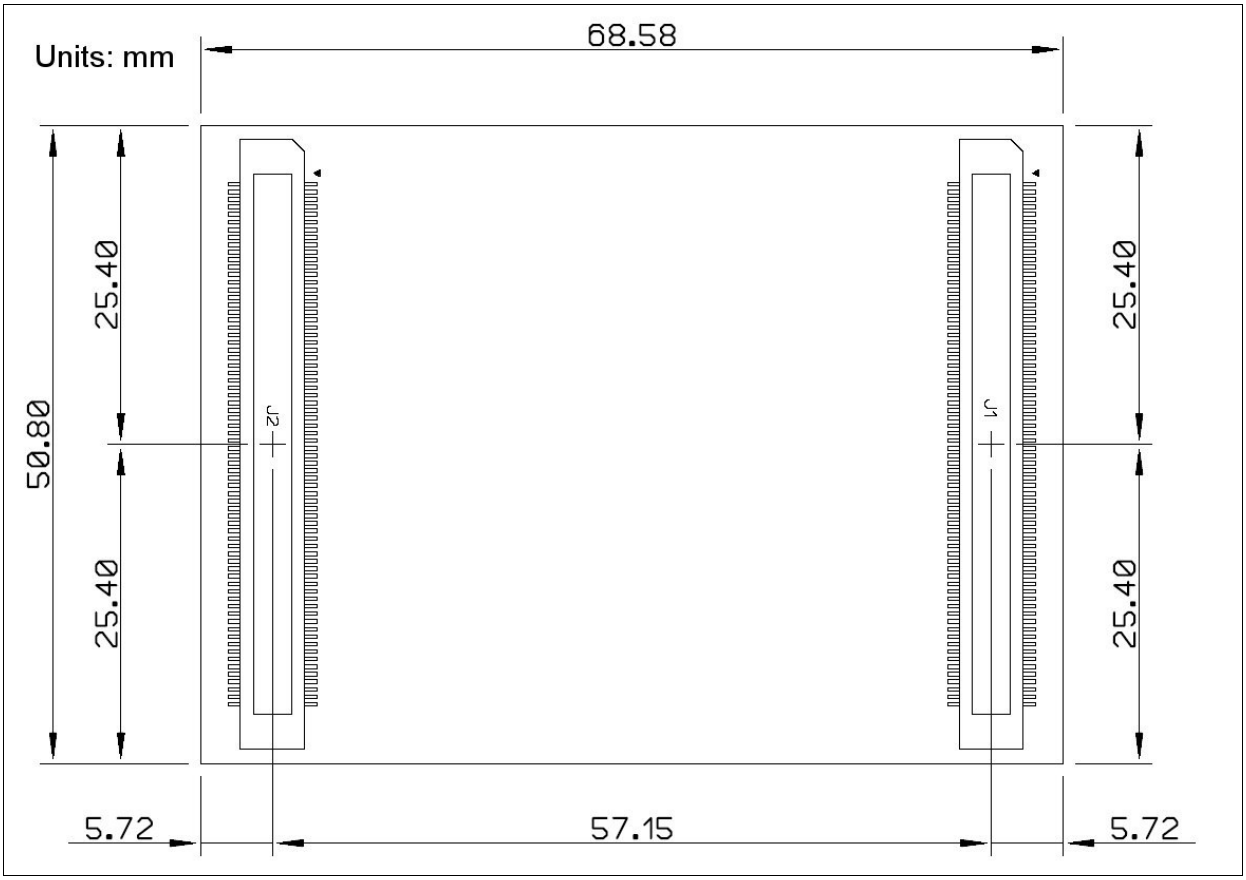

Fig. 1 – Zefeer board mechanical layout (BOTTOM VIEW)

4 - Interfaces and pinout

All connections are carried over the connectors J1 and J2. In following tables, all interfaces for modules DZA, DZB, DZN and DZQ have been reported. Names of the signals often remind the names of the microprocessor signals, if they are connected to the microprocessor itself. Main function only is indicated in the tables below under the column “name”, being several pins available for multiple purposes. In order to know in detail which pins can be used with an alternate function, user should refer to the Data Sheet of the microprocessor manufacturer. Also detailed electrical specifications (levels, tolerances, timings and so on) must be verified on official document released by manufacturer.

Please, take note that Addresses and Data relative to the Peripheral Bus are annotated with the convention that the zeroed bit is always the Least Significant Bit. That is D0 is the LSB of the Data and A0 is the LSB of the Addresses.

As a doublecheck, you can verify where the pin is connected to the microprocessor, by looking at the second column (uP pin).

n.c. means that a pin is not used. Leave this pin vacant during regular operations.

d.c. means that this pin must be left unconnected.

In case UART’s signals (as RXD0 , TXD0) will be used without RS232 transceiver or are not used it’s strong recommended to pull-up these signals. These good practice can avoid some undesirable behaviour of the board[1].

ATTENTION! **In the following table J1 connector pinout change slightly in dependence by specific zefeer model. In particular for DZG. DZN and DZQ, some models can mount or “Intel P30” nor flash either “Intel J3” nor flash and can integrates RTC DS1374 on-board. So J1 conn. pinout presents some minimal differences. Such differences on pinout are explained in the following table for different order codes and are reported in red colour .** For example in Section 4.3 at page 28 with refer to DZN/DZQ pinout, pin 9 is “SDWEN” for all modules that have a marking code analogue to “DZxxxxxx1” that means all valid order codes that have the last digit equals to “1” (DZN3600C1, DZQ8300I1 and so on), while pin 9 is “DNU” for all modules that have a code analogue to “DZxxxxxx3” that means all modules that have the last digits eqauls to “1” (DZQ3610C3, DZQ3610I3, DZN8600I3, and so on). For further information about order code structure, please refer to section10.

[1] If you have a development kit, please refer to the software manual for further details about this problem.

4.1 DZA/DZB pinout

Pin	*uP pin*	*name*	*DZA & DZB J1 ODD 1-69 (1/8)*
1		GND	Ground reference
3		GND	Ground reference
5		n.c.	
7		n.c.	
9	14	SDWEn	SDRAM write enable out
11	21	RASn	SDRAM RAS out
13		GND	Ground reference
15	208	SDCLKEN	SDRAM clock enable out
17		n.c	
19		n.c.	
21		n.c	
23		n.c.	
25		n.c	
27		n.c.	
29		n.c.	
31		n.c.	
33		n.c.	
35		GND	Ground reference
37		n.c.	
39		n.c.	
41		n.c.	
43	132	ADC3	External Analog Measurement Input
45	134	ADC1	External Analog Measurement Input
47		n.c.	
49		n.c.	
51		n.c.	
53		n.c.	
55		n.c.	
57		n.c.	
59		n.c.	
61		n.c.	
63		GND	Ground reference
65		n.c.	
67		n.c.	
69		n.c.	

Pin	uP pin	name	DZA & DZB J1 ODD 71-139 (2/8)
71		n.c.	
73	202	HGPIO5	General purpose I/O
75	201	HGPIO4	General purpose I/O
77	200	HGPIO3	General purpose I/O
79	199	HGPIO2	General purpose I/O
81		n.c.	
83		n.c.	
85		n.c.	
87		n.c.	
89		GND	Ground reference
91		n.c.	
93		n.c.	
95		n.c.	
97		n.c.	
99		n.c.	
101		n.c.	
103		n.c.	
105		n.c.	
107		n.c.	
109		n.c.	
111		n.c.	
113		GND	Ground reference
115		n.c.	
117		n.c.	
119		n.c.	
121		n.c.	
123		n.c.	
125		n.c.	
127		n.c.	
129		n.c.	
131		n.c.	
133		n.c.	
135		n.c.	
137		n.c.	
139		GND	Ground reference

Pin	uP pin	name	DZA & DZB J1 EVEN 2-70 (3/8)
2		GND	Ground reference
4		GND	Ground reference
6		n.c.	
8		n.c.	
10	22	CASn	SDRAM CAS out
12	10	SDCLK	SDRAM clock out
14	16	SDCSn2	SDRAM chip selects out
16	18	SDCSn0	SDRAM chip selects out
18		n.c.	
20		n.c.	
22		n.c.	
24		n.c.	
26		n.c.	
28		GND	Ground reference
30		n.c.	
32		n.c.	
34		n.c.	
36		n.c.	
38		n.c.	
40		ADC4	External Analog Measurement Input
42		ADC2	External Analog Measurement Input
44		ADC0	External Analog Measurement Input
46		n.c.	
48		n.c.	
50		n.c.	
52		GND	Ground reference
54		n.c.	
56		n.c.	
58		n.c.	
60		n.c.	
62		n.c.	
64		n.c.	
66		n.c.	
68		n.c.	
70		n.c.	

Pin	uP pin	name	DZA & DZB J1 EVEN 72-140 (4/8)
72	115	CGPIO0	General purpose I/O
74	168	FGPIO3	General purpose I/O
76		GND	Ground reference
78	169	FGPIO2	General purpose I/O
80	170	FGPIO1	General purpose I/O
82		n.c.	
84		n.c.	
86		n.c.	
88		n.c.	
90		LCSn6	Boot configuration pin active during reset. By default it is pulled up with a 10 kΩ resistor. See 5.4 for details.
92		n.c.	
94		n.c.	
96		n.c.	
98		n.c.	
100		GND	Ground reference
102		n.c.	
104		n.c.	
106		n.c.	
108		n.c.	
110		n.c.	
112		n.c.	
114		n.c.	
116		n.c.	
118		n.c.	
120		n.c.	
122		n.c.	
124		n.c.	
126		GND	Ground reference
128		n.c.	
130		n.c.	
132		n.c.	
134		n.c.	
136		n.c.	
138		n.c.	
140		GND	Ground reference

Pin	uP pin	name	DZA & DZB J2 ODD 1-69 (5/8)
1		3V3	Power supply (3.3V)
3		GND	Ground reference
5	74	D0	Share Data bus in/out
7	70	D2	Share Data bus in/out
9	64	D4	Share Data bus in/out
11	60	D6	Share Data bus in/out
13	47	D8	Share Data bus in/out
15	43	D10	Share Data bus in/out
17	37	D12	Share Data bus in/out
19	31	D14	Share Data bus in/out
21	48	A0	Share Address bus out
23	44	A2	Share Address bus out
25	38	A4	Share Address bus out
27	32	A6	Share Address bus out
29	73	A8	Share Address bus out
31	69	A10	Share Address bus out
33	63	A12	Share Address bus out
35		3V3	Power supply (3.3V)
37		GND	Ground reference
39	59	A14	Share Address bus out
41	195	A16	Share Address bus out
43	205	A18	Share Address bus out
45	207	A20	Share Address bus out
47	25	A22	Share Address bus out
49	9	A24	Share Address bus out
51		d.c.	Leave unconnected
53	4	CSn2	Chip select out **- internal pull-up (10 kΩ)**
55	2	CSn6	Chip select out **- internal pull-up (10 kΩ)**
57		WEn	SRAM write strobe out
59	103	INT0	External interrupts
61		n.c.	External interrupts
63	89	ASYNC	AC97 frame sync
65		3V3	Power supply (3.3V)
67		GND	Ground reference
69	93	SCLK1	SPI bit clock

Pin	uP pin	name	DZA & DZB J2 ODD 71 –139 (6/8)
71	154	ARSTn	AC97 reset output
73	94	SFRM1	SPI frame clock output
75	153	EGPIO0	Enhanced GPIO
77	151	EGPIO2	Enhanced GPIO
79	147	EGPIO4	Enhanced GPIO
81	145	EGPIO6	Enhanced GPIO
83	143	EGPIO8	Enhanced GPIO
85	141	EGPIO10	Enhanced GPIO
87	165	EGPIO12	Enhanced GPIO
89	163	EGPIO14	Enhanced GPIO
91	124	RSTn	User Reset (open drain)
93		RLED	Red LED
95		LBOOT0	Boot configuration pin active during reset. By default it is pulled down with a 10 kΩ resistor. See 5.4 for details.
97		n.c.	
99		n.c.	
101		3V3	Power supply (3.3V)
103		GND	Ground reference
105		TDI	JTAG data in
107		TMS	JTAG test mode select
109	125	PORSTn	Power on reset input (active low)
111		LED4	LED signal from LAN PHY.
113		LED3	LED signal from LAN PHY.
115		LED2	LED signal from LAN PHY.
117		LED1	LED signal from LAN PHY.
119		LED0	LED signal from LAN PHY.
121	113	TXD0	Transmit out UART1
123	104	RTS0n	Ready to send UART1
125	75	DSR0n	Data set ready UART1
127		CTTD	Reference for Tx wiring central tap. Connect as in 5.3
129		ETH TX -	Transmit - differential signal to Xformer. Connect as in 5.3
131		ETH TX +	Transmit + differential signal to Xformer. Connect as in 5.3
133		ETH RX +	Receive + differential signal to Xformer. Connect as in 5.3
135		ETH RX -	Receive - differential signal to Xformer. Connect as in 5.3
137		CTRD	Reference for Rx wiring central tap. Connect as in 5.3
139		GND	Ground reference

Pin	uP pin	name	DZA & DZB J2 EVEN 2-70 (7/8)
2		GND	Ground reference
4	72	D1	Shared Data bus in/out
6	68	D3	Shared Data bus in/out
8	62	D5	Shared Data bus in/out
10	56	D7	Shared Data bus in/out
12	45	D9	Shared Data bus in/out
14	39	D11	Shared Data bus in/out
16	33	D13	Shared Data bus in/out
18	29	D15	Shared Data bus in/out
20		GND	Ground reference
22	46	A1	Share Address bus out
24	40	A3	Share Address bus out
26	36	A5	Share Address bus out
28	30	A7	Share Address bus out
30	71	A9	Share Address bus out
32	65	A11	Share Address bus out
34	61	A13	Share Address bus out
36	55	A15	Share Address bus out
38	196	A17	Share Address bus out
40	206	A19	Share Address bus out
42	26	A21	Share Address bus out
44	11	A23	Share Address bus out
46	6	A25	Share Address bus out
48	5	CSn1	Chip select out **- internal pull-up (10 kΩ)**
50	3	CSn3	Chip select out **- internal pull-up (10 kΩ)**
52	1	CSn7	Chip select out **- internal pull-up (10 kΩ)**
54		GND	Ground reference
56		RDn	SRAM read active low
58	24	DQMn0	Shared data mask out active low
60	23	DQMn1	Shared data mask out active low
62		WAITn	SRAM Wait in active low
64	102	INT1	External interrupt
66	101	INT3	External interrupt
68		ABITCLK	AC97 bit clock
70		ASDI	AC97 primary input

Pin	uP pin	name	DZA & DZB J2 EVEN 72-140 (8/8)
72		SSPRX1	SPI Input
74		ASDO	AC97 output
76		SSPTX1	SPI output
78	152	EGPIO1	Enhanced GPIO
80	148	EGPIO3	Enhanced GPIO
82		GND	Ground reference
84	146	EGPIO5	Enhanced GPIO
86	144	EGPIO7	Enhanced GPIO
88	142	EGPIO9	Enhanced GPIO
90	140	EGPIO11	Enhanced GPIO
92	164	EGPIO13	Enhanced GPIO
94	160	EGPIO15	Enhanced GPIO
96	79	TD0	JTAG data out
98	77	TCK	JTAG clock in
100	155	TRSTn	JTAG reset
102		MRSTn	Master reset input (open drain) normally pulled up. See 5.2 for details.
104	97	GLED	Green LED
106	87	EECLK	EEPROM / Two – wire Interface clock
108	88	EEDAT	EEPROM / Two – wire Interface data
110		LEECLK	Boot configuration pin active during reset. By default it is pulled up with a 10 kΩ resistor. See 5.4for details.
112		LASDO	Boot configuration pin active during reset. By default it is pulled udown with a 10 kΩ resistor. See 5.4for details.
114		nWc	Write protection signal (active low) of the EEPROM. Normally it is pulled low and writing is allowed. Pull it high to protect data.
116		GND	Ground reference
118		LCSn7	Boot configuration pin active during reset. By default it is pulled down with a 10 kΩ resistor. See 5.4for details.
120	114	TXD1	Transmit / IrDA output
122	110	RXD1	Receive / IrDA input
124	106	USBP0	USB positive signals
126	158	USBP2	USB positive signals
128	109	RXD0	Receive in
130	108	CTS0n	Clear to send UART1
132	76	DTR0n	Data terminal ready output UART1
134	105	USBM0	USB negative signals
136	157	USBM2	USB negative signals
138		3V3	Power supply (3.3V)
140		GND	Ground reference

4.2 DZG pinout

Pin	uP pin	name	DZG J1 ODD 1-69 (1/8)
1		GND	Ground reference
3		GND	Ground reference
5	X	USBM1	
7	X	RXD2	
9 (DZxxxxxx0) (DZxxxxxx1)	**G3**	**SDWEn**	**SDRAM write enable out**
9 (DZxxxxxx3)	**-**	**DNU**	**Do Not connect**
9 (DZxxxxxx4)		**VBACK**	**Vbackup pin on DS1374 RTC device. Connect a 3V Battery. (See section 9) ((Dzxxxxxx4) have DS1374 on- board)**
11 (DZxxxxxx0) (DZxxxxxx1)	**H3**	**RASn**	**SDRAM RAS out**
11 (DZxxxxxx3)	**-**	**DNU**	**Do not connect**
11 (DZxxxxxx4)	**-**	**RTC_INT**	**RTC Interrupt output pin that DS1374 can generate upon alarm or wathcdog event. ((Dzxxxxxx4) have DS1374 on- board) (See section 9)**
13		GND	
15	X	SDCLKEN	
17	X	n.c	
19	X	DQMn2	
21	X	D31	
23	X	D29	
25	X	D27	
27	X	D25	
29	X	D23	
31	X	D21	
33	X	D19	
35		GND	
37	X	D17	
39		TOUCHXp	
41		TOUCHXm	
43		TOUCHYp	
45		TOUCHYm	
47	X	P17	
49	X	P15	
51	X	P13	

53	X	P11	
55	X	P9	
57	X	P7	
59	X	P5	
61	X	P3	
63		GND	
65	X	P1	
67	X	BRIGHT	
69		VSYNCFP	

Pin	*uP pin*	*name*	*DZG J1 ODD 71-139 (2/8)*
71		SPCLK	
73	X	ROW7	
75	X	ROW5	
77	X	ROW3	
79	X	ROW1	
81	X	COL7	
83	X	COL5	
85	X	COL3	
87	X	COL1	
89		GND	
91		n.c.	
93		n.c.	
95		n.c.	
97		n.c.	
99		n.c.	
101		n.c.	
103		n.c.	
105		n.c.	
107		n.c.	
109		n.c.	
111		n.c.	
113		GND	
115		n.c.	
117		n.c.	
119		n.c.	
121		n.c.	
123		n.c.	
125		n.c.	
127		n.c.	
129		n.c.	
131		n.c.	
133		n.c.	
135		n.c.	
137		n.c.	
139		GND	

Pin	uP pin	name	DZG J1 EVEN 2-70 (3/8)
2		GND	
4		GND	
6	X	USBP1	
8	X	TXD2	
10 (DZxxxxxx1)	**x**	**CASn**	**SDRAM CAS out**
10 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
12 (DZxxxxxx1)	**x**	**SDCLK**	**SDRAM clock out**
12 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
14 (DZxxxxxx1)	**x**	**SDCSn2**	**SDRAM chip selects out**
14 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
16	x	SDCSn0	SDRAM chip selects out
18	x	DQMn3	Shared data mask out
20	x	D30	Shared Data bus in/out
22	X	D28	
24	X	D26	
26	X	D24	
28		GND	
30	X	D22	
32	X	D20	
34	X	D18	
36	X	D16	
38	X	TOUCH SXp	
40		TOUCH SXm	
42		TOUCH SYm	
44		TOUCH SYp	
46	X	P16	
48	X	P14	
50	X	P12	
52		GND	
54	X	P10	
56	X	P8	
58	X	P6	
60	X	P4	
62	X	P2	
64	X	P0	

66	X	BLANK	
68	X	HSYNCLP	
70	X	PWMOUT	

Pin	*uP pin*	*name*	*DZG J1 EVEN 72-140 (4/8)*
72	X	ROW6	
74	X	ROW4	
76		GND	
78	X	ROW2	
80	X	ROW0	
82	X	COL6	
84	X	COL4	
86	X	COL2	
88	X	COL0	
90		LCSn6	Boot configuration pin active during reset. By default it is pulled up with a 10 kΩ resistor. See 5.4 for details.
92		n.c.	
94	X	GGPIO2	
96		n.c.	
98		n.c.	
100		GND	
102		n.c.	
104	X	FGPIO0	
106		n.c.	
108	X	HGPIO2	
110	X	HGPIO3	
112	X	HGPIO4	
114	X	HGPIO5	
116	X	HGPIO6	
118	X	HGPIO7	
120		n.c.	
122		n.c.	
124		n.c.	
126		GND	
128		n.c.	
130	X	FGPIO0	
132	X	FGPIO5	
134	X	FGPIO7	
136		n.c.	
138		n.c.	
140		GND	

Pin	*uP pin*	*name*	*DZG J2 ODD 1-69 (5/8)*
1		3V3	
3		GND	Ground reference
5	X	D0	
7	X	D2	
9	X	D4	
11	X	D6	
13	X	D8	
15	X	D10	
17	X	D12	
19	X	D14	
21	X	A0	
23	X	A2	
25	X	A4	
27	X	A6	
29	X	A8	
31	X	A10	
33	X	A12	
35		3V3	
37		GND	
39	X	A14	
41	X	A16	
43	X	A18	
45	X	A20	
47	X	A22	
49	X	A24	
51		d.c.	Leave unconnected
53	X	CSn2	Chip select out **- internal pull-up (10 kΩ)**
55	X	CSn6	Chip select out **- internal pull-up (10 kΩ)**
57		WEn	
59	X	INT0	
61	X	INT2	
63		ASYNC	
65		3V3	
67		GND	
69		SCLK1	

Pin	uP pin	name	DZG J2 ODD 71 –139 (6/8)
71		ARSTn	
73		SFRM1	
75	X	EGPIO0	
77	X	EGPIO2	
79	X	EGPIO4	
81	X	EGPIO6	
83	X	EGPIO8	
85	X	EGPIO10	
87	X	EGPIO12	
89		n.c.	
91	X	RSTn	
93		RLED	
95		LBOOT0	
97		n.c.	
99		SLA0	
101		3V3	
103		GND	
105		TDI	
107		TMS	
109	H15	PORSTn	
111		LED4	
113		LED3	
115		LED2	
117		LED1	
119		LED0	
121	X	TXD0	
123	X	RTS0n	
125	X	DSR0n	
127		CTTD	
129		ETH TX -	
131		ETH TX +	
133		ETH RX +	
135		ETH RX -	
137		CTRD	
139		GND	

Pin	*uP pin*	*name*	*DZG J2 EVEN 2-70 (7/8)*
2		GND	
4	X	D1	
6	X	D3	
8	X	D5	
10	X	D7	
12	X	D9	
14	X	D11	
16	X	D13	
18	X	D15	
20		GND	
22	X	A1	
24	X	A3	
26	X	A5	
28	X	A7	
30	X	A9	
32	X	A11	
34	X	A13	
36	X	A15	
38	X	A17	
40	X	A19	
42	X	A21	
44	X	A23	
46	X	A25	
48	X	CSn1	Chip select out **- internal pull-up (10 kΩ)**
50	X	CSn3	Chip select out **- internal pull-up (10 kΩ)**
52	X	CSn7	Chip select out **- internal pull-up (10 kΩ)**
54		GND	
56		RDn	
58	X	DQMn0	
60	X	DQMn1	
62		WAITn	
64	X	INT1	
66		n.c.	
68		ABITCLK	
70		ASDI	

Pin	uP pin	name	DZG J2 EVEN 72-140 (8/8)
72		SSPRX1	
74		ASDO	
76		SSPTX1	
78	X	EGPIO1	
80	X	EGPIO3	
82		GND	
84	X	EGPIO5	
86	X	EGPIO7	
88	X	EGPIO9	
90	X	EGPIO11	
92	X	EGPIO13	
94	X	EGPIO15	
96	X	TD0	
98	X	TCK	
100	X	TRSTn	
102		MRSTn	
104	X	GLED	
106	X	EECLK	
108	X	EEDAT	
110		LEECLK	
112		LASDO	
114		Nwc	
116		GND	
118		LCSn7	
120	X	TXD1	
122	X	RXD1	
124	X	USBP0	
126	X	USBP2	
128	X	RXD0	
130	X	CTS0n	
132	X	DTR0n	
134	X	USBM0	
136	X	USBM2	
138		3V3	
140		GND	

4.3 DZN and DZQ

Pin	uP pin	name	DZN & DZQ J1 ODD 1-69 (1/8)
1		GND	Ground reference
3		GND	Ground reference
5	T16	USBM1	USB1 negative signals
7	W20	RXD2	Receive
9 (DZxxxxxx0) (DZxxxxxx1)	**G3**	**SDWEn**	**SDRAM write enable out**
9 (DZxxxxxx3)	**-**	**DNU**	**Do Not connect**
9 (DZxxxxxx4)		**VBACK**	**Vbackup pin on DS1374 RTC device. Available for attach a 3V Battery.**
11 (DZxxxxxx0) (DZxxxxxx1)	**H3**	**RASn**	**SDRAM RAS out**
11 (DZxxxxxx3)	**-**	**DNU**	**Do not connect**
11 (DZxxxxxx4)	**-**	**RTC_INT**	**RTC Interrupt output pin that DS1374 can generate upon alarm or watchdog event. ((Dzxxxxxx4) have DS1374 on- board)**
13		GND	Ground reference
15	D4	SDCLKEN	SDRAM clock enable out
17	G2	n.c	
19	J4	DQMn2	Shared data mask out
21	B2	D31	Share Data bus in/out
23	C4	D29	Share Data bus in/out
25	B4	D27	Share Data bus in/out
27	D2	D25	Share Data bus in/out
29	E2	D23	Share Data bus in/out
31	J1	D21	Share Data bus in/out
33	K4	D19	Share Data bus in/out
35		GND	Ground reference
37	L2	D17	Share Data bus in/out
39	H20	TOUCHXp	Touchscreen ADC X axis
41	J18	TOUCHXm	Touchscreen ADC X axis
43	J19	TOUCHYp	Touchscreen ADC Y axis
45	J20	TOUCHYm	Touchscreen ADC Y axis
47	R3	P17	Pixel databus out
49	U2	P15	Pixel databus out

51	T3	P13	Pixel databus out
53	V2	P11	Pixel databus out
55	W 2	P9	Pixel databus out
57	U4	P7	Pixel databus out
59	W 4	P5	Pixel databus out
61	W 5	P3	Pixel databus out
63		GND	Ground reference
65	V6	P1	Pixel databus out
67	P4	BRIGHT	PWM brightness control out
69	T5	VSYNCFP	Vertical or composite synchronization/frame pulse out

Pin	***uP pin***	***name***	***DZN & DZQ J1 ODD 71-139 (2/8)***
71	T4	SPCLK	Pixel clock in/out
73	P20	ROW7	Key matrix row outputs
75	R20	ROW5	Key matrix row outputs
77	R18	ROW3	Key matrix row outputs
79	U20	ROW1	Key matrix row outputs
81	L18	COL7	Key matrix column inputs
83	L17	COL5	Key matrix column inputs
85	M18	COL3	Key matrix column inputs
87	N19	COL1	Key matrix column inputs
89		GND	Ground reference
91	V4	DIDE15	IDE data bus **– internal series terminated with a 33 Ω resistor**
93	V5	DIDE13	IDE data bus **– internal series terminated with a 33 Ω resistor**
95	D3	DIDE11	IDE data bus **– internal series terminated with a 33 Ω resistor**
97	D6	DIDE9	IDE data bus **– internal series terminated with a 33 Ω resistor**
99	B5	DIDE7	IDE data bus **– internal series terminated with a 33 Ω resistor**
101	D7	DIDE5	IDE data bus **– internal series terminated with a 33 Ω resistor**
103	B6	DIDE3	IDE data bus **– internal series terminated with a 33 Ω resistor**
105	Y2	DIDE1	IDE data bus **– internal series terminated with a 33 Ω resistor**
107	C20	DMACKn	IDE DMA acknowledge output **– internal series terminated with a 33 Ω resistor**
109	C19	IORDY	IDE ready input **– internal series terminated with a 82 Ω resistor**
111	E17	DIOWn	IDE Write strobe output **– internal series terminated with a 33 Ω resistor**
113		GND	Ground reference
115	D19	DIORn	IDE Read strobe output **– internal series terminated with a 33 Ω resistor**
117	X (DZQ)	MCRESETn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
119	X (DZQ)	MCWRn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**

121	X (DZQ)	MCRDn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
123	X (DZQ)	IOWRn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
125	X (DZQ)	IORDn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
127	X (DZQ)	MCELn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
129	X (DZQ)	MCEHn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
131	X (DZQ)	MCREGn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
133	X (DZQ)	MCADENn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
135	X (DZQ)	MCDAENn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
137	X (DZQ)	MCDIR	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
139		GND	Ground reference

Pin	uP pin	name	DZN & DZQ J1 EVEN 2-70 (3/8)
2		GND	Ground reference
4		GND	Ground reference
6	Y19	USBP1	USB1 positive signals
8	T18	TXD2	Transmit
10 (DZxxxxxx1)	**H2**	**CASn**	**SDRAM CAS out**
10 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
12 (DZxxxxxx1)	**G4**	**SDCLK**	**SDRAM clock out**
12 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
14 (DZxxxxxx1)	**H4**	**SDCSn2**	**SDRAM chip selects out**
14 (Dzxxx0xx3) (Dzxxx1xxx)	**-**	**DNU**	**Do not connect. Reserved for future use.**
16	G1	SDCSn0	SDRAM chip selects out
18	H1	DQMn3	Shared data mask out
20	B3	D30	Shared Data bus in/out
22	A2	D28	Shared Data bus in/out
24	E3	D26	Shared Data bus in/out
26	F3	D24	Shared Data bus in/out
28		GND	Ground reference
30	F2	D22	Shared Data bus in/out
32	K2	D20	Shared Data bus in/out
34	L1	D18	Shared Data bus in/out
36	L3	D16	Shared Data bus in/out
38	K20	TOUCH SXp	Touchscreen ADC X axis feedback
40	K19	TOUCH SXm	Touchscreen ADC X axis feedback
42	K17	TOUCH SYm	Touchscreen ADC Y axis feedback
44	K18	TOUCH SYp	Touchscreen ADC Y axis feedback
46	V1	P16	Pixel data bus out
48	R4	P14	Pixel data bus out
50	W1	P12	Pixel data bus out
52		GND	Ground reference
54	U3	P10	Pixel data bus out
56	V3	P8	Pixel data bus out
58	U5	P6	Pixel data bus out
60	U6	P4	Pixel data bus out
62	Y4	P2	Pixel data bus out
64	U7	P0	Pixel data bus out
66	T2	BLANK	Pixel data bus out
68	Y1	HSYNCLP	Horizontal synchronization – line pulse
70	U16	PWMOUT	Pulse width modulator out

Pin	uP pin	name	DZN & DZQ J1 EVEN 72-140 (4/8)
72	P19	ROW6	Key matrix row outputs
74	T20	ROW4	Key matrix row outputs
76		GND	Ground reference
78	T19	ROW2	Key matrix row outputs
80	R17	ROW0	Key matrix row outputs
82	M19	COL6	Key matrix column inputs
84	M17	COL4	Key matrix column inputs
86	N20	COL2	Key matrix column inputs
88	N18	COL0	Key matrix column inputs
90		LCSn6	Boot configuration pin active during reset. By default it is pulled up with a 10 kΩ resistor. See 5.4 for details.
92	T6	DIDE14	IDE data bus **– internal series terminated with a 33 Ω resistor**
94	Y3	DIDE12	IDE data bus **– internal series terminated with a 33 Ω resistor**
96	C5	DIDE10	IDE data bus **– internal series terminated with a 33 Ω resistor**
98	A4	DIDE8	IDE data bus **– internal series terminated with a 33 Ω resistor**
100		GND	Ground reference
102	C6	DIDE6	IDE data bus **– internal series terminated with a 33 Ω resistor**
104	A5	DIDE4	IDE data bus **– internal series terminated with a 33 Ω resistor**
106	C7	DIDE2	IDE data bus **– internal series terminated with a 33 Ω resistor**
108	W3	DIDE0	IDE data bus **– internal series terminated with a 33 Ω resistor**
110	W10	IDECSn1	IDE data bus **– internal series terminated with a 33 Ω resistor**
112	V10	IDECSn0	IDE data bus **– internal series terminated with a 33 Ω resistor**
114	V11	AIDE2	IDE data bus **– internal series terminated with a 33 Ω resistor**
116	W11	AIDE1	IDE data bus **– internal series terminated with a 33 Ω resistor**
118	Y11	AIDE0	IDE data bus **– internal series terminated with a 33 Ω resistor**
120	X (DZQ)	MCWAITn	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
122	X (DZQ)	WP	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
124	X (DZQ)	READY	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
126		GND	Ground reference
128	X (DZQ)	MCBVD2	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
130	X (DZQ)	MCBVD1	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
132	X (DZQ)	MCD2	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
134	X (DZQ)	MCD1	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
136	X (DZQ)	VS2	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
138	X (DZQ)	VS1	PCMCIA - **DZQ signal only. In DZN this pin is a n.c.pin.**
140		GND	Ground reference

Pin	*uP pin*	*name*	*DZN & DZQ J2 ODD 1-69 (5/8)*
1		3V3	Power supply (3.3V)
3		GND	Ground reference
5	U10	D0	Share Data bus in/out
7	V9	D2	Share Data bus in/out
9	Y7	D4	Share Data bus in/out
11	Y6	D6	Share Data bus in/out
13	T1	D8	Share Data bus in/out
15	P2	D10	Share Data bus in/out
17	N2	D12	Share Data bus in/out
19	M2	D14	Share Data bus in/out
21	U1	A0	Share Address bus out
23	R1	A2	Share Address bus out
25	P1	A4	Share Address bus out
27	M3	A6	Share Address bus out
29	Y10	A8	Share Address bus out
31	Y8	A10	Share Address bus out
33	V8	A12	Share Address bus out
35		3V3	Power supply (3.3V)
37		GND	Ground reference
39	V7	A14	Share Address bus out
41	D8	A16	Share Address bus out
43	A3	A18	Share Address bus out
45	C3	A20	Share Address bus out
47	K1	A22	Share Address bus out
49	D1	A24	Share Address bus out
51		d.c.	Leave unconnected
53	B1	CSn2	Chip select out **- internal pull-up (10 kΩ)**
55	E4	CSn6	Chip select out **- internal pull-up (10 kΩ)**
57	B7	WEn	SRAM write strobe out
59	T15	INT0	External interrupts
61	V16	INT2	External interrupts
63	V14	ASYNC	AC97 frame sync
65		3V3	Power supply (3.3V)
67		GND	Ground reference
69	W15	SCLK1	SPI bit clock

Pin	uP pin	name	DZN & DZQ J2 ODD 71 –139 (6/8)
71	D18	ARSTn	AC97 reset output
73	Y17	SFRM1	SPI frame clock output
75	E18	EGPIO0	Enhanced GPIO
77	F17	EGPIO2	Enhanced GPIO
79	F18	EGPIO4	Enhanced GPIO
81	F19	EGPIO6	Enhanced GPIO
83	F20	EGPIO8	Enhanced GPIO
85	G19	EGPIO10	Enhanced GPIO
87	A17	EGPIO12	Enhanced GPIO
89	D15	EGPIO14	Enhanced GPIO
91	L19	RSTn	User Reset I/O (open drain)
93	Y18	RLED	Red LED
95		LBOOT0	Boot configuration pin active during reset. By default it is pulled down with a 10 kΩ resistor. See 5.4for details.
97	W18	SLA1	Flash programming voltage control . Leave open
99	W19	SLA0	Flash programming voltage control . Leave open
101		3V3	Power supply (3.3V)
103		GND	Ground reference
105	V12	TDI	JTAG data in
107	W13	TMS	JTAG test mode select
109	L20	PORSTn	Power on reset input (active low)
111		LED4	LED signal from LAN PHY.
113		LED3	LED signal from LAN PHY.
115		LED2	LED signal from LAN PHY.
117		LED1	LED signal from LAN PHY.
119		LED0	LED signal from LAN PHY.
121	V20	TXD0	Transmit out UART1
123	V17	RTS0n	Ready to send UART1
125	U11	DSR0n	Data set ready UART1
127		CTTD	Reference for Tx wiring central tap. Connect as in 5.3
129		ETH TX -	Transmit - differential signal to Xformer. Connect as in 5.3
131		ETH TX +	Transmit + differential signal to Xformer. Connect as in 5.3
133		ETH RX +	Receive + differential signal to Xformer. Connect as in 5.3
135		ETH RX -	Receive - differential signal to Xformer. Connect as in 5.3
137		CTRD	Reference for Rx wiring central tap. Connect as in 5.3
139		GND	Ground reference

Pin	uP pin	name	DZN & DZQ J2 EVEN 2-70 (7/8)
2		GND	Ground reference
4	Y9	D1	Shared Data bus in/out
6	U9	D3	Shared Data bus in/out
8	W7	D5	Shared Data bus in/out
10	W6	D7	Shared Data bus in/out
12	P3	D9	Shared Data bus in/out
14	N3	D11	Shared Data bus in/out
16	N1	D13	Shared Data bus in/out
18	L4	D15	Shared Data bus in/out
20		GND	Ground reference
22	R2	A1	Share Address bus out
24	N4	A3	Share Address bus out
26	M4	A5	Share Address bus out
28	M1	A7	Share Address bus out
30	W9	A9	Share Address bus out
32	W8	A11	Share Address bus out
34	U8	A13	Share Address bus out
36	Y5	A15	Share Address bus out
38	A6	A17	Share Address bus out
40	D5	A19	Share Address bus out
42	K3	A21	Share Address bus out
44	E1	A23	Share Address bus out
46	F4	A25	Share Address bus out
48	C1	CSn1	Chip select out **- internal pull-up with 10 kΩ**
50	C2	CSn3	Chip select out **- internal pull-up with 10 kΩ**
52	A1	CSn7	Chip select out **- internal pull-up with 10 kΩ**
54		GND	Ground reference
56	A7	RDn	SRAM read active low
58	J2	DQMn0	Shared data mask out active low
60	J3	DQMn1	Shared data mask out active low
62	B19	WAITn	SRAM Wait in active low
64	U15	INT1	External interrupts
66	W17	INT3	External interrupts
68	Y20	ABITCLK	AC97 bit clock
70	E16	ASDI	AC97 primary input

Pin	uP pin	name	DZN & DZQ J2 EVEN 72-140 (8/8)
72	U14	SSPRX1	SPI Input
74	Y16	ASDO	AC97 output
76	V15	SSPTX1	SPI output
78	D20	EGPIO1	Enhanced GPIO
80	E19	EGPIO3	Enhanced GPIO
82		GND	Ground reference
84	E20	EGPIO5	Enhanced GPIO
86	G17	EGPIO7	Enhanced GPIO
88	G18	EGPIO9	Enhanced GPIO
90	G20	EGPIO11	Enhanced GPIO
92	B17	EGPIO13	Enhanced GPIO
94	A18	EGPIO15	Enhanced GPIO
96	Y13	TD0	JTAG data out
98	W12	TCK	JTAG clock in
100	B20	TRSTn	JTAG reset
102		MRSTn	Master reset input (open drain) normally pulled up. See 5.2 for details.
104	W16	GLED	Green LED
106	W14	EECLK	EEPROM / Two – wire Interface clock
108	Y15	EEDAT	EEPROM / Two – wire Interface data
110		LEECLK	Boot configuration pin active during reset. By default it is pulled up with a 10 kΩ resistor. See 5.4for details.
112		LASDO	Boot configuration pin active during reset. By default it is pulled udown with a 10 kΩ resistor. See 5.4for details.
114		nWC	Write protection signal (active low) of the EEPROM. Normally it is pulled low and writing is allowed. Pull it high to protect data.
116		GND	Ground reference
118		LCSn7	Boot configuration pin active during reset. By default it is pulled down with a 10 kΩ resistor. See 5.4for details.
120	U19	TXD1	Transmit / IrDA output
122	U18	RXD1	Receive / IrDA input
124	V18	USBP0	USB positive signals
126	C18	USBP2	USB positive signals
128	T17	RXD0	Receive in
130	V19	CTS0n	Clear to send UART1
132	Y12	DTR0n	Data terminal ready output UART1
134	U17	USBM0	USB negative signals
136	D17	USBM2	USB negative signals
138		3V3	Power supply (3.3V)
140		GND	Ground reference

5 - Pin Description and Off-Board Settings

Users plug Zefeer boards over an host PCB where customized interfaces and electronics have been designed. In order to reduce the amount of setting needed to set up properly the board, most of the bootstrapping logic has been embedded on the board. Consequently, very few settings are mandatory on the host board to get Zefeer properly working.

In the following paragraphs, most important notes related on how to interface to the module are listed.

5.1 Power (3V3 and GND)

Power consumption of the board is around 1.0 Watt in average almost equally shared among 3.3V and 1.8V. Power is fed directly from host board. It means that user should be sure to provide at least this amount of current. Tolerances in power supply should not exceed +/- 5%.

Values for maximum current should be equally distributed among power and ground pins of the module. Although needed current per single pin is very low, it is suggested to design the layout below the module with wide power and ground planes, in order to reduce current parasitic loops.

Refer to Chapter 6 for details related to power supply.

5.2 RESET (MRSTn, PORSTn, RSTn, TRSTn)

This group of pins rules over reset behaviour.

MRSTn is the reset input by which user can reset the board exactly as they switch it on from power supply down. This input acts on both PORSTn and RSTn, forcing them low in chain as explained below. As a consequence all device on board are reset. MRSTn is an Open Collector input.

PORSTn is the "power-on reset" input of the microprocessor that start microprocessor at the power up and re-start microprocessor from scratch every time exactly as it was a novel power up (see ref.). It is an Input for the microprocessor and it is connected to the Open Collector output of the CPU supervisor. It is reflected to the output connector mostly for monitoring of internal processes.

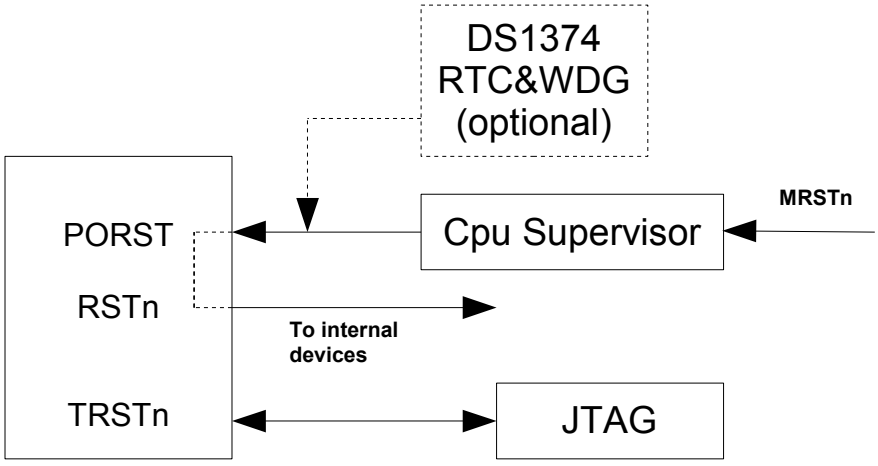

Fig. 2: Reset Connections

RSTn is the “user reset” Open Collector bidirectional pin of the microprocessor. If used as an input (from external) it reset microprocessor only partially (see ref.). In this case is responsible also for reset of some devices on board. If used as an output it “reflects” signal PORSTn when it applied.

WARNING: Cirrus Logic strongly reccommends to use this pin as only output, and buffer it as it comes out from the connector.

TRSTn is the reset signal of the JTAG interface. It should be connected externally to the signal RSTn in order to automatically generate a reset to the microprocessor when using JTAG or reset JTAG interface when powering up the board.

For modules that mounts DS1374 as RTC, remember that signal RST# that comes out from RTC, is connected to EP93xx PORST# signal. This allow to reset microprocessor upon watchdog event, and from sw command via i2c interface.

5.3 ETHERNET (TX+, TX-, RX+, RX-, CTTR, CTRD)

This group of pins allows connection with magnetics and connectors of a LAN. These pin are to be routed to magnetics and RJ45 with a certain care. Following routing indications are listed below:

- Route differential pairs close together and away from everything else.
- Avoid vias and layer changes.
- Keep both traces of each differential pairs as close to the same length as possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate with a ground plane layer.

Magnetics can be embedded or not in the RJ45 case, even if RJ45 connectors with embedded transformers are more and more popular.

Suggested magnetics are F0059 from InNet, LU1S041 from Bothhand or XFATM9N-COMBO1-2MS from XFRMS.

A possible design solution for these last ones is depicted in Fig. 3.

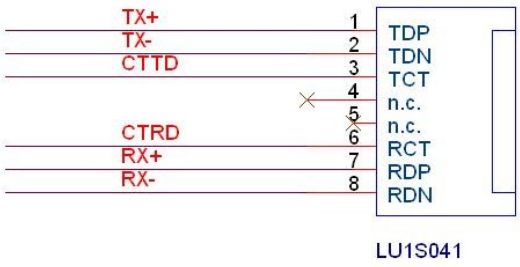

Fig. 3 - Connecting To Magnetics and RJ45

5.4 Bootstrapping options

Bootstrapping of microprocessors of EP93XX family is very flexible. Zefeer modules allow users to make use of this flexibility but – also – recognize that some solutions are to be preferred to many others. Nevertheless Zefeer modules implement most of the logic needed to adopt different bootstrapping options.

In table 1 bootstrapping options are summarized. Coloured strip identify default configuration of bootstrapping pins. In other words it means that – during reset period – these pins are pulled down or up with a 10 kΩ resistor. If users want to modify precharged bootstrapping strategy, they should pull pins with a 1 kΩ resistor.

Boot configuration	**LEECLK**	**LBOOT0**	**LASDO**	**LCSn7**	**LCSn6**
External boot from 16bit Sync Flash	L	L	H	L	L
External boot from 16bit Sync ROM	L	L	H	L	H
External boot from 32bit Sync Flash	L	L	H	H	L
External boot from 32bit Sync ROM	L	L	H	H	H
External boot from 8bit SRAM	L	L	L	L	L
External boot from 16bit SRAM	L	L	L	L	H
External boot from 32bit SRAM	L	L	L	H	L
External boot from 32bit SRAM	L	L	L	H	H
32bit serial boot	H	H	X	H	H
32bit serial boot	H	H	X	H	L
16bit serial boot	H	H	X	L	H
Internal SPI boot	H	L	X	X	X
Internal boot from on-chip ROM w/ Sync Memory at 16bit	H	L	H	L	L
Internal boot from on-chip ROM w/ Sync Memory at 16bit	H	L	H	L	H
Internal boot from on-chip ROM w/ Sync Memory at 32bit	H	L	H	H	L
Internal boot from on-chip ROM w/ Sync Memory at 32bit	H	L	H	H	H
Internal boot from on-chip ROM w/ Async Memory at 8bit	H	L	L	L	L
Internal boot from on-chip ROM w/ Async Memory at 16bit	H	L	L	L	H
Internal boot from on-chip ROM w/ Async Memory at 32bit	H	L	L	H	L
Internal boot from on-chip ROM w/ Async Memory at 32bit	H	L	L	H	H

Tab. 1 - Bootstrapping options. Red cells indicate default. Shadowed lines do not apply to DZA and DZB models

As an example, if user want to boot from an external 32bit SRAM, they must connect one 1 kΩ pull –down resistor on signal LEECLK and one 1 kΩ pull–up resistor on signal LCSn7.

See EP93xx manuals for further informations.

5.5 NOR Flash Memory

Zefeer modules can mounts up to 2 chip flash memory. The first chip mounted by defatult is connected to CSn0, while the second slot chip is connected to CSn7. If your module mount only one flash memory chip, CSn7 is free. Zefeer can mounts two type of flash memories: Intel P30 NOR Flash type and Intel J3 Strata Flash type. **These two memories are not compatible.** So, user must pay attention to order the modules with right flash and program it with right sw code. If you are in possess of ZELK Kit, please refer to [1] for details about software. **Modules that mount P30 or J3 Strata flash have different Order Codes.** All Order codes that have the third digit equals to "1" (for example DZQ36**1**0) mount P30 flash Type (more generally all codes as"DZxxx1x"). Order codes that have the third digit equals to "0" (for example DZQ36**0**0) mount J3 flash Type (more generally all codes as"DZxxx0x"). For further details about order codes refer to Section 10.

5.6 Interrupts

EP93xx microprocessor comes with some native interrupt sorces named as INT0,INT1,INT2,INT3 other than some GPIOs that can configured as interrupt source (up to 54 total interrupt sources). Though EP9301 and EP9302 lucks of INT2, so while DZQ and DZG module come with all four native interrupts, DZA and DZB comes with only INT0,INT1,INT3. No Interrupts signal is utilized internally into Zefeer module. This means that user can utilize these signal at connetor J1,J2 that directly comes out without pull-up or pull-down. For pin number of these signals on the connector J1,J2, please refer to chapter 4.

5.7 Asynchronous Chip selects

EP93xx microprocessor comes with some native Chip selects from asynchornous memory type as SRAM, NOR FLASH etc. These come out to J1, J2 connectors and are: Csn1, Csn2, Csn3, Csn6, CSn7. For pin number of these signals on the connector J1, J2, please refer to chapter 4. It's worthwhile to remember that CSn0 is utilized internally as flash memory chip select, so **USER MUST NOT USE IT**. All the others are available for user purpose, and are pulled-up internally with a 10 kΩ resistor since this signals are active low.

6 - Power Supply

Powering is usually a delicate operation. In Zefeer modules this operation has been embedded in the module and therefore power sequencing is self-contained and simplified.

Nevertheless power must be provided from host board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters.

The only power input is 3.3V. In Tab. 2- Power supply ranges are summarized limits for power supply values. Beyond this limits, proper working is not guaranteed since reset circuits are triggered to start on these limits. Further details about reset, see Chapter 6. Powering is usually a delicate operation. In Zefeer modules this operation has been embedded in the module and therefore power sequencing is self-contained and simplified.

	MIN	MAX
3.3V Power supply	3.15V	3.45

Tab. 2- Power supply ranges

A slope steeper than 0.5 V/ms is recommended for power supply voltage, even if not mandatory. Also the ripple should be reduced as much as possible, under 50mV peak-to-peak. We never noticed problems particular spectral composition of the ripple noise.

In Tab. 3 are summarized nominal current consumptions and power consumption at 3.3V. Also power and current absorption are indicated in case of low-power.

Device	Type	DZA/DZB	DZN/DZQ
CPU	I/O + Core + PLL	100 to 675 mW	100 to 750 mW
SDRAM	Average	590 mW	1180 mW
NOR Flash	writing	70 mW	70 mW
Watchdog/Reset		≈ 0 mA	≈ 0 mA
Ethernet	STE100P	300 mW	300 mW
Operative Power		1060 - 1635 mW	1060 – 1710 mW
Operative Current @ 3.3V		(≈ 0.32 – 0.5 A)	(≈ 0.32-0.52 A)
Stand-by current		< 50 mA	< 50 mA

Tab. 3- Summary of the budgetary power consumption

7 - Voltage Monitoring

In order to guarantee that microprocessor is monitored accurately, we should consider possible range of its supply, that are summarized below:

- 1.8V (min. 1.65V – max. 1.95V)
- 3.3V (min. 3.0V – max. 3.6V)

Due to the fact that power supply regulation is provided from external circuitry, it is mandatory to monitor accurately both voltages.

As far as 3.3V is concerned, a reset threshold at 3.08V with a maximum, possible temperature variation of +/- 2.5% in the range –40°C to +125°C has been adopted. In practice reset threshold has a variation from 3.00V to 3.15V all over the extended temperature range.

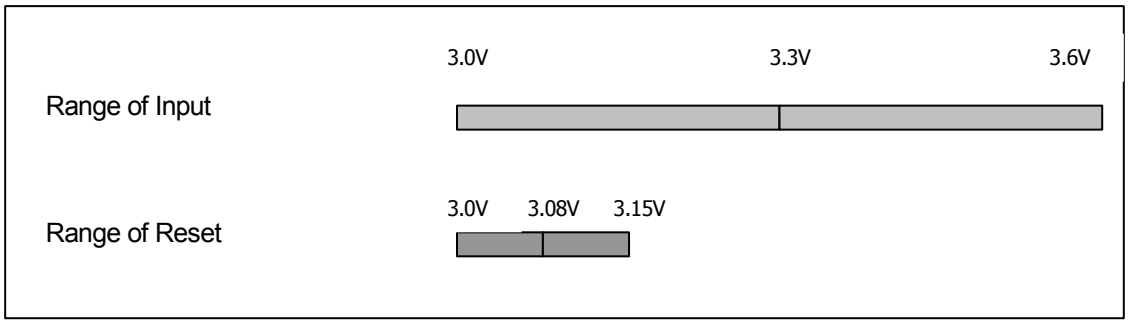

Fig. 4 – Graphical representation of reset thresholds for 3.3V [–40°C to +125°C]

Same considerations hold for 1.8V supply as in Fig. 5.

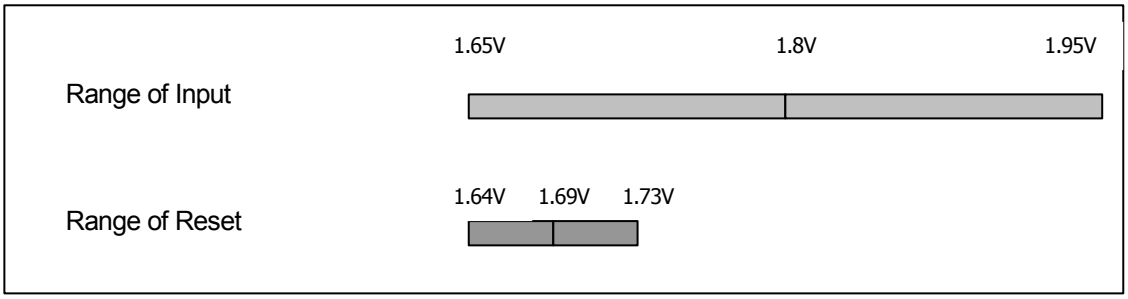

Fig. 5 - Graphical representation of reset thresholds for 1.8V [0°C to +80°C]

This combined values – although in a extended temperature range – limit in practice the range of possible power supply voltages in the range 3.15 to 3.6V for I/O supply voltage, and 1.73V to 1.95V for Core voltage.

Limitation to 3.15V-3.45V and 1.73V-1.95V is due to the other component restrictions. See Chapter 5for that.

8 - Resource allocation

Table 4 show how chip selects are used. Yellow highlighted rows show the differences between modules manufactured before and after October 2005.

No interrupts lines are used.

Chip select	***Peripheral***	
	Modules manufactured after October 2005	***Modules manufactured before October 2005***
nCS0	16-bit StrataFlash (boot memory)	Not used
nCS1	Not used	Not used
nCS2	Not used	Not used
nCS3	Not used	Not used
nCS6	Not used	16-bit StrataFlash (boot memory)
nCS7	16-bit StrataFlash #2 (optional, DZN/ DZQ only)	16-bit StrataFlash #2 (optional, DZN/ DZQ only)
nSDCE0	Not used	Not used
nSDCE1	SDRAM	SDRAM
nSDCE2	Not used	Not used
nSDCE3	Not used	Not used

Tab. 4 - Chip selects utilization

9 - RTC & WDG - DS1374U-33 (Optional)

Some Zefeer models mounts Dallas DS1374U-33 device on-board as RTC with Watchdog functionality (**in order to know what models have DS1374 on-board, see Section 10**)). This device is controlled by microprocessor, via I2C serial interface. Watchdog period can be modified by register and can varies from a min of 250ms to a maximum of 4096 sec. DS1374 RST# signal is connected directly to EP93xx PORST# signal (See Section).This device provide an input for battery backup named “Vbackup” (for further details refer to Dallas DS1374 Datasheet available manufacturer web site.) “Vbackup” signal comes out from pin 9 of J1 connector. User can connect directly a 3V lithium battery to this pin. In order to avoid battery discharge during stock phase, it's recommended to insert a jumper from pin J1.9 and battery device. Remember that Zefeer Models mounting DS1374 as RTC and WDG, have EP93xx native watchdog disabled by default during bootstrap phase (via bootstrap options.).

10 - Naming, order codes and standard releases

Each Zefeer module report a marking code label on top side that identify the specific model according to order code.

Product: Zefeer DZA/DZB

Code structure

DZ	p	f	s	k	c	t	n	iiii
Family	**Processor**	**Flash memory size**	**SDRAM memory size**	**Flash memory type**	**Connectors**	**Temperature range**	**Submodel**	**Identifier**
DZ = Dave Zefeer	A = EP9301 B = EP9302	1 = 16MB 4 = 4MB 8 = 8MB	1 = 16MB 3 = 32MB 6 = 64MB	0 = J3 1 = P30	0 = both connectors 1 = J1 removed (hole)	C = commercial (0/+70°C) I = industrial(-40/+85 °C)	See table below	Combined with other fields, identifies univocally the product

Submodel	Description
0 or <blank>	Flash memory connected to CSn6, NO RTC DS1374, EP93xx WDT enabled
1	Flash memory connected to CSn0, NO RTC DS1374, EP93xx WDT enabled, PCB REV.A

Note: Industrial modules work at reduced clock speed when operating in the extended temperature range (-40/+85°C); anyway, industrial modules could be used at full speed (200MHz) in the commercial temperature range (0-70°C).

Valid combinations (for combinations not listed here please contact our sales department)

DZA4100C1R	
DZA4101C1R	
DZB4100C1R	
DZB8300C1R	
DZB8301C1R	

Product: Zefeer DZG/DZN/DZQ

Code structure

DZ	p	f	s	k	c	t	n	iiii
Family	**Processor**	**Flash memory size**	**SDRAM memory size**	**Flash memory type**	**Connectors**	**Temperature range**	**Submodel**	**Identifier**
DZ = Dave Zefeer	G = EP9307 N = EP9312 Q = EP9315	1 = 16MB 3 = 32MB 4 = 4MB 8 = 8MB	1 = 16MB 2 = 128MB 3 = 32MB 6 = 64MB	0 = J3 1 = P30	0 = both connectors	C = commercial (0/+70°C) I = industrial(-40/+85 °C)	See table below	Combined with other fields, identifies univocally the product

Submodel	Description
0 or <blank>	Flash memory connected to CSn6, NO RTC DS1374, EP93xx WDT enabled
1,2	Flash memory connected to CSn0, NO RTC DS1374, EP93xx WDT enabled, PCB REV.A
3	Flash memory connected to CSn0, NO RTC DS1374 ,EP93xx WDT enabled,PCB REV.B, Pinout changed respect 2
4	Flash memory connected to CSn0, RTC AND WDT BY DS1374 ON-BOARD, EP93xx WDT disabled,PCB REV.B, pinout changed respect 2

Note: All ROHS products have code with a suffix "R".

Note: Industrial modules work at reduced clock speed when operating in the extended temperature range (-40/+85°C); anyway, industrial modules could be used at full speed (200MHz) in the commercial temperature range (0-70°C).

Valid combinations (for combinations not listed here please contact our sales department)

DZN3610C3R	
DZQ3610I3R	
DZQ3610C3R	
DZQ3610I4R	
DZN3610I4R	
DZQ3610C4R	

11 - Agency approvals

Even if there is no obligation to do it, DAVE is proud to claim that all CPU modules have been approved by an agency authorized to release them

Only some test have been reputed to be inherent and applicable, namely:

- EN 55022 : Emission of radiated disturbances
- EN 61000-4-3 : Immunity to RF electromagnetic fields
- EN 61000-4-4 : Immunity to fast transient bursts (mains)
- EN 61000-4-4 : Immunity to fast transient bursts (communication lines)
- EN 61000-4-6 : Immunity to RF conducted disturbances (mains)
- EN 61000-4-6 : Immunity to RF conducted disturbances (communication lines)

Test reports are available on request.

12 - History

Rev.	Date	Hw Rev.	Details
1.0.0	Nov 04	CS034304, CS024204	Preliminary specs
1.0.1	Jan 05	CS034304, CS024204	Small Fixes
1.0.2	Jan 05	CS034304, CS024204	Small Fixes
1.0.3	Jan 05	CS034304A, CS024204	New hw-revison CS034304A for DZN/DZQ model; New sections about interrupt, and asyn-chip selects.
1.0.4	Mar 05	CS034304A, CS024204A	New hw-revison CS024204A for DZA/DZB model; changed pinout of JP1 for DZA/DZB
1.0.5	May 05	CS034304A, CS024204A	Fig.1 bottom view
1.1.0	Oct 05	CS034304A, CS024204A	Changed default boot configuration. Small fixes.
1.2.0	Dec 06	CS034304B, CS024204A	CS034304B (DZN/DZQ) small changes to pinout. New models that supports new features: RTC on board, Flash P30.
1.2.1	Sep 07	CS034304B, CS024204A	Product Codes Updated; small fixes.
1.2.2	Oct 07	CS034304B, CS024204A	Note about Industrial modules
1.2.3	Oct 07	CS034304B, CS024204A	Small fixes (Hirose connector model)
1.2.4	Nov 07	CS034304B, CS024204A	Small fixes (Connectors signals)

13 - Support

To contact technical support, please send an e-mail to address support-zefeer@dave.eu

14 - References

[1] DAVE Zefeer Embedded Linux Kit (ZELK) – Software Manual
[2] DAVE Zefeer eCos development kit (ZECK) Kit – Software Manual
[3] DAVE Zefeer Windows CE BSP (ZWCK) – Software Manual
[4] DAVE Zefeer Evaluation Board EVB User Manual
[5] AMP site (www.amp.com)
[6] HIROSE site (http://www.hirose.com)
[7] STM, STE100P data sheet
[8] CIRRUS LOGIC EP93XX Users Manual