Freescale Semiconductor
User's Manual Addendum

MCF5282UMAD
Rev. 15, 05/2007

MCF5282 User's Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5282 ColdFire Microcontroller User's Manual*, order number MCF5282UM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

Table of Contents

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1 Errata for Revision 2.3

Table 1. MCF5282UM Rev 2.3 Errata

Location	Description
Table 2-1/Page 2-4	Remove last sentence in C bit field description.
Table 2-3/Page 2-7	Change PC's Written with MOVEC entry to "No".
Section 2.5/Page 2-8	Change last bullet to "Use of separate system stack pointers for user and supervisor modes"
Section 2.5/Page 2-9	Change last sentence in fourth paragraph (step 2) to "The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address."
Figure 3-6/Page 3-8	Add minus sign to the exponent so that it is "–(i + 1 – N)".
Table 4-3/Page 4-5	Change reset value of ACR0, ACR1 to "See Section" since some of the bits are undefined after reset.
Figure 4-2/Page 4-6	Change CACR fields to R/W, since they may be read via the debug module.
Table 4-5/Page 4-8	For split instruction/data cache entry, swap text in parantheses in the description field. Instruction cache uses the upper half of the arrays, while data cache uses the lower half.
Figure 4-3/Page 4-9	Change reset value of ACR: Bits 31-16, 14-13, 6-5, and 2 are undefined, and other bits are cleared. Change ACR fields to R/W, since they may be read via the debug module.
Section 4.4.2.2/Page 4-9	Change note to: **NOTE** Peripheral (IPSBAR) space should not be cached. The combination of the CACR defaults and the two ACR*n* registers must define the non-cacheable attribute for this address space.
Figure 5-1/Page 5-2	Change RAMBAR fields to R/W, since they may be read via the debug module.
Table 5-1/Page 5-2	The PRI1/PRI2 text description does not match the table below it. It should be: "If a bit is set, CPU has priority. If a bit is cleared, DMA has priority."
Chapter 8	Remove any references to the core watchdog timer being able to reset the device. It is only able to interrupt the processor. Use the peripheral watchdog timer described in Chapter 18 if needing a watchdog timer to reset the device.
Table 9-4/Page 9-7	In the table for MFD bit definition, footnote (1) equation should read: $f_{sys} = \frac{f_{ref} \times 2(MFD + 2)}{2^{RFD}}$; $f_{ref} \times 2(MFD + 2) \leq f_{sys(max)}$; $f_{sys} \leq f_{sys(max)}$ Where $f_{sys(max)}$ is the maximum system frequency for the particular MCF5282 device (66MHz or 80MHz)
Section 10.3.6/Page 10-11	Include the following text in the section description and as a note in Figure 10-9. "It is the responsibility of the software to program the ICR*n*x registers with unique and non-overlapping level and priority definitions. Failure to program the ICR*n*x registers in this manner can result in undefined behavior. If a specific interrupt request is completely unused, the ICR*n*x value can remain in its reset (and disabled) state."
Figure 10-6/Page 10-9	Interrupt Force Register Low (INTFRCL*n*) is illustrated as read-only in the figure. However, this register should be read/write.

Table 1. MCF5282UM Rev 2.3 Errata (continued)

Location	Description
Table 10-14/Page 10-15	Change flag clearing mechanism for sources 24-26. They should read as follows: Write ERR_INT = 1 after reading ERR_INT = 1 Write BOFF_INT = 1 after reading BOFF_INT = 1 Write WAKE_INT = 1 after reading WAKE_INT = 1
Table 12-7/Page 12-7	BAM bit field description, the first example should read “So, if CSAR0 = 0x0000 and CSMR0[BAM] = 0x0001” instead of “So, if CSAR0 = 0x0000 and CSMR0[BAM] = 0x0008”.
Table 10-2/Page 10-4	In footnote, remove mention of the SWIACK register, as it is not supported in the global IACK space.
Section 10.3.7/Page 10-16	Change last paragraph to: “In addition to the IACK registers within each interrupt controller, there are global L*n*IACK registers. A read from one of the global L*n*IACK registers returns the vector for the highest priority unmasked interrupt within a level for all interrupt controllers. There is no global SWIACK register. However, reading the SWIACK register from each interrupt controller returns the vector number of the highest priority unmasked request within that controller.”
Table 15-1/Page 15-3	NOP command entry. Replace “$\overline{\text{SRAS}}$ asserted” with “$\overline{\text{SDRAM\_CS}}$[1:0] asserted”
Table 15-5/Page 15-7	Add the following note to the DACR*n*[CBM] field description: **Note:** It is important to set CBM according to the location of the command bit.
Section 16.5/Page 16-11	Remove last sentence in this section starting with “BCR*n* decrements...” since SAA bit is not supported.
Chapter 17	The maximum buffer size of the FEC is 2032 bytes. Replace any mention of the max size being 2047 bytes with 2032 bytes.
Section 17.4.6/Page 17-7	Add the following subsection entitled “Duplicate Frame Transmission”: The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. In order to remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC will fetch from memory a BD that has already been processed but not yet written back (that is, it is read a second time with the R bit still set). In this case, the data is fetched and transmitted again. Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for either large or small frames, one of the following must be true: • The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared. • Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched. • The FEC software driver ensures a minimum frame size, *n*. The minimum number of TxBDs is then (Tx FIFO Size ÷ (*n* + 4)) rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.
Table 17-9/Page 17-17	Correct MIB block counters end addresses to IPSBAR + 0x12FF.
Table 17-11/Page 17-19	Add RMON_R_DROP with an IPSBAR Offset of 0x1280 and a description of ‘Count of frames not counted correctly’.
Figure 17-26/Page 17-41	Change EMRBR register address from “IPSBAR + 0x11B8” to “IPSBAR + 0x1188”.
Section 20.5.13/Page 20-12	Deleted reference to nonexistent CF bits in the figure and bit descriptions for the GPTFLG2 register.

Table 1. MCF5282UM Rev 2.3 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Figure 23-18/Page 23-18</td><td>Remove the two 16-bit divider blocks from timer input, as the divider is not available using external clock sources.</td></tr>
<tr><td>Section 23.5.1.2.2/Page 23-19</td><td>Remove 16-bit divider from equation, as the divider is not available using external clock sources.</td></tr>
<tr><td>Section 25.5.8/Page 25-25</td><td>Change end of last sentence from “...and can be written by the host to ‘0’.” to “...and can be written by the host to ‘1’.”</td></tr>
<tr><td>Table 25-17/Page 25-29</td><td>Remove the following information from the BITERR and ACKERR descriptions as these fields are read only: “To clear this bit, first read it as a one, then write it as a one. Writing zero has no effect.” (This is a rescindment of a previous documentation errata.)
Change last sentence in ERRINT description from: “To clear this bit, first read it as a one, then write as a zero. Writing a one has no effect.” to “To clear this bit, first read it as a one, then write a one. Writing a zero has no effect.”
Add the following information to the BOFFINT and WAKEINT descriptions: “To clear this bit, first read it as a one, then write it as a one. Writing zero has no effect.”</td></tr>
<tr><td>Table 25-17/Page 25-27</td><td>Definition of bits ERRINT and BOFFINT are incorrect for register ESTAT: ERRINT should be bit 1, BOFFINT should be bit 2. They should be cleared by writing a one instead of a zero.</td></tr>
<tr><td>Table 26-1/Page 26-5</td><td>Change description field for DTOUT1 from “DMA timer 1 output / Port TD[3]...” to “DMA timer 1 output / Port TD[2]...”
Change description field for DTIN0 from “DMA timer 0 input / Port TD[3]...” to “DMA timer 1 output / Port TD[1]...”
Change description field for DTOUT0 from “DMA timer 0 output / Port TD[3]...” to “DMA timer 1 output / Port TD[0]...”</td></tr>
<tr><td>Table 30-12/Page 30-14</td><td>Add the following note to the PBR[Address] field description:
Note: PBR[0] should always be loaded with a 0.</td></tr>
<tr><td>Table 30-20/Page 30-35</td><td>Change CSR’s initial state to 0x0000_0000.</td></tr>
<tr><td>Chapter 33</td><td>Add the following note:
“It is crucial during power-up that VDD never exceeds VDDH by more that ~0.3V. There are diode devices between the two voltage domains, and violating this rule can lead to a latch-up condition.”</td></tr>
<tr><td>Table 33-3/Page 33-3</td><td>In the V_{OH} and V_{OL} entries, change the respective I_{OH} and I_{OL} specs from “I_{OH} = -2.0mA” to “I_{OH} = -5.0mA” and “I_{OL} = +2.0mA” to “I_{OL} = +5.0mA”</td></tr>
<tr><td>Table 33-8/Page 33-7</td><td>In the PLL Electrical Specifications table, only specs for the 80MHz MCF5282 device were listed. Insert specs for the 66MHz device in the first 2 rows and also declare symbol $f_{sys(max)}$, as shown below:
<table>
<tr><th rowspan="2">Characteristic</th><th rowspan="2">Symbol</th><th rowspan="2">Min</th><th colspan="2">Max</th><th rowspan="2">Unit</th></tr>
<tr><th>66MHz</th><th>80MHz</th></tr>
<tr><td>PLL Reference Frequency Range
Crystal reference
External reference
1:1 Mode</td><td>
$f_{ref\_crystal}$
f_{ref_ext}
$f_{ref\_1:1}$</td><td>
2
2
33.33</td><td>
8.33
8.33
66.66</td><td>
10.0
10.0
80</td><td>MHz</td></tr>
<tr><td>System Frequency [1]
External Clock Mode
On-Chip PLL Frequency</td><td>f_{sys}</td><td>
0
f_{ref} / 32</td><td>$f_{sys(max)}$
66.66
66.66</td><td>$f_{sys(max)}$
80
80</td><td>MHz</td></tr>
</table>
</td></tr>
</table>

Table 1. MCF5282UM Rev 2.3 Errata (continued)

Location	Description
Table 33-8/Page 33-7	Change EXTAL Input High Voltage (V_{IHEXT}) Crystal Mode minimum spec from "V_{DD} - 1.0" to "V_{XTAL} + 0.4". Change EXTAL Input Low Voltage (V_{ILEXT}) Crystal Mode maximum spec from "1.0" to "V_{XTAL} - 0.4".
Section 33.13.1/Page 33-21	Remove second sentence: "There is no minimum frequency requirement."
Section 33.13.2/Page 33-22	Remove second sentence: "There is no minimum frequency requirement." Remove second paragraph as this feature is not supported on this device: "The transmit outputs (ETXD[3:0], ETXEN, ETXER) can be programmed to transition from either the rising or falling edge of ETXCLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs. Refer to the Ethernet chapter for details of this option and how to enable it."
Table A-3/Page A-4	The CSMR1 and CSCR1 register addresses are incorrect. They should be IPSBAR + 0x090 and IPSBAR + 0x096 respectively

2 Errata for Revision 2.1 & 2.2

Table 2. MCF5282UM Rev 2.1 & 2.2 Errata

Location	Description
Figure 4-2/4-6	Changed bit 23 from DIDI to DISI
Table 4-6/4-9	Under 'Configuration' for 'Instruction Cache' the 'Operation' entry changed to "Invalidate 2 KByte data cache"
Table 4-6/4-9	Under 'Configuration' for 'Data Cache' the 'Operation' entry changed to "Invalidate 2 KByte instruction cache"
Figure 6-3/6-6	Changed bit 8 to write-only instead of read/write
Table 6-10/6-15	Removed "selected by BKSL[1:0]" as these are internal signal names not necessary for end-user.
Table 9-4/9-7	In the table for MFD bit definition, footnote (1) equation should read: $f_{sys} = \frac{f_{ref} \times 2(MFD + 2)}{2^{RFD}}$; $f_{ref} \times 2(MFD + 2) \leq f_{sys(max)}$; $f_{sys} \leq f_{sys(max)}$ Where $f_{sys(max)}$ is the maximum system frequency for the particular MCF5282 device (66MHz or 80MHz)
10.3.2/10-8	Add the following note: 'If an interrupt source is being masked in the interrupt controller mask register (IMR) or a module's interrupt mask register while the interrupt mask in the status register (SR[I]) is set to a value lower than the interrupt's level, a spurious interrupt may occur. This is because by the time the status register acknowledges this interrupt, the interrupt has been masked. A spurious interrupt is generated because the CPU cannot determine the interrupt source. To avoid this situation for interrupts sources with levels 1-6, first write a higher level interrupt mask to the status register, before setting the mask in the IMR or the module's interrupt mask register. After the mask is set, return the interrupt mask in the status register to its previous value. Since level seven interrupts cannot be disabled in the status register prior to masking, use of the IMR or module interrupt mask registers to disable level seven interrupts is not recommended.'

Table 2. MCF5282UM Rev 2.1 & 2.2 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Chapter 17</td><td>The maximum buffer size of the FEC is 2032 bytes. Replace any mention of the max size being 2047 bytes with 2032 bytes.</td></tr>
<tr><td>Table 17-2/17-5</td><td>In PALR/PAUR entry, delete “(only needed for full duplex flow control)”</td></tr>
<tr><td>Figure 17-23/17-39</td><td>Change FRSR to read/write instead of read-only.</td></tr>
<tr><td>25.4.10/25-16</td><td>Change CANICR to ICRn.</td></tr>
<tr><td>Table 25-17/25-29</td><td>Add the following information to BITERR and ACKERR descriptions: “To clear this bit, first read it as a one, then write it as a one. Writing zero has no effect.”</td></tr>
<tr><td>Table 25-17/25-30</td><td>Change bit ordering: ERRINT should be bit 2 and BOFFINT should be bit 1.</td></tr>
<tr><td>Table 25-19/25-32</td><td>Change BUFnI field description from “To clear an interrupt flag, first read the flag as a one, then write it as a zero” to “To clear an interrupt flag, first read the flag as a one, then write it as a one.”</td></tr>
<tr><td>Chapter 33</td><td>It is crucial during power-up that VDD never exceeds VDDH by more that ~0.3V. There are diode devices between the two voltage domains, and violating this rule can lead to a latch-up condition.</td></tr>
<tr><td>Table 33-8/33-7</td><td>In the PLL Electrical Specifications table, only specs for the 80MHz MCF5282 device were listed. Insert specs for the 66MHz device in the first 2 rows and also declare symbol $f_{sys(max)}$, as shown below:
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External Clock Mode
On-Chip PLL Frequency</td><td>f_{sys}</td><td>
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f_{ref} / 32</td><td>$f_{sys(max)}$
66.66
66.66</td><td>$f_{sys(max)}$
80
80</td><td>MHz</td></tr>
</table>
</td></tr>
</table>

3 Errata for Revision 2.0

Table 3. MCF5282UM Rev 2.0 Errata

Location	Description
Table 33-8/33-9	Reference to ‘TA = TL to TH’ was not deleted. Delete.

4 Errata for Revision 1.0

Table 4. MCF5282UM Rev 1.0 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>1.1/1-1</td><td>Change ‘Real time debug support, with two user-visible hardware breakpoint registers’
To ‘Real time debug support, with one user-visible hardware breakpoint register’</td></tr>
<tr><td>Table 2-2/2-7</td><td>Change the I field description to read: “Interrupt level mask. Defines the current interrupt level. Interrupt requests are inhibited for all priority levels less than or equal to the current level, except the edge-sensitive level 7 request, which cannot be masked.”</td></tr>
<tr><td>Table 5-1/5-2</td><td>Replace the description of PRI1 and PRI2 with the following:
<table>
<tr><th>Description</th></tr>
<tr><td>Priority bit. PRI1 determines if DMA or CPU has priority in upper 32K bank of memory. PRI2 determines if DMA or CPU has priority in lower 32K bank of memory. If bit is set, DMA has priority. If bit is reset, CPU has priority. Priority is determined according to the following table.
<table>
<tr><th>PRI[1:2]</th><th>Upper Bank Priority</th><th>Lower Bank Priority</th></tr>
<tr><td>00</td><td>DMA Accesses</td><td>DMA Accesses</td></tr>
<tr><td>01</td><td>DMA Accesses</td><td>CPU Accesses</td></tr>
<tr><td>10</td><td>CPU Accesses</td><td>DMA Accesses</td></tr>
<tr><td>11</td><td>CPU Accesses</td><td>CPU Accesses</td></tr>
</table>
NOTE: The Motorola-recommended setting for the priority bits is 00.</td></tr>
</table></td></tr>
<tr><td>Table 5-1/5-3</td><td>Add the following note to the SPV bit description: “The BDE bit in the second RAMBAR register must also be set to allow dual port access to the SRAM. For more information, see Section 8.4.2, ‘Memory Base Address Register (RAMBAR).’”</td></tr>
</table>

Table 4. MCF5282UM Rev 1.0 Errata (continued)

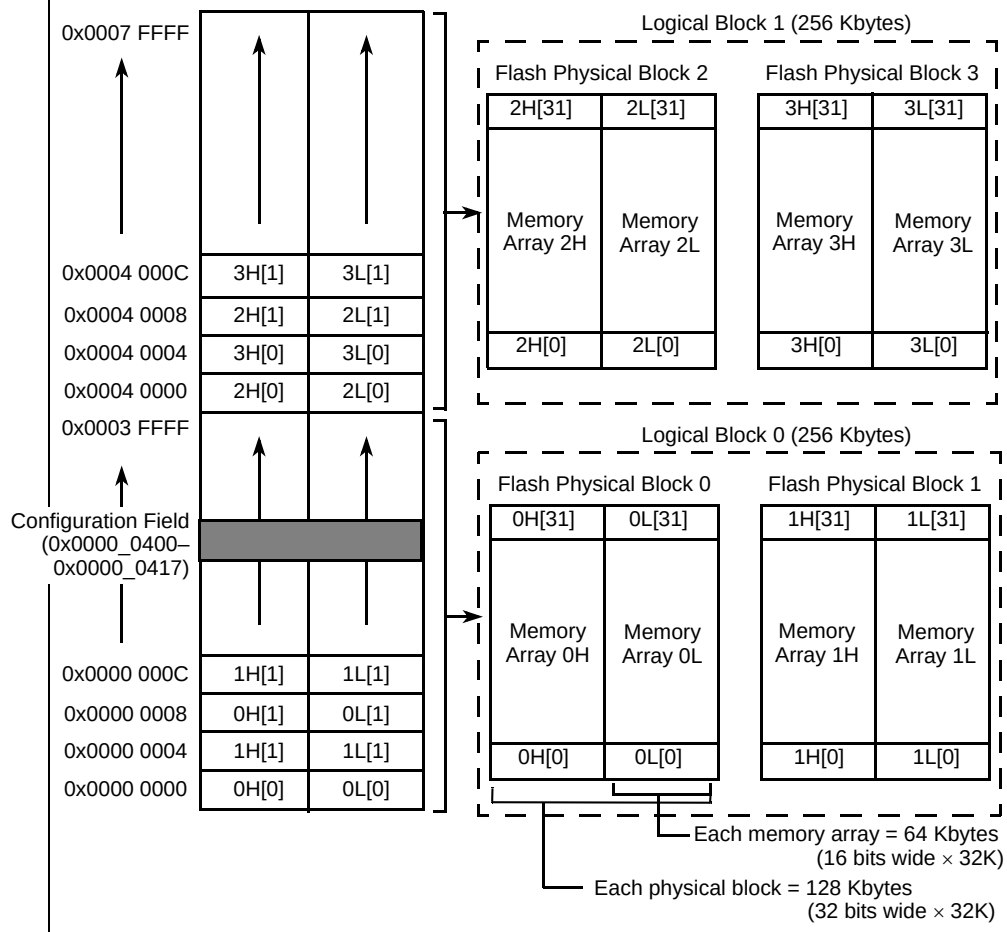
Location	Description
Figure 6-2/6-4	Replace Figure 6-2, “CFM 512K Array Memory Map,” with the figure below.  **Figure 6-2. CFM 512K Array Memory Map**
Table 6-12/6-16	Change value for page erase verify command to 0x06.
Table 6-13/6-20	Change value for page erase verify command to 0x06.
Table 8-3/8-5	Add the following note the BDE bit description: “The SPV bit in the CPU’s RAMBAR must also be set to allow dual port access to the SRAM. For more information, see Section 5.3.1, ‘SRAM Base Address Register (RAMBAR).’”
Figure 9-1/9-3	Remove ÷ 2 from CLKGEN block.
10.3.6/10-11	Add this text to the end of the first paragraph: “If a specific interrupt request is completely unused, the ICR*nx* value can remain in its reset (and disabled) state.”
10.5/10-17	Add the following note: “The wakeup mask level taken from LPICR[6:4] is adjusted by hardware to allow a level 7 IRQ to generate a wakeup. That is, the wakeup mask value used by the interrupt controller must be in the range of 0–6.”
Figure 12-4/12-8	Change CSCR*n* to reflect that AA is set to ‘1’ at reset.
13.5/13-15	Remove final paragraph. The paragraph incorrectly states that the MCF5282 does not have a bus monitor.

Table 4. MCF5282UM Rev 1.0 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 17-13/17-26</td><td>Change encodings for bits 31–9 to:
0The corresponding interrupt source is masked.
1The corresponding interrupt source is not masked.</td></tr>
<tr><td>Chapter 19</td><td>Change PIT1–PIT4 to PIT0–PIT3 throughout chapter. When a timer is referenced individually, PIT1 should be PIT0, PIT2 should be PIT1, PIT3 should be PIT2, and PIT4 should be PIT3. Other chapters in the user's manual use the correct nomenclature: PIT0–PIT3.</td></tr>
<tr><td>19.6.3/19-7</td><td>Change timeout period equation to the equation below.
$\text{Timeout period} = \frac{\text{PRE[3:0]} \times (\text{PM[15:0]} + 1) \times 2}{\text{system clock}}$</td></tr>
<tr><td>Figure 23-11</td><td>Change UISR bits 5–3 to reserved bits</td></tr>
<tr><td>24.6.1/24-11</td><td>Change 'I2CR = 0xA' to 'I2CR = 0xA0.'</td></tr>
<tr><td>27.2.1/27-2</td><td>Change 'When interfacing to 16-bit ports, the port C and D pins and PJ[7:6] (BS[3:2]) can be configured as general-purpose input/output (I/O)'
To 'When interfacing to 16-bit ports, the port C and D pins and PJ[5:4] (BS[1:0]) can be configured as general-purpose input/output (I/O)'</td></tr>
<tr><td>32.2/32-7</td><td>Added additional device number order information to Table 32-2.</td></tr>
</table>

Table 32-2. Orderable Part Numbers

Motorola Part Number	Description	Speed	Temperature
MCF5280CVF66	MCF5280 RISC Microprocessor, 256 MAPBGA	66.67 MHz	-40° to +85° C
MCF5280CVF80	MCF5280 RISC Microprocessor, 256 MAPBGA	80 MHz	-40° to +85° C
MCF5281CVF66	MCF5281 RISC Microprocessor, 256 MAPBGA	66.67 MHz	-40° to +85° C
MCF5281CVF80	MCF5281 RISC Microprocessor, 256 MAPBGA	80 MHz	-40° to +85° C
MCF5282CVF66	MCF5282 RISC Microprocessor, 256 MAPBGA	66.67 MHz	-40° to +85° C
MCF5282CVF80	MCF5282 RISC Microprocessor, 256 MAPBGA	80 MHz	-40° to +85° C

<table>
<tr><td>Chapter 33</td><td>Delete references to 'TA = TL to TH'.</td></tr>
<tr><td>Table 33-1/33-1</td><td>The Digital Input Voltage (V_{IN}) absolute maximum rating should be -0.3 to 6.0 V</td></tr>
<tr><td>Table 33-6/33-8</td><td>The normal operation analog supply current (I_{DDA}) maximum value has been changed to 5.0 mA.</td></tr>
</table>

Table 4. MCF5282UM Rev 1.0 Errata (continued)

Location	Description
Figure 33-5/33-16	Replace Figure 33-5, ‘SDRAM Read Cycle’ with the figure below.
Table 14-3/14-11	Change ‘Internal Pull-Up’ column to pull-up indications in the table below.

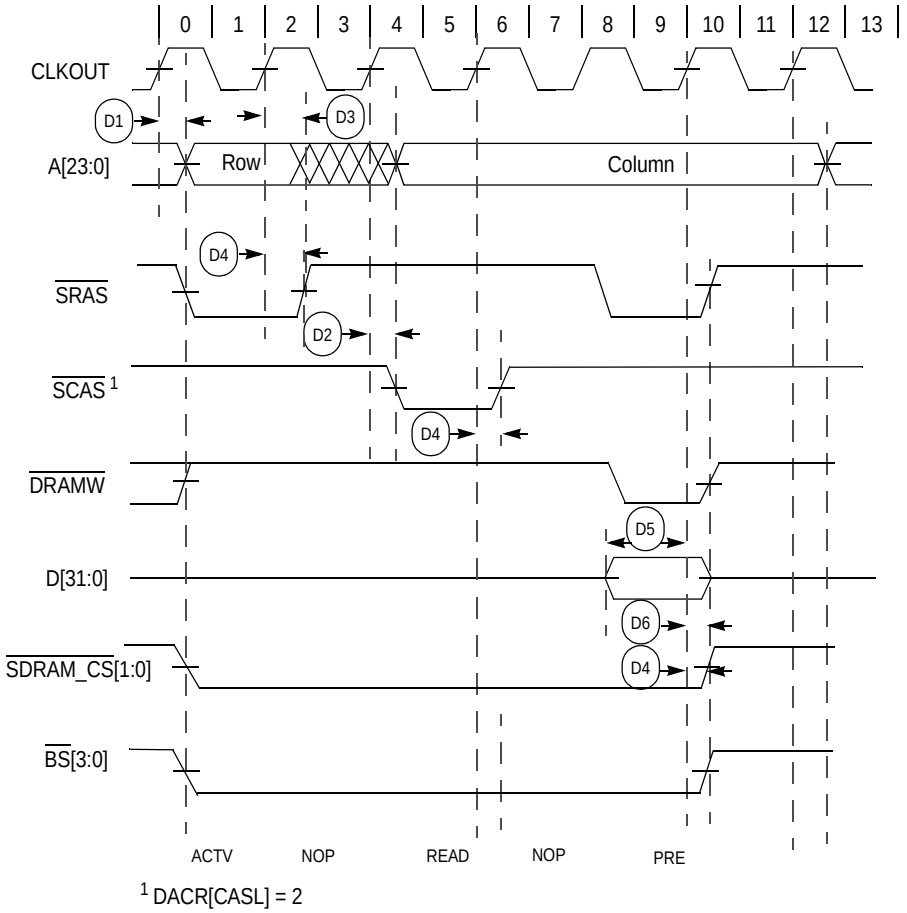


Figure 33-5. SDRAM Read Cycle

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
Reset						
R11	$\overline{\text{RSTI}}$	—	—	Reset in	I	Yes
P11	$\overline{\text{RSTO}}$	—	—	Reset out	O	—
Clock						
T8	EXTAL	—	—	External clock/crystal in	I	—

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
R8	XTAL	—	—	Crystal drive	O	—
N7	CLKOUT	—	—	Clock out	O	—
Chip Configuration/Mode Selection						
R14	CLKMOD0	—	—	Clock mode select	I	Yes
T14	CLKMOD1	—	—	Clock mode select	I	Yes
T11	$\overline{\text{RCON}}$	—	—	Reset configuration enable	I	Yes
H1	D26	PA2	—	Chip mode	I/O	—
K2	D17	PB1	—	Chip mode	I/O	—
K3	D16	PB0	—	Chip mode	I/O	—
J4	D19	PB3	—	Boot device/data port size	I/O	—
K1	D18	PB2	—	Boot device/data port size	I/O	—
J2	D21	PB5	—	Output pad drive strength	I/O	—
External Memory Interface and Ports						
C6:B6:A5	A[23:21]	PF[7:5]	$\overline{\text{CS}}$[6:4]	Address bus	O	Yes
C4:B4:A4:B3:A3	A[20:16]	PF[4:0]	—	Address bus	O	Yes
A2:B1:B2:C1: C2:C3:D1:D2	A[15:8]	PG[7:0]	—	Address bus	O	Yes
D3:D4:E1:E2: E3:E4:F1:F2	A[7:0]	PH[7:0]	—	Address bus	O	Yes
F3:G1:G2:G3: G4:H1:H2:H3	D[31:24]	PA[7:0]	—	Data bus	I/O	—
H4:J1:J2:J3: J4:K1:K2:K3	D[23:16]	PB[7:0]	—	Data bus	I/O	—
L1:L2:L3:L4: M1:M2:M3:M4	D[15:8]	PC[7:0]	—	Data bus	I/O	—
N1:N2:N3:P1: N5:T6:R6:P6	D[7:0]	PD[7:0]	—	Data bus	I/O	—
P14:T15:R15:R16	$\overline{\text{BS}}$[3:0]	PJ[7:4]	—	Byte strobe	I/O	Yes
N16	$\overline{\text{OE}}$	PE7	—	Output enable	I/O	—
P16	$\overline{\text{TA}}$	PE6	—	Transfer acknowledge	I/O	Yes
P15	$\overline{\text{TEA}}$	PE5	—	Transfer error acknowledge	I/O	Yes
N15	R/$\overline{\text{W}}$	PE4	—	Read/write	I/O	Yes
N14	SIZ1	PE3	SYNCA	Transfer size	I/O	Yes[3]

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
M16	SIZ0	PE2	SYNCB	Transfer size	I/O	Yes[4]
M15	$\overline{TS}$	PE1	SYNCA	Transfer start	I/O	Yes
M14	$\overline{TIP}$	PE0	SYNCB	Transfer in progress	I/O	Yes
Chip Selects						
L16:L15:L14:L13	$\overline{CS}$[3:0]	PJ[3:0]	—	Chip selects 3-0	I/O	Yes
C6:B6:A5	A[23:21]	PF[7:5]	$\overline{CS}$[6:4]	Chip selects 6-4	O	Yes
SDRAM Controller						
H15	$\overline{SRAS}$	PSD5	—	SDRAM row address strobe	I/O	—
H16	$\overline{SCAS}$	PSD4	—	SDRAM column address strobe	I/O	—
G15	$\overline{DRAMW}$	PSD3	—	SDRAM write enable	I/O	—
H13:G16	$\overline{SDRAM\_CS}$[1:0]	PSD[2:1]	—	SDRAM chip selects	I/O	—
H14	SCKE	PSD0	—	SDRAM clock enable	I/O	—
External Interrupts Port						
B15:B16:C14:C15: C16: D14:D15	$\overline{IRQ}$[7:1]	PNQ[7:1]	—	External interrupt request	I/O	—
Ethernet						
C10	EMDIO	PAS5	URXD2	Management channel serial data	I/O	—
B10	EMDC	PAS4	UTXD2	Management channel clock	I/O	—
A8	ETXCLK	PEH7	—	MAC Transmit clock	I/O	—
D6	ETXEN	PEH6	—	MAC Transmit enable	I/O	—
D7	ETXD0	PEH5	—	MAC Transmit data	I/O	—
B11	ECOL	PEH4	—	MAC Collision	I/O	—
A10	ERXCLK	PEH3	—	MAC Receive clock	I/O	—
C8	ERXDV	PEH2	—	MAC Receive enable	I/O	—
D9	ERXD0	PEH1	—	MAC Receive data	I/O	—
A11	ECRS	PEH0	—	MAC Carrier sense	I/O	—
A7:B7:C7	ETXD[3:1]	PEL[7:5]	—	MAC Transmit data	I/O	—
D10	ETXER	PEL4	—	MAC Transmit error	I/O	—
A9:B9:C9	ERXD[3:1]	PEL[3:1]	—	MAC Receive data	I/O	—
B8	ERXER	PEL0	—	MAC Receive error	I/O	—

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
FlexCAN						
D16	CANRX	PAS3	URXD2	FlexCAN Receive data	I/O	—
E13	CANTX	PAS2	UTXD2	FlexCAN Transmit data	I/O	—
I^2C						
E14	SDA	PAS1	URXD2	I^2C Serial data	I/O	Yes[5]
E15	SCL	PAS0	UTXD2	I^2C Serial clock	I/O	Yes[6]
QSPI						
F13	QSPI_DOUT	PQS0	—	QSPI data out	I/O	—
E16	QSPI_DIN	PQS1	—	QSPI data in	I/O	—
F14	QSPI_CLK	PQS2	—	QSPI clock	I/O	—
G14:G13:F16:F15	QSPI_CS[3:0]	PQS[6:3]	—	QSPI chip select	I/O	—
UARTs						
R7	URXD1	PUA3	—	U1 receive data	I/O	—
P7	UTXD1	PUA2	—	U1 transmit data	I/O	—
N6	URXD0	PUA1	—	U0 receive data	I/O	—
T7	UTXD0	PUA0	—	U0 transmit data	I/O	—
C10	EMDIO	PAS5	URXD2	U2 receive data	I/O	—
B10	EMDC	PAS4	UTXD2	U2 transmit data	I/O	—
D16	CANRX	PAS3	URXD2	U2 receive data	I/O	—
E13	CANTX	PAS2	UTXD2	U2 transmit data	I/O	—
E14	SDA	PAS1	URXD2	U2 receive data	I/O	Yes[5]
E15	SCL	PAS0	UTXD2	U2 transmit data	I/O	Yes[6]
K16	DTIN3	PTC3	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	U1/U0 Request to Send	I/O	—
K15	DTOUT3	PTC2	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	U1/U0 Request to Send	I/O	—
K14	DTIN2	PTC1	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	U1/U0 Clear to Send	I/O	—
K13	DTOUT2	PTC0	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	U1/U0 Clear to Send	I/O	—
J16	DTIN1	PTD3	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	U1/U0 Request to Send	I/O	—

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
J15	DTOUT1	PTD2	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	U1/U0 Request to Send	I/O	—
J14	DTIN0	PTD1	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	U1/U0 Clear to Send	I/O	—
J13	DTOUT0	PTD0	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	U1/U0 Clear to Send	I/O	—
General Purpose Timers						
T13:R13:P13:N13	GPTA[3:0]	PTA[3:0]	—	Timer A IC/OC/PAI	I/O	Yes
T12:R12:P12:N12	GPTB[3:0]	PTB[3:0]	—	Timer B IC/OC/PAI	I/O	Yes
N14	SIZ1	PE3	SYNCA	Timer A synchronization input	I/O	Yes[3]
M16	SIZ0	PE2	SYNCB	Timer B synchronization input	I/O	Yes[4]
M15	$\overline{\text{TS}}$	PE1	SYNCA	Timer A synchronization input	I/O	Yes
M14	$\overline{\text{TIP}}$	PE0	SYNCB	Timer B synchronization input	I/O	Yes
DMA Timers						
K16	DTIN3	PTC3	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	Timer 3 in	I/O	—
K15	DTOUT3	PTC2	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	Timer 3 out	I/O	—
K14	DTIN2	PTC1	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	Timer 2 in	I/O	—
K13	DTOUT2	PTC0	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	Timer 2 out	I/O	—
J16	DTIN1	PTD3	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	Timer 1 in	I/O	—
J15	DTOUT1	PTD2	$\overline{\text{URTS1}}$/ $\overline{\text{URTS0}}$	Timer 1 out	I/O	—
J14	DTIN0	PTD1	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	Timer 0 in	I/O	—
J13	DTOUT0	PTD0	$\overline{\text{UCTS1}}$/ $\overline{\text{UCTS0}}$	Timer 0 out	I/O	—
Queued Analog-to-Digital Converter (QADC)						
T3	AN0	PQB0	ANW	Analog channel 0	I/O	—
R2	AN1	PQB1	ANX	Analog channel 1	I/O	—
T2	AN2	PQB2	ANY	Analog channel 2	I/O	—
R1	AN3	PQB3	ANZ	Analog channel 3	I/O	—

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
R4	AN52	PQA0	MA0	Analog channel 52	I/O	—
T4	AN53	PQA1	MA1	Analog channel 53	I/O	—
P3	AN55	PQA3	ETRIG1	Analog channel 55	I/O	—
R3	AN56	PQA4	ETRIG2	Analog channel 56	I/O	—
P4	VRH	—	—	High analog reference	I	—
T5	VRL	—	—	Low analog reference	I	—
Debug and JTAG Test Port Control						
R9	JTAG_EN	—	—	JTAG Enable	I	—
P9	DSCLK	$\overline{\text{TRST}}$	—	Debug clock / TAP reset	I	Yes[7]
T9	TCLK	—	—	TAP clock	I	Yes[7]
P10	$\overline{\text{BKPT}}$	TMS	—	Breakpoint/TAP test mode select	I	Yes[7]
R10	DSI	TDI	—	Debug data in / TAP data in	I	Yes[7]
T10	DSO	TDO	—	Debug data out / TAP data out	O	—
C12:D12:A13:B13	DDATA[3:0]	PDD[7:4]	—	Debug data	I/O	—
C13:A14:B14:A15	PST[3:0]	PDD[3:0]	—	Processor status data	I/O	—
Test						
N10	TEST	—		Test mode pin	I	—
Power Supplies						
R5	VDDA	—	—	Analog positive supply	I	—
P5:T1	VSSA	—	—	Analog ground	I	—
P2	VDDH	—	—	ESD positive supply	I	—
N8	VDDPLL	—	—	PLL positive supply	I	—
P8	VSSPLL	—	—	PLL ground	I	—
A6:C11	VPP	—	—	Flash (stress) programming voltage	I	—
A12:C5:D5:D11	VDDF	—	—	Flash positive supply	I	—
B5:B12:	VSSF	—	—	Flash module ground	I	—
N11	VSTBY	—	—	Standby power	I	—

Table 14-3. MCF5282 Signals and Pin Numbers Sorted by Function (continued)

MAPBGA Pin	Pin Functions			Description	Primary I/O	Internal Pull-up [1]
	Primary[2]	Secondary	Tertiary			
E6-E11:F5:F7-F10: F12:G5:G6:G11: G12:H5:H6:H11: H12:J5:J6:J11:J12: K5:K6:K11:K12:L5: L7-L10:L12: M6-M11	VDD	—	—	Positive supply	I	—
A1:A16:E5:E12:F6: F11:G7-G10:H7-H10: J7-J10:K7-K10:L6: L11:M5:M12:T16	VSS	—	—	Ground	I	—

NOTES:
1 Pull-ups are not active when GPIO functions are selected for the pins.
2 The primary functionality of a pin is not necessarily its default functionality. Pins that have GPIO functionality will default to GPIO inputs.
3 Pull-up is active only with the SYNCA function.
4 Pull-up is active only with the SYNCB function.
5 Pull-up is active only with the SDA function.
6 Pull-up is active only with SCL function.
7 Pull-up is active when JTAG_EN is driven high.

5 Revision History

Table 5 provides a revision history for this document.

Table 5. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	Initial release.	07/2003
1	Added page erase verify errata for Chapter 6, “ColdFire Flash Module (CFM).”	09/2003
2	• Added errata for UART interrupt status register. • Added errata for PIT timer timeout equation. • Added I2CR write errata. • Added errata for ‘Internal Pull-Up’ column in ‘MCF5282 Signals and Pin Numbers Sorted by Function’ table. • Added errata for “SDRAM Read Cycle’ figure.	11/2003
3	• Added errata for Chapter 19. PIT1–PIT4 should be PIT0–PIT3.	01/2004
4	• Added errata for spurious interrupt. • Added errata for Table 33-8. Single instance of $T_A = T_L$ to T_H was overlooked in revision 2.0 of the manual. This instance has now been removed.	03/2004
5	• Added errata for Section 25.4.10: change CANICR to ICR*n.* • Added errata for BITERR and ACKERR field descriptions. • Added errata for BOFFINT and ERRINT bit sequence. • Added errata for BUF*n*I field description.	03/2004

Table 5. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
6	• Added errata for Table 17-2 • Added errata for FRSR register diagram	11/2004
7	• Added errata for Figure 4-2, Table 4-6, Figure 6-3, and Table 6-10	11/2004
Added the below errata for MCF5282UM Rev 2.3		
8	• Added FEC max buffer size errata. • Added VDD/VDDH power-up requirement. • Added MFD bit definition footnote errata. • Added PLL spec table entries for 66MHz device.	01/2005
9	• Added INTFRCL*n* figure errata. • Added BAM bit field example errata.	03/2005
10	• Added SDRAM NOP command errata. • Added UART clock source errata.	07/2005
11	• Added PRI1/PRI2 text description errata. • Added CSMR1/CSCR1 register address errata. • Removed Table 23-5 errata that was added in revision 10 of this document, as it was incorrect. Only the internal UART clock source is prescaled by the 16-bit divider. • Added 2 UART external clock source errata, removing the 16-bit divider from a figure and equation.	08/2005
12	• Added core watchdog unable to reset the device errata. • Added EMRBR register address errata. • Added I_{OH} and I_{OL} errata.	12/2005
13	• Added FlexCAN flag clearing mechanism errata in interrupt controller. • Added FlexCAN ESTAT register description errata for various bits. • Added ICR*n*x note regarding unique and non-overlapping level and priority definitions. • Added DTOUT1, DTIN0, DTOUT0 description field errata in GPIO chapter. • Added FEC MII transmit and receive specification section errata.	08/2006
14	• Deleted reference to nonexistent CF bits in the figure and bit descriptions for the GPTFLG2 register. • Added RMON_R_DROP counter errata.	11/2006
15	• Added various core, EMAC, cache, SRAM and debug chapter errata. • Added V_{IH} and V_{IL} crystal mode spec changes. • Added DACR*n*[CBM] field description note. • Added FEC MIB counter memory map errata. • Added “Duplicate Frame Transmission” section to FEC chapter. • Added DMA SAA bit errata. • Added global IACK register space errata.	05/2007

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