

FM480

User Manual

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Revision History

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1 Acronyms and related documents

1.1 Acronyms

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DCI	Digitally Controlled Impedance
DDR	Double Data Rate
DSP	Digital Signal Processing
EPROM	Erasable Programmable Read-Only Memory
FBGA	Fineline Ball Grid Array
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
JTAG	Join Test Action Group
LED	Light Emitting Diode
LVTTL	Low Voltage Transistor Logic level
LVDS	Low Differential Data Signaling
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory
SRAM	Synchronous Random Access memory

Table 1: Glossary

1.2 Related Documents

- IEEE Std 1386.1-2001 : IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC).
- ANSI/VITA 39-2003 : PCI-X for PMC and Processor PMC.
- ANSI/VITA 20-2001 : Conduction Cooled PMC.
- IEEE Std 1386-2001 : IEEE Standard for a Common Mezzanine Card (CMC) Family.
- [Xilinx Virtex-4 user guide](#)
- [Xilinx PCI-X core datasheet](#)

1.3 General description

The FM480 is a high performance PMC dedicated to digital signal processing applications with high bandwidth and complex algorithms requirements. PCI-X and PCI backward compatible, the FM480 offers various interfaces, fast on-board memory resources and one Virtex-4 FPGA. It can be utilized, for example, to accelerate frequency-domain algorithms with off-the-shelf Intellectual Property cores for applications that require the highest level of performances. The FM480 is mechanically and electrically compliant to the standard and specifications listed in section 1.2 of this document.

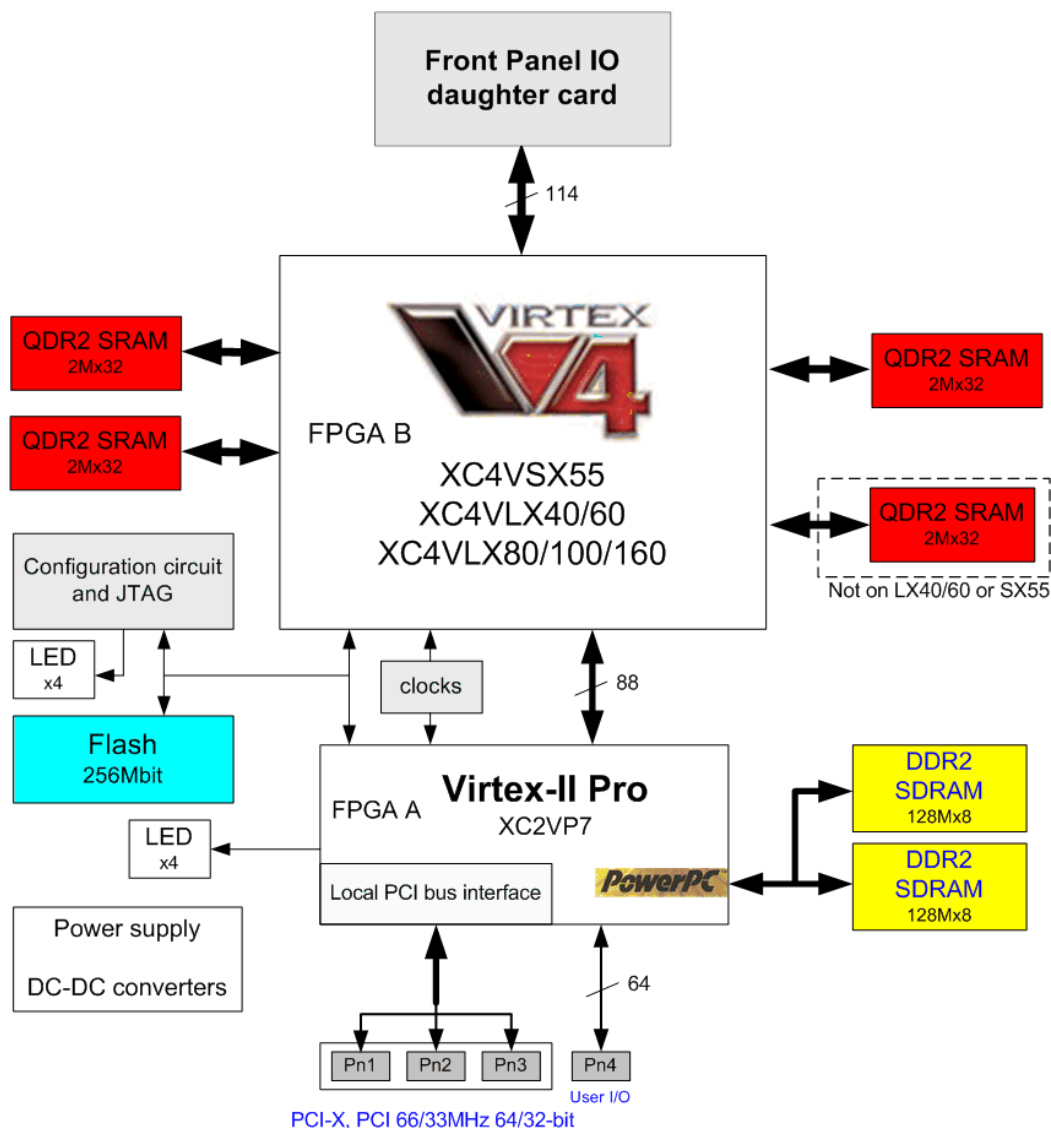


Figure 1: FM480 block diagram

2 Installation

2.1 Requirements and handling instructions

- The FM480 must be installed on a motherboard compliant to the IEEE Std 1386-2001 standard for 3.3V PMC
- Do not flex the board
- Observe SSD precautions when handling the board to prevent electrostatic discharges.
- Do not install the FM480 while the motherboard is powered up.

2.2 Firmware and software

Drivers, API libraries and a program example working in combination with a pre-programmed firmware for both FPGAs are provided. The FM480 is delivered with an interface to the Xilinx PCI core in the Virtex-II Pro device and an example VHDL design in the Virtex-4 device so users can start performing high bandwidth data transfers over the PCI bus right out of the box. For more information about software installation and FPGA firmware, please refer the FM480 Get Started Guide.

3 Design

3.1 FPGA devices

The Virtex-II Pro and Virtex-4 FPGA devices interface to the various resources on the FM480 as shown on Figure 1. They also interconnect to each other via 86 general purpose pins and 2 clock pins.

3.1.1 Virtex-II Pro device A

3.1.1.1 Virtex-II Pro device A family and package

The Virtex-II Pro device is a XC2VP7 in a Finline Ball Grid array with 672 balls (FF672).

3.1.1.2 Power PC embedded processor

One IBM PowerPC RISC processor cores is available in the Virtex-II Pro device A. This core can be used to execute C based algorithms and control the logic resources implemented in the FPGA.

3.1.1.3 Virtex-II Pro device A external memory interfaces

The Virtex-II Pro device A is connected to two 128Mbytes SDRAM devices with 16-bit data bus width. These memory resources can be used by the PowerPC core or can serve as data buffers.

3.1.1.4 PCI interface

The Virtex-II Pro device A interfaces directly to the PCI bus via the PMC P1n, P2n and P3n connectors. An embedded PCI core from Xilinx is used to communicate over the PCI bus with the host system on the motherboard. PCI-X 64-bit 66MHz/133MHz, PCI 64-bit 66MHz

and PCI 32-bit 33MHz are supported on the FM480. The bus type must be communicated at the time of the order so the right Virtex-II Pro firmware can be loaded into the flash prior delivery.

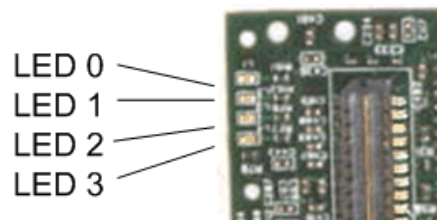
The following performances have been recorded with the FM480 transferring data on the bus:

- **PCI-X 64-bit 133MHz: 650Mbytes/s sustained**
- **PCI-X 64-bit 66MHz: 450Mbytes/s sustained**
- **PCI 32-bit 33MHz: 120Mbytes/s sustained**

3.1.1.5 LED

Four LEDs are connected to the Virtex-II Pro device. In the default FPGA firmware, the LEDs are driven by the Virtex-4 device via the Virtex-II Pro / Virtex-4 interface.

The LEDs are located on side 2 of the PCB in the front panel area.



3.1.1.6 Pn4 user I/O connector

The 64-pin Pn4 connector is wired to the Virtex-II Pro device A. All signals are user-defined 3.3V LVTTLL.

Connector pin	Signal name	FPGA pin		FPGA pin	Signal name	Connector pin
1	Pn4_IO0	P2		P3	Pn4_IO1	2
3	Pn4_IO2	P4		P5	Pn4_IO3	4
5	Pn4_IO4	P6		P7	Pn4_IO5	6
7	Pn4_IO6	R1		R2	Pn4_IO7	8
9	Pn4_IO8	R3		R4	Pn4_IO9	10
11	Pn4_IO10	R5		R6	Pn4_IO11	12
13	Pn4_IO12	P8		R8	Pn4_IO13	14
15	Pn4_IO14	T1		T2	Pn4_IO15	16
17	Pn4_IO16	T3		T4	Pn4_IO17	18
19	Pn4_IO18	T5		T6	Pn4_IO19	20
21	Pn4_IO20	R7		T7	Pn4_IO21	22
23	Pn4_IO22	T8		U7	Pn4_IO23	24
25	Pn4_IO24	U1		V1	Pn4_IO25	26
27	Pn4_IO26	U3		U4	Pn4_IO27	28
29	Pn4_IO28	U5		U6	Pn4_IO29	30
31	Pn4_IO30	V2		V3	Pn4_IO31	32
33	Pn4_IO32	V4		V5	Pn4_IO33	34
35	Pn4_IO34	V6		V7	Pn4_IO35	36
37	Pn4_IO36	W1		W2	Pn4_IO37	38
39	Pn4_IO38	W3		W4	Pn4_IO39	40
41	Pn4_IO40	W5		W6	Pn4_IO41	42
43	Pn4_IO42	Y1		AA1	Pn4_IO43	44
45	Pn4_IO44	Y3		Y4	Pn4_IO45	46
47	Pn4_IO46	Y5		Y6	Pn4_IO47	48
49	Pn4_IO48	N7		N6	Pn4_IO49	50
51	Pn4_IO50	N5		N4	Pn4_IO51	52
53	Pn4_IO52	N3		N2	Pn4_IO53	54
55	Pn4_IO54	AB3		AB4	Pn4_IO55	56
57	Pn4_IO56	AC1		AC2	Pn4_IO57	58
59	Pn4_IO58	AD1		AD2	Pn4_IO58	60
61	Pn4_IO60	AE1		AF2	Pn4_IO59	62
63	Pn4_IO62	AC3		AD4	Pn4_IO60	64

Table 2 : Pn4 pin assignment

3.1.2 Virtex-4 device B

3.1.2.1 Virtex-4 device B family and package

The Virtex-4 device B is dedicated to Digital Signal Processing applications and can be chosen from the SX or LX family devices. Its package is based on Fineline Ball Grid array with 1148 balls. In terms of logic and dedicated DSP resources, it is available in 5 different sizes: SX55, LX40, LX60, LX80, LX100 and LX160. The speed grade and temperature operating range can be chosen upon customer requirements.

3.1.2.2 Virtex-4 device B external memory interfaces

The Virtex-4 device B interfaces to four 8Mbytes QDR2 SRAM devices with 32-bit data bus, Please note that the four QDR2 SRAM devices are only available with the LX80, LX100 and LX160 devices. For smaller Virtex-4 FPGAs (LX40, LX60 and SX55) only three QDR2 SRAM devices are connected to the FPGA.

3.1.2.3 Virtex-4 device B interface to Front Panel daughter card

The Virtex-4 device B interfaces to the front panel daughter card on the FM480 via a high speed connector. 120 I/Os are available from the FPGA to/from the daughter card.

Refer to the Front Panel I/O section of this document for more details about the daughter card connector electrical characteristics.

3.2 FPGA devices configuration

3.2.1 Flash storage

The FPGA firmware is stored on board in a flash device. The 256Mbit device is partly used to store the configuration for both FPGAs. In the default CPLD firmware configuration, the Virtex-II Pro and Virtex-4 devices are directly configured from flash if a valid bitstream is stored in the flash for each FPGA. The flash is pre-programmed in factory with the default Virtex-II pro firmware and a Virtex-4 firmware example.

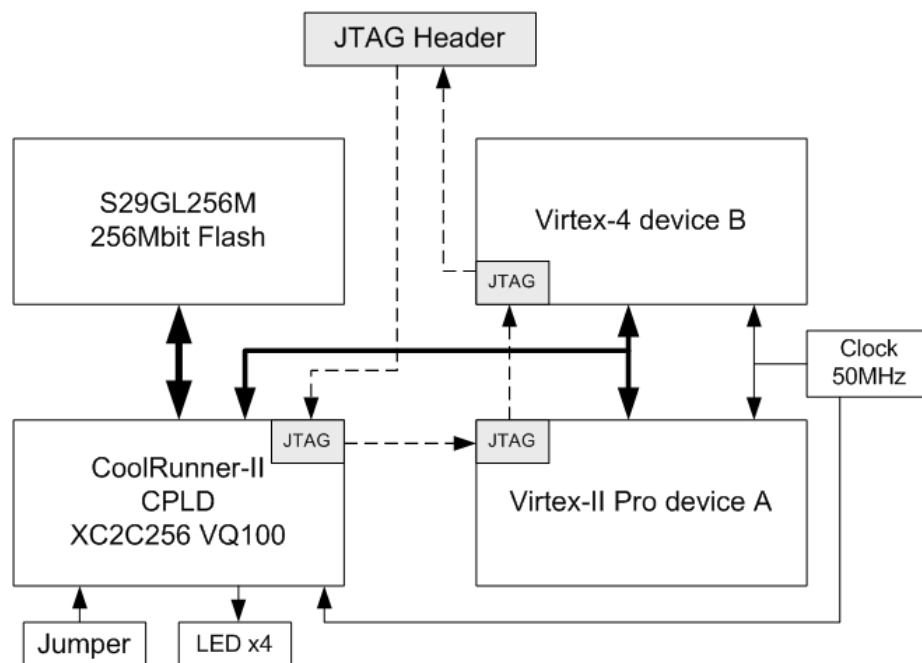


Figure 2 : Configuration circuit

3.2.2 CPLD device

As shown on Figure 2, a CPLD is present on board to interface between the flash device and the FPGA devices. It is of type CoolRunner-II. The CPLD is used to program and read the flash. The data stored in the flash are transferred from the host motherboard via the PCI bus to the Virtex-II Pro device A and then to the CPLD that writes the required bit stream to the storage device. A 50 MHz clock connects to the CPLD and is used to generate the configuration clock sent to the FPGA devices. At power up, if the CPLD detects that an FPGA configuration bitstream is stored in the flash for both FPGA devices, it will start reading programming the devices in SelecMap mode.

Do NOT reprogram the CPLD without 4DSP approval

The CPLD configuration is achieved by loading with a Xilinx download cable a bitstream from a host computer via the JTAG connector. The FPGA devices configuration can also be performed using the JTAG.

3.2.2.1 Jumper

A Jumper (J1) is connected to the CPLD and is used to choose the FPGA configuration scheme. The jumper is located next to the Pn3 connector. The Jumper positions are defined as follows.

ON	JTAG chain enabled for FPGAs configuration, FPGAs are not configured from the flash
OFF	Configuration from the flash enabled if valid FPGA bitstreams are stored in the flash
OFF to ON	The Virtex-II Pro safety configuration is loaded from the Flash into the Virtex-II Pro. This scheme is to be used only to allow a user to reprogram the flash with valid FPGA bitstreams.

Table 3: Jumper

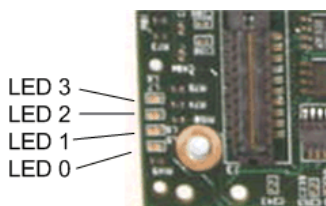
3.2.2.2 LED and board status

Four LEDs connect to the CPLD and give information about the board status.

LED 1	Blinking	FPGA A or B bitstream or user_ROM_register is currently being written to the flash
	ON	FPGA A not configured
	OFF	FPGA A configured
LED 2	Blinking	FPGA A or B bitstream or user_ROM_register is currently being written to the flash
	ON	FPGA B not configured
	OFF	FPGA devices configured
LED 3	Blinking	The Virtex-II Pro FPGA has been configured with the safety configuration bitstream programmed in the flash at factory. Please write a valid Virtex-II Pro bitstream in the flash.
	ON	Flash is busy writing or erasing
	OFF	Flash device is not busy
LED 4	ON	CRC error. Presumably a wrong or corrupted FPGA bitstream has been written to the flash. Once on this LED remains on
	OFF	No CRC error detected

Table 4: LED board status

The LEDs are located on side 2 of the PCB in the front panel area.



3.2.3 JTAG

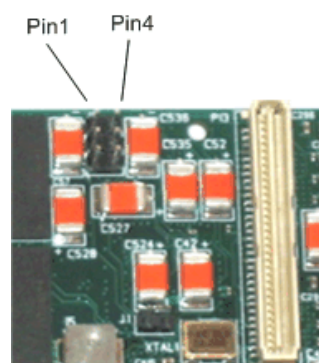
A JTAG connector is available on the FM480 for configuration purposes. The JTAG can also be used to debug the FPGA design with the Xilinx Chipscope.

Please note that three Xilinx devices will be detected in the JTAG chain. The JTAG connector is located on side 1 of the PCB in front of Pn3.

The JTAG connector pinout is as follows:

Pin #	Signal	Signal	Pin #
1	1.8V	TMS	4
2	GND	TDI	5
3	TCK	TDO	6

Table 5 : JTAG pin assignment



3.3 Clocks

A 50MHz oscillator on-board connects to a low skew 1:4 clock buffer (ICS553). Each FPGA device and the CPLD receive this 50MHz clock. By using the DCM resources inside the FPGA, clocks are generated for the various interfaces on board. Figure 2 shows how the clocks signals between the FPGAs and the CPLD are connected. The IO pin number is provided for each device.

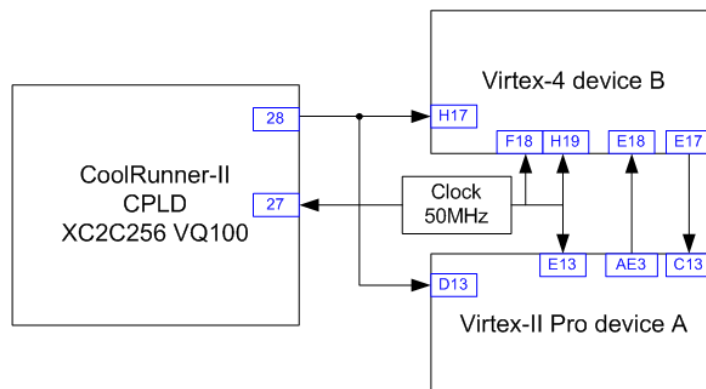


Figure 3 : Clocks

3.4 Memory resources

3.4.1 QDR2 SRAM

Four independant QDR2 SRAM devices are connected to the Virtex-4 device B. The QDR2 SRAM devices available on the FM480 are 2M words deep (8Mbytes per memory device).

Please note that only three QDR SRAM devices are available to the user if the XC4VLX40, XC4VLX60 or XC4VSX55 FPGA device is mounted on board.

3.4.2 DDR2 SDRAM

Two 8-bit DDR2 SDRAM devices are connected to Virtex-II Pro device A. The two memories share a common address bus and can be considered as a single DDR2 SDRAM bank of 128Mbytes with a 16-bit data bus width. These memory resources are primarily intended to be accessed by the PowerPC processor in the Virtex-II Pro device A. They can however be used for any purpose.

3.5 Front Panel IO daughter card

3.5.1 Virtex-4 device B to I/O front Panel daughter card

(only available with daughter card purchase)

The Virtex-4 device B interfaces to a 120-pin connector placed in the Front panel I/O area (on both side 1 and side 2 of the PCB). It serves as a base for a daughter card and offers I/O diversity to the FM480 PMC. On side 2 of the PCB, the connectors and mounting holes placement complies with the SLB standard except for the 2.5V mounting holes that are not present on this module.

The FPGA I/O banks are powered either by 1.8V, 2.5V or 3.3V. Using the Xilinx DCI termination options to match the signals impedance allows many electrical standards to be supported by this interface. All signals are routed as 100-ohm LVDS pairs. The VRP and VRN pins on the I/O banks connected to the daughter card connector are respectively pulled up and pulled down with 50-ohm resistors in order to ensure optimal performances when using the Xilinx DCI options. The VREF pins are connected to 0.85V for DDR2 DCI terminations. Please, contact 4DSP Inc. for more information about the daughter card types available.

The 120-pin Samtec connector pin assignment is as follows. All signals are shown as LVDS pairs in the table but they can be used for any standard that does not breach the electrical rules of the Xilinx I/O pad.

Connector pin	Signal Name	FPGA pin		FPGA pin	Signal name	Connector pin
1	FP_P0	W24		AA23	FP_P1	2
3	FP_N0	Y24		AA24	FP_N1	4
5	FP_P2 ⁽²⁾	AA25		AA28	FP_P3	6
7	FP_N2 ⁽²⁾	AA26		AA29	FP_N3	8
9	FP_P4	AB30		AC28	FP_P5	10
11	FP_N4	AA30		AB28	FP_N5	12
13	FP_P6	AB22		AD27	FP_P7	14
15	FP_N6	AB23		AC27	FP_N7	16
17	FP_P8	AC29		AC32	FP_P9	18
19	FP_N8	AC30		AC33	FP_N9	20
21	FP_P10 ⁽²⁾	AD34		AE32	FP_P11	22
23	FP_N10 ⁽²⁾	AC34		AD32	FP_N11	24
25	FP_P12	AE29		AF31	FP_P13	26
27	FP_N12	AD29		AE31	FP_N13	28
29	FP_P14	AE33		AF33	FP_P15	30
31	FP_N14	AE34		AF34	FP_N15	32
33	FP_P16 ⁽¹⁾	AH19		AF29	FP_P17 ⁽²⁾	34
35	FP_N16 ⁽¹⁾	AH18		AF30	FP_N17 ⁽²⁾	36
37	FP_P18 ⁽¹⁾	AG18		AG30	FP_P19	38
39	FP_N18 ⁽¹⁾	AG17		AG31	FP_N19	40

Table 6 : Front Panel IO daughter card pin assignment Bank A

⁽¹⁾ Connected to a global clock pin on the FPGA. LVDS output not supported.

⁽²⁾ Connected to a regional clock pin on the FPGA. LVDS output not supported.

Connector pin	Differential	FPGA pin	FPGA pin	Differential	Connector pin
41	FP_P20	AG32	AJ34	FP_P21	42
43	FP_N20	AG33	AH34	FP_N21	44
45	FP_P22	AH32	AJ30	FP_P23	46
47	FP_N22	AH33	AH30	FP_N23	48
49	FP_P24 ⁽²⁾	AK31	AK33	FP_P25	50
51	FP_N24 ⁽²⁾	AK32	AK34	FP_N25	52
53	FP_P26	AL33	AM31	FP_P27	54
55	FP_N26	AL34	AL31	FP_N27	56
57	FP_P28	AM32	AP30	FP_P29	58
59	FP_N28	AM33	AN30	FP_N29	60
61	FP_P30	AM30	AH28	FP_P31	62
63	FP_N30	AL30	AH29	FP_N31	64
65	FP_P32	AK29	AL28	FP_P33	66
67	FP_N32	AJ29	AL29	FP_N33	68
69	FP_P34	AP29	AN28	FP_P35 ⁽²⁾	70
71	FP_N34	AN29	AM28	FP_N35 ⁽²⁾	72
73	FP_P36 ⁽²⁾	AG27	AG28	FP_N36 ⁽²⁾	74
75	3.3V/2.5V/1.8V			Vbatt ⁽³⁾	76
77	3.3V/2.5V/1.8V			0.9V	78
79	3.3V/2.5V/1.8V			3.3V/2.5V/1.8V	80
81	FP_P37	AF28	AJ27	FP_P38	82
83	FP_N37	AE27	AH27	FP_N38	84
85	FP_P39	AM26	AP27	FP_P40	86
87	FP_N39	AM27	AN27	FP_N40	88
89	FP_P41	AP25	AL26	FP_P42	90
91	FP_N41	AP26	AK26	FP_N42	92
93	FP_P43	AG25	AF26	FP_P44	94
95	FP_N43	AG26	AE26	FP_N44	96
97	FP_P45 ⁽²⁾	AL24	AN25	FP_P46	98
99	FP_N45 ⁽²⁾	AL25	AM25	FP_N46	100
101	FP_P47	AP24	AK24	FP_P48	102
103	FP_N47	AN24	AJ24	FP_N48	104
105	FP_P49	AG23	AK22	FP_P50	106
107	FP_N49	AF24	AK23	FP_N50	108
109	FP_P51	AL23	AN22	FP_P52	110
111	FP_N51	AM23	AN23	FP_N52	112
113	FP_P53 ⁽¹⁾	AJ17	AP21	FP_P54	114
115	FP_N53 ⁽¹⁾	AH17	AP22	FP_N54	116
117	FP_P55 ⁽¹⁾	AE17	AK21	FP_P56	118
119	FP_N55 ⁽¹⁾	AE16	AL21	FP_N56	120

Table 7 : Front Panel IO daughter card pin assignment Bank B and C

⁽¹⁾ Connected to a global clock pin on the FPGA. LVDS output not supported.

⁽²⁾ Connected to a regional clock pin on the FPGA. LVDS output not supported.

⁽³⁾ Vbatt is connected to Virtex-II Pro device A and Virtex-4 device B Vbatt pin.

3.5.2 Power connection to the front panel I/O daughtercard

The Front Panel I/O daughter card on side 1 of the PCB is powered via a 7-pin connector of type BKS (Samtec). Each pin can carry up to 1.5A. The power connector's pin assignment is as follows.

Pin #	Signal	Signal	Pin #
1	+3.3V	+3.3V	2
3	+5V	GND	4
5	+12V	GND	6
7	-12V		

Table 8: Daughter card power connector pin assignment on PMC side 1

On side 2 of the PCB, the daughter card is powered via a 33-pin connector of type BKS (Samtec). Each pin can carry up to 1.5A. The power connector's pin assignment is as follows.

Pin #	Signal	Signal	Pin #
1	+3.3V	GND	2
3	+3.3V	GND	4
5	+3.3V	GND	6
7	+3.3V	GND	8
9	+5V	GND	10
11	+5V	GND	12
13	+5V	GND	14
15	+5V	GND	16
17	+12V	GND	18
19	+12V	GND	20
21	-12V	GND	22
23	-12V	GND	24
25	GND	reserved	26
27	reserved	reserved	28
29	reserved	reserved	30
31	reserved	reserved	32
33	GND		

Table 9: Daughter card power connector pin assignment on PMC side 2

4 Power requirements

The Power is supplied to the FM480 via the PMC connectors. Several DC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board. Optionally, the FM480 can be used as a stand alone module and is powered via the external power connector. The FM480 power requirements are as follow.

Device/Interface	Voltage	Maximum current
DCI and memory reference voltage	0.85V	0.5 A
Virtex-4 device B core	1.2V	12A
Virtex-II Pro device A core	1.5V	6A
QDR2, DDR2 SDRAM core and I/O banks, Virtex-4 abd Virtex-II Pro devices I/O banks	1.8V	10A
Virtex-4 device B I/O bank connected to the front panel daughter card	1.8V/2.5V/3.3V	1.5A
Virtex-II Pro device A I/O bank connected to the PCI bus, Flash, CPLD, front Panel I/O daughter card	3.3V	2A
Front Panel IO daughter card	5V	1A
Front Panel IO daughter card	12V	0.5A
Front Panel IO daughter card	-12V	0.5A

Table 10 : Power supply

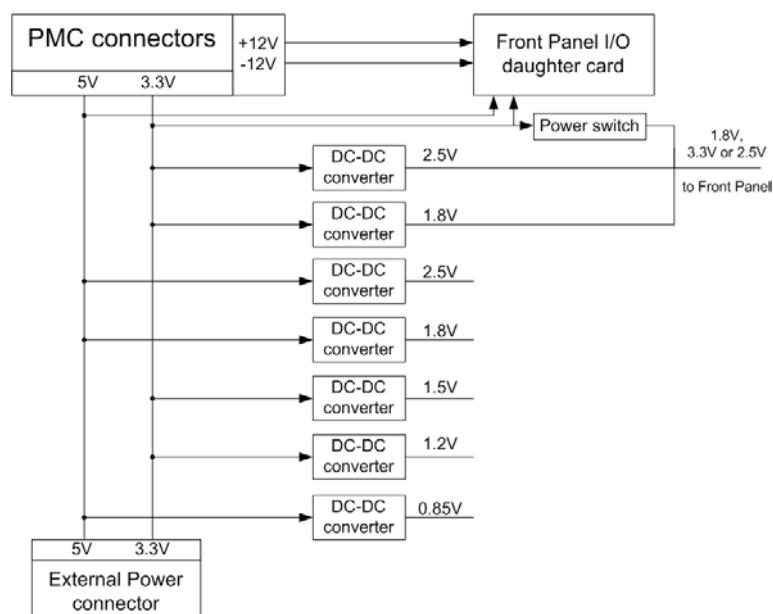


Figure 4 : Power supply

An ADT7411 device is used to monitor the power on the different voltage rails as well as the temperature. The ADT7411 data are constantly passed to the Virtex-II Pro device. Measurements can be accessed from the host computer via the PCI bus. A software utility delivered with the board allows the monitoring of the voltage on the 2.5V, 1.8V, 1.2V and 0.85V rails. It also displays the Virtex-4 junction temperature.

4.1 External power connector

An external power connector (J2) is available on side 2 of the PMC, next to the PMC connectors. It is used to power the board when it is in stand alone mode. This is a right angled connector and it will be mounted on board only if the card is ordered in its stand alone version (FM480-SA). The height and placement of this connector on the PCB breaches the PMC specifications and the module should not be used in an enclosed chassis compliant to PMC specifications if the external power connector is present on board.

Do not connect an external power source to J1 if the board is powered via the PMC connectors. Doing so will result in damaging the board.

The external power connector is of type Molex 43045-1021. Each circuit can carry a maximum current of 5A. The connector pin assignment is as follows:

Pin #	Signal	Signal	Pin #
1	3.3V	3.3V	2
3	5V	5V	4
5	GND	GND	6
7	GND	GND	8
9	-12V	12V	10

Table 11 : External power connector pin assignment

5 Environment

5.1 Temperature

Operating temperature

- 0°C to +60°C (Commercial)
- -40°C to +85°C (Industrial)

Storage temperature:

- -40°C to +120°C

5.2 Convection cooling

600LFM minimum

5.3 Conduction cooling

The FM480 can optionally be delivered as conduction cooled PMC. The FM480 is compliant to ANSI/VITA 20-2001 standard for conduction cooled PMC.

6 Safety

This module presents no hazard to the user.

7 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

8 Warranty

	Hardware	Software/Firmware
Basic Warranty (included)	1 Year from Date of Shipment	90 Days from Date of Shipment
Extended Warranty (optional)	2 Years from Date of Shipment	1 Year from Date of Shipment