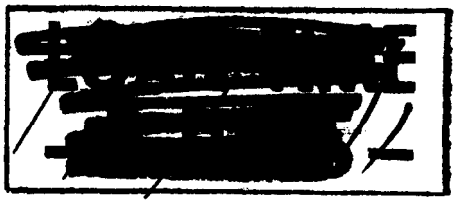
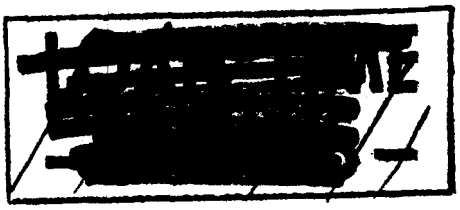
NIM MODEL 3001

QVT
MULTICHANNEL ANALYZER





Manual Version Number: 1.01

GENERAL PRODUCT WARRANTY AND SERVICE POLICY

GENERAL PRODUCT WARRANTY

LeCroy Research Systems warrants operation of its products within published specifications for a period of one year from the date of shipment. This warranty is provisional on the correct and proper use of the equipment as expressed in the operation manual accompanying that product.

If during this period a product is found to be defective it should be returned to the factory, or for European customers, to the nearest authorized European service location, for repair or replacement at the discretion of LeCroy. The customer must pay shipping charges for the return of any equipment to the factory or authorized se&e location. LeCroy will pay the return shipping charges for in-warranty repairs.

OEM PRODUCTS

The above general one year warranty applies only to equipment desrgned and manufactured by LeCroy Research Systems. All non-LeCroy products which accompany or are provided with a System are covered by the Original Equipment Manufacturer's warranty, which is typically 90 days from the date of shipment. In some cir cumstances and for out-of-warranty repair. It may be more expeditious to contact the OEM set-vice facility directly. OEM product warranties and service locations are listed below.

Model 3500-35 Quad Serial Interface
Central Data Corporation
1602 Newton Drive
Champaign, IL 61821-1098
(217) 359-8010

Warranty Period--1 Year

Model 3500-37 Time and Date Unit
Digital Pathways Inc.
1260 First Mortgage Circle
Palo Alto, CA 94303
(415) 493-8544

Warranty Period 90 Days

Model 3500-38 GPIB Interface
Fastech Corporation
3493 Bucano Court
San Luis Obispo, CA 93401
(805) 541-0488

Warranty Period—1 Year

Model 3500-39 Bubble Memory
Intel Products Service
2402 West Beardsley Road
Phoenix, Arizona 65027
800-528-0595

Warranty Period - 90 Days

Model Rimfire 38A Hard Disk Controller
Computer Products Corporation
3405 Annapolis Lane
Plymouth MN 55441
(2) 2034

Warranty Period—90 Days

Model 3921 Dual Floppy Disk Drive
Data Systems, Inc.
2241 Lundy Ave.
San Jose, California 95131
Telephone: 408-946-5800

or

Data Systems, Inc.
81 Morgan Drive
Norwood, Massachusetts 02062
Telephone: 617-769-7620

Warranty Period—1 Year

Model 3931A Printer/Plotter
Hi-G Co., Inc.
Printer Products Service Center
580 Spring Street
Windsor Locks, Connecticut 06096
Telephone: 203-623-3363

Warranty Period—1 Year

Model 3932 Plotter/Printer
Houston Instruments
1 Houston Square
Austin, Texas 78753
Telephone: 512-837-2820

or

Houston Instruments
Rochesterlaan 6
8240 Gistel
Belgium
Telephone 3359-27445
Telex 61399 Bausch

Warranty period—1 Year

Model 3955 Streaming Tape Drive
Cipher Data Products
7221 Orangewood Avenue
Garden Grove, CA 92641
(714) 891-3711

Warranty Period—1 Year

Model DPP-7 Printer
Datel Intersil
11 Cabot Boulevard
Mansfield, Massachusetts 02048
Telephone 617-339-9341

Warranty Period—1 Year

SOFTWARE

LeCroy warrants only software and firmware which has been written and developed by LeCroy. LeCroy assumes no responsibility for user-written software. When a customer encounters a problem with LeCroy developed software, a System 3500 Software/Firmware Problem Report (provided in the Operator's Manual) should be sub mitted to LeCroy. in which the customer identifies the Program and Version Number and defines the problem. LeCroy will respond to the Problem Report within two weeks of receipt and. if the problem is in the software, will resolve the problem by issuing a new software release. In some cases. a solution may be provided to the customer by lelephone.

LeCroy's responsibility in the event of software defects is limited to resolution of the problem by correction and/or replacement of the defective software.

INSTALLATION

Installation of equipment purchased from LeCroy will be the responsibility of the customer unless installation arrangements and terms are defined at the time of purchase.

WARRANTY EXCLUSIONS

The foregoing warranties will not apply to replacement or repairs of parts whose failure is caused by accident transportation neglect misuse. intentional damage, alterations (which shall include but not be limited to any change in circuit or structural equipment design as provided by LeCroy, installation or removal of LeCroy features, or any other modification or maintenance related activities. *Whenever any of the foregoing* are performed by other than LeCroy representatives) any machine or device other than those sold by LeCroy or the use of the equipment for other than data acquisition and/or processing purposes for which sold, to be determined by LeCroy.

LeCroy shall not be responsible for failure to provide replacement parts due to causes beyond its control. Including strikes of labor stoppages or acts of God or be required to adjust or repair any equipment or part if it would be impractical to do so because of the alterations in the equipment or its connection by electrical or mechanical means to another machine or device

This warranty shall become void if customer fails to operate equipment in accordance with LeCroy written instructions or, in case of disc drive read/write reads if customer uses other than approved magnetic recording media. Approved media shall be only diskettes manufactured to quality standards equal to or exceeding those of diskettes manufactured by International Business Machines (IBM) and Dysan

This warranty is in and all other warranties expressed by implied regarding the equipment supplied hereunder, including any regarding merchantability or fitness for a particular purpose. This warranty apples only to end user customers of LeCroy.

LeCroy reserves the right to make changes without prior notice and without incurring obligations.

LeCROY RESEARCH SYSTEMS CORPORATION
700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
(914) 425-2000

SERVICE POLICY

In general, LeCroy provides factory service only from its Spring Valley, New York facility. Service for customers in New Mexico, Southern Nevada, Arizona. Colorado. and El Paso County, Texas is provided at this Branch Office:

LeCROY RESEARCH SYSTEMS CORPORATION
New Mexico Service Facility
14800 Central Avenue SE
Albuquerque New Mexico 87123

For European customers. service is also provided at the following LeCroy Branch Offices:

LeCROY RESEARCH SYSTEMS SA
European Products Division
Rue Cardinal-Journet 27
1217 Meyrin 1 -Geneva. Switzerland
Telephone: (022) 82 33 55
Telex: 28230

LeCROY RESEARCH SYSTEMS LTD.
Elms Court
Botley, Oxford CX2 9LP, U.K.
Telephone: (0865) 72 72 75
Telex: 837539

LeCROY RESEARCH SYSTEMS SARL
Avenue du Parana
Z.A. de Courtaboeuf
F-91940 Les Ulis, France
Telephone: (6) 907 38-97
Telex: 692.838

LeCROY RESEARCH SYSTEMS GMBH
Tiefschkestrasse 3
6900 Heidelberg, W. Germany
Telephone: (06221) 28192
Telex: 04-61680

LeCroy reserves the right to repair or replace defective components.

FIELD SERVICE

On Site Repairs are at the discretion of LeCroy and are limited to the diagnosis of the defect. For on site repairs during the warranty period, parts and labor are at LeCroy's expense. The user must provide payment for the field service representative's traveling expenses and living expenses while on the site.

REPLACEMENT ORDERING PROCEDURE

Replacement parts, subassemblies, or modules are dispatched to the customer from the factory or branch office for replacement in the defective equipment by the customer. Should this not prove successful in solving the problem, the equipment must be returned to the factory or nearest office for repairs.

In some circumstances a user may request replacement of a defective plug in subassembly or module prior to returning the defective item. In these instances, a replacement will be supplied if the user issues a purchase order for the replacement item. If the defective assembly or module is in warranty and is not returned to the factory within 30 days from the date o! shipment of the replacement, the user will be invoiced for the replacement.

POST WARRANTY REPAIRS

For all LeCroy products in need of repair after the warranty period. the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

RETURN PROCEDURE

For all products returned to the factory for repair, include the product model number, serial number, ECN number, an accurate description of the defect or failure, and the name and phone number of the user. Before reiurning a product for repair, whether in or out of warranty, the user should contact the Engineering Services Department at the factory (Phone No. 914 425-2000) for a Return Authorization Number. This number is used to identify the product for repair and to reference any correspondence concerning that repair. Return shipping costs are a! the customer's expense LeCroy will not accept C.O.D. or Collect Return Shipments. Products should be returned in their original shipping cartons where possible.

February 1984

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refineandimprove the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

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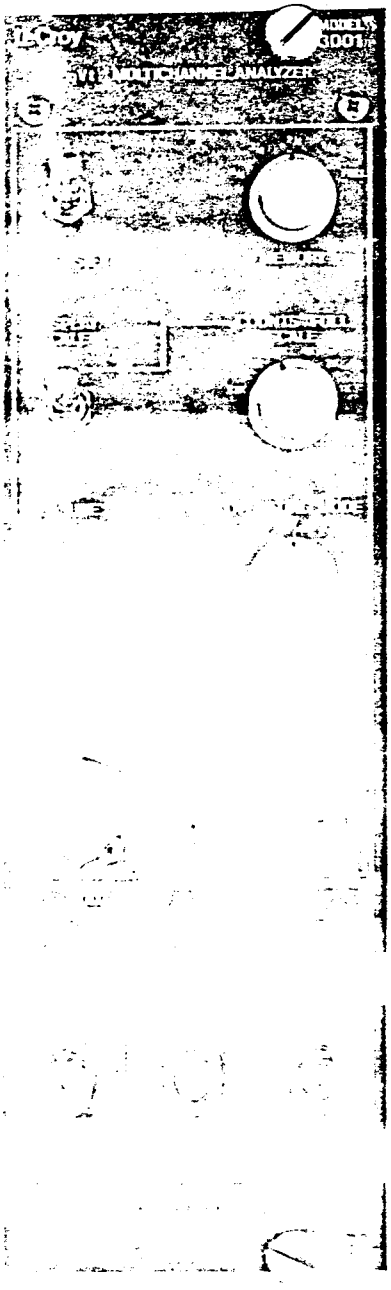
LeCroy

qVt®

NIM Model 3001
Multichannel Analyzer



The Model 3001 is a research grade multichannel analyzer which provides exceptional versatility at relatively low cost. The Model 3001 features:

- 3-Mode Analysis-Charge (Q, area) and voltage (V, peak) analog-to-digital conversion and time-to-dioital conversion (T, start/stop) modes mean direct compatibility with photomultiplier anodes and elimination of charge-sensitive preamps and time-to-amplitude converters (TAC's).

- High Sensitivity-Cl = 0.25 pC sensitivity in charge mode, V = 1 mV resolution in peak mode (0 to 1 or 0 to 10 volt inputs), and T = 100 psec resolution in time mode mean direct compatibility with low-level signals from a variety of sources and the ability to precisely measure short time intervals.

- Segmentable Memory -- 4 x 256 (quadrants) or 1 x 1024 (full scale) gives the flexibility to accumulate, display, and compare up to four different spectra or to display quadrants of a full 1024-channel spectrum.

- High Count Capacity -- 2^16 1(65 535) counts capacity permits enough data accumulation to satisfy applications including cosmic ray and high energy experiments and many nuclear spectroscopy ane Mossbauer applications.

- Nanosecond Logic Functions -- Internal trigger ing mode permits the 3001 to be used as a stand-alone device, while the external modes permit either internal gate generation upon application of an external trigger or direct application of an external gate signal.

- **Choice of I/O**—Interfaces, through accessory modules, to an X-Y plotter, line printer, or the CAMAC dataway.

- Compact Packaging -- Complete 1024-channel analyzer compactly packaged in a #2 NIM-standard module gives greater portabilityt, lower cost, and enhanced reliability.

- **Versatile Display**—Highly accurate digitally derived logarithmic and linear display permits viewing the memory content at optimum amplitude resolution.

- **Drives Any X-Y Scope**—The use of the 3001 with any external X-Y scope in your lab means smaller basic analyzer size, greater mobility, and saves you the expense of a built-in scope which you may already have available.

February 1983

LECROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

GENERAL DESCRIPTION

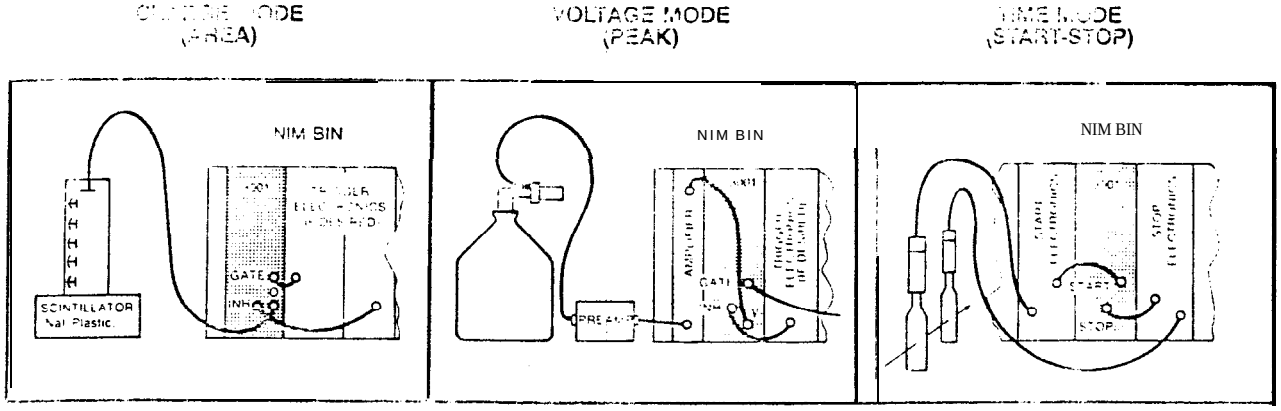
The Model 3001 is a new, low cost, 1024-channel multichannel analyzer offering three analysis modes: charge (area), voltage (peak), and time (start/stop). Packaged as a double-width NIM module, it is significantly more compact than even the smallest analyzers previously avaiiable. Each of the 3001's 1024 channels has a count capacity of 16 bits (65,535). The contents may be displayed in log/linear fashion on any X-Y oscilloscope. The display is active on a time-available basis, thus affording display during data accumulation. A front-panel switch selects intensification of every tenth or fiftieth channel. Data may be accumulated and displayed in selected 256-channel quadrants or in the full 1024-channel memory. In addition to both an internal and external trigger capability with variable gate width, the 3001 provides external gate and inhibit inputs, which are also used as start and stop inputs in the time mode.

Rear-panel digital outputs are supplied to allow for data transfer to interface options including a readout device (e.g., printer) or a CAMAC Dataway. The output connector may also be used to load or increment any one of the 16-bit words in memory. This feature allows the 3001 to be used as an additional 1024 words of memory and to act as a histogram display module.

The 10-bit ADC used for the Q (charge) mode has a sensitivity of 0.25 pC/channel, directly compatible with photomultiplier anodes pulses, thus obviating the need for a charge-sensitive preamplifier. In the Q mode, the input current is integrated for a duration ranging from 10 nsec to 1 μsec. A front-panel-adjustable internal gate is generated by either an internal or an external trigger, or an external gate pulse may be directly applied to the MCA. Operating in the Internal mode. the Model 3001 is a stand-alone device. possessing an internal discriminator of 1 mV minimum threshold. The Q input is terminated in 50 Ω and all analog circuitry is dc-coupled, thus eliminating the need for dc restoration instrumentation.

The 10-bit TDC used for the T (time) mode of the Model 3001 digitizes time intervals by the start-stop technique and stores their spectra. Full-scale time intervals are 102 nsec and 1024 nsec, offering respective resolutions of 100 psec/channel and 1 nsec/channel. The start and stop inputs are ieading edge triggered, responding to NIM (negative) signals. Uses of the T mode include time of flight, counter timing, and delay measurement, time correlation spectra, and drift chamber calibration.

In the V (voltage) mode, the output of any voltage source, e.g., a charge-sensitive preamplifier, may be analyzed. The maximum (peak) voltage (of signals > 50 nsec risetime) applied to the input during the gating interval is digitized, thus making external stretching circuits unnecessary. The full-scale input in the V mode is + 1 volt (- 10 V is switch selectable), offering a resolution of 1 mV (10 mV) consistent with that of a Si(Li) detector. The internal gate may be extended to 5 μsec in this mode.



For direct digitizing of photomultiplier anode current pulses. No charge-sensitive preamp is required, permitting high counting rates and pile-up elimination.

For use as a conventional Pulse Height Analyzer. Accepts positive voltage signals or dc levels.

For Start-Stop timing measurements. Not multisclaing. No TAC necessary.

SPECIFICATIONS
NIM Model 3001
qVt MULTICHANNEL ANALYZER

GENERAL OPERATIONAL CHARACTERISTICS

Analysts Modes:

Q: Current Integrating (charge sensitive); integration interval 20 nsec to 1 μsec; full scale, 256 pC ± 10% sensitivity, 0.25 pC/channel.

V: Peak voltage: input signal risetime, ≥ 50 nsec: full scale, + 1 volt or + 10 volt ± 10%; resolution, 1 mV or 10 mV/channel; external gate width, 100 nsec minimum to 1 μsec or switch selectable 5 μsec maximum.

T: Time interval (Start/Stop); full scale internally swatch-selectable, 102 or 1024' nsec ± 10%; resolution, 100 psec and 1 nsec respectively.

Number of Channels: 1024 (lo-bits); 256 (8-bits) in quadrants; overflow counts are stored rn the last address of the selected memory segment.

Memory Size: 16 bits – 1 per channel (65.535 counts).

Digitizing Time: 12 μsec + 0.05 μsec/channel.

Temperature Stability: ± .03% of full scale/%.

Long-Term Stability: ± 0.2% of full scale/week. maximum.

Integral Non-linearity: ± 0.25% of reading ± 2 channels.

Display: 100 sweeps/second

Channel Intensification: Every 10th or 50th channel. front-panel selectable.

PHYSICAL CHARACTERISTICS

Packaging: #2 width, RF-shielded NIM-standard module. conforming to specifications outlined in AEC Report TID-20893.

Voltages Used: ± 24 volts, ± 12 volts (Note: a rear-panel switch permits operation from ± 6 volts to available) instead of ± 12 volts.)

Current Requirements:

+ 24 V at 24 mA	-24 V at 125mA
+12 V at 06 mA	– 12 V at 127 mA
+6 V at 1.35 A	- 6 V at 510 mA

Note: ± 6 V requirements add to ± 12 V requirements when ± 6 V option is unused.

Front-Panel Connectors: BNC.

INPUT CHARACTERISTICS

Analog Input (Q and V Modes): Direct-coupled; impedance, 50 Ω optionally, 93 Ω in V mode; protected to ± 30 volts for 1 μsec; linear range, 0 to – 1 volt in Q mode, 0 to + 1 volt in V mode.

External Gate/External Trigger/ Start/Internal Gate View: One Common front-panel connector, functionally controlled by trigger mode switch; requires – 600 mV signal into 50 Ω.

Q and V Modes: In External Gate (EXT. GATE) mode, the gate width is equal to the duration of the gate pulse applied to this connector.

In External Trigger mode (EXT. TRIG), the internal gate is triggered by the leading edge of a fast NIM signal applied to this connector (min. trigger width, 10 nsec).

In Internal (INT) mode, the internally-generated gate may be viewed at this connector. Amplitude – 100 mV.

Q Mode: Usable gate duration, 20 nsec to 1μsec.

V Mode: Minimum duration, 100 nsec. Maximum duration, 5 μsec. Gate must enclose peak of input signal to be measured.)

T Mode: The leading edge of Start input begins the start-stop time measurement, minimum pulse width, 10 nsec. External trigger mode only.

Inhibit/Stop: One common front-panel connector; requires – 600 mV into 50 Ω.

Q and V Modes: Conversion is inhibited by application of a NIM inhibit signal. This level must be established before, and persist at least 20 nsec after the leading edge of the gate trigger. Inhibit is ignored after conversion is begun.

T Mode: Leading edge of stop pulse terminates the interval measurement, minimum pulse width, 10 nsec.

FRONT PANEL CONTROLS

Gate Width Front-panel minimum gate width control for Internal and External Trigger modes; duration with range of 20 nsec to 1 μsec (5 μsec switch selectable for longer time range). Setting stability ± 10% or 1 nsec, whichever is greater. Output monitors permit switch selectable viewing of internal gate pulse for precise adjustment. Lower level discriminator triggers internal gate.

*Range 120 to 1120 nsec.

Threshold:	Front-panel screwdriver-adjustable potentiometer determines threshold setting in internal trigger (INT) mode. Range, – 1 mV to – 15 mV in 0 mode, + 1 mV to + 15 mV in V mode. Front-panel monitor point gives output voltage equal to 1000X actual threshold setting. Threshold stability < 0.2%/°C over 20°C to 60°C operating range.
Operating Mode:	One of the three analysis modes (Q, V, or T) is selected by a 3-position switch.
Trigger Mode:	A 3-position switch selects internal trigger operation (INT). External Trigger operation (EXT TRIG), or operation via an externally-applied gate pulse (EXT GATE).
Continuous/Stop at Overflow:	A 2-position switch either permits continuous data collection and display or limits each channel to a full scale capacity.
Intensify:	Either every 10th or every 50th channel is intensified on the display, determined by a front-panel 2-position switch.
Display LIN/LOG:	Selects linear or logarithmic display.
Start/Stop:	Front-panel two-position. spring-return toggle switch. Start position initiates new measurement cycle after a Stop or Clear. Stop position stops measurement cycle.
Clear:	Front-panel spring-return toggle clears all memory and register. Start/Stop switch must be simultaneously placed in stop position.
Memory Select: Full-',!!-¼-¾-4/4	In the Full position, all 1024 channels accept and display input data. In the ¼ position, the first quadrant (256 channels) accepts and displays input data. Full-scale range settings remain the same (i.e.. 256 pC, + 1 volt, and 102 or 1024 nsec); srmiiar for ²/₄, ¾, 4/4.
Vertical Gain:	In LIN (linear) mode. an e-position switch selects a maximum number of counts to be displayed per channel, between 512 and 65 k.
FRONT PANEL INPUTS	
Q Input:	Analog input; 50 Ω impedance: dc coupled. Accepts input charge of 0 to 256 pC. Protected to ± 100 volts.
V input:	Analog input 50 Ω impedance (93 optional). Accepts inpu! voltage of 0 to + 1 V (with switch selection 0 to 10 V range). Protected to ± 100 volts.
Gate Input/Output:	Multifunctional connector. Acts as trigger or gate input/output in Q or V mode. Acts as Start input in T mode. Input impedance 50 Ω. Accepts NIM fast signals. [See detailed specifications.)
Inhibit/Stop	Accepts fast NIM signals, Ads as inhibit in Q or V mode and slop input in T mode, Impedance 50 Ω.
FRONT PANEL OUTPUTS	
Threshold Test Point:	Reads 1300X preset threshold value in internal mode operation.
Internal Gate Views	internally generated gate is available for oscilloscope monitoring on the Gate Connector when Internal Trigger *is* selected. Amplitude: – 100 mV
Internal Gate Test Point:	Internally-generated gate is available for oscilloscope monitoring when Internal or External Trigger mode is selected. Amplitude: – 200 mV.
Busy:	TTL low level output during conversion time.
Horizontal Out:	Horizontal deflection voltage for CRT proportional to channel number; 0-5 volts for full or qudrant display. Minimum load impedance 1 kΩ.
Vertical Out:	Vertical deflection voltage for CRT propotional to number of counts Linearity ± 0.2% of full scale. Full-scale output of 5 volts corresponds to 200 db/volt in the log mode. Minimum load impedance 1 k!!.
REAR PANEL OUTPUTS	
Connector Type:	44-contact card-edge connector; mates with AMP 582358-2 (hood number 530087-4).
Memory Overflow (22):	A high TTL level* indicates channel overflow. Available during memory load only.
External Enable (4):	Low TTL level* enables external functions accessed by the rear connector.
External Memory Address Latch (R):	The trailing edge of a positive-going TTL-compatible* pulse of minimum duration 200 nsec. latches the address applied to the 10 Memory Address lines (A,B,C,D,E,F,G,H,J,K,L), corresponding to 2^0 to 2^9 respectively.
Memory Enable (21):	TTL-Compatible high level' causes the contents of the memory address latched in lines A-L to Se loaded into the internal incrementing, register. A low level permits loading of the 16-External Data Input levels** into the incrementing Register

**Pin 6 : 2^0	Pin 10 : 2^4	Pin 14 : 2^8	Pin 18 : 2^{12}
5 : 2^1	9 : 25	13 2^9	17 : 2'3
7 : 2^2	11 : 2^6	15: 2^{10}	19 : 2^{14}
a : 2^3	12 : 27	16 : 11"	20 : 2'5

External Load (N):	A low level latches the internal Incrementing Register Data must be quiescent during load interval Minimum duration 200 nsec.
External Read/Write (M):	Causes data to be read from the memory to the internal Incrementing Register or written in memory from the Internal Incrementing Register. Low for read, high for write.*
Incrementing Register (P):	Leading edge of positive-going TTL level causes the contents of the incrementing register to be incremented by 1.

*TTL levels Low: – 0.8 V; High + 3.0 V

SPECIFICATIONS SUBJECT TO CHANGE.

INTRODUCTION

The Model 3001 Multichannel Analyzer is a versatile, high speed, pulse height and time interval analyzer designed to operate in a NIM system. The entire analyzer is packaged in a double NIM module and is otherwise self contained requiring only an addition of a standard X-Y display oscilloscope to form a complete analysis system. The MCA offers three operational modes permitting measurement of total charge, positive peak voltage and time intervals. Capability for generating internal qating for the first two modes is provided by inclusion of a low threshold discriminator set to detect levels down to 1 mV. The width of the internally generated gate may be adjusted by means of a multi-turn front panel control.

The analog-to-digital converter of the MCA provides a resolution of 1024 channels with an integral linearity of 0.25%. The converted data is stored in a 1024 x 16 bit semiconductor memory which may be used either in its full or quadrant configuration. This feature provides capability for storage and subsequent retrieval of up to four 256 channel spectra. All overflow events are stored in the 1024th channel. A high speed flickerless display with a repetition rate of approximately 100 sweeps per second presents the memory contents in real-time while the measurement is in progress providing a constant monitoring facility. The diqitally generated analog output can be displayed in linear format or in a log-compressed format. The log format allows channels with only 1 count to be differentiated from zero while also displaying a full scale channel.

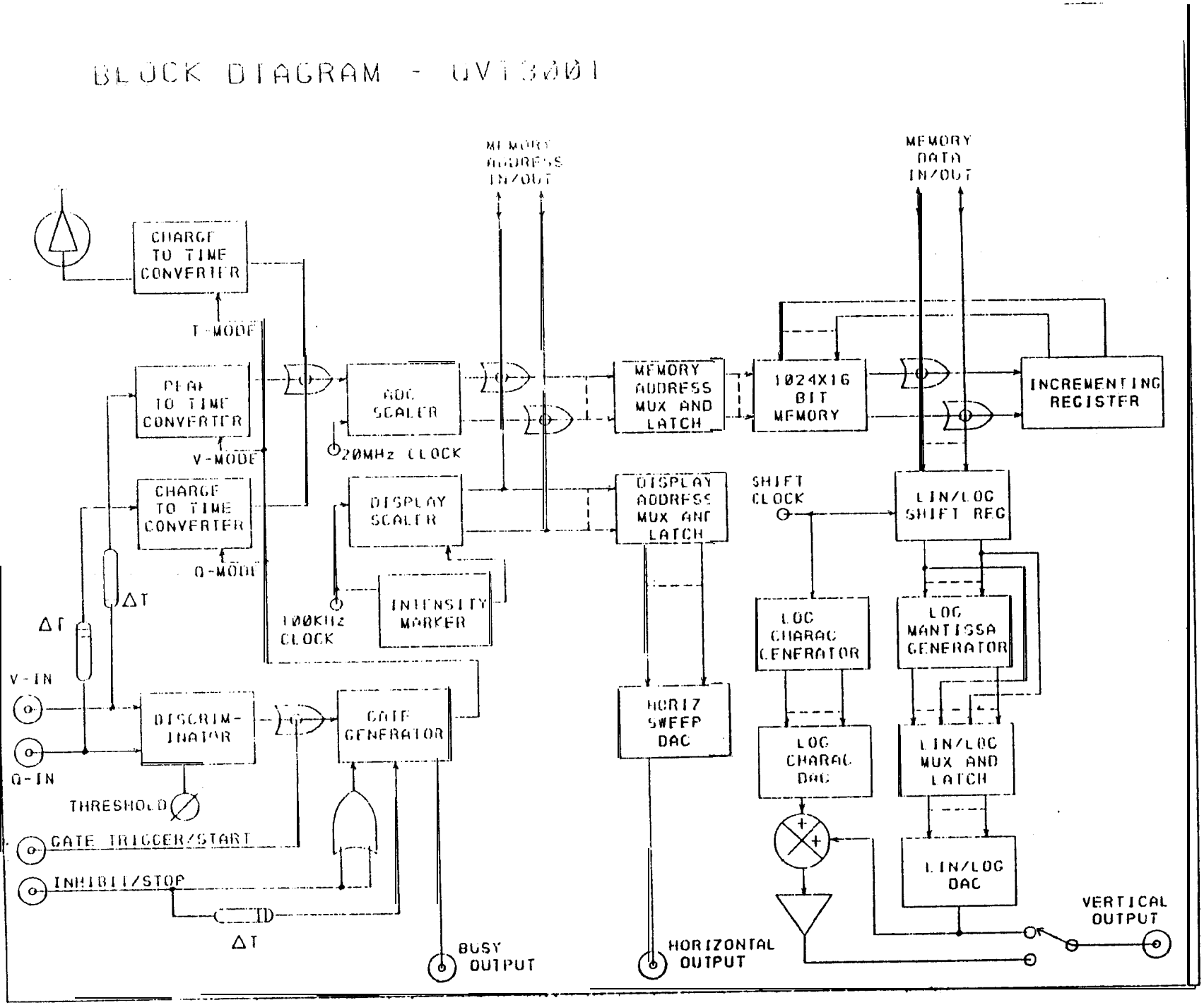

BLOCK DIAGRAM - UVT3001
MEMORY ADDRESS IN/OUT
MEMORY DATA IN/OUT
CHARGE TO TIME CONVERTER
T-MODE
PEAK TO TIME CONVERTER
V-MODE
CHARGE TO TIME CONVERTER
Q-MODE
ADC SCALER
20MHz CLOCK
DISPLAY SCALER
100KHz CLOCK
INTENSITY MARKER
MEMORY ADDRESS MUX AND LATCH
1024X16 BIT MEMORY
INCREMENTING REGISTER
DISPLAY ADDRESS MUX AND LATCH
SHIFT CLOCK
LIN/LOG SHIFT REG
LOG CHARAC GENERATOR
LOG MANTISSA GENERATOR
HORIZ SWEEP DAC
LOG CHARAC DAC
LIN/LOG MUX AND LATCH
LIN/LOG DAC
VERTICAL OUTPUT
HORIZONTAL OUTPUT
ΔT
ΔT
V-IN
Q-IN
DISCRIM-INATOR
GATE GENERATOR
THRESHOLD
GATE TRIGGER/START
INHIBIT/STOP
ID
ΔT
BUSY OUTPUT

Fig. 1

OPERATION

Power

The Model 3001 utilized ±6 V, ±12 V, and ±24 V. Because some NIM bins do not supply ±6 V, ±6 V supplies, operating off of the ±12 V supplies have been incorporated in the qVt. A rear panel switch selects this feature. Note that the current required for the ±6 V sections is then drawn from the ±12 V supplies.

Display

The HORIZ OUT and VERT OUT connectors of the Model 3001 supply 0 to +5.0 V. Intensification of every 10th or 50th channel is selected by the INTENSIFICATION switch. Channel intensification is accomplished by pausing. Any oscilloscope capable of X-Y operation may be used. The oscilloscope should be used with unterminated (high impedance) inputs to use the 0 to +5.0 V calibration of the 3001's outputs.

The DISPLAY SCALE switch selects the mode of display. In the LIN position, the display is linear with a full scale (+5.0 V) as set by the COUNTS FULL SCALE switch. In the LOG position, the display is logarithmic the +5.0 V corresponding to LOG 65.5 K counts. In the LOG display mode, the COUNTS FULL SCALE switch is inactive.

Accumulation and Memory Clear

After the START/STOP switch is placed in the START position, the Model 3001 will accept data. It will remain live until it receives a STOP command. When the MEASURE switch is in the STOP AT OVERFLOW position, the analyzer generates a STOP when the contents of any channel exceeds the capacity of the memory. $(1^{16}-1)$. A STOP command is also generated when the START/STOP switch is placed in the STOP position. if the MEASURE switch is in CONTINUE, the analyzer memory will oveflow but will continue acquisition.

The memory display of the 3001 remains active at all times. A slight flicker is discernable only at very high input rates. The portion of memory in use (full or quadrant) will be cleared (set to zero) by moving the CLEAR switch to the right (CLEAR position) and simultaneously moving the START/STOP switch to the left (STOP position). This is a protection feature to guard against inadvertant clearing of the memory.

Memory Control

The MEMORY switch allows the user to select the part of the memory he wishes to use. In the FULL position, the entire 1024 channels are used for both histogramming and display. In the 2/4 position only channels 256 to 511 (Quadrant 2) are used, etc. When the analyzer is operated in the quadrant mode, the CLEAR operation effects only the quadrant in use.

Busy out

The BUSY OUT supplies a TTL low during conversion and a TTL high at all other times. This signal is intended to allow determination of live time and to count the number of accepted events

Operating Modes

The OPERATING MODE switch selects the q, V, or tmode. It allows the operating controls, inputs, and outputs, to have varying functions. Those described above, however, are independent of the OPERATING MODE. Operati of the 3001 in each of the 3 modes will be discussed below.

q Mode The q MODE is intended for analysis of photcmultiplier anode signals without amplifying or shaping. Analog-to-digital conversion is performed on the quantity of charge received at the Q-INPUT within a well defined time interval. A block diagram of the analog front-end of the q-MODE section of the 3001 is shown in Fig. 2. A gate pulse (internally or externally generated) activates the linear gate and allows the current at the Q-INPUT to be integrated on the capacitor C. Thus the analog "pulse height" is stored for ADC. Since the input to the amplifier is a "virtual ground", the input impedance of the Q-INPUT is 50 Ω. This mode exhibits best stability when driven from source impedances > 1 KΩ such as a photomultiplier.

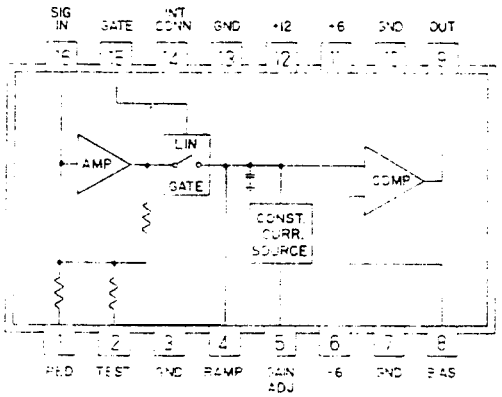


Fig 2

q Mode Gating An internal gate generator may be used to generate gates in the q MODE. This generator may be triggered either by an internal discriminator operating on the analog input signal (INT) or by an externally applied NIM-fast logic pulse on the GATE INPUT (EXT TRIG). An externally applied NIM pulse derived from external logic may be applied as the gate pulse (EXT GATE).

* The Gate Generator: The gate generator is a triggerable monostable whose output may be adjusted by a 22-turn front-panel GATE WIDTH potentiometer. Fully counter-clockwise, this control sets a gate width of approximately 20 nsec and fully clockwise, it sets a width > 1 μsec. The actual gate width can be determined by viewing the NIM gate pulse at the test point adjacent to the GATE WIDTH potentiometer. In the INT mode, the GATE INPUT/GATE VIEW connector serves as an output of the gate pulse with an amplitude of approximately -100 mV. The test point and GATE VIEW outputs supply gate pulses whenever the gate generator is triggered.

* INT Trigger Mode: In the TNT GATE trigger mode, an internal discriminator on the analog signal is used to trigger the gate generator. The discriminator level is set by the 22 turn THRESH potentiometer. Set fully counter-clockwise, a threshold of approximately -1 mV is obtained. Fully clockwise, the threshold is approximately -20 mV. The test point adjacent to the input THRESH potentiometer gives a voltage approximately 1000 x the threshold. No connection should Se made to the V-INPUT.

  In this node, the GATE INPUT/GATE VIEW connector serves as gate view output giving a -100 mV amplitude gate output (into 50 Ω) each time the 3001 gate generator is fired. The INHIBIT IN ccnnsctor allows the output of the internal discriminator to be inhibited. A NIM-fast pulse of 10 nsec minimum duration should be applied simultaneous with the leading edge of the analog input pulse at the Q-INPUT to inhibit. The GATE INHIBIT inputs are ignored after conversion is begun.

* EXT Trigger Mode: Operation in the EXT TRIG Mode is intended for applications in which a somewhat more extensive trigger is required. In this mode, a NIM-fast pulse applied to the GATE INPUT is used to trigger the internal gate generator. The INHIBIT IN input accepts NIM-fast pulses which may be used to veto the trigger. The internal discriminator is therefore defeated in this mode. The leading edge of the gate trigger pulse should occur 3 nsec after the leading edge of the analog input at the Q-INPUT connector.

A fast NIM inhibit pulse of minimum 10 nsec duration should be applied simultaneous with the leading edge of the GATE TRIGGER pulse in order to inhibit conversion. The GATE and INHIBIT inputs are ignored after conversion is begun.

* EXT GATE Mode: In the EXT GATE Mode, the 3001 accepts an external gate pulse rather than employing the internal gate generator. In fact, the WIDTH setting has no effect on performance in this mode. The integration time in this mode is equal to the width of the gate pulse. Gates as short as 10 nsec may be used. Because of internal delays, the leading edge of a NIM-fast pulsemust be applied to the GATE INPUT 3 nsec after the leading edge of the Q-INPUT analog pulse. Note that

THIS REQUIRES 5 NSEC OF ADDITIONAL SIGNAL DELAY

as compared with LRS Model 2249A operation. The INHIBIT INPUT requires a NIM-fast pulse of 10 nsec minimum duration in order to inhibit the gate pulse. The leading edge of the Inhibit pulse should be coincident with the leading edge of the gate pulse. After conversion has begun, the GATE and INHIBIT inputs are ignored.

q MODE Input Signals The Q INPUT is terminated in 50 Ω. Because of the high speed nature of this mode, attention should be paid to proper impedance matching throughout the system. The reflections caused by impedance mismatches will cause a loss of resolution.

The Q INPUT accepts negative analog signals. Signals as large as -20 mA (1 V into 50 Ω) are handled linearly. Larger signals cause a gradual deviation from linearity. Two volt input signals, for example, register approximately 10% lower than 1 V signals of twice the duration. The input is protected against ±100 V transients of duration ≤1 μsec. Although such transients will not cause circuit damage, tney may, however cause the data in the analyzer to become disturbed.

q Mode Slope and Pedestal The action of the charge sensitive ADC in the Model 3002 is to produce a digital output, related to the input charge q by the relationship

$$q = S(N-No) \qquad (N \geq N_0)$$

Here S is the slope, approximately 0.25 pC/count or 1 pC/count in the full

or quadrant modes respectively. NO is the pedestal or the channel number obtained for a conversion with no Q signal. Pedestal also depends upon the output impedance of the signal source. Although S is fixed, NO is not. Increasing the gate width will cause an increase in the pedestal (see enclosed specifications). A trimmer capacitor mounted on the digital board adjacent to the QT100C hybrid affords pedestal adjustment over a range of approximately 50 counts. In general, a pedestal >0 counts is advantageous in that it allows the experimenter to be aware of the origin of his histogram. This is of particular significance for the Model 3001 in that it maintains linearity even in the first few channels above pedestal.

v Mode

The V Mode is intended for analysis of the output of voltage sources such as spectroscopic amplifiers or Mossbauer velocity drives. Analog-to-digital conversion is performed upon the maximum voltage within the gating interval. The input impedance of the V-INPUT is 93 Ω. Because the V-INPUT is intended for slower signals, the gate timing is less critical.

V Mode Gating An internal gate generator may be used to generate gates in the V MODE. This generator may be triggered either by an internal discriminator on the analog input signal (INT) or by an externally applied NIM-fast logic pulse on the GATE INPUT (EXT TRIG). An externally applied NIM pulse derived from estemal logic may be applied as the gate pulse (EXT GATE).

* The Gate Generator: The gate generator is a triggerable monostable whose output may be adjusted by a 22-turn front-panel GATE WIDTH potentiometer. Fully counter-clockwise, this control sets a gate width of approximately 20 nsec and fully clockwise, it sets a width > 1 μsec. The minimum gate width for V MODE operation is 100 nsec. The actual gate width can be determined by viewing the NIM gate pulse at the test point adjacent to the GATE WIDTH potentiometer. in the INT mode, the GATE INPUT/GATE VIEW connector serves as an Output of the gate pulse with an amplitude of approximately -100 mV. The test point and GATE VIEW outputs supply gate pulses whenever the gate generator is triggered.

* INT Trigger Mode: In the INT GATE trigger mode, an internal discriminator on the analog signal is used to trigger the gate generator. The discriminator level is set by the 22-turn THRESH potentiometer. Set fully counter-clockwise, a threshold of approximately +1 mV is obtained. Fully clockwise, the threshold is approximately +20 mV. The test point adjacent to the input THRESH potentiometer gives a voltage approximately 1000 X the threshold. No connection should be made to the Q INPUT.

In this mode, the GATE INPUT/GATE VIEW connector serves as a gate view output giving a -100 mV amplitude gate output (into 50 Ω) each time the Model 3001 gate generator is fired. The INHIBIT IN connector allows the output of the internal discriminator to be inhibited. The INHIBIT pulse, a NIM-fast.pulse, should overlap the gate for proper operation. The GATE INHIBIT inputs are ignored after conversion is begun.

* EXT Trigger Mode: Operation in the EXT TRIG Mode is intended for applications in which a somewhat more extensive trigger is required. In this mode, a NIM-fast pulse applied to the GATE INPUT is used to trigger the internal gate generator. The INHIBIT IN input accepts NIM-fast pulses which may be used to veto the trigger. The internal discriminator is therefore defeated in this mode. The leading edge of the gate trigger pulse shouid be coincident in time with the leading edge of the analog input at the V-INPUT connector.

A fast NIM inhibit pulse of minimum 10 nsec duration should be applied simultaneous with the leading edge of the GATE TRIGGER pulse in order to inhibit conversion. The GATE and INHIBIT inputs are ignored after conversion is begun.

* EXT GATE Mode: In the EXT GATE Mode, the 3001 accepts an external gate pulse rather than employing the internal gate generator. In fact, the WIDTH setting has no effect on performance in this mode. The peak search time in this mode is equal to the width of the gate pulse. Gate as short as 100 nsec may be used. Because of internal delays, the leading edge of a NIM-fast pulse applied to the GATE INPUT should be coincident with the leading edge of the V-INPUT analog pulse. The INHIBIT INPUT pulse will veto a gate pulse if a NIM-fast level is present coincident with the leading edge of a gate pulse and persists for at least 10 nsec.

V Mode Input Signals — The V-INPUT is terminated in 93 Ω and accepts input signals of 50 nsec risetime or greater. Generally, gaussian shaped pulses are used as analog inputs but the 3001 allows other shapes also. For example, a ramp input may be used. If no peak is obtained during the gating interval, the maximum voltage will be analyzed.

The V-INPUT accepts positive analog signals. The range of the ADC for this mode allows signals to 1 V into 93 Ω. Larger signals give an off-scale result and are treated as a full scale (ch 1024) signal. The input is protected against ±100 V transients of < 1 μsec duration. Although such transients will not cause circuit damage, they may, however, cause the data in the analyzer to become disturbed.

V Mode Slope and Pedestal — The action of the peak sensing ADC in the Model 3001 is to produce a digital output, N, related to largest voltage in the gate interval by:

$$V = S(N-No) \qquad (N > No)$$

Here S is the slope, approximately 1 mV/count or 4 mV/count in the full or quadrant modes respectively. NO is the pedestal or the channel number obtained for a conversion with the V-INPUT open. Although S is fixed, No is not. Increasing the gate width will effect the pedestal in the V Mode only slightly.

t Mode

In the t-MODE, tie GATE switch must be in the EXT TRIG position. In this mode, the GATE TRIG input is the T START input and the INHIBIT input is the T STOP input. The time between the T START and T STOP pulses is digitized without the use of a time-to-amplitude converter (TAC).

A side panel switch is used to select the full scale time. Two ranges are available (100 nsec full scale (0 to 100 nsec) and 1 μsec full scale (100 nsec to 1100 nsec). Two spare switch positions are supplied to allow selection or alternate conversion gains. Full scale time may range

from 100 nsec minimum to 7 usec maximum. Selection of resistance values for alternate gains is based on the following relationships:

$$\text{GAIN} = \left(\frac{R}{1.97}\right) \cdot 10^{-13} \text{ sec/channel}$$

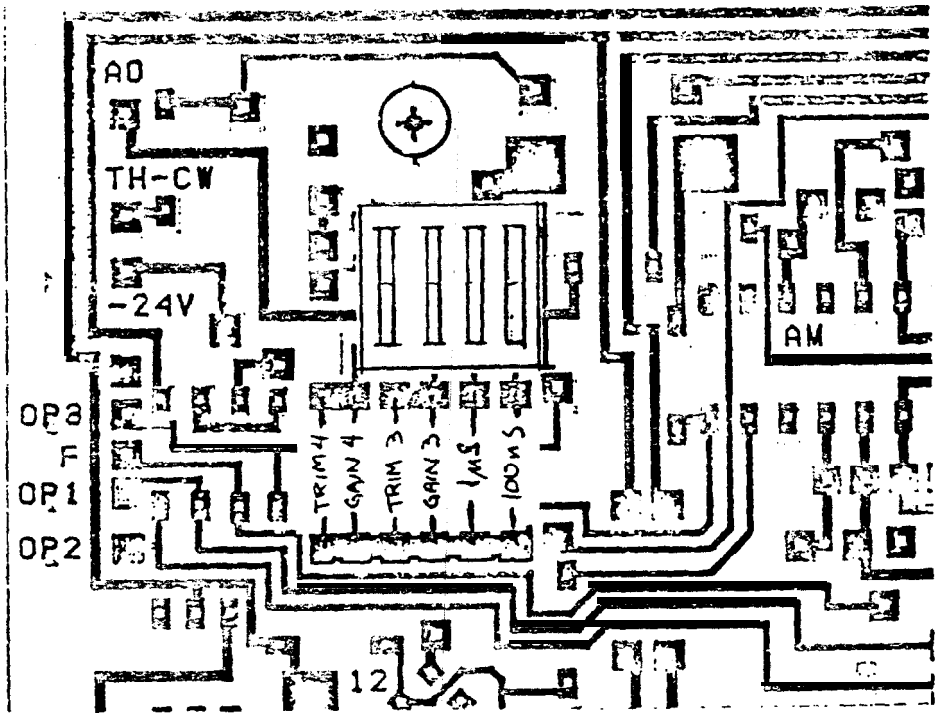
where 10^{-10} sec/chan. $\leq$ GAIN $\leq$ 6 x 10^{-9} sec/chan.

and where R is expressed in ohms.

A pedestal of approximately 14% of full scale must be provided externally because of the inherent negative pedestal of the system. Therefore, a selected gain of 6 x 10^{-9} sec/count will range from ≈.84 usec to 6.84 usec full scale.

Pedestal (external) ≈ 140 x GAIN

At any time of operation, only one time range should be selected. The following diagram illustrates positions for alternate conversion gain components. Access to the PC board illustrated below is gained by sliding back the right hand side **cover** having the cutout that exposes the t-mode range select switch. For best results use a 1% resistor value. A second resistor position is provided in each of the two alternate gain locations for a fine trim of the gain if desired.



Analog Front End

The operation of the 3001 is shown by the block diagram in Fig. 1. The ADC employed is a run-down type consisting of three separate front ends one of which is selected to gate clock pulses to a scaler. The three front-ends are the hybrid circuits QTlOOC, VT100, and QTlOOT used for the q, V, and t modes respectively. See page 2 of the schematic diagram.

The QTlOOC and QTlOOT are charge-to-time converters consisting of "virtual ground" inputs (Pin 16) capable of current amplifying the input pulse received during the time that a gate (>-12 V) is applied to Pin 15. Full scale charge is about 300 pC and 1500 pC for the QTlOOC and QTlOOT respectively. When a gate pulse is received by either of these hybrids, an internal capacitor is charged and a run-down is begun. For the duration of the run-down, a TTL clamp-to-ground is present at Pin 9. This "T output" width is proportional to the amount of charge transferred to the capacitor.

The VT100 has an identical pin configuration to that of the QT100 described above. The input is also a "virtual ground" but it is non-integrating. An amount of charge proportional to the maximum input current applied during the gating interval is stored on the internal capacitor. Run-down is identical to that of the QT100's Full scale is -10 mA.

In the q MODE, the QT100C is biased on by applying +50 mV to Pin 8. In the V and t modes, it is biased off by applying -200 mV to Pin 8. In the q MODE , a gate may be generated either internally or applied from an external source. The Internal Gate Generator is shown on Sheet 1 of the schematic. The Q-INPUT is connected directly to the ***Internal Discriminator*** an LD604LG hybrid, and then via a 25.5 nsec 50 Ω delay cable to a 50 Ω termination at the QTlOOC. Since the input impedance of the LD604LG is very high, the Q-INPUT performs as a low reflection transmission line Well terminated at the QTlOOC. In the INT gate mode, the LD604LG is used to generate a gate trigger, for the internal gate generator circuit. The purpose of the delay line is to account for the propagation delay through the LD604LG and gate circuitry.

In the t MODE an amount of charge proportional to the gate width is deposited in the QTlOOT. A constant current source based upon the -24 V NIX supply is used. A side panel switch selects a series resistance

thus determining the full scale time. Two spare switch positions are available. Pads are available for both fixed and trim resistors. The gate applied to the QTlOOT is based upon the T-START and T-STOP input pulses. The T-START clocks the *Start Flip-Flop.* The clock for the *Start Flip-Flop* is kept high by the busy level (derived from the Busy Generator. See sheet 1 of the schematic. Similarly, the *Stop Flip-Flop* is clocked by a signal derived from the T-STOP input. Its circuitry is activated by the *Start Flip-Flop.* The transistors Q11 and Q12 are used to form the gate pulse applied to the QT100T.

Digital Section

The master clock employed in the 3001 is based upon a 20 MHz LC oscillator (see page 3 of the schematic). The circuit was designed to allow rapid start-up and shut-down gating. When conversion is initiated, the clock is stopped and remains off until the 7 µsec *Wait Monostable,* completes its cycle. The clock may also be inhibited by the user through the pad labeled CI located between TP and TQ, a TTL high inhibits.

When a conversion is in process, Channel A of the dual 11-bit 20 MHz scaler, Model SC100, is used. The output of the hybrid front-end is used to gate the master clock. Thus, after a conversion is completed, the binary data (address) is available at the SC100 outputs. See sheet 4 of the schematic.

The scaler address is latched into the *Memory Address Latch.* See sheet 4. In the quadrant mode, the word is shifted right two bits and the two most significant bits are determined by the MEMORY switch. The word in the *Memory Address Latch* addresses the memory which is normally in a READ state. The resulting data work is latched into the *Incrementing Register* incremented by 1 and replaced in the *Memory* in the same address as given by the *Memory Address Latch.*

Display Section

The display is active except when an analog signal is being received or the results of a conversion are being entered in the *Memory.* The clock continuously cycles Channel B of the SC100 through 1024 counts. The resulting addresses latched into the Memory Address *Latch* are supplied to

the Horizontal Sweep DAC and to the Memory. In the quadrant mode, the memory address is shifted right as in the digital section discussed above. The data read from *Memory* and latched into the *Data Scalar* are processed either by an 8-bit linear or 16-bit logarithmic vertical DAC. See Sheet 6. Display mode is selected by the DISPLAY SCALE switch. In the linear mode, data is shifted right in accordance with the setting of the COUNTS FULL SCALE switch and presented to the *LIN/Mantissa DAC.* In the logarithmic mode, the "characteristic" is generated by counting the number of shifts left required to obtain a left justified logic "1". The remaining data are used to generate a mantissa using a programmed-read-Only memory. The analog mantissa is generated by the 8-bit *LIN/Mantissa DAC* and the analog characteristic is generated by the 8-bit *"characteristic".*

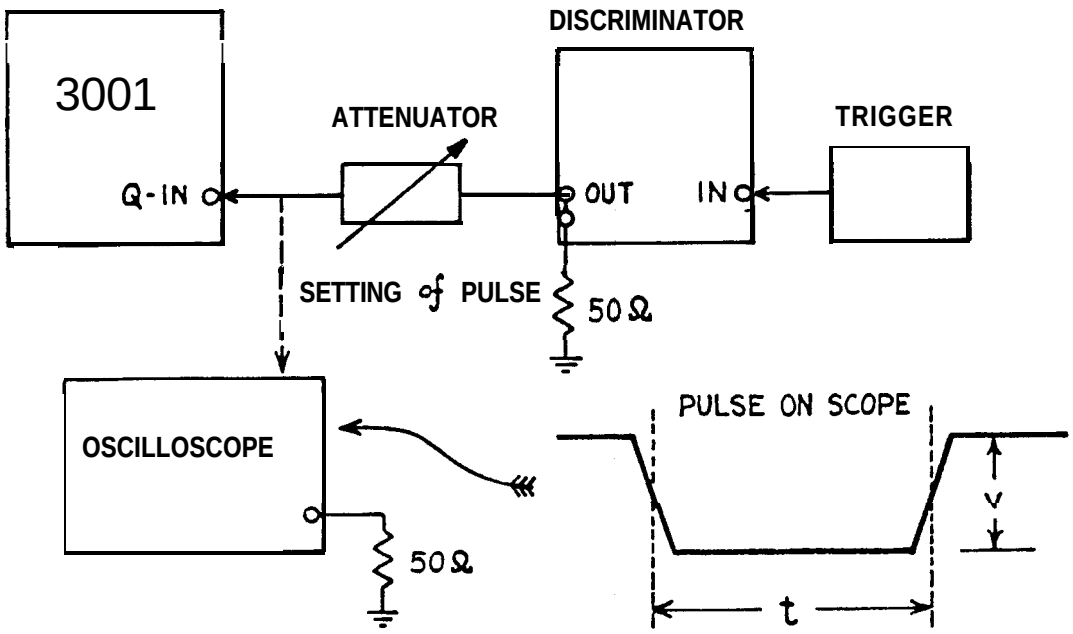
APPENDIX I

A simplified method for calibrating Q-mode pedestal and gain using standard lab equipment.

General

The inherent 51 Ω termination of the Model 3001 Q-input allows one to obtain a well defined amount of charge from the area of a well defined pulse, given by the relation Q = (V/51) t.

Block Diagram of 3001 Q-Mode Full-Scale Calibration



List of Test Equipment which can be used:

1. Attenuator: LeCroy Yodels A101, A101L or A102
2. Discriminator: LeCroy Models 621BL, 621BLP, or 623, etc.
3. Trigger: Oscillator Fan-In/Out 1923 or Instapulser IP-1.
4. Oscilloscope: Textronix 475 or 485

Procedure

1. Set the Model 3001 gate width to 150 nsec using a NIM input pulse and with the gate switch in EXT TRIG position.

2. Terminate the scope input (50 Ω) and with the calibration set-up as shown in the block diagram, select and set the Q-input pulse.

   For a pedestal of 30, a charge of 243 pc is required to obtain a peak in channel 1000 (based on 0.25 pc/channel sensitivity). One therefore obtains the relation t=(12.368)/V(nsec), from it t can be determined if V is selected (Note: V must be between 0.2 and 0.5 volts). Furthermore, measurements showed that the above value of t must be connected by increasing its value by about 8-10%.

   Example: Let V=0.30 volts which gives t=41 nsec and the increased t is 45 nsec. This value of t is used for the calibration pulse.

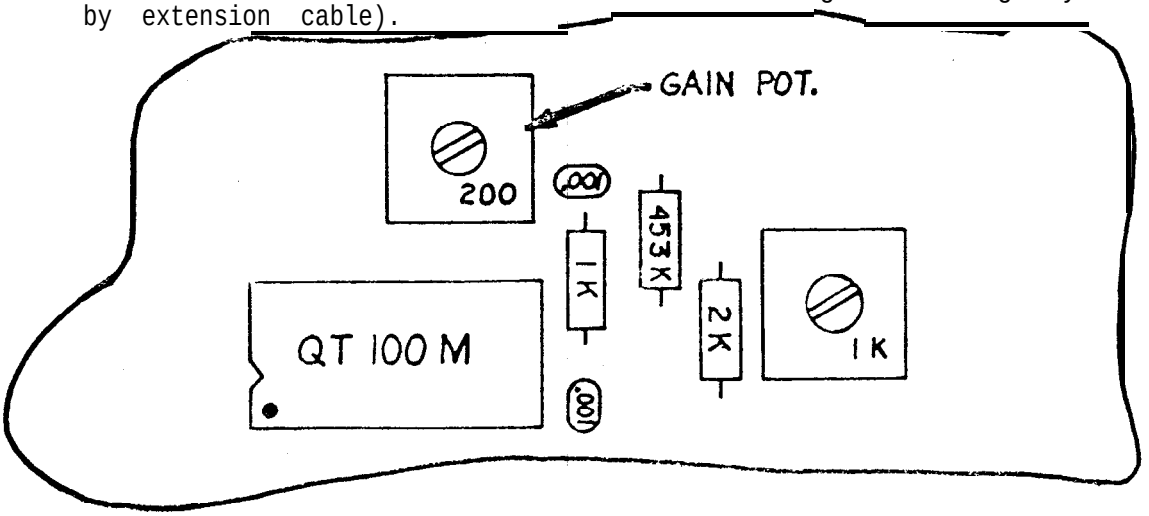
3. Terminate the q-INPUT with 50 Ω and switch the channel intensification (i.e. INTENSIFY) to 10th. (Note: The NIM input pulse is still connected to the GATE INPUT).

4. On the scope, select the XY-mode and adjust the Q-mode pedestal to channel 30 via the 6-20 pF trim capacitor on pin 16 of QT-100M.

5. Remove the terminator from the q-INPUT and connect the output of the attenuator to it. Set gate switch to INT, INTENSIFY to 50th and adjust Q-mode gain* for counts in channel 1000.

6. Repeat steps (4) and (5) until pedestal and pulse occur in channels 30 and 1000 respectively.

* The Q-mode gain is set with the 200 Ω pot at pin 12 of QTlOOM. (NOTE: Gain should be checked with unit in NIM bin since gain setting may be affected by extension cable).



Location
Q-Mode ga

QVT SYSTEM INTERFACE CONNECTIONS

The following is a list of signals provided at the QVT rear panel connector. Usage in the LeCroy Model 2301 CAMAC interface and the Model 3157 printer interface is indicated.

J2 Connector Contact Usage

Signal	2291	3157	Designation	Pin No.	Characteristic
Memory Address	X	x	MA-0	A	Least significant bit of memory address, a positive true TTL level. When used as input address, data must be supplied by an open collector or Tri-state driver. Internal 2 KΩ pull-up resistors are provided in the MCA. The transmission of address must be enabled only when the EXT.EN. is low. Address is read into *the Address Register* on negative going transition of MAL (pin R). The line serves as a memory address output when EXT.EN. is high. Logic is positive true. The line will drive one low power TTL load.
Memory Address	X	x	MA-l	B	As above but 2^1 bit
Memory Address	X	x	MA-2	C	As above but 2^2 bit
Memory Address	X	x	MA-3	D	As above but 2^3 bit
Memory Address	X	x	MA-4	E	As above but 2^4 bit
Memory Address	X	x	MA-5	F	As above but 2^5 bit
Memory Address	X	x	MA-6	G	As above but 2^6 bit
Memory Address	X	x	MA-7	J	As above but 2^7 bit
Memory Address	X	x	MA-8	K	As above but 2^8 bit
Memory Address	X	x	MA-9	L	As above but 2^9 bit

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

J2 Connector Contact Usage

Signal	2301	3157	Designation	Pin No.	Characteristic
EXTERNAL ENABLE	X	X	$\overline{\text{EXT.EN.}}$	4	Low TTL compatible level disables internal control thus enabling external memory control functions.
Memory Enable,	*X*		*ME*	21	TTL low disables (Tri-Stat the memory output and prev it from being written into TTL high enables memory in or output. Low level permits loading external data into the *Incrementing Register.* Input data must be quiescent and should be low until external load (EXT LD) is returned high state. EXT LD must be high during write interval.
$\overline{\text{External Load}}$	X	X	$\overline{\text{EXT LD}}$	N	External data (ED00 to ED1) is loaded into the *Incrementing Register* by trailing ec of a low going TTL compatible pulse, 200 nsec minimum duration. Data must be quiescent during load interval. (See Note).
$\overline{\text{Increment Register}}$	*X*		$\overline{\text{INCR REG}}$	P	The contents of MCA's *Incrcmenting Register is increment* by 1 by the positive going transition of the $\overline{\text{INCR REG}}$ pulse, a TTL compatible, 200 nsec minimum width pulse When unused, must be a TTL high during EXT ENB (See Note)

J2 Connector Contact Usage

Signal	2301	3157	Designation	Pin No.	Characteristic
External Read/Write	X		R/$\overline{W}$	M	The contents of the ***Incrementing Register*** are written into the memory of minimum duration 600 nsec. The R/W must be high for reading. Read or write operations require ME high level. (See Note).
External Memory Address Latch	X	X	MAL	R	The data applied to the ten MA lines, A-L, are latched ***on*** the trailing edge of a TTL compatible positive 200 nsec minimum duration pulse. Address data must be quiescent at least 200 nsec prior to the latching edge. (See Note).
External Data Input/ Data Output	X		ED00	6	The least significant bit (2^0) of external data. Coding is TTL high true. Data source must be from either an open-collector or Tri-State source. Input of external data is permitted when ME is in Low State. No internal pull-up resistors are supplied. Data are loaded into ***the Incrementing Register*** by an EXT LD pulse. The 16 ED lines serve as memory data output when ME is in the High State. Outputs will drive one standard TTL load. Length of interconnecting data cables should be limited to 6 feet.

NOTE: The signals $\overline{\text{EXT LD}}$, $\overline{\text{INC REG}}$, R/W and MAL can be applied only during the interval that $\overline{\text{EXT ENB}}$ is low.

J2 Connector Contact Usage

Signal	2301	3157	Designation	Pin No.	Characteristic
External Data Input/ Data Output	X		EDØ1	5	As above but 2^1 bit
" "	X		ED02	7	As above but 2^2 bit
" "	X		ED03	8	As above but 2^3 bit
" "	X		ED04	10	As above but 2^4 bit
" "	X		ED05	9	As above but 2^5 bit
" "	X		ED06	11	As above but 2^6 bit
" "	X		ED07	12	As above but 2^7 bit
" "	X		ED08	14	As above but 2^8 bit
" "	X		ED09	13	As above but 2^9 bit
" "	X		ED10	15	As above but 2^{10} bit
" "	X		ED11	16	As above but 2^{11} bit
" "	X		ED12	18	As above but 2^{12} bit
" "	X		ED13	17	As above but 2^{13} bit
" "	X		ED14	19	As above but 2^{14} bit
" "	X		ED15	20	As above but 2^{15} bit
Memory Overflow	X		MO/F	22	A high level output indicate an overflow in the 16th bit of the memory.
Clock Inhibit		X	CK INH	1	A high TTL inhibits internal clock halting operation use to generate an intensified display marker provided inhibit is synchronous with display sweep.

J2 Connector Contact Usage

Signal	2301	3157	Designation	Pin No.	Characteristic
ADC Data			SEL	S	Active Low TTL signal of 200 nsec duration indicates ADC data is present on pins A to L.
Clear qVt	X		CLR	T	TTL low level of 100 msec minimum duration clears the qvt. EXT.EN. not required.
Start qVt	X		START	U	TTL low of 2 µsec minimum duration starts the qVt EXT.EN. not required.
stop qvt	X		STOP	V	TTL low of 2 µsec minimum duration stops the qVt. EXT.EN. not required.
Display Clock	X		DCLK	W	TTL level display 50 kHz, 400 nsec wide clock pulses available when clock inhibit is low.
Display Reset		X	DR	X	TTL low of 500 nsec duration indicates that the display sweep has begun.
Decrement Register		X	$\overline{\text{DREG}}$	Y	Positive going TTL edge decrements *Incrementing Register.* Internal pull-up is provided.
Zero Register		X	$\overline{\text{ZREG}}$	Z	A TTL low of 500 nsec duration indicates the data in the *Incrementing Register* is zero.
qVt Status	X	STATUS		2	A TTL output indicating the state of the qVt. Low for stopped, high for started.
Common	X	X	GND		

Digital Input/Output

The digital connector, J2 on the 3001 is a 44 contact edge connector which mates with AMP connector number 582358-2. The contacts are named A *thru Z* (excluding G, I, 0 and Q) and.1 through 22. The extreme contacts, A, Z, 1 and 22 are labeled on the board. All signals are TTL standard. Read-out, writing in and histogramming may be performed through this connector. The details and definitions of each of the 44 input or output requirements are described in the next section.

A block diagram of the memory and register section of the 3001 is shown in figure 3.

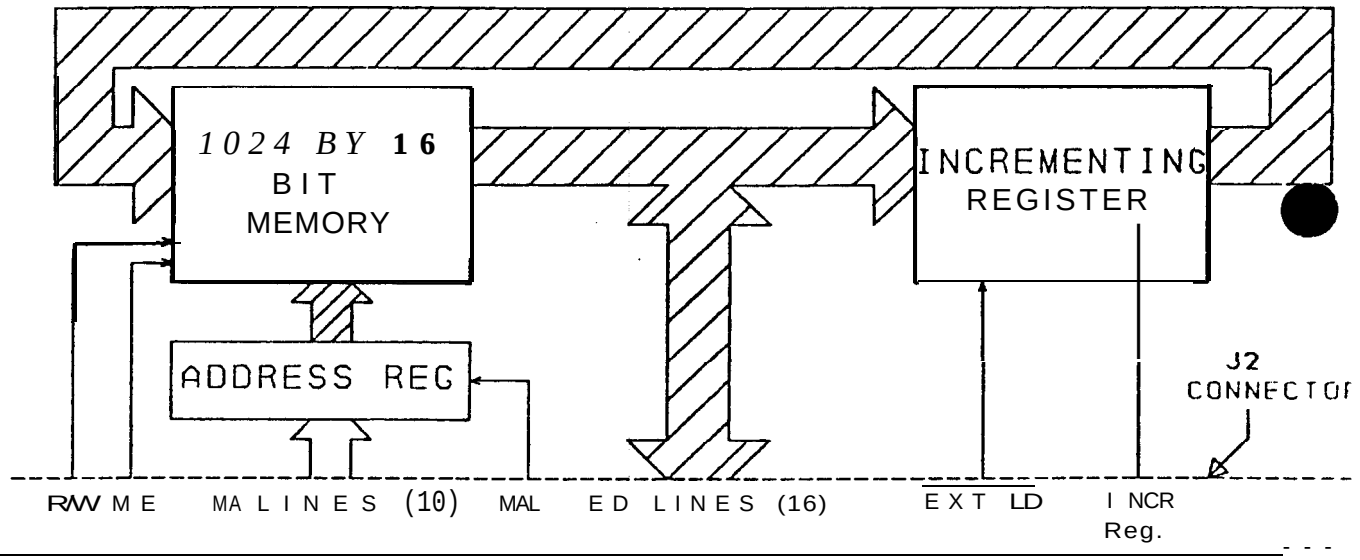


fig. 3

Data may be read from or written into any channel of the 3001 by latching an address into the *Memory Address Latch* and supplying the appropriate strobes.

Latching Into The *Memory Address Latch*

In order to read out or write into the memory of the 3001, it is necessary to latch an address into the *Memory Address Latch.* Tne procedure is shown in figure 4. The memory address lines should be driven from either an open collector or tri-state source activated by a low level on the external line

Data Read-Out (See Figure 4)

If the state of the R/W line is high, the data contained in the address latched into the ***Memory Address Latch*** will settle on the ED lines within 400 nsec of the trailing edge of the MAL pulse. Data levels persist on the ED lines for the duration of the EXT ENB level.

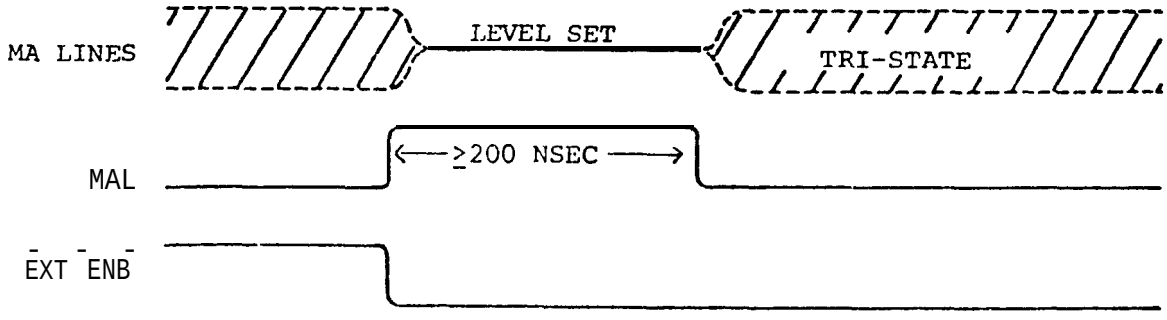


FIGURE 4

Writing Into the Model 3001 (See Figure 5)

In order to write into the Model 3001, data must also be latched into the ***Incrementing Register*** by an EXT LD pulse. Data levels may be set on the ED lines only after the memory is disabled (ME low).

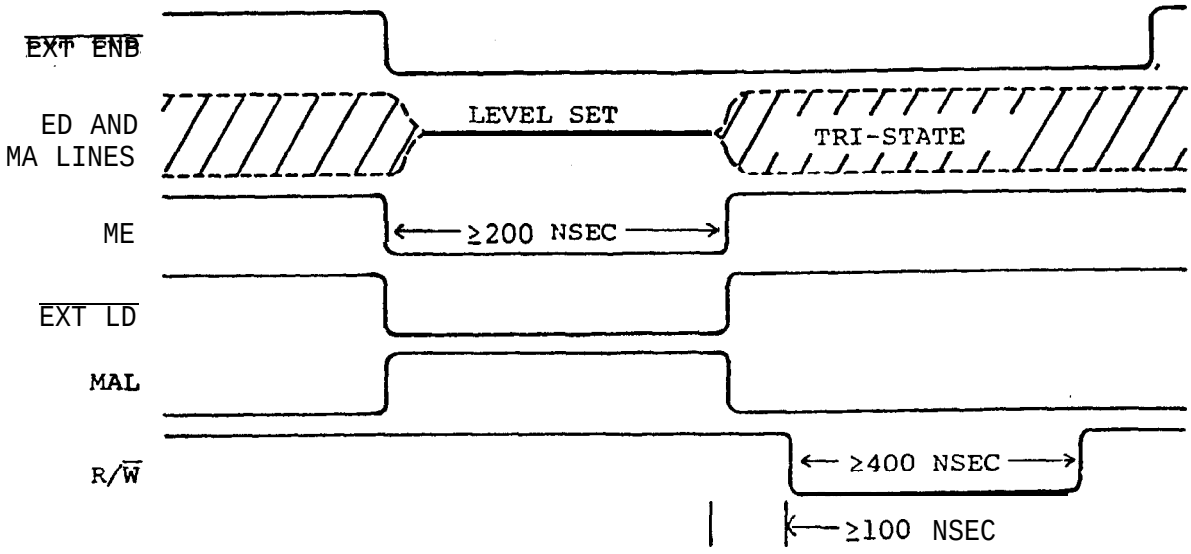


FIGURE 5