CML Microcircuits

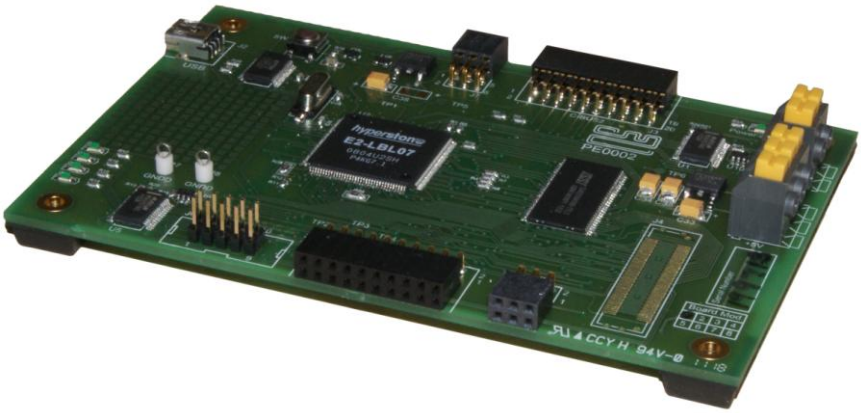
COMMUNICATION SEMICONDUCTORS

PE0002
Evaluation Kit Interface Card

UM0002/5 December 2012 Provisional Issue

Features

- **Global interface for new generation IC evaluation kits**
- **Target IC C-BUS read and write operations**
- **32-Bit RISC/DSP Microprocessor based operation**
- **Mating interface for wide range of target evkit boards**
- **PC GUI and hardware provided**
- **Function Image™ handling for *FirmASIC*®-based projects**
- **High-speed real-time script execution**
- **PC control/communications via USB**
- **Software configurable GPIO lines and LED bank**



1 Brief Description

The PE0002 EvKit interface card is a global interface system for use with evaluation kits for CML's new generation ICs, including *FirmASIC*®–based products. This greatly simplifies the approach to the evaluation and design-in process.

Based around the operation of Hyperstone's E2 32-bit RISC/DSP Microprocessor and using a PC GUI, the information generated is formatted, timed and delivered to the target IC via its Evkit's C-BUS serial interface. The supplied control software can be used to perform C-BUS read and write operations or to run scripting functions.

In the case of *FirmASIC*® IC evaluations, the Function Image™ can be loaded onto the CMX{target} device or programmed into serial memory on the {target} card.

Communications with the evaluating PC GUI are via a USB port.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

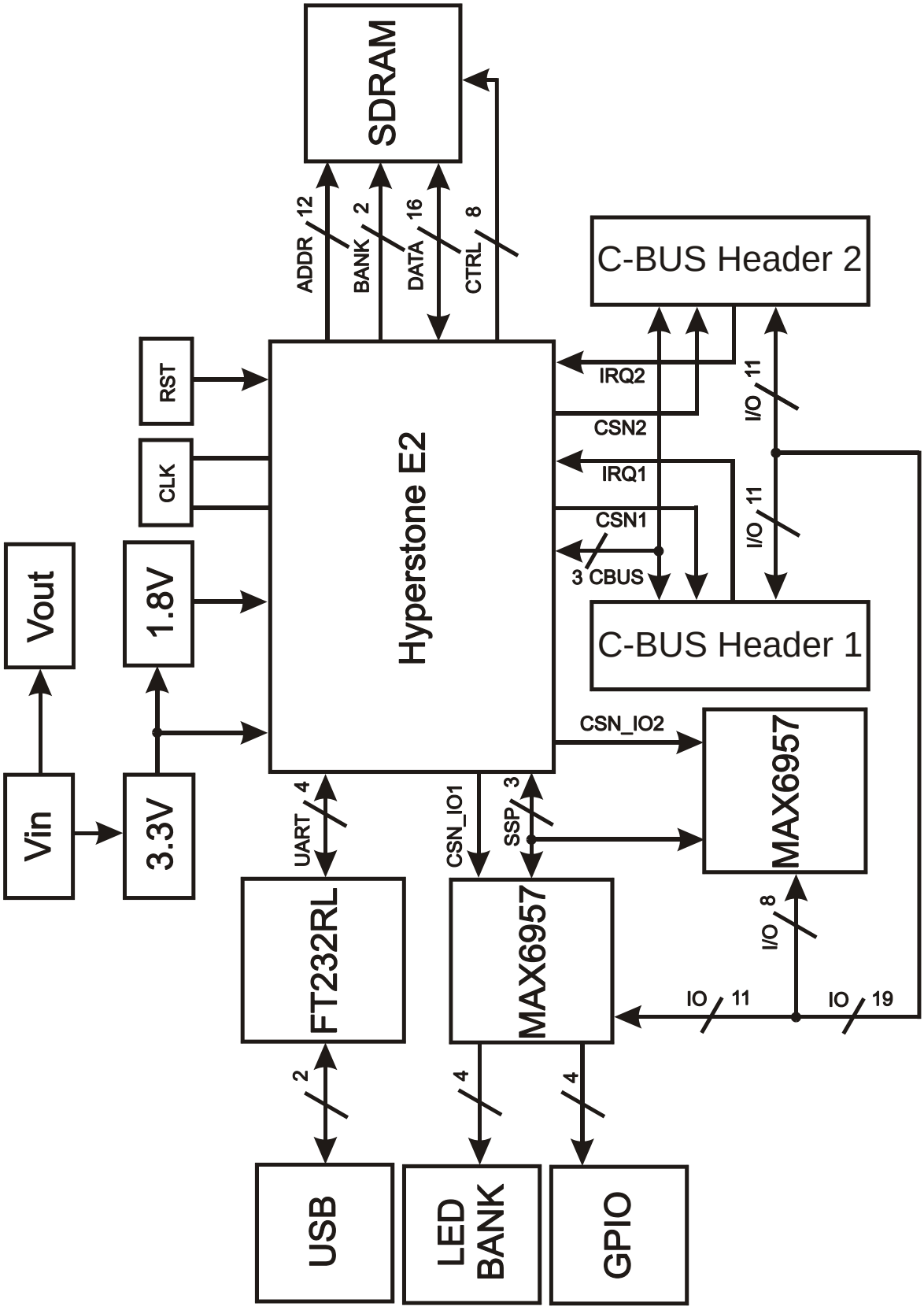


Figure 1 Block Diagram

2. Preliminary Information

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

2.1.1 Power Supply

A 5 Volt dc un-regulated power supply.

2.1.2 PC

With the following requirements:

- One of the following Windows operating systems installed: 2000sp4, XPsp2, 32-bit Vista or 32-bit Win7.
- USB port.
- Minimum screen resolution 800 x 600. Recommended resolution 1024 x 768.

2.1.3 USB type A male to mini B male cable

2.2 Precautions

Like most evaluation kits, this product is designed for use in a laboratory environment. The following practices will help ensure its proper operation.

2.2.1 Static Protection

This product uses low power CMOS circuits which can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items detailed on the separate information sheet (EK0002) and notify CML within 7 working days if the delivery is incomplete.

3. Quick Start

This section provides instructions for users who wish to experiment immediately with the evaluation kit. A fuller description of the kit and its use appears later in this document.

3.1 Setting-Up

- Copy the file 'ES0002xx.zip', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect the PE0002 Interface Card to the Target Card, via the right angle connector, J5 or J3.
- Connect a dc supply to the PE0002 Interface Card and set to the voltage level to 5V.
- Connect a dc supply to the Target Card and set to the voltage level specified in the relevant Target Card User Manual.
- Attach a USB cable between connector J2 of the PE0002 Interface Card and the USB port of the PC.
- Turn on the power supply. The power-on indicator D6 will light.
- Install the USB driver when requested. The driver is in the same folder where the 'ES0002xx.zip' files were extracted to '..\Driver'. Follow instructions on the screen to install the USB driver. Click the 'Continue Anyway' button when the Message Box below is displayed.

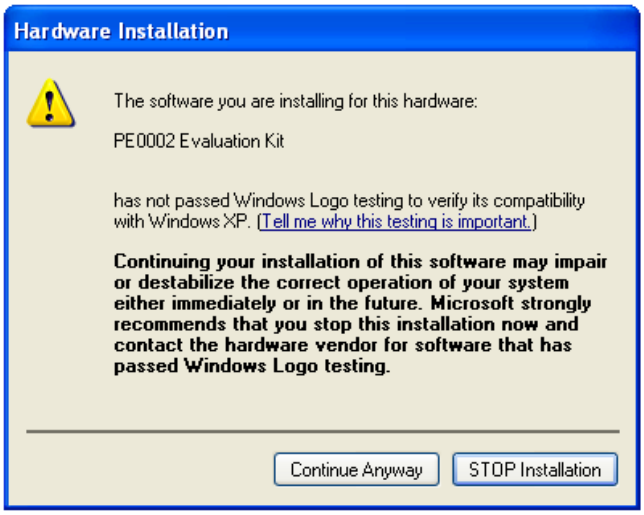


Figure 2 USB Driver Installation Message Box

3.2 Adjustments

None.

3.3 Operation

- Run the application ES0002xx.exe.
- Press the reset switch (SW1) on the PE0002 board when requested.

4. Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J2	1	VBUS		USB Mini B type connector - USB power supply
	2	D-		USB Mini B type connector - USB data signal minus
	3	D+		USB Mini B type connector - USB data signal plus
	4	n/c		
	5	GNDD		USB Mini B type connector - Digital ground
	6	SHELL		USB Mini B type connector - USB connector shell
	7	n/c		
J3	1	IO8	BI	Spare I/O
	2	CSN2	O/P	C-BUS chip select
	3	IO9	BI	Spare I/O
	4	CDATA	O/P	C-BUS command data
	5	IO10	BI	Spare I/O
	6	SCLKCBUS	O/P	C-BUS serial clock
	7	IO11	BI	Spare I/O
	8	RDATA	I/P	C-BUS reply data
	9	IO12	BI	Spare I/O
	10	IRQN2	I/P	C-BUS interrupt request
	11,12	GNDD	Power	Digital ground
	13	BOOTEN1	O/P	Hardware boot control
	14	BOOTEN2	O/P	Hardware boot control
	15	RS232/C-BUS	O/P	Hardware boot control
	16	IO13	BI	Spare I/O
	17	IO14	BI	Spare I/O
	18	IO15	BI	Spare I/O
	19, 20	n/c		

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J5	1	IO0	BI	Spare I/O
	2	CSN1	O/P	C-BUS chip select
	3	IO1	BI	Spare I/O
	4	CDATA	O/P	C-BUS command data
	5	IO2	BI	Spare I/O
	6	SCLKCBUS	O/P	C-BUS serial clock
	7	IO3	BI	Spare I/O
	8	RDATA	I/P	C-BUS reply data
	9	IO4	BI	Spare I/O
	10	IRQN1	I/P	C-BUS interrupt request
	11,12	GNDD	Power	Digital ground
	13	BOOTEN1	O/P	Hardware boot control
	14	BOOTEN2	O/P	Hardware boot control
	15	RS232/C-BUS	O/P	Hardware boot control
	16	IO5	BI	Spare I/O
	17	IO6	BI	Spare I/O
	18	IO7	BI	Spare I/O
	19, 20	n/c		
J6	1	GPIO0	BI	Spare I/O
	2	n/c		
	3	GPIO1	BI	Spare I/O
	4	n/c		
	5	GPIO2	BI	Spare I/O
	6	n/c		
	7	GPIO3	BI	Spare I/O
	8	n/c		
	9	GNDD	Power	Digital ground
	10	VCC3V3	Power	+3.3V power supply
J7	1, 2	GNDD	Power	Digital ground
	3, 4, 5, 6	VCCIN	Power	+5.0V power supply

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J8	1	GNDD	Power	Digital ground
	2	VCCIN	Power	+5.0V power supply
J9	1,2	GNDD	Power	Digital ground
	3, 4, 5, 6	VCCIN	Power	+5.0V power supply
J10	1	GNDD	Power	Digital ground
	2,3	VCCIN	Power	+5.0V power supply

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	VCC1V8	+1.8V power supply to the core of the E2 Microprocessor
TP2		Not used
TP3		Not used
TP4		Not used
TP5	CLKOUT	Clock signal output of the E2 Microprocessor
TP6	VCC3V3	+3.3V power supply
TP7	GNDD	Digital ground
TP8	GNDD	Digital ground

SWITCHES		
Switch Ref.	**Default Position**	**Description**
SW1	O/C	Push to reset the E2 Microprocessor

Notes: I/P = Input
O/P = Output
BI = Bidirectional
O/C = Open circuit

5. Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as a separate high resolution pdf file. This can be found on the CML website.

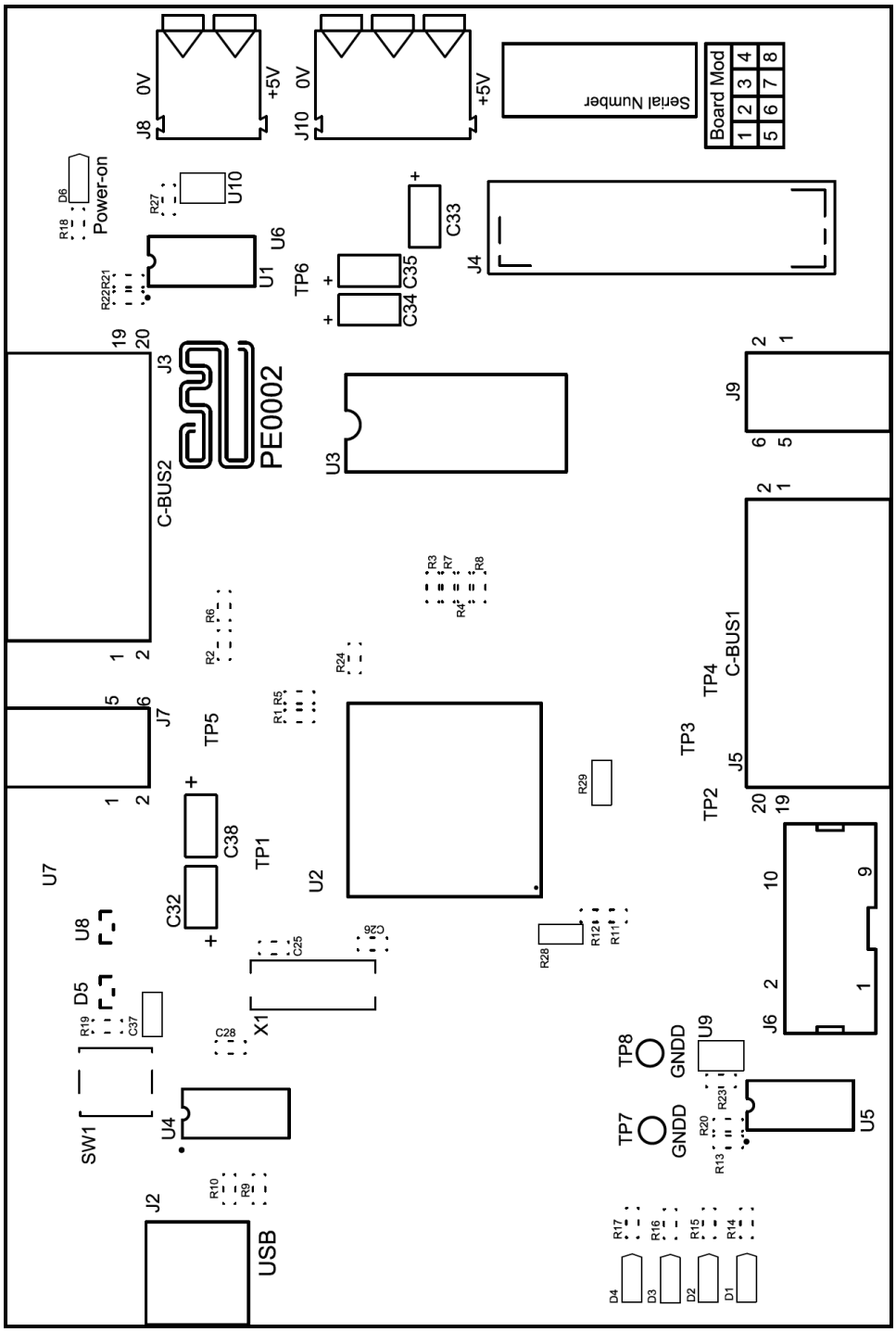


Figure 3 PE0002 Interface Card Layout

6. Detailed Description

6.1 Hardware Description

The board is fitted with two voltage regulators. U6 and U7 provide the +1.8V and +3.3V digital supply rails respectively. The input to these two regulators is provided by an external un-regulated power supply at, nominally, 5V dc, which is connected to the board via connector J8 (2 position terminal block). The external un-regulated power supply is available at connector J10 (3 position terminal block) and connectors J7 and J9 (right angle female headers).

The +1.8V and +3.3V supply voltage levels can be monitored on test points TP1 and TP6 respectively.

Digital ground can be monitored on test points TP7 and TP8.

D6 will illuminate, confirming presence of the on-board regulated +3.3V dc digital voltage supply.

The PE0002 Interface Card is based around the Hyperstone E2 32-Bit RISC\DSP Microprocessor. There are 32kBytes of RAM on-chip and 64Mbits of external SDRAM.

The board uses the fitted 20MHz crystal as the clock source for the E2 Microprocessor.

Two C-BUS outputs, J3 and J5, are provided for control of up to two CMX{target} devices on the selected {target} cards. The C-BUS signals, 3 boot control signals and 16 I/O signals are brought out on these connectors and can be programmed in the GUI.

There are 4 software configurable general purpose I/O signals connected to the output J6 and 4 software configurable LEDs.

The link to a host PC is via a full speed USB 2.0 port.

Note: PE0002 uses a high-performance microprocessor so the 20MHz crystal is used with an on-chip PLL to generate internal clock frequencies, including 45MHz and 160MHz. As the PCB is unscreened, electromagnetic energy (radiated or conducted) could affect the RF performance of Development Boards or Evaluation Kits which are connected to the PE0002. Appropriate screening measures may need to be taken by the customer in order to minimise the interference to sensitive circuits. It should also be noted that the precise interference effects will vary depending on the activity of the microprocessor.

6.1.1 C-BUS Interface

The C-BUS interface provides for the transfer of data and control or status information between the target device's internal registers and the Microprocessor over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the Microprocessor, which may be followed by one or more data byte(s) sent from the Microprocessor to be written into one of the target device's registers, or one or more byte(s) of data read out from one of the target device's registers, as illustrated in Figure 4.

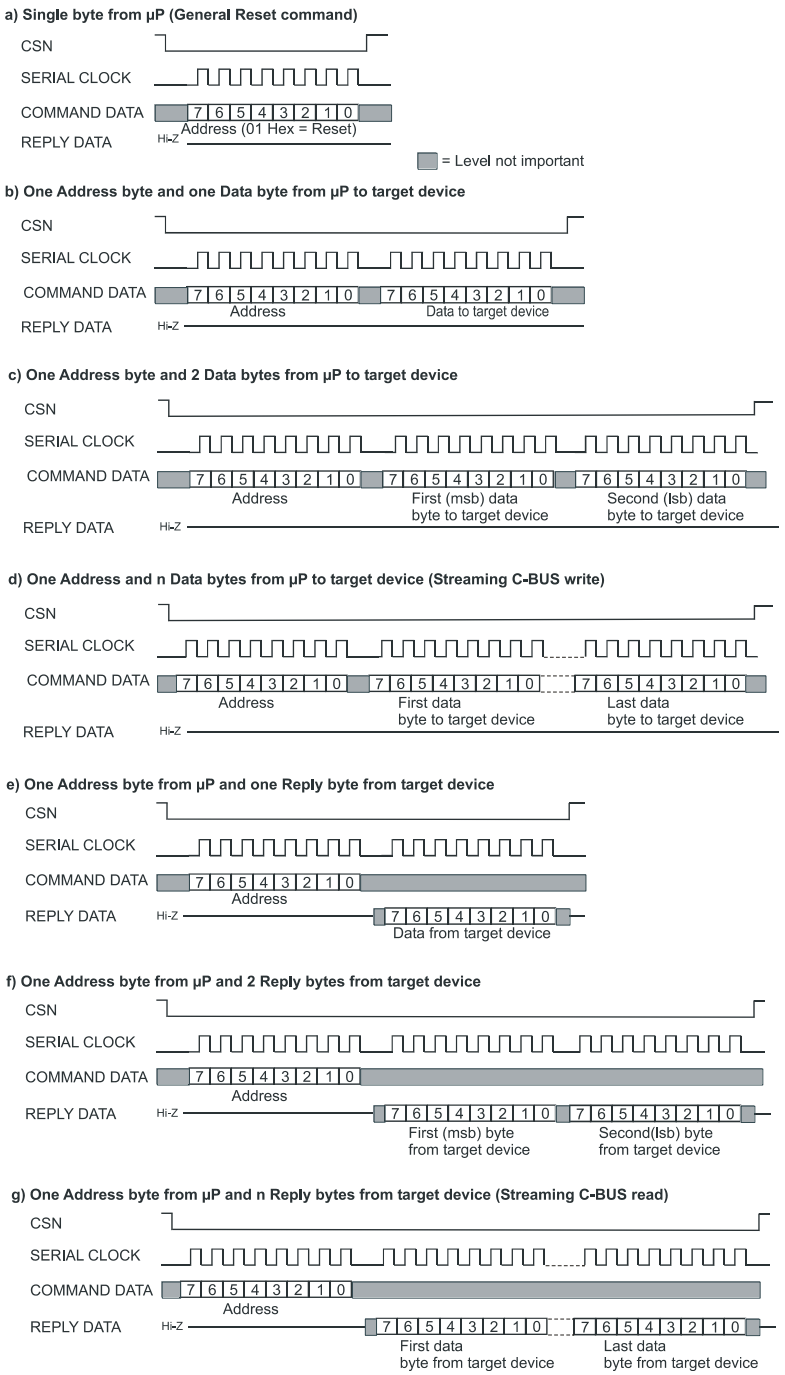


Figure 4 C-BUS Transactions

All writes and reads to the C-BUS output occur via the Serial Interface Engine of the E2 Microprocessor.

Two different CMX{target} devices can be selected by taking CSN1 or CSN2 low on connectors J5 and J3 respectively.

The CMX{target} device can issue an interrupt by taking IRQN1 or IRQN2 low on connectors J5 and J3 respectively.

6.2 Adjustments and Controls

None.

6.3 Embedded Software Description

On power up the Microprocessor will monitor the USB port to download the Firmware from the host PC to the internal RAM of the Microprocessor and the external SDRAM and will jump to the start address of the Firmware when requested by the host PC.

6.4 Software Description

A single executable 'ES0002xx.EXE' running in a Windows environment supports a range of Target Cards. Visit the CML website for the latest information.

When the ES0002xx.EXE application is run, if communication cannot be established a message box will be displayed to indicate the failure. If the message box in Figure 5 is displayed, press the Reset Switch SW1 on the PE0002. The Firmware is automatically downloaded to the PE0002 board and a tabbed dialog box is then displayed, which is the main application dialog.

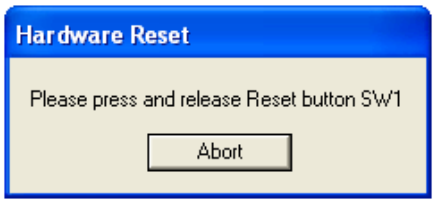


Figure 5 Start Message Box

There are six sheets within the tabbed dialog box structure and these are described in the following sections.

More than one PE0002 can be connected to a single PC. When plugging in an additional PE0002, Windows will request suitable drivers. Use the 'Let Windows search for drivers' option as these will already be available from the initial installation. A separate instance of the GUI must be started. The PC resources will be shared between each PE0002.

6.4.1 The C-BUS Control Tab

This tab provides basic C-BUS read, write and general reset functions. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The radio buttons select an 8-bit or 16-bit read/write operation. The lengths of the entered values are limited to 2 characters (1 byte) for read or write register addresses and 2 or 4 characters (1 or 2 bytes) for the register write data. The General Reset button writes 01_H to the CMX{target} device. The radio buttons select read/write operation to the CMX{target} device 1 using CSN1 on connector J5 or to the CMX{target} device 2 using CSN2 on connector J3.

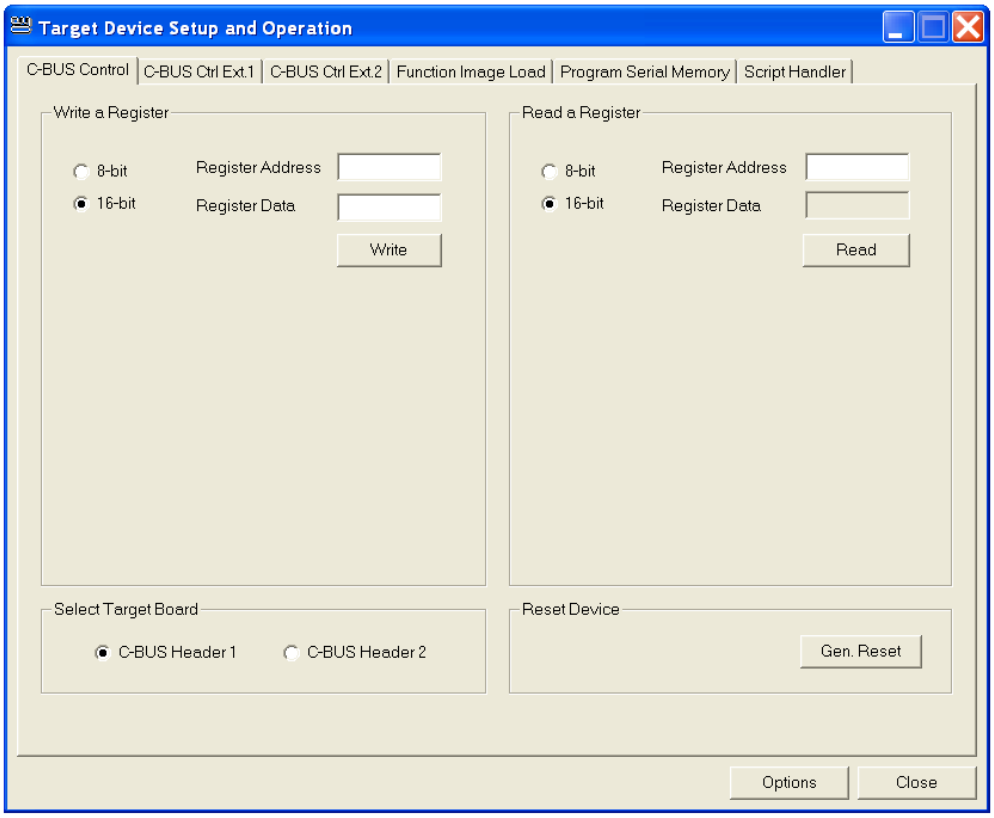


Figure 6 C-BUS Control Tab

6.4.2 The C-BUS Control Extended Tab (C-BUS Ctrl Ext. 1 and 2)

This tab provides multiple C-BUS read and write functions. Each row in the table represents a single C-BUS register. Select the C-BUS register type from the drop down list. The Update button and the Data edit box will be configured according to the selection. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The lengths of the entered values are limited to 2 characters (1 byte) for register addresses and 2 or 4 characters (1 or 2 bytes) for the register data. Click the Update button to read or write a single C-BUS register. For multiple C-BUS read or write operations select the C-BUS registers using the Selected check boxes and click on the 'Wr all', 'Rd all' or 'Wr\Rd all' buttons. Click on the 'Wr all' button to write all the selected write type C-BUS registers. Click on the 'Rd all' button to read all the selected read type C-BUS registers. Click on the 'Wr\Rd all' button to read or write all the selected C-BUS registers.

Click on the 'Clear all' button to reset the table. Click on the 'Clear data' button to reset the Data edit boxes.

When the ‘Lock’ button is selected the Description, Address and Type controls are disabled, preventing accidental changes.

Use the ‘Save Config…’ button to save the current table. The Description, Address, Type, Data and Select columns are saved in the specified file. Use the ‘Open Config…’ button to load a previously saved table.

The radio buttons select read/write operation to the CMX{target} device 1 using CSN1 on connector J5 or to the CMX{target} device 2 using CSN2 on connector J3.

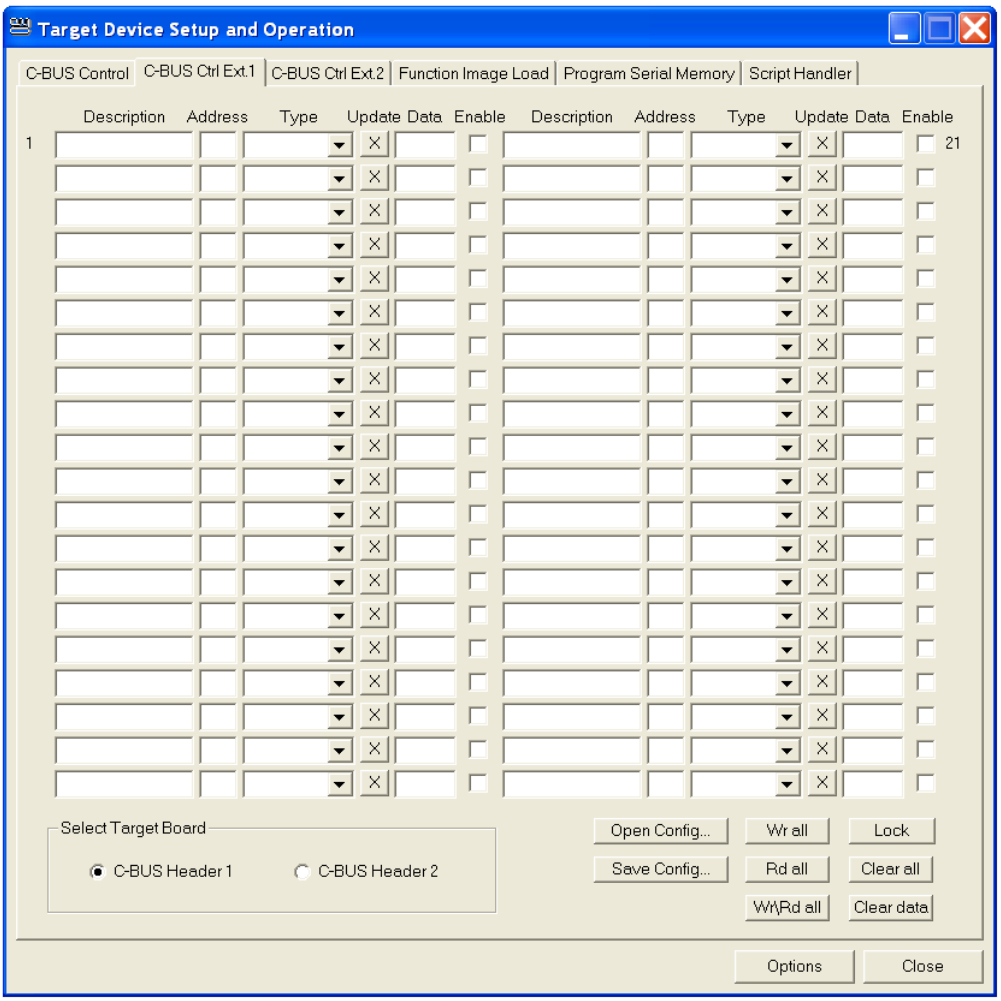


Figure 7 C-BUS Control Extended Tab

6.4.3 The Function Image™ Load Tab

This tab provides Function Image™ load and activation utilites for *FirmASIC*® products. The operation of this tab is described in the user manuals of the {target} cards to which it applies.

6.4.4 The Serial Memory Programming Tab

This tab provides a serial memory programming facility for *FirmASIC*® {target} cards where a serial EEPROM or flash memory can be used for non-volatile storage of a Function Image™. The operation of this tab is described in the user manuals of the {target} cards to which it applies.

6.4.5 The Script Handler Tab

The Script Handler tab allows the execution of scripts. These are plain text files on the PC which are compiled by the GUI, but executed on the E2 Microprocessor on the board. The script language is documented separately in the “Script Language Reference” document, which can be downloaded with the PE0002 support package from the CML website.

To select a script file, click on the ‘Select Script’ button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on ‘>’ button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the ‘Save Results’ or ‘Clear Results’ buttons, respectively. When a script file is being executed the ‘Run Script’ button will change to be the ‘Abort’ button, the rest of the tab will be disabled and the other tabs cannot be selected.

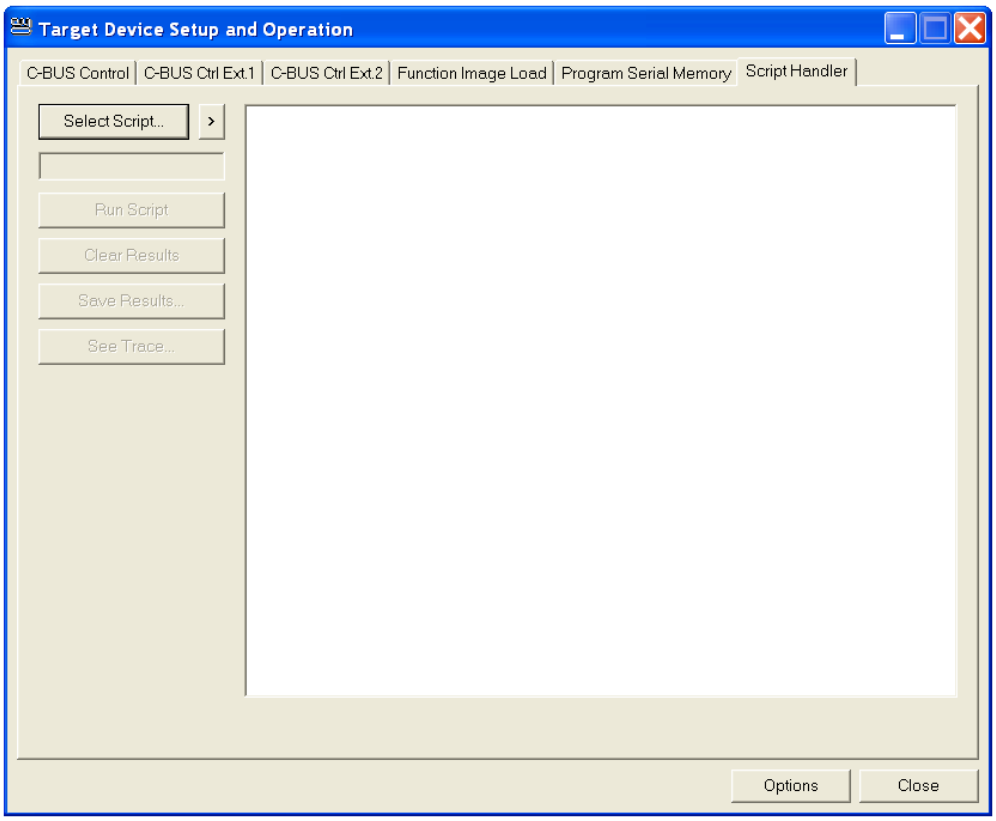


Figure 8 Script Handler Tab

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Up to 131072 C-BUS transactions can be logged in the PE0002 board. Click in the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.

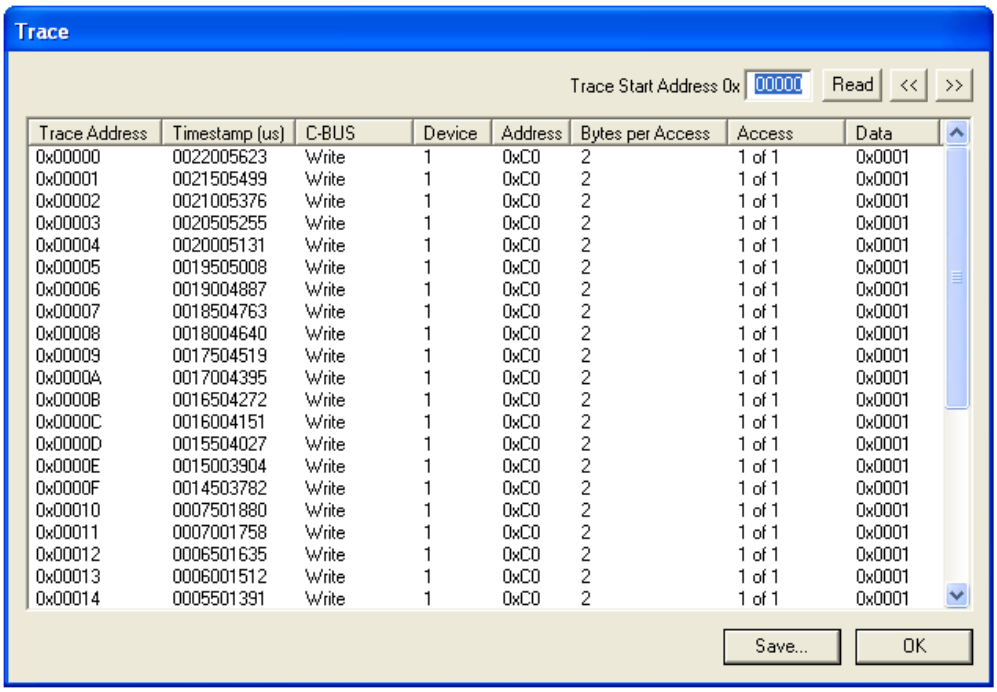


Figure 9 Trace Dialog Box

Click on the '>>' or '<<' buttons to upload and display the next or previous C-BUS transaction data block. Click on the 'Read' button to upload and display the C-BUS transaction data block starting at the address displayed in the Trace Start Address edit box. Use the 'Save…' button to save the trace data to a file.

6.4.6 The Options Dialog Box

Click on the 'Options' button on the main application dialog to display the 'Options' dialog box.

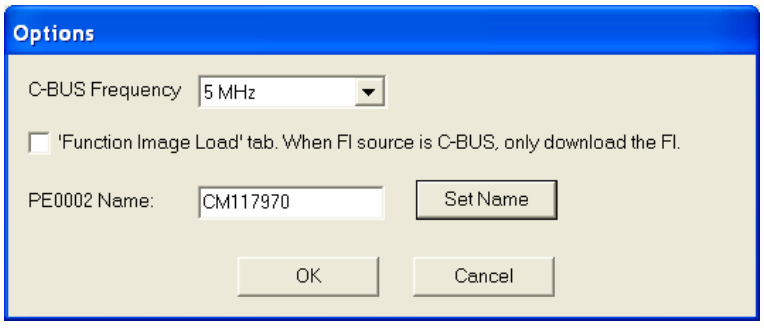


Figure 10 Option Dialog Box

Use the 'C-BUS Frequency' drop down list to select the C-BUS clock frequency for all C-BUS transactions between the PE0002 and the {target} card. This options is set to 5MHz by default.

With the ‘Function Image Load tab. When FI source is C-BUS, only download the FI’ checkbox selected, no Activation Code, Checksum or Status register checking is performed when a Function Image™ is downloaded to the {target} card using the C-BUS source in the Function Image™ Load tab.

The PE0002 Name option allows the software to give a name to the PE0002 board. The name is displayed in the caption of the main window.

6.5 Evaluation Tests

Details of any {target} cards specific tests are included in the relevant {target} cards user manual.

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (VCCIN - GNDD)	-0.3	5.5	V
Voltage on any connector pin to GNDD	-0.3	3.6	V
Current into or out of VCCIN and GNDD pins	-50	+300	mA
Current into or out of any other connector pin	-20	+20	mA
Storage Temperature	-10	+70	°C
Operating Temperature	+10	+35	°C

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (VCCIN - GNDD)		4.8	5.5	V
Operating Temperature		+10	+35	°C
Xtal Clock Frequency		19.99	20.01	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 20MHz
VCCIN = 5.0V, Tamb = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{CCIN} (not powersaved)	1, 2		150	250	mA
I/O pins					
Input logic "1" level	3	70%			3.3V
Input logic "0" level	3			30%	3.3V
Input leakage current	3	-100	±1	+100	nA
Output Logic '1' Level at I_{OH} = 1.6 mA	3	2.8			V
Output Logic '0' Level at I_{OL} = -1.5 mA	3			0.4	V
C-BUS Interface					
Input logic "1" level	4	2.9		3.6	V
Input logic "0" level	4	-0.3		0.6	V
Input leakage current	4			±10	µA
Output leakage current	4			±10	µA
Output Logic '1' Level at I_{OH} = 1.0 mA	4	2.4			V
Output Logic '0' Level at I_{OL} = -4 mA	4			0.45	V
Input/Output Capacitance	4			10	pF
C-BUS clock frequency		1.0	5.0	10.0	MHz

Notes:

1. Not including any current drawn from the output pins by external circuitry.
2. No Target Card connected.
3. RS232/CBUS, BOOTEN1, BOOTEN2, GPIO0, GPIO1, GPIO2, GPIO3, IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO8, IO9, IO10, IO11, IO12, IO13, IO14 and IO15.
4. CSN1, CSN2, IRQN1, IRQN2, RDATA, CDATA and SCLKCBUS pins.

Infinite Capabilities . . .
FirmASIC®
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About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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