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sercos EasySlave-IO Evaluation kit

User Manual

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Abstract:
This document is a technical manual for the sercos EasySlave-IO Evaluation Kit. It contains detailed information of the EasySlave Modules.

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Revision History

Date	Version	Revision	Authors
11.09.2012	0.1	Document created	C. Hayer
17.09.2012	0.2	Connector pinouts added	C. Hayer
19.11.2012	0.3	Technical Data	C. Hayer

Contents

1 Definitions and abbreviations

Definition	Description
FPGA	Field-programmable gate array is a device where the logic network can be programmed into the device after its manufacture. An FPGA consists of an array of logic elements, either gates or lookup table RAMs, flip-flops and programmable interconnect wiring.
sercos III	third generation sercos is an industrial standard which specifies real-time Ethernet communication for automation.
EasySlave	A free IP core for low-cost FPGA chips, which allows SERCOS III to be integrated into basic I/O slave devices with minimal development and integration effort.
FSP IO	Function Specific Profile IO is a sercos III device profile for I/O applications.
S/IP	All IPS services, which are based on TCP and UDP.
TFTP	Trivial File Transfer Protocol is a very simple file transfer protocol which is typically based on UDP.
SDDML	sercos Device Description Markup Language is a markup language, which contains sercos III-defined tags, in order to describe the functionality that a sercos III device supports, in the form of an XML file.
IDN	Identification number of a SERCOS parameter.
UC channel (UCC)	Unified Communication Channel, Standard Ethernet Frames like UDP & TCP will be transmitted and services like Ping will be transmitted also.
RT channel	Real-time channel is a certain time span of the communication cycle in which real-time telegrams are sent.
Ethernet	A widely used type of local area network and compatible to ISO/IEC 8802-3 standard.
Hot-plug	Possibility to insert a slave in the sercos III network, inclusive its initialization, while the sercos III network is running.

2 Introduction

2.1 Sercos – the automation bus

Industrial Ethernet has become the de facto standard for manufacturing information networking, and the market is requesting Ethernet connectivity for servo drives. Ethernet offers high-speed data throughput at 10-100 times faster than fieldbus solutions. It uses standard off-the-shelf components and cabling and offers consistent IT implementation from office to the machine level. The problem is that Industrial Ethernet is characterized by high bandwidth and low hardware costs, but is not deterministic. Office communications and certain single-axis motion applications can tolerate delays and data re-transmissions, but that would be disastrous for coordinated multi-axis robots or high-speed machine tools.

The sercos automation bus, on the other hand, is optimized for high-speed deterministic motion control, which is required for the exact synchronization of multiple drives. Sercos also defines a protocol structure and includes an ample variety of profile definitions for control of motion and I/O devices.

Sercos III is the open, IEC-standardized third-generation of sercos that "right engineers" Industrial Ethernet for real-time control, combining the best of both Ethernet and previous Sercos designs to provide the highly deterministic bi-directional real time motion and I/O control required by modern production equipment. It overcomes the wasted bandwidth in other TCP/IP-based Ethernet bus solutions, because it is based directly on Ethernet frames, defining a new, registered EtherType for sercos. In addition to real-time communications between all drives and the motion control, sercos III provides rich I/O communication capabilities, while also enabling other protocols, such as EtherNet/IP, TCP/IP, UDP and others, to be transmitted over the same Ethernet network efficiently in parallel with sercos real-time communication. Sercos III is a truly a universal automation bus for machine production and system implementation.

Sercos III offers several fundamental performance and technology benefits for OEMs and end-users:

- Cycle times as low as 31.25 microseconds.
- High speed: it uses Fast Ethernet (100 Mb/s).
- Support for either line or ring topologies; in addition hierarchical, synchronized and real-time coupled network structures can be implemented.
- Support for up to 511 slave devices in one network, with multiple networks possible in a system.
- Bumpless cable break recovery in ring mode within 25 microseconds.
- Advanced cross communications—both slave-to-slave and controller-to-controller (sometimes called machine-to-machine).
- Capable of hot-plugging devices and network segments—adding machine or line components to a network with synchronization up and running, without having to reset the network or cycle power.
- Support for safety functions up to SIL3 according to IEC 61508 via CIP Safety for sercos.
- I/O profile that provides an XML-based device and profile description language for I/O device configuration.
- Energy profile that defines parameters and commands for the reduction of energy consumption in a uniform vendor-independent manner.
- Encoder profile that provides a standard method to integrate encoders into a sercos III network.
- Lower hardware costs.

There are several key advantages that manufacturers, systems engineers and machine builders can leverage when using sercos III—advantages that enable drive and control systems with vastly improved flexibility and performance.

2.2 Sercos EasySlave

The sercos EasySlave is an FPGA-based single-chip controller, enabling inexpensive development of simple sercos III slave devices such as I/O. I/O applications are synchronized in the sercos cycle. An IP core is provided as a netlist for the Xilinx Spartan-6 FPGA family. The IP core contains all the functions of a sercos slave connection, including the associated software library for I/O devices (e.g., analog inputs, encoders). The user can add IP cores for I/O from Xilinx and his own application code and can integrate the controller into his own board. A reference design is available.

Technical support for the EasySlave is provided by Steinbeis-Transferzentrum Systemtechnik (TZS) in Esslingen, Germany. TZS offers an EasySlave evaluation kit to facilitate a quick and easy introduction to Sercos slave development. The evaluation kit includes a development board based on a Xilinx Spartan-6 XC6SLX25 FPGA and can be extended using plug-in modules. The evaluation kit includes all other required material and documents (Ethernet cable, power supply, and documentation). TZS can provide assistance in the integration and commissioning of EasySlave.

Features and Specifications for EasySlave FPGA-based Single-Chip Controller

- FPGA-based single chip controller containing a reduced sercos slave IP core
- Target devices: analog/digital I/Os, simple sensors and actuators
- FPGA-internal RAM for sercos stack, application and data
- Real-time channel with max. 32 bytes output and max. 32 bytes input data (1 input and 1 output connection)
- Supported cycle times down to 31,25 µs
- Synchronization of application to sercos cycle
- Parameterization over service channel
- Hot-plug support
- Service channel with hardware support
- IP channel for ARP, Ping and firmware update over TFTP
- Design currently targeted to Xilinx Spartan-6 FPGA series
- FPGA reference design (Xilinx EDK V13.4) and Software-API (Xilinx MicroBlaze / gcc) available

Various EasySlave licensing models are available from sercos international, with sercos member companies offered special prices. In addition, a license-free IP core version (loaded with a bitstream IP core) with a limited functionality is available, under the product name EasySlave-IO.

3 EasySlave-IO Evaluation kit

The EasySlave-IO Evaluation kit consists of a development board and the necessary accessories. The development board is designed for an easy start into the sercos slave development. The development board has a modular concept which can be easy extended by other modules.

The sercos EasySlave Evaluation Kit includes:

- EasySlave FPGA-Modul base board, including XILINX Spartan-6 XC6SLX25-FT256 FPGA
- EasySlave AddOn Module ETH-Connect with two RJ45 Ethernet connectors
- EasySlave 24V I/O interface board
- Documentation:
  - sercos EasySlave Evaluation Kit – Getting Started Guide
- Cable and power supply:
  - AC power adapter (24 V_{DC})
  - Two CAT6 Ethernet cables
- USB flash drive with documentation, reference designs, software tools and board files

Figure: EasySlave Evaluation-Kit

The development board is a fully functional sercos slave and can be used as a reference design for new IO slave devices.

4 EasySlave Modules

The EasySlave-IO development board consists of the following modules:

- **EasySlave FPGA-Modul**
- **EasySlave AddOn ETH-Connect**
- **EasySlave IO-Modul**

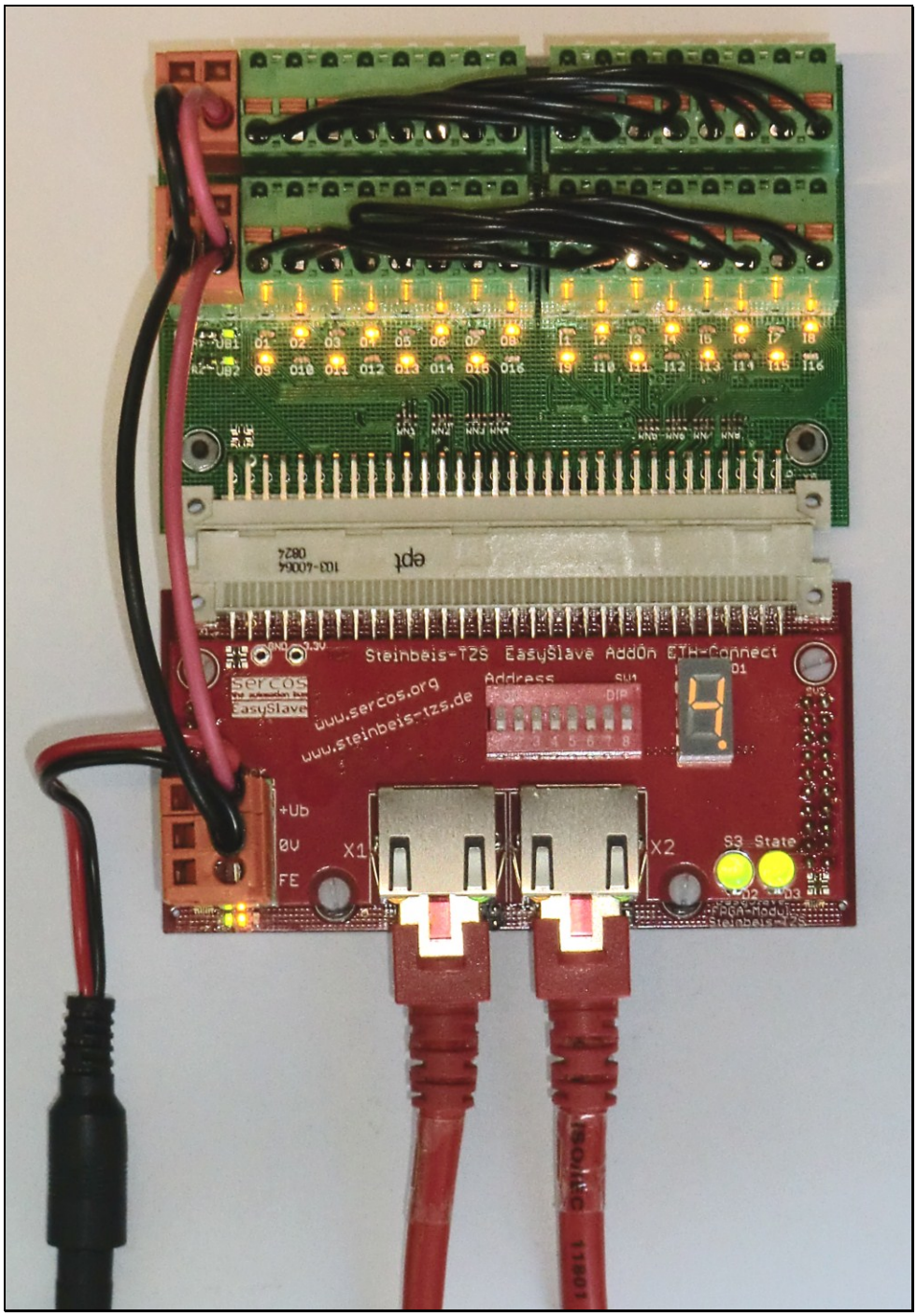
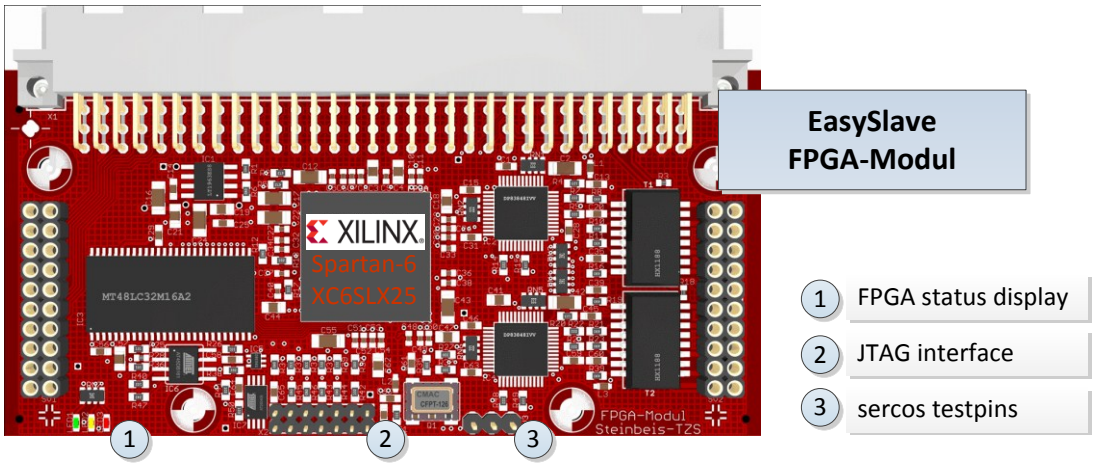


Figure: EasySlave Development Board

4.1 EasySlave FPGA-Modul

This module is the core of the EasySlave and contains the FPGA, the flash memory and the Ethernet PHYs.



4.1.1 FPGA status display

On the FPGA-Module are three colored LED's.

- Green: Power supply for FPGA is OK (3.3V)
- Yellow: FPGA is active (application started)
- Red: Power reset required (fatal error or after firmware update)

4.1.2 JTAG interface

The JTAG interface is for programming, debug and tracing the FPGA. This interface is for development use only. The interface is compatible to the XILINX Platform Cable USB II ribbon cable.

Connector X2 – JTAG (2x7 2.0mm grid)							
Pin	1	3	5	7	9	11	13
Signal	GND	GND	GND	GND	GND	GND	GND
Pin	2	4	6	8	10	12	14
Signal	VCC	TMS	TCK	TDO	TDI	n.c.	n.c.

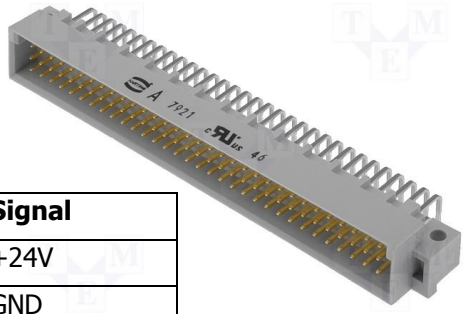
4.1.3 Sercos testpins

The sercos standard specifies two hardware testpins for debugging if IP core signals.

Connector SV3 - Testpins			
Pin	1	2	3
Signal	GND	TST0	TST1

4.1.4 FPGA Interface

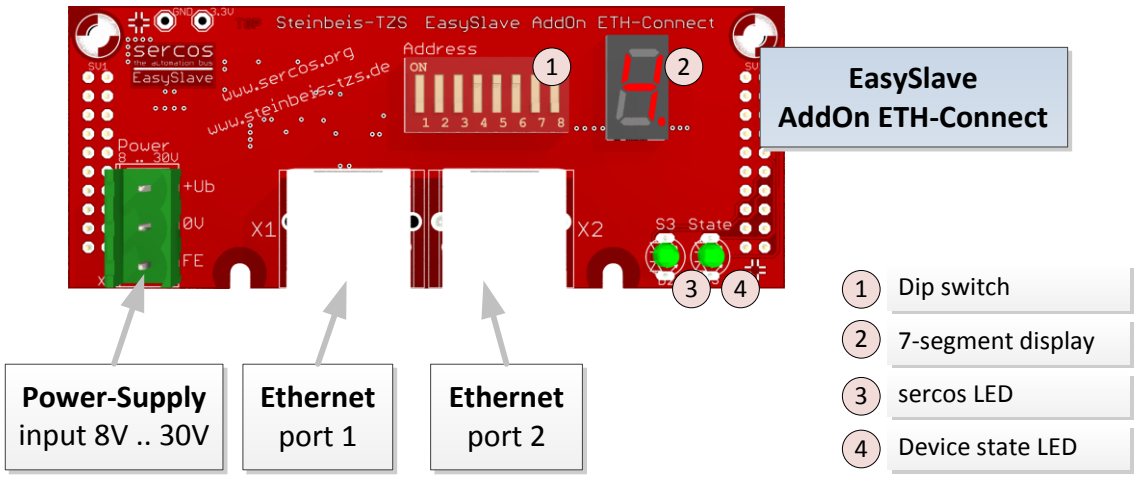
96 way DIN41612 connector, male



Row A	Signal	Row B	Signal	Row C	Signal
A1	+24V	**B1**	DIP_SW_1	**C1**	+24V
A2	GND	**B2**	DIP_SW_2	**C2**	GND
A3	SPI_MOSI	**B3**	DIP_SW_3	**C3**	SPI_MISO
A4	SPI_CLK	**B4**	DIP_SW_4	**C4**	SPI_CS0
A5	SPI_CS1	**B5**	DIP_SW_5	**C5**	SPI_CS2
A6	EXT0	**B6**	DIP_SW_6	**C6**	EXT1
A7	EXT2	**B7**	DIP_SW_7	**C7**	EXT3
A8	EXT4	**B8**	DIP_SW_8	**C8**	EXT5
A9	EXT6	**B9**	7SEG_DISP_P	**C9**	EXT7
A10	EXT8	**B10**	7SEG_DISP_A	**C10**	EXT9
A11	EXT10	**B11**	7SEG_DISP_B	**C11**	EXT11
A12	EXT12	**B12**	7SEG_DISP_C	**C12**	EXT13
A13	EXT14	**B13**	7SEG_DISP_D	**C13**	EXT15
A14	UART_RX	**B14**	7SEG_DISP_E	**C14**	UART_TX
A15	IO0	**B15**	7SEG_DISP_F	**C15**	IO1
A16	IO2	**B16**	7SEG_DISP_G	**C16**	IO3
A17	IO4	**B17**	S3_LED_GN	**C17**	IO5
A18	IO6	**B18**	S3_LED_RD	**C18**	IO7
A19	IO8	**B19**	STATE_LED_GN	**C19**	IO9
A20	IO10	**B20**	STATE_LED_RD	**C20**	IO11
A21	IO12	**B21**	LINK_A	**C21**	IO13
A22	IO14	**B22**	ACT_B	**C22**	IO15
A23	IO16	**B23**	LINK_B	**C23**	IO17
A24	IO18	**B24**	ACT_A	**C24**	IO19
A25	IO20	**B25**	ETH_A_TX+	**C25**	IO21
A26	IO22	**B26**	ETH_A_TX-	**C26**	IO23
A27	IO24	**B27**	ETH_A_RX+	**C27**	IO25
A28	IO26	**B28**	ETH_A_RX-	**C28**	IO27
A29	IO28	**B29**	ETH_B_TX+	**C29**	IO29
A30	IO30	**B30**	ETH_B_TX-	**C30**	IO31
A31	GND	**B31**	ETH_B_RX+	**C31**	GND
A32	VCC (3,3V)	**B32**	ETH_B_RX-	**C32**	VCC (3,3V)

4.2 EasySlave AddOn ETH-Connect

The AddOn Module ETH-Connect contains all necessary external interfaces for the EasySlave, like Power Supply and Ethernet connectors.



Connector X3 - 24V Power Supply			
Pin	1	2	3
Signal	Field Earth (FE)	0V	+24V

Connector X2 - Ethernet Port A								
Pin	1	2	3	4	5	6	7	8
Signal	TX+	TX-	RX+	TERM	OUT12	TERM	TERM	TERM

Connector X1 - Ethernet Port B								
Pin	1	2	3	4	5	6	7	8
Signal	TX+	TX-	RX+	TERM	OUT12	TERM	TERM	TERM

Header SV1 - Display + Switch										
Pin	1	3	5	7	9	11	13	15	17	19
Signal	VCC	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	+Ub
Pin	2	4	6	8	10	12	14	16	18	20
Signal	GND	SEG_P	SEG_G	SEG_F	SEG_E	SEG_D	SEG_C	SEG_B	SEG_A	GND

Header SV2 - Ethernet + LED										
Pin	1	3	5	7	9	11	13	15	17	19
Signal	GND	A_TX+	A_TX-	A_RX+	A_RX-	GND	B_TX+	B_TX-	B_RX+	B_RX-
Pin	2	4	6	8	10	12	14	16	18	20
Signal	A_ACT	A_LNK	VCC	S3_GN	S3_RD	ST_GN	ST_RD	VCC	B_LNK	B_ACT

4.2.1 Power Supply

The module provides a 3.3V power supply with a current rate of 2A for the EasySlave. The input is protected against over-voltage and reverse voltage. The input voltage can be provided within the range from 8V to 30V.

4.2.2 Ethernet Ports

The Ethernet ports are connected to the PHY chips on the FPGA module via pcb header. Each port has two LED's for link (green) and activity (orange).

4.2.3 Dip switch (sercos address)

The dip switch can be used to set a fix sercos address for the slave. The address is read one time after power-up. The address range is from 1 to 255. If the dip switch is 0 the address is configured by software.

The device supports both ways of address configuration, it have the following behavior:

1. **If the address switch indicates an address, which is not 0**
   The device applies the address, which is shown on the address switch S-0-1040 is write protected. The write request shall be declined by the slave with a SVC error (0x7004 (Operation data cannot be changed) or 0x700C (Operation data is write protected, due to other settings)).
2. **If the address switch indicates the address 0**
   The sercos address can only be configured via the SVC S-0-1040 is not write protected

4.2.4 7-segment display

The 7-segment display is used to display further device state information.

- 8 segment test after power up
- n NRT communication mode
- 0 CP0 communication mode
- 1 CP1 communication mode
- 2 CP2 communication mode
- 3 CP3 communication mode
- 4 CP4 communication mode
- F Device error (device status)

4.2.5 Sercos LED

The sercos LED (S3) is used for displaying the communication state of the device. It's controlled by the EasySlave IP core according the sercos specification.

4.2.6 Device state LED

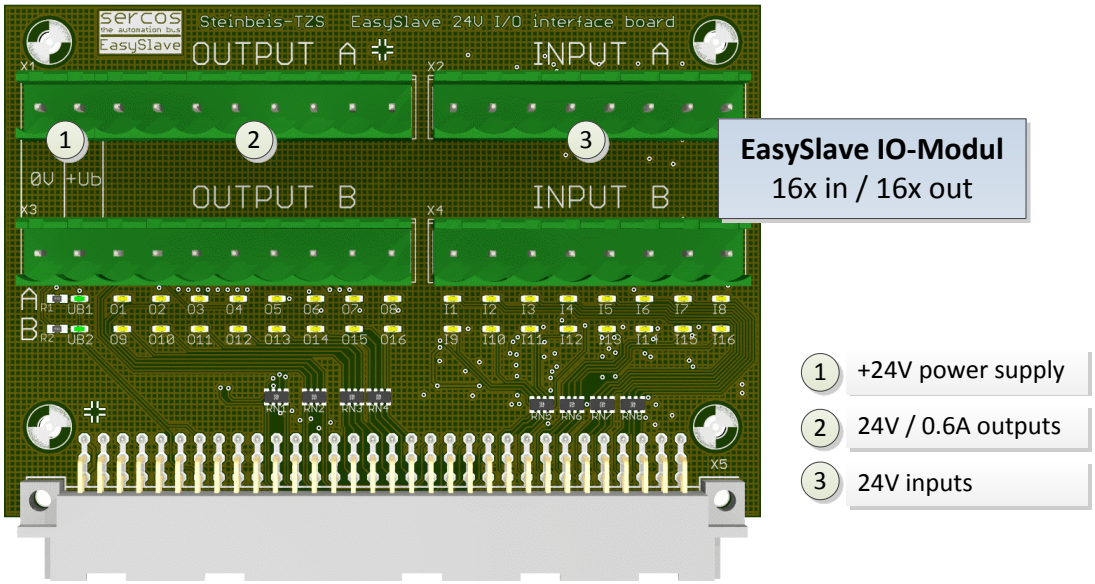
The device state LED is used for displaying the device state.

- Green: the Device is OK
- Red: the Device has some errors

4.3 EasySlave IO-Modul

The IO-Modul is specially designed for the EasySlave-IO and provides 16 digital outputs and 16 digital inputs. This is the typical application of the free sercos EasySlave-IO. For testing the outputs and inputs are connected one-to-one for loopback.

4.3.1 Pinout



Connector X1 - Digital Outputs Segment A										
Pin	1	2	1	2	3	4	5	6	7	8
Signal	0V	+24V	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7

Connector X3 - Digital Outputs Segment B										
Pin	1	2	1	2	3	4	5	6	7	8
Signal	0V	+24V	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13	OUT14	OUT15

Connector X2 - Digital Inputs Segment A								
Pin	1	2	3	4	5	6	7	8
Signal	INP8	INP9	INP10	INP11	INP12	INP13	INP14	INP15

Connector X4 - Digital Inputs Segment B								
Pin	1	2	3	4	5	6	7	8
Signal	INP0	INP1	INP2	INP3	INP4	INP5	INP6	INP7

Connector X5 - FPGA Interface (64 way DIN41612 connector, female)			
Row A	**Signal**	**Row C**	**Signal**
A1	+24V	**C1**	+24V
A2	GND	**C2**	GND
A3	*not used*	**C3**	*not used*
A4	*not used*	**C4**	*not used*
A5	*not used*	**C5**	*not used*
A6	DIAG_A (EXT0)	**C6**	DIAG_B (EXT1)
A7	PWR_A (EXT2)	**C7**	PWR_B (EXT3)
A8	*not used*	**C8**	*not used*
A9	*not used*	**C9**	*not used*
A10	*not used*	**C10**	*not used*
A11	*not used*	**C11**	*not used*
A12	*not used*	**C12**	*not used*
A13	*not used*	**C13**	*not used*
A14	*not used*	**C14**	*not used*
A15	IO0	**C15**	IO1
A16	IO2	**C16**	IO3
A17	IO4	**C17**	IO5
A18	IO6	**C18**	IO7
A19	IO8	**C19**	IO9
A20	IO10	**C20**	IO11
A21	IO12	**C21**	IO13
A22	IO14	**C22**	IO15
A23	IO16	**C23**	IO17
A24	IO18	**C24**	IO19
A25	IO20	**C25**	IO21
A26	IO22	**C26**	IO23
A27	IO24	**C27**	IO25
A28	IO26	**C28**	IO27
A29	IO28	**C29**	IO29
A30	IO30	**C30**	IO31
A31	GND	**C31**	GND
A32	VCC (3,3V)	**C32**	VCC (3,3V)

4.3.2 Digital outputs

The EasySlave IO-Modul has 16 digital 24V outputs. The outputs are split in two sections. Each section has its own 24V power supply. The outputs are driven by an 8 channel high-side switch chip (ITS 4880 R from Infineon Technologies).

Facts of the ITS 4880 R [I1] chip:

- Operating supply voltage 11 ... 45 V
- On-state resistance R_{ON} 200 mΩ
- Output current 0,625 A per channel
- Short circuit protection
- Maximum current internally limited
- Overload protection
- Overvoltage protection (including load dump)
- Undervoltage shutdown with autorestart and hysteresis
- Switching inductive loads
- Thermal shutdown with restart
- Thermal independence of separate channels
- ESD - Protection
- Loss of GND and loss of Vbb protection
- Reverse battery protection
- Common diagnostic output for overtemperature

4.3.3 Digital inputs

The EasySlave IO-Modul has 16 digital 24V inputs. The inputs don't provide any sensor supply. For input signal change

4.3.4 Diagnosis

For diagnosis some signals are routed to the FPGA to indicate IO errors. Both output sections have a separate diagnosis channel for under voltage and output error.

5 Technical Data

5.1 General

Board size without connectors:	
- FPGA Module + ETH-Connect	100mm x 57mm x 34mm
- IO-Extension	100mm x 70mm x 20mm
Size of the evaluation kit case:	330mm x 250mm x 90mm
Weight of the evaluation kit case:	2500g (Boards only 200g)
Operating temperature:	0°C … 50°C
Storage temperatur:	-10°C … 85°C
Humidity:	10% … 95%
Degree of protection:	no
Protection class:	Class 3 (SELV/PELV)

5.2 Power Supply

Rated voltage:	$24V_{dc}$
Voltage range:	$8V_{dc}$ … $30V_{dc}$
Rated Current:	0.1A
Over-voltage and reverse voltage protection:	yes

5.3 Digital inputs and outputs

Rated load voltage:	$24V_{dc}$
Load voltage range:	$11V_{dc}$ … $45V_{dc}$
Output current (IO):	0.6A per channel
Output overload protection:	min. 0.7A
Input level change (low > high):	~15V (2mA)
Input level change (high > low):	~11V (1.5mA)

5.4 Timing

Startup time:	max. 5s
Latency of output change (low > high):	typ. 75µs, max. 125µs
Latency of output change (high > low):	typ. 100µs, max. 175µs

5.5 Sercos

Sercos specification:	1.1.2
Profiles:	FSP-GDP, FSP-IO
Supported SCP classes:	SCP_FIXCFG, SCP_NRT
Hot-Plug service:	yes
S/IP server:	yes
Supported S/IP services:	SupportedUDPServices [61] ReadOnlyData [71] Nameplate [89] Browse [91] Identify [93] SetIp [95] BroadcastNameplate [99]
Firmware update via TFTP:	COD and PAR
Test IDN S-0-0390:	yes

6 Addendum

6.1 Evaluation kit important notice

Steinbeis-Transferzentrum Systemtechnik (TZS) provides the enclosed product under the following conditions:

This evaluation kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TZS to be a finished end-product fit for general use. Persons handling the product must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation kit not meet the specifications indicated in the User's Manual, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TZS from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

7 References

[TZS1] Getting Started sercos EasySlave-Kit (2012-09-18)

[TZS2] User Guide sercos EasySlave (2012-09-18)

[TZS3] Datasheet sercos EasySlave-IO (2012-09-18)

[I1] Data sheet ITS4880R_DS_11.pdf (Rev.1.1, 2008-09-29)
Infineon Technologies

Quellennachweis:

- Fotolia: 10056459, 10056460, 10056608, 11720149, 15998435, 28412929, 4598958, 4812346