ERM1602-5 Series

Character Module User Manual

EastRising Technology Co., Limited

Attention:

A. Click" CONTENTS" list could be directed to the detail page. Click "Return to CONTENTS" could be directed to CONTENTS Page.

B. Some specifications of IC are not listed in this manual. Please refer to the IC manual for more details.

C. The drawing for related touch panel, schematic drawing, demo code is all available, please contact with our sales if you need.

D. Please pay more attention to "INSPECTION CRITERIA" in this manual. We assume you already agree with these criterions when you place an order with us. No more recommendations.

REV	DESCRIPTION	RELEASE DATE
1.0	Preliminary Release	May-10-2012

CONTENTS

1. ORDERING INFORMATION

1.1 ERM1602-5 Series Table **>>Return to CONTENTS**

*The number of series table is in accordance with number of the below series image 1.2.

No.	Part Number	LCD Type	Backlight Color	Graphic & Font Color	Background Color
1	ERM1602SYG-5	STN Positive	Yellow Green Color	Dark Blue	Yellow Green Color
2	ERM1602SBS-5	STN Negative Blue	White Color	White Color	Blue Color
3	ERN1602FS-5	FSTN Positive	White Color	Black Color	White Color
4	ERM1602FR-5	FSTN Positive	Red Color	Black Color	Red Color
5	ERM1602FG-5	FSTN Positive	Green Color	Black Color	Green Color
6	ERM1602FB-5	FSTN Positive	Blue Color	Black Color	Blue Color
7	ERM1602FP-5	FSTN Positive	Purple Color	Black Color	Purple Color
8	ERM1602FAM-5	FSTN Positive	Amber Color	Black Color	Amber Color
9	ERM1602DNYG-5	FFSTN Negative	Yellow Green Color	Yellow Green Color	Black Color
10	ERM1602DNS-5	FFSTN Negative	White Color	White Color	Black Color
11	ERM1602DNR-5	FFSTN Negative	Red Color	Red Color	Black Color
12	ERM1602DNG-5	FFSTN Negative	Green Color	Green Color	Black Color
13	ERM1602DNB-5	FFSTN Negative	Blue Color	Blue Color	Black Color
14	ERM1602DNP-5	FFSTN Negative	Purple Color	Purple Color	Black Color
15	ERM1602DNAM-5	FFSTN Negative	Amber Color	Amber Color	Black Color

1.2 ERM1602-5 Series Image **>>Return to CONTENTS**

*The number of series image is in accordance with number of the above series table 1.1.

1 

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2. ATTRIBUTES

2.1 Display Attributes **>>Return to CONTENTS**

ITEM	STANDARD VALUE	UNIT
Resolution	16 Characters x 2 Lines	--
Display Connector	Pin Header,16 or 10 Pins	--
Operating Temperature	-20 ~ +70	℃
Storage Temperature	-30 ~ +80	℃
Touch Panel Optional	N/A	--
Font Chip Optional	N/A	--
*Sunlight Readable	No1,No3,No4,No5,No6,No7,No8	--

*Number of sunlight readable is from 1.1 ERM1602-5 Series Table of the manual.

2.2 Mechanical Attributes **>>Return to CONTENTS**

ITEM	STANDARD VALUE	UNIT
Outline Dimension	80.0(W) × 36.0(H) × 11.0(T) (MAX)	mm
Visual Area	64.5(W) × 14.5(H)	mm
Active Area	55.70(W) × 11.00(H)	mm
Character Size	2.90(W) × 5.15(H)	mm
Dot Size	0.54 × 0.60	mm
Dot Pitch	0.59 × 0.65	mm
Net Weight	31	g

2.3 Electrical Attributes **>>Return to CONTENTS**

ITEM	STANDARD VALUE	UNIT
IC Package	COB	--
Drive Voltage	5	V
Interface	6800 8-bit Parallel, 6800 4-bit Parallel, 3-Wire SPI,4-Wire SPI	--

2.4 Optical Attributes **>>Return to CONTENTS**

ITEM	STANDARD VALUE	UNIT
LCD Type	Refer to 1.1 ERM1602-5 Series Table	--
Backlight Color	Refer to 1.1 ERM1602-5 Series Table	--
Viewing Direction	6:00	Clock
LCD Duty	1/16	Duty
LCD Bias	1/5	Bias

3. OUTLINE DRAWING

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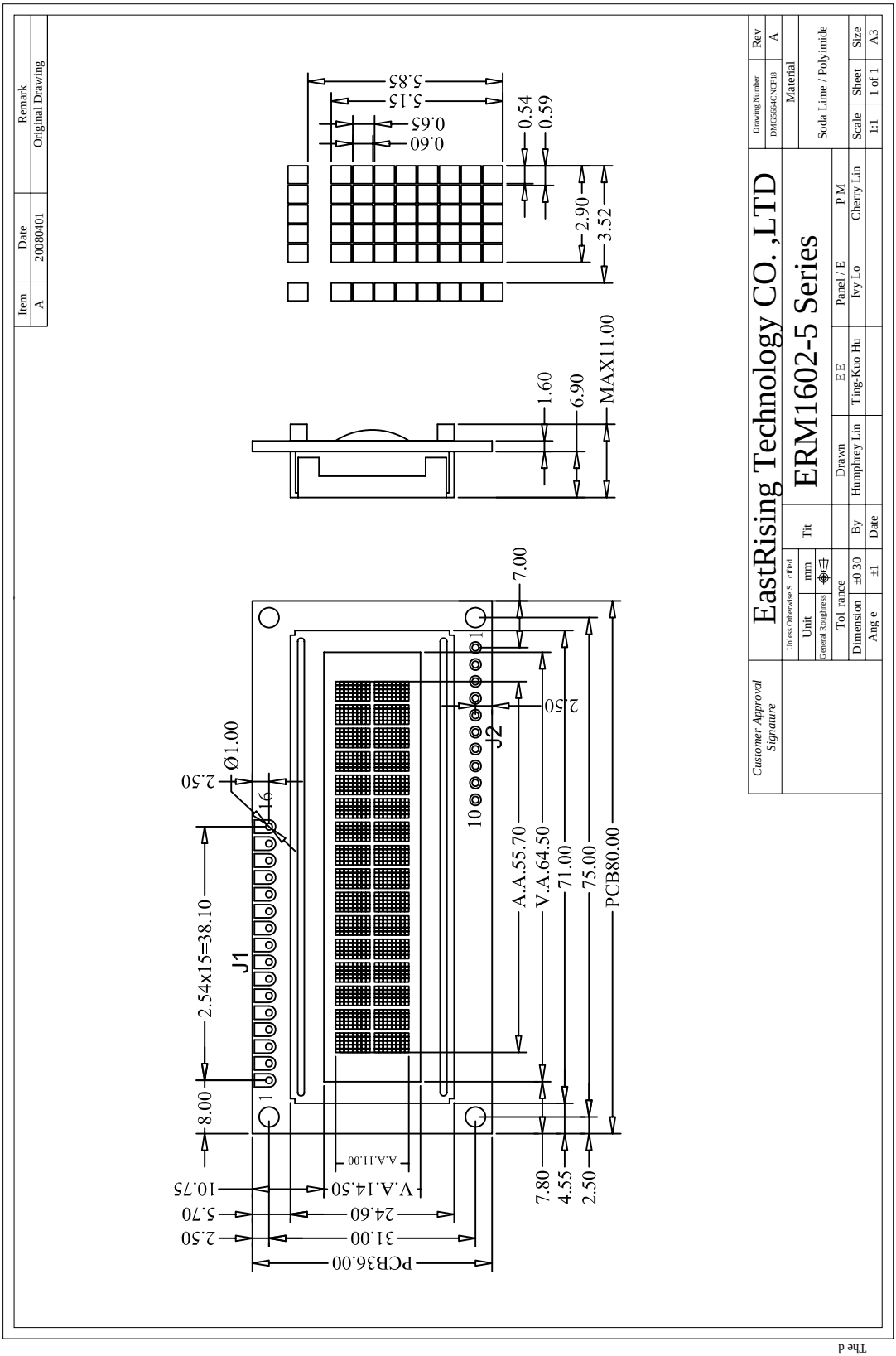

4. ELECTRICAL SPEC

4.1 Pin Configuration **>>Return to CONTENTS**

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Pin No.	Pin Name	Descriptions
1	GND	Power Ground
2	VCC	Power supply for logic
3	V0	Contrast adjust
4	RS	H : Data L:Command
5	R/W	H : Read mode, L : Write mode
6	E	Enable signal
7-14	DB0-DB7	Data Bus
15	LED A	Backlight Anode
16	LED K	Backlight Cathode

J-2

Pin No.	Pin Name	Descriptions
1	GND	Power Ground
2	VCC	Power Supply for Logic
3	V0	Contrast adjust
4	CS	Chip Selection Signal,Low Active
5	CLK	Serial Clock Signal
6	DI	Serial Data Signal
7	RS	H:Paralell interface L:Serial interface
8	RST	Reset Signal,Low Active
9	LED A	Backlight Anode
10	LED K	Backlight Cathode

4.2 Absolute Maximum Ratings **>>Return to CONTENTS**

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply for Logic	VDD-VSS	-0.3	-	+5.5	V
Power Supply for LCD	VLCD	-0.3	-	+7.0	V
Input Voltage	VIN	-0.3	-	Vcc+0.3	V
Supply Current for Backlight	ILED	-	-	20	mA

4.3 Electrical Characteristics **>>Return to CONTENTS**

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply for LCM	VDD-VSS	-	4.50	5.0	5.50	V
Input Voltage	V_{IL}	L Level	-0.3	-	0.6	V
	V_{IH}	H Level	2.2	-	VDD	V
LCD Driving Voltage	V_{LCD}	V0-Vss	3.0	-	7.0	V
Supply Current for LCM	IDD	VDD=5.0V	-	200	500	uA
Supply Current for Backlight	ILED	-	-	15	20	mA

5. INSPECTION CRITERIA

5.1 Acceptable Quality Level **>>Return to CONTENTS**

Each lot should satisfy the quality level defined as follows

PARTITION	AQL	DEFINITION
A. Major	0.4%	Functional defective as product
B. Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic stanard

5.2 Definition of Lot

One lot means the delivery quantity to customer at one time.

5.3 Condition of Cosmetic Inspection **>>Return to CONTENTS**

◆ INSPECTION AND TEST

-FUNCTION TEST

-APPEARANCE INSPECTION

-PACKING SPECIFICTION

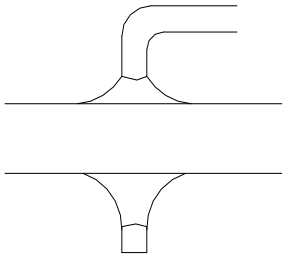
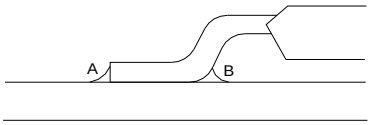
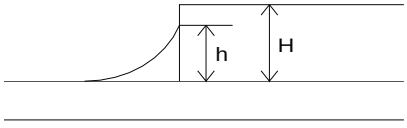
◆ INSPECTION CONDITION

- Put under the lamp (20w¡Á2) at a distance 100mm from
- Tilt upright 45 degree by the front (back) to inspect LCD appearance.

◆ AQL INSPECTION LEVEL

- SAMPLING METHOD: MIL-STD-105D
- SAMPLING PLAN: SINGLE
- MAJOR DEFECT: 0.65% (MAJOR)
- MINOR DEFECT: 2.5% (MINOR)
- GENERAL LEVEL: II/NORMAL

5.4 Module Cosmetic Criteria **>>Return to CONTENTS**

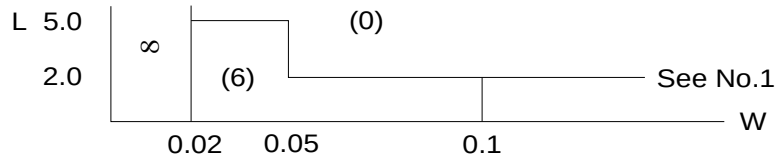
NO.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern Peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing	Major
		No soldering bridge	Major
		No cold soldering	Minor
4	Resist flaw on substrate	Invisible copper foil(∅0.5mm or more)on substrate pattern	Minor
5	Accretion of metallic	No soldering dust	Minor
	Foreign matter	No accretion of metallic foreign matters(Not exceed∅0.2mm)	
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading,rusting and discoloring	Minor
8	Solder amount 1.Lead parts	a. Soldering side of PCB Solder to form a'Filet' all around the lead. Solder should not hide the lead form perfectly.(too much)  b.Components side (In case of 'Through Hole PCB') Solder to reach the Components side of PCB	Minor
	2.Flat packages	Either 'toe'(A) or 'heal' (B) of the lead to be covered by 'Filet'  Lead form to be assume over Solder.	Minor
	3.Chips	(3/2) H≧h≧(1/2)H 	Minor

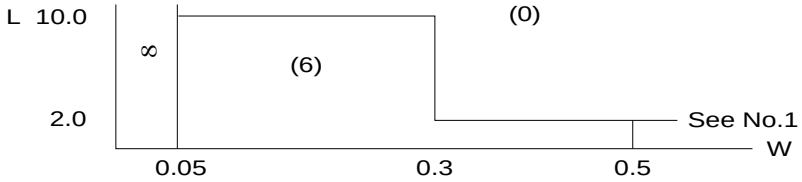
9	Backlight defects	1.Light fails or flickers.(Major) 2. Color and luminance do not correspond to specifications. (Major) 3.Exceeds standards for display's blemishes, foreign matter, dark lines or scratches.(Minor)	See list ←
10	PCB defects	Oxidation or contamination on connectors.* 2. Wrong parts, missing parts, or parts not in specification.* 3.Jumpers set incorrectly.(Minor) 4.Solder(if any)on bezel,LED pad,zebra pad,or screw hole pad is not smooth.(Minor) *Minor if display functions correctly.Major if the display fails.	See list ←
11	Soldering defects	1. Unmelted solder paste. 2. Cold solder joints,missing solder connections,or oxidation.* 3. Solder bridges causing short circuits.* 4. Residue or solder balls. 5. Solder flux is black or brown. *Minor if display functions correctly.Major if the display fails.	Minor

5.5 Screen Cosmetic Criteria (Non-Operating) **>>Return to CONTENTS**

<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td colspan="2">In accordance with Screen Cosmetic Criteria (Operating) No.1.</td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td colspan="2">In accordance with Screen Cosmetic Criteria (Operation) No.2.</td><td>Minor</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">Bubbles in Polarizer</td><td colspan="2"></td><td rowspan="2">Minor</td></tr>
<tr><td>Size: d mm</td><td>Acceptable Qty in active area</td></tr>
<tr><td>d≦0.3
0.3<d≦1.0
1.0<d≦1.5
1.5<d</td><td>Disregard
3
1
0</td></tr>
<tr><td>4</td><td>Scratch</td><td colspan="2">In accordance with spots and lines operating cosmetic criteria, When the light reflects on the panel surface, the scratches are not to be remarkable.</td><td>Minor</td></tr>
<tr><td>5</td><td>Allowable density</td><td colspan="2">Above defects should be separated more than 30mm each other.</td><td>Minor</td></tr>
<tr><td>6</td><td>Coloration</td><td colspan="2">Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.</td><td>Minor</td></tr>
<tr><td>7</td><td>Contamination</td><td colspan="2">Not to be noticeable.</td><td>Minor</td></tr>
</table>

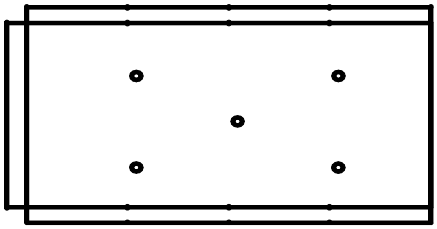
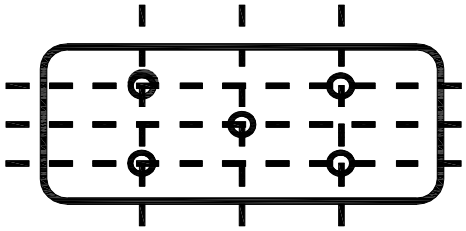
5.6 Screen Cosmetic Criteria (Operating) >>Return to CONTENTS

<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear
<table>
<tr><th>Size:d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d≦0.1</td><td>Disregard</td></tr>
<tr><td>0.1<d≦0.2</td><td>6</td></tr>
<tr><td>0.2<d≦0.3</td><td>2</td></tr>
<tr><td>0.3<d</td><td>0</td></tr>
</table>
Note: Including pin holes and defective dots which must be within one pixel Size.
B) Unclear
<table>
<tr><th>Size:d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d≦0.2</td><td>Disregard</td></tr>
<tr><td>0.2<d≦0.5</td><td>6</td></tr>
<tr><td>0.5<d≦0.7</td><td>2</td></tr>
<tr><td>0.7<d</td><td>0</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>A) Clear
 

Note: () – Acceptable Qty in active area
L - Length (mm)
W -Width(mm)
∞-Disregard
B) Unclear
 
</td><td>Minor</td></tr>
</table>

'Clear' = The shade and size are not changed by Vo.

'Unclear' = The shade and size are changed by Vo.

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95%~105%of the dot size (Typ.) in drawing. Partial defects of each dot (ex.pin-hole) should be treated as'spot'. (see Screen Cosmetic Criteria (Operating) No.1)	Minor
7	Brightness (only back-lit Module)	Brightness Uniformity must be BMAX/BMIN≦2 - BMAX :Max.value by measure in 5 points - BMIN : Min.value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure. 	Minor
8	Contrast Uniformity	Contrast Uniformity must be BmAX/BMIN≦2 Measure 5 points shown in the following figure. Dashed lines divide active area into 4 vertically and horizontally. Measuring points are located at the inter-sections of dashed line.  Note: BMAX – Max.value by measure in 5 points. BMIN – Min.value by measure in 5 points. O – Measuring points in ∅10mm.	Minor

Note:

(1) Size : d=(long length + short length)/2

(2) The limit samples for each item have priority.

(3) Complexed defects are defined item by item, but if the number of defects is defined in above table, the total number should not exceed 10.

(4) In case of 'concentration', even the spots or the lines of 'disregarded' size should not be allowed. Following three situations

Should be treated as 'concentration'.

-7 or over defects in circle of ¢5mm.

-10 or over defects in circle of ¢10mm

-20 or over defects in circle of ¢20mm

6. PRECAUTIONS FOR USING

6.1 Handling Precautions **>>Return to CONTENTS**

- This device is susceptible to Electro-Static Discharge (ESD) damage. Observe Anti-Static precautions.
- EastRising display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- If EastRising display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- Do not apply excessive force to the EastRising display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the EastRising display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- If EastRising display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following Isopropyl or alcohol.
- Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the Water.
- Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- Install the EastRising LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the cable or the backlight cable.
- Do not attempt to disassemble or process EastRising LCD module.
- NC terminal should be open. Do not connect anything.
- If the logic circuit power is off, do not apply the input signals.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

  -Be sure to ground the body when handling EastRising LCD modules.

  -Tools required for assembling, such as soldering irons, must be properly grounded.

  -To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

6.2 Power Supply Precautions **>>Return to CONTENTS**

◆ Identify and, at all times, observe absolute maximum ratings for both logic and LC drivers. Note that there is some variance between models.

◆ Prevent the application of reverse polarity to VDD and VSS, however briefly.

◆ Use a clean power source free from transients. Power-up conditions are occasionally jolting and may exceed the maximum ratings of EastRising modules.

◆ The VDD power of EastRising module should also supply the power to all devices that may access the display. Don't allow the data bus to be driven when the logic supply to the module is turned off.

6.3 Operating Precautions **>>Return to CONTENTS**

◆ DO NOT plug or unplug EastRising module when the system is powered up.

◆ Minimize the cable length between EastRising module and host MPU.

◆ For models with backlights, do not disable the backlight by interrupting the HV line. Unload inverters produce voltage extremes that may arc within a cable or at the display.

◆ Operate EastRising module within the limits of the modules temperature specifications.

6.4 Mechanical/Environmental Precautions **>>Return to CONTENTS**

◆ Improper soldering is the major cause of module difficulty. Use of flux cleaner is not recommended as they may seep under the electrometric connection and cause display failure.

◆ Mount EastRising module so that it is free from torque and mechanical stress.

◆ Surface of the LCD panel should not be touched or scratched. The display front surface is an easily scratched, plastic polarizer. Avoid contact and clean only when necessary with soft, absorbent cotton dampened with petroleum benzene.

◆ Always employ anti-static procedure while handling EastRising module.

◆ Prevent moisture build-up upon the module and observe the environmental constraints for storage tem

◆ Do not store in direct sunlight

◆ If leakage of the liquid crystal material should occur, avoid contact with this material, particularly ingestion. If the body or clothing becomes contaminated by the liquid crystal material, wash thoroughly with water and soap

6.5 Storage Precautions **>>Return to CONTENTS**

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep EastRising modules in bags (avoid high temperature / high humidity and low temperatures below 0C Whenever possible, EastRising LCD modules should be stored in the same conditions in which they were shipped from our company.

6.6 Others **>>Return to CONTENTS**

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If EastRising LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

-Exposed area of the printed circuit board.

-Terminal electrode sections.

7. USING LCD MODULES

7.1 Liquid Crystal Display Modules

>>Return to CONTENTS

EastRising LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- When EastRising display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
- Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- Avoid contacting oil and fats.
- Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
- Do not put or attach anything on EastRising display area to avoid leaving marks on.
- Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinated to the polarizers).
- As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

7.2 Installing LCD Modules

>>Return to CONTENTS

- Cover the surface with a transparent protective plate to protect the polarizer and LC cell.
- When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be±0.1mm.

7.3 Precaution for Handling LCD Modules >>Return to CONTENTS

Since EastRising LCM has been assembled and adjusted with a high degree of precision; avoid applying excessive shocks to the module or making any alterations or modifications to it.

- Do not alter, modify or change the shape of the tab on the metal frame.
- Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- Do not damage or modify the pattern writing on the printed circuit board.
- Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- Do not drop, bend or twist EastRising LCM.

7.4 Electro-Static Discharge Control >>Return to CONTENTS

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

- Make certain that you are grounded when handing LCM.
- Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

7.5 Precaution for Soldering to EastRising LCM >>Return to CONTENTS

- Observe the following when soldering lead wire, connector cable and etc. to the LCM.
  -Soldering iron temperature : 280℃±10℃
  -Soldering time: 3-4 sec.
  -Solder: eutectic solder.
  If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.
- When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

7.6 Precaution for Operation **>>Return to CONTENTS**

- Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.
- Driving the EastRising LCD in the voltage above the limit shortens its life.
- Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
- If EastRising display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40℃, 50% RH.
- When turning the power on, input each signal after the positive/negative voltage becomes stable.

7.7 Limited Warranty **>>Return to CONTENTS**

Unless agreed between EastRising and customer, EastRising will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with EastRising LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to EastRising within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of EastRising limited to repair and/or replacement on the terms set forth above. EastRising will not be responsible for any subsequent or consequential events.

7.8 Return Policy **>>Return to CONTENTS**

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

-Broken LCD glass.
-PCB eyelet damaged or modified.
-PCB conductors damaged.
-Circuit modified in any way, including addition of components.
-PCB tampered with by grinding, engraving or painting varnish.
-Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals

.

Table 1 Correspondence between Character Codes and Character Patterns (b8=0)

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Table 2 Correspondence between Character Codes and Character Patterns

Character Code (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)							
b8	b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
						0	0	0				0	0	1				0	0	1	0	0
						0	0	0				0	1	0				0	0	1	0	0
						0	0	0				0	1	1				0	0	1	0	0
						0	0	0				1	0	0				0	0	1	0	0
						0	0	0				1	0	1				0	0	1	0	0
						0	0	0				1	1	0				0	0	1	0	0
						0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
						0	0	1				0	0	1				1	0	0	0	1
						0	0	1				0	1	0				1	0	0	0	1
						0	0	1				0	1	1				1	1	1	1	0
						0	0	1				1	0	0				1	0	1	0	0
						0	0	1				1	0	1				1	0	0	1	0
						0	0	1				1	1	0				1	0	0	0	1
						0	0	1				1	1	1				0	0	0	0	0

Table 3 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
"-": Indicates no effect.

■ Instructions

There are four categories of instructions that:

- **Designate IC functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**

Instruction Table:

Instruction	Instruction Code										Description	Description Time (270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
EXT = 0 or 1												
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Display ON/OFF	0	0	0	0	0	0	1	D	C	P	D=1:entire display on C=1:cursor on P: font table page selection	37 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us
Function Set	0	0	0	0	1	DL	N	EXT	x	x	DL: interface data is 8/4 bits N: number of line is 2/1	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37 us
EXT = 0												
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37 us

EXT = 1												
Bias resistor select	0	0	0	0	0	0	0	1	Rb1	Rb0	Used internal resister only provide 1/5 bias mode . Rb[1:0]=00→External Resister Rb[1:0]=01~11→Internal Resistor	37 us
COM、SEG direction select	0	0	0	1	0	0	C1	C2	S1	S2	C1：com1~8→com8~1 C2：com9~16→com16~9 S1：seg1~40→seg40~1 S2：seg41~80→seg80~41	37 us
Set display data length	0	0	1	L6	L5	L4	L3	L2	L1	L0	To specify the number of data bytes(3SPI mode)	37 us

Note:
Be sure the IC is not in the busy state (BF = 0) before sending an instruction from the MPU to the IC. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

■ Instruction Description

EXT=0 or 1

- **Clear Display**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

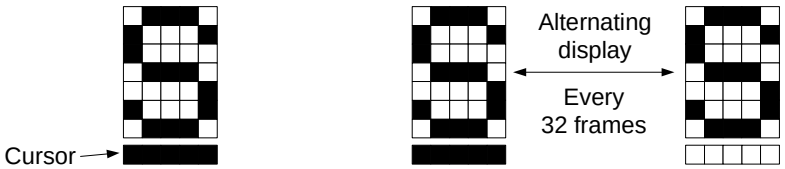
- **Display ON/OFF**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	P

Control display/cursor/blink ON/OFF 1 bit register.

➢ **D : Display ON/OFF control bit**
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

➢ **C : Cursor ON/OFF control bit**
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.



➢ **P : Font table selection bit**
When P = "Low", it select page 1 of font table.(set DDRAM data bit-8=0)
When P = "High", it select page 2 of font table(set DDRAM data bit-8=1)

- **Cursor or Display Shift**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	x	x

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	EXT	x	x

- **DL : Interface data length control bit**
  When DL = "High", it means 8-bit bus mode with MPU.
  When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
  When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**
  When N = "Low", it means 1-line display mode.
  When N = "High", 2-line display mode is set.
- **EXT : Select basic or extended instruction set**
  When EXT="L" the commands 'Entry Mode Set' , 'Set CGRAM address' and 'Set DDRAM address' can be performed , when EXT="H" the commands 'Bias resistor select' , 'COM、SEG direction select' and 'Set display data length' can be performed. Other command can be executed in both cases.
  When EXT="L" : disable extension instruction
  When EXT="H" : enable extension instruction

- **Read Busy Flag and Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = “High”, indicates that the internal operation is being processed.So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. DDRAM data bit-8 is come from “P”(Display on/off instruction) register setting

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

EXT=0

- **Entry Mode Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

- **I/D : Increment / decrement of DDRAM address (cursor or blink)**
  When I/D = "High", cursor moves to right and DDRAM address is increased by 1.
  When I/D = "Low", cursor moves to left and DDRAM address is decreased by 1.
  * CGRAM operates the same as DDRAM, when read from or write to CGRAM.
- **S: Shift of entire display**
  When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Set CGRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and
DDRAM address in the 2nd line is from "40H" to "67H".

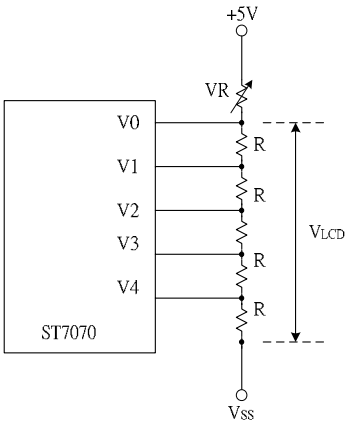
EXT=1

- **Bias resistor select**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	Rb1	Rb0

Set internal bias resistor value.

Rb1	Rb0	Description
L	L	External bias resistor select.
L	H	Build-in resistor select (R=**2.2**K).
H	L	Build-in resistor select (R=**6.8**K).
H	H	Build-in resistor select (R=**9.0**K).



- **COM、SEG direction select**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	0	0	C1	C2	S1	S2

The SEG and COM output in IC all have bi-direction control by the register.

COM OUTPUT :

COM output C1	**COM1**		**COM8**
0	COM1 →	Common Address	→ COM8
1	COM8 →	Common Address	→ COM1

COM output C2	**COM9**		**COM16**
0	COM9 →	Common Address	→ COM16
1	COM16 →	Common Address	→ COM9

SEG OUTPUT :

SEG output S1	**SEG1**		**SEG40**
0	SEG1 →	Segment Address	→ SEG40
1	SEG40 →	Segment Address	→ SEG1

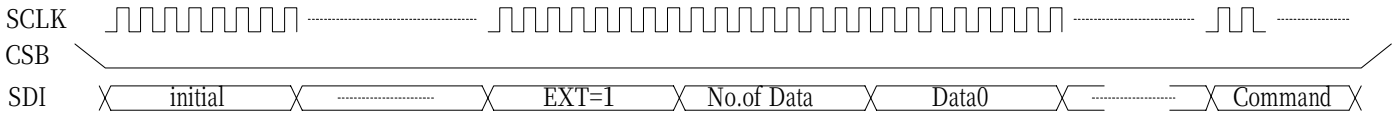
SEG output S2	**SEG41**		**SEG80**
0	SEG41 →	Segment Address	→ SEG80
1	SEG80 →	Segment Address	→ SEG41

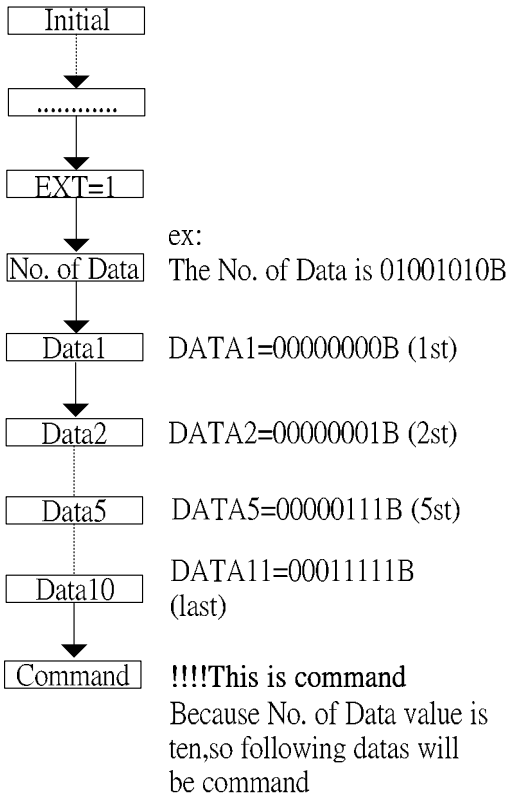
Set display data length

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	L5	L4	L3	L2	L1	L0

L6	L5	L4	L3	L2	L1	L0	Data length
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
….	…	…	…	…	…	….	…
1	0	0	1	1	1	0	79
1	0	0	1	1	1	1	80

Only in 3line-SPI interface will use the register to set the number of display data(Max=4F).
To write data to DDRAM , send Data Direction Command in 3-pin SPI . Data is latched at the rising edge of SCLK . And the DDRAM column address pointer will be increased by one automatically.





ex:
The No. of Data is 01001010B

DATA1=00000000B (1st)

DATA2=00000001B (2st)

DATA5=00000111B (5st)

DATA11=00011111B
(last)

!!!!This is command
Because No. of Data value is ten,so following datas will be command

■ Reset Function

Initializing by Internal Reset Circuit

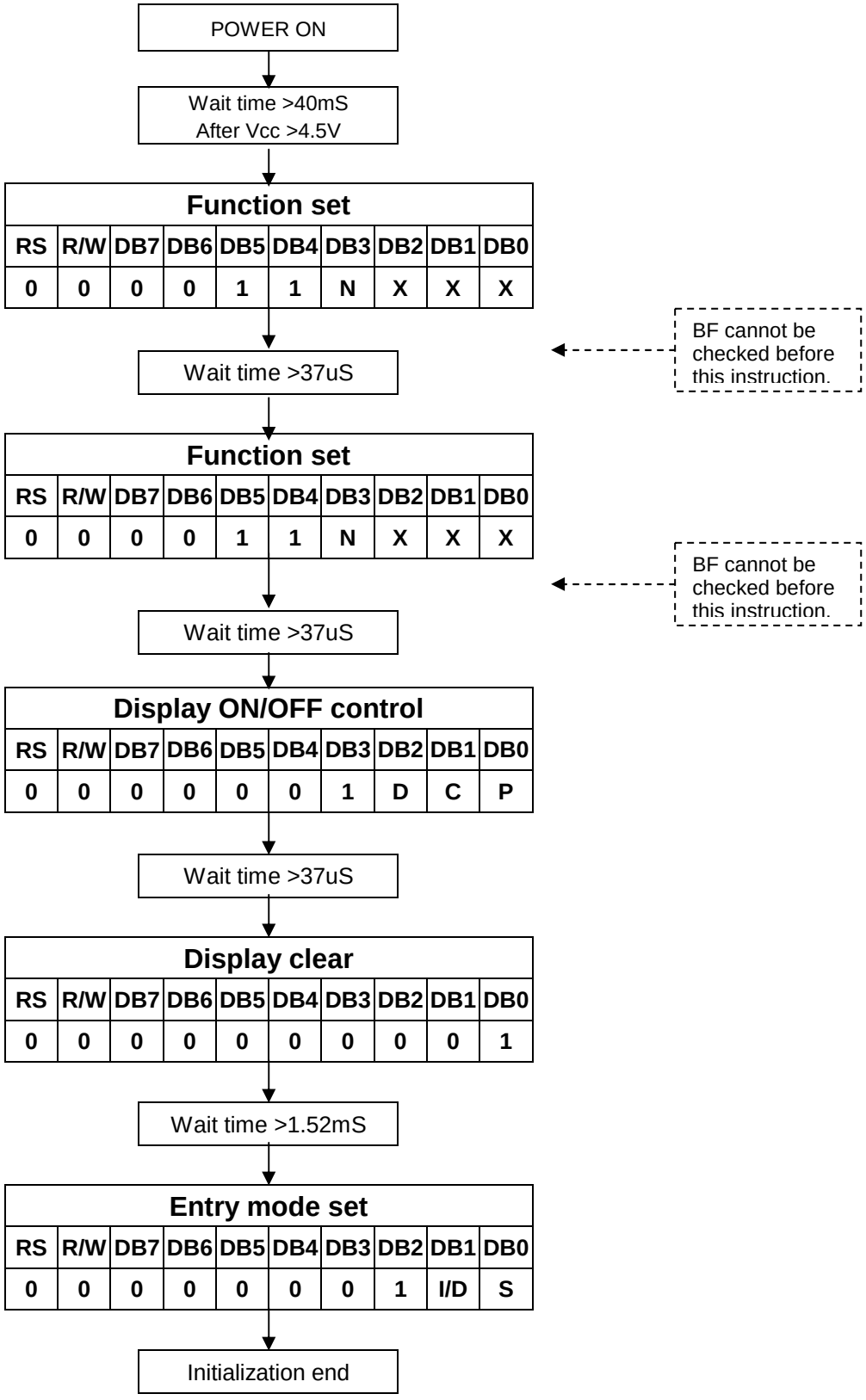
An internal reset circuit automatically initializes the IC when the power is turned on or hardware reset pin has low. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 1; 2-line display
   EXT=0;disable extension instruction.
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   P = 0; Page 1 of font table(DDRAM data b8=0)
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift
5. Bias resistor select:
   Rb1=0;Rb2=0 select external bias resistor.
6. COM、SEG direction select:
   C1=0;C2=0;S1=0;S2=0 not reverse.

Note:
If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the IC. For such a case, initialization must be performed by the MPU as explain by the following figure.

■ Initializing by Instruction

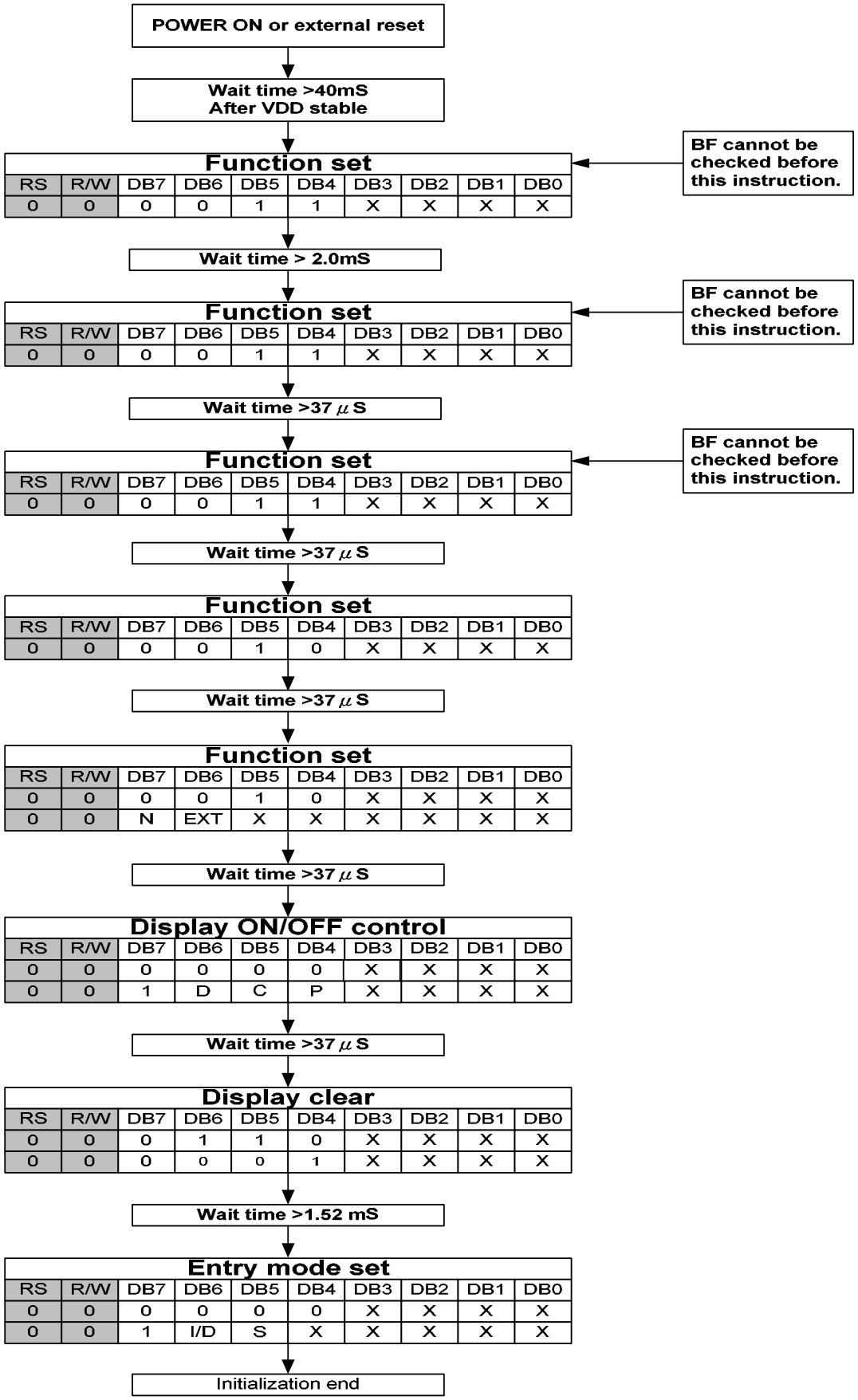
- **8-bit Interface (fosc=270KHz)**



➢ **Initial Program Code Example For 8051 MPU(8 Bit Interface):**

```
;-------------------------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK       ;CURSOR MOVES TO RIGHT
        CALL    DELAY37uS
;-------------------------------------------------------------------------------
MAIN_START:

        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
;-------------------------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        CLR     RS                      ;EX:Port 3.0
        CLR     RW                      ;EX:Port 3.1
        SETB    E                       ;EX:Port 3.2
        MOV     P1,A                    ;EX:Port 1=Data Bus
        CLR     E
        MOV     P1,#FFH                 ;For Check Busy Flag
        RET
;-------------------------------------------------------------------------------
CHK_BUSY:                               ;Check Busy Flag
        CLR     RS
        SETB    RW
        SETB    E
        JB      P1.7,$
        CLR     E
        RET
```

- **4-bit Interface (fosc=270KHz)**

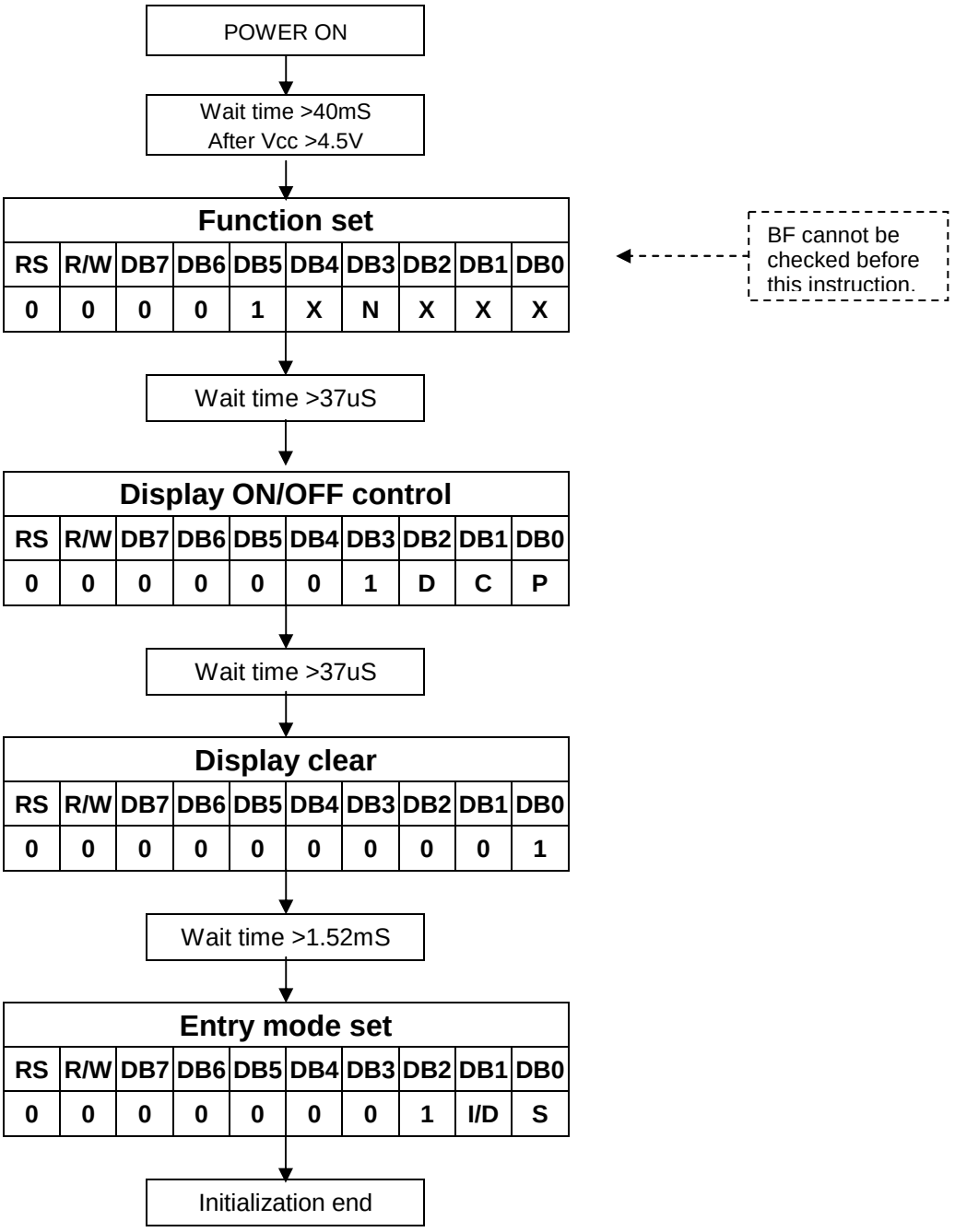


➢ **Initial Program Code Example For 8051 MPU(4 Bit Interface):**

```
;---------------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY2mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY37uS


        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK
        CALL    DELAY37uS
;---------------------------------------------------------------------
MAIN_START:
        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
```

```
;---------------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        PUSH    A
        ANL     A,#F0H
        CLR     RS              ;EX:Port 3.0
        CLR     RW              ;EX:Port 3.1
        SETB    E               ;EX:Port 3.2
        MOV     P1,A            ;EX:Port1=Data Bus
        CLR     E
        POP     A
        SWAP    A
WRINS_ONCE:
        ANL     A,#F0H
        CLR     RS
        CLR     RW
        SETB    E
        MOV     P1,A
        CLR     E
        MOV     P1,#FFH         ;For Check Bus Flag
        RET
;---------------------------------------------------------------------
CHK_BUSY:                       ;Check Busy Flag
        PUSH    A
        MOV     P1,#FFH
$1
        CLR     RS
        SETB    RW
        SETB    E
        MOV     A,P1
        CLR     E
        MOV     P1,#FFH
        CLR     RS
        SETB    RW
        SETB    E
        NOP
        CLR     E
        JB      A.7,$1
        POP     A
        RET
```

Serial Interface (fosc=270KHz)

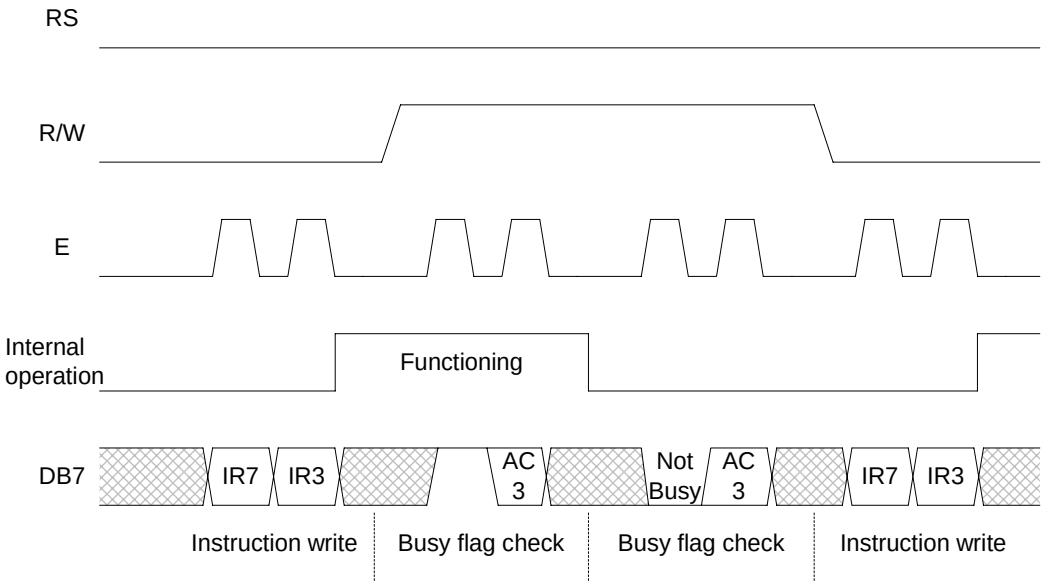


■ Interfacing to the MPU

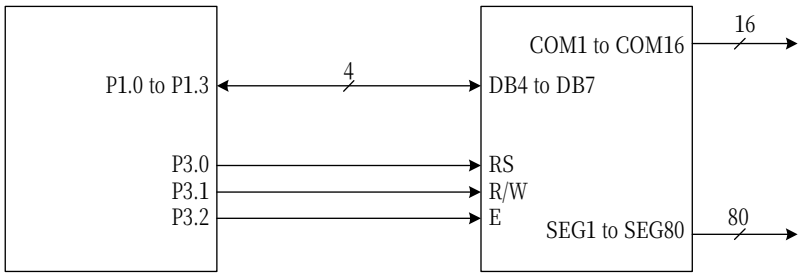
The IC can send data in either two 4-bit operations or one 8-bit operation or serial operation, thus allowing interfacing with 4- or 8-bit or serial MPU.

- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.** Bus lines DB0 to DB3 are disabled. The data transfer between the IC and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

➢ **Example of busy flag check timing sequence**

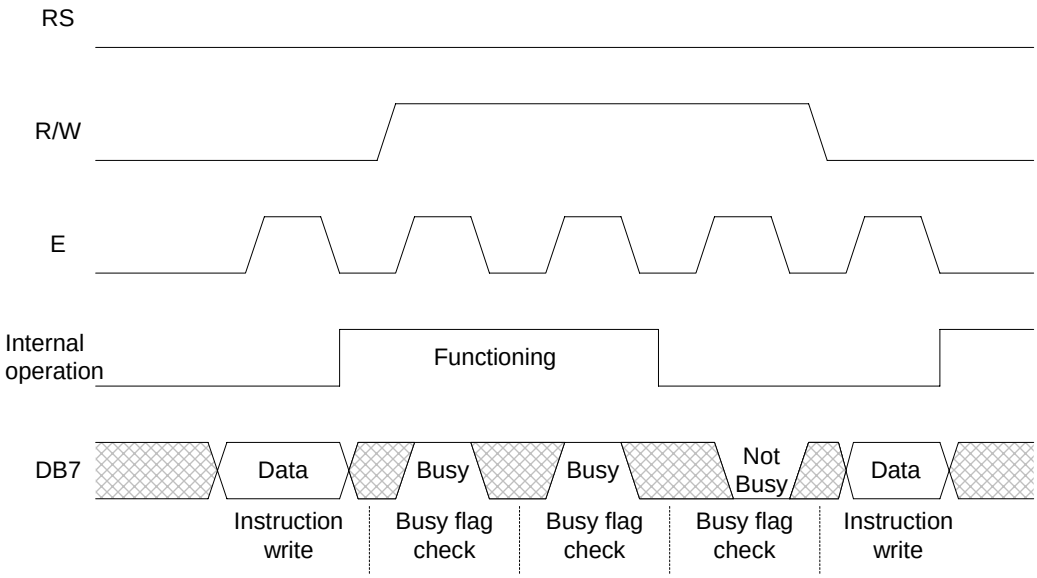


➢ **Intel 8051 interface**

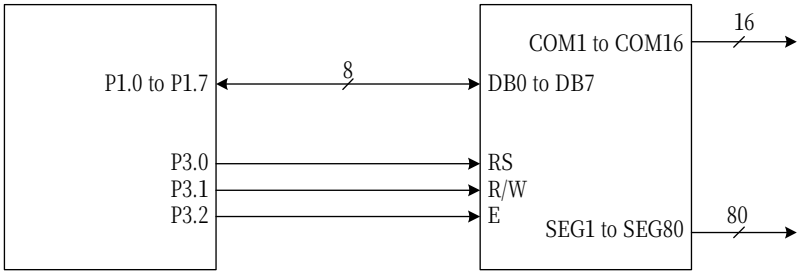


- **For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.**

➢ **Example of busy flag check timing sequence**

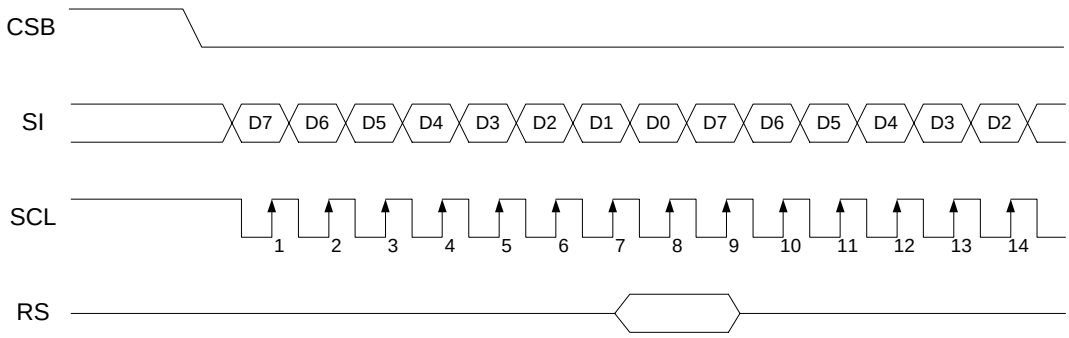


➢ **Intel 8051 interface**

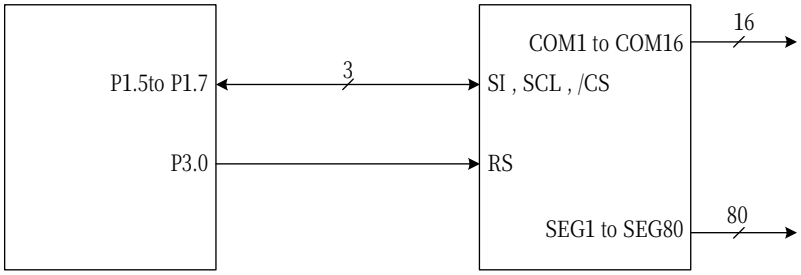


- **For serial interface data, bus lines (DB5 to DB7) are used. 4-Pin SPI**

➢ **Example of timing sequence**

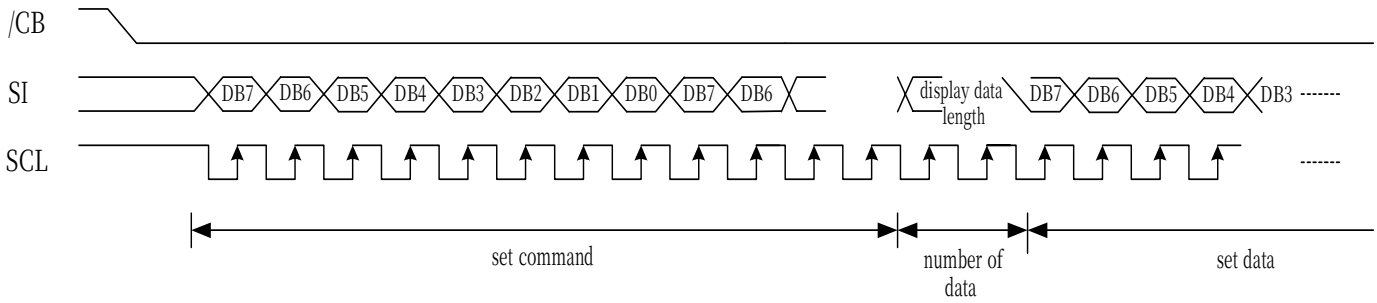


➢ **Intel 8051 interface(Serial)**

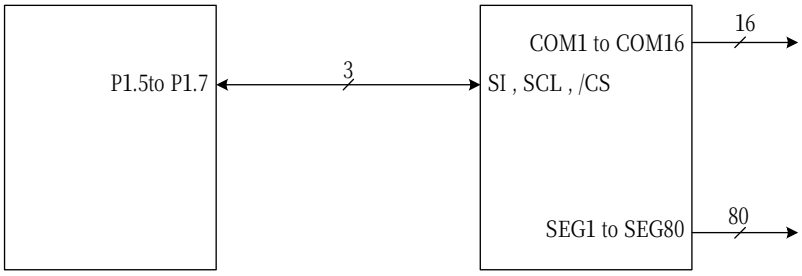


- **For serial interface data, bus lines (DB5 to DB7) are used. 3-Pin SPI**

➢ **Example of timing sequence**



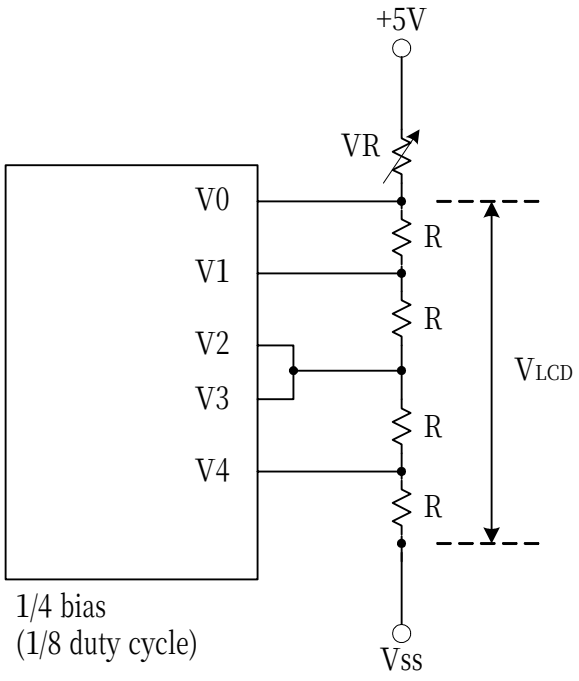
➢ **Intel 8051 interface(Serial)**

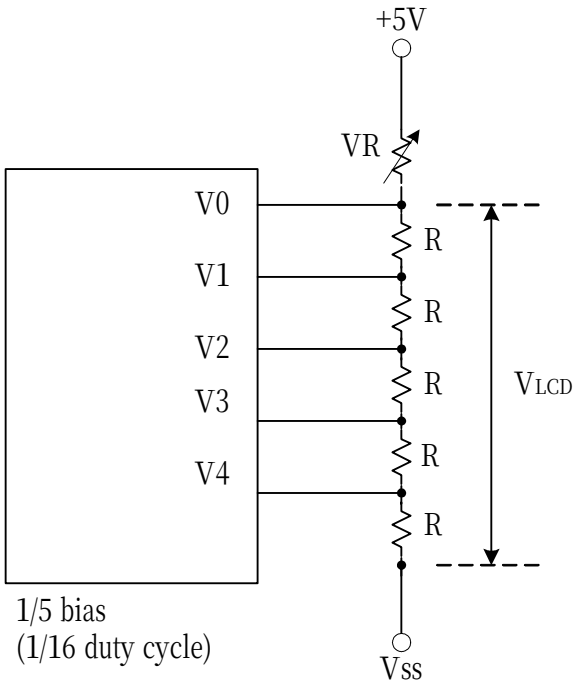


■ Supply Voltage for LCD Drive

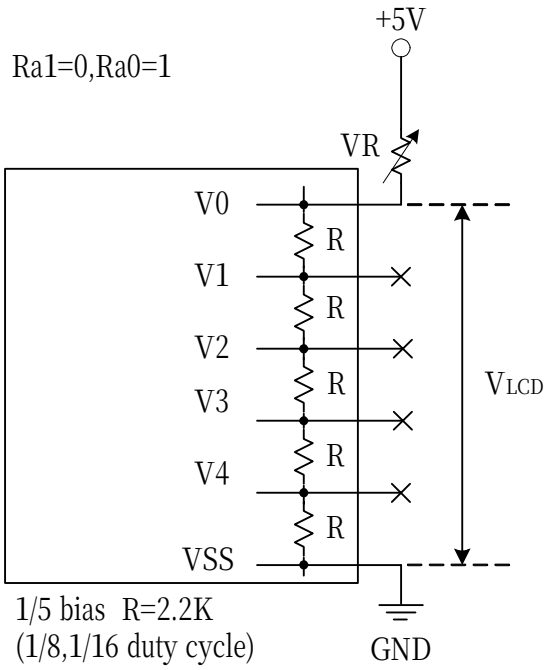
There are different voltages that supply to IC's pin (V0 – V4) to obtain LCD drive waveform. We could use the register command (Ra1,Ra0) to set up the Internal or External Bias Resister. The relations of the bias, duty factor and supply voltages are shown as below. External Bias Resistor could set up to 1/4 bias and 1/5 bias, but Internal Bias Resistor only could set up to 1/5 bias.

External Resistor	**Duty Factor**	
	1/8	1/8,1/16
	Bias	
Supply Voltage	1/4	1/5
Bias Resistor Select	Ra1=0,Ra0=0	Ra1=0,Ra0=0
V0	VLCD	VLCD
V1	3/4VLCD	4/5VLCD
V2	1/2VLCD	3/5VLCD
V3	1/2VLCD	2/5VLCD
V4	1/4VLCD	1/5VLCD

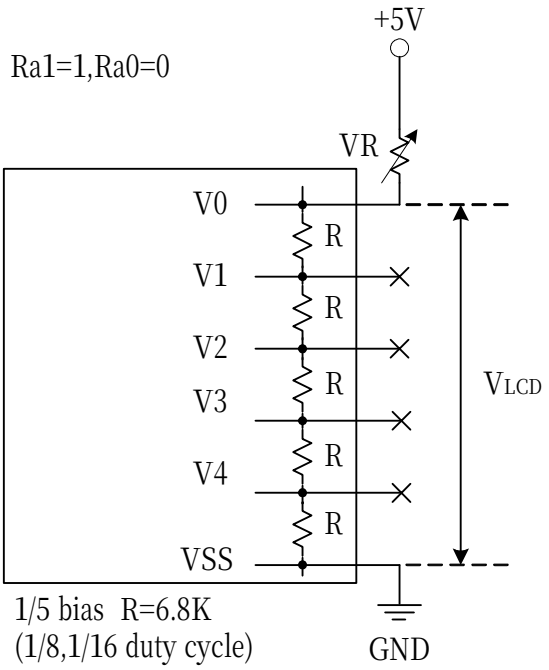




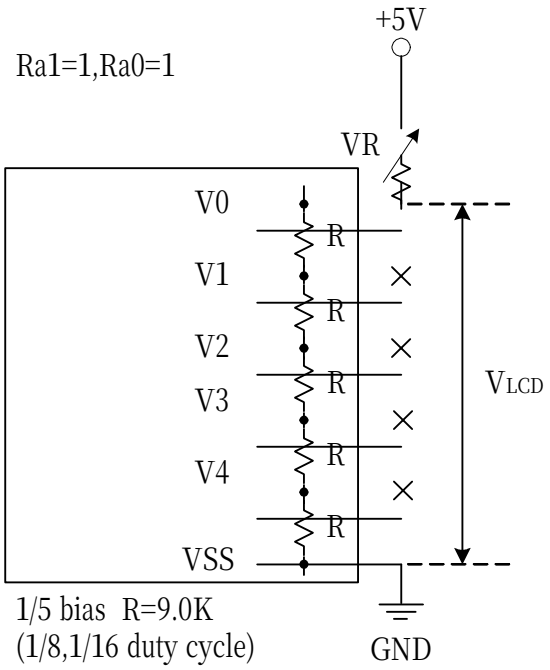
Internal Resistor	Duty Factor		
	1/8 , 1/16		
	Bias		
Supply Voltage	1/5	1/5	1/5
Bias Resistor Select	Ra1=0,Ra0=1	Ra1=1,Ra0=0	Ra1=1,Ra0=1
Internal Resistor	R=2.2K	R=6.8K	R=9.0K
V0	VLCD	VLCD	VLCD
V1	4/5VLCD	4/5VLCD	4/5VLCD
V2	3/5VLCD	3/5VLCD	3/5VLCD
V3	2/5VLCD	2/5VLCD	2/5VLCD
V4	1/5VLCD	1/5VLCD	1/5VLCD



1/5 bias R=2.2K
(1/8,1/16 duty cycle)



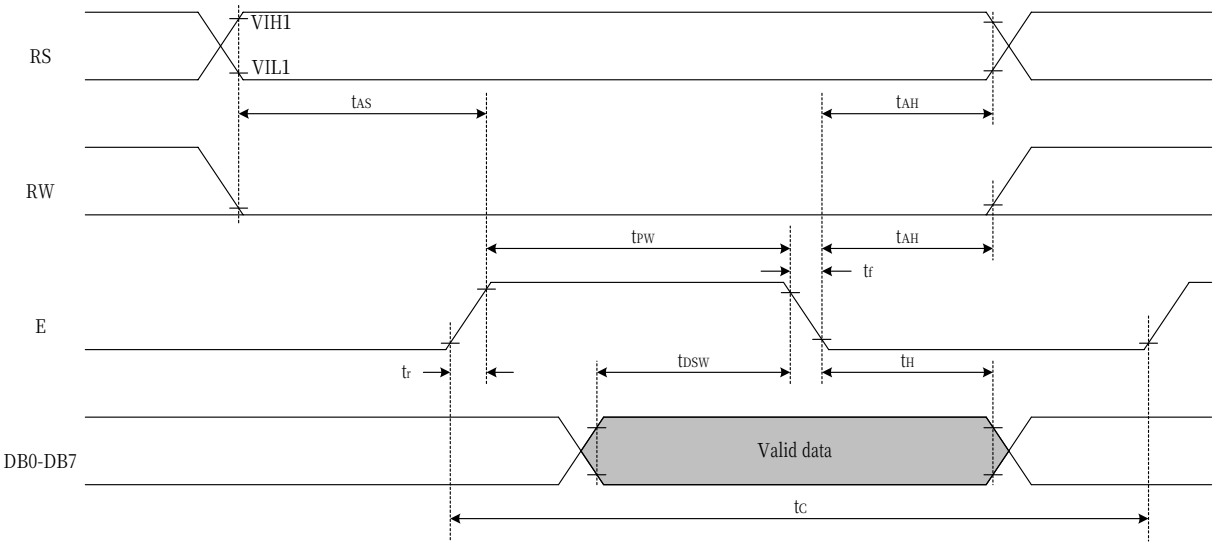
1/5 bias R=6.8K
(1/8,1/16 duty cycle)



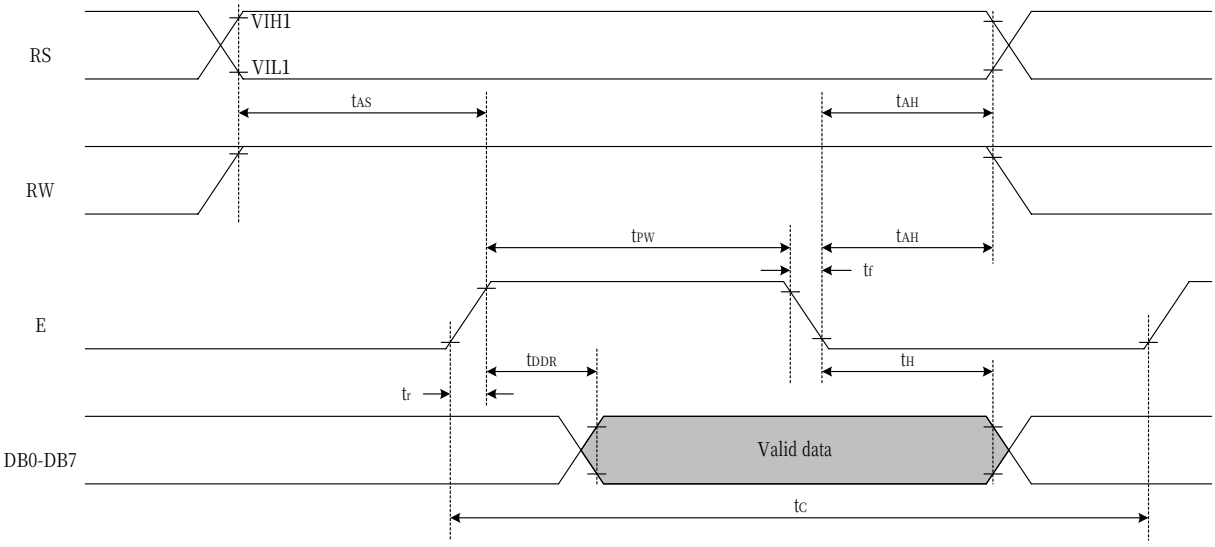
1/5 bias R=9.0K
(1/8,1/16 duty cycle)

■ Timing Characteristics

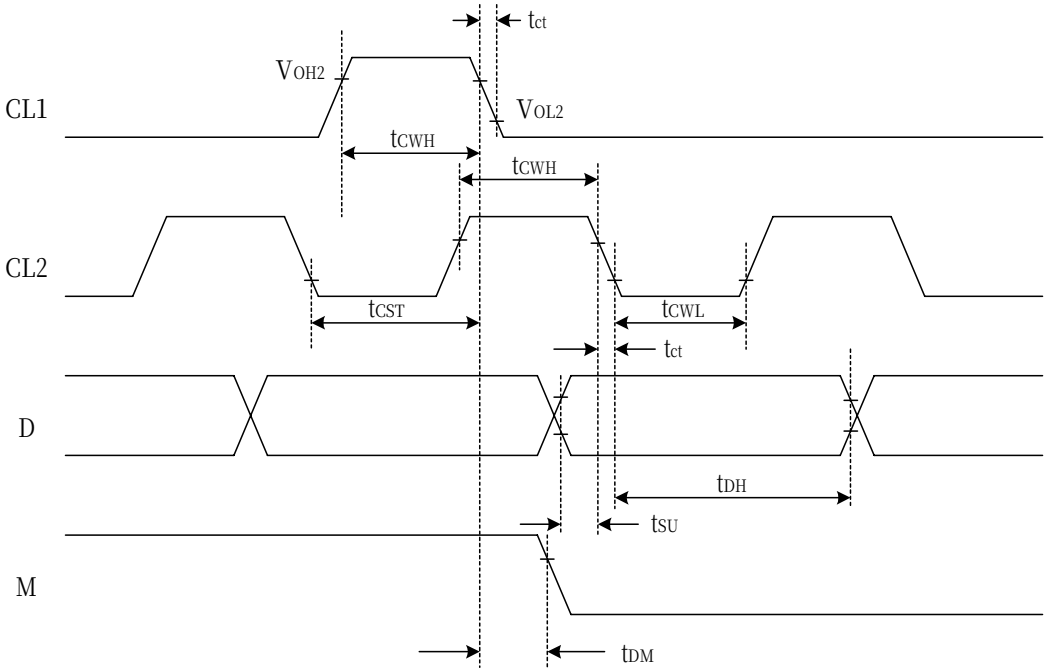
- **Writing data from MPU to IC**



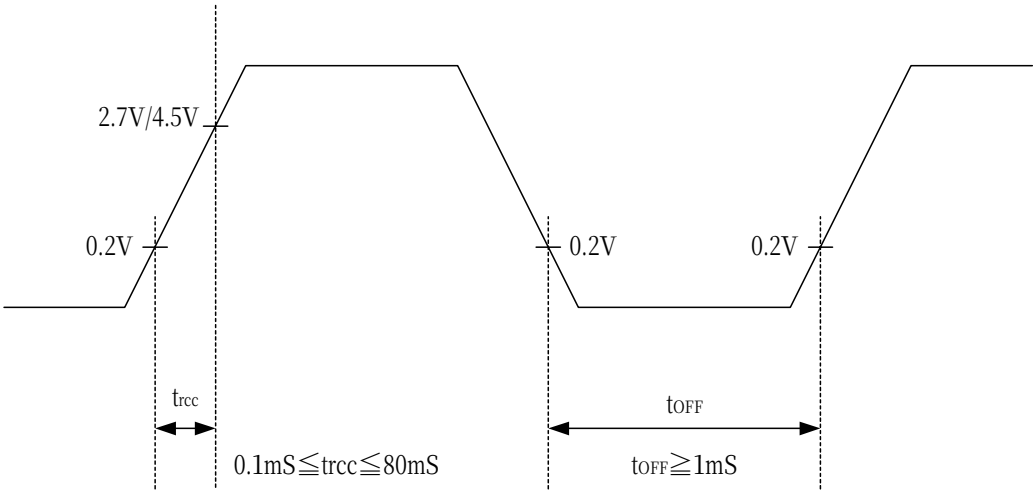
- **Reading data from IC to MPU**



- **Interface Timing with External Driver**



- **Internal Power Supply Reset**



Notes:

- tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation,and at 2.7V for 3V operation.
- For if 4.5V is not reached during 5V operation,teh internal reset circuit will not operate normally.

■ AC Characteristics

In 6800 interface

(TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to Controller)						
T_C	Enable Cycle Time	Pin E	40	-	-	us
T_{PW}	Enable Pulse Width	Pin E	40	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	20	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from Controller to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	480	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	320	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ AC Characteristics

In 6800 interface
(TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to Controller)						
T_C	Enable Cycle Time	Pin E	20	-	-	us
T_{PW}	Enable Pulse Width	Pin E	40	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	20	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from Controller to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7921)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ AC Characteristics

In Serial interface
(TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to controller)						
T_C	Enable Cycle Time	Pin E	2000	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	950	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,E	50	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	10	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	50	-	-	ns
Interface Mode with LCD Driver						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ AC Characteristics

In Serial Interface
(TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to Controller)						
T_C	Enable Cycle Time	Pin E	800	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	40	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,E	50	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	10	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	50	-	-	ns
Interface Mode with LCD Driver						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{CC}	-0.3 to +5.5
LCD Driver Voltage	V_{LCD}	Vss+7.0 to Vss-0.3
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

■ DC Characteristics

(TA = 25℃ , VCC = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V0 - Vss	3.0	-	7.0	V
I_{CC}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=3.0V	-	0.1	0.25	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2Vcc	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.75 Vcc	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.2Vcc	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	V_{CC} = 3V	10	60	120	μA

NOTE : External bias resistor select , so Idd doesn't include the follower current.

That's the end of the Manual