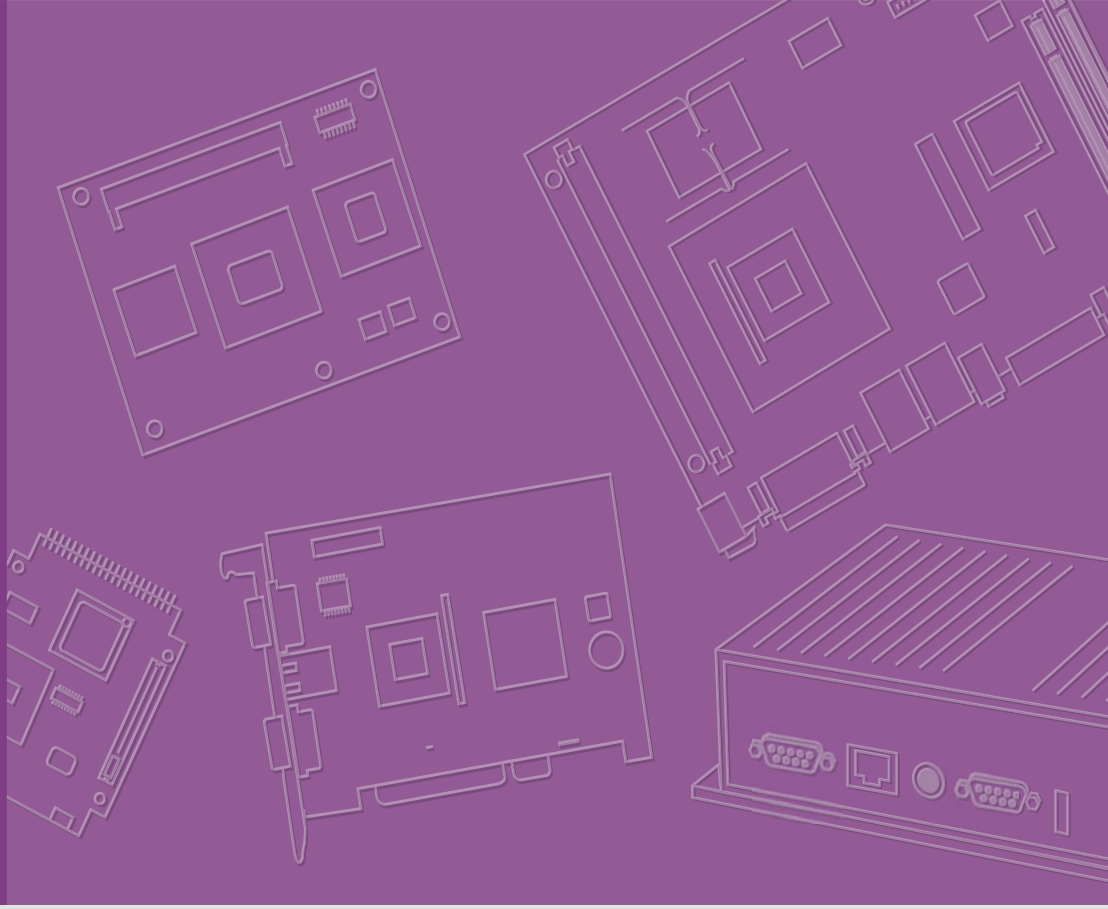


User Manual

MIC-5603

Advanced Mezzanine Card Processor AMC

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgements

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your Advantech sales representative and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your Advantech sales representative. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Part No. 2002560300 Edition 1

Printed in Taiwan February 2013

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class B

Note: This equipment, without HDMI cable connected to the front panel I/O interface, has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing - to: support@advantech.com

Packing List

- MIC-5603 Processor Advanced Mezzanine Card
- Warranty certificate document

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Keep this equipment away from humidity.
4. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
5. All cautions and warnings on the equipment should be noted.
6. Never pour any liquid into an opening. This may cause fire or electrical shock.
7. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
8. If one of the following situations arises, get the equipment checked by service personnel:
   - The power cord or plug is damaged.
   - Liquid has penetrated into the equipment.
   - The equipment has been exposed to moisture.
   - The equipment does not work well, or you cannot get it to work according to the user's manual.
   - The equipment has been dropped and damaged.
   - The equipment has obvious signs of breakage.
9. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Product Configurations

Model Number	On-Board Option
MIC-5603AFZ-M4E	Full-size front panel, 4GB DDR3 with ECC, AMC Mezzanine Module with optional on-board flash
MIC-5603AFZ-M8E	Full-size front panel, 8GB DDR3 with ECC, AMC Mezzanine Module with optional on-board flash
MIC-5603AM-M4E	Mid-size front panel, 4GB DDR3 with ECC, CFast module with optional on-board flash
MIC-5603AM-M8E	Mid-size front panel, 8GB DDR3 with ECC, CFast module with optional on-board flash

We Appreciate Your Input

Note!

1. *CFast module is available as an option.*
2. *Full size front panel design will be available upon request.*

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

Glossary

AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
BMC	Baseboard Management Controller
DMI	Direct Media Interface
ECC	Error Checking and Correction
EHCI	Enhanced Host Controller Interface
FRU	Field Replaceable Unit
FPGA	Field Programmable Gate Arrays
GbE	Gigabit Ethernet
HPM	Hardware Platform Management
IOL	IPMI-Over-LAN
IPMB	Intelligent Platform Management Bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
MCH	MicroTCA Carrier Hub
MMC	Module Management Controller
MTBF	Mean Time Between Failures
NCSI	Network Controller Sideband Interface
NVRAM	Non-Volatile Random-Access Memory
OOS	Out Of Service
PATA	Parallel Advanced Technology Interface
PCH	Platform Controller Hub
PCIe	PCI Express
PICMG	PCI Industrial Computer Manufacturers Group
PXE	Pre-boot Execution Environment
RX	Receive
RMCP	Remote Management Control Protocol
SATA	Serial Advanced Technology Attachment
SDR	Sensor Data Record
SerDes	Serializer/Deserializer
SOL	Serial-Over-LAN
SPI	Serial Peripheral Interface
TPM	Trusted Platform Module
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter

Contents

Chapter 1

Product Overview

This chapter describes briefly the product technology of the MIC-5603.

1.1 Introduction

The MIC-5603 is a highly integrated single-width, Full/mid-size processor AMC. Its design is based on the low power, high-performance Intel 2nd Generation Core™ i7 mobile processors combined with the high-performance Intel QM67 PCH. The board includes 4 or 8 GB of soldered DDR3 1333 MHz memory with ECC for higher MTBF and optimum cooling. To facilitate development, test and integration whilst offering typical network connectivity once deployed, the front panel provides two-gigabit Ethernet connector, a serial port and a USB 2.0 host port.

The MIC-5603 maximizes AMC edge connector connectivity for the best design flexibility. Two-gigabit Ethernet ports provide AMC.2 compliance and offer control and data plane connectivity to facilitate the migration of existing applications. Both ports connect to the Intel 82850 data throughput. Dual SATA interfaces provide AMC.3 compliant storage, One SATA routed to CFast daughter board for optional and One USB ports offer further connectivity opportunities.

A dedicated Module Management Controller (MMC) monitors onboard conditions and manages hot swap operation for field upgrades or module replacement without the need to power down the underlying system.

1.2 Applications

It is designed to allow communication equipment manufacturers to add modular and upgradeable computing functionality to their AdvancedTCA or MicroTCA proprietary baseboards and provide the localized capability necessary for applications such as protocol processing, packet processing, data management, and I/O management. This AMC module is hot-swappable, which allows it to be replaced by operators or service organizations in the field without bringing down an entire AdvancedTCA blade or system.

1.3 Functional Block Diagram

The hardware concept can be illustrated by the following functional block diagram. Refer to table 2.1 for the product's detailed technical specification.

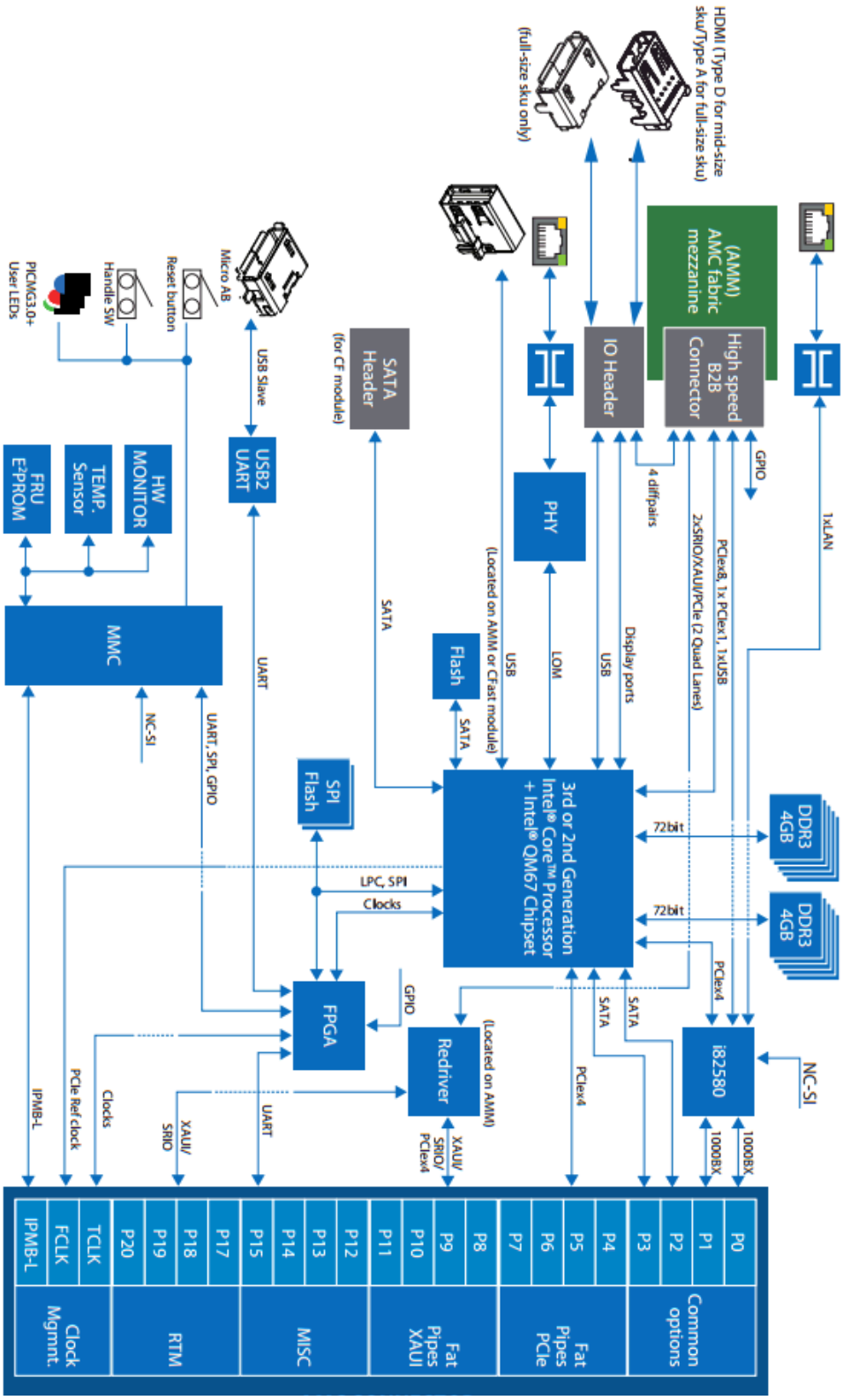


Figure 1.1 MIC-5603 Block Diagram

Chapter 2

Board Specification

This chapter describes the hardware features of the MIC-5603.

2.1 Technical Data

Table 2.1: Advantech MIC-5603 Processor AMC Technical Data			
Processor System	CPU	Intel 2nd Generation Core™ i7 mobile processors up to 2.2 GHz (4 MB L2 cache)	
	Chipset	Intel QM67	
	BIOS	AMI (1. Dual images with update rollback, 2. NVRAM settings can be changed over IPMI, and 3. CMOS backup works without battery)	
Bus	DMI	5.0 GT/s point-to-point DMI interface to PCH	
Memory	Technology	Dual channel DDR3 1066MT/s and 1333MT/s SDRAM with ECC	
	Max. Capacity	8 GB RAM (soldered on-board memory)	
Ethernet	Controller	IntelR 82580EB Quad-port Gigabit Ethernet controller	
	Interface	One GbE accessible on front panel via RJ-45 and two SerDes links to AMC ports 0 and 1	
Mass Storage	Compact Flash	Module with CFast socket	
	On CF Module	8 (default) or 16 GB industrial grade internal flash disk (optional)	
SATA Interface	AMC Edge Connector	Two SATA interfaces (6Gbps) to common option ports 2..3	
	Other	One SATA routed to CF daughter board	
Serial Interface	I/O	Routed to front panel as USB Slave interface through onboard USB to Serial converter	
USB Interface	I/O	One USB 2.0 compliant host port (standard USB Connector) on front panel	
Watchdog Timer	Supervision	One MMC watchdog, One payload watchdog	
Management Controller	Controller	NXP LPC 1768	
	IPMI Compliancy	IPMI 2.0	
Firmware	Source Code	Advantech IPMI Core	
	Update Standard	HPM.1 compliant	
Operating System	Compatibility	WindRiver PNE-LE 3.0, RHEL, CentOS, Windows Server 2008, Windows 7 Enterprise	
Form Factor	AMC	Mid-size (or Full-size),	
	Interface	AMC.0 compliant	
Miscellaneous	LEDs	x1 blue for hot swap, x1 red for failure and OOS, x1 green for general purpose	
Power Requirement	Configuration	Intel Core i7-2610UE + QM67 + 8GB on-board DDR-III memory	
	Consumption	40 watts	
Physical	Dimension	180.6 mm x 73.5 mm	
Environment		Operating	Non-operating
	Temperature	-5 ~ 55° C (23 ~ 122° F) Note	-40 ~ 70° C (-40 ~ 140° F)
	Humidity	IEC60068-2-78 (95%RH @ 40° C)	
	Vibration (5 ~ 500Hz)	IEC60068-2-6 (0.002 G2/Hz, 1 Grms)	
	Shock	IEC60068-2-27 (10 G, 11 ms)	
	Altitude	Sea level to 4,000m above sea level	10,000m above sea leve

Regulatory	Conformance	UL94V0, FCC Class B, CE, RoHS & WEEE Ready
	NEBS Level 3	Designed for GR-63-CORE and GR-1089-CORE
Compliance	Standards	PICMG AMC.0, AMC.1, AMC.2, AMC.3, IPMI2.0, HPM.1

2.2 Product Features

2.2.1 CPU

The MIC-5603 supports the low wattage Intel 2nd Generation Core? i7 mobile processors on 32nm technology with core frequencies up to 2.2 GHz and 5.0 GT/s point-to-point DMI interface to PCH. These processors are validated with the integrated Intel QM67 PCH. This chipset provides greater flexibility for developers of embedded applications by integrating the memory and I/O control functions into a single component, addressing the needs for high-performance, high-reliability, and low-power consumption within a small form factor such as the MIC-5603. Current supported processors are listed in the table below.

Table 2.2: Intel Processor Selection for the MIC-5603

Model	Core Speed	DMISpeed	Intel Smart Cache	TDP	Package
Intel Core i7-2655LE	2.2 GHz	5 GT/s	4 MB	25 W	FCBGA1023
Intel Core i7-2610UE	1.5 GHz	5 GT/s	4 MB	17 W	FCBGA1023

2.2.2 BIOS

Two 8 MB SPI Flashes contain board-specific BIOS (from AMI) designed to meet telecom and embedded system requirements. The BIOS boot sector contains the early start-up code.

2.2.3 Chipset

The QM67 PCH includes a four-channel Enhanced Direct Memory Access (EDMA) controller, offering low-latency and high throughput data transfer capability with no CPU intervention for higher overall system performance. It also integrates I/O controller features such as Serial ATA, PCI, and USB, saving board real estate and power by removing the need for a separate, legacy I/O bridge chip. For demanding I/O and networking applications, the PCIe interfaces support for up to eight ports with transfers up to 5 GT/s. Refer to the following figure for the PCH I/O interfaces.

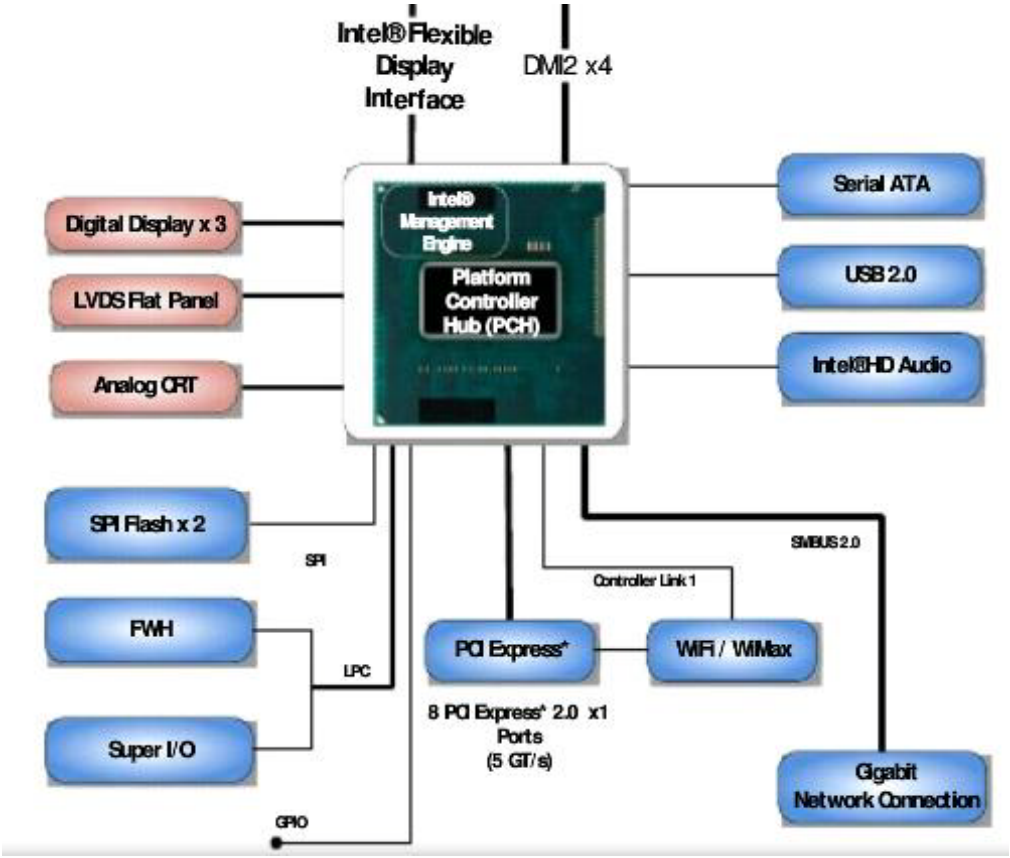


Figure 2.1 INTEL QM67 Chipset

2.2.4 Memory

The 2nd Generation Intel Core Processor provides two channels of system memory with nine DDR3 SDRAMs per channel & supports memory DDR3 data transfer rates of 1333MT/S with ECC. The 2nd Generation Intel Core Processor supports 1 Gbit and 2 Gbit and 4Gbit memory technologies. However, according to product options, the MIC-5603 uses 18 pieces of either 2 Gbit (256 Mb x 8) or 4Gbit (512Mb x 8) SDRAMs (with total capacity of 4GB or 8GB, respectively).

2.2.5 Ethernet Controller

The MIC-5603 uses one Intel 82580EB LAN controller, connected to the 2nd Generation Intel Core Processor through a PCIe x4 interface, to provide two GbE connections (1000BX) to Port 0 & Port 1 & one GbE accessible on the AMC front panel via RJ45 port.

2.2.6 SATA Interface

The QM67 PCH has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 6.0 Gb/s (600 MB/s) on up to two ports while all ports support rates up to 3.0 Gb/s (300 MB/s) and up to 1.5 Gb/s (150 MB/s). Two of these six ports, namely SATA 0 and SATA 1 are routed to AMC edge connector, SATA 3 to the Compact Flash expansion board connector for SATA-PATA interface conversion & SATA 2 for on-board Flash.

2.2.7 USB Host Interface

The QM67 PCH also has USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate-matching hubs provide support for up to fourteen USB 2.0 ports

2.2.8 MMC

The management firmware of the MIC-5603 is implemented on NXP's LPC1768, which is based on a 32-bit ARM Cortex-M3 core. It contains 512 kB internal Flash, a total of 64 kB SRAM and operates with up to 100MHz. An external SPI EEPROM is used for storing FRU inventory data and non-volatile configurations. The deferred firmware image is stored in an external SPI flash.

2.2.8.1 Key Features

- Advantech Integrity Sensor
- Based on Advantech IPMI Core, designed for μTCA and ATCA
- IPMI 1.5 and IPMI 2.0 Specification compliant
- IPMI-over-LAN
- Serial-over-LAN
- KCS interface for direct IPMI communication between Operating System and MMC
- BIOS fail over, including BIOS watchdog
- Full BMC Watchdog support as defined in IPMI specification
- Full MMC Firmware redundancy
  - Manual roll back
  - Automatic roll back if update failed
- HPM.1 for in field updates, supporting:
  - MMC Firmware
  - FPGA
  - BIOS
  - NVDATA (BIOS settings)
- Proven interoperability with different μTCA and ATCA vendors
- Specification compliance tested with Polaris Compliance Tester
- Automatic UART muxing between all serial interfaces for easy console access
- Additional sensors for hardware monitoring

2.2.9 Integrated Clock Controller

The PCH contains a Fully Integrated Clock Controller (ICC) generating various platform clocks from a 25 MHz crystal source. The ICC contains up to eight PLLs and four Spread Modulators for generating various clocks suited to the platform needs The ICC supplies up to ten 100 MHz PCI Express 2.0 Specification compliant clocks, one 100 MHz BCLK/DMI to the processor, four 33 MHz clocks for SIO/LPC/TPM devices and four Flex Clocks that can be configured to various frequencies that include 14.318 MHz, 33 MHz and 24/48 MHz for use with SIO, LPC, and discrete Graphics devices.

2.2.10 Legacy USB Support

The legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. The legacy USB support allows the user to access the BIOS setup menu and install an operating system that supports USB. The legacy USB support is set to "Enabled" by default.

Note! *The legacy USB support is for keyboards, mice and hubs only. It does not support other USB devices except bootable devices like CD-ROM drives and floppy disk drives.*

2.2.11 On-board Storage Flash Chip

An on-board 8GB storage chip, located on the CFast expansion mezzanine module is the single device, solid-state drives supports standard SATA protocol. The built in microcontroller and file management firmware communicates with SATA standard interfaces. It provides complete SATA Hard Disk Drive functionality and compatibility in a BGA package.

Note! *A 16GB storage option is available for the NAND flash's capacity.*

2.2.12 CFast Expansion Module

CFast expansion mezzanine module is a standard feature on the AMC. The CFast card provides high capacity data storage that electrically complies with the Serial ATA International Organization standard & Applications that demand low power (Flash based CF consumes less than 5 percent the power of 1.8- and 2-inch disk drives) And as the disk drive industry ends the manufacturing of PATA drives, CFast becomes an attractive and less-expensive alternative to SATA hard drives

2.2.13 Trusted Platform Module (Optional)

As an option, a Trusted Platform Module can be available on the board. It provides single chip, turnkey solution, enabling high levels of hardware security and interoperability, while maintaining exceptional user convenience and privacy for embedded application. It implements version 1.2 of the Trusted Computing Group specification for Trusted Platform Modules. The chip communicates with the system through the LPC interface.

2.2.14 Handle Switch

A handle switch is implemented to facilitate the insertion, locking, and extraction of the AMC module from the carrier board in addition to the state change of the hot swap micro-switch. When the handle is pushed towards the front panel by the user, the switch is toggled to confirm AMC insertion. On the other hand, when the handle is pulled away from the front panel, the micro-switch will resume its original position to indicate a request for AMC extraction to the Module Management Controller (MMC). The MMC sends a Module Hot Swap event message to the Carrier IPMC when the hot swap micro-switch changes state. The handle switch type and location are designed according to the PICMG AMC.0 Rev2.0 specification.

2.2.15 Front Panel Ports and Indicators

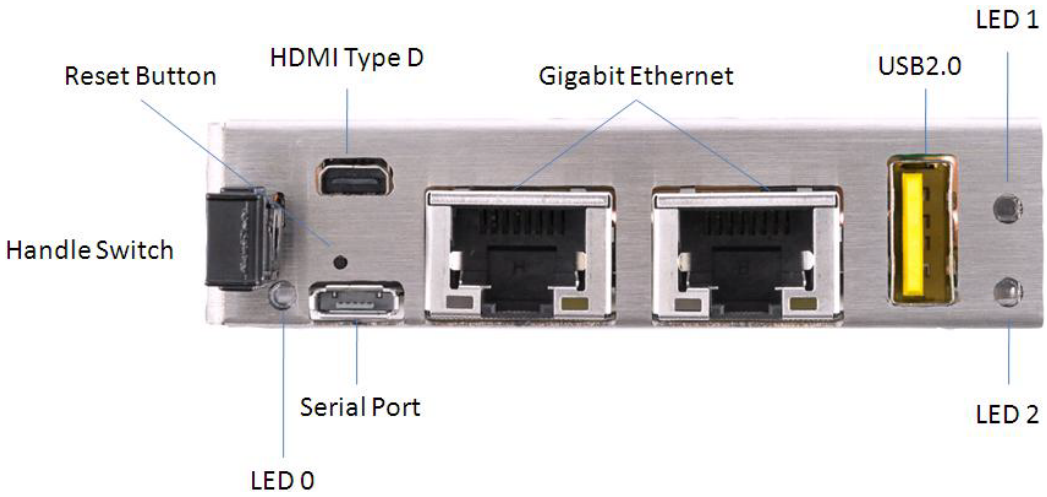


Figure 2.2 MIC-5603 Front Panel

2.2.15.1 Reset Button

The reset button on the front panel is controlled by the MMC. Two different reset button modes are supported.

- When the reset button is pressed and released within 1 second, the payload (x86 system) will reset.
- When the reset button is pressed for more than 5 seconds, the MMC will cold reset.

Note! *As long as the reset button is active-pressed, the red LED will light in order to indicate a successful reset contact.*

2.2.15.2 Micro USB Console Port

A micro USB 2.0 compliant slave port is used for debugging, diagnostic information and implementation of a serial console interface. This function is derived from the on-board USB-to-Serial converter.

2.2.15.3 USB 2.0 Port

There is a USB 2.0 compliant host port on the front panel for USB 2.0 device connection.

2.2.15.4 RJ-45 LAN Port

Two RJ45 are available on the front panel for 10/100/1000 Base-T Ethernet connection which come through PCIe based Intel 82580 & 82579 MAC/PHY.

Table 2.3: LAN LEDs

LED	Color	Description
0	Green	Solid = Link Flashing = Activity
1	Green/Orange	Off = 10 Mbps Green = 100 Mbps Orange = 1000 Mbps

2.2.15.5 MMC LED Indicators

The MIC-5603 supports three front panel LEDs.

Table 2.4: Front Panel LEDs

LED	Color	Description
0	Blue	Hot swap indicator
1	Red	Out of service indicator
2	Green	Flashing = FW application active, payload (x86) in sleep Solid = FW application active, payload (x86) active

Chapter 3

Console Terminal Setup

This chapter describes, through an example, how to setup a console for the MIC-5603.

3.1 USB to UART Bridge

TThe MIC-5603 contains a console port (micro-USB) on the front panel. The MIC-5603 uses a USB-to-UART bridge called CP2102 from Silicon Laboratories to convert data traffic between USB and UART formats. This chip includes a complete USB 2.0 full-speed function controller, bridge control logic, and a UART interface with transmit/receive buffers and modem handshake signals.

For a terminal PC to bridge successfully to the console function on the MIC-5603, the CP2102 driver available for download from Silicon Laboratories website (hyperlink below) must be installed on the terminal PC (for example, running on Linux 2.4 or 2.6 Kernel or Windows XP).

https://www.silabs.com/products/interface/usbtouart/Pages/default.aspx

3.2 Terminal Emulator

A terminal emulator application must be available on the terminal PC in order to access the console screen. If your terminal PC runs on Microsoft Windows, a common application that can act as a client for the SSH, Telnet, rlogin, and raw TCP protocols called PuTTY can be installed and used. It was originally written for Microsoft Windows; however, it has also been ported to various Unix-like operating systems. And, it is free and open source software available for download from the internet.

3.3 PuTTY Configuration

Assuming both CP2102 driver and PuTTY have been installed successfully in the terminal PC with Microsoft Windows, you can check the COM port (UART) number under "COM and LPT" in the "Device Manager", which can be accessed by entering the "Control Panel" followed by opening up "System" and then "Hardware".

Let us assume the CP210x USB to UART Bridge Controller has been assigned with "**COM5**", you can open up PuTTY and begin the configuration as shown below.

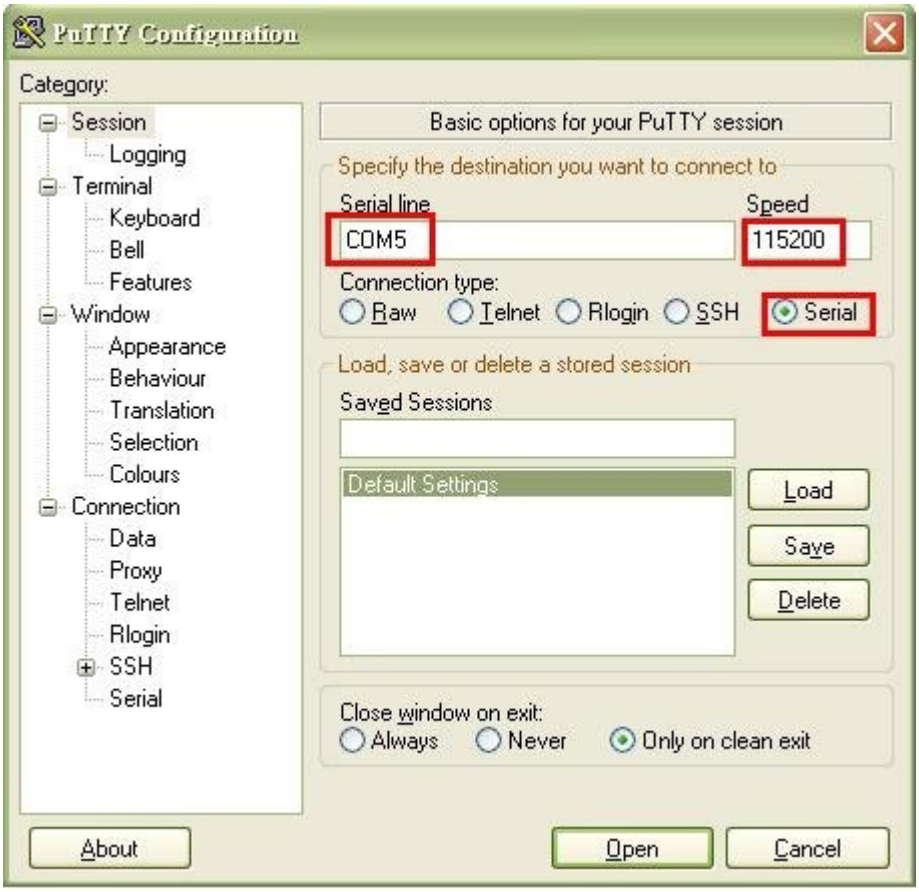


Figure 3.1 PuTTY configuration

- Specify **COM5** under serial line and **115200** for speed.
- Check **Serial** for connection type.
- Click the "Open" button and a PuTTY terminal screen as shown below will appear.

Figure 3.2 PuTTY screen

If the connection is successful, upon boot up the MIC-5603's BIOS POST will be displayed on the PuTTY screen.

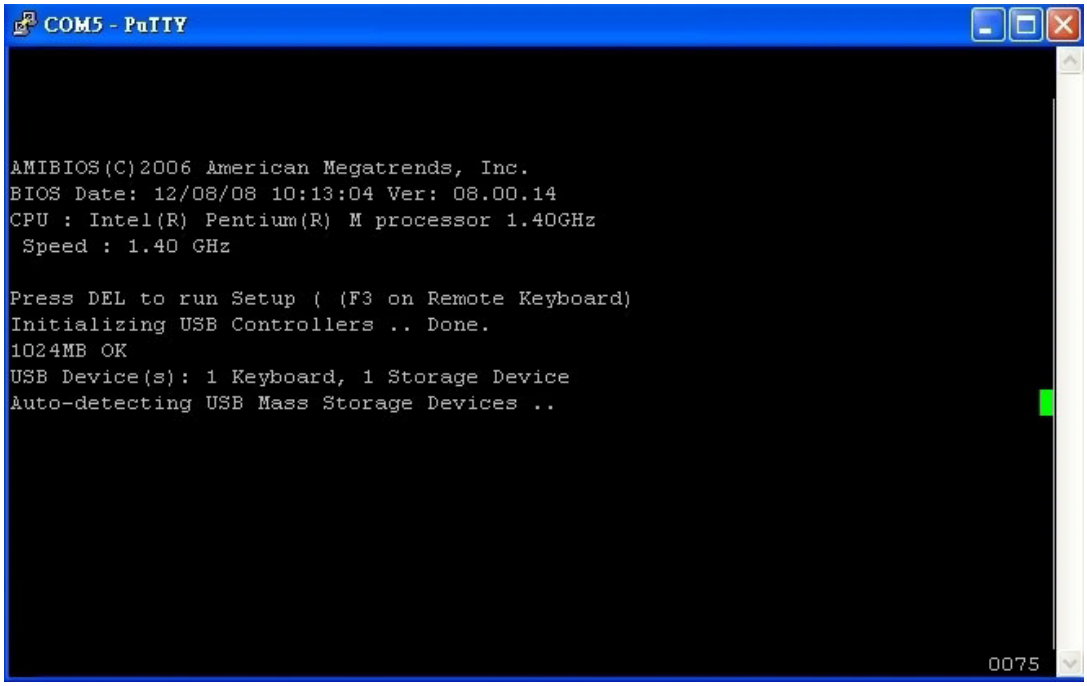


Figure 3.3 MIC-5603 BIOS POST Shown on PuTTY Screen

Chapter 4

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

4.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for over a decade. This section describes the BIOS which has been specifically adapted to the MIC-5603. With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of the MIC-5603. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-5603 setup screens.

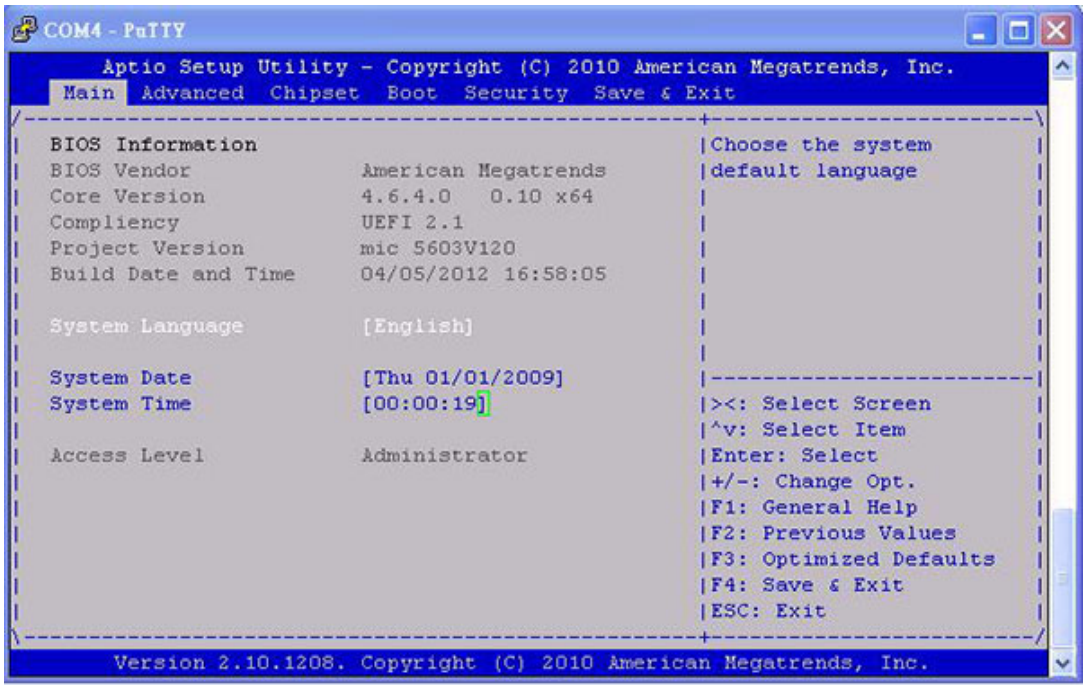


Figure 4.1 Setup Program Initial Screen

The BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration.

4.2 Entering Setup

To run the BIOS setup menu, simply press the <DEL> or <F2> key on the USB keyboard when the boot-up screen (see Figure 4.2) appears following system power up.

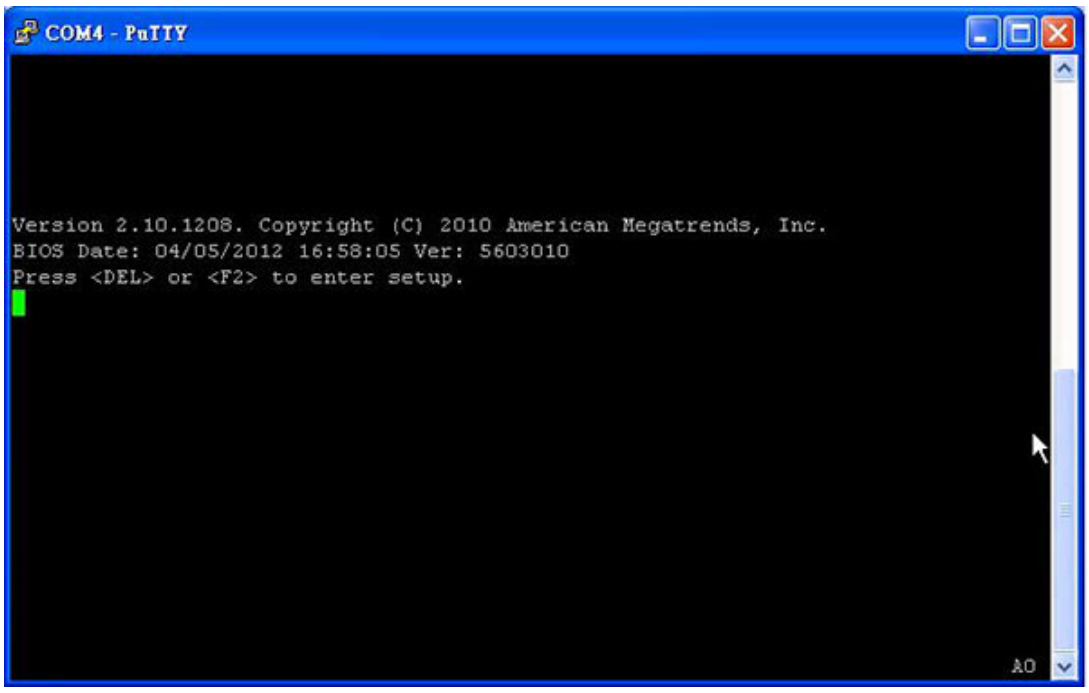


Figure 4.2 Press <DEL> to Run Setup

4.3 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

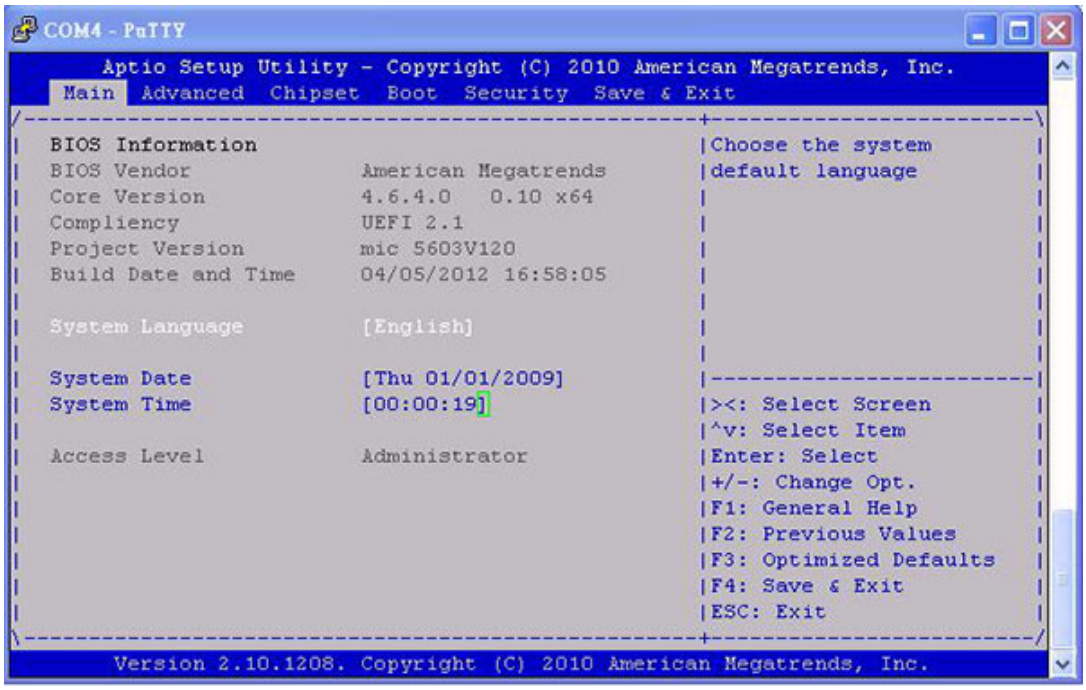


Figure 4.3 Main Setup Screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured while options in blue can. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

4.3.1 System Time and System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note! *There is no battery-backed up RTC on the MIC-5603 standard model therefore the system time and date will not be updated continuously when the power to the processor AMC is off.*

4.4 Advanced BIOS Feature Setup

Select the Advanced tab from the MIC-5603 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

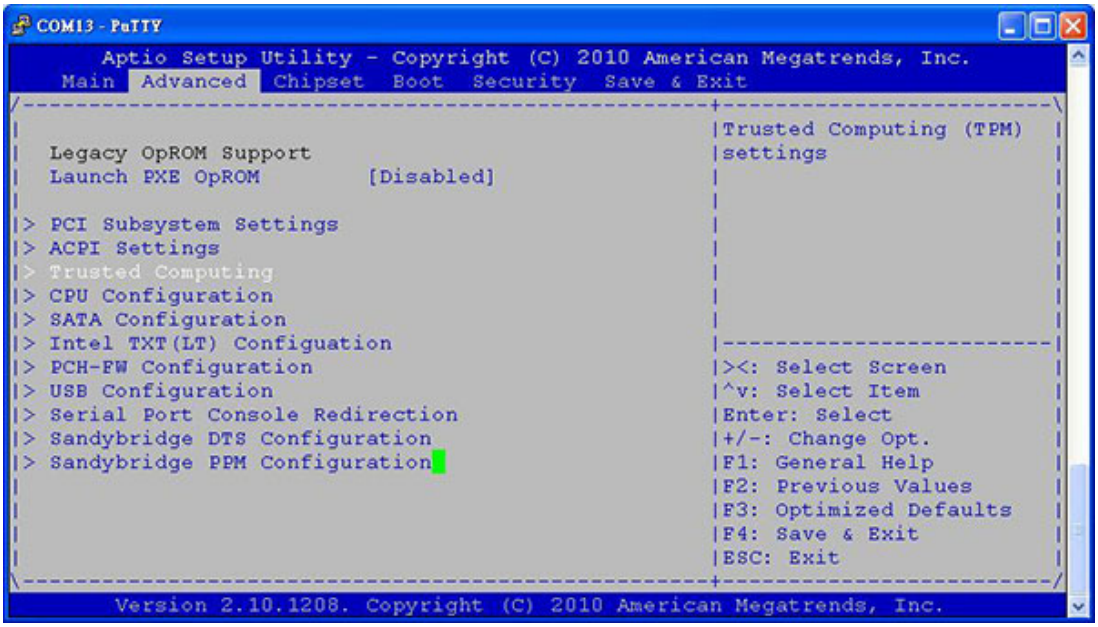


Figure 4.4 Advanced BIOS Features Setup Screen

4.4.1 Launch PXE OpROM [Disabled]

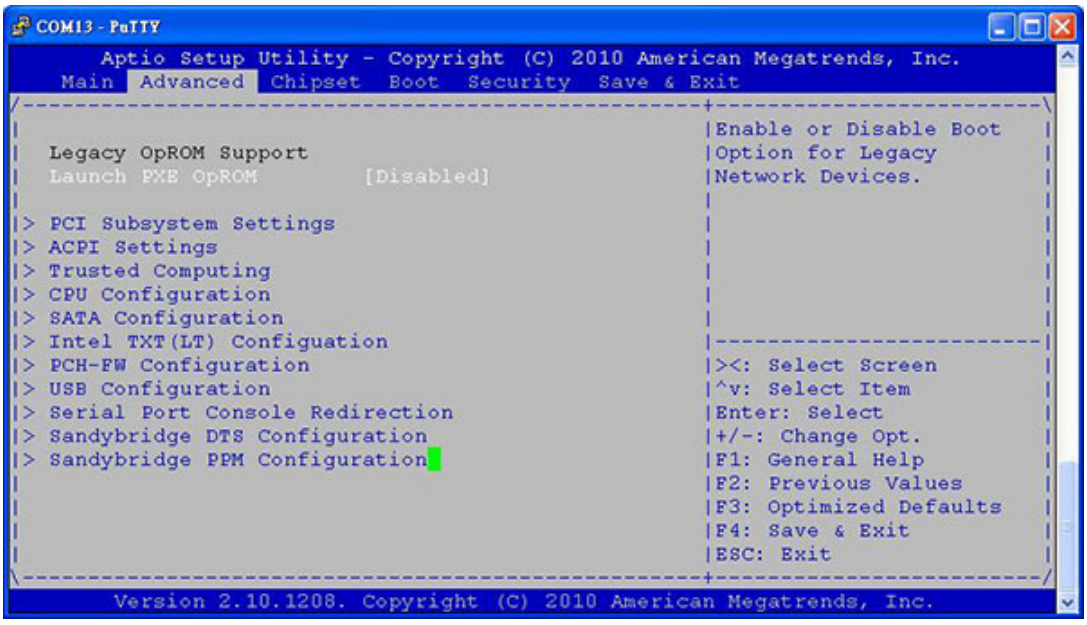


Figure 4.5 Launch PXE OpROM

Disabled: Use this setting to ignore all PXE Option ROMs

Enabled: Use this setting to load PXE Option ROMs. To limit the PXE support to particular devices

4.4.2 PCI Subsystem Setting

This screen provides functions for specifying the PCI Express device settings

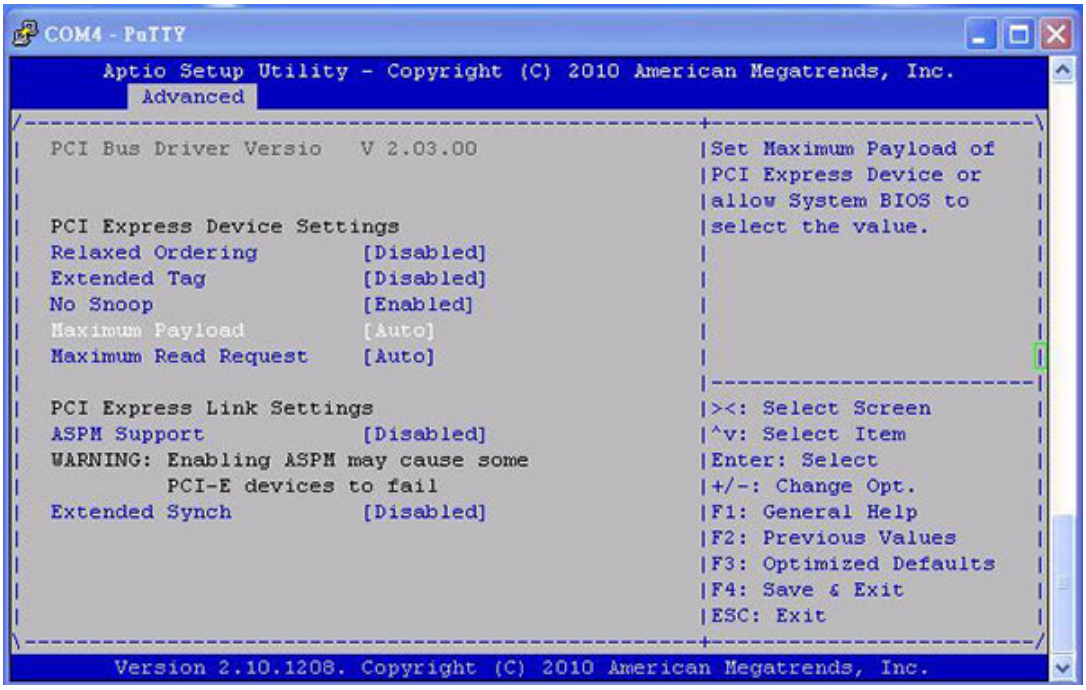


Figure 4.6 PCI Express subsystem settings

4.4.2.1 Relaxed Ordering

Relaxed ordering allows certain transactions to violate the strict-ordering rules of PCI; that is, a transaction may be completed prior to other transactions that were already enqueued.

4.4.2.2 Extended Tag

When set, this bit enables a Function to use an 8-bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field.

4.4.2.3 No Snoop

If this bit is set, the function is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency

4.4.2.4 Maximal Payload

Packet size from 128Bytes to 4092Bytes

4.4.2.5 Minimal Read Request

Packet size from 128Bytes to 4092Bytes

ASPM Support

This feature allows power to individual serial Links in a PCI Express fabric to be incrementally reduced as a Link becomes less active. The default setting is "Disabled"

Warning! *Enable ASPM may cause some PCIe device to Fail*

4.4.2.6 Extended Synch

This bit when set forces the transmission of additional ordered sets when exiting the L0s state & when in the Recovery state.

4.4.3 ACPI Configuration

ACPI is the newer power management in the hands of the operating system. APM is controlled by the BIOS. In addition, it is available by default when ACPI is disabled.

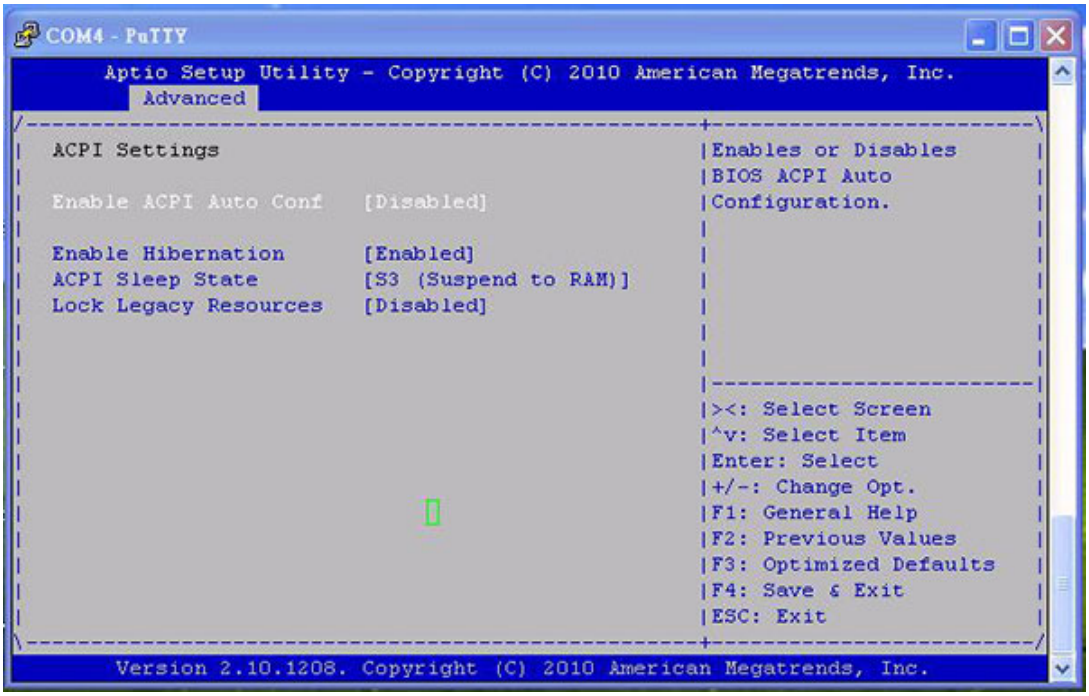


Figure 4.7 ACPI settings

Note! *If ACPI is disabled, the functionality of graceful OS shutdown becomes unavailable.*

4.4.3.1 Enable Hibernation [Enabled]

All is powered off, but the memory was saved like temporary file on the hard drive. This mode is called "Save to disk".

4.4.3.2 ACPI Sleep State [S3 (Suspend to RAM)]

S1 (Sleep): The CPU is stopped; The RAM is regenerated; the system functions in reduced power.

S3 (Standby): The CPU does not have any power; The RAM regenerates at minimum; the power supply unit is in mode of reduced power. This mode is also called "Suspend to RAM".

4.4.3.3 Lock Legacy Resources [Disabled]

When enabled (locked), this option prevents the operating system from modifying assignments for legacy resources (serial, parallel, and PS/2 ports).

4.4.4 Trust Computing

This screen provides functions for specifying the TPM configuration settings and TPM displaying status information.

Figure 4.8 Trust Computing

The hardware support for TPM on the MIC-5603 series is available by request therefore the default setting for this feature is "No" in BIOS.

4.4.5 CPU Configuration

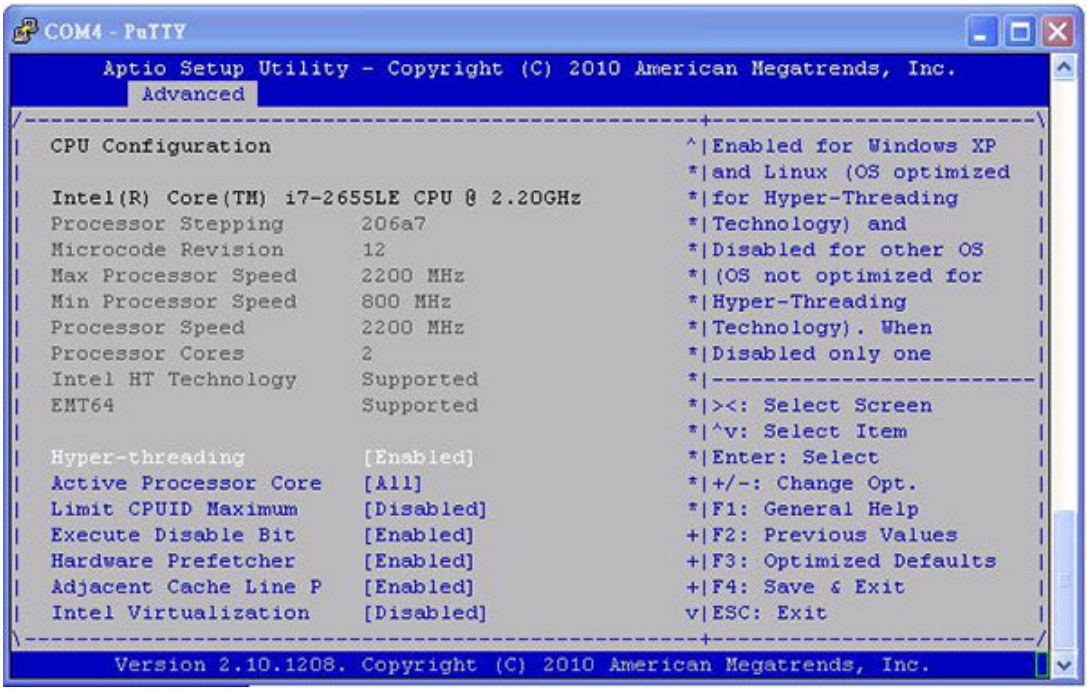


Figure 4.9 CPU Configuration

4.4.5.1 CPU Configuration

This is a display-only function indicating general information about the installed CPU.

4.4.5.2 Hyper-threading [Enabled]

Intel's proprietary HT Technology is used to improve parallelization of computations (doing multiple tasks at once) performed on PC microprocessors

4.4.5.3 Active Processor Core [All]

Select the numbers of cores in each processor package.

Configuration options: [All] [1] (It depends on each CPU type.)

4.4.5.4 Limit CPUID Maximum [Disabled]

This function is used to limit the return value for the maximum CPUID input value to 03h when queried.

4.4.5.5 Execute Disable Bit [Enabled]

Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.

4.4.5.6 Hardware Prefetcher [Enable]

The Processor has a hardware prefetcher that automatically analyzes its requirements a prefetched data & instructions from the memory into the Level 2 cache. This reduces the latency associated with memory reads

4.4.5.7 Adjacent cache line P [Enable]

The processor has a hard ware adjacent cache line prefetch mechanism that automatically fetched an extra 64-byte cache line whenever the processor requests for a 64-byte cache line this reduces cache latency by making the next cache line immediately available if the processor requires it as well

4.4.5.8 Intel Virtualization

This function is used to enable a Virtual Machine Manager (VMM) to utilize the additional hardware capabilities provided by the Vanderpool Technology. To change the state of this function, a hardware reset is necessary.

4.4.6 SATA Configuration

This is a display-only function indicating if a device is connected to the corresponding port. If no device is connected, the functions indicate Not Present. Otherwise, they show the device's built-in reference name followed by the device's size if the device is a hard drive.

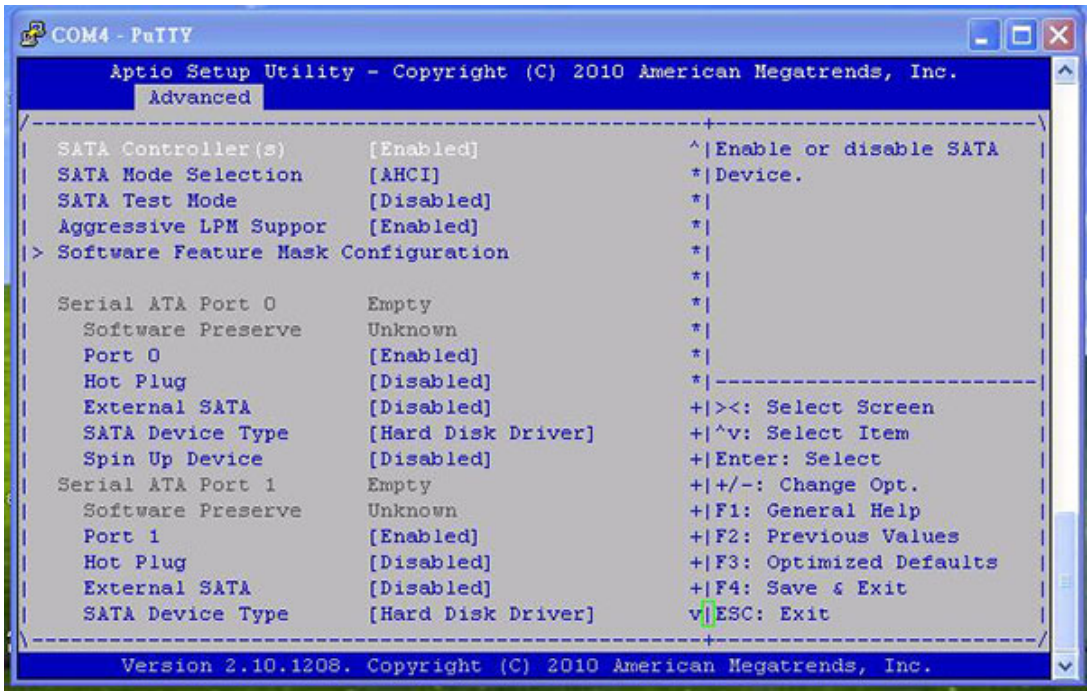


Figure 4.10 SATA configuration menu

4.4.6.1 SATA Mode Selection [AHCI]

- **AHCI Mode:** Use this setting to attach all SATA channel to one ACHI-compatible PCI mass storage controller
- **IDE mode:** When this setting is used, the following applies:
  The SATA channels 0 to 1 are logically attached to one legacy ATA compatible PCI device where channel 0 forms the primary master, channel 1 the primary slave, channel 2 the secondary master and
- **RAID mode:** Use this setting to specify that e2 channels are attached to one RAID PCI controller.

4.4.6.2 SATA Test Mode [Test Mode]

4.4.6.3 Aggressive LPM Support [Enable]

Aggressive Link Power Management (ALPM) is a power-saving Technique that helps the disk save power by setting a SATA Link to the disk to a low-Power setting during idle time (that is when there is no I/O).

4.4.6.4 Software Feature Mask Configuration

Field	Description
RAID0	Enable/Disable RAID0 feature
RAID1	Enable/Disable RAID1 feature
RAID10	Enable/Disable RAID10 feature
RAID5	Enable/Disable RAID5 feature
Intel Rapid Recovery Technology	Enable/Disable Intel Rapid Recovery Technology
OROM UI and BANNER	If enabled, shows a UI and BANNER of RAID volume info
HDD Unlock	If enabled, OS can change HDD password
LED Locate	If enabled, OS can change LED locate
IRRT Only on eSATA	If enabled, IRRT volume can span internal SATA drives and external SATA drives

4.4.7 Intel Trusted Execution Technology

Display Intel Trusted Execution Technology configuration

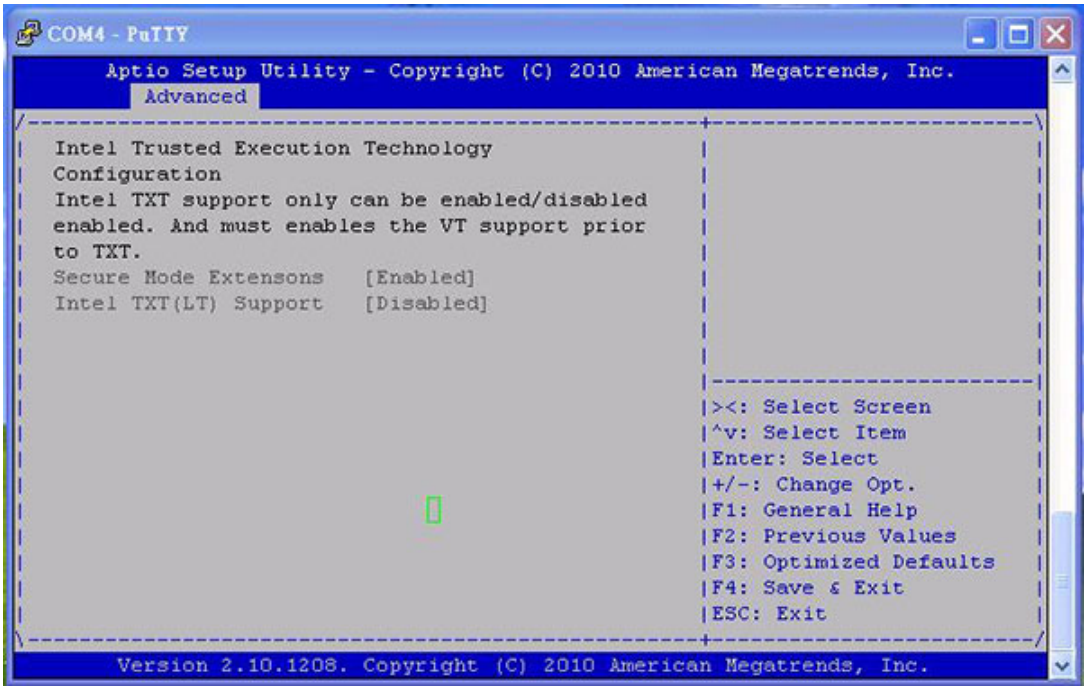


Figure 4.11 Intel Trusted Execution Technology configuration menu

4.4.8 Intel FW configuration

Display Intel FW configuration

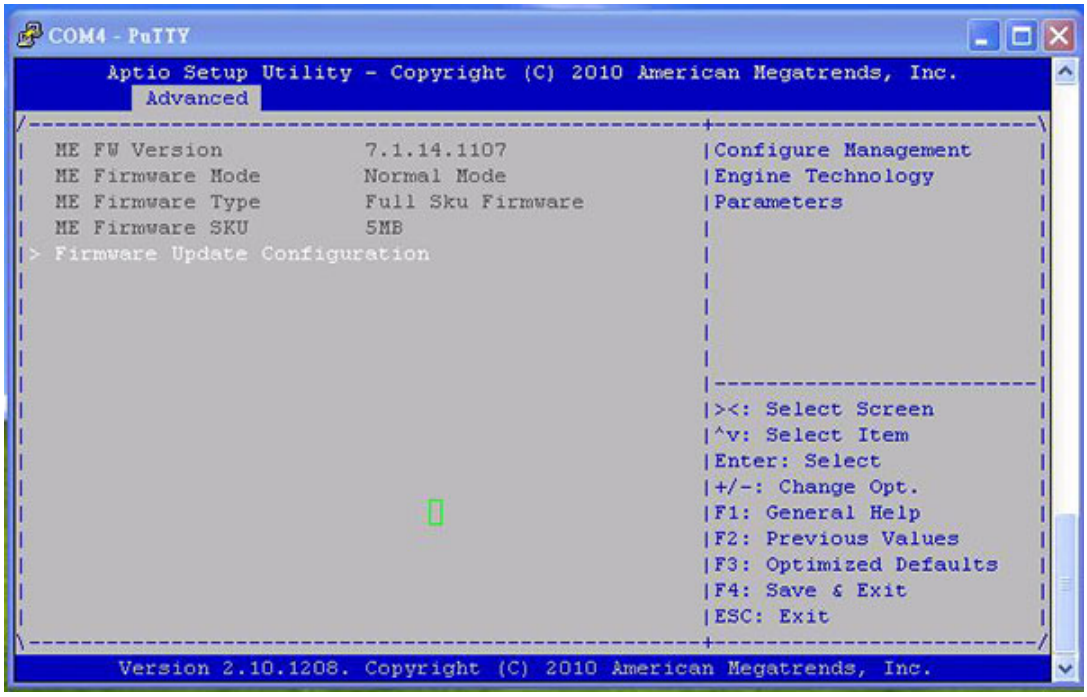


Figure 4.12 Intel Management Engine firmware configuration menu

4.4.9 USB Configuration

This is a display-only function providing general information about the USB module and the USB devices detected.

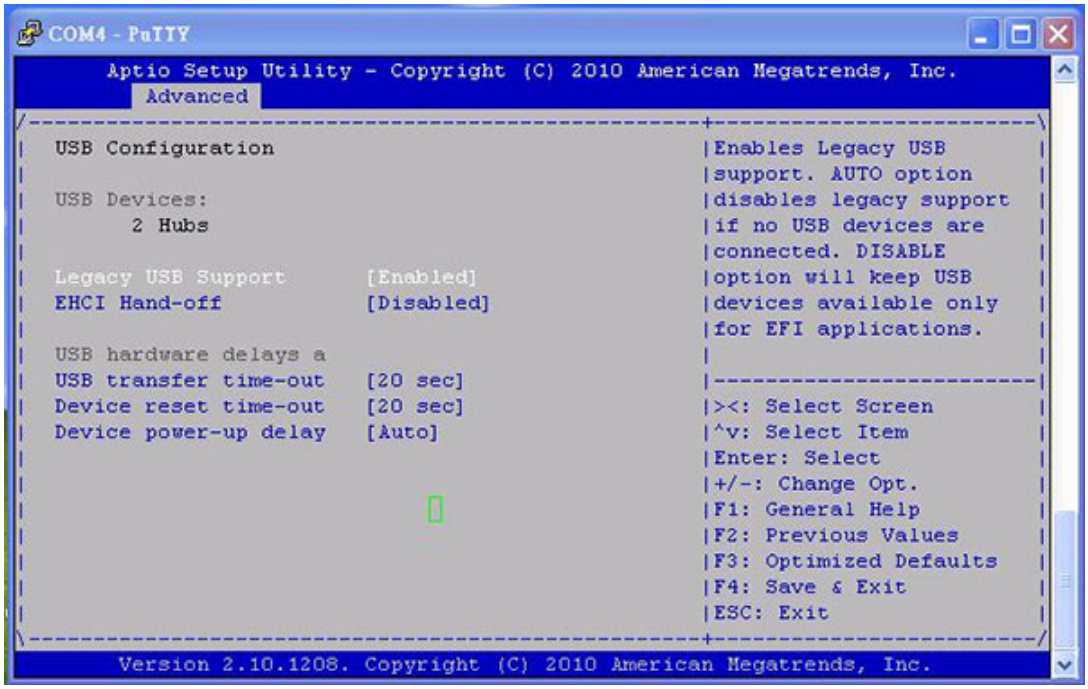


Figure 4.13 USB configuration menu

4.4.9.1 Legacy USB Support [Enable]

This function is required for booting from USB devices and for operating systems, which do not support USB themselves (mainly DOS and some BootLoaders).

4.4.9.2 EHCI Hands-Off [Disabled]

[Enabled] Enables the support for OS without an EHCI hand-off feature.

[Disabled] Disables the function.

4.4.9.3 USB Transfer Time Out [20sec.]

This setting specifies the timeout in seconds for Control, Bulk, and Interrupt transfers. The default is 20 seconds

4.4.9.4 Device Reset Timeout [20sec.]

This setting specifies the number of seconds the Power-On Self Test will wait for a USB mass storage device to 20 seconds

4.4.9.5 Device Power Up Delay [Auto]

Maximum time the device will take before it properly reports itself to the Host Control

4.4.10 Serial Port Console Redirection

This screen provides information about functions for specifying the Serial Port Console Redirection configuration settings.

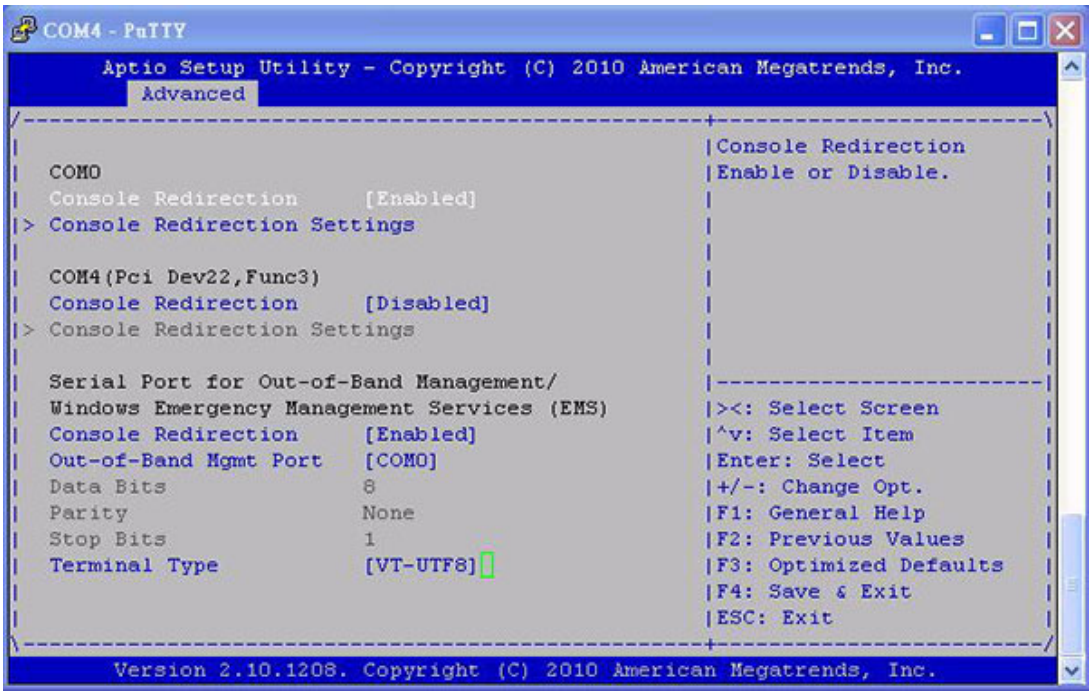


Figure 4.14 Console redirection configuration menu

4.4.10.1 COM0

Console Redirection [Enabled]

4.4.10.2 COM4 (Pci Dev22, Func3)

Console Redirection [Enabled]

4.4.10.3 Serial Port for out-of Band Management/Windows Emergency Management Services (EMS)

- **Console Redirection [Enabled]**

Use this setting to add the SPCR table to the ACPI tables. The OS can further use the information provided for serial redirection services.

- **Out-of-Band Management [COM0]**

Microsoft Windows Emergency management Services (EMS) allows for remote management of a Windows Server OS though a serial port.

- **Data Bits**

This is a display-only function providing information about the frame width for the Out-of-Band Management.

- **Parity**

This is a display-only function providing information about the parity for Out-of-Band Management.

- **Stop Bits**

This is a display-only function providing information about the number of stop bits for Out-of-Band Management.

- **Terminal Type [VT-UTF8]**

Use one of following settings to select the terminal type for out-of-band management.

VT100
VT100+
VT-UTF8
ANSI

4.4.11 Sandy Bridge DTS Configuration

This is a display-only function providing information about Sandybridge DTS configuration.

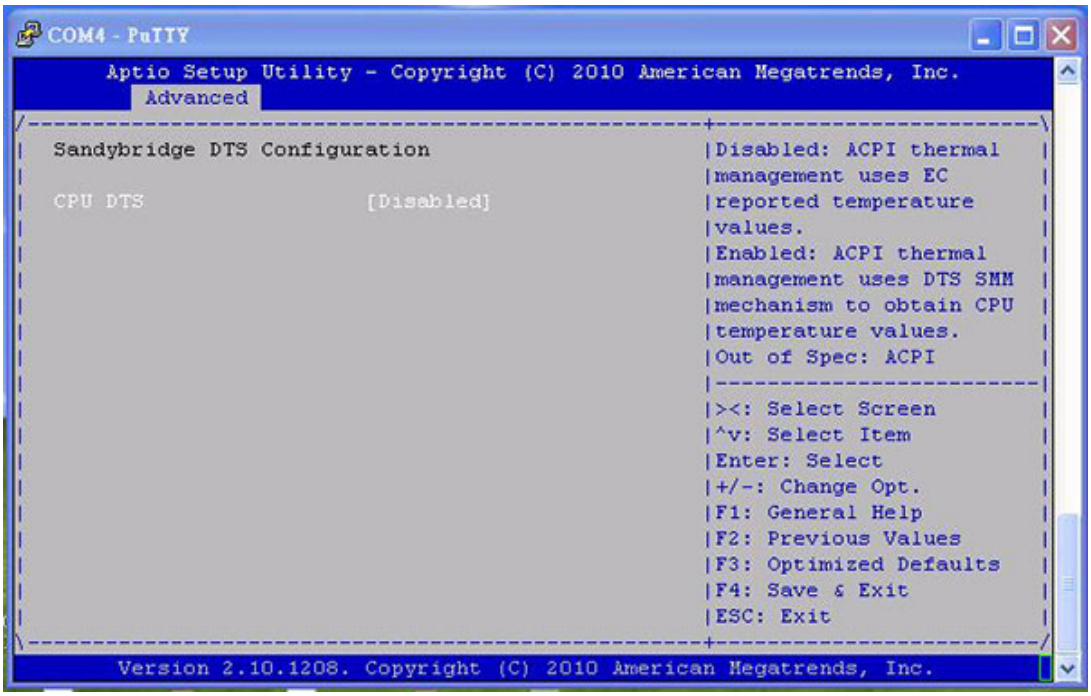


Figure 4.15 Processor Digital Thermal Sensor setting

4.4.12 Sandybridge PPM Configuration

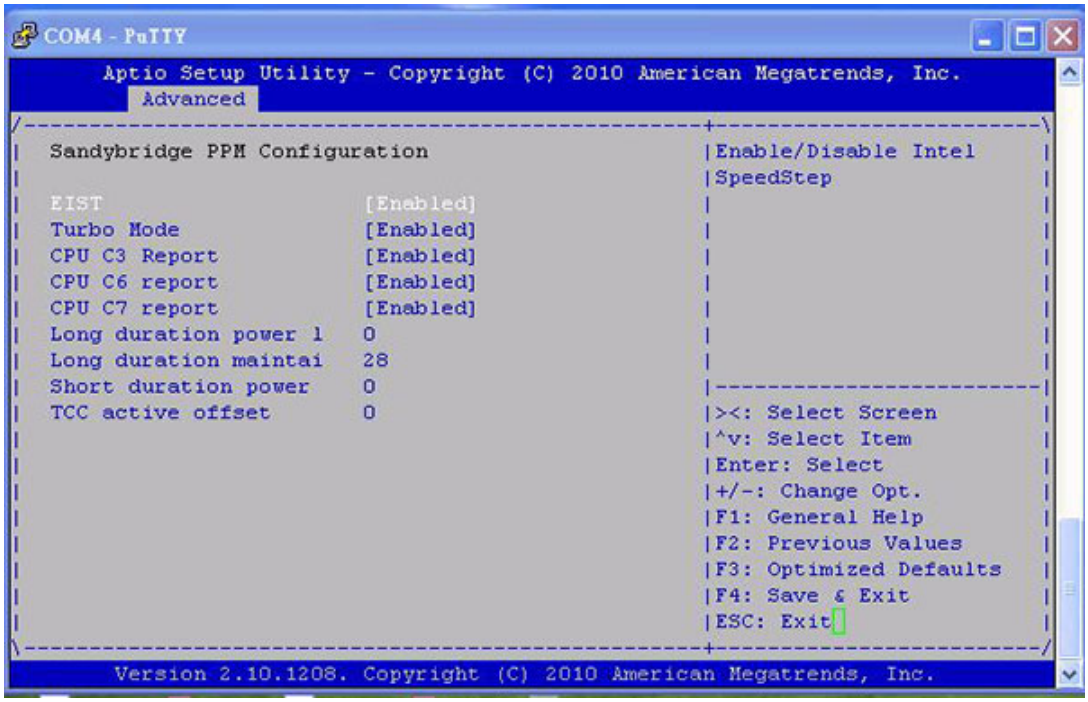


Figure 4.16 Processor PPM configuration menu

4.4.12.1 EIST [Enabled]

Enable or Disable Intel Speedstep.

4.4.12.2 Turbo Mode [Enabled]

Enable or Disable Intel Turbo Mode.

4.4.12.3 CPU C3 Report [Enabled]

Enable or Disable CPU C3 report to S0.

4.4.12.4 CPU C6 Report [Enabled]

Enable or Disable CPU C6 report to S0.

4.4.12.5 CPU C7 Report [Enabled]

Enable or Disable CPU C7 report to S0.

4.4.12.6 Long Duration power limit [0]

Long duration power limit in watts, 0 means use factory default.

4.4.12.7 Long Duration power maintained [28]

Time window, which long duration power, is maintained.

4.4.12.8 Short Duration power limit [0]

Short duration power limit in watts, 0 means use factory default.

4.4.12.9 TCC active offset [0]

Offset from the factory TCC activation temperature.

4.5 Chipset

4.5.1 System Agent (SA) Configuration

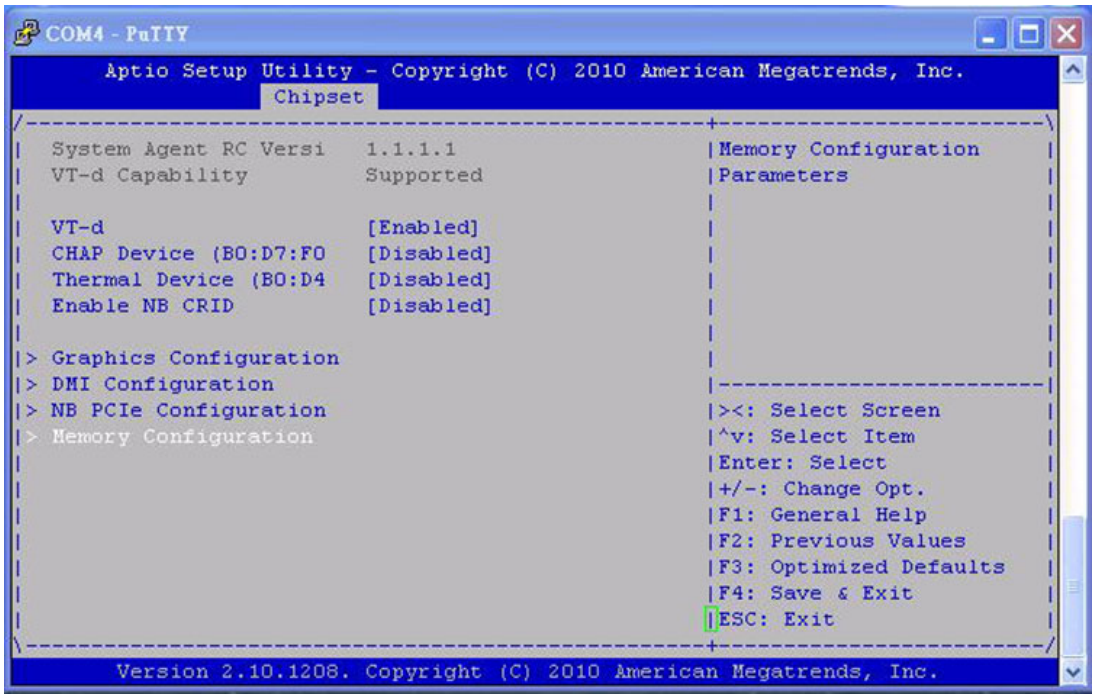


Figure 4.17 System Agent configuration menu

4.5.1.1 VT-d [Enabled]

Check to enable VT-d function on CPU

4.5.1.2 CHAP Device (B0: D7: F0) [Disabled]

Enable or disable SA CHAP Device

4.5.1.3 Thermal Device (B0: D4) [Disabled]

Enable or disable SA Thermal Device

4.5.1.4 Enable NB CRID [Disabled]

Enable or disable NB CRID Work Around

4.5.1.5 Graphics Configuration

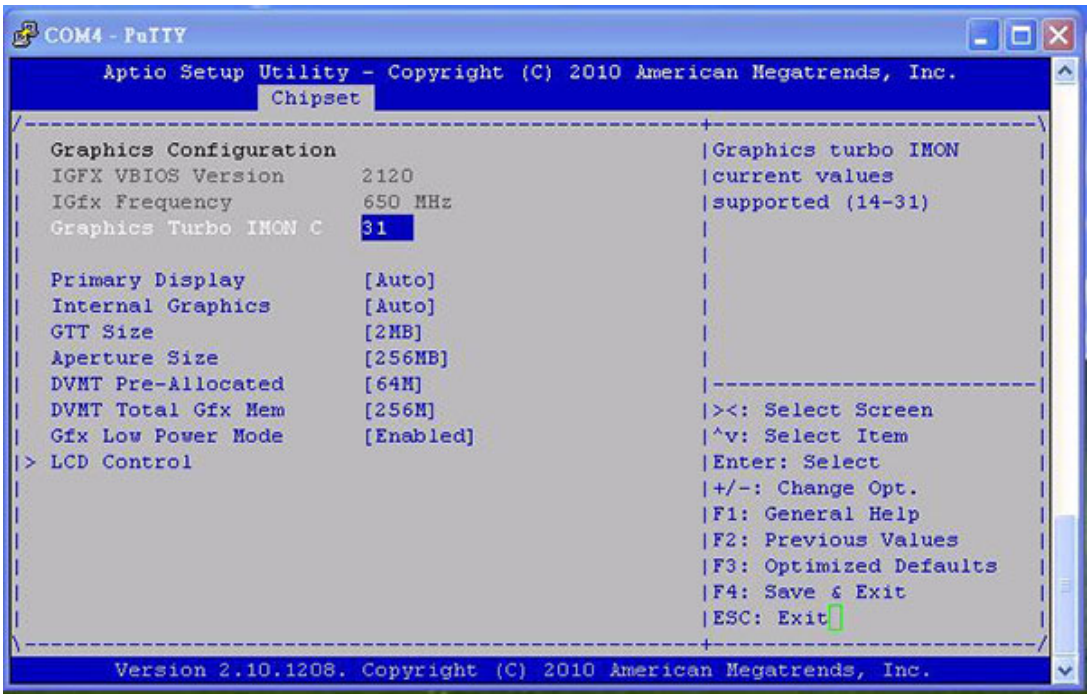


Figure 4.18 Intel graphics engine configuration menu

- **Graphics Turbo IMON Current [31]**

Graphics turbo IMON current values supported (14-31)

- **Primary Display [Auto]**

Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.

- **Internal Graphics [Auto]**

Keep IGD enabled based on the setup options.

- **GTT Size [2MB]**

Select the GTT Size

- **Aperture Size [256MB]**

Select the Aperture Size

- **DVMT Pre-Allocated [64MB]**

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

- **DVMT Total Gfx Mem [256M]**

Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.

- **Gfx Low power Mode [Enabled]**

LCD Control

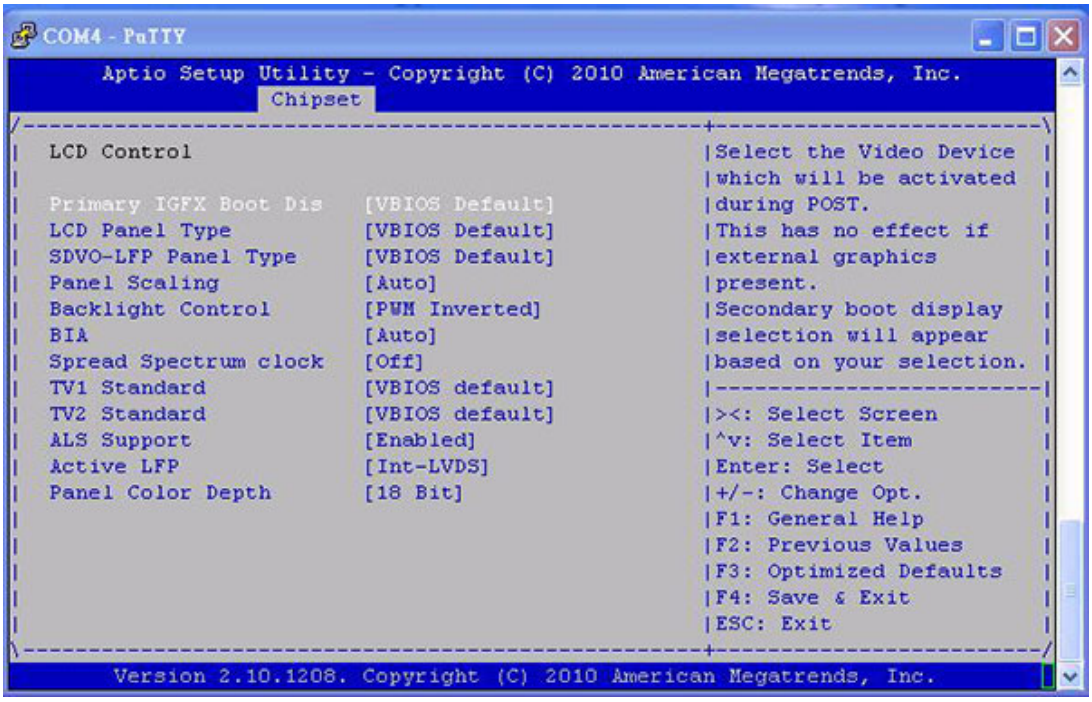


Figure 4.19 LCD control configuration menu

Primacy IGFX Boot Display [VBIOS Default]

Select the video Device, which will be activated during POST. Secondary boot display selection will appear based on selection. VGA modes will be supported only on primary display.

LCD Panel Type [VBIOS Default]

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

SDVO-LFP Panel Type [VBIOS Default]

Select SDVO panel used by Internal Graphics Device by selecting the appropriate setup item.

Panel Scaling [Auto]

Select the LCD panel scaling option used by the Internal Graphics Device

Backlight Control [PWM Inverted]

Back Light Control Setting

BIA [Auto]

Spread Spectrum clock Chip [Off]

TV1 Standard [VBIOS Default]

Select the ability to configure a TV Format

TV2 Standard [VBIOS Default]
Select the ability to configure a TV Minor Format
ALS Support

ALS Support [Enable]
Legacy = ALS Support through the IGD INT10 function,
ACPI = ALS support through an ACPI ALS driver.

Active LFP [Int-LVDS]
Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP Driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth [18 Bit]
Select the LFP Panel Color Depth
The Option: 18 Bit, 24 Bit

4.5.1.6 DMI

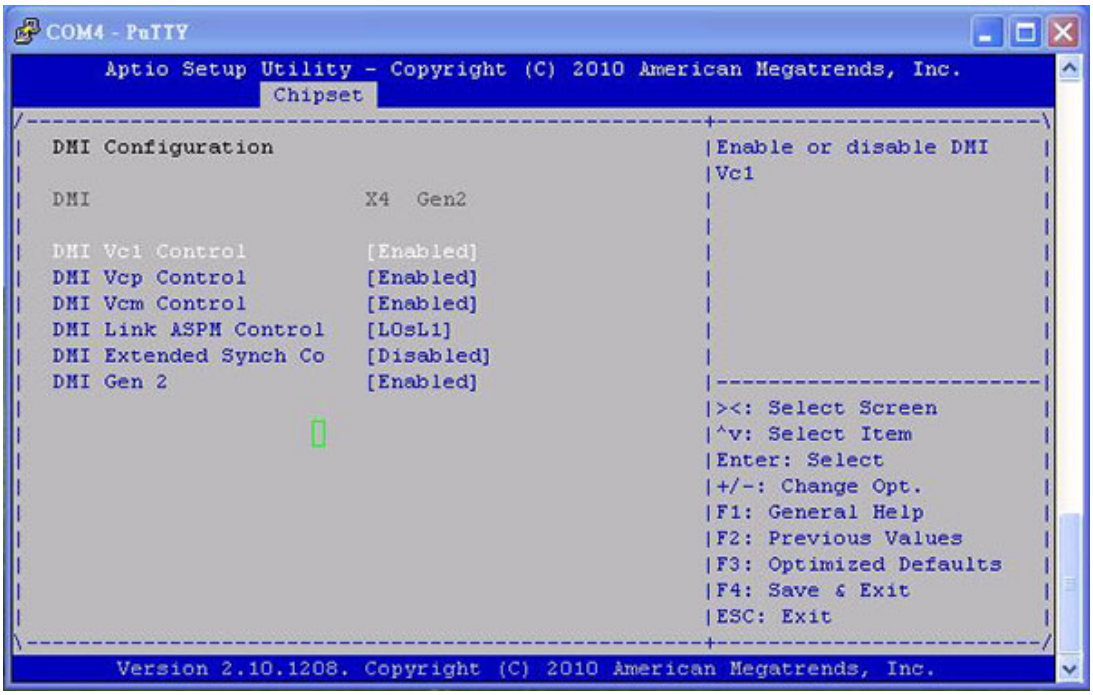


Figure 4.20 DMI configuration menu

- **DMI Vc1 Control [Enabled]**
- **DMI Vcp Control [Enabled]**
- **DMI Vcm Control [Enabled]**
- **DMI Link ASPM Control [L0sL1]**

Enable or disable the control of Active State Power Management on SA side of the DMI Link.

- **DMI Extended Synch Control [Disabled]**

Enable DMI Extended Synchronization.

- **DMI Gen 2 [Enabled]**

Enable or disable DMI Gen 2

4.5.1.7 NB PCIe Configuration

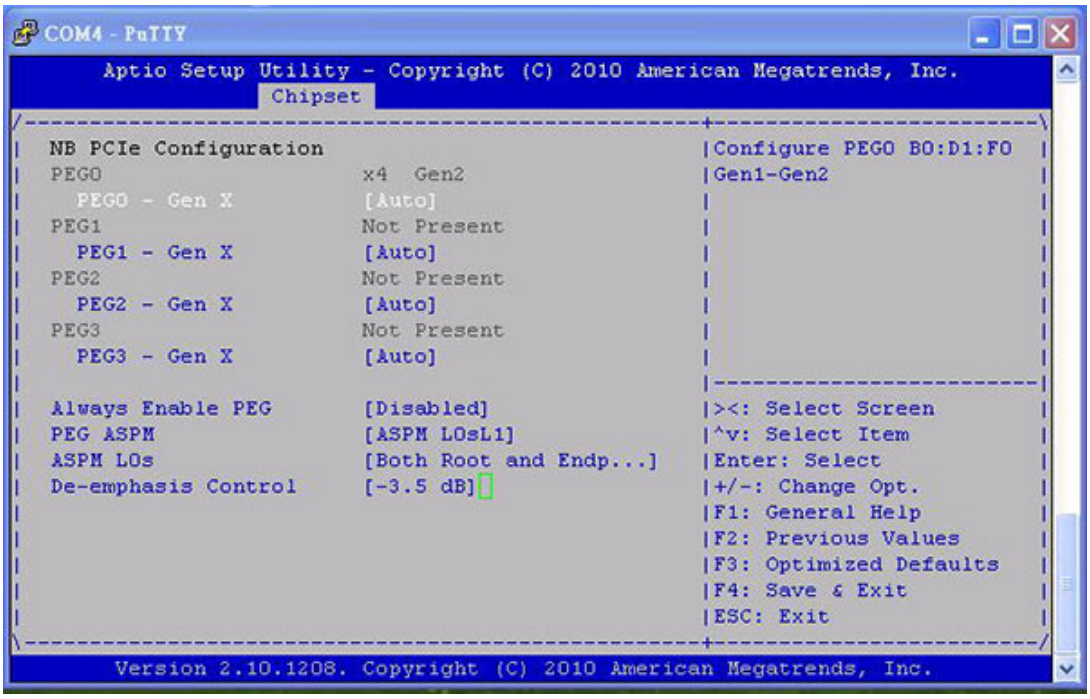


Figure 4.21 NB PCI Express configuration menu

- **PEG0- Gen X**

Configure PEG0 B0:D1:F0 Gen1-Gen2

- **PEG1 - Gen X**

Configure PEG1 B0:D1:F1 Gen1-Gen2

- **PEG2 - Gen X**

Configure PEG2 B0:D1:F2 Gen1-Gen2

4.5.1.8 Memory Configuration

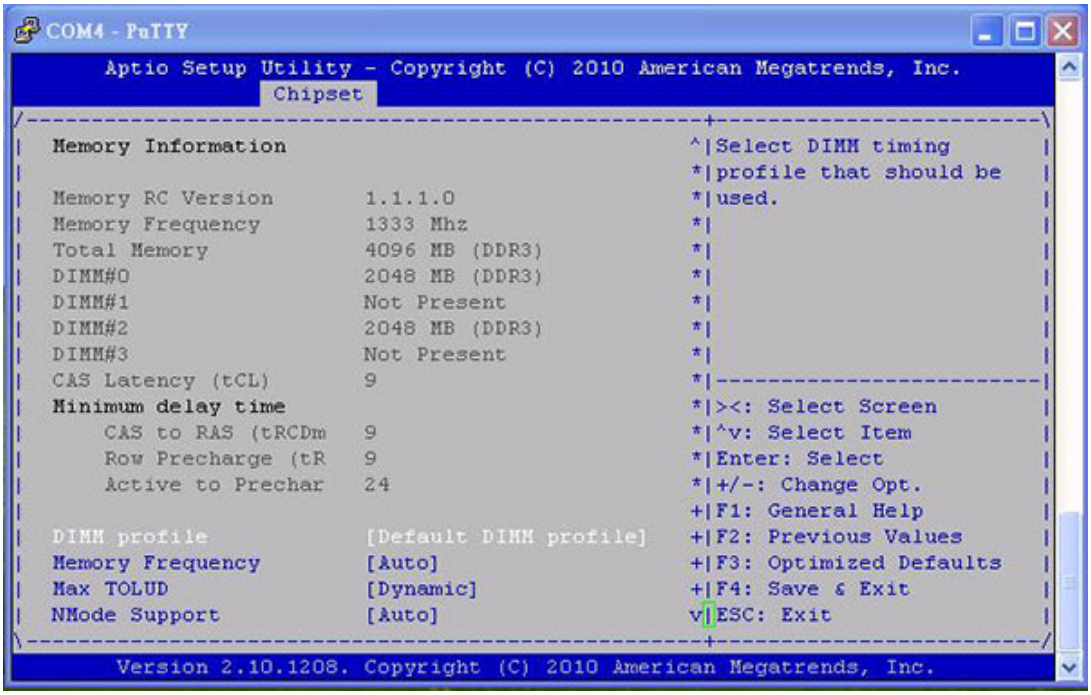


Figure 4.22 System memory configuration menu

- **DIMM profile [Default DIMM Profile]**

Select DIMM timing profile that should be used.

- **Memory Frequency [Auto]**

Maximum Memory Frequency Selections in Mhz.

- **Max TOLUD [Dynamic]**

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller

- **NMode Support [Auto]**

NMode Support Option.

4.5.2 PCH - IO Configuration

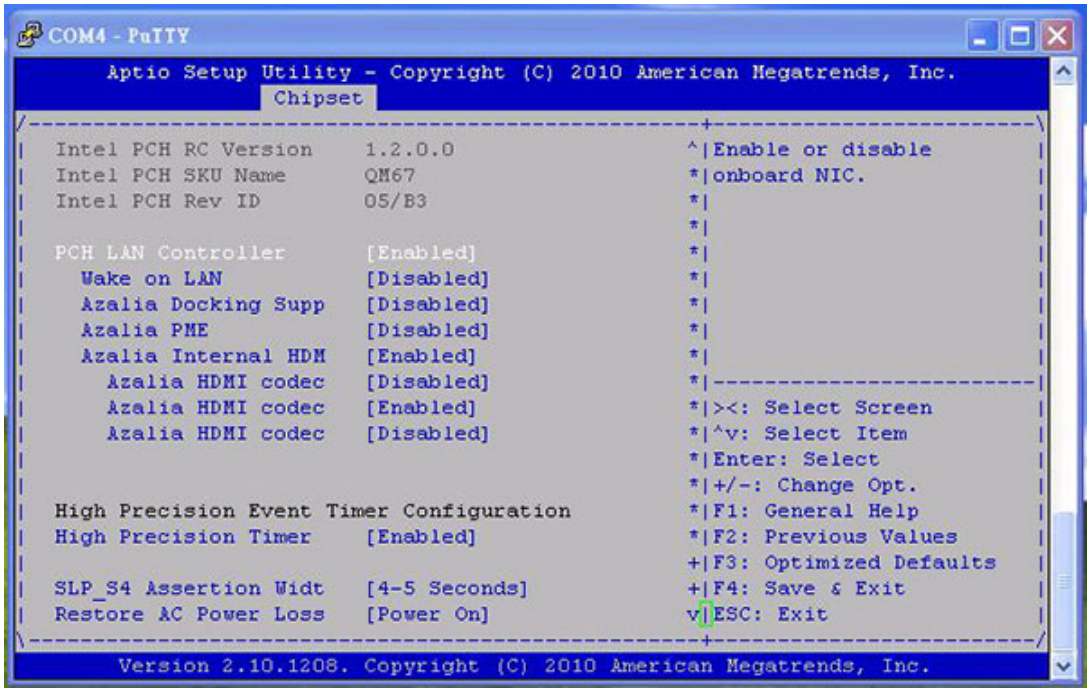


Figure 4.23 Intel PCH configuration menu

4.5.2.1 PCH LAN Controller [Enabled]

Enable/Disable LAN1 Controller

4.5.2.2 Wake on LAN1 from S5 [Disabled]

Disabled/Enabled Wake on Lan1 from S5

4.5.2.3 Azalia internal HDMI codec [Enabled]

Enable or Disable Azalia internal HDMI codec

4.5.2.4 Azalia Docking Supp [Enabled]

Enable or disable Azalia Docking Support of Audio Controller

4.5.2.5 Azalia PME [Disabled]

Enable or disable Power Management Capability of Audio Controller.

4.5.2.6 High Precision Timer [Enabled]

Enable or Disable the High Precision Timer

4.5.2.7 SLP_S4# Assertion Width [4~5 Seconds]

This item set the minimum assertion width of the SLP-S4# signal to guarantee the DRAM has been safely power-cycled

4.5.2.8 Restore AC Power Loss [Power On]

Select AC power state when power is re-applied after a power failure.

4.6 Boot Configuration

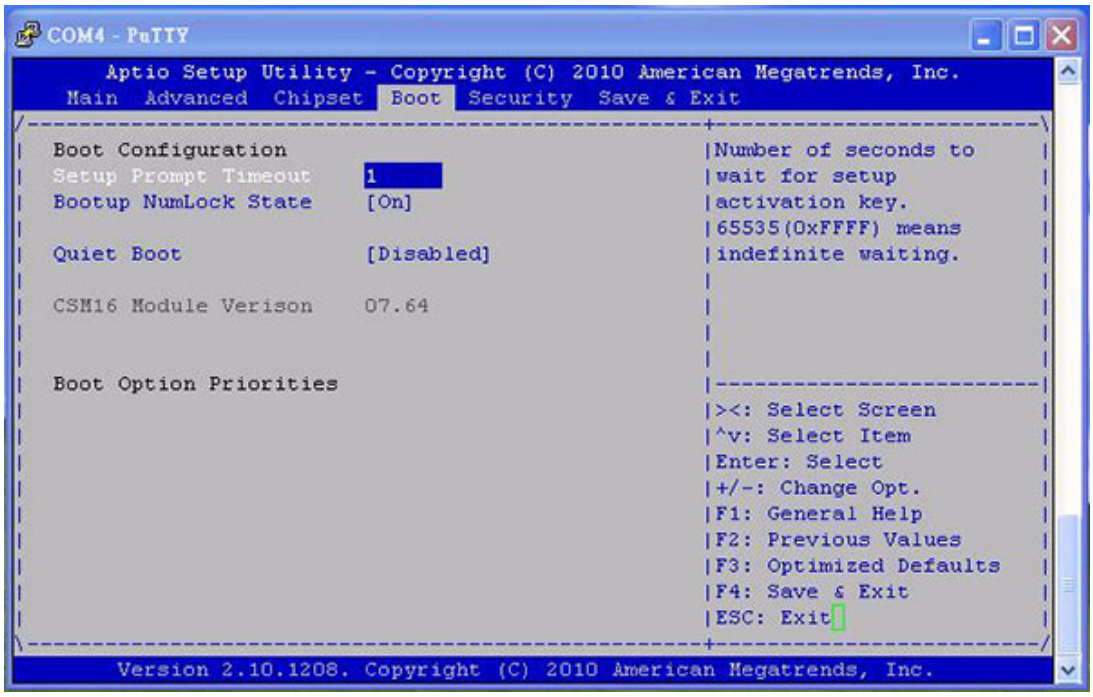


Figure 4.24 Boot configuration menu

4.6.1 Setup Prompt Timeout [1]

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting

4.6.2 Boot up NumLock State [On]

Select the keyboard NumLock state

4.6.3 Quick Boot [Disabled]

4.6.4 CSM16 Module Version [07.64]

Display CSM16 Module Version.

4.6.5 Boot option priorities [Built-in EFI Shell]

4.7 Security

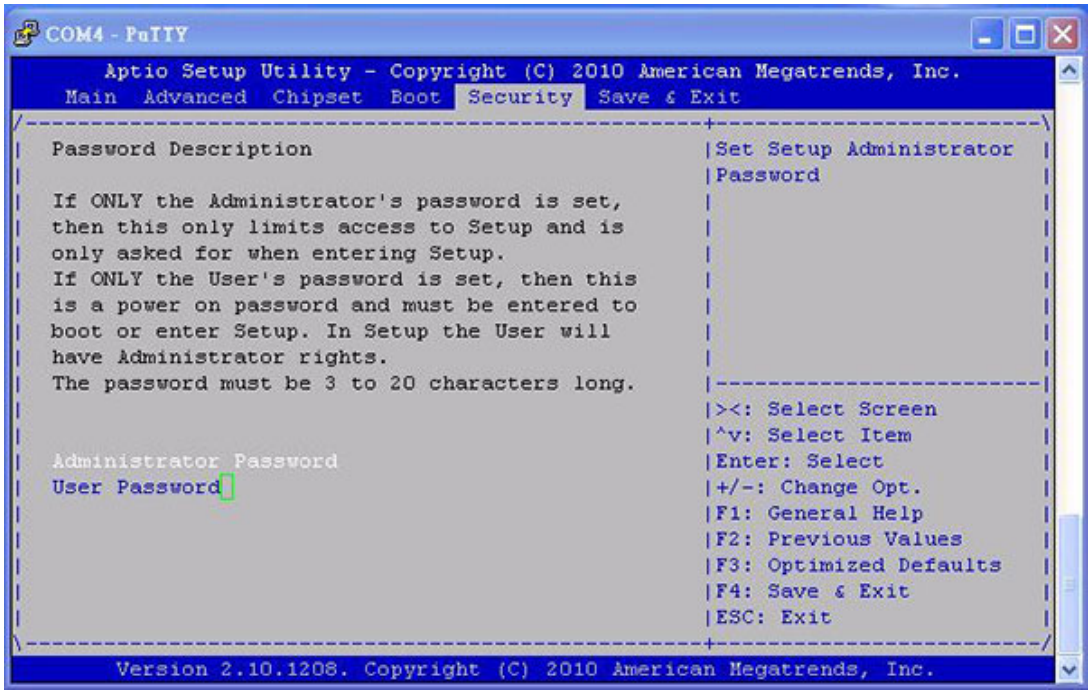


Figure 4.25 Security setup menu

4.7.1 Administrator Password

Set setup Administrator Password

4.7.2 User Password

Set User Password

4.8 Save & Exit

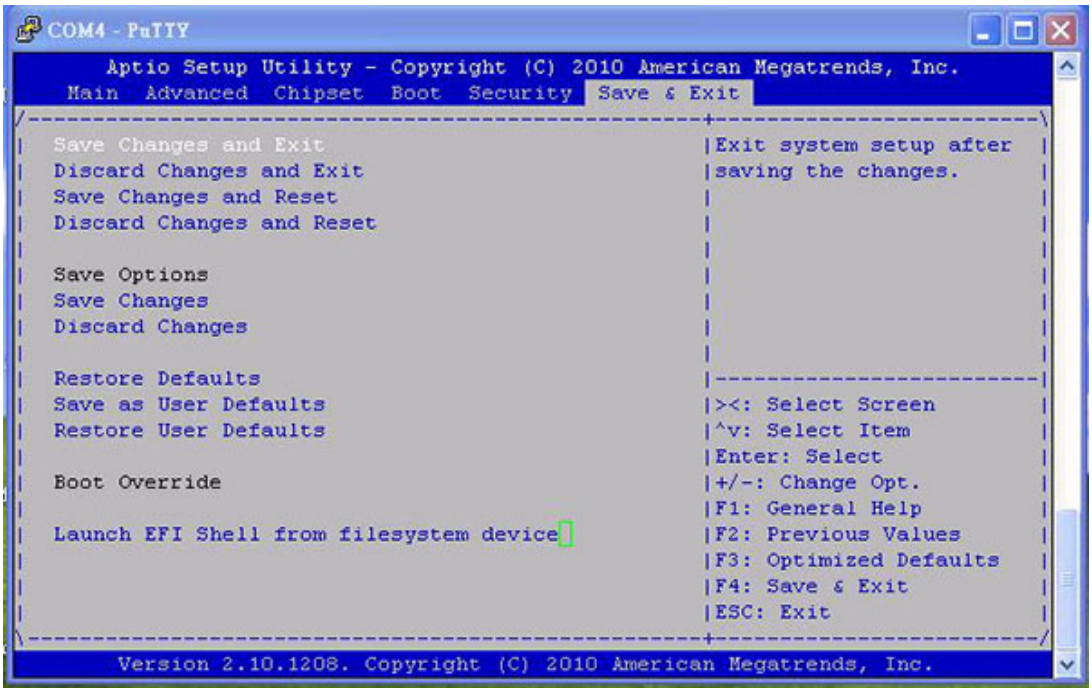


Figure 4.26 Save and Exit menu

4.8.1 Save changes and Exit

Exit system setup after saving the changes.

4.8.2 Discard changes and Exit

Exit system setup without saving the changes.

4.8.3 Save changes and Reset

Reset the system after saving the changes.

4.8.4 Discard changes and Reset

Reset the system without saving the changes.

4.8.5 Save changes

Save changes done so for to any of the setup option.

4.8.6 Discard changes

Discard changes done so for to any of the setup option.

4.8.7 Restore Defaults

Restore/Load default values for all the setup option.

4.8.8 Save as User Defaults

Save the changes done so far as User Defaults.

4.8.9 Restore User Defaults

Restore the user defaults to all the setup options

Chapter 5

MMC Firmware Operation

This chapter describes the MMC firmware features.

5.1 Module Management

The term "Module Management Controller" (MMC) describes an IPMI Baseboard Management Controller (BMC) located on a PICMG compliant AMC module. The MMC is the essential part of the MIC-5603 AMC module. It is implemented on NXP's ARM Cortex-M3 LPC1768 controller and acts as standard IPMI management controller with additional AMC functionality extensions. Main tasks are the module healthy (monitoring voltage and temperature sensors), hot swap state management participation, AMC information data storage and providing several IPMI communication interfaces.

5.2 IPMI Interfaces

The MIC-5603 provides three main IPMI messaging interfaces to connect to the modules MMC. These are the local IPMB bus (IPMB-L) for basic communication with the Carrier Manager, the LAN side band interface (RMCP/RMCP+) and the on-board payload interface to x86 (KCS).

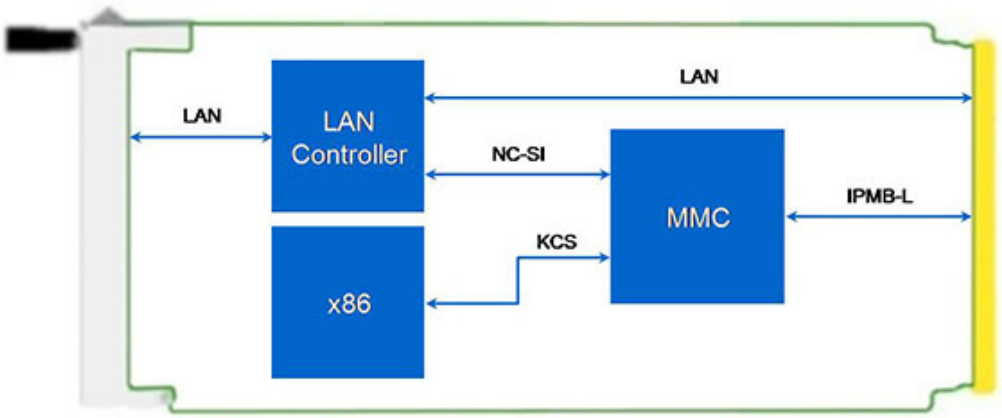


Figure 5.1 IPMI interfaces

5.2.1 IPMB-L

Basic IPMI connection of an AMC MMC is the I2C based, serial IPMB-L interface routed to the AMC edge-connector. Once plugged in an AMC carrier bay and supplied with management power, the MMC discovers the slot connector Geographic Address (GA). The GA is used to assign a unique IPMB address according to the AMC site number. With this IPMB-L address, the MMC is able to communicate with the connected AMC Carrier Manager. The main benefit of the IPMB-L interface is the independence from payload state, means it can be used at any time.

The open source IPMItool can be used to access the MMC via IPMB-L. Access to the local MMC to CM connection can only be achieved with help of Carrier Manager/ Shelf Manager interfaces. IPMItool supports "bridge" commands to bypass the Carrier and Shelf Managers in xTCA environments. Below example shows a double-bridged access to IPMB-L:

```
ipmitool -I lan -H <ShMC-IP-Address> -A <Auth-type> -T
<CM-IPMB-Address> (-B 0) -t <MMC-IPMB-Address> -b 7 <Command>
```

Command Line Syntax:

-I lan	Specifies that Ethernet is used as Shelf Manager interface
-H <ShMC-IP-Address>	IP address assigned to the Shelf Manager
-A <Auth-type>	Authentication type (depending on supported types by the Shelf Manager), default: NONE
-T <CM-IPMB-Address>	Remote transit address (IPMB-0 address of Carrier Manager) to which requests should be bridged by the Shelf Manager
-B 0	Remote transit channel (0 = IPMB-0, default interface, parameter can be skipped)
-t <MMC-IPMB-Address>	Remote target address (MMC IPMB-L address) to which requests should be bridged by the Carrier Manager
-b 7	Remote target channel (7 = IPMB-L)

5.2.2 KCS

The Keyboard Controller Style (KCS) protocol is used as IPMI system interface connection to the x86 part on MIC-5603. It is based on the Low Pin Count (LPC) bus. And it is used as the local MMC interface to BIOS and the Operating System (OS) on the Processor AMC. KCS is a fast IPMI interface compared to IPMB, but requires active payload.

IPMI driver support is needed to be able to use the IPMItool from OS level via the KCS MMC interface (refer to Appendix B - Driver and Tools). With working IPMI driver, the MMC can be accessed easily from OS via KCS. No interface parameters are needed at all, to use the local onboard IPMI connection:

```
ipmitool <Command>
```

5.2.3 LAN

The IPMI LAN Interface on MIC-5603 is accomplished by using a shared LAN Controller together with the x86 system. In addition to systems PCI-Express link, a LAN controller side-band interface (Network Controller Sideband Interface, short NC-SI) is connected to the MMC. This NC-SI channel is used by the MMC to receive and transmit IPMI management traffic from and to network with help of the LAN controller.

IPMI over LAN (IOL) uses the Remote Management Control Protocol (RMCP, specified in IPMI v1.5) in request-response manner for IPMI communication. IPMI v1.5 LAN messages are encapsulated in RMCP packets, while IPMI v2.0 specification added an enhanced protocol (RMCP+) for transferring IPMI messages and other types of payloads. RMCP+ uses RMCP overall packet format, but defines extensions, such as encryption and the ability to carry additional traffic types (e.g. serial data) in addition to IPMI messages (refer to Chapter 5.12 - Serial over LAN).

Three of MIC-5603's Ethernet interfaces can be used for IPMI over LAN:

- Both AMC fabric interfaces: AMC Port 0 and 1
- The front panel LAN2 RJ-45 connector

Note! *The LAN controller used for IPMI communication is connected to the payload power domain. Thus, the payload needs to be powered, to be able to use IPMI over LAN!*

Following IPMItool parameters are needed to connect to the MMC vial LAN:

```
ipmitool -I lan -H <IP-Address> -U <User> -P <Password> <Command>
```

Command Line Syntax:

-I lan	Specifies Ethernet interface
-H <IP-Address>	IP address assigned to the MMC
-U <User>	User account, default "administrator"
-P <Password>	Password used with specified user account (default password for user "administrator" is "advantech")

5.3 Sensors

Monitoring board voltages and temperatures in one of the main tasks of the MMC populated on the MIC-5603 Processor AMC. All important voltages and temperatures are connected to the MMC sensor part.

Moreover, the MMC Management Subsystem also registers below logical sensors:

- PICMG Hot Swap sensor
- BMC Watchdog sensor
- FW Progress sensor
- Version change sensor
- Advantech OEM Sensor: Integrity Sensor

5.3.1 Sensor list

All sensors available on the MIC-5603 Processor AMC are listed in the table below (inclusive FRU Device Locator record):

Table 5.1: Sensor list

No.	Sensor ID	Sensor Type (Event/Reading Type)	Description
0	MIC-5603		IPMI FRU Device Locator
1	HOTSWAP	Hot Swap (Discrete)	Module Hot Swap sensor
2	MP-VOL	Voltage (Threshold)	AMC Management Power +3.3V
3	V12-VOL	Voltage (Threshold)	AMC Payload Power +12V
4	V5_0-VOL	Voltage (Threshold)	AMC Board +5.0V voltage
5	V0_75-VOL	Voltage (Threshold)	AMC Board DDR3 VTT voltage
6	V1_8-VOL	Voltage (Threshold)	AMC Board +1.8V voltage
7	V1_5-VOL	Voltage (Threshold)	AMC Board +1.5V voltage
8	V1_0-VOL	Voltage (Threshold)	AMC Board +1.0V voltage
9	V0_85-VOL	Voltage (Threshold)	AMC CPU +0.85V voltage
10	V1_05-VOL	Voltage (Threshold)	AMC Board +1.05V voltage
11	V3_3-VOL	Voltage (Threshold)	AMC Board +3.3V voltage
12	VCC-RTC-VOL	Voltage (Threshold)	AMC RTC supply voltage
13	REAR-AMC-TMP	Temperature (Threshold)	AMC Board temperature close to AMC Connector
14	OUTLET-TMP	Temperature (Threshold)	AMC Board Outlet temperature
15	CPU-TMP	Temperature (Threshold)	CPU PECI temperature
16	PCH-TMP	Temperature (Threshold)	PCH temperature
17	INTEGRITY	OEM	Advantech Integrity sensor
18	BMC_WATCHDOG	Watchdog 2 (Discrete)	IPMI BMC Watchdog sensor
19	FW_PROGRESS	System Firmware Progress (Discrete)	IPMI FW Progress sensor
20	VERSION_CHANGE	Version Change (Discrete)	IPMI Version Change sensor

5.3.2 Threshold based sensors

According to the IPMI specification, sensor event thresholds are classified as Non-critical, Critical, or Non-recoverable. When different thresholds are reached, different actions may be executed by carrier or shelf manager (e.g. fan speed adjustment for temperature sensor events).

Below table list, the six sensor thresholds specified for threshold based sensors in the following subchapters.

Table 5.2: Threshold descriptions

Threshold	Description
UNR	Upper Non-recoverable
UC	Upper Critical
UNC	Upper Non-critical
LNC	Lower Non-critical
LC	Lower Critical
LNR	Lower Non-recoverable

5.3.2.1 Voltage sensors

All listed voltages listed below are monitored by the MMC and readable via IPMI.

Table 5.3: Voltage sensor list

Sensor Name	Nominal Value	LNR	LCR	LNC	UNC	UCR	UNR
MP-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
V12-VOL	12.0	9.90	10.2	10.8	13.2	13.8	14.1
V5_0-VOL	5.00	4.40	4.50	4.75	5.25	5.50	5.60
V0_75-VOL	0.75	0.60	0.675	0.71	0.79	0.825	0.90
V1_8-VOL	1.8	1.58	1.62	1.71	1.89	1.98	2.02
V1_5-VOL	1.5	1.26	1.35	1.425	1.575	1.65	1.74
V1_0-VOL	1.0	0.88	0.90	0.93	1.07	1.10	1.12
V0_85-VOL	0.85	0.71	0.765	0.80	0.90	0.935	0.99
V1_05-VOL	1.05	0.88	0.945	0.99	1.11	1.155	1.22
V3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
VCC-RTC-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70

5.3.2.2 Temperature sensors

The MIC-5603 Processor AMC supports some temperature sensors, either via board populated IC's (e.g. TMP75) or readings from CPU/Chipset interfaces (PECI/ SMBus).

Table 5.4: Temperature sensor list

Sensor Name	Value	LNR	LCR	LNC	UNC	UCR	UNR
REAR-AMC-TMP	25	-15	-10	-5	65	75	85
OUTLET-TMP	25	-15	-10	-5	65	75	85
CPU-TMP	40	-15	-10	-5	80	90	105
PCH-TMP	40	-15	-10	-5	85	95	112

Note! *The PCH temperature sensors can only measure values greater/equal to 44 degrees C.*

5.3.3 Discrete sensors

5.3.3.1 MMC device locator

Each MMC provides a PICMG compliant FRU device locator for the subsystem. This record is used to hold location and type information of the MMC.

5.3.3.2 FRU hotswap sensor

The MMC contains a PICMG compliant Hot Swap sensor inside it's sensor data repository.

5.3.3.3 BMC watchdog sensor

The BMC Watchdog sensor is supported according to the Watchdog 2 sensor type listed in the IPMI specification.

5.3.3.4 FW progress sensor

The MMC SDR contains a FW Progress sensor in order to support logging of the OS boot process.The MMC supports adding and forwarding of SEL entries from the BIOS/OS system firmware progress events by sending 'Add sel entry' commands with the matching sensor type to the MMC through the KCS interface.

5.3.3.5 Version change sensor

A Version Change sensor is supported according to the IPMI specification.

5.3.4 Example sensor data

Below example shows, a MIC-5603 sensor-reading list printed with the open source IPMItool:

```
[root@localhost ~]# ipmitool sdr elist all
MIC-5603         | 00h | ok  | 193.98 | Dynamic MC @ 20h
HOTSWAP          | 01h | ok  | 193.98 | Module Handle Closed
MP-VOL           | 02h | ok  | 193.98 | 3.24 Volts
V12-VOL          | 03h | ok  | 193.98 | 12.22 Volts
V5_0-VOL         | 04h | ok  | 193.98 | 4.98 Volts
V0_75-VOL        | 05h | ok  | 193.98 | 0.74 Volts
V1_8-VOL         | 06h | ok  | 193.98 | 1.79 Volts
V1_5-VOL         | 07h | ok  | 193.98 | 1.50 Volts
V1_0-VOL         | 08h | ok  | 193.98 | 1.01 Volts
V0_85-VOL        | 09h | ok  | 193.98 | 0.87 Volts
V1_05-VOL        | 0Ah | ok  | 193.98 | 1.03 Volts
V3_3-VOL         | 0Bh | ok  | 193.98 | 3.26 Volts
VCC-RTC-VOL      | 0Ch | ok  | 193.98 | 3.22 Volts
REAR-AMC-TMP     | 0Dh | ok  | 193.98 | 30 degrees C
OUTLET-TMP       | 0Eh | ok  | 193.98 | 32 degrees C
CPU-TMP          | 0Fh | ok  | 193.98 | 45 degrees C
PCH-TMP          | 10h | ok  | 193.98 | 44 degrees C
INTEGRITY        | 11h | ns  | 193.98 | Disabled
BMC_WATCHDOG     | 12h | ok  | 193.98 |
FW_PROGRESS      | 13h | ok  | 193.98 |
VERSION_CHANGE   | 14h | ok  | 193.98 |
```

5.3.5 Integrity sensor

5.3.5.1 Overview

The Advantech Integrity Sensor is an OEM sensor according to the SDR (Sensor Data Record) definitions in the IPMI specification. Its main purpose is to monitor internal firmware states and report events to the operator that would otherwise go unnoticed (hence "integrity sensor").

Examples for those events are checksum errors, firmware update success/failure, firmware rollbacks.

5.3.5.2 Sensor characteristics

The Integrity sensor does not support sensor reading, but generates event messages only. These events are stored in the local System Event Log (SEL) and sent to the default event receiver.

The event message contains three bytes of event data. The first byte defines how the event is supposed to be treated: the value of 0xA0 defines that event data 2 and 3 contain OEM data (please verify the IPMI specification for details on OEM sensors).

Event data 2 is used to identify which component the event relates to. This can either be a HPM.1 component, a logical component/feature on the board (for example FRU, RTC) or simply a board specific event.

Event data 3 [7..3] identifies the action or a subcomponent. For example: If the component in byte 2 was a HPM.1 component, it might report if this was an update, a rollback, or boot failure. If the component in byte 2 was "FRU", it might indicate the subcomponent = area within the FRU that the event relates to.

Event data 3 [2..0] holds the result code. For the HPM.1 example above, it might report that an update or rollback either succeeded or failed. For the FRU example, it might indicate a checksum error.

5.3.5.3 Event data byte definition

The following list provides the exact Integrity sensor event bytes definition.

Table 5.5: Integrity sensor event definitions

Data Byte	[Bit]	Description	Value	Event Data
1	[7:0]	IPMI Header	0xA0	Event data 2 & event data 3 used as OEM data
2	[7:0]	Component	0x00 – 0x07 0x08 – 0xFE 0xFF	HPM.1 component (FW, FPGA, BIOS…) Logical component (FRU, RTC…) Board specific event
3	[7:3]	Action / Subcomponent	b00000 b00001 b00010 b00011 b00100 b00101 b00110 b00111 b01000 b01001 b01010 b01011 b01100 b01101 b01110 b01111… …b11111	Update Recovery/Rollback Manual Rollback Automatic Rollback Activation Flash 0 Boot Flash 1 Boot Common Header Internal Area Chassis Info Area Board Info Area Product Info Area Multi Record Area Time synchronization Graceful Shutdown Not defined yet… Not defined yet
3	[2:0]	Result	b000 b001 b010 b011 b100 b101 b110 b111	Successful Failed Aborted Checksum Error Timeout Initiated Finished Unspecified Error

5.3.5.4 Event data translation

The structured definition allows simple translation of each Integrity Sensor event message. Below is an example Integrity Sensor SEL event (0x0A0100). The three event data bytes could be translated in following manner:

Data 1: 0x0A: Header

Data 2: 0x01: logical Component (MMC FW)

Data 3: 0x00: b 0 0 0 0 00 0 0

Update Successful

The example Integrity Sensor event reports a successful MMC Firmware update.

5.3.5.5 Event data table

All event data combinations supported by the MMC Integrity Sensor can be found in following list.

Table 5.6: Integrity sensor's event data table

Component	Action / Subcomponent	Result	Byte 1	Byte2
MMC FW	Update	Successful	0x01	0x00
	Update	Timeout	0x01	0x04
	Update	Aborted	0x01	0x02
	Activation	Failed	0x01	0x21
	Manual Rollback	Initiated	0x01	0x15
	Automatic Rollback	Initiated	0x01	0x1D
	Rollback	Finished	0x01	0x0E
	Rollback	Failed	0x01	0x09
	Graceful Shutdown	Timeout	0x01	0x74
FPGA	Update	Successful	0x02	0x00
	Update	Timeout	0x02	0x04
	Update	Aborted	0x02	0x02
	Recovery	Finished	0x02	0x0E
BIOS	Update	Successful	0x03	0x00
	Update	Timeout	0x03	0x04
	Update	Aborted	0x03	0x02
	Flash 0 Boot	Failed	0x03	0x29
	Flash 1 Boot	Failed	0x03	0x31
NVRAM	Update	Successful	0x04	0x00
	Update	Timeout	0x04	0x04
	Update	Aborted	0x04	0x02
RTC	Time sync	Successful	0x09	0x68
	Time sync	Failed	0x09	0x69

5.3.5.6 Example event identification

The Integrity Sensor is listed as last MIC-5603 sensor (verify below IPMItool example).

```
[root@localhost ~]# ipmitool sdr elist
HOTSWAP          | 01h | ok  | 193.100 | Module Handle Closed
…
INTEGRITY        | 10h | ns  | 193.100 | Disabled
```

As mentioned before, the Integrity Sensor does not provide a sensor reading (disabled), but supports event generation at any time.

Occurred events are stored as records in the System Event Log and can be read out with following IPMItool command:

```
[root@localhost ~]# ipmitool sel elist
   1 | 04/23/2012 | 10:04:46 | Module Hot Swap #0x01    | Module Han-
dle Closed | Asserted
…
   e | 04/23/2012 | 10:13:31 | OEM | OEM Specific | Asserted
…
```

Detailed information to single system events (event data bytes) in the SEL can be displayed with IPMItool "sel get <entry>"

```
[root@localhost ~]# ipmitool sel get 0x0e
SEL Record ID          : 000e
 Record Type           : 02
 Timestamp             : 04/23/2012 10:13:31
 Generator ID          : 0074
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 10
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data            : a00100
 Description           : OEM Specific
```

The "Event Data" field reflects the three needed bytes to identify the occurred Integrity Sensor event.

5.4 FRU Information

The MMC provides IPMI defined Field Replaceable Unit (FRU) information about the AMC module. The MIC-5603 FRU data include general board information's such as product name, HW version or serial number. A total of 2 kB non-volatile storage space is reserved for the FRU data. The boards IPMI FRU information can be made accessible via all MMC interfaces and the information can be retrieved at any time.

5.4.1 PICMG FRU records

In addition to the standard IPMI FRU data areas, the AMC FRU stores AMC.0 specification defined PICMG records. These FRU records (e.g. Module Current Requirements or E-Keying information) are mandatory for the AMC module functionality.

Please note that the PICMG FRU data records are essential for any AMC module. Improper record data or wrong modifications can influence the correct activation and behavior of the AMC through the carrier manager!

5.4.2 FRU Information access commands

The FRU device IPMI commands are supported by the MMC to read and write the AMC module FRU information. Correct and board specific FRU data is programmed to each single module in factory. Please be very careful using the regular IPMI FRU write command (avoid if possible). Wrong FRU data content could destroy the AMC payload functionality!

5.4.3 Example FRU data

Below example shows a default MIC-5603 FRU data excerpt (Board and Product Info areas) using the Linux "IPMItool":

```
[root@localhost ~]# ipmitool fru
FRU Device Description : Builtin FRU Device (ID 0)
 Board Mfg Date        : Mon Jan  1 07:00:00 1996
 Board Mfg             : Advantech
 Board Product         : MIC-5603
 Board Serial          : AKA1234567
 Board Part Number     : MIC-5603
 Product Manufacturer  : Advantech
 Product Name          : MIC-5603
 Product Part Number   : MIC-5603
 Product Version       : A1 03
 Product Serial        : AKA1234567
```

5.5 E-Keying

Electronic Keying (E-Keying) has been added to the PICMG AMC.0 R2.0 Specification to remove the need for any mechanic keying. It defines the process in which a Carrier determines a matching configuration of channel and clock connections to an AMC Module. Main purpose is to prevent board damage and miss operation. Furthermore, it helps to verify the Carrier to AMC module compatibility.

The MIC-5603 FRU data includes an important PICMG AMC point-to-point connectivity record for E-Keying (refer to Chapter 5.4 - FRU Information). This record describes the AMC port connectivity (gold finger connector) and is parsed by the Carrier Manager during AMC initialization. The Carrier Manager will only enable matching interfaces (with identical AMC port protocols per channel) between Carrier and AMC Module, when the CM powers and activate the AMC module.

5.5.1 AMC connector Interfaces and E-Keying channels

The table below lists the MIC-5603 AMC gold finger connector protocols per AMC port and where the ports are connected. The last column relates the AMC ports to the used E-keying channel numbers.

Table 5.7: AMC port vs. E-Keying channel

AMC Port	Region	Protocol	Connected Resource	E-Keying channel No.
0	Common Options	GbE 1000Base-BX	LAN Controller	0
1		GbE 1000Base-BX	LAN Controller	1
2		SATA	PCH	2
3		SATA	PCH	3
4	Fat Pipes	PCIE	PCH	4
5		PCIE	PCH	
6		PCIE	PCH	
7		PCIE	PCH	
8		FI1 (LVDS)	AMM (optional)	
9		FI1 (LVDS)	AMM (optional)	
10		FI1 (LVDS)	AMM (optional)	
11		FI1 (LVDS)	AMM (optional)	
12	Extended Options	LVDS	FPGA	
13		LVDS	FPGA	
14		LVDS	FPGA	
15		UART	FPGA (UART MUX)	5
17	Extended Options	FI2 (LVDS)	AMM (optional)	
18		FI2 (LVDS)	AMM (optional)	
19		FI2 (LVDS)	AMM (optional)	
20		FI2 (LVDS)	AMM (optional)	
TCLKA	Clocks	Telecom Clock	FPGA	
TCLKB		Telecom Clock	FPGA	
TCLKC (16)		Telecom Clock	FPGA	
TCLKD (16)		Telecom Clock	FPGA	
FCLKA		Fabric Clock	PCH (PCIe ref. clock)	Clock E-Keying

5.5.2 E-keying channel states

Users can read out the AMC E-Keying channel states via IPMI (Get AMC Port State command). Below printout shows MIC-5603 channels with the open IPMItool:

```
[root@localhost ~]# ipmitool picmg amcportstate getall
   Link device :          AMC
   Link Grouping ID:      0x00
   Link Type Extension:   1000BASE-BX (SerDES Gigabit)
   Link Type:             ETHERNET
   Link Designator:
      Channel Number:     0x00
      Port Flag:          0x01
   STATE:                 enabled

   Link device :          AMC
   Link Grouping ID:      0x00
   Link Type Extension:   1000BASE-BX (SerDES Gigabit)
   Link Type:             ETHERNET
   Link Designator:
      Channel Number:     0x01
      Port Flag:          0x01
   STATE:                 disabled

   Link device :          AMC
   Link Grouping ID:      0x00
   Link Type Extension:   Serial ATA
   Link Type:             STORAGE
   Link Designator:
      Channel Number:     0x02
      Port Flag:          0x01
   STATE:                 disabled

   Link device :          AMC
```

5.5.3 Clock E-keying

The AMC.0 R2.0 Specification defines additional Clock E-Keying for the AMC Clock Interfaces. These AMC clocks are comprised of four Telecom clocks (TCLKA, TCLKB, TCLKC and TCLKD) plus one fabric clock (FCLKA).

5.5.3.1 Fabric PCI-Express clock

The MIC-5603 AMC module connects FCLKA with a PCI Express reference clock from its PCH chipset (=Root Complex). This means the PCIE reference clock is generated locally and the AMC acts as clock source to connected PCI Express Endpoints. The FRU data describes the AMC's PCIE clock details in a PICMG Clock Configuration Record (according to AMC.1 R2.0 PCI Express on AdvancedMC Specification).

To establish PCIE connections from the MIC-5603 Root Complex to PCIE Endpoints (on other AMC modules or on Carrier devices), the clock signal need to be connected to this PCIE device. This implicate that the Carrier Manager and Backplane must support clock routing in HW and SW (Clock E-Keying).

5.6 OEM commands

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI defined OEM/Group Network Function (NetFn) Codes 2Eh, 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response. Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The MIC-5603 MMC supports Advantech IPMI OEM commands listed in below table.

Table 5.8: OEM command overview

Command	LUN	NetFn	CMD
Store Configuration Settings	00h	2Eh, 2Fh	40h
Read Configuration Settings	00h	2Eh, 2Fh	41h
Read Port 80 (BIOS POST Code)	00h	2Eh, 2Fh	80h
Clear NVRAM data	00h	2Eh, 2Fh	81h
Read MAC Address	00h	2Eh, 2Fh	E2h
Load Default Configuration	00h	2Eh, 2Fh	F2h

5.6.1 IPMItool raw command

To be able to use the Advantech OEM commands with the open source IPMItool, users have to employ the "raw" command of IPMItool. Please find below command structure details of the IPMItool raw command.

General raw request:

```
ipmitool raw <netfn> <cmd> [data]
```

Response, if raw <netfn> is 2Eh (OEM/Group):

```
<IANA Enterprise Number> [data]
```

5.6.2 Configuration setting OEM commands

The Read and Store Configuration OEM commands can be used to read and change several important board settings. The following sub-chapters describe the needed command details.

5.6.3 LAN controller interface selection

The MMC firmware provides an OEM IPMI command to allow users to switch the MMC connected NC-SI interface between one front panel LAN IO RJ-45 connector and the AMC connector Base interface (AMC Ports 0 & 1). These commands can be used to read out the actual selected IPMI-over-LAN / Serial-over-LAN interface and to change the selection.

LAN controller interface selection settings:

00h: Front panel LAN IO

01h: AMC connector LAN BI (default)

Read LAN Interface selection:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x00
```

Response:

```
39 28 00 <setting>
```

Change LAN Interface selection:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x00 <setting>
```

Response:

```
39 28 00
```

5.6.3.1 LAN controller channel selection and priority

In addition to the selected LAN controller interface, users may need to configure each single LAN controller channel (port) as dedicated NC-SI interface to the MMC. Additional OEM commands for the configuration of the NC-SI LAN controller channel selection and priority are provided to allow a flexible configuration.

LAN channel selection priority setting list:

0 = The first channel that links up, gets the NC-SI connection to the MMC.

1 = Channel 1 is the preferred port if it is up, otherwise use channel 2 if it is up.

2 = Channel 2 is the preferred port if it is up, otherwise use channel 1 if it is up.

3 = Channel 1 is the only allowed port, always use it, never change to channel 2.

4 = Channel 2 is the only allowed port, always use it, never change to channel 1.

The NC-SI LAN controller channel setting will be stored permanently (non-volatile EEPROM). The default value is 0.

Read LAN channel selection priority:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x01
```

Response:

```
39 28 00 <setting>
```

Change LAN channel selection priority:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x01 <setting>
```

Response:

```
39 28 00
```

5.6.4 FPGA COM port UART MUX

MIC-5603 implements several serial interfaces, which can be configured in some ways. This is done inside the FPGA with the help of an UART MUX (refer to Chapter 5.6 - UART and UART Multiplexer). The MMC provides OEM commands to configure these UARTs via IPMI. Following COM1 / COM2 port settings are available (Caution: Verify note below about the UART dependency!):

COM interfaces:

Table 5.9: OEM interfaces

Port	Interface
0x00	COM1
0x01	COM2

COM1 MUX:

Table 5.10: COM1 UART MUX settings

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL)
0x02	Front panel Micro-USB (default)
0x03	AMC connector port 15

COM2 MUX:

Table 5.11: COM2 UART MUX settings

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL) (default)
0x02	Front panel Micro-USB
0x03	AMC connector port 15

Note!

The COM1 UART is the main interface with higher priority! There is an important dependency between COM1 and COM2 UARTs, users should know and aware of:

The COM2 MUX can ONLY be used, if the COM1 MUX is set to SOL (0x01)! If the COM1 MUX has any other settings than SOL, COM2 is permanently fixed to SOL and the COM2 MUX OEM command setting is ignored.

Read COM port UART MUX setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x08 <port>
```

Response:

```
39 28 00 <setting>
```

Change COM port UART MUX setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x08 <port> <setting>
```

Response:

```
39 28 00
```

5.6.5 Read Port 80 (BIOS POST Code) OEM command

To be able to read out the actual BIOS boot state via IPMI, the MMC provides an Advantech OEM command to reflect the actual BIOS POST (Port 80) code.

```
ipmitool raw 0x2e 0x80 0x39 0x28 0x00
```

Response:

```
39 28 00 <POST Code>
```

5.6.6 Clear NVRAM data OEM command

The MMC implements an OEM command to be able to clear the BIOS settings in NVRAM from SW side without the need of extracting the AMC module and performing any jumper plug and re-plug . This command can be used to load the default BIOS settings.

```
ipmitool raw 0x2e 0x81 0x39 0x28 0x00
```

Response:

```
39 29 00
```

5.6.7 MAC address mirroring OEM command

The AMC module LAN Controller MAC addresses will also be stored in the FRU EEPROM, making the MAC's available even if the payload is not powered. This helps to relate the MAC address and the physical/logical AMC module location.

The MIC-5603 board is equipped with 5 MAC addresses in total. Please find below the used order in the FRU EEPROM Internal Use Area:

Table 5.12: MAC address mapping table

MAC Number	LAN Interface
0	AMC port 0 (BI 0) - 82580 MAC 0
1	AMC port 1 (BI 1) - 82580 MAC 1
2	FP LAN 1 (IO 0) - 82579 MAC
3	FP LAN 2 (IO 1) - 82580 MAC 3
4	MMC MAC

Read MAC Address OEM command:

```
ipmitool raw 0x2e 0xe2 0x39 0x28 0x00 <MAC Number>
```

Response:

```
39 28 00 <MAC-Address>
```

5.6.8 Load default configuration OEM command

Several configurations settings are provided by the MMC. To reset all of them to their default values, a single OEM command is available to perform this with only one IPMI command.

```
ipmitool raw 0x2e 0xF2 0x39 0x28 0x00
```

Response:

```
39 28 00
```

5.7 UART and UART-Multiplexer

The x86 subsystem of MIC-5603 has access to 2 UARTs implemented insight the FPGA. These UARTs are 16550 compatible and mapped to the standard IO address ranges 0x2F8-0x2FF and 0x3F8-0x3FF. This chapter gives an overview of the implementation details and the resulting use cases.

5.7.1 UART block diagram

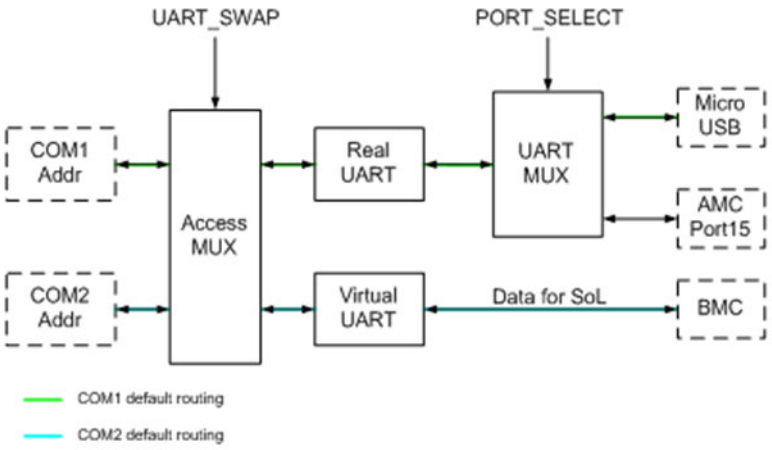


Figure 5.2 UART functional block overview

5.7.2 UART implementation

The MIC-5603 FPGA implements two different kinds of UART's. The "real" UART is a 16550 compatible UART with complete RS232 serial interface support. An UART multiplexer (MUX) is used to connect the main serial interfaces (front panel microUSB connector and AMC connector Port15) to the "real" UART.

The "virtual" UART is only used for Serial-over-LAN (SOL) and not fully 16550 compatible. Means it only has a 16550 compatible register interface for x86, but a reduced FIFO interface for the MMC access only.

An access multiplexer is used to avoid that SOL and the serial interface is fixed to a specific COM port (IO address range). It allows to swap the COM port functionality with help of IPMI commands (verify Chapter 5.6 - OEM Commands for details).

5.7.3 Limitation

Because there's only one "real" UART to x86 available, users can only connect to one physical serial interface at the same time.

Below table gives a quick overview about the supported UART MUX combinations:

Table 5.13: COM port usage combinations

Serial Interface	COM1	COM2
Supported Function	MicroUSB	SOL
	AMC Port15	SOL
	SOL	MicroUSB
	SOL	AMC Port15

Caution! *COM1 is the serial interface with higher priority! COM2 can ONLY be routed to the "real" UART serial interfaces (front panel microUSB and AMC Port15), if COM1 is set to SOL. If COM1 has access to the "real" UART (any other setting than SOL), COM2 is permanently fixed to SOL.*

5.8 Hot swap/ACPI

Hot swapping the MIC-5603 means to plug and remove the AMC Module from a system (AMC Carrier) while the power is still on and the system is still operating. If the MIC-5603 will be removed from a powered system, the MMC need to interact with the payload to safely shut down the payloads operating system (OS). This chapter describes the supported ACPI mechanism to achieve this on the Processor AMC.

5.8.1 ACPI featured graceful shutdown

Note! *The payload OS used with MIC-5603 need to support ACPI to benefit from the module graceful shutdown feature!*

If there's an AMC shutdown request (e.g. hot swap front panel handle "open" event or IPMI FRU Deactivate command), the MMC will initiate the OS shutdown with help of the ACPI Power Button signal routed to the x86 system. The ACPI daemon running on the payload OS start to shutdown the system once it detects the ACPI event. At the time the OS shutdown is finished, the payload will indicate the achieved sleep state to the MMC. Last step for the MMC is to forward this information to the Carrier Manager ("quiesced" hot swap event), who will power off the AMC payload subsequently.

5.8.2 Graceful shutdown timeout

A Graceful Shutdown timeout is implemented for payload operating systems without ACPI support or in case the shutdown process is not finished (no active x86 sleep state).

If the MMC does not get the activated sleep state signal within the timeout value of 60 seconds, it will report the "quiesced" hot swap event to the Carrier Manager anyway.

5.9 BIOS failover/redundancy

5.9.1 Overview

The MIC-5603 Processor AMC supports BIOS redundancy handled by the MMC. Two BIOS SPI flashes are populated on the AMC module and BIOS redundancy is responsible to manage the flash failover, if the actual selected BIOS fail to boot.

An example of use is a BIOS update over HPM.1 (verify chapter <x.x.x - HPM.1 Updates>). If the BIOS HPM.1 update was done and the new BIOS version does not boot, the MMC will switch back to the previous used BIOS version.

5.9.2 BIOS boot watchdog

An IPMI compliant BMC Watchdog (verify Chapter 5.10 - Support watchdogs) implemented in the MMC, is used to monitor the BIOS boot progress. The MMC will initiate the BIOS SPI flash swap in case of a BMC Watchdog bite during BIOS execution (e.g. selected BIOS corrupt).

5.9.3 MMC part

The BMC Watchdog is programmed by MMC with a predefined timeout and started when payload power for the x86 subsystem is turned on (payload reset detected). The watchdog timeout action is configured to do a "hardware reset" and the timer use is set to BIOS.

If a BMC Watchdog timeout occurs with this configuration, the BIOS flash failover is initiated by MMC. It's followed by a x86 system reset and the watchdog timer restart.

BMC Watchdog timeout events are logged in the MMC System Event Log (SEL) and BIOS failover details are stored in SEL via the Advantech Integrity Sensor (verify Chapter 5.3.5 - Integrity sensor).

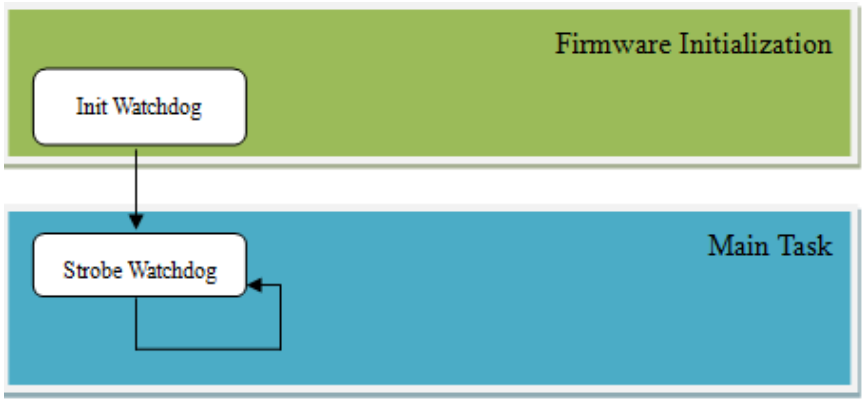
5.9.4 BIOS participation

Active involvement of BIOS in the redundancy mechanism is limited, but necessary. The BMC Watchdog status is changed by BIOS at the end of its execution (transition to OS) and if users enter the BIOS setup menu.

5.10 Supported watchdogs

5.10.1 Firmware watchdog

The FW Watchdog monitors the MMC functionality. If the MMC hangs and stops execution, the watchdog will not be restarted. The watchdog "bites" after a timeout and resets the MMC to recover the controller from current error state.



If the Watchdog is triggered, the IPMB-L is isolated from the controller. The AMC Payload is not affected and the FRUs operational state stays untouched.

5.10.2 BMC watchdog

The BMC Watchdog is full IPMI v2.0 Specification compliant. It supports the following IPMI commands:

- Reset Watchdog Timer (IPMI 2.0 Specification 27.5)
- Set Watchdog Timer (IPMI 2.0 Specification 27.6)
- Get Watchdog Timer (IPMI 2.0 Specification 27.7)

To ensure a high reliability of the MIC-5603 Payload, the BMC Watchdog is enabled by default for BIOS monitoring. The details are described in BIOS failover chapter (Chapter 5.9 - BIOS failover/redundancy).

5.11 Resets

Several different reset types are support by AMC modules. This chapter helps to clarify the used naming and the differences between the available resets.

5.11.1 Module management controller resets

The MIC-5603 MMC support two different resets types: cold and warm resets according to the IPMI specification.

5.11.1.1 MMC cold reset

The cold MMC reset causes default setting of all internal and external data/states (e.g. message buffers, interrupt settings, sensor and event configurations, E-keying port states, and FRU LED states) and power up defaults to be restored.

Following events lead to MMC cold resets:

- When the MMC is powered on, a cold MMC reset is performed.
- In case management power drops below some critical value, the MMC is cold reset. When the management power returns to its normal value, the MMC is brought out of reset.

- Another example for the cold reset scenario is if the internal watchdog timer of the MMC expires and reset the MMC.
- User can force a MMC cold reset by pressing the front panel reset button for more than five seconds.
- Finally, a cold reset can also be executed by software with help of the standard IPMI "Cold Reset" command.

5.11.1.2 MMC warm reset

The warm MMC reset is similar to cold reset, but with additional preserved data/ states (e.g. addresses, enables, and E-keying port states). On a warm reset, which can be executed by a standard IPMI command, the MMC firmware recovers its state from local memory.

5.11.2 Payload reset

In addition to the management controller reset types, the AMC module also support payload resets. The x86 system represents the payload of the MIC-5603 processor AMC module.

5.11.2.1 Payload cold reset

A payload cold reset means hardware reset to the modules payload part, similar to a power on reset. Following events cause AMC payload cold resets:

- Payload power activation after hot swap state change.
- The front panel reset button is pressed for a short period (less than five seconds).
- The mandatory PICMG "FRU Control (Cold Reset)" IPMI command is send to the MMC.
- IPMI BMC Watchdog events.
- "Control-Alt-Delete", also known as the "three-finger salute" (on a connected keyStandard operating system reset commands (e.g. Linux "reboot").

5.12 SOL setup

Serial over LAN (SOL) is an extension to IPMI over LAN (IOL) and allows to transmit serial data via LAN in addition to IPMI commands (verify Chapter 5.1 - IPMI Interfaces, LAN). It's defined in the IPMI v2.0 specification and based on the RMCP+ protocol to encapsulate serial data in network packets and exchange them via LAN.

With the help of SOL, user can connect to a virtual serial console (e.g. payload x86 system) from remote. SOL can be used on MIC-5603 for serial-based OS and pre-OS communication over LAN (e.g. OS command-line interface and serial redirected BIOS menu).

5.12.1 Preconditions for SOL

5.12.1.1 Supported LAN interfaces

Three of MIC-5603's Ethernet interfaces can be used for Serial over LAN:

- Both AMC base interfaces: AMC Port 0 and 1
- The front panel LAN2 RJ-45 connector

Note! *The LAN controller used for SOL is connected to the payload power domain. To be able to use Serial over LAN, the payload needs to be powered!*

5.12.1.2 LAN controller and UART MUX configuration

The LAN and UART configuration of the Processor AMC is flexible and allows different configurations. To avoid "wrong" setups, users should always verify the actual LAN and UART configuration settings (Chapter 5.6.2 - Configuration setting OEM commands), before working with SOL:

- Select the LAN interface to be used (front panel or AMC base interface)
- Make sure the LAN channel priority is appropriate
- Select UART interface to be used (COM1 or COM2)

5.12.1.3 Default parameter

Following default parameters are good to know for the initial MIC-5603 LAN setup:

IP-Address: 192.168.1.1

LAN Channel Number: 5

Username: "administrator"

Password: "advantech"

5.12.2 LAN configuration with IPMItool

The open source IPMItool utility is used in this chapter for the MIC-5603 SOL and LAN parameter configuration. Any other utility, based on standard IPMI commands, can be used as well.

To get an overview of all possible commands within an IPMItool command group, please use the single keywords (e.g. "lan", "user" or "sol") only.

5.12.2.1 LAN commands

- lan print [channel number]

Get the LAN configuration parameters for a given channel.

```
[root@localhost ~]# ipmitool lan print
Set in Progress         : Set Complete
Auth Type Support       : NONE MD5 PASSWORD
Auth Type Enable        : Callback : NONE MD5 PASSWORD
                        : User     : NONE MD5 PASSWORD
                        : Operator : NONE MD5 PASSWORD
                        : Admin    : NONE MD5 PASSWORD
                        : OEM      :
IP Address Source       : Static Address
IP Address              : 192.168.1.1
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0b:ab:3e:45:87
Default Gateway IP      : 0.0.0.0
RMCP+ Cipher Suites     : 0,1,2,3,6,7,8,11,12
Cipher Suite Priv Max   : aaaaaaaaaXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
                        :     O=OEM
```

- lan set <channel> <command> [option]

This command can be used to change several MMC LAN parameters (e.g. IP address, netmask, gateway IP address,…). Below example demonstrates how to change the MMC IP address.

```
[root@localhost ~]# ipmitool lan set 5 ipaddr 172.21.35.104
Setting LAN IP Address to 172.21.35.104
```

5.12.2.2 User commands

- user list

Get the list of all supported users.

```
[root@localhost ~]# ipmitool user list
ID  Name             Callin  Link Auth  IPMI Msg   Channel Priv Limit
1                     true    true       true       NO ACCESS
2   callback          true    true       true       NO ACCESS
3   user              true    true       true       NO ACCESS
4   operator          true    true       true       NO ACCESS
```

- user set name <user id> [username]

This command can be used to change the user name.

```
[root@localhost ~]# ipmitool user set name 2 newuser
```

- user set password <user id> [password]

This command can be is used change the user password.

```
[root@localhost ~]# ipmitool user set password 2 newpassword
```

5.12.3 SOL session with IPMItool

Advantech recommends using IPMItool to successful open a SOL session with MIC-5603. The "lanplus" interface (RMCP+) of IPMItool must be used to be able to change SOL parameters and establish SOL sessions.

Following general IPMItool parameters are needed for RMCP+ and IPMItool "sol" commands:

```
ipmitool -I lanplus -H <IP-Address> -U <User> -P <Password> sol
<SOL-Command>
```

Command Line Syntax:

-I lanplus	Specifies RMCP+ as desired protocol
-H <IP-Address>	IP address assigned to the MMC
-U <User>	User account, default "administrator"
-P <Password>	Password used with specified user account (default password for user "administrator" is "advantech")

5.12.3.1 SOL parameter commands

- sol info [channel number]

Read out the SOL configuration parameters for a given channel.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol info
Set in progress                 : set-complete
Enabled                         : false
Force Encryption                : true
Force Authentication            : true
Privilege Level                 : ADMINISTRATOR
Character Accumulate Level (ms) : 250
Character Send Threshold        : 32
Retry Count                     : 2
Retry Interval (ms)             : 1000
Volatile Bit Rate (kbps)        : 115.2
Non-Volatile Bit Rate (kbps)    : 115.2
Payload Channel                 : 7 (0x07)
Payload Port                    : 623
```

- sol set <parameter> <value> [channel]

This command allows modifying special SOL configuration parameters.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol set

SOL set parameters and values:

  set-in-progress             set-complete | set-in-progress | com-
mit-write
  enabled                     true | false
  force-encryption            true | false
  force-authentication        true | false
  privilege-level             user | operator | admin | oem
  character-accumulate-level  <in 5 ms increments>
  character-send-threshold    N
  retry-count                 N
  retry-interval              <in 10 ms increments>
  non-volatile-bit-rate       serial | 9.6 | 19.2 | 38.4 | 57.6 |
115.2
  volatile-bit-rate           serial | 9.6 | 19.2 | 38.4 | 57.6 |
115.2
```

5.12.3.2 SOL session activation

Finally, the IPMItool "sol activate" command need to be issued to establish the SOL session to MIC-5603 from remote.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol acti-
vate
[SOL Session operational.  Use ~? for help]
…
~. [terminated ipmitool]
```

To terminate an active IPMItool SOL session, please use the key sequence"~" + "." (tilde and dot).

Note! *There can only be one Serial over LAN session active at once!*

Chapter 6

HPM.1 Update

This chapter describes the update of following software / firmware components.

Sections include:

- **MMC Firmware**
- **FPGA Configuration**
- **BIOS Image**
- **- NVRAM Image (BIOS Settings)**

6.1 HPM.1 preconditions

6.1.1 IPMItool

Before upgrading, users need to prepare a HPM.1 capable update utility. Advantech recommends to use the open and verified "IPMItool" (>= version 1.8.10).

In general, any tool compliant to the PICMG HPM.1 R1.0 specification can be used.

6.1.2 Interfaces

HPM.1 provides a way to upgrade firmware via different interfaces (verify Chapter 5.1 - IPMI interfaces).

The MIC-5603 Processor AMC supports following IPMI interfaces:

- KCS (local payload interface, active payload and OS support needed)
- IPMB-L (remote, bridged via Carrier-/Shelf Manager, independent of payload)
- LAN interface (remote, active payload required)

The upgrade procedures in the following chapters are described with the help of KCS, since this is the easiest method. Using LAN or IPMB is similar, only the IPMI-tool interface parameters, which need to be used, are different.

6.2 MMC firmware upgrade

6.2.1 Load new MMC firmware image

Type IPMItool HPM.1 upgrade command and select the new MMC firmware image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic5603_standard_hpm_fw_00_24.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/
n y
OK

Performing upgrade stage:

--------------------------------------------------------------------
------------
|ID | Name      |    Versions          |    Upload Progress  | Upload|
Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time
| Size  |
|---|-----------|-------|-------|-------||----+----+----+----||----
---|-------|
| 1 |5603 MMC   |  0.22 |  0.20 |  0.24 ||...................|| 02.16
| 39d60 |
--------------------------------------------------------------------
------------

Firmware upgrade procedure successful
```

6.2.2 Activate MMC firmware

Although the new MMC FW is successfully downloaded to the board (called "deferred" version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:

Waiting firmware activation...OK
```

The front panel FRU LED's 1 and 2 (red OOS and green payload LED) are flashing during the FW update activation! This procedure needs around 60 seconds to finalize the update.

6.3 FPGA configuration upgrade

6.3.1 Load new FPGA image

Type IPMItool HPM.1 upgrade command and select the new FPGA image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic5603_standard_hpm_fpga_02_12.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/
n y
OK

Performing upgrade stage:

------------------------------------------------------------------
------------
|ID | Name     |    Versions          |    Upload Progress  | Upload|
Image |
|   |          | Active| Backup| File  |0%      50%     100%| Time
| Size  |
|---|-----------|-------|-------|-------||----+----+----+----||----
---|-------|
|*2 |5603 FPGAA |  2.10 |  2.08 |  2.12 ||...................|| 02.21
| 3bf70 |
------------------------------------------------------------------
------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

6.3.2 Activate FPGA configuration

Although the new FPGA configuration is successfully stored on the board ("deferred" version), it needs to be activated before it's loaded into the FPGA chip. Following two actions are needed to finish the upgrade.

6.3.2.1 HPM.1 activate command

Schedule the FPGA load with the HPM.1 "Activate" command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:
```

6.3.2.2 Payload cold reset

In order to activate the new FPGA image a payload cold reset is required.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways:

- If the user is working on the local OS (KCS), a linux "reboot","poweroff" or "halt".
- If the user accesses the MMC through the other interfaces (LAN/IPMB), a deactivation and activation cycle is needed, in order to update the FPGA.

The front panel FRU LED's 1 and 2 (red OOS and green payload LED) are flashing during the FW update activation! This procedure needs around 200 seconds to finalize the update.

6.4 BIOS upgrade

6.4.1 Load new BIOS image

Type IPMItool HPM.1 upgrade command and select the new BIOS image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic5603_standard_hpm_bios_00_10.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/
n y
OK

Performing upgrade stage:

------------------------------------------------------------------------
------------
|ID | Name      |    Versions          |    Upload Progress  | Upload|
Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time
| Size  |
|---|-----------|-------|-------|-------||----+----+----+----||----
---|-------|
|*3 |5603 BIOSS |  0.08 |  0.09 |  0.10 ||...................|| 25.21
| 7c000c|
------------------------------------------------------------------------
------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

6.4.2 Activate BIOS image

Although the new BIOS image is successfully loaded ("deferred" version), it needs to be activated before users can boot the new BIOS. Following two actions are needed to finish the upgrade.

6.4.2.1 HPM.1 activate command

Schedule the BIOS load with the HPM.1 "Activate" command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.2:
```

6.4.2.2 Payload cold reset

A payload cold reset is required to activate the new BIOS image.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways:

- If the user is working on the local OS (KCS), a linux “reboot”,”poweroff” or “halt”.
- If the user accesses the MMC through the other interfaces (LAN/IPMB), a deactivation and activation cycle is needed to load the new BIOS image.

6.5 NVRAM upgrade

In contrast to the BIOS image update, a BIOS setting (NVRAM) update image is not directly written to any of the BIOS SPI flashes. The BIOS settings are stored in the external SPI flash of the MMC to support deferred activation. For extended flexibility, the external SPI flash supports different sections to store up to four BIOS setting images at the same time. Each of these four NVRAM images can be set to "active" at any time and will be copied to the active BIOS flash at the next OS boot.

6.5.1 Select NVRAM upgrade section (optional)

As described above, the MMC provides multiple upgrade sections for different NVRAM images. An IPMI OEM command (verify Chapter 5.6 - OEM Commands for details) can be used to select the one of the BIOS setting sections in the external flash.

```
[root@localhost ~]# ipmitool raw 0x2E 0x40 0x39 0x28 0x00 0x03 0x01
<section>
```

Default section for a NVRAM update is section zero, if the OEM command is not used.

6.5.2 Load new NVRAM image

Type IPMItool HPM.1 upgrade command and select the new NVRAM image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic5603_standard_hpm_nvram_00_03.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? y/
n y
OK

Performing upgrade stage:

------------------------------------------------------------------
------------
|ID | Name      |    Versions          |    Upload Progress  | Upload|
Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time
| Size  |
|---|-----------|-------|-------|-------||----+----+----+----||----
---|-------|
|*4 |5603 NVRAMM|  0.02 | --.-- |  0.03 ||...................|| 02.31
| 4000c |
------------------------------------------------------------------
------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

6.5.3 Activate NVRAM image

Following two actions are needed to boot BIOS with the new NVRAM image and BIOS settings.

6.5.3.1 OEM NVRAM section activate command

Since there are more than one NVRAM sections provided by the MMC, another IPMI OEM command is used to activate a selected NVRAM section (default = 0).

```
[root@localhost ~]# ipmitool raw 0x2E 0x40 0x39 0x28 0x00 0x03 0x02
<section>
```

6.5.3.2 Payload cold reset

A payload cold reset is required to activate the new NVRAM image.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways:

- If the user is working on the local OS (KCS), a linux "reboot","poweroff" or "halt".
- If the user accesses the MMC through the other interfaces (LAN/IPMB), a deactivation and activation cycle is needed to load the new NVRAM image.

6.6 Verify successful upgrades

To verify successful updates, the IPMItool hpm check command can be used.

```
[root@localhost ~]# ipmitool hpm check

PICMG HPM.1 Upgrade Agent 1.0.2:

-------Target Information-------
Device Id          : 0x21
Device Revision    : 0x81
Product Id         : 0x5603
Manufacturer Id    : 0x2839 (Unknown (0x2839))


---------------------------------
|ID | Name      |    Versions   |
|   |           | Active| Backup|
---------------------------------
| 0 |5603 BLL   |  0.22 | --.-- |
| 1 |5603 MMC   |  0.24 |  0.22 |
|*2 |5603 FPGAA |  2.12 |  2.10 |
|*3 |5603 BIOSS |  0.10 |  0.08 |
|*4 |5603 NVRAMM|  0.03 | --.-- |
---------------------------------
(*) Component requires Payload Cold Reset
```

After a successful upgrade, the new backup version should be the former active version (if "Backup" versions are supported). And the new "Active" version should be the version of the used upload file.

Appendix A

IPMI/PICMG Command Subset Supported by MMC

A.1 Standard IPMI Commands (v2.0)

IPM Device "Global" Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get Device ID	20.1	App	01h	Mandatory	Mandatory	Yes
Cold Reset	20.2	App	02h	Optional	Optional	Yes
Warm Reset	20.3	App	03h	Optional	Optional	Yes
Get Self Test Results	20.4	App	04h	Mandatory	Optional	Yes
Manufacturing Test On	20.5	App	05h	Optional	Optional	No
Set ACPI Power State	20.6	App	06h	Optional	Optional	No
Get ACPI Power State	20.7	App	07h	Optional	Optional	No
Get Device GUID	20.8	App	08h	Optional	Optional	Yes
Broadcast 'Get Device ID'	20.9	App	01h	Optional/ Mandatory	Mandatory	Yes

BMC Watchdog Timer Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Reset Watchdog Timer	27.5	App	22h	Mandatory	Optional	Yes
Set Watchdog Timer	27.6	App	24h	Mandatory	Optional	Yes
Get Watchdog Timer	27.7	App	25h	Mandatory	Optional	Yes

BMC Device and Messaging Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Set BMC Global Enables	22.1	App	2Eh	Mandatory	Optional	Yes
Get BMC Global Enables	22.2	App	2Fh	Mandatory	Optional	Yes
Clear Message Flags	22.3	App	30h	Mandatory	Optional	Yes
Get Message Flags	22.4	App	31h	Mandatory	Optional	Yes
Enable Message Channel Receive	22.5	App	32h	Optional	Optional	No
Get Message	22.6	App	33h	Mandatory	Optional	Yes
Send Message	22.7	App	34h	Mandatory	Optional	Yes
Read Event Message Buffer	22.8	App	35h	Optional	Optional	Yes
Get BT Interface Capabilities	22.10	App	36h	Mandatory	Optional	No
Get System GUID	22.14	App	37h	Optional	Optional	Yes
Get Channel Authentication Capabilities	22.13	App	38h	Optional	Optional	Yes
Get Session Challenge	22.15	App	39h	Optional	Optional	Yes

Activate Session	22.17	App	3Ah	Optional	Optional	Yes
Set Session Privilege Level	22.18	App	3Bh	Optional	Optional	Yes
Close Session	22.19	App	3Ch	Optional	Optional	Yes
Get Session Info	22.20	App	3Dh	Optional	Optional	Yes
Get AuthCode	22.21	App	3Fh	Optional	Optional	No
Set Channel Access	22.22	App	40h	Optional	Optional	Yes
Get Channel Access	22.23	App	41h	Optional	Optional	Yes
Get Channel Info	22.24	App	42h	Optional	Optional	Yes
Set User Access	22.26	App	43h	Optional	Optional	Yes
Get User Access	22.27	App	44h	Optional	Optional	Yes
Set User Name	22.28	App	45h	Optional	Optional	Yes
Get User Name	22.29	App	46h	Optional	Optional	Yes
Set User Password	22.30	App	47h	Optional	Optional	Yes
Activate Payload	24.1	App	48h	-	Optional	Yes
Deactivate Payload	24.2	App	49h	-	Optional	Yes
Get Payload Activation Status	24.4	App	4Ah	-	Optional	No
Get Payload Instance Info	24.5	App	4Bh	-	Optional	No
Set User Payload Access	24.6	App	4Ch	-	Optional	Yes
Get User Payload Access	24.7	App	4Dh	-	Optional	Yes
Get Channel Payload Support	24.8	App	4Eh	-	Optional	No
Get Channel Payload Version	24.9	App	4Fh	-	Optional	No
Get Channel OEM Payload Info	24.10	App	50h	-	Optional	No
Master Write-Read	22.11	App	52h	Mandatory	Optional	Yes
Get Channel Cipher Suites	22.15	App	54h	-	Optional	Yes
Suspend/Resume Payload Encryption	24.3	App	55h	-	Optional	No
Set Channel Security Keys	22.25	App	56h	-	Optional	Yes
Get System Interface Capabilities	22.9	App	57h	-	Optional	No

Chassis Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get Chassis Capabilities	28.1	Chassis	00h	Mandatory	Optional	No
Get Chassis Status	28.2	Chassis	01h	Optional/ Mandatory	Optional	No
Chassis Control	28.3	Chassis	02h	Optional/ Mandatory	Optional	No
Chassis Reset	28.4	Chassis	03h	Optional	Optional	No
Chassis Identify	28.5	Chassis	04h	Optional	Optional	No
Set Front Panel Button Enables	28.6	Chassis	0Ah	-	-	No
Set Chassis Capabilities	28.7	Chassis	05h	Optional	Optional	No
Set Power Restore Policy	28.8	Chassis	06h	Optional	Optional	No
Set Power Cycle Interval	28.9	Chassis	0Bh	-	-	No
Get System Restart Cause	28.11	Chassis	07h	Optional	Optional	No
Set System Boot Options	28.12	Chassis	08h	Optional	Optional	No
Get System Boot Options	28.13	Chassis	09h	Optional	Optional	No
Get POH Counter	28.14	Chassis	0Fh	Optional	Optional	No

Event Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Set Event Receiver	29.1	S/E	00h	Mandatory	Mandatory	Yes
Get Event Receiver	29.2	S/E	01h	Mandatory	Mandatory	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	02h	Mandatory	Mandatory	Yes

PEF and Alerting Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get PEF Capabilities	30.1	S/E	10h	Mandatory	Optional	No
Arm PEF Postpone Timer	30.2	S/E	11h	Mandatory	Optional	No
Set PEF Configuration Parameters	30.3	S/E	12h	Mandatory	Optional	No
Get PEF Configuration Parameters	30.4	S/E	13h	Mandatory	Optional	No
Set Last Processed Event ID	30.5	S/E	14h	Mandatory	Optional	No
Get Last Processed Event ID	30.6	S/E	15h	Mandatory	Optional	No
Alert Immediate	30.7	S/E	16h	Optional	Optional	No
PET Acknowledge	30.8	S/E	17h	Optional	Optional	No

Sensor Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get Device SDR Info	35.2	S/E	20h	Optional	Mandatory	Yes
Get Device SDR	35.3	S/E	21h	Optional	Mandatory	Yes
Reserve Device SDR Repository	35.4	S/E	22h	Optional	Mandatory	Yes
Get Sensor Reading Factors	35.5	S/E	23h	Optional	Optional	No
Set Sensor Hysteresis	35.6	S/E	24h	Optional	Optional	No
Get Sensor Hysteresis	35.7	S/E	25h	Optional	Optional	No
Set Sensor Threshold	35.8	S/E	26h	Optional	Optional	Yes
Get Sensor Threshold	35.9	S/E	27h	Optional	Optional	Yes
Set Sensor Event Enable	35.10	S/E	28h	Optional	Optional	Yes
Get Sensor Event Enable	35.11	S/E	29h	Optional	Optional	Yes
Re-arm Sensor Events	35.12	S/E	2Ah	Optional	Optional	Yes
Get Sensor Event Status	35.13	S/E	2Bh	Optional	Optional	Yes
Get Sensor Reading	35.14	S/E	2Dh	Mandatory	Mandatory	Yes
Set Sensor Type	35.15	S/E	2Eh	Optional	Optional	No
Get Sensor Type	35.16	S/E	2Fh	Optional	Optional	No

FRU Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get FRU Inventory Area Info	34.1	Storage	10h	Mandatory	Mandatory	Yes
Read FRU Data	34.2	Storage	11h	Mandatory	Mandatory	Yes
Write FRU Data	34.3	Storage	12h	Mandatory	Mandatory	Yes

SDR Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get SDR Repository Info	33.9	Storage	20h	Mandatory	Optional	Yes
Get SDR Repository Allocation Info	33.10	Storage	21h	Optional	Optional	No
Reserve SDR Repository	33.11	Storage	22h	Mandatory	Optional	Yes
Get SDR	33.12	Storage	23h	Mandatory	Optional	Yes
Add SDR	33.13	Storage	24h	Mandatory	Optional	No
Partial Add SDR	33.14	Storage	25h	Mandatory	Optional	No
Delete SDR	33.15	Storage	26h	Optional	Optional	No
Clear SDR Repository	33.16	Storage	27h	Mandatory	Optional	Yes
Get SDR Repository Time	33.17	Storage	28h	Optional/ Mandatory	Optional	Yes
Set SDR Repository Time	33.18	Storage	29h	Optional/ Mandatory	Optional	Yes
Enter SDR Repository Update Mode	33.19	Storage	2Ah	Optional	Optional	No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	Mandatory	Optional	No
Run Initialization Agent	33.21	Storage	2Ch	Optional	Optional	No

SEL Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get SEL Info	31.2	Storage	40h	Mandatory	Optional	Yes
Get SEL Allocation Info	31.3	Storage	41h	Optional	Optional	No
Reserve SEL	31.4	Storage	42h	Optional	Optional	Yes
Get SEL Entry	31.5	Storage	43h	Mandatory	Optional	Yes
Add SEL Entry	31.6	Storage	44h	Mandatory	Optional	Yes
Partial Add SEL Entry	31.7	Storage	45h	Mandatory	Optional	No
Delete SEL Entry	31.8	Storage	46h	Optional	Optional	No
Clear SEL	31.9	Storage	47h	Mandatory	Optional	Yes
Get SEL Time	31.10	Storage	48h	Mandatory	Optional	Yes
Set SEL Time	31.11	Storage	49h	Mandatory	Optional	Yes
Get Auxiliary Log Status	31.12	Storage	5Ah	Optional	Optional	No
Set Auxiliary Log Status	31.13	Storage	5Bh	Optional	Optional	No

LAN Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Set LAN Configuration Parameters	23.1	Transport	01h	Optional/ Mandatory	Optional	Yes
Get LAN Configuration Parameters	23.2	Transport	02h	Optional/ Mandatory	Optional	Yes
Suspend BMC ARPs	23.3	Transport	03h	Optional/ Mandatory	Optional	No
Get IP/UDP/RMCP Statistics	23.4	Transport	04h	Optional	Optional	No

Serial/Modem Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Set Serial/Modem Configuration	25.1	Transport	10h	Optional/ Mandatory	Optional	No
Get Serial/Modem Configuration	25.2	Transport	11h	Optional/ Mandatory	Optional	No
Set Serial/Modem Mux	25.3	Transport	12h	Optional	Optional	No
Get TAP Response Codes	25.4	Transport	13h	Optional	Optional	No
Set PPP UDP Proxy Transmit Data	25.5	Transport	14h	Optional	Optional	No
Get PPP UDP Proxy Transmit Data	25.6	Transport	15h	Optional	Optional	No
Send PPP UDP Proxy Packet	25.7	Transport	16h	Optional	Optional	No
Get PPP UDP Proxy Receive Data	25.8	Transport	17h	Optional	Optional	No
Serial/Modem Connection Active	25.9	Transport	18h	Optional/ Mandatory	Optional	No
Callback	25.10	Transport	19h	Optional	Optional	No
Set User Callback Options	25.11	Transport	1Ah	Optional	Optional	No
Get User Callback Options	25.12	Transport	1Bh	Optional	Optional	No
SOL Activating	26.1	Transport	20h	-	-	Yes
Set SOL Configuration Parameters	26.2	Transport	21h	-	-	Yes
Get SOL Configuration Parameters	26.3	Transport	22h	-	-	Yes

Bridge Management Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get Bridge State	[ICMB]	Bridge	00h	Optional/ Mandatory	Optional	No
Set Bridge State	[ICMB]	Bridge	01h	Optional/ Mandatory	Optional	No
Get ICMB Address	[ICMB]	Bridge	02h	Optional/ Mandatory	Optional	No
Set ICMB Address	[ICMB]	Bridge	03h	Optional/ Mandatory	Optional	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	Optional/ Mandatory	Optional	No
Get Bridge Statistics	[ICMB]	Bridge	05h	Optional/ Mandatory	Optional	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	Optional/ Mandatory	Optional	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	Optional/ Mandatory	Optional	No
Get Bridge Proxy Address	[ICMB]	Bridge	09h	Optional/ Mandatory	Optional	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	Optional/ Mandatory	Optional	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	Optional/ Mandatory	Optional	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	Optional/ Mandatory	Optional	No

Discovery Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Prepare For Discovery	[ICMB]	Bridge	10h	Optional/ Mandatory	Optional	No
Get Addresses	[ICMB]	Bridge	11h	Optional/ Mandatory	Optional	No
Set Discovered	[ICMB]	Bridge	12h	Optional/ Mandatory	Optional	No
Get Chassis Device ID	[ICMB]	Bridge	13h	Optional/ Mandatory	Optional	No
Set Chassis Device ID	[ICMB]	Bridge	14h	Optional/ Mandatory	Optional	No

Bridging Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Bridge Request	[ICMB]	Bridge	20h	Optional/ Mandatory	Optional	No
Bridge Message	[ICMB]	Bridge	21h	Optional/ Mandatory	Optional	No

Event Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get Event Count	[ICMB]	Bridge	30h	Optional/ Mandatory	Optional	No
Set Event Destination	[ICMB]	Bridge	31h	Optional/ Mandatory	Optional	No
Set Event Reception State	[ICMB]	Bridge	32h	Optional/ Mandatory	Optional	No
Send ICMB Event Message	[ICMB]	Bridge	33h	Optional/ Mandatory	Optional	No
Get Event Destination	[ICMB]	Bridge	34h	Optional/ Mandatory	Optional	No
Get Event Reception State	[ICMB]	Bridge	35h	Optional/ Mandatory	Optional	No

OEM Commands for Bridge NetFn

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
OEM Commands	[ICMB]	Bridge	C0h-FEh	Optional/ Mandatory	Optional	No

Other Bridge Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Error Report	[ICMB]	Bridge	FFh	Optional/ Mandatory	Optional	No

PICMG IPMI Commands

AdvancedTCA (PICMG 3.0 R3.0 AdvancedTCA Base Specification)

Command	PICMG 3.0 Table	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get PICMG Properties	3-11	PICMG	00h	-	Mandatory	Yes
Get Address Info	3-10	PICMG	01h	-	N/A	No
Get Shelf Address Info	3-16	PICMG	02h	-	N/A	No
Set Shelf Address Info	3-17	PICMG	03h	-	N/A	No
FRU Control	3-27	PICMG	04h	-	Mandatory	Yes
Get FRU LED Properties	3-29	PICMG	05h	-	Mandatory	Yes
Get LED Color Capabilities	3-30	PICMG	06h	-	Mandatory	Yes
Set FRU LED State	3-31	PICMG	07h	-	Mandatory	Yes
Get FRU LED State	3-32	PICMG	08h	-	Mandatory	Yes
Set IPMB State	3-70	PICMG	09h	-	N/A	No
Set FRU Activation Policy	3-20	PICMG	0Ah	-	N/A	No
Get FRU Activation Policy	3-21	PICMG	0Bh	-	N/A	No
Set FRU Activation	3-19	PICMG	0Ch	-	N/A	No
Get Device Locator Record ID	3-39	PICMG	0Dh	-	Mandatory	Yes
Set Port State	3-59	PICMG	0Eh	-	N/A	No
Get Port State	3-60	PICMG	0Fh	-	N/A	No
Compute Power Properties	3-82	PICMG	10h	-	N/A	No
Set Power Level	3-84	PICMG	11h	-	N/A	No
Get Power Level	3-83	PICMG	12h	-	N/A	No
Renegotiate Power	3-91	PICMG	13h	-	N/A	No
Get Fan Speed Properties	3-86	PICMG	14h	-	N/A	No
Set Fan Level	3-88	PICMG	15h	-	N/A	No
Get Fan Level	3-87	PICMG	16h	-	N/A	No
Bused Resource	3-62	PICMG	17h	-	N/A	No
Get IPMB Link Info	3-68	PICMG	18h	-	N/A	No

Get Shelf Manager IPMB Address	3-38	PICMG	1Bh	-	N/A	No
Set Fan Policy	3-89	PICMG	1Ch	-	N/A	No
Get Fan Policy	3-90	PICMG	1Dh	-	N/A	No
FRU Control Capabilities	3-26	PICMG	1Eh	-	Mandatory	Yes
FRU Inventory Device Lock Control	3-42	PICMG	1Fh	-	Optional	No
FRU Inventory Device Write	3-43	PICMG	20h	-	Optional	No
Get Shelf Manager IP Addresses	3-36	PICMG	21h	-	Optional	No
Get Shelf Power Allocation	3-85	PICMG	22h	-	N/A	No
Get Telco Alarm Capability	3-93	PICMG	29h	-	-	No
Set Telco Alarm State	3-94	PICMG	2Ah	-	-	No
Get Telco Alarm State	3-95	PICMG	2Bh	-	-	No
Get Telco Alarm Location	3-96	PICMG	39h	-	-	No
Set FRU Extracted	3-25	PICMG	3Ah	-	-	No

AMC.0 (R2.0)

Command	**AMC.0 Table**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Module MMC Req.**	**Advantech MMC support**
Set AMC Port State	3-27	PICMG	19h	-	Optional/ Mandatory	Yes
Get AMC Port State	3-28	PICMG	1Ah	-	Optional/ Mandatory	Yes
Set Clock State	3-44	PICMG	2Ch	-	Optional/ Mandatory	Yes
Get Clock State	3-45	PICMG	2Dh	-	Optional/ Mandatory	Yes

HPM.1 (R1.0)

Command	HPM.1 Table	NetFn	CMD	IPMI BMC Req.	Module MMC Req.	Advantech MMC support
Get target upgrade capabilities	3-3	PICMG	2Eh	-	Mandatory	Yes
Get component properties	3-5	PICMG	2Fh	-	Mandatory	Yes
Abort Firmware Upgrade	3-15	PICMG	30h	-	Optional	Yes
Initiate upgrade action	3-8	PICMG	31h	-	Mandatory	Yes
Upload firmware block	3-9	PICMG	32h	-	Mandatory	Yes
Finish firmware upload	3-10	PICMG	33h	-	Mandatory	Yes
Get upgrade status	3-2	PICMG	34h	-	Optional/ Mandatory	Yes
Activate firmware	3-11	PICMG	35h	-	Mandatory	Yes
Query Self-test Results	3-12	PICMG	36h	-	Optional/ Mandatory	Yes
Query Rollback status	3-13	PICMG	37h	-	Optional/ Mandatory	Yes
Initiate Manual Rollback	3-14	PICMG	38h	-	Optional/ Mandatory	Yes

OEM/Group IPMI Commands

Advantech OEM Commands

Command	**NetFn**	**CMD**	**IPMI BMC Req.**	**Module MMC Req.**	**Advantech MMC support**
Store Configuration Settings	OEM/ Group	40h	-	-	Yes
Read Configuration Settings	OEM/ Group	41h	-	-	Yes
Read Port 80	OEM/ Group	80h	-	-	Yes
Clear CMOS	OEM/ Group	81h	-	-	Yes
Read MAC Address	OEM/ Group	E2h	-	-	Yes
Load Default Configuration	OEM/ Group	F2h	-	-	Yes

Appendix B

Driver & Tools

B.1 OpenIPMI

The OpenIPMI project provides an IPMI Kernel driver which is available in most of the Linux distributions

Source: OpenIPMI Page (http://openipmi.sourceforge.net/)

The Open IPMI Linux device driver is designed as a full-function IPMI device driver with the following features:

- Allows multiple users.
- Allows multiple interfaces.
- Allows both kernel and userland things to use the interface.
- Fully supports the watchdog timer.
- It works like IPMI drivers are supposed to. It tracks outgoing messages and matches up their responses automatically. It automatically fetches events, received messages, etc.
- It supports interrupts (I have tested them now).
- It has backwards-compatability modules for supporting the Radisys IPMI driver and the Intel IMB driver.
- It's modular. You don't have to have the standard userland interface. You don't have to have the watchdog. Etc.
- It supports generating an event on a panic.

More information regarding the IPMI driver can be found on the OpenIPMI Project page, http://openipmi.sourceforge.net/

The KCS register interfaces are at 0xCA2 /0xCA3 and used by the OpenIPMI driver as default.

B.2 IPMITool

The IPMITool provides an easy-to-use set of functions and commands, to access the MMC via the KCS interface within the Operating System of the MIC-5603 or via Ethernet through NC-SI from external. The IPMI Tool also supports bridged IPMI commands to access the MMC, if the carrier manager provides an IPMI-over-LAN interface. See Chapter 5 for a more detailed description of different access methods and IPMITool calls.

The IPMITool source code can be downloaded from the official project page, http://ipmitool.sourceforge.net.

Built binaries and executable for Windows and Linux can be downloaded from the Advantech page in 2012 Q3

Additional drivers and tools which are useful on/with MIC-5603 will be ready in 2013 Q1

BSP - Board Support Packag will be ready in 2013 Q1

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