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VCB8004 VME 64x INDUSTRY PACK CARRIER BOARD

USERS MANUAL

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1. PRODUCT DESCRIPTION

The VCB 8004 is a 6U (double height) VME board constructed to the VME64x standard, with EMC front panel, injector/ejector handles, guide pin and slot keying, static discharge protection, hot swap capability, blue power up LED, geographical or jumper selected addressing, 5-row P1 and P2 connectors and 5-row P0 connector.

The module features hot-swap capability with auto power up and host interaction. An on-board FPGA allows full mapping of the IP board memory, I/O and ID spaces.

The VME interface supports short I/O access A16: D16:D08 (EO), standard I/O access A24:D16:D08 (EO) and extended memory access A32: D64: D32: D16.

The module also has the ability to carry out MBLT A32 D64 and BLT A32:D32:D16 data transfers on IP memory space.

Four Industry Pack sites are available and can accept 4 single-size Industry Packs. The board has the capability to multiple-address the memory of IP sites and read/write data to them simultaneously using a data width of 32 or 64 bits.

The carrier board supports 8MHz and 32MHz IP interfaces.

One of VMEbus interrupt lines IRQ1 to IRQ7 can be selected and enabled by writing to an on-board register. The Industry Pack interrupt lines IntReq0* and IntReq1* from each of the four sites can be enabled on an individual basis and mapped to the selected VME IRQ line.

Four front panel mounted LED’s flash to visually confirm completed IP access cycles to individual slots.

There is a TTL ‘Inhibit’ input on the front panel that allows connection to any or all of the IP card Strobe* lines through jumpers. The signal is routed through this pin on the IP logic connector to allow overall control to be applied to IP boards in data acquisition systems.

The ‘GO’ output can be connected to the ‘Inhibit’ input through a jumper to synchronise timing between carrier boards.

The carrier board has some thickened I/O tracks to allow the IP boards to be powered externally to give full isolation.

All I/O is via the VME backplane P0 and P2 connectors as specified in the VME64 extensions specification. The signals connect to the industry pack sites according to the VME64x Greenspring pinout for IP module carriers.

Hytec has a number of rear-mounted transition cards with high-density 50-way [SCSI2] connectors, which can cater for all 200 IP I/O signals and provide any necessary signal conditioning.

1.1 Key Features

- VME64 extensions / Industry Pack Carrier Board
- VME64x rear panel I/O
- Base Address decoding by either Geographical addressing or jumper selectable
- IP memory space accesses software configurable from 1Mbyte to 8Mbytes
- MBLT D64 operation for simultaneous memory data access to all four IP sites
- BLT or Single D32 operation for simultaneous memory data access to two IP sites
- BLT or Single D16 operation for memory data access to one IP site
- IP module Clock speeds can be individually selected to be 8MHz or 32MHz by software.
- Full EMC shielding and insertion/extraction handles
- Fully Hot-Swap capable with auto power-up and host interaction
- 6U (double height) VME base card
- User selectable VME interrupt level via software programmable registers
- Up to two interrupt requests are supported for each IP module
- Interrupt release mechanism RORA or ROAK software selectable
- Front panel TTL Go/Inhibit signals allow control of IP timing synchronisation
- Thickened I/O lines to allow externally power supply to IPs
- VME 64x Configuration ROM
- On-board 32MHz clock generation
- VME64x guide pin and slot keying
- 3.3V and 5V supply to P2 connector
- Self-resetting PTC fuses on all the IP power supplies

2. USE OF THE VME DATA BUS AND MEMORY ACCESS

2.1 VME Addressing

The module uses A16/D16/D08 (EO) (Even and Odd byte3) or A24/D16/D08 (EO) for accesses to the IP I/O, IP ID and Carrier board Configuration Registers.
The base address of these areas are set either by PCB jumpers (J6 to J10) or by VME64x geographical addressing lines GA0 to GA4.

Address	Offset	Range	Assignment	Size
I/O Base+	0x0000	0x0000 0x007E	IP A I/O Space	128 Bytes
I/O Base+	0x0080	0x0080 0x00FE	IP A ID Space	128 Bytes
I/O Base+	0x0100	0x0100 0x017E	IP B I/O Space	128 Bytes
I/O Base+	0x0180	0x0180 0x01FE	IP B ID Space	128 Bytes
I/O Base+	0x0200	0x0200 0x027E	IP C I/O Space	128 Bytes
I/O Base+	0x0280	0x0280 0x02FE	IP C ID Space	128 Bytes
I/O Base+	0x0300	0x0300 0x037E	IP D I/O Space	128 Bytes
I/O Base+	0x0380	0x0380 0x03FE	IP D ID Space	128 Bytes
I/O Base+	0x0400	0x0400 0x041E	Carrier on board registers	32 Bytes
I/O Base +	0x0420	0x0420 0x043E	SHARC Control Registers (option)	32 Bytes
I/O Base +	0x0440	0x0440 0x047E	Dual-Ported SRAM accessible from VME and SHARC (option)	64 Bytes
I/O Base+	0x0480	0x0480 0x04FF	Green Springs Type ID	128 Bytes
I/O Base+	0x0600	0x0600 0x07FF	VME64x configuration ROM (See **appendix B)**	512 Bytes

8004 A16 and A24 address Map

2.1.1 Short Addressing (A16 AM29h and 2Dh)

In Short address mode the geographical addressing lines equate to the address lines GA0 =A11 to GA4=A15 and the jumper address setting J6=A11 to J10=A15.
A11 - A15 is the module address determined by the setting of the relevant PCB jumpers or geographical address lines
IP I/O, IP ID and Carrier board Configuration Registers:
AM29 Short (A16) non-privileged.
AM2D Short (A16) supervisory.

2.1.2 Standard Addressing (A24 AM39h and 3Dh)

The A24 base address is determined either by PCB jumper settings J6=A19 to J10=A23 or by geographical addressing lines GA0 =A19 to GA4=A23.
IP I/O, IP ID and Carrier board Configuration Registers:
AM39 Standard (A24) non-privileged.
AM3D Standard (A24) supervisory.

2.1.3 Carrier board Configuration ROM (A24 AM2Fh)

See **appendix B** for the contents of the configuration ROM.
AM2F Configuration ROM/Control & Status Registers. Address selection as above

2.2 Memory Access

The module uses A32/D64/D32/D16 for accesses to the IP memory.
The base address of the memory can be set by either the Geographical address lines/Manual jumpers or by using the Memory Offset Register. Writing a '1' to bit '6' of the CSR CB (base+8h) selects the Memory Offset Register to set the base address.
Using the Memory Offset Register to store the base address allows the address lines A22 to A31 to be used to set the base address.
Geographical addressing uses the lines GA0=A22 to GA4=A26.
First need to select whether Geographical address lines or the Memory Offset register are to define the extended memory start address. This is selected using MEM MODE (bit 6) of the CSR CB register.

MEM MODE (bit 6 CSR)	**Memory Addressing Mode**
0	Geographical address lines
1	Memory Offset register

Bit 6 CSR CB setting the memory address mode

2.2.1 IP Memory Size

Some controllers have a limited memory range so to take account of this when using geographical and register addressing the memory size allocated to each IP card can be controlled:-

CSR CB		IP Memory Size	Address Lines	
IPMS1 (bit 8)	IPMS0 (bit 7)		Geographical Addressing	Memory Offset Reg
0	0	1MB	A22-A26	A22-A31
0	1	2MB	A23-A26	A23-A31
1	0	4MB	N/A	A24-A31
1	1	8MB	A27-A31	A25-A31

Here the GA address is shifted up one. This only allows 16 slots to be used with geographical Addressing

2.2.2 Carrier Board IP Memory Map

Address	**Memory Range**	**Memory**

	1MB	2MB	4MB	8MB	**Assignment**
Memory Base +	0x000000 0x0FFFFF	0x000000 0x1FFFFF	0x000000 0x3FFFFF	0x000000 0x7FFFFF	IP A
Memory Base +	0x100000 0x1FFFFF	0x200000 0x3FFFFF	0x400000 0x7FFFFF	0x800000 0xFFFFFF	IP B
Memory Base +	0x200000 0x2FFFFF	0x400000 0x5FFFFF	0x800000 0xBFFFFF	0x1000000 0x17FFFF	IP C
Memory Base +	0x300000 0x3FFFFF	0x600000 0x6FFFFF	0xC00000 0xFFFFFF	0x1800000 0x1FFFFF	IP D

2.2.3 Extended Addressing (A32 AM08, AM0C AM09, AM0D, AM0B and AM0F)

A32 Memory Address Modifiers:
Single - AM09 or AM0D (extended non-priv. or supervisory)
BLT - AM0B or AM0F (extended non-priv. or supervisory)
MBLT - AM08 or AM0C (extended non-priv. or supervisory) 64 bit block transfer.

3. ON BOARD FEATURES

The configuration and control of the 8004 module is achieved by the following registers:

Base	**Offset**	**Register**	**Description**
Base +	0x400	IP Status	Allows state of IP INT and Error flags to be monitored
Base +	0x404	Memory Offset	Sets base address of IP memory areas
Base +	0x408	Control & Status Register CB	Set up of 8004 carrier card
Base +	0x40C	IP Interrupt Select	Selects IP interrupts to be mapped to VME IRQ
Base +	0x410	Not Use	None

8004 On-Board Registers

3.1 IP Status Register (Read Only)

Address: Read = Base + 0x0400

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DMA REQ D0	DMA REQ C0	DMA REQ B0	DMA REQ A0	NU	NU	NU	IP ERR	INT REQ D1	INT REQ C1	INT REQ B1	INT REQ A1	INT REQ D0	INT REQ C0	INT REQ B0	INT REQ A0

Two interrupt status, one DMA status (not used) and one error status bits for each of IP sites A – D.
IP ERR Open drain signal can be driven by any IP card. The Industrial I/O Pack specification states that the error signals indicate a non-recoverable error from the IP module. See your IP documentation for a description of the error signal if used.

3.2 Memory Offset (Read/Write)

Address: Base + 0x0404

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	x	x	x	x	x	x

'x' = don't care
This register defines the IP memory base address when selected by MEMMODE='1' in CSR CB.

3.3 Control & Status Register Carrier Board (CSR CB)

Control (Write)
Address: Base + 0x0408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
AB 32Bit	CD 32Bit	IP D CLK	IP C CLK	IP B CLK	IP A CLK	INT RELS	IPMS 1	IPMS 0	MEM MODE	IPCLK SEL	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

Status (Read)
Address: Base + 0x0408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
AB 32Bit	CD 32Bit	IP D CLK	IP C CLK	IP B CLK	IP A CLK	INT RELS	IPMS 1	IPMS 0	MEM MODE	IPCLK SEL	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

Rst Clears status register to zero when written as a '1'.
INTEN Enable interrupt from carrier board to VMEbus backplane.
INTSEL0 Select VME interrupt level.
INTSEL1 Select VME interrupt level. (See section 4).
INTSEL2 Select VME interrupt level.
IPCLKSEL 0= Sel 8MHz IP clock or as set by IP A to D CLK 1=32MHz clock on all sites
MEMMODE Select memory base address to be defined by geographical address lines=0 or by Memory offset vector register=1.
IP MS0 Set IP memory size.
IP MS1 Set IP memory size. (See section 2.2)
INT RELS Interrupt release RORA=0 and ROAK = 1 (see section 4)
IP A CLK Set IP A clock speed 0 = 8MHz and 1 = 32MHz (If IPCLKSEL=1 overrides this setting).
IP B CLK Set IP B clock speed 0 = 8MHz and 1 = 32MHz (If IPCLKSEL=1 overrides this setting).
IP C CLK Set IP C clock speed 0 = 8MHz and 1 = 32MHz (If IPCLKSEL=1 overrides this setting).
IP D CLK Set IP D clock speed 0 = 8MHz and 1 = 32MHz (If IPCLKSEL=1 overrides this setting).
CD32bit Enables 32-bit data access to IP sites C&D
AB32bit Enables 32-bit data access to IP sites A&B

3.4 IP Interrupt Select Register (Read/Write)

Address: Base + 0x040C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	NU	IPINT D1	IPINT C1	IPINT B1	IPINT A1	IPINT D0	IPINT C0	IPINT B0	IPINT A0

This selects which IP interrupt request lines will be enabled.
'1' = corresponding IP card interrupt enabled.

3.5 VME System and Board Resets

3.5.1 A VME system reset will clear the following registers:

- CSR CB
- Memory Offset Register
- IP Interrupt Select register

3.5.2 A board reset generated from the CSR CB bit 0 will clear the following registers:

- CSR CB
- IP Interrupt Select register

4. INTERRUPT SETTINGS

The interrupt level generated by the carrier board is set using the CSR CB register INTSEL0 (bit 2), INTSEL1 (bit 3), and INTSEL2 (bit 4).

Interrupt Level	INTSEL 2	INTSEL 1	INTSEL 0
None	0	0	0
IRQ 1	0	0	1
IRQ 2	0	1	0
IRQ 3	0	1	1
IRQ 4	1	0	0
IRQ 5	1	0	1
IRQ 6	1	1	0
IRQ 7	1	1	1

VME Interrupt Level Select

The IP Interrupt Select register allows the user to enable only the IP interrupts required and mask off the rest.
To select an IP interrupt write a ‘1’ to the appropriate bit of the register see **section 3.4** above.
The interrupt vector is held on the individual IP cards.
To enable VME interrupts from the carrier board to the VMEbus backplane set bit 1 of the CSR CB to ‘1’.
Writing a ‘0’ to this register disables the interrupts.
The VME interrupt is released by clearing the interrupt enable bit INTEN (bit 1) in the CSR on acknowledge.
If bit 9 set to ‘1’ in CSR The VME interrupt is cleared when it is acknowledged [ROAK protocol].
If bit 9 set to ‘0’ in the CSR the interrupt is released when the interrupt service routine clears the interrupt enable bit [RORA protocol]. in the CSR (bit 1 INTEN) .

The IP interrupts are prioritised in the 8004 where IP A has the highest and IP D the lowest.

Each IP card can be loaded with a separate IP vector and when an interrupt occurs the controller will be given the interrupt vector of the highest priority IP card currently asserting either of its interrupt lines.

If all four card interrupt at the same time then IP A will be serviced first then IP B then IP C and finally IP D.

Reading the IP Status register of the 8004 at base + 0x0400 (READ ONLY) shows which IP cards have interrupts pending.

5. MEMORY 32BIT OR 64BIT DATA TRANSFERS

To carry out a 32bit data transfer set the relevant AB32(bits 15) or CD32(bits 14) bits in the CSR and address the first IP module of the pair i.e. 'A' for AB32 and 'C' for CD32.
There is no need to set AB32 or CD32 for a MBLT data transfer as these are ignored as it is 64 bit only.
When doing an MBLT must address IP site 'A'.
When doing a 32bit or 64bit data transfer the clocks for the IP modules involved must be the same either 8MHz or 32MHz as set in the CSR bits 10 to 13.

6. VME64x KEYING AND ALIGNMENT PINS

The keying mechanism provides for three key holes on top and three keying holes on the bottom of each board and subrack slot. Each key hole can be keyed with a "No Key" or a keying peg in one of four positions. With three key holes top and bottom the scheme provides a total of 15,625 keying combinations.

APPENDIX A PCB JUMPERS

Hytec 8004 IP Carrier Board

J1 Connects the common strobe line from the FPGA to Industry Pack C Logic Connector pin 46.
J2 Must be **IN** Factory set.
J3 Connects the common strobe line from the FPGA to Industry Pack A Logic Connector pin 46.
J4 Supplies switched and fused +5V to pins P2 A32 and P2 C32 (Delivered Not selected).
J5 Connects the common strobe line from the FPGA to Industry Pack B Logic Connector pin 46.
J6 – J10 Base address:. Make according to required A11-A15 base address short IO addressing or A19 – A23 for A24 Standard addressing
J11 Connects the common strobe line from the FPGA to Industry Pack D Logic Connector pin 46.
J12 This is Factory set.
J17 Selects GO to be driven by either INHIBIT front panel lemo or from FPGA logic in this version of the firmware the FPGA drives GO high. In this version the jumper should be either removed or in the INH position.

Note: The reference to the 'Common Strobe Line' refers to the front panel Inhibit signal which is passed through by the FPGA unprocessed, thus asserting the Inhibit input low will drive all connected IP logic connector pins 46 (Strobe*) low.

J13, J14, ,J15 and J16 Not used in this version.

Set Base Address Jumpers J6 – J10

To use VME64 geographical addressing lines all jumpers should be inserted in to position AUTO.

To use the user set base address removing all Base address jumpers from positions AUTO and insert the required jumpers in to positions MANUAL.
With no jumpers in position MANUAL for J6 to J10 the address is 0x0000 A16 or 0x000000 A24.
With one jumpers in position MANUAL for J6 the address is 0x0800 A16 or 0x080000 A24.
With all jumpers in position MANUAL for J6 to J10 the address is 0xF800 A16 or 0xF80000 A24.

Base Addrs (Hex)		A15 (Manual)	A14 (Manual)	A13 (Manual)	A12 (Manual)	A11 (Manual)
A16	A24					
0000	000000	OUT	OUT	OUT	OUT	OUT
0800	080000	OUT	OUT	OUT	OUT	IN
1000	100000	OUT	OUT	OUT	IN	OUT
1800	180000	OUT	OUT	OUT	IN	IN
: :	: :	: :	: :	: :	: :	: :
E000	E00000	IN	IN	IN	OUT	OUT
E800	E80000	IN	IN	IN	OUT	IN
F000	F00000	IN	IN	IN	IN	OUT
F800	F80000	IN	IN	IN	IN	IN

APPENDIX B Carrier Board Configuration ROM

Address Offset	Value	Definition
0x03	C1	Check Sum
0x07	00	Length of ID ROM MSB
0x0B	02	Length of ID ROM
0x0F	00	Length of ID ROM LSB
Configuration ROM data access width		
0x13	0x83	
CSR data access width		
0x17	0x83	
CSR space Specification ID		
0x1B	0x02	VME64x-1997
Identify a Valid CR		
0x1F	0x43	‘C’
0x23	0x52	‘R’
Manufacturer’s ID		
0x27	0x00	
0x2B	0x80	
0x2F	0x03	
Board ID		
0x33	0x80	
0x37	0x04	
0x3B	0x00	
0x3F	0x00	
Revision ID		
0x43	0x01	PCB issue
0x47	0x05	Xilinx version
0x4B	0x00	Xilinx revision nos
0x4F	0x01	Xilinx revision nos
ASCII string null terminated or 0x000000		
0x53	0x00	
0x57	0x00	
0x5B	0x00	
Program ID code		
0x7F	0x01	No program, ID ROM only
Interrupt Capabilities		
0xF7	0xFE	Denotes support for Int levels 7 – 1.
Data Access Width		
0x103	0x84	Accepts D32, D16 or D08(EO) cycles
Board Serial Number		
0xCB, 0xCF, 0xD3	0x	BEG_SN MSB
0xD7, 0xDB, 0xDF	0x	END_SN LSB
AM code mask		
0x123.. 0x13F	0x2200A2000000BB00	AM codes 3D, 39, 2F, 2D, 29, 0F, 0D, 0C, 0B, 09, 08

Reading the Configuration ROM using A16 (AM29 and AM2D) or A24 (AM39 and AM3D) the address is VME base address + 0x0600, the Configuration ROM offset.
Can read Configuration ROM using A24 AM2F starting at base address + 0x0000.

APPENDIX C ID PROM Registers (GreenSpring Format)

Address Offset	Value	Definition
0x481	0x49	ASCII “I”
0x483	0x50	ASCII “P”
0x485	0x41	ASCII “A”
0x487	0x43	ASCII “H”
0x489	0x80	Manufacturer’s ID
0x48B	0x84	Model Number
0x48D	0x0x	Revision
0x48F	0x00	Reserved
0x491	0x00	Driver ID, low byte
0x493	0x00	Driver ID, high byte
0x495	0x0C	No of bytes used
0x487		CRC

The low four bytes contain the ASCII text “IPAH” this signifies that the 8004 carrier board supports the 8MHz and 32MHz IP interfaces.

PRODUCT SPECIFICATIONS

Power Requirements
+5V @ 600mA typical
+12V @ 30mA
-12V @ 30mA
+3.3V @ approx 10mA
Additional power maybe consumed by Industry Packs.

Operating Temperature Range
0 to +45 deg Celsius ambient.

Mechanical
6U single width VME module with access to 5 row P0, P1 and P2 connectors.

IP Memory Mapping
VME Access Single A32:D32, D16, D8 (EO) AM Codes: 09h and 0Dh.
VME Access BLT A32:D32, D16, D8 (EO) AM Codes: 0Bh and 0Fh.
VME Access MBLT A32:D64 AM Codes: 08h and 0Ch

IP I/O Mapping
VME Access A16:D16:D8 (EO) AM Codes: 29h and 2Dh.
VME Access A24:D16:D8 (EO) AM Codes: 39h and 3Dh.

Front Panel Indicators and Inputs

'VME'	LED (green)	Illuminates for a minimum of 20msecs whenever the module is accessed via the VME bus.
'Not Configured	LED (blue)	Indicates the state of the VME module during hot swap operation.
IP ACK	4 LED's (red)	Indicate when an IP card has sent an ACK.

Front Panel Connectors

Inhibit Input to supply common IP sites
Single TTL input. This input has a 10K pull-up resistor to 3.3Volt supply.
Connector type: LEMO '00'

Go Single output. This output may be connected by a jumper to the Inhibit input signal for propagation of Inhibit from carrier to carrier.
Connector type: LEMO '00'

VME64x PIN ASSIGNMENTS

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	IODO1	P0.B01	IOD02	P0.C01	IOD03	P0.DO1	IOD04	P0.E01	IOD05	P0.F01	GND
P0.A02	IOD06	P0.B02	IOD07	P0.C02	IOD08	P0.D02	IOD09	P0.E02	IODlO	P0.F02	GND
P0.A03	IOD11	P0.B03	IOD12	P0.C03	IOD13	P0.D03	IOD14	P0.E03	IOD15	P0.F03	GND
P0.A04	IOD16	P0.B04	IOD17	P0.C04	IOD18	P0.D04	IOD19	P0.E04	IOD20	P0.F04	GND
P0.A05	IOD21	P0.B05	IOD22	P0.C05	IOD23	P0.D05	IOD24	P0.E05	IOD25	P0.F05	GND
P0.A06	IOD26	P0.B06	IOD27	P0.C06	IOD28	P0.D06	IOD29	P0.E06	IOD30	P0.F06	GND
P0.A07	IOD31	P0.B07	IOD32	P0.C07	IOD33	P0.D07	IOD34	P0.E07	IOD35	P0.F07	GND
P0.A08	IOD36	P0.B08	IOD37	P0.C08	IOD38	P0.D08	IOD39	P0.E08	IOD40	P0.F08	GND
P0.A09	IOD41	P0.B09	IOD42	P0.C09	IOD43	P0.D09	IOD44	P0.E09	IOD45	P0.F09	GND
P0.A10	IOD46	P0.B10	IOD47	P0.C10	IOD48	P0.D10	IOD49	P0.E10	IOD50	P0.F10	GND
P0.A11	IOC01	P0 B11	IO002	P0.C11	IOC03	P0.D11	IOC04	P0 E11	IOC05	P0.F11	GND
P0.A12	IOC06	P0.B12	IO007	P0.C12	IOC08	P0.D12	IOC09	P0.E12	IOC10	P0.F12	GND
P0.A13	IOC11	P0.B13	IO012	P0.C13	IOC13	P0.D13	IOC14	P0.E13	IOC15	P0.F13	GND
P0.A14	IOC16	P0.B14	IO017	P0.C14	IOC18	P0.D14	IOC19	P0.E14	IOC20	P0.F14	GND
P0.A15	IOC21	P0.B15	IOC22	P0.C15	IOC23	P0.D15	IOC24	P0.E15	IOC25	P0.F15	GND
P0.A16	IOC26	P0.B16	IO027	P0.C16	IOC28	P0.D16	IOC29	P0.E16	IOC30	P0.F16	GND
P0.A17	IOC31	P0.B17	IO032	P0.C17	IOC33	P0.D17	IOC34	P0.E17	IOC35	P0.F17	GND
P0.A18	IOC36	P0.B18	IO037	P0.C18	IOC38	P0.D18	IOC39	P0.E18	IOC40	P0.F18	GND
P0.A19	IOC41	P0.B19	IO042	P0.C19	IOC43	P0.D19	IOC44	P0.E19	IOC45	P0.F19	GND

P0 pin assignments

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	+5V	P1.Z32	GND

P1 Pin Assignments

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	IOB41	P2.B01	+5V	P2.C01	IOB42	P2.D01	IOC47	P2.Z01	IOC46
P2.A02	IOB43	P2.B02	GND	P2.C02	IOB44	P2.D02	IOC48	P2.Z02	GND
P2.A03	IOB45	P2.B03	N/C	P2.C03	IOB46	P2.D03	IOC50	P2.Z03	IOC49
P2.A04	IOB47	P2.B04	A24	P2.C04	IOB48	P2.D04	IOB0l	P2.Z04	GND
P2.A05	IOB49	P2.B05	A25	P2.C05	IOB50	P2.D05	IOB03	P2.Z05	IOB02
P2.A06	IOA01	P2.B06	A26	P2.C06	IOA02	P2.D06	IOB04	P2.Z06	GND
P2.A07	IOA03	P2.B07	A27	P2.C07	IOA04	P2.D07	IOB06	P2.Z07	IOB05
P2.A08	IOA05	P2.B08	A28	P2.C08	IOA06	P2.D08	IOB07	P2.Z08	GND
P2.A09	IOA07	P2.B09	A29	P2.C09	IOA08	P2.D09	IOB09	P2.Z09	IOB08
P2.A10	IOA09	P2.B10	A30	P2.C10	IOA10	P2.D10	IOB10	P2.Z10	GND
P2.A11	IOA11	P2.B11	A31	P2.C11	IOA12	P2.D11	IOB12	P2.Z11	IOB11
P2.A12	IOA13	P2.B12	GND	P2.C12	IOA14	P2.D12	IOB13	P2.Z12	GND
P2.A13	IOA15	P2.B13	+5V	P2.C13	IOA16	P2.D13	IOB15	P2.Z13	IOB14
P2.A14	IOA17	P2.B14	N/C	P2.C14	IOA18	P2.D14	IOB16	P2.Z14	GND
P2.A15	IOA19	P2.B15	N/C	P2.C15	IOA20	P2.D15	IOB18	P2.Z15	IOB17
P2.A16	IOA21	P2.B16	N/C	P2.C16	IOA22	P2.D16	IOB19	P2.Z16	GND
P2.A17	IOA23	P2.B17	N/C	P2.C17	IOA24	P2.D17	IOB21	P2.Z17	IOB20
P2.A18	IOA25	P2.B18	N/C	P2.C18	IOA26	P2.D18	IOB22	P2.Z18	GND
P2.A19	IOA27	P2.B19	N/C	P2.C19	IOA28	P2.D19	IOB24	P2.Z19	IOB23
P2.A20	IOA29	P2.B20	N/C	P2.C20	IOA30	P2.D20	IOB25	P2.Z20	GND
P2.A21	IOA31	P2.B21	N/C	P2.C21	IOA32	P2.D21	IOB27	P2.Z21	IOB26
P2.A22	IOA33	P2.B22	GND	P2.C22	IOA34	P2.D22	IOB28	P2.Z22	GND
P2.A23	IOA35	P2.B23	N/C	P2.C23	IOA36	P2.D23	IOB30	P2.Z23	IOB29
P2.A24	IOA37	P2.B24	N/C	P2.C24	IOA38	P2.D24	IOB31	P2.Z24	GND
P2.A25	IOA39	P2.B25	N/C	P2.C25	IOA40	P2.D25	IOB33	P2.Z25	IOB32
P2.A26	IOA41	P2.B26	N/C	P2.C26	IOA42	P2.D26	IOB34	P2.Z26	GND
P2.A27	IOA43	P2.B27	N/C	P2.C27	IOA44	P2.D27	IOB36	P2.Z27	IOB35
P2.A28	IOA45	P2.B28	N/C	P2.C28	IOA46	P2.D28	IOB37	P2.Z28	GND
P2.A29	IOA47	P2.B29	N/C	P2.C29	IOA48	P2.D29	IOB39	P2.Z29	IOB38
P2.A30	IOA49	P2.B30	N/C	P2.C30	IOA50	P2.D30	IOB40	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	N/C	P2.Z31	+3.3V
P2.A32	Out+5V	P2.B32	+5V	P2.C32	Out+5V	P2.D32	+5V	P2.Z32	GND

P2 pin assignments

Denotes pins with thickened tracks which can be used for power inputs

Note:
'Out+5V' is provided by the 8004 board and can be put on to the pins by fitting jumper J4.