# EGG 1232

# MICROLOK INTERLOCKING SIMULATION SYSTEM (MISS) DESIGN GUIDELINES

Version 1.2

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# Document control

Version	Date	Summary of change
1.0	14 September 2010	New document.
1.1	1 November 2010	2.5.3.5 Control Panels: reworded for NX as well as OCS panels; 2.5.3.7 OCS added to title to read OCS Route control Function; 2.5.3.8 new section titled NX Route control Function to describe behaviour of screen-based buttons for commence and finish functionality; 1 Reference documents – QSDP68 added; 2.1 new paragraph added re MISS data and QSDP 68.
1.2	27 November 2012	Apply correct document template for Guideline type document. Renumber TMG E1232 to EGG 1232 to comply with updated TMA 400 Engineering Publications Manual.

# Summary of changes from previous version

Summary of change	Section
Added Introduction as section 1 containing 1.1 Purpose, 1.2 Scope and 1.3 Referenced Documents.	1
Sections 2.2.1 (A) renumbered to 2.2.1.1 and section 2.2.1 (B) renumbered to 2.2.1.2	2.2.1
Description added to figure captions	2

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# 1 Introduction

# 1.1 Purpose

This specification is applicable to the Microlok Interlocking Simulation System (MISS).

# 1.2 Scope

This specification provides guidance on the configuration, testing and operation of the MISS.

# **1.3 Referenced Documents**

The following documents provide supporting information or referenced information to that provided by this document.

US&S Documents

- Microlok Interlocking Simulation System Users Manual
- Microlok Interlocking Simulation System Getting Started Guide
- Microlok Interlocking Simulation System Trakplan User Manual
- Microlok II System Description SM-6800A
- Microlok II Hardware Installation SM-6800B
- Microlok II System Start up, Trouble Shooting and Maintenance SM-6800C
- Microlok II System Application Logic Programming Guide SM-6800D
- Microlok II Programmable Controller Platform Safety Application Issues

RailCorp Documents

- Design of Microlok II Interlockings SPG 1230
- Microlok File Control, Microlok Data Design and Factory Acceptance Test QSDP16
- Re-Testing of Microlok Data QSDP31
- Checking of Microlok Circuit and Data Designs QSDP33
- Application of MISS, Replay & Emergency Control Software QSDP68

# 2 MICROLOK INTERLOCKING SIMULATION SYSTEM

# 2.1 General

The MISS software and hardware has been developed to allow for the simulation and testing of the application data for Microlok II based signal interlockings. This system allows the testing of the functional characteristics of each interlocking in an office/test room environment. It also allows for the evaluation of the performance of the interlocking logic.

The system includes a simulation computer running the MISS software and two specially designed Microlok II cardfiles.

There is no provision for Microlok II I/O cards in the MISS hardware so there is a requirement to modify the Microlok II application logic of the vital processors to re-route the I/O from the physical cards to the serial communication ports to allow this I/O to be simulated.

Wherever possible "turn around" logic is to be provided in the MISS configuration files to allow data bits to be automatically generated from an output to an input as required.

This document describes a level of simulation functionality that is required for all projects. Reduced functionality, such as lack of coloured route set lines or tabulated I/O instead of geographically arranged I/O are not acceptable.

Additionally, MISS data is to be suitable for control and replay purposes as required by QSDP68.

# 2.2 Hardware Configuration

# 2.2.1 General

### 2.2.1.1 Microlok Master-slave Style Configurations

The MISS hardware includes a simulation computer mounted in a 19-inch computer rack. This computer may be connected to up to 5 monitors.

The computer rack also includes Microlok II cardfiles, power supply units, a Cyclades 16 port serial I/O expansion unit and Traktronics electronic patch panels, each with 16 port connections.

There are Traktronics electronic patch panels suitable for an RS232 hardware interface and an electronic patch panel suitable for an RS423/485 hardware interface.

The simulation computer is connected to the Microlok II CPU cards via the electronic patch panels. Each of the 4 ports associated with the Microlok II CPU cards are wired to the electronic patch panels and the connectivity between each port is configured via the MISS software.

Drawings showing the serial port wiring from the simulation computer to the electronic patch panels and from the Microlok II CPU cards to the electronic patch panels can be found in the appendix. These drawings will need to be referred to when preparing the MISS signal interlocking configuration drawing.

# 2.2.1.2 Microlok Peer to Peer Configurations

The MISS hardware for testing systems that use peer to peer protocols include RS400 switches. This permits the RS400 data to also be tested, although in a conglomerated file rather than the separated files that would be used in the field installation. This document does not specifically address the peer to peer workstation. However, the testing functionalities described here-in are to be applied to all applications.

In addition to the RS400 switches, instead of the Cyclades expansion unit used on the Master-Slave configuration, the peer-peer simulator has a MOXA serial port expander. The cardfiles are wired for up to 18 CPU cards.

# 2.2.2 Test Configurations

The testing configuration of every Signal Interlocking to be tested will be different. Prior to the development of the MISS configuration files it is recommended that a MISS configuration drawing shall be produced to confirm all hardware requirements and the necessary serial port connections required for the simulation.

An example of a MISS configuration drawing can be found in Appendix B.

# 2.2.2.1 RailCorp Testing Facilities

Signal Design has (in 2010) two MISS testing facilities. One MISS is a dedicated masterslave system, while the other can be configured to operate either as a peer-to-peer system or as a master-slave system

These testing facilities are available for Design Integrity testing of Microlok II based signal interlockings.

The testing facilities includes a separate desktop PC running the Microlok II tools software, which may be used to interrogate the diagnostics of the Microlok CPU cards and monitor the application data variables as required. Where there is a requirement to interrogate more than one CPU card during testing additional desktop PCs or laptop PCs may be used.

NOTE: The simulation computer also includes the Microlok II tools software and a port connection is available for use to also interrogate the diagnostics of the Microlok II CPU cards.

Where the testing configuration includes connection to an ATRICS computer, this computer may be connected to any spare port of the electronic patch panels. The configuration of the files should not be changed after testing. Therefore the settings used for the simulation should be set to the configuration used on site.

A photo of the testing facilities is shown in Figure 1.



Figure 1 RailCorp MISS Test Facility

# 2.3 Software Configuration

# 2.3.1 General

MISS.exe is the executable program required to run the Microlok Interlocking Simulation System. Generally this software would only be run from the simulation computer in the Microlok test room.

Trakplan.exe is the executable program required for producing the Track Side Panel and the Mimic/Control Panel. These panels are used by MISS to simulate and control the interlocking via a mouse or keyboard interface. This software is required to be installed on the Design Engineers PC for the development of the necessary panels.

Note: When commencing a new simulation, known versions of MISS.exe and Trakplan.exe shall be used and the version recorded in the test results. The latest versions should be used where possible to maximise the features and functionality.

# 2.3.2 Configuration Files

#### 2.3.2.1 General

The following configuration and data base files are required to run the simulation system:

- MISSCOM.mdb
- CONTROL PANEL.mdb
- TRACK PANEL.mdb
- PORT\_INFO.csv
- ePATCH.csv
- BIT LIST.csv

#### 2.3.2.2 MISSCOM.mdb

The MISSCOM.mdb file is a data base file that includes a table called MissStatn Tbl is used. An example of this table is shown in Figure 2

Microsoft A	lccess	i - [MissStatnTbl : Table]			
🛄 <u>F</u> ile <u>E</u> dit	⊻iew	Insert Format <u>R</u> ecords <u>T</u> ools	<u>W</u> indow <u>H</u> elp		
Station	_ID	Station_Name	Db_File_Name	Mimic_Db_Name	Track_Db_Name
	1	LEIGHTONFIELD	ANYNAME.mdb	LEIGHTONFIELDCP.MDB	LEIGHTONFIELDTP.MDB
(AutoNu	mber)				

#### Figure 2 'MissStatn' table

Generally the Station\_ID field will always remain as 1.

The "Station\_Name" field is to be the name of the interlocking location.

The "Db\_File\_Name" field is generally not used but requires an entry in the field so ANYNAME.mdb is recommended.

The "Mimic\_Db\_Name" field contains the name of the data base file created for the Mimic/Control Panel. If there is no requirement for this panel the field shall be blank.

The "Track\_Db\_Name" field contains the name of the data base file created for the Track Panel. If there is no requirement for this panel the field shall be blank.

Once a project folder is created, the files to which MISSCOM refers are located within that folder. This prevents them from becoming confused with the files of other projects. If default names are used for all files, MISSCOM.mdb never requires to be edited. However, should it be necessary to edit the MISSCOM.mdb file. Microsoft ACCESS 97 must be used for the editing.

#### 2.3.2.3 CONTROL PANEL.mdb

The CONTROL PANEL.mdb file is created where the testing configuration requires a Control Panel for the sending of controls and displaying of indications to simulate the final Control Panel. This file can be modified using the TrakPlan.exe program.

NOTE: Where the final Control Panel is ATRICS it would be preferred that an ATRICS PC is used when testing the interlocking during FAT. However where the ATRICS design is not available the MISS Control Panel will be required.

### An example of a Control Panel is shown in Figure 3



Figure 3 Control Panel

# 2.3.2.4 TRACK PANEL.mdb

The TRACK PANEL.mdb file is created where the testing configuration requires a Track Side Panel for the simulation of the trackside equipment and where required the indication of signal aspects etc. This file can be modified using the TrakPlan.exe program.

An example of a Track Side Panel is shown in Figure 4



Figure 4 Track Side Panel

#### 2.3.2.5 PORT INFO.csv

The PORT INFO.csv file (comma separated variable file) provides a description of the serial port connections and protocols for each of the links that are required in the simulation configuration. The information required in this file is taken directly from the Microlok data and the MISS configuration drawing designed for the interlocking under test. An example of an interlocking MISS configuration drawing can be found in the appendix.

An example of this file is shown in Figure 5

	licrosoft Excel - po	rt_info								
1	File Edit View Ins	ert F <u>o</u> rmat <u>T</u> ools <u>D</u> ata <u>W</u> in	dow <u>H</u> elp							
	A36 🔻	=								
	A	В	С	D	E	F	G	Н	1	J
1	From Processor	To Processor	Protocol	Station Address	PC Port Number	Baud Rate	Data Bits	Parity	Stop Bits	Rts Mode
2	PCSIM	ePatch	ePatch	999	3	9600	8	None	1	DISABLE
3	PCSIM	TRACK PANEL	master	999	14	19200	8	None	1	DISABLE
4	PCSIM	CONTROL PANEL	master	999	15	19200	8	None	1	DISABLE
5	PCSIM	ATRICS	slave	50	4	9600	8	None	1	DISABLE
6	PCSIM	SP27.4	Vmaster	93	5	9600	8	None	1	DISABLE
7	PCSIM	SP26.8	Vmaster	90	6	9600	8	None	1	DISABLE
8	PCSIM	SP118	Vmaster	86	7	9600	8	None	1	DISABLE
9	PCSIM	SP107	Vmaster	83	8	9600	8	None	1	DISABLE
10	PCSIM	SP91	Vmaster	80	9	9600	8	None	1	DISABLE
11	PCSIM	SP81	Vmaster	76	10	9600	8	None	1	DISABLE
12	PCSIM	SP69	Vmaster	73	11	9600	8	None	1	DISABLE
13	PCSIM	SP61	Vmaster	70	12	9600	8	None	1	DISABLE
14 15	PCSIM	SP55_LEIGHTONFIELD	Vmaster	43	13	9600	8	None	1	DISABLE

Figure 5 PORT INFO.csv file

The "From Processor" field is generally always PCSIM (simulation PC)

The "To Processor" field includes the names of the Bit List files that have been created for the simulation configuration. The entry "ePatch" is a standard requirement.

The "Protocol" field describes the communication protocol of that serial link. For example "Vmaster" defines a Microlok Master protocol and "master" defines a Genisys Master protocol. "ePatch" defines the protocol for the ePatch link.

Note that the "Protocol" field is the protocol used at the OTHER end of the link. "Vmaster" means the Microlok on the other end is the Master end of a vital link (i.e. the MISS slave). The same situation applies for the non-vital links. Normally the interlocking is a Genisys slave of the control system, so the PORT INFO needs to state "slave", even though the MISS is the Master of the link.

The "Station Address" field describes the serial link address for that particular serial link as provided in the Microlok data. Where an address of 999 is shown, this number may be any number below 999 that has not been used in the simulation configuration.

The "PC Port Number" field describes the MISS PC port number used for that communication link. Port numbers 1 and 2 may not be used and port number 3 is generally always used for the ePatch units. Reference would need to be made to the MISS circuits for the port numbers available for use. These circuits can be found in the appendix.

The "Baud Rate", "Data Bits", "Parity" and "Stop Bits" fields describes the appropriate value for each communication link. Where the link is not related to the Microlok data directly, a value of 9600 or 19200 may be used.

The "Rts Mode" is generally set to DISABLE for all communication links.

### 2.3.2.6 ePatch.csv

The ePatch.csv file defines the ePatch port connections for each serial link in the testing configuration that is required to pass through the ePatch units.

It is recommended that a MISS configuration drawing, (as shown in the appendix), is produced for each interlocking under test. This drawing shall show the configuration of the Microlok CPU cards and the port connections required for the simulation.

Reference would need to be made to the MISS circuits when producing the MISS configuration drawing.

An example of the ePatch file is shown in Figure 6.

<u></u>	File Fait Alen	٧	Insert For	mat <u>L</u> ools <u>D</u> ata	Window He	9p
	A36 🔄	-	=			
	A			В	С	D
1	From Port	-	To Port			
2	3	35		38		
3		36		3		
4	E	50		6		
5	6	52		9		
6	6	54		12		
7	6	56		15		
8	ŧ	58		16		
9	E	60		19		
10	6	52		22		
11	6	64		25		
12	3	34		28		
13	3	37	2,5,8,11,	14,18,21,24,27		
14			-32-2222-32			

The port numbers shown in the table are the port numbers of the ePatch panels, numbers 1 to 16 apply to ePatch panel 1 and ports 17 to 32 apply to ePatch panel 2 and port numbers 33 to 48 apply to ePatch panel 3 etc.

The "From Port" field is generally the master port of the link.

The "To Port" field is generally the slave port of the link.

These entries do not need to be in any particular numeric order.

Line 13 indicates an example of a multi-drop link; note the use of a comma for each of the slave ports of that multi-drop link.

NOTE: There is a limitation of 16 links that can be defined with the current hardware configuration. Where the interlocking under test requires a greater amount of links, any link that is a direct serial connection between two Microlok II CPU card ports may be connected together directly, bypassing the ePatch units.

# 2.3.2.7 Bit List.csv

Generally a separate Bit List file is created for each connection as defined in the PORT\_INFO.csv file. Each link is usually related to a Microlok serial link and the information in each bit list file is taken from the relevant Microlok data. These bit list files include the listings of the inputs and outputs of the serial link and may include "Auto-Configuration" or "Turn Around" logic for simulation purposes.

A bit list file is also generally created for each simulation panel, the Track Panel and the Control Panel. These files contain any "intermediate bits" that are required to be created to aid the auto-configuration or simulation of the interlocking.

Section 2.3.3 describes the auto-configuration logic in more detail.

	1icrosoft Excel -	SP27.4						
	<u>File E</u> dit <u>V</u> iew	Insert Format Tools	Data Window	Help				
_	A29 🔻	=						
	A	В	С	D	E	F	G	Н
1	Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	OnDelay	OffDelay	
2	OUT	27.4HP	1	0	27.4HR	0	0	
3	OUT	27.4HDP	2	0	27.4HDR	0	0	
4	OUT	27.4DP	3	0	27.4DR	0	0	
5	OUT	27.4NGPZ	4	1	~27.4HR*~27.4HDR*~27.4DR	0	0	
6	OUT	27.4VNP	5	0	~27.4VR*27.4VNRLINK	0	0	
7	OUT	27.4VRP	6	0	27.4VR*27.4VRRLINK	0	0	
8	OUT	102HZ	7	0		0	0	
9	OUT	102HDZ	8	0		0	0	
10	OUT	26.7HZ	9	0		0	0	
11	OUT	L17.1AT	10	1		0	0	
12	OUT	L19.8DT	11	1		0	0	
13	OUT	27.4AT	12	1		0	0	
14	OUT	26.7BT	13	1		0	0	
15	OUT	SPARE	14	0		0	0	
16	OUT	SPARE	15	0		0	0	
17	IN	27.4HR	1	0		0	0	
18	IN	27.4HDR	2	0		0	0	
19	IN	27.4DR	3	0		0	0	
20	IN	27.4VR	4	0		0	0	
21	IN	27.4VCSR	5	0		0	0	
22	IN	25.5ABTPR	6	0		0	0	
23	IN	26.7ATPR	7	0		0	0	
24	IN	26.1ABTPR	8	0		0	0	
25	IN	SPARE	9	0		0	0	
26	IN	SPARE	10	0		0	0	
27								

An example of a Bit List file is shown in Figure 7.

#### Figure 7 Bit List file

The "Direction" field defines the bit as an input received from the MISS computer or an output sent to the MISS computer.

The "Bit Name" field defines the bit name, usually taken from the Microlok data, and is the name to be used if required in the MISS panel logic.

The "Bit Offset" field defines the order of the bits; the bit offset is started from 1 for both the inputs and outputs.

The "Bit Value" field defines the output bit value as 1 or 0 at start up. Input bits must have a value of 0.

The "Auto Config Bit" field allows logic to be provided for the setting or clearing of that bit value. This field requires standard Microlok Boolean syntax; any bits defined in the Bit List files may be used. Note that the "Auto Config Bit" field does not ese exactly the same Boolean syntax as the other values in that it must not contain spaces and does not support exclusive or (XOR  $^{\text{A}}$ ).

The "Off Delay" and "On Delay" fields are used to create a slow to clear or slow to set functions if they are required to be applied to that bit. (For example- point setting)

# 2.3.3 Auto-Configuration

The Auto-Configuration function is applied to various functions to allow for the simulation of the operation and indication of the field equipment. The control bits normally used as outputs to operate field equipment (relays) are used in the "Auto Config Bit" field of the Bit List files to manipulate the inputs back into the signal interlocking automatically, simulating the operation of the field equipment.

Where there is a requirement for a disconnect point or link for testing purposes, such as breaking Points detection etc. an intermediate bit is created to simulate a link. These bits are defined in a separate Bit List file (Track Panel.csv). It is recommended that a separate Bit List file be created for both the Track Panel and the Control Panel.

# 2.3.3.1 Signal Auto-Configuration Functions

To simulate the operation of relay driven signals the signal control bits that would normally drive the output relays are used in turn around logic and brought back into the interlocking. Data is provided in the "Auto Config Bit" field for each input associated with the signal as shown in Table 1

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	112MAHP		0	112MAHR	0	0
OUT	112MBHP		0	112MBHR	0	0
OUT	112HDP		0	112HDR	0	0
OUT	112DP		0	112DR	0	0
OUT	112SAHP		0	112SAHR	0	0
OUT	112SBHP		0	112SBHR	0	0
OUT	112NGPZ		0	~112MAHR*~112MBH R*~112SAHR *~112SBHR	0	0

#### Table 1

NOTE: The RGKR function is usually created within the Microlok data.

If there is a requirement to display actual signal aspects on the Track Panel the logic associated with this is created within the Track Panel screen design. This is covered later in the document.

#### 2.3.3.2 Trainstop Auto-Configuration Functions

To simulate the operation of the Train Stop the control bit that would normally drive the VR output relay is used in turn around logic and brought back into the interlocking. Data is provided in the "Auto Config Bit" field for each input associated with the Train Stop detection as shown in Table 2

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	112VNP		0	~112VR*112VNRLINK	0	0
OUT	112VRP		0	112VR*112VRRLINK	0	0

#### Table 2

NOTE: The logic in the "Auto Config Bit" field includes intermediate bits named VRRLINK and VNRLINK. These bits are used to enable the breaking of the Train Stop detection for testing purposes. These intermediate bits are created in the "Track Panel" Bit List file as shown in Table 3

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	112VRRLINK		1		0	0
OUT	112VNRLINK		1		0	0

#### Table 3

NOTE: The Bit Value is set at 1 due to the link or switch being normally closed. The manipulation or opening of this link is carried out via a drop-down menu on the Track Panel.

# 2.3.3.3 Track Auto-Configuration Functions

To simulate the operation of Track Circuits the input bit that is brought into the interlocking is manipulated (or opened and closed) via a drop-down menu on the Track Panel. The entry in the "Bit Value" field is set at 1 to ensure all tracks are simulated as un-occupied at the start up of the interlocking. The data is created in the Bit List file as shown in Table 4.

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	99BT		1		0	0
OUT	107CT		1		0	0
OUT	107BT		1		0	0
OUT	107AT		1		0	0

Та	bl	е	4
		-	-

#### 2.3.3.4 Points Auto-Configuration Functions

To simulate the operation of Points the control bits that would normally drive the Points output relays (NWR, RWR & IR) are used in turn around logic and brought back into the interlocking. Data is provided in the "Auto Config Bit" field for each input associated with the Points as shown in Table 5

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	225ANKR		0	225NWZR*225ANLINK	0	0
OUT	225ARKR		0	225RWZR*225ARLINK	0	0
OUT	225BNKR		0	225NWZR*225BNLINK	0	0
OUT	225BRKR		0	225RWZR*225BRLINK	0	0
OUT	225EOL		1		0	0
OUT	225ICR		0	~225IR	0	0

#### Table 5

To simulate the operation of the EOL the input bit that is brought into the interlocking is manipulated (or opened and closed) via a drop-down menu on the Track Panel. The entry in the "Bit Value" field is set at 1 to ensure the EOL is simulated as closed at the start up of the interlocking.

To simulate the operation of the Points Isolation Relay the control bit that would normally drive the IR output relay is used in turn around logic and brought back into the interlocking.

NOTE: The logic in the "Auto Config Bit" field for the NKR and RKR functions include "link" intermediate bits. These bits are used to enable the breaking of the Point detection for testing purposes. These bits are created in the "Track Panel" Bit List file as shown in Table 6.

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	225ANLINK		1		0	0
OUT	225ARLINK		1		0	0
OUT	225NWZR		0	(225NWR*225IR+225 NWZR*~225RWR)	3000	
OUT	225RWZR		0	(225RWR*225IR+225 RWZR*~225NWR)	3000	

#### Table 6

NOTE: The Bit Value for the ANLINK and ARLINK is set at 1 to simulate the links or switches being normally closed. The manipulation (or opening) of these links is carried out via a drop-down menu on the Track Panel. Similarly for the BNLINK and BRLINK.

An "On Delay" of 3000 milliseconds has been applied to the NWZR and RWZR bits to simulate the transition of the points operation to be more closely simulated.

NOTE: that it is necessary to test each end of each detection separately to confirm that each input bit is correctly in the data. However, once this is proven, only one of the normal and one of the reverse need to be manipulated for control table testing.

Miscellaneous Auto-Configuration Functions

Miscellaneous functions such as Power Supply Units or Diversity Link Controllers where there are input bits that are brought back into the interlocking and are included in the Bit List file, have the entry in the "Bit Value" field is set at 1 to ensure they are simulated as true at the start up of the interlocking.

# 2.3.4 Hot Standby Configurations

Hot Standby configurations generally include the duplication of Microlok master processors. As the application data is duplicated in each processor it is considered not necessary to test the duplicated data in a dual hot standby configuration on a MISS.

Field testing needs to be carried out as described in SPG 1230.

Should there be a requirement to specifically test Hot Standby application logic it is recommended that an ATRICS computer be included in the testing configuration. This is to avoid the need to produce a complex MISS Control Panel.

Where a MISS Control Panel is to be provided there would be a requirement to include a separate Bit List file for each of the 2 master processors and the bits names in these files would need to be different to allow the separation of the controls and indications for each master processor in the MISS data base.

The MISS Track Panel produced for a Hot Standby configuration would be as normal due to the testing only being required to single slave processors.

# 2.4 Miscellaneous Tips

- a) Ensure the same version of Microsoft Access running on the MISS computer is used when creating the required database files. Otherwise there will need to be a requirement to convert the databases before MISS will run. (MS ACCESS 97)
- b) It is recommended that the Design Engineer copies and modifies the MISS files of an existing project, rather than designing from new "blank" files.
- c) The file extension ".mdb" should be included on the file names specified in the MISSCOM.mdb file.
- d) Consider assigning CPS.STATUS to LED.8 (where not already used) in the Microlok II application data to allow the tester to more easily confirm the CPU functionality.
- e) Consider assigning the MISS port status bits to LEDs 1-4 as provided in the Microlok II application data.
- f) The "Track Plan" panel would normally be designed first and copied and renamed to the "Control Panel"

Copying the track panel to make the control panel does not save very much time in preparation. One must return to the control map for every grid map item and change the logic. This presents the risk that some of the entries will be missed. For example a track item on the control panel is driven by the "field" bit as used on the track panel rather than using the control system indication bit.

Where multiple bitmaps have been stacked in a single grid square to build a complex object (e.g. signal + trainstop), one cannot delete a single bitmap. One needs to keep all or delete all.

Track panel may be spread out to fit all the objects (e.g. 6-light signal with shunts and route indicator), but the control panel does not need to be spread out as much. The more compact the control panel can be drawn, the easier it is to be able to view the whole picture.

g) Flashing indications may be provided in the screen design by creating a FLASH bit and utilising the "On Delay" and "Off Delay" fields in the Bit List files. However this will cause the MISS log file to be almost unusable. (Hence this is not recommended)

The use of flashing indications can be very useful.

Should it be necessary to review the log, it can be opened using MS Excel and the flash bits that tend to flood the file can be filtered out to leave the important bits visible.

- h) The PC Port Number in the Port\_Info file should start with port 3 as this is actually port 1 of the 16 port expansion unit. Ports 1 and 2 of the MISS computer are available for other uses, such as for the Microlok II Tools software.
- i) MISS bit names are case sensitive.
- j) The I/O from the Microlok application data can be copied into the Bit List file. The command "Find and Replace" can be used to separate the I/O bits into

separate lines. For example, find "," and replace with "시" (control L), will replace the comma separation with line returns.

k) A blank bitmap can be placed in position on the screen design for the route indication aspects of signals, and this blank bitmap is "substituted" with a route indication character when the bit (Shunt HR) is true.

# 2.5 Screen Design (Trakplan.exe)

# 2.5.1 General

The screen design is to be carried out using the Trakplan.exe program. This software may be used to create and modify the Track Panel and/or Control Panel, depending on the testing configuration and requirements.

The screen design may be carried out on any desk top PC or laptop loaded with the required software.

The screen design includes the production of a screen layout using individual bitmap drawings. These are symbols created specifically for this purpose. A grid may be turned on or off as required to aid the screen design.

Logic may be applied to individual symbols on the screens to either change the colour or shape of the symbol, depending on the value of the bit assigned to that symbol. This is carried out utilising the "Indication Map" command.

Drop-down menus may be created to allow the manipulation of the bits defined in the Bit List files. This is carried out utilising the "Control Map" command.

Text may be placed on the screen using the "Text" command. The text may be inserted in any font, style, size or colour as required. Clicking the mouse on the screen and selecting the Text command will allow the placement of text on the screen. Note that the text will be placed from the point that the mouse was clicked on the screen and aligned to the left.

# 2.5.2 Bitmaps

Bitmaps are drawings of individual symbols that may be placed on a grid of the Track Panel or Control Panel screen design. Multiple bitmaps may be placed on the same grid to form a more complex symbol. (This is referred to as a Grid Map) For example a signal symbol on the Track Panel is made up of separate bitmaps, one bitmap for each signal lamp and others for the signal post etc.

The bitmaps are created and modified using the Microsoft "Paint" software.

The MISS bitmaps are stored in a separate folder "Bitmaps" on the simulation computer.

The bitmap drawings are generally numbered from 100 - 1000 and any spare number may be used for a new bitmap drawing.

It is essential that Design Engineers do not create duplicate bitmaps or bitmaps with identical filenames for different projects. For this reason it is proposed that a master bitmap folder be provided on the network to ensure only standard bitmaps are used and stored in this folder. The Bitmap folder on the simulation computer shall be identical to this.

To ensure consistency in presentation Design Engineers shall only use bitmaps from the network folder. Any new bitmaps to be created shall be consistent with current existing bitmaps and are to be saved in the monochrome format only.

Following the creation of the new bitmap it shall be the Design Engineers responsibility to ensure the new bitmap is copied into both the network and simulation computer Bitmap folder.

When the Track Panel or Control Panel is being created the bitmaps are placed on the screen by selecting the bitmap from the bitmap palette and dropping it in the required grid on the screen. The bitmap palette is a scrollable region at the bottom of the screen design window seen when "Trakplan.exe" is running.

# 2.5.3 Track Panels

Where there is a requirement to simulate the field equipment during design testing a Track Panel may be designed using the Trakplan.exe software.

This panel may show the layout of the track arrangements, including Points, Signals, Train Stops, Platforms, and Track Circuits. Additional indications can be provided such as interface functions, warning lights, individual signal aspects, lamp failures, and EOL's.

This panel can allow the manipulation of functions through drop-down menus, including track circuits, train stop detection, point detection, and other miscellaneous functions as required.

### 2.5.3.1 Points

Point detection is indicated on the Track Panel for each set of Points. An indication is displayed separately for both normal and reverse points detection, and a yellow indication is displayed when the detection is made. Loss of detection will result in a grey indication.



An indication is also provided for the Points EOL and a yellow

indication is displayed when the EOL detection is made. Loss of detection will result in a grey indication.

Clicking on the indication and selecting from the drop-down menu may break Point and EOL detection where required.

An example of the logic associated with the Points indication is as shown in Figure 8.



#### Figure 8 Example of the logic associated with the Points Indication

The colour yellow is substituted for the standard bitmap colour when the result of the logic in the Logic Element field is true.

An example of the logic associated with the Points detection control menu is as shown in Figure 9.

ымар	12	1	0	
Add Menu Delete Menu	Ok	Cancel		
Gridmap				
٠				
N 01				
Menu String		Logic Bit		
BREAK NORMAL DETECTION	will set	Logic Bit 225NLink	FALSE	Emulates Pushbutton
Menu String BREAK NORMAL DETECTION Menu String	will set	Logic Bit 225NLink Logic Bit	FALSE	Emulates Pushbutton 🗔
Menu String BREAK NORMAL DETECTION Menu String MAKE NORMAL DETECTION	will set	Logic Bit 225NLink Logic Bit 225NLink	FALSE	Emulates Pushbutton F
Menu String BREAK NORMAL DETECTION Menu String MAKE NORMAL DETECTION Menu String	will set	Logic Bit 225NLink Logic Bit 225NLink	FALSE	Emulates Pushbutton 🗖 Emulates Pushbutton 🗖

Figure 9 Example of logic associated with the Points Detection

For example, when clicking on the Points normal detection indication a menu will appear with 2 options, to make or break the normal detection. Selecting the appropriate option will toggle the logic bit 225NLink true or false.

### 2.5.3.2 Train Stops

Train Stops are indicated on the Track Panel and the symbol is displayed in the raised or lowered position for simulation purposes. The Train Stop symbol is shown as magenta when the detection is made. The centre of the Train Stop symbol changes to magenta to indicate the VR function is true and the Train Stop symbol will be shown in the lowered position when the VRR function is true. The manipulation of the Train Stop detection is carried out by clicking on the Train Stop symbol. A drop-down menu will be displayed where the Train Stop normal or reverse detection can be opened or closed.

🐯 TrakPlan								
Indication Map								
Substitute Bitma	p Substitute (	Color Delete	OK	Cancel		<<	>>	
G Substitute Substitute B Substitute	iridMap itmap do When   itmap when	Displays Logic Element 68VR*68VRRLINK Logic Element Logic Element	Bitmap A in is set	Color as I Substitute Substitute	olor olor olor when olor when	Logic Ele  68VR*68VRRLI Logic Ele  ~68VR*68VNRI	ment NK ment LINK	is set
Substitute	When		is set	Substitute				is set
	Figure 10	D Example of t	he indication	n logic for t	he Train	Stop		

An example of the indication logic for the Train Stop is as shown in Figure 10.

NOTE: The Train Stop normal symbol (bitmap) is substituted by a Train Stop reverse symbol when the VR and VRR LINK functions are true and the symbol colour is shown as magenta when the detection is made. (VNR LINK or VRR LINK) Any loss of detection will result in this symbol displaying the default grey colour.

An example of the menu logic for the Train Stop is as shown in Figure 11.

	1	11	1	- (	
dd Menu	Delete Menu	0k	Cancel		
Gridmap					
١	1enu String		Logic Bit		
BREAK NOF	RMAL DETECTION	will set	68VNRLINK	FALSE	Emulates Pushbutton
	Menu String		Logic Bit		
MAKE NORI	MAL DETECTION	will set	68VNRLINK	TRUE	Emulates Pushbutton
	Menu String		Logic Bit		
BREAK REV	ERSE DETECTION	will set	68VRRLINK	FALSE	Emulates Pushbutton
	Menu String		Logic Bit		
		26 Sec.11 55			

### Figure 11 Example of menu logic for Train Stop

NOTE: The train stop normal or reverse detection functions are toggled, setting the link bit true or false, depending on the menu item selected.

#### 2.5.3.3 Signals

The true form of the signal can be shown on the Track Panel, including the appropriate aspects. This allows the testing to include full aspect sequence simulation.

The logic behind each signal aspect indication is as per the standard signal operating logic, utilising the signal control bits from the Bit List files.



When using the trackplan.csv file, the correctness of the logic needs to be reviewed by a correspondence test before using for the function test.

#### 2.5.3.4 Tracks

Track indications are shown on the Track Panel as grey for track un-occupied and red for track occupied depending on the status of the track circuit bit.

When clicking on a section of the track, a drop-down menu will appear to provide the option to pick or drop that particular track circuit. This will toggle the track circuit output bit.

Route lights are not shown on the Track Panel.

# 2.5.3.5 Control Panels

Where there is a requirement to simulate the Signal Box control panel for design testing a Control Panel may be designed using the Trakplan.exe software.

The design of the panel for a completely new interlocking should allow for indication and control in a similar way to a conventional OCS panel. When there is a project that is required to interface with an existing NX panel, the design should be made to simulate the NX style of panel. These panels should include the layout of the track arrangements, points, signal repeaters, track timers, platforms and track circuits. Additional indications can be provided such as warnings or alarms, auto re-clearing and hot standby functions.

### 2.5.3.6 Points Control Functions

Points detection, Points in Transit and Points Free are indicated on the Control Panel for each set of Points. A yellow indication is displayed when the detection is made, a green indication is displayed when the Points are free and a red indication is displayed when the Points are in transit. Note the Points transit indication does not flash.



An arrow in the centre of the indication set shows the position of the "Points Key", or the last command that was sent, to be displayed. By clicking on the arrow a drop-down menu will be displayed which gives the option to set the Points normal, reverse or centre.

An example of the logic associated with the Points key indications are as shown in Figure 12.



Figure 12 Example of the logic associated with the Points key indications

The arrow symbol is substituted for an alternate bitmap to indicate normal or reverse when the particular logic in the Logic Element field is true.

An example of the logic associated with the Points Key Control menu is as shown in Figure 13.

nap Menu String Logic Bit ial will set [225NKEY IRUE  Emulates Pushbutton  Menu String Logic Bit e will set [225CKEY IRUE  Emulates Pushbutton	dd Menu	Delete Menu	Ok	c Cancel	1	
nap Menu String Logic Bit Ial will set 225NKEY IBUE  Emulates Pushbutton  Menu String Logic Bit e will set 225CKEY IBUE  Emulates Pushbutton						
Menu String Logic Bit Ial will set 225NKEY IRUE ─ Emulates Pushbutton IV Menu String Logic Bit e will set 225CKEY IRUE ─ Emulates Pushbutton IV	0.11					
Menu String Logic Bit al will set 225NKEY TRUE Emulates Pushbutton V Menu String Logic Bit e will set 225CKEY TRUE Emulates Pushbutton V	Gridmap					
Menu String     Logic Bit       Ial     will set     225NKEY     TRUE     Emulates Pushbutton       Menu String     Logic Bit       e     will set     225CKEY     TRUE     Emulates Pushbutton	Đ					
Menu String     Logic Bit       Ial     will set     225NKEY     TRUE     Emulates Pushbutton       Menu String     Logic Bit       e     will set     225CKEY						
Al will set 225NKEY TRUE : Emulates Pushbutton Menu String Logic Bit e will set 225CKEY TRUE : Emulates Pushbutton V						
Menu String Logic Bit e will set [225CKEY] TRUE I Emulates Pushbutton	1	Menu String		Logic Bit		
e Logic Bit 225CKEY TRUE He Emulates Pushbutton	Normal	Menu String	will set	Logic Bit 225NKEY	TRUE	Emulates Pushbutton 🔽
e Will set 1225CKEY I HUE 🛨 Emulates Pushbutton 🗸	l Normal	Menu String	will set	Logic Bit 225NKEY		Emulates Pushbutton 🔽
	Normal	Menu String Menu String	will set	Logic Bit 225NKEY Logic Bit	TRUE	Emulates Pushbutton
	Normal	Menu String	will set	Logic Bit		Emulates Pusht
	Normal	Menu String Menu String	will set will set	Logic Bit 225NKEY Logic Bit 225CKEY		Emulates Pushbutton 🔽 Emulates Pushbutton 🔽
Menu String	  Normal  Centre	Menu String Menu String Menu String	will set will set	Logic Bit 225NKEY Logic Bit 225CKEY Logic Bit	TRUE	Emulates Pushbutton 🔽 Emulates Pushbutton 🔽

Figure 13 Example of the logic associated with the Points Key Control menu

When clicking on the Points Key arrow, a menu will appear with 3 options, to set the Points "key" normal, centre or reverse. Selecting either option will send that control bit to the interlocking. The bit value is "pulsed" true, due to the "Emulates Pushbutton" field being selected.

The bit in the Logic Bit field is an intermediate bit, which is defined in the Control Panel Bit List file (Control Panel.CSV). The configuration logic associated with this bit is found in another Bit List file, which is created for the control panel indications and controls serial link. In this example the Bit List file is named ATRICS as it defines the I/O bits between the Microlok interlocking and ATRICS.

Direction	Bit Name	Bit Offset	Bit Value	AutoConfigBit	On Delay	Off Delay
OUT	225NR		0	225NKEY+~225RKEY*~22 5CKEY*225NR	0	0
OUT	225RR		0	225RKEY+~225NKEY*~22 5CKEY*225RR	0	0
OUT	225CZ		1	225CKEY+~225NKEY*~22 5RKEY*225CZ	0	0

An example of this configuration logic is as shown in Table 7.

Table 7 Configuration Logic

# 2.5.3.7 OCS Route Control Functions

Signal route controls are sent to the interlocking via a drop-down menu, which will provide an option to select the route to be set or an option to cancel the route set for that signal. When clicking on the signal repeater symbol the route selection menu will be displayed. When the route is set the associated route lights will be indicated on the Control Panel.



An example of the logic associated with the Route command menu is as in Figure 14.



#### Figure 14 Example of the logic associated with the Route command menu

Depending on the menu item selected, that particular control bit will be sent to the interlocking. The control bits, including the signal cancel bit are "pulsed" to momentarily set the control bit "true".

#### 2.5.3.8 NX Route Control Functions

Push button controls for setting signal routes are sent to the panel processor via a dropdown menu, which provides an option to the push button to set a main or shunt route, or to pull the button to cancel the route that has been set for that signal. The symbol on the button indicates the available functions that may be selected. When clicking a push button symbol, the button selection drop-down menu is displayed. When a button has been selected as a commence action, the outline of the button on the screen flashes white until a finish button for a valid route from the button is selected. The outline of the commence button changes to steady white when the correct track and locking conditions are true and the normal lock relay de-engerised.

If the finish button operation is not successful, the flashing outline of the commence button is extinguished.



The following figure shows an example of a push button layout on a NX route panel.

Figure 15 Example of a push button layout on a NX route panel

The colour of the symbols on the buttons configured for Commence and Finish functions are shown with the following colours when set to 'true'.

- Yellow for Down Main direction routes
- Blue for Up Main routes
- Red for shunt routes

### 2.5.3.9 Signal Indications

A Signal repeater is provided for each controlled signal on the Control Panel. The signal repeater will indicate red or green depending on the value of the indication bits received from the interlocking. The signal repeater may flash red (ALSR function) or flash green (LPR function), where required.



Note that a signal should show grey when no indication is received.

#### 2.5.3.10 Automatic Re-clearing

An "A" button is provided adjacent to the signal repeaters for the control an indication where the Auto Re-clearing function is required. Clicking on this "A" button will result in a drop-down menu being displayed, giving the option to set or cancel the Auto Re-clearing function. When a signal/route is set in the Auto Re-clearing mode a white "A" will be displayed in the centre of the button.

Examples of the logic associated with the Auto Re-clear indications and selection menu are as shown in Figure 16 and Figure 17.

ubstitute Bitmap	Substitute Color	Delete	OK	Cancel	~~	>>>
Grie	dMap		Bitmap			
	2	Displays	O in	as Default		

# Figure 16 Example of logic associated with the Auto Re-clear Indications and selection menu

Add Menu	Delete Menu	Ok	Cancel		
Gridmap					
275					
	Menu String		Logic Bit		
	Menu String RECLEAR	will set	Logic Bit	TRUE	Emulates Pushbutton
SET AUTO	Menu String RECLEAR Menu String	will set	Logic Bit  61ARR Logic Bit	TRUE 🚟	Emulates Pushbutton

Figure 17 Example of logic associated with the Auto Re-clear Indications and selection menu

### 2.5.3.11 Track Indications

Track indications are provided for each track circuit on the Control Panel. These indications include a red indication for track occupied, a grey indication for track unoccupied, a green indication for main route set and a yellow indication for shunt route set.



Figure 18 Track Indications

The indications for the tracks over Points do not flash with loss of point detection.

An example of the logic associated with the Track Circuit Indications is as follows:

Intermediate bits are required where track route lights are to be provided. These intermediate bits are defined in the Control Panel Bit List file. The intermediate bit names shall follow the typical NX panel circuits, as shall be the logic associated with these bits.

An example of the logic associated with the Track route light indications is in Table 8

Direction	Bit Name	Bit Off set	Bit Value	AutoConfigBit	On Delay	Off Delay
-----------	----------	-------------------	--------------	---------------	-------------	--------------

OUT	96MAUR	0	(~96MA_NLRK+~9 6ATK*96MAUR)	0	0
OUT	96SAUR	0	(~96SA_NLRK+~96 ATK*96SAUR)	0	0
OUT	96MAU2R	0	(96MAUR+~96BTK *96MAU2R)	0	0
OUT	96SAU2R	0	(96SAUR+~96BTK* 96SAU2R)	0	0
OUT	96MAU3R	0	(96MAU2R+~96CT K*96MAU3R)	0	0
OUT	96SAU3R	0	(96SAU2R+~96CT K*96SAU3R)	0	0
OUT	91ATUR	0	(91MBUR+91SBUR +94SBU2R+94MB U2R+91AT)	0	0

#### Table 8

### 2.5.3.12 Track Timer Indications

Track Timer lights are provided in the vicinity of the associated track circuit. This indication displays a red light when the relevant timing function bit is set.

An example of the logic associated with the Track Timer Indication is as shown in Figure 19.

ubstitute Bitmap	Substitute Color	Delete	OK	Cancel		>>	
Grid	IM ap	E Displays	3itmap • in	Color	fault		
Substitute	map Lo	gic Element	is set	Colo Substitute	r Log When 55BT_JR	ic Element	is set

Figure 19 Track Timer Indication

#### 2.5.3.13 Miscellaneous Indications and Controls

Miscellaneous indications and controls may be provided on the Control Panel as required.

Particular consideration will need to be given to the interfaces of the interlocking boundaries and to how these interfaces are to be tested or simulated.

Miscellaneous indications such as Power Supplies, Lamp Failure or Hot Standby indications may be required on the Control Panel for testing purposes. All miscellaneous indication bits however may also be tested using the I/O Display Screen as discussed further in the document.

# 2.5.4 I/O Display Screen

When MISS is running, sub-windows associated with each Bit List file are available to be opened and interrogated during testing. These windows display the status of all the input

bits and output bits defined within that Bit List file. The bit value will be displayed as blue for true (1) and red for false (0).

It is possible to manually alter (transmit command) the status of the bits in the output list or reset (reset command) these bits to the original logic state.

It is recommended that these windows are used for the through testing of non vital or miscellaneous bits that may not be indicated on the Track or Control panel. For example the bit status in the slave location Bit List file can be transmitted (change of state) and the corresponding bit in the ATRICS Bit List file can be confirmed to that change of state.

Testing in this manner will reduce the need to provide numerous non-vital or miscellaneous indications on the Track or Control Panel that would only be required to be tested the once.

An example of an I/O Display screen is as shown in Figure 20

💻 SP1 1/O Displa	ıy				
0/P BITS TO INT			I/P BITS FROM IN	IT	
1HP	420AT	SP	1HR	SPARE	
1HDP	12DT	SP	1HDR	SPARE	
1DP	1AT	SP	1DR	SPARE	
1NGPZ	1BT	SP	1VB	SPARE	
1VNP	SP1_120VPOP	SP	1VCSR		
1VRP	SP1_A_DLC	SP	416ALZR		
420HZ	SP1_A_MAIN	SP	SPARE		
420HDZ	SP1_A_DIV	SP	SPARE		
1ALSZ	SP1_B_DLC	401	SPARE		
1_3ALSZ	SP1_B_MAIN	405	SPARE		
407FT	SP1_B_DIV	41:	SPARE		
<		>	SPARE		

Figure 20 I/O Display Screen

# 3 MICROLOK II APPLICATION DATA

#### 3.1 General

The Microlok II development system tools are to be used to develop and compile an application logic program, debug the program, and upload the application program to the Microlok II central processing unit (CPU) card.

For the comprehensive procedures to create the complete Microlok II application program, reference should be made to the US&S Microlok II System Application Logic Programming Guide. SM-6800D manual.

The application logic is to be designed in accordance with the Signal Design Quality Procedures;

QSDP16: Microlok File Control, Microlok Data Design and Factory Acceptance Testing,

QSDP31: Retesting of Microlok Data,

QSDP33: Checking of Microlok Circuits and Data Designs.

As the MISS cubicle does not include the facility to install the final Microlok cardfile configuration, the application data is required to be modified accordingly.

The application data is to be modified with minimal change, allowing the application data to be simulated as closely as possible to the final configuration. To achieve this the Interface section of the application data is only to be modified.

The Design Engineer preparing the application data shall establish the proposed method of testing the application data prior to the commencement of the initial data design. Where the MISS is to be utilised for testing the data the initial design is to include the provisions for MISS testing as explained in the following section.

# 3.2 Application Data Modifications for MISS

# 3.2.1 Initial Design

The interface section of the Microlok II application data includes two sub-sections, LOCAL and COMM.

The LOCAL sub-section specifies the interface I/O boards installed in the Microlok cardfile and defines the individual data bits associated with each board.

The COMM sub-section specifies the interface serial communication links to be defined, including the individual data bits associated with the inputs and outputs of each serial link.

As the MISS does not include a facility to test the physical I/O boards, the LOCAL subsection is to be designed as per the final configuration and then modified to suit the MISS configuration by temporarily commenting out the relevant sections.

The I/O defined in the LOCAL section is then to be duplicated in the COMM section including the same bit names. A spare serial port is to be utilised for this purpose.

An example of the application data alterations designed for MISS can be found in the appendix.

# 3.2.2 Pre-commissioning

Following the testing of the application data the data is to be modified for the commissioning.

In an effort to reduce the amount of modifications to the application data, and in order to retain the simulation data for any possible future testing, the simulation data is not to be deleted.

In the commissioning version of application data, the previously commented out data in the LOCAL sub-section of the data is to be instated. The simulation data provided for the serial link in the COMM sub-section is then to be commented out.

The application data is then to be checked as per the relevant procedures prior to the commissioning.

# 4 **TESTING PROCEDURES**

# 4.1 Introduction

The MISS allows for the simulation and testing of the Microlok II application data. This process is to check the integrity and to evaluate the performance of the interlocking logic.

Additional testing will be required prior to or during the signal commissioning to prove a complete through test and correct operation of the field equipment, and the control of this equipment from the Control System, including all interfaces to the interlocking.

A separate desk top computer running the Microlok II tools software is available to be used during testing if there is a requirement to interrogate the bit status of any boolean bit or serial data bit within the application logic of any Microlok II CPU card. Additional computers may be provided if there is a requirement to interrogate more than one CPU card at any time.

The MISS I/O Display Screen may be referred to if there is a requirement to interrogate the status of any MISS bit as defined in the Bit List files. Refer to section 2.5.5 for further information related to the I/O Display Screen.

The MISS log file may also be referred to during testing if required. Refer to section 5.4 for further information related to the MISS logging.

Reference shall be made to the FAT Plan that is produced for the project to confirm the specific tests to be carried out.

Prior to the commencement of the testing the Design Engineer is to carry out the set to work process to ensure the correct configuration and settings required for simulation.

Following the set to work check the through testing and design integrity testing shall be carried out.

# 4.2 Set to Work

The set to work shall be carried out by the Design Engineer and include the following tests:

- All CPU cards are loaded with the correct executive version and correct version of application data.
- All serial links are functioning as required and as per the configuration drawing.
- All routes correctly set and indicated, with signals clearing for each route.
- All signals correctly cancel and automatically normalise if required.
- All points can be operated normal, reverse and free and are correctly indicated and detected normal and reverse.
- The signal Auto Re-clearing controls and indication function correctly where provided.
- The correct route lights and track occupied indications are displayed when a train is simulated through each route.
- Miscellaneous testing of various unique or unusual interlocking functions or features, for example; points sequencing, level crossing and warning light operation.

The set to work tests need not be comprehensive and shall not be considered proof of the integrity of the interlocking.

# 4.3 Through Testing

The through testing shall be carried out to ensure individual functions are correctly passed through the serial links and the application data.

The through testing shall include the following:

• Correspond all controls from the Control System serial link that are inputs into the signal interlocking to the relevant function.

- Correspond all outputs from the signal interlocking to the field equipment.
- Correspond all inputs from the field equipment to the relevant functions within the signal interlocking or to the Control System serial link.

Generally this testing is carried out by the Design Engineer and the tests are recorded in the FAT document for that project.

Design Integrity Testing to Control Tables

The design integrity testing shall be carried out in accordance with the Inspection and Testing of New and Altered Signalling Works, Inspection and testing procedures. (SPG 0711.4)

An accredited Engineer that is independent to the interlocking design process shall carry out this testing.

The testing shall be performed using the approved Signalling Plan, Control Tables, Circuit Books and other documentation deemed necessary to complete the work. Particular attention shall be made to the signalling interfaces to ensure the required input and output functionality has been provided and tested.

The Test Engineer shall liaise with the Design Engineer prior to commencement of testing to ensure familiarisation with the testing configuration provided and the systems in place for diagnostic support.

Where the MISS design allows, the design integrity testing may include the aspect sequence testing. This testing may not remove the requirement to complete a formal aspect sequence test on site.

Any testing that cannot be carried out utilising MISS shall be carried out during the signal commissioning. The testing Engineer shall ensure these tests are incorporated into the commissioning test plan.

# 5 RUNNING MISS

# 5.1 Folder Structure

The files created for a MISS project are to be provided in a certain structure both for consistency and correct operation of MISS.

This folder structure to be followed on the MISS computer is as follows:

- My Computer
- Local Disk (C:)
  - MISS (folder) contains a folder for each MISS project
    - Project/Location Name (folder) contains the following files and 2 folders
      - Control Panel.mdb
      - Track Panel.mdb
      - Misscom.mdb
        - □ Microlok Data (folder) contains all Microlok data
        - $\hfill\square$  Location Name (folder) contains the following files
          - Bit List.csv
          - Port Info.csv

- ➢ ePatch.csv
- Date.log (Automatically created by MISS)
- Date.alm (Automatically created by MISS)

# 5.2 Shortcut (MISS.exe)

#### Error! Objects cannot be created from editing field codes.

A shortcut is generally provided on the desktop of the MISS computer to run the MISS software for a particular project.

With the project being provided with a relevant name and folders having been created for that project, an existing shortcut on the desktop can be copied and modified as required.

The shortcut would then be required to be name changed and the 2 fields "Target" and "Start in:" will also need to be modified.

The full "Target" description is C:\Program Files\Union Switch & Signal Pty Ltd\Microlok Interlocking Simulation System\Miss.exe" Project Name

The "Start in" description is C:\MISS\Project Name\

# 5.3 Alarms

An alarm file is automatically created to record the alarms generated while MISS is running. This file can be referred to during the initial set up of the project, this information helps to identify errors or aids fault finding during the design process.

The Alarms file name includes the date that the file created, and a new file is created for the new day to record any alarms raised during that day.

cut Compatibility	
itevetown	
Application	are
n: Microlok Interlocking Simulation System	
king Simulation System\Miss.exe'' STEVETOWN	MISS
C:\MISS\STEVETOWN\	an
None	
Normal window	
	wa
d Target Change Icon Advanced	
d Target Change Icon Advanced	
	Compatibility       Stevetown       Application       n: Microlok Interlocking Simulation System       king Simulation System\Miss.exe'' STEVETOWN       C:\MISS\STEVETOWN\       None       Normal window       I       d Target     Change Icon

# 5.4 Logging

A log file is automatically

created when MISS is running. This file can be referred to during the simulation testing to view the change of status of the data bits within the Bit List files.

The MISS log may be accessed during testing by selecting the Data Log View from the Tools menu. The log file includes the bit name, the status of the bit and the time of the status change.

The file name includes the date that the file was created, and a new file is created for each new day that MISS is running.

# 6 APPENDIX

# 6.1 Appendix A – Application Data Modified for MISS

MICROLOK\_II PROGRAM SP1\_LOCATION;

INTERFACE

/\*=====COMMENTED OUT FOR MISS

LOCAL

//=======LOCAL IO

BOARD: OUT\_SLOT1 ADJUSTABLE ENABLE: 1 TYPE: OUT16 OUTPUT:

1HR,	1HDR,	1DR,	1VR,
1VCSR,	416ALZR,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE;

//------

BOARD: IN\_SLOT2 ADJUSTABLE ENABLE: 1 TYPE: IN16 INPUT:

1HP,	1HDP,	1DP,	1NGPZ,
1VNP,	1VRP,	420HZ,	420HDZ,
1ALSZ,	1_3ALSZ,	407FT,	420AT,
12DT,	1AT,	1BT,	120VPOP;

//-----LOCAL\_IO

BOARD:NVIN32\_SLOT3ADJUSTABLE ENABLE:1TYPE:NV.IN32NV.INPUT:1

A_DLC,	A_MAIN,	A_DIV,	B_DLC,
B_MAIN,	B_DIV,	DIAG_DLC,	DIAG_MAIN,
DIAG_DIV,	12V_PSU1,	12V_PSU2,	50V_PSU1,
50V_PSU2,	120V_ELD,	401ABTK,	405AT.371R_407ABCDTK,
412AT_416ATK,	420BTK,	420_NGK,	420_RGK,
G18.5ABCTK,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE;

======END OF COMMENTED OUT FOR MISS==\*/

COMM

//----- NEW DATA PROVIDED FOR MISS

// TEMPORARY SERIAL DATA FOR MISS COMMUNICATIONS LINK - PORT 2

LINK:	COMM2
ADJUSTABLE ENABLE:	1
PROTOCOL:	MICROLOK.MASTER
FIXED PORT:	2;
ADJUSTABLE POINT.POINT:	1;
ADJUSTABLE BAUD:	19200;
FIXED STOPBITS:	1;
FIXED PARITY:	NONE;
FIXED KEY.ON.DELAY:	12;
FIXED KEY.OFF.DELAY:	12;
ADJUSTABLE MASTER.TIMEOUT:	100:MSEC;
ADJUSTABLE POLLING.INTERVAL:	50:MSEC;
ADJUSTABLE STALE.DATA.TIMEOUT:	4:SEC;
ADDRESS:	33
ADJUSTABLE ENABLE:	1

OUTPUT: //=====PORT 2 OUTPUTS

1HR,	1HDR,	1DR,	1VR,
1VCSR,	416ALZR,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE;

INPUT: //====PORT 2 INPUTS

1HP,	1HDP,	1DP,	1NGPZ,
1VNP,	1VRP,	420HZ,	420HDZ,
1ALSZ,	1_3ALSZ,	407FT,	420AT,
12DT,	1AT,	1BT,	120VPOP,
A_DLC,	A_MAIN,	A_DIV,	B_DLC,
B_MAIN,	B_DIV,	DIAG_DLC,	DIAG_MAIN,
DIAG_DIV,	12V_PSU1,	12V_PSU2,	50V_PSU1,
50V_PSU2,	120V_ELD,	401ABTK,	405AT.371R_407ABCDTK,
412AT_416ATK,	420BTK,	420_NGK,	420_RGK,
G18.5ABCTK,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE,
SPARE,	SPARE,	SPARE,	SPARE;

//====END NEW DATA PROVIDED FOR MISS

NOTE: In the log section of the Microlok II data, where it includes the logging of the enable bit associated with each local I/O board in the cardfile, these bits will be required to be commented out due to the modifications made for MISS. This may be carried out as follows:

//-----LOG

LOG BITS

//LOCAL\_IO-----LOG

//OUT_SLOT1.ENABLED,	====COMMENTED OUT FOR MISS
//IN_SLOT2.ENABLED,	====COMMENTED OUT FOR MISS
//NVIN32_SLOT4.ENABLED,	====COMMENTED OUT FOR MISS



# 6.2 Appendix B – MISS Configuration Example

# 6.3 Appendix C – MISS Circuits



